VNH9045AQ

Datasheet

Automotive fully integrated H-bridge motor driver

QFN 6x6 triple pad 26+2L

Product status link
VNH9045AQ

Product summary	
Order code	VNH9045AQTR
Marking	VNH9045AQ
Package	QFN 6x6 triple pad 26+2L
Packing	Tape and reel

Features

Type	$R_{DS(on)}$ typ.	I_{OUT}	V_{CC} max.
VNH9045AQ	45 mΩ (per leg)	23 A	36 V

- AEC-Q100 qualified
- ISO 26262 ready
- 3 V CMOS compatible inputs
- Undervoltage shutdown
- Overvoltage clamp
- Thermal shutdown
- Cross-conduction protection
- Current and power limitation
- Very low standby power consumption
- Protection against loss of ground and loss of V_{CC}
- PWM operation up to 25 kHz
- Multisense monitoring functions
  - Analog motor current feedback
  - Chip temperature monitoring
- Multisense diagnostic functions
  - Output short to ground detection
  - Thermal shutdown indication
  - OFF-state open-load detection
  - High-side power limitation indication
  - Low-side overcurrent shutdown indication
  - Output short to V_{CC} detection
- Output protected against short to ground and short to V_{CC}
- Standby mode
- Half bridge operation

Application

- Motor control automotive applications supplied by 12 V board-net

Description

The VNH9045AQ is a full bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side driver and two low-side switches. All switches are designed using STMicroelectronics well known and proven proprietary VIPower technology that allows to efficiently integrate on the same die a true Power MOSFET with an intelligent signal/protection circuitry. The three dices are assembled in a QFN 6x6 triple pad 26+2L package equipped with three exposed islands for optimized dissipation performances. This package is specifically designed for the harsh automotive environment and offers improved thermal performance thanks to exposed die pads. The input signals INA and INB can directly interface the microcontroller to select the motor direction and the brake to V_{CC} condition. Two selection pins (SEL0 and SEL1) to address the information are available on the multisense to the microcontroller. The multisense pin allows monitoring the motor current by delivering a current proportional to the motor current value and provides the diagnostic feedback and Case temperature according to the implemented truth table. The PH_OUT pin provides feedback on the OUTA and OUTB state for safety-relevant functions. The PWM, up to 25 kHz, allows controlling the speed of the motor in all possible conditions or selecting the brake to GND condition. In all cases, a low-level state on the PWM pin turns off both the LSA and LSB switches.

1 Block diagram and pin description

Figure 1. Block diagram

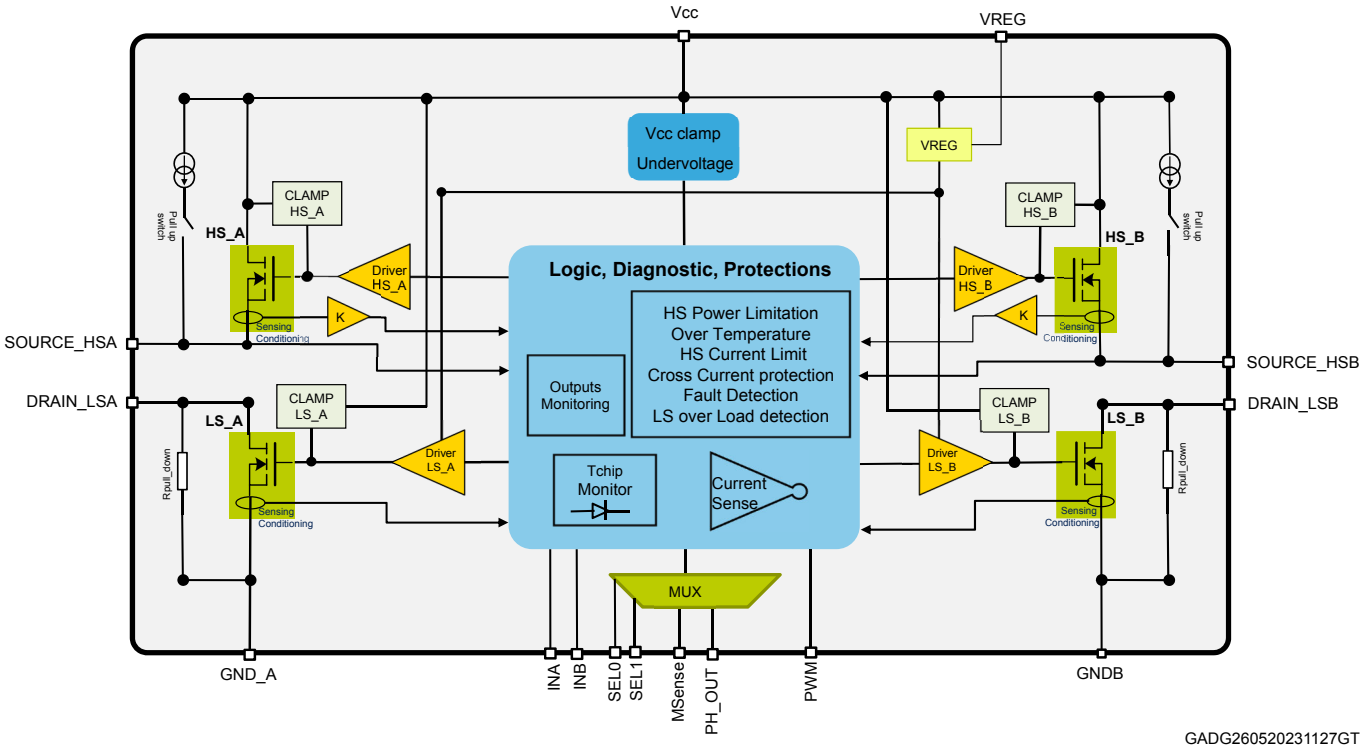

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Table 1. Block description

Name	Description
Logic control	Allows the turn-on and the turn-off of the high-side and the low-side switches according to the Truth table: operative condition and diagnostic.
Undervoltage	Shuts down the device for battery voltage below (4 V).
High-side and low-side driver	Drives the gate of the concerned switch to allow a proper $R_{DS(on)}$ for the leg of the bridge.
High-side current limitation	Limits the motor current in case of short circuit.
High-side and low-side overtemperature protection	In case of overload that increase the junction temperature, it shuts down the concerned driver to prevent degradation and to protect the die.
Low-side overcurrent detector	Detects when low-side current exceeds shutdown current and latches off the concerned low side.
Fault detection	Signalizes an abnormal condition of the switch (output shorted to ground or output shorted to battery) by feedback on the multisense.
High-side power limitation	Limits the power dissipation of the high-side driver inside safe range in case of short to ground condition.
Tchip warning	Provides a warning signal of the chip temperature by feedback on the multisense.
VREG	Internal voltage regulator that provides the supply for the gates of the low-side switches.
Output monitoring	Provides feedback of OUTA and OUTB state in ON state and OFF state.

Figure 2. Configuration diagram (bottom view)

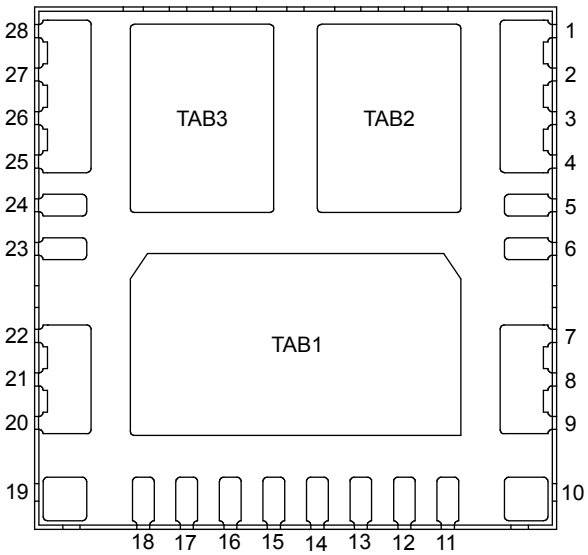

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Table 2. Pin definition and function

Pin	Symbol	Function
1, 2, 3, 4	GNDB	Source of low-side switch B.
5, 6, TAB2	DRAIN_LSB	Drain of low-side switch B.
7, 8, 9	SOURCE_HSB	Source of high-side switch B.
10, 19, TAB1	VCC	Power supply voltage.
11	INB	Counterclockwise input.
12	PH_OUT	Output of phase OUT diagnostic feedback.
13	SEL1	Address the multisense multiplexer.
14	SEL0	Address the multisense multiplexer.
15	MSense	Output of current sense and diagnostic feedback.
16	PWM	PWM input. Voltage controlled input pin with hysteresis, CMOS compatible. Gates of low-side Power MOSFETs. Active high.
17	VREG	Internal voltage regulator that provides the supply for the gates of the internal low-side switches.
18	INA	Clockwise input.
20, 21, 22	SOURCE_HSA	Source of high-side switch A.
23, 24, TAB3	DRAIN_LSA	Drain of low-side switch A.
25, 26, 27, 28	GNDA	Source of low-side switch A.

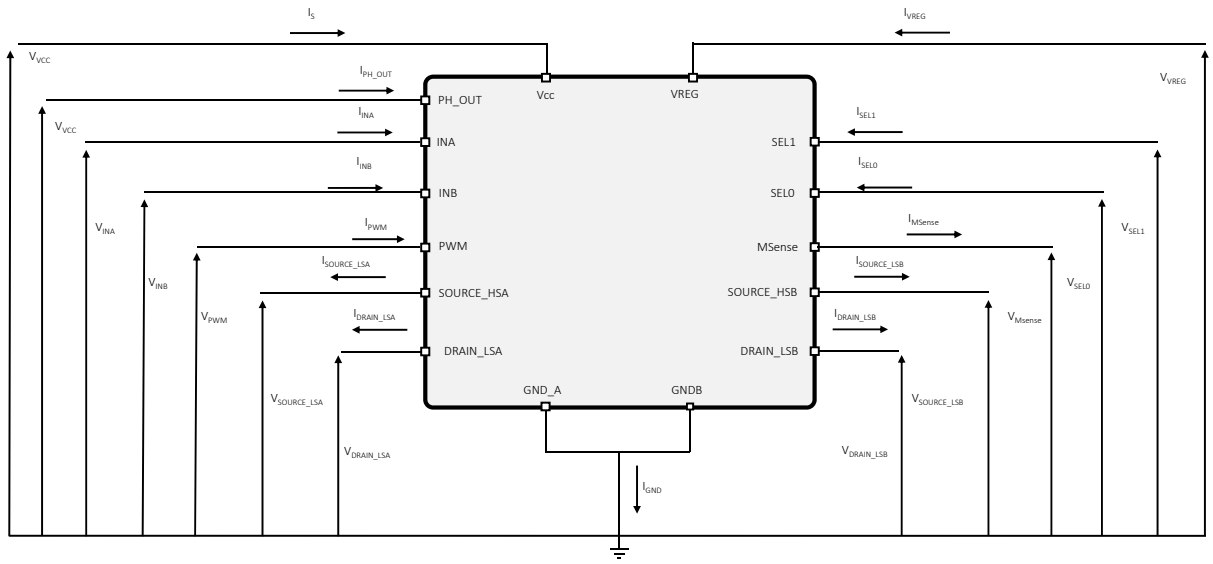
Table 3. Suggested connection for unused pin

Connection/ pin	MultiSense	NC	SOURCE_HSx	DRAIN_LSx	INx, PWM, SELx	VREG	PH_OUT
Floating	Not allowed	X(1)	X(1)	X(1)	X(1)	Not allowed	X(1)
To ground	Through 1 kΩ resistor	X(1)	Not allowed	X(1)	Through 15 kΩ resistor	Through 220 Ω resistor + 100 nF capacitor	X(1)

1. *X: do not care.*

2 Electrical specifications

Figure 3. **Current convention**



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2.1 Absolute maximum ratings

All voltages are referred to GND.

Table 4. **Absolute maximum ratings**

Ref	Symbol	Parameter	Value	Unit
1.1	V_{CC}	Supply voltage	-0.3 to 36	V
1.2	Imax.	DC output current (continuous)	Internally limited	A
1.3	DRAIN_LSA, DRAIN_LSB, SOURCE_HSA, SOURCE_HSB	OUT clamp voltage	-0.3 to V_{CC}	V
1.4	I_R	Reverse output current (continuous)(1)	-9	A
1.5	IN_A, IN_B, SEL0, SEL1, PWM	Input current	-1 to 10	mA
1.6	PH_OUT	Phase out pin	7	V
1.7	MSense	DC output current (V_{GND} = V_{CC} and V_{MSense} < 0 V)	10	mA
		DC output current in reverse (V_{CC} < 0 V)	-20	mA
		DC output operating voltage (continuous)	4	V
1.8	VREG	Internal low side pre-driver regulator	-0.3 to 8.2	V
1.9	T_J	Operating junction temperature range	-40 to 150	°C
1.10	T_{stg}	Storage temperature range	-55 to 150	°C

1. *Based on the internal wires capability.*

2.2 ESD protections

Table 5. ESD protections

Symbol unit	Parameter	Value	Unit
Electrostatic discharge (Human body model: R = 1.5 kΩ; C = 100 pF)	INA, INB, PWM, Multisense, SEL0, SEL1, VREG, PH_OUT	2	kV
	V_{CC}, DRAIN_LSA, DRAIN_LSB, SOURCE_HSA, SOURCE_HSB	4	

2.3 Thermal data

Table 6. Thermal data

Symbol	Parameter	Max. value	Unit
R_{thJB}	Thermal resistance, junction-to-board (measured on 6L PCB)	8.3	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	See Table 17	°C/W

2.4 Electrical characteristics

Table 7. Supply and supply monitoring

Ref.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SOURCE_HSA shorted to DRAIN_LSA = OUTA, SOURCE_HSB shorted to DRAIN_LSB = OUTB, V_{CC} = 7 V up to 28 V, -40 °C < T_J < 150 °C, unless otherwise specified							
2.1	V_{CC}	Operating supply voltage		4		28	V
2.2	I_S	Supply current	Standby: INA = INB = PWM = 0, SEL0,1 = 0, T_J = 25 °C, V_{CC} = 13 V			1	µA
2.3			Standby: INA = INB = PWM = 0, SEL0,1 = 0, T_J = 125 °C, V_{CC} = 13 V			3	µA
2.4			Off-state (no standby): INA = INB = PWM = 0, V_{CC} = 13 V, SEL0 = SEL1 = 5 V, T_J = 125 °C			3	mA
2.5			On-state: INA or INB = 5 V , PWM = 5 V, no load V_{CC} = 13 V			3	mA
2.6	t_{D_STBY}	Standby mode blanking time	V_{CC} = 13 V, INA = INB = PWM = 0 V, SEL1 or SEL0 from 0 V to 5 V		300	500	µs
2.7	R_{ONHS}	Static high-side resistance	I_{OUTx} = 4 A, T_J = 25 °C		25		mΩ
2.8			I_{OUTx} = 4 A, T_J = - 40 °C to 150 °C			60	
2.9			V_{CC} = 4 V, I_{OUTx} = 4 A, T_J = 25 °C		28		
2.10	R_{ONLS}	Static low-side resistance	I_{OUTx} = 4 A, V_{CC} ≥ 10 V, T_J = 25 °C		20		mΩ

Ref.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
2.11	R_{ONLS}	Static low-side resistance	I_{OUTx} = 4 A, V_{CC} ≥ 10 V, T_J = - 40 °C to 150 °C			40	mΩ
2.12			V_{CC} = 4 V, I_{OUTx} = 4 A, T_J = 25 °C		30		
2.13	V_f	High-side free-wheeling diode forward voltage	I_{OUTx} = -4 A, T_J = 150 °C			0.7	V
2.14	$I_{L(off)}$	Standby output current of one leg	T_J = 25 °C, V_{CC} = 13 V, SEL0 = SEL1 = 0 INA = INB = PWM = 0, V_{OUTx} = 0			1	µA
2.15			T_J = 125 °C, V_{CC} = 13V, SEL0 = SEL1 = 0, INA = INB = PWM = 0, V_{OUTx} = 0			3	µA

Table 8. Logic inputs (INA, INB, PWM, SEL0, SEL1)

Ref.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SOURCE_HSA shorted to DRAIN_LSA = OUTA, SOURCE_HSB shorted to DRAIN_LSB = OUTB, V_{CC} = 7 V up to 28 V, -40 °C < T_J < 150 °C, unless otherwise specified							
3.1	V_{IL}	Input low level voltage				0.9	V
3.2	V_{IH}	Input high level voltage		2.1			V
3.3	V_{IHYST}	Input hysteresis voltage		0.2			V
3.4	V_{ICL}	Input clamp voltage (except SEL1)	I_{IN} = 1 mA	6		8.5	V
3.5			I_{IN} = -1 mA		-0.7		V
3.6	I_{INH}	Input current	V_{IN} = 2.1 V			10	µA
3.7	I_{INL}	Input current	V_{IN} = 0.9 V	1			µA
SEL1 (V_{CC} = 7 V up to 18 V), -40 °C < T_J < 150 °C							
3.8	V_{SELCL}	Input clamp voltage SEL1	I_{SEL} = 1 mA	9		12	V
3.9			I_{SEL} = -1 mA		-0.7		

Table 9. Logic outputs (PH_OUT) open drain output

Ref.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SOURCE_HSA shorted to DRAIN_LSA = OUTA, SOURCE_HSB shorted to DRAIN_LSB = OUTB, V_{CC} = 7 V up to 18 V, -40 °C < T_J < 150 °C, R_{Pup} = 10 kΩ, unless otherwise specified							
4.1	V_{OL_PH}	Output low level voltage	R_{Pup} = 10 kΩ			0.4	V
4.2	t_{DELAYr}	Phase out delay time on rising OUT	From 90% of OUTx to 90% of PH_OUT INA = INB= PWM = 0V, Voutx = 4V, SEL0 = High , SEL1=Low (Sel0 = Low, SEL1 = High) (see Figure 12)			1.5	µs
4.3	t_{DELAYf}	Phase out delay time on falling OUT	From 10% of OUTx to 10% of PH_OUT (see Figure 12)			1.5	µs
4.4	t_{DELAY2}	Phase out delay time from SELx to OUTPUT	SEL_0 = from 0 to 1 or from 1 to 0, up to 90% or 10% respectively (see Figure 13)			1.5	µs

Table 10. Switching

Ref.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SOURCE_HSA shorted to DRAIN_LSA = OUTA, SOURCE_HSB shorted to DRAIN_LSB = OUTB, V_{CC} = 13 V, R_{LOAD} = 3.25 Ω, -40 °C < T_J < 150 °C, unless otherwise specified							
5.1	f	PWM frequency				25	kHz
5.2	t_{on}	Turn-on time	PWM = 0 V, SELx = 5 V (no standby), INx from 0 to 5 V, V_{OUTx} to 90% of V_{CC} (see Figure 7)		57	110	µs
5.3	t_{off}	Turn-off time	PWM = 0 V, SELx = 5 V (no standby), INx from 5 V to 0 V, V_{OUTx} to 10% of V_{CC} (see Figure 7)		38	60	µs
5.4	t_r	Rise time	INx = SELx = 5 V (no standby), PWM from 5V to 0V, V_{OUTx} from 10% to 80%			0.8	µs
5.5	t_f	Fall time	INx = SELx = 5 V (no standby), PWM from 0V to 5V, V_{OUTx} from 90% to 20%			0.9	µs
5.6	t_{cross}	Low-side turn-on delay time	(see Figure 8)	40		300	µs

Table 11. Protections and diagnostics

Ref.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SOURCE_HSA shorted to DRAIN_LSA = OUTA, SOURCE_HSB shorted to DRAIN_LSB = OUTB, 7 V < V_{CC} < 18 V, -40 °C < T_J < 150 °C unless otherwise specified							
6.1	V_{USD}	Undervoltage shutdown	V_{CC} falling			4	V
6.2	$V_{USDreset}$	Undervoltage shutdown	V_{CC} rising			5	V
6.3	$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.3		V
6.4	I_{LIM_HSD}	High-side current limitation	V_{CC} = 13 V	23		46	A
6.5			4 V < V_{CC} < 18 V			46	A
6.6	I_{SD_LSD}	Shutdown LS current		28		56	A
6.7	t_{SD_LSD}	Low-side shutdown time	INA = INB = 0, PWM = 5 V, I_{OUT} = I_{SD_LSD} (see Figure 9)		2		µs
6.8	V_{CL_HSD}	High-side clamp voltage (V_{CC} to V_{OUTx} = 0 V)	I_{OUT} = 100 mA, t_{clamp} = 1 ms, I_{clamp} = 100 mA	36	38	45	V
6.9	V_{CL_LSD}	Low-side clamp voltage (V_{OUTx} = V_{CC} to GND)	I_{OUT} = 100 mA, t_{clamp} = 1 ms, I_{clamp} = 100 mA	36	38	45	V
6.10	V_{CL}	Total clamp voltage from V_{CC} to GND	I_{OUT} = 100 mA, t_{clamp} = 1 ms, I_{clamp} = 100 mA	36	38	45	V
6.11	T_{TSD}	High-side and low-side thermal shutdown temperature		150	175	200	°C
6.12	T_{TR}	Thermal reset temperature		135			°C
6.13	T_{HYST}	Thermal hysteresis (T_{TSD} - T_{TR})			7		°C
6.14	ΔT_{J_SD}	Dynamic temperature			70		°C
6.15	V_{OL}	OFF-state open-load voltage detection threshold	INA = INB = 0, PWM = 0 V_{SEL0} = 5 V, V_{SEL1} = 0 V for CHA, V_{SEL0} = 0 V, V_{SEL1} = 5 V for CHB	2	3	4	V

Ref.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
6.16	$I_{L(off2)}$	OFF-state output sink current	INA = INB = 0, V_{OUTx} = V_{OL}, PWM = 0, SEL0 = 1, SEL1 = 0 for CHA, SEL0 = 0, SEL1 = 1 for CHB	-100		-10	µA
6.17	t_{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT	INA = 5 V to 0 V, INB = 0, PWM = 0, V_{SEL0} = 5 V, V_{SEL1} = 0 V, I_{OUTA} = 0 A, V_{OUTA} = 4 V (see Figure 5)	40	160	300	µs
6.18	t_{D_VOL}	OFF-state diagnostic delay time from rising edge of V_{OUT}	INA = INB = 0, PWM = 0, V_{OUTx} = 0 V to 4 V, SEL0 = 1, SEL1 = 0 for CHA, SEL0 = 0, SEL1 = 1 for CHB (see Figure 14)		1.2	10	µs
6.19	t_{Latch_RST}	Minimum input reset time	V_{INx} = 5 V to 0 V (on HSDx fault) or V_{INx} = 0 V to 5 V (on LSDx Fault) (see Figure 10)	15			µs

Table 12. Multisense

Ref.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
SOURCE_HSA shorted to DRAIN_LSA = OUTA, SOURCE_HSB shorted to DRAIN_LSB = OUTB, 7 V < V_{CC} < 18 V, -40 °C < T_J < 150 °C							
7.1	V_{MSense_CL}	Multisense clamp voltage	SEL0 = SEL1 = 0, I_{SENSE} = -1 mA		7		V
			SEL0 = SEL1 = 0, I_{SENSE} = 1 mA	-9	-8	-7	
7.2	K_{OL}	I_{OUT}/I_{MSense}	I_{OUTx} = 0.05 A, V_{MSense} = 0.5 V	6825	10500	14175	
7.3	K_0	I_{OUT}/I_{MSense}	I_{OUTx} = 0.3 A, V_{MSense} = 0.5 V	7875	10500	13125	
7.4	K_1	I_{OUT}/I_{MSense}	I_{OUTx} = 1 A, V_{MSense} = 3.5 V	8925	10500	12075	
7.5	K_2	I_{OUT}/I_{MSense}	I_{OUTx} = 4 A, V_{MSense} = 3.5 V	9765	10500	11235	
7.6	K_3	I_{OUT}/I_{MSense}	I_{OUTx} = 7 A, V_{MSense} = 3.5 V	9765	10500	11235	
7.7	dK_{OL}/K_{OL}	Analog sense current drift	I_{OUTx} = 0.05 A, V_{MSense} = 0.5 V	-30%		30%	
7.8	dK_0/K_0	Analog sense current drift	I_{OUTx} = 0.3 A, V_{MSense} = 0.5 V	-25%		25%	
7.9	dK_1/K_1	Analog sense current drift	I_{OUTx} = 1 A, V_{MSense} = 3.5 V	-10%		10%	
7.10	dK_2/K_2	Analog sense current drift	I_{OUTx} = 4 A, V_{MSense} = 3.5 V	-6%		6%	
7.11	dK_3/K_3	Analog sense current drift	I_{OUTx} = 7 A, V_{MSense} =3.5 V	-5%		5%	
7.12	$I_{Msense0}$	Multisense leakage current	INA = INB = PWM = 0 V, SEL0 = SEL1 = 0 V, standby			0.5	µA
7.13			INA = INB = 5 V, PWM = 0 V, legX diagnostic selected, I_{OUTx} = 0 A			5	µA
7.14			PWM = 0 V, HSx OFF, legX diagnostic selected: • SEL0 = 5 V, SEL1 = 0 V, INA = 0 V, INB = 5 V, I_{OUTB} = 4 A, • SEL0 = 0 V, SEL1 = 5 V, INB = 0 V, INA = 5 V, I_{OUTA} = 4 A			5	µA

Ref.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
7.15	V_{SENSEH}	Multisense output voltage in fault condition	9 V < V_{CC} < 18 V, R_{SENSE} = 0.7 kΩ, V_{OUT} = 4 V	5		7.5	V
7.16	V_{OUT_MSD}(1)	Output voltage for Multisense shutdown	INA = SEL0 = 5V, INB = SEL1 = 0 V, R_{SENSE} = 2.7 kΩ, I_{OUTx} = 4 A		5		V
7.17	V_{SENSE_SAT}	Multisense saturation voltage	V_{CC} = 7 V, SEL0 = INA = 5 V, INB = SEL1 = 0 V, R_{SENSE} = 10 kΩ, I_{OUTA} = 7 A, T_J = -40 °C	4.8			V
7.18	I_{SENSE_SAT}(1)	Multisense saturation current	V_{CC} = 7 V, V_{MSense} = 3.5 V, SEL0 = 5V, INA = 5 V, INB = SEL1 = 0 V, T_J = 150 °C	2			mA
7.19	I_{OUT_SAT}(1)	Output saturation current	V_{CC} = 7 V, V_{MSense} = 3.5 V, INA = SEL0 = 5 V, INB = SEL1 = 0 V, T_J = 150 °C	13			A
7.20	I_{SENSEH}(1)	Multisense current in fault condition	9 V < V_{CC} < 18 V, V_{MSense} = 5 V, Multisense in fault condition	7		12	mA
		Chip temperature analog warning					
7.21	$T_{CASE\_Warning}$	Multisense = V_{SENSEH}	SEL1 = SEL0 = 5 V, Multisense = V_{SENSEH}		140		°C
		Multisense timings (multiplexer transition times), R_{SENSE} = 1 kΩ					
7.22	t_{D_AtoB}	Multisense transition delay from legA to legB	INA = INB = 5 V, PWM = 0 V, SEL0 = 5 V to 0 V, SEL1 = 0 V to 5 V, I_{OUTA} = 200 mA, I_{OUTB} = 6 A			20	µs
7.23	t_{D_BtoA}	Multisense transition delay from legB to legA	INA = INB = 5 V, PWM = 0 V, SEL0 = 0 V to 5 V, SEL1 = 5 V to 0 V, I_{OUTB} = 200 mA, I_{OUTA} = 6 A			20	µs
		Multisense timings (Current sense mode)					
7.24	$t_{DSENSE1H}$	Current sense settling time from rising edge of V_{SELx}	V_{INA} = V_{PWM} =5 V, V_{INB} = 0 V, V_{SEL0} = 0 V to 5 V, R_{SENSE} = 0.7 kΩ, R_L = 3.25 Ω, V_{SEL1} = 0 V			60	µs
7.25	$t_{DSENSE1L}$	Current sense disable time from falling edge of V_{SELx}	V_{INA} = V_{PWM} =5 V, V_{INB} = 0 V, V_{SEL0} = 5 V to 0 V, R_{SENSE} = 0.7 kΩ, R_L = 3.25 Ω, V_{SEL1} = 0 V			20	µs
7.26	$t_{DSENSE2H}$	Current sense settling time from rising edge of V_{INx}	V_{SEL0} = V_{PWM} =5 V, V_{INB} = 0 V, V_{SEL1} = 0 V, V_{INA} = 0 V to 5 V, R_{SENSE} = 0.7 kΩ, R_L = 3.25 Ω			150	µs
7.27	$t_{DSENSE2L}$	Current sense disabling time from falling edge of V_{INx}	V_{SEL0} = V_{PWM} =5 V, V_{INB} = 0 V, V_{SEL1} = 0 V, V_{INA} = 5 V to 0 V, R_{SENSE} = 0.7 kΩ, R_L = 3.25 Ω			20	µs

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

Figure 4. Current sense timings (current sense mode)

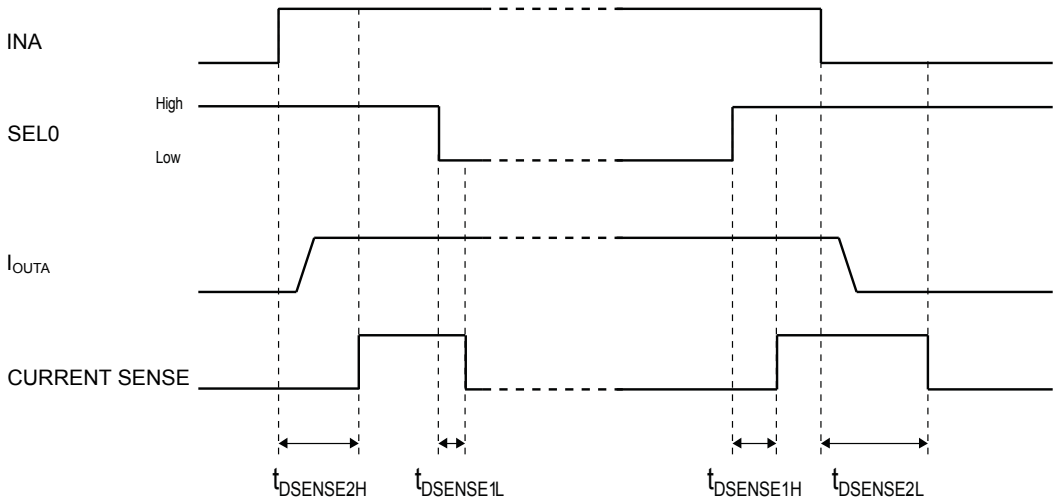

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Figure 5. t_{DSTKON}

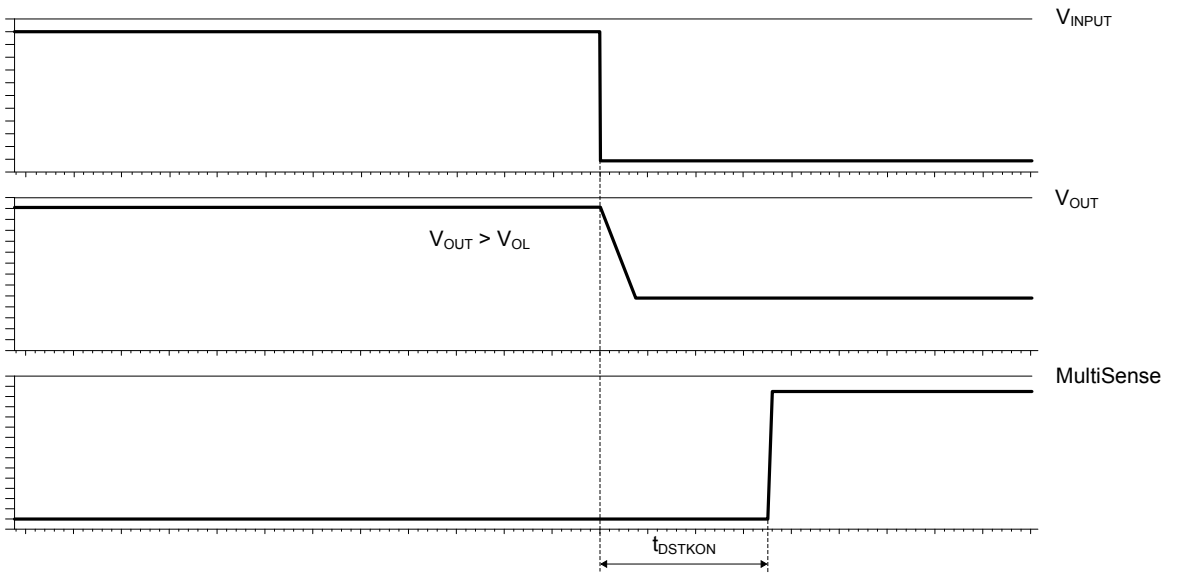

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Figure 6. **Definition of the low-side switching times**

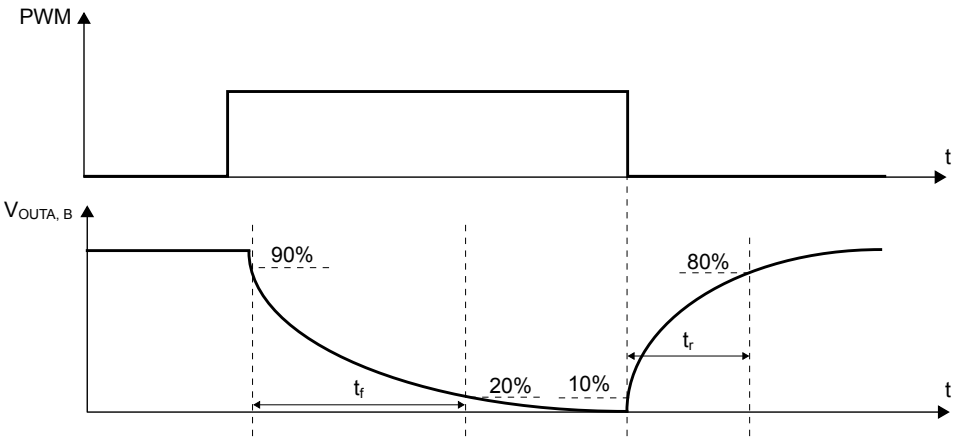

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Figure 7. **Definition of the high-side switching times**

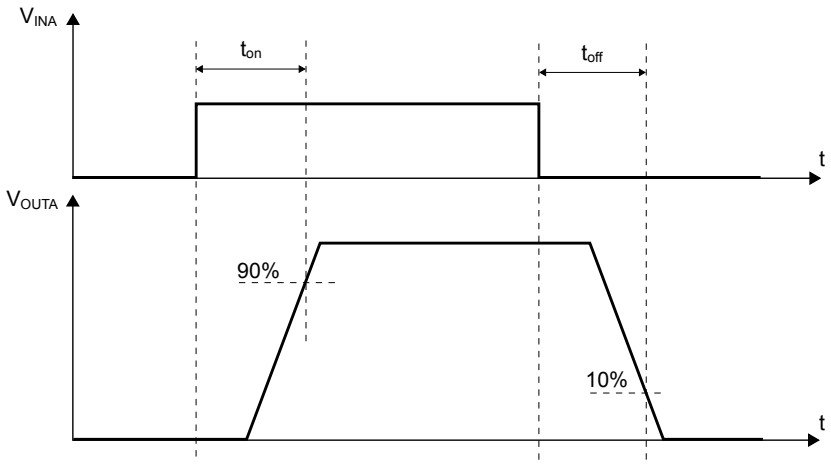

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Figure 8. **Low-side turn-on delay time**

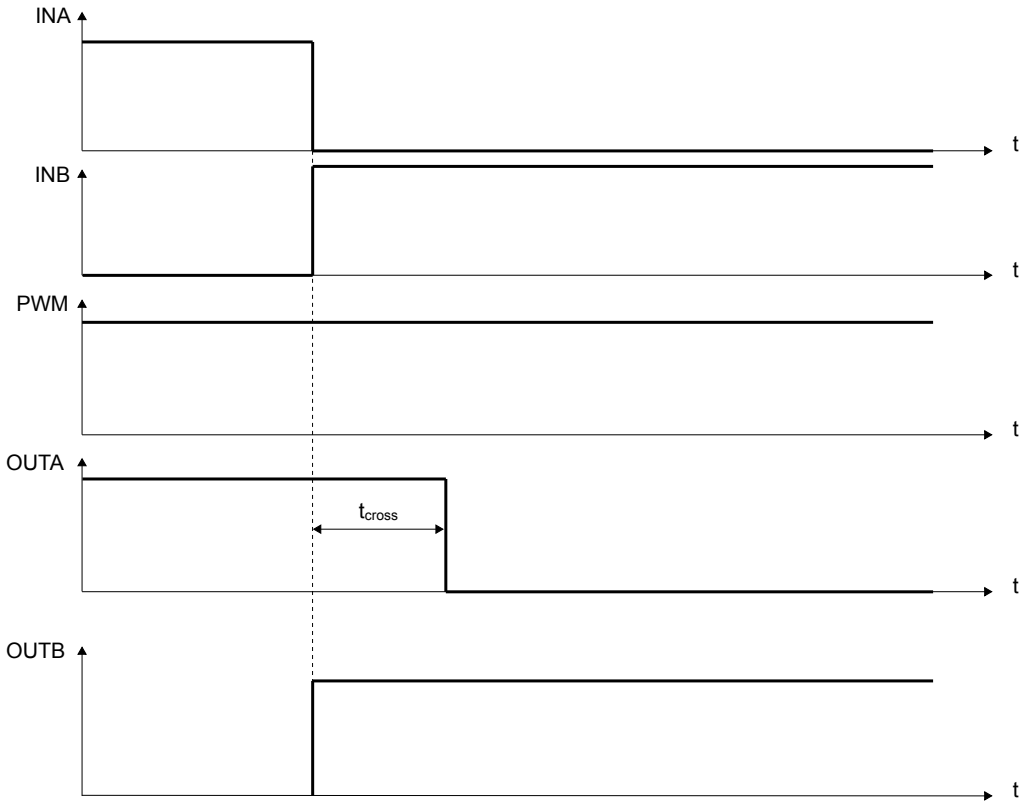

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Figure 9. **Time to shutdown for the low-side driver**

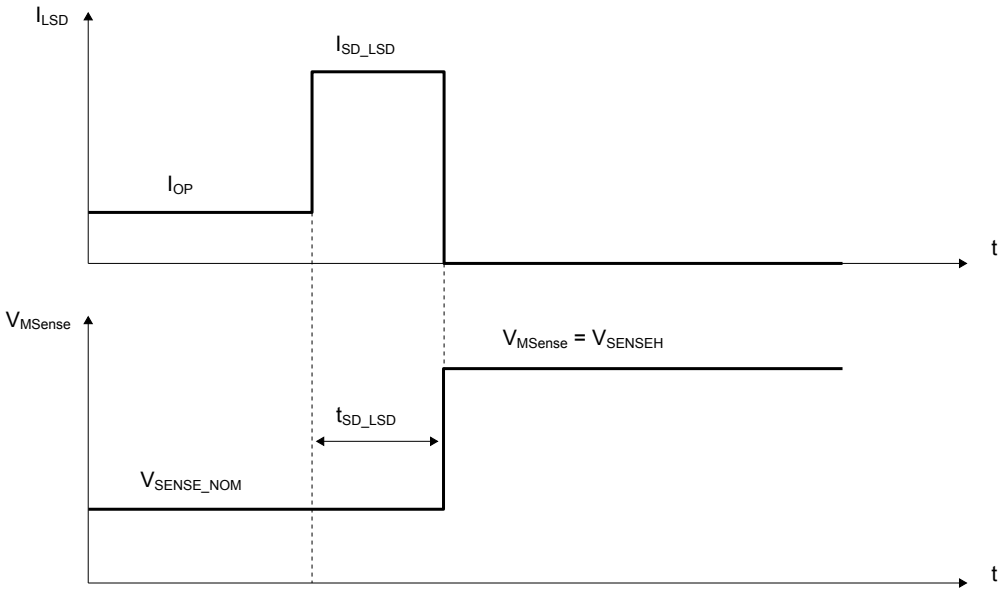

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Figure 10. **Input reset time for HSD-fault unlatch**

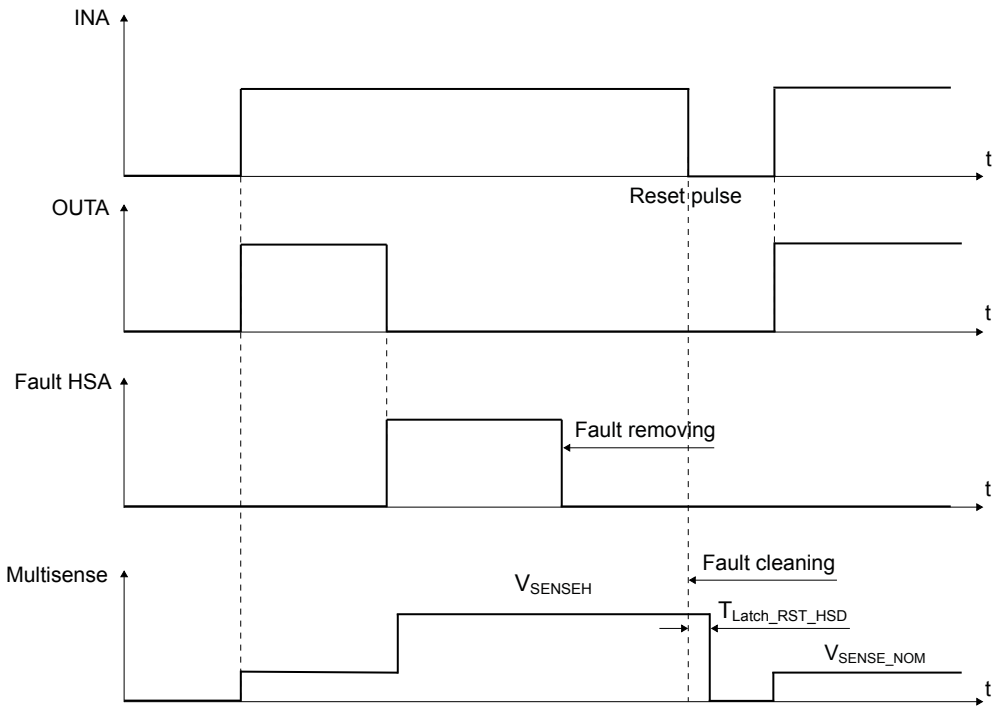

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Figure 11. **Input reset time for LSD-fault unlatch**

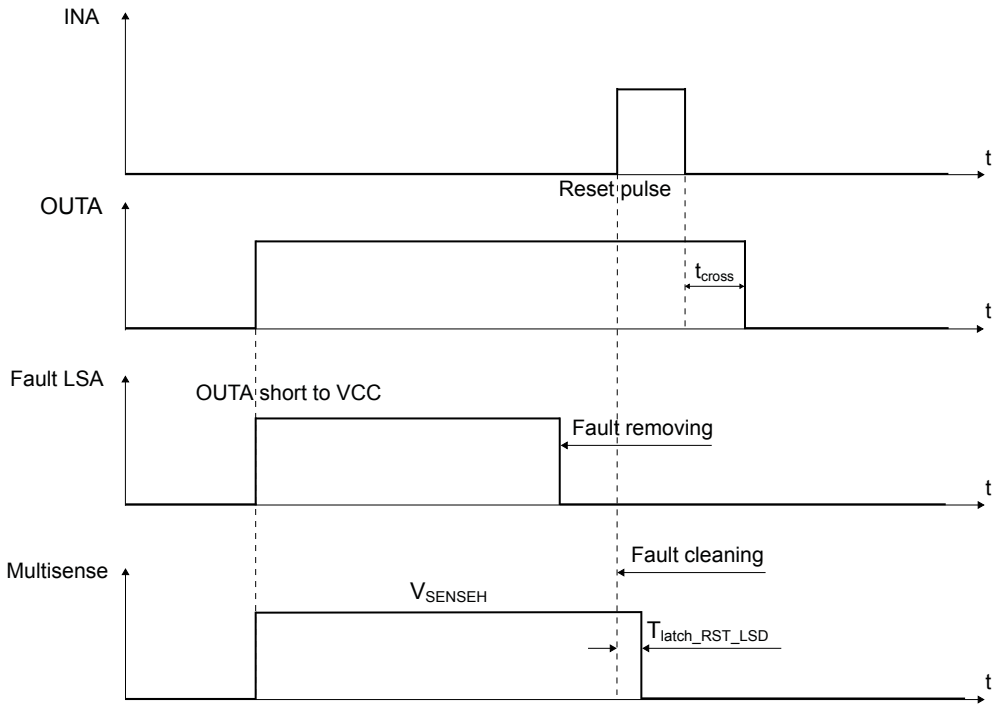

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Figure 12. **PH_OUT delay time on out switch**

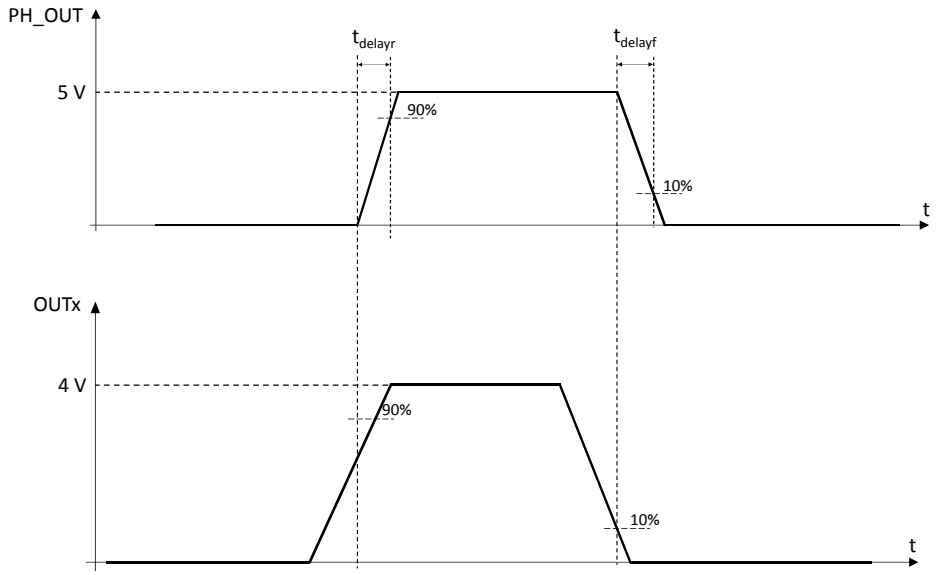

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Figure 13. **PH_OUT delay time on SELx change**

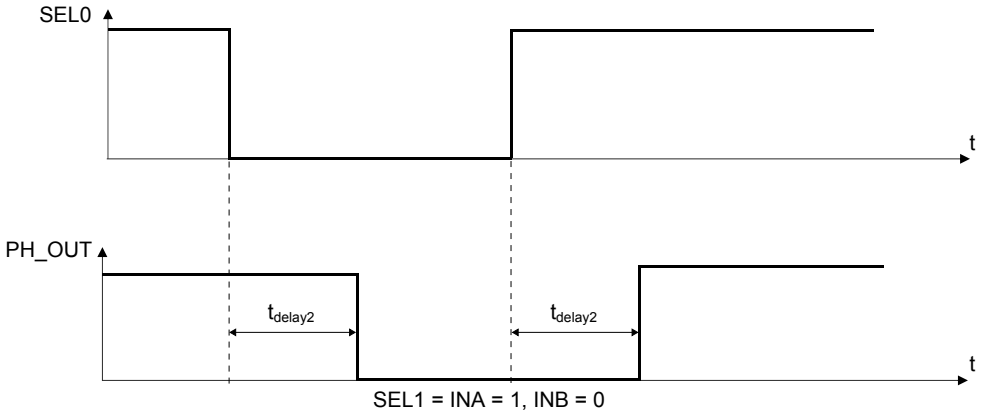

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Figure 14. **OFF-state diagnostic delay time from rising edge of V_{OUT} (t_{D_VOL})**

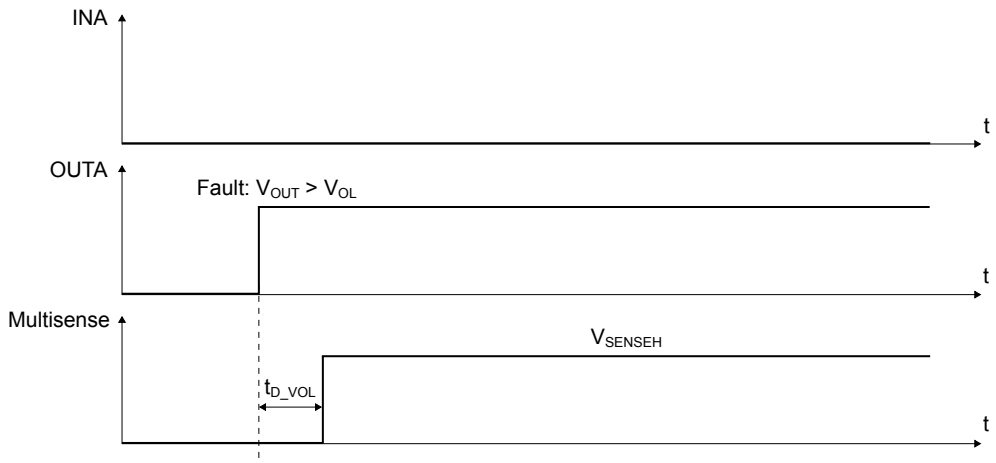

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Table 13. **Truth table: operative condition and diagnostic**

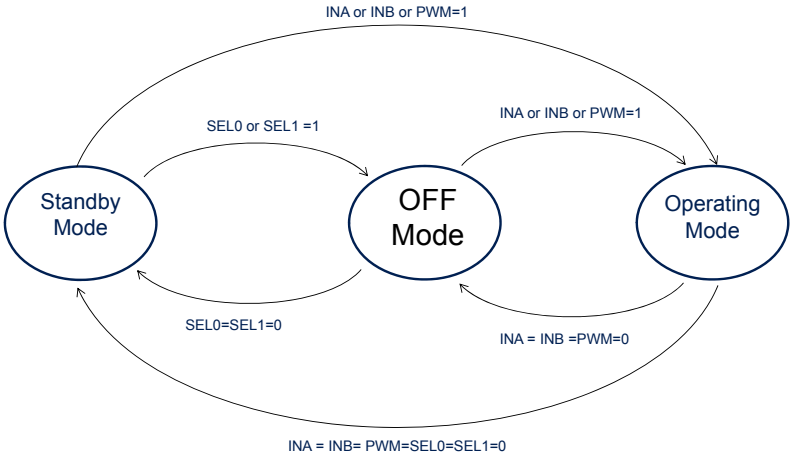
SEL0	SEL1	INA	INB	PWM	HB status	PH_OUT	Multisense	Diagnostic multisense = V_{SENSEH}	Comments
1	0	1	0	1	Clock	MONITOR A	Current sense ON HSA	ON state HSA protection triggered, HSA latched off	
		0	1	1	Counterclock	MONITOR A	HIZ	ON state LSA protection triggered, LSA latched off	
		1	1	0	BRAKE VCC	MONITOR A	Current sense ON HSA	ON state HSA protection triggered, HSA latched off	
		0	0	1	BRAKE GND	MONITOR A	HIZ	ON state LSA protection triggered, LSA latched off	
		1	0	0	HSA ON	MONITOR A	Current sense ON HSA	ON state HSA protection triggered, HSA latched off	
		0	1	0	HSB ON	MONITOR A	HIZ		
		0	0	0	OFF	MONITOR A	HIZ	$V_{OUTA} > V_{OL}$: NO open-load in full bridge configuration, OUTA shorted to VCC in half bridge configuration	Pull up on OUTB - diagnostic in off state
		1	1	1	BRAKE VCC	MONITOR A	Current sense ON HSA	ON state HSA protection triggered, HSA latched off	
0	1	1	0	1	Clock	MONITOR B	HIZ	ON state LSB protection triggered, LSB latched off	
		0	1	1	Counterclock	MONITOR B	Current sense ON HSB	ON state HSB protection triggered, HSB latched off	
		1	1	0	BRAKE VCC	MONITOR B	Current sense ON HSB	ON state HSB protection triggered, HSB latched off	

SEL0	SEL1	INA	INB	PWM	HB status	PH_OUT	Multisense	Diagnostic multisense = V_{SENSEH}	Comments
0	1	0	0	1	LSB ON/ LSA OFF	MONITOR B	HIZ	ON state LSB protection triggered, LSB latched off	Half bridge on LSB - Pull up on OUTB
		1	0	0	HSA ON	MONITOR B	HIZ		
		0	1	0	HSB ON	MONITOR B	Current sense ON HSB	ON state HSB protection triggered, HSB latched off	
		0	0	0	OFF	MONITOR B	HIZ	$V_{OUTB} > V_{OL}$: NO open-load in full bridge configuration, OUTB shorted to VCC in half bridge configuration	Pull up on OUTA - diagnostic in off state
		1	1	1	BRAKE VCC	MONITOR B	Current sense ON HSB	ON state HSB protection triggered, HSB latched off	
1	1	1	0	1	Clock	MONITOR A	HIZ	TCHIP WARNING	
		0	1	1	Counterclock	MONITOR A	HIZ	TCHIP WARNING	
		1	1	0	BRAKE VCC	MONITOR A	HIZ	TCHIP WARNING	
		0	0	1	LSA ON/LSB OFF	MONITOR A	HIZ	ON state protection triggered, LSA latched off	Half bridge on LSA - Pull up on OUTA
		1	0	0	HSA ON	MONITOR A	HIZ	TCHIP WARNING	
		0	1	0	HSB ON	MONITOR A	HIZ	TCHIP WARNING	
		0	0	0	OFF	MONITOR A	HIZ	Full bridge configuration: OUTA shorted to VCC, $V_{OUTA} > V_{OL}$	
		1	1	1	BRAKE VCC	MONITOR A	HIZ	TCHIP WARNING	
0	0	1	0	1	Clock	MONITOR B	HIZ		
		0	1	1	Counterclock	MONITOR B	HIZ		
		1	1	0	BRAKE VCC	MONITOR B	HIZ		
		0	0	1	BRAKE GND	MONITOR B	HIZ	ON state LSB protection triggered, LSB latched off	
		1	0	0	HSA ON	MONITOR B	HIZ		
		0	1	0	HSB ON	MONITOR B	HIZ		
		0	0	0	STAND BY	HIZ	HIZ		
		1	1	1	BRAKE VCC	MONITOR B	HIZ		

Note:

1. *SOURCE_HSA shorted to DRAIN_LSA = OUTA, SOURCE_HSB shorted to DRAIN_LSB = OUTB.*
2. *In brake to GND condition (INA = INB = L, PWM = H) settling the pin SEL1 = 1 AND SEL0 = 0 or SEL1 = 1 AND SEL0 = 1 it is possible to keep one leg in high-Z for half bridge configuration and diagnostic.*
3. *When INA = INB = PWM = SEL0 = SEL1 = 0 the device enters in standby after T_{DSTBY}.*

Figure 15. **State diagram**



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3 Protections

3.1 Power limitation (high-side driver)

The power limitation protection consists of an indirect measurement of the junction temperature swing ΔT_J through the direct measurement of the spatial temperature gradient on the device surface. As soon as ΔT_J exceeds the safety level of ΔT_{J_SD}, the Power MOSFET output is automatically shut off. The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue. When power limitation is reached, the device enters in latch mode and generates the fault flag on multisense = V_{senseH} when the faulty leg diagnostic is selected (please refer to the Truth table: operative condition and diagnostic). The concerned high-side can be switched ON again by applying the reset pulse as described in Figure 10.

3.2 Thermal shutdown (high-side and low-side)

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175 °C), it automatically switches off and the diagnostic indication is triggered on Multisense (please refer to the Truth table: operative condition and diagnostic). The device can switch on again as soon as: T_J drops below thermal reset temperature, then by applying the reset pulse as described in Figure 10 or Figure 11.

3.3 Current limitation and overcurrent detector

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (for example bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow.

High side current limitation: in case of short-circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIM_HSD}, by operating the output Power MOSFET in the active region.

Low side overcurrent detector: this protection senses the current flowing in the low side. If the current exceeds a safety level I_{SD_LS}, the device switches off after a filtering time t_{SD_LSD}.

In the case of fault conditions caused by power limitation or overtemperature or open load/short to VCC in OFF state, the fault is indicated by the Multisense pin being internally switched to a “current limited” voltage source pulled to level V_{SENSEH} (please refer to the Truth table: operative condition and diagnostic).

4 Typical application schematic

Figure 16. **Typical application schematic**

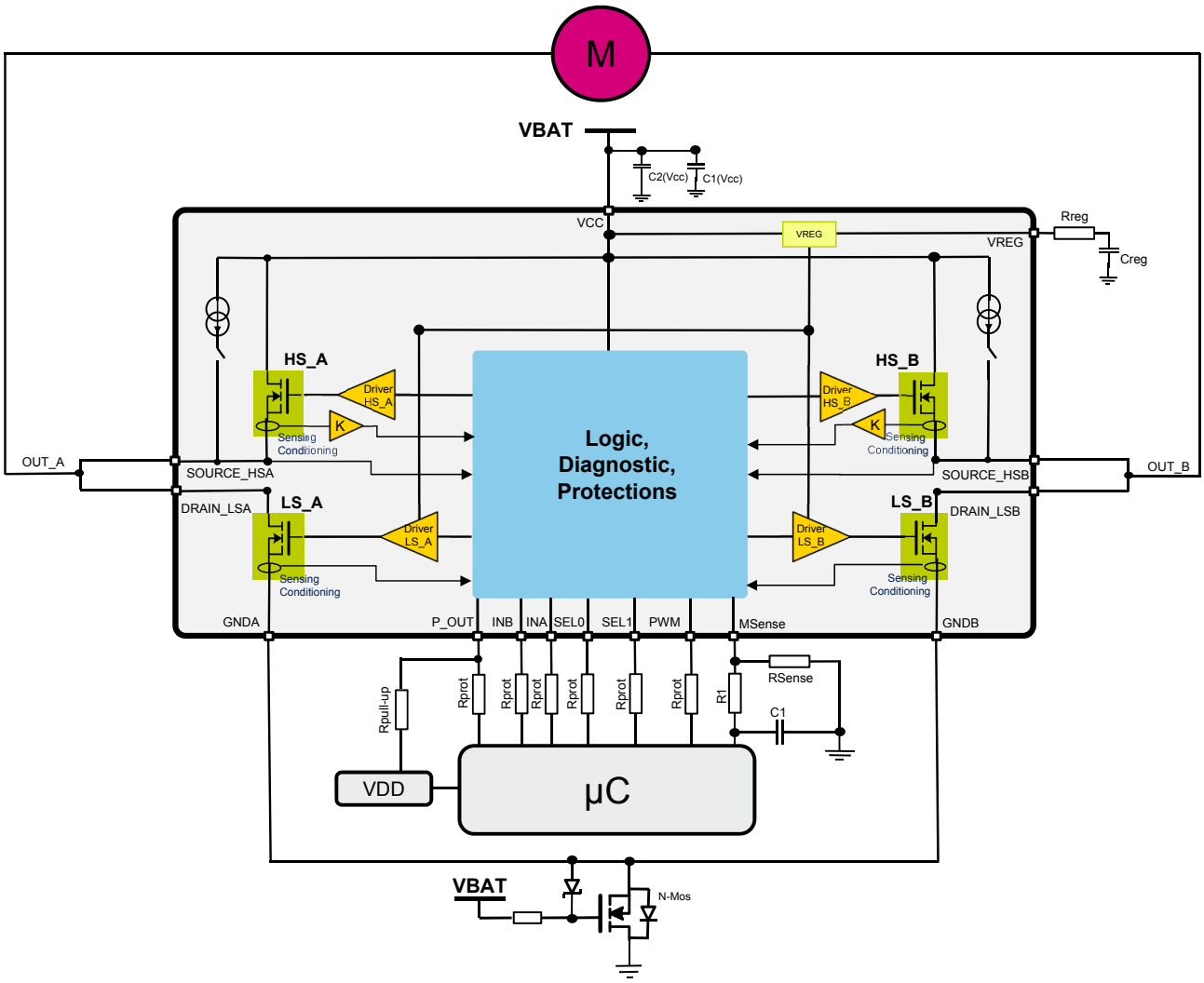

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Table 14. **Suggested external components**

Component	Value
C1 (V_{CC})	100 nF
C2 (V_{CC})	470 µF
R_{Reg}	220 Ω
C_{Reg}	100 nF
R_{Prot}	1.5 kΩ
R1	10 kΩ
R_{Sense}	0.7 kΩ
C_{Sense}	10 nF
R_{Pup}	10 kΩ

5 Multisense operation

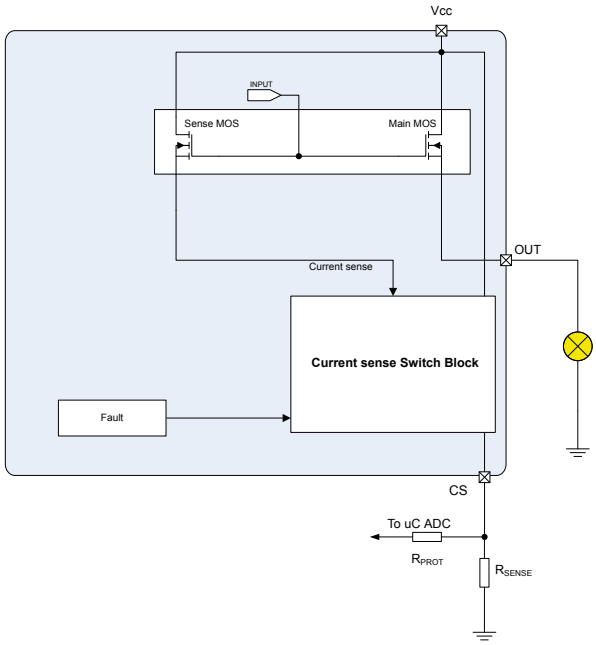
5.1 Multisense analog current monitoring

Diagnostic information on device and load status is provided by an analog output pin (Multisense) delivering the current mirror of high-side output current.

The signal is routed through an analog multiplexer, which is configured and controlled by means of SELx pins, according to the address map in Multisense multiplexer addressing table.

5.1.1 Current sense signal generation principle

Figure 17. Current sense block diagram



Current sense

The output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named K
- Diagnostics flag in fault conditions delivering a current I_{SENSEH} converted into a voltage (V_{SENSEH}) by using an external sense resistor

The current delivered by the current sense circuit, I_{SENSE}, can be easily converted into a voltage V_{SENSE} by using an external sense resistor, R_{SENSE}, allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault)

While the device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations.

Current provided by MultiSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE}: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is the voltage measurable on the R_{SENSE} resistor
- I_{SENSE} is the current provided from current sense pin in current output mode
- I_{OUT} is the current flowing through output

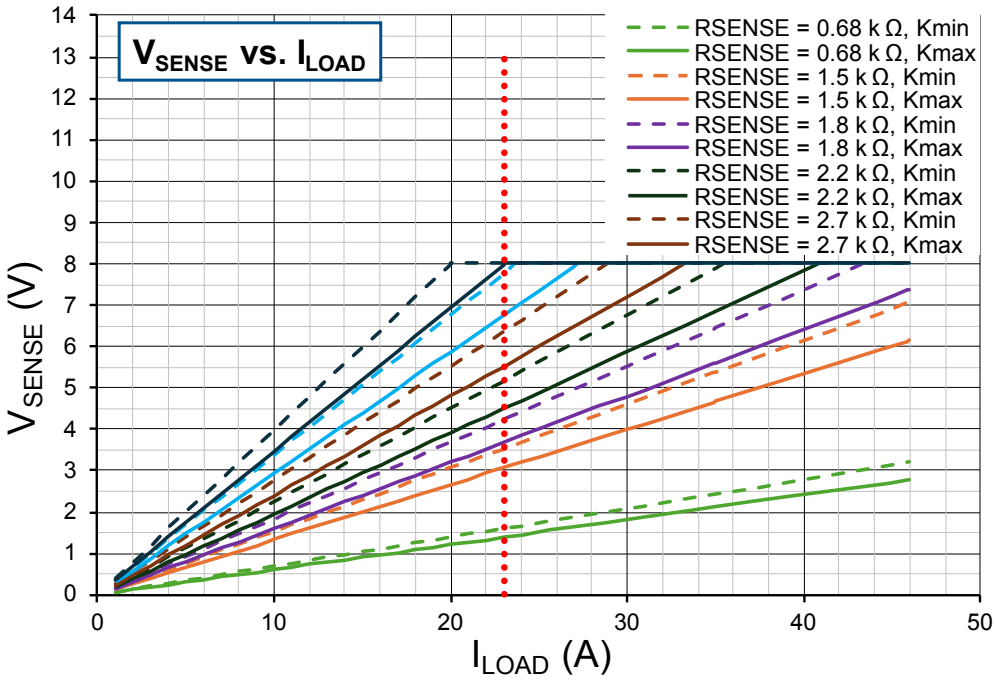
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying the ratio between I_{OUT} and I_{SENSE}.

Current sense voltage saturation

In current sense mode the multisense pin has an intrinsic voltage dynamic range that depends on V_{CC} battery voltage. When the MSense pin exceeds the V_{SENSE_SAT} value, the current sense loses its linear behavior and saturates. At V_{CC} = 13 V, V_{SENSE_SAT} value is typically ~7.5 V, while the minimum $V_{SENSE\_SAT\_MIN}$ = 4.8 V is at V_{CC} = 7 V and T_J = -40 °C.

A proper dimensioning of R_{SENSE} value can ensure current sense linearity over the load current range. The Figure 18 shows the V_{SENSE} behavior for several values of R_{SENSE}:

Figure 18. V_{SENSE} vs I_{LOAD} at V_{CC} = 13 V



5.2 Multisense diagnostics flag in fault conditions

Selecting multisense output as per Table 13, MSense pin delivers a current I_{SENSEH} converted to a voltage (V_{SENSEH}) by using an external sense resistor:

- Fault condition on **activated high-side** (in ON state) triggered by power limitation, overtemperature protection, where multisense output is selected as per Table 13 to high-side in fault state.
- Fault condition on a**ctivated low-side** (in ON state) triggered by overcurrent shutdown, overtemperature protection, where Multisense output is selected as per Table 13 to the same leg (of high-side) where low-side is in fault state.
- Short circuit to VCC on OUT in OFF state (INA = INB = PWM = 0).
- T_{CASE} warning: when T_{chip} exceeds $T_{CASE\_Warning}$ (typ. 140 °C).

5.3 Diagnostic in off-state

The diagnostic in off-state operates when output is deactivated (it means INA = INB = PWM = 0). The detection is performed by reading the multi sense output (V_{SENSEH} or HIZ) and also checking the PH_OUT status pin.The output to be monitored and internal pull-up are selectively switched through SEL0 and SEL1 as per Table 13.

Pulling output voltage above the maximum open-load detection voltage (VOL MAX) allows to detect short to VCC or open-load conditions before starting the motor.

6 VREG and Driver_LS block

The VREG pin is the output of an internal low drop voltage regulator. The VREG block is designed to power the driver of LS Power MOSFET and it allows a proper MOSFET transition.

An external capacitor C_{REG} = 100 nF and series resistor R_{REG} = 220 Ω must be connected to the pin VREG that is needed to properly polarize the circuit (see Figure 16). The VREG output voltage is VREG = 7 V if VBAT > 7 V, while VREG = VBAT if VBAT < 7 V.

7 Output monitoring

The device features the possibility to provide a digital signal through the PH_OUT pin to let an external microcontroller the read of the OUT phase according to the Table 13. Truth table: operative condition and diagnostic.

It allows the system to detect if a single Power MOSFET remains permanently ON or OFF independently from input state in both ON state and OFF state. The microcontroller selecting the input SEL0 and SEL1 according to the Table 13 checks that the output state is consistent with input logic (INA, INB, and PWM) and provides the reaction of unwanted motor activation. The detection of phase readout requires the internal pull-up and pull-down resistor RPU connecting the output (refer to the Table 13).

- During clockwise and counterclockwise motor activations, external R_{PULL_UP} is not needed.
- During brake to VBAT, the microcontroller alternatively switches off one of the two high-side blocks and thanks to the embedded pull-down resistor the microcontroller can detect if the related high side is failing short through the PH_OUT pin.
- During brake to GND, the microcontroller alternatively switches off one of the two low-side blocks and thanks to the embedded pull-up the microcontroller can detect if the related low side is failing short through the PH_OUT pin.

Note: In brake to GND condition (INA = INB = L, PWM = H) settling the pins SEL1 and SEL0 according to Truth table: operative condition and diagnostic it is possible to keep one leg in high-Z to use the device in full half bridge operation.

8 MCU I/Os protection

If a ground protection network is used and negative transients are present on the VCC line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

9 Immunity against transient electrical

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the VCC pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010. The related function performance status classification is shown in Table 15. Test pulses are applied directly to DUT (device under test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the current device only, with external components as shown in Figure 16. Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

Table 15. ISO 7637-2 – electrical transient conduction along supply line

Test pulse 2011 (E)	Test pulse severity level with status II functional performance status		Minimum number of pulses or test time	Burst cycle/ pulse repetition time		Pulse duration and pulse generator internal impedence
	Level	U_S[1]		Min.	Max.	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
4[2]	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2: 2010						
Test B[3]		35 V	5 pulses	1 min.		400 ms, 2 Ω

1. *US is the peak amplitude as defined for each test pulse in ISO 7637-2: 2011 (E), chapter 5.6.*
2. *Test pulse from ISO 7637-2: 2004 (E).*
3. *With 35 V external suppressor referred to ground (-40 °C < T_J < 150 °C).*

10 Package and PCB thermal data

10.1 QFN 6x6 triple pad 26+2L PCB layout

Figure 19. QFN 6x6 26+2L PCB 6 layers

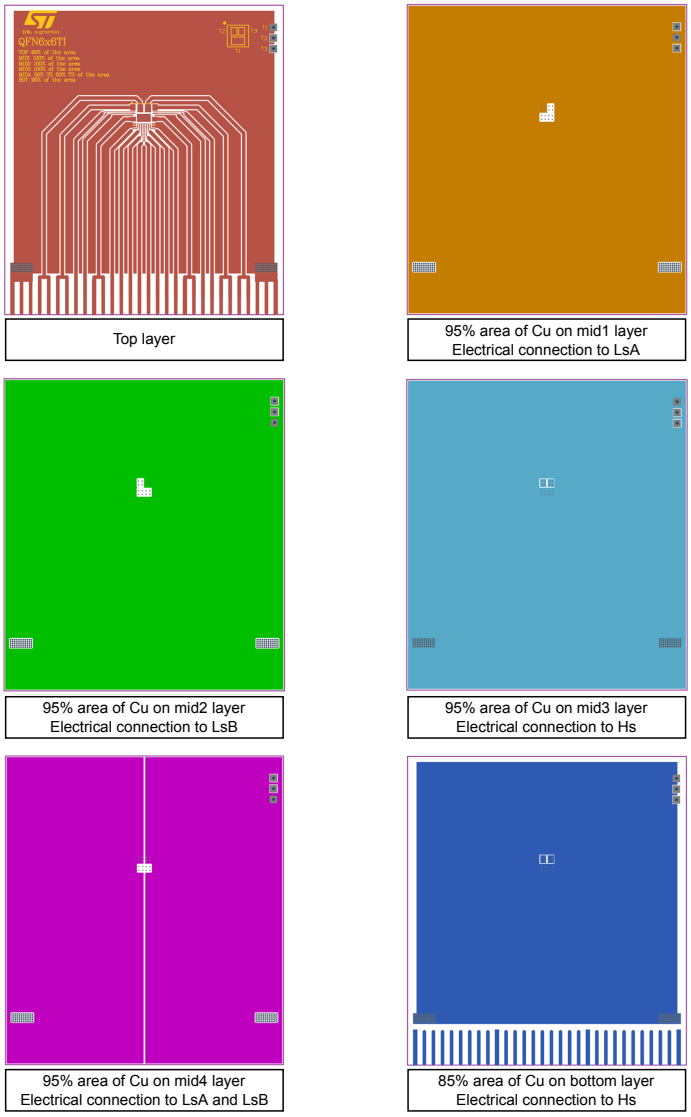


Table 16. **PCB properties**

Dimension	Value
Board	Six layers
Board finish thickness	1.6 mm ±10%
Board dimension	78 mm x 86 mm
Board material	FR4
Cu thickness (outer layers)	0.070 mm
Cu thickness (inner layers)	0.035 mm
Thermal vias spaced on a	1.2 mm x 1.2 mm grid.
Vias pad clearance thickness	0.2 mm
Thermal vias diameter	0.3 mm ±0.08 mm
Cu thickness on vias	0.025 mm

Figure 20. **Chipset configuration**

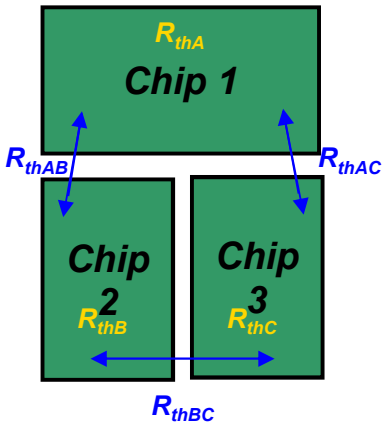


Table 17. **$R_{thJ\text{-}Amb}$ vs Cu area dissipation**

Thermal resistance (°C/W)	6L
R_{thA}	24.8
$R_{thB} = R_{thC}$	28.5
$R_{thAB} = R_{thAC}$	10.1
R_{thBC}	11.2

Note: The $R_{thJ\text{-}PCB}$ is measured on 6L = 8.3 °C/W.

10.1.1 Thermal resistances definition

The values are defined according to the PCB heatsink area:

- $R_{thHS} = R_{thHSA} = R_{thHSB}$ = high side chip thermal resistance junction to ambient (HSA or HSB in ON state)
- $R_{thLS} = R_{thLSA} = R_{thLSB}$ = low side chip thermal resistance junction to ambient
- $R_{thHSLS} = R_{thHSALSB} = R_{thHSBLSA}$ = mutual thermal resistance junction to ambient between high side and low side chips
- $R_{thLSLS} = R_{thLSALSB}$ = mutual thermal resistance junction to ambient between low side chip.

Table 18. **Thermal model for junction temperature calculation in steady-state conditions**

Chip 1	Chip 2	Chip 3	T_{jchip1}	T_{jchip2}	T_{jchip3}
ON	OFF	ON	$P_{dchip1} \cdot R_{thA} + P_{dchip3} \cdot R_{thAC} + T_A$	$P_{dchip1} \cdot R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_A$	$P_{dchip1} \cdot R_{thAC} + P_{dchip3} \cdot R_{thC} + T_A$
ON	ON	OFF	$P_{dchip1} \cdot R_{thA} + P_{dchip2} \cdot R_{thAB} + T_A$	$P_{dchip1} \cdot R_{thAB} + P_{dchip2} \cdot R_{thB} + T_A$	$P_{dchip1} \cdot R_{thAC} + P_{dchip2} \cdot R_{thBC} + T_A$
ON	OFF	OFF	$P_{dchip1} \cdot R_{thA} + T_A$	$P_{dchip1} \cdot R_{thAB} + T_A$	$P_{dchip1} \cdot R_{thAC} + T_A$
ON	ON	ON	$P_{dchip1} \cdot R_{thA} + (P_{dchip2} + P_{dchip3}) \cdot R_{thAB} + T_A$	$P_{dchip2} \cdot R_{thB} + P_{dchip1} \cdot R_{thAB} + P_{dchip3} \cdot R_{thBC} + T_A$	$P_{dchip1} \cdot R_{thAB} + P_{dchip2} \cdot R_{thBC} + P_{dchip3} \cdot R_{thC} + T_A$

10.1.2 Thermal characterization during transients

$T_{hs} = P_{dhs} * Z_{hs} + Z_{hsls} * (P_{dlsA} + P_{dlsB}) + T_{Amb}$

$T_{lsA} = P_{dlsA} * Z_{ls} + P_{dhs} * Z_{hsls} + P_{dlsB} * Z_{lsls} + T_{Amb}$

$T_{lsB} = P_{dlsB} * Z_{ls} + P_{dhs} * Z_{hsls} + P_{dlsA} * Z_{lsls} + T_{Amb}$

Figure 21. **HSD thermal impedance junction ambient single pulse**

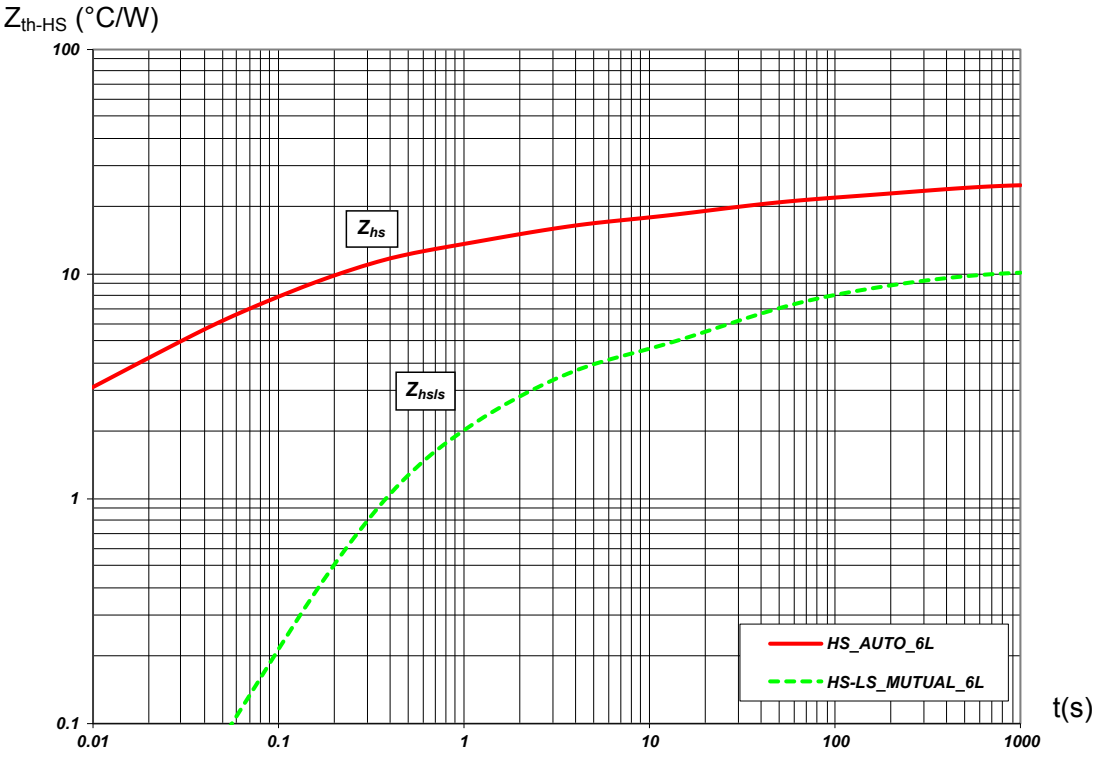


Figure 22. **LSD thermal impedance junction ambient single pulse**

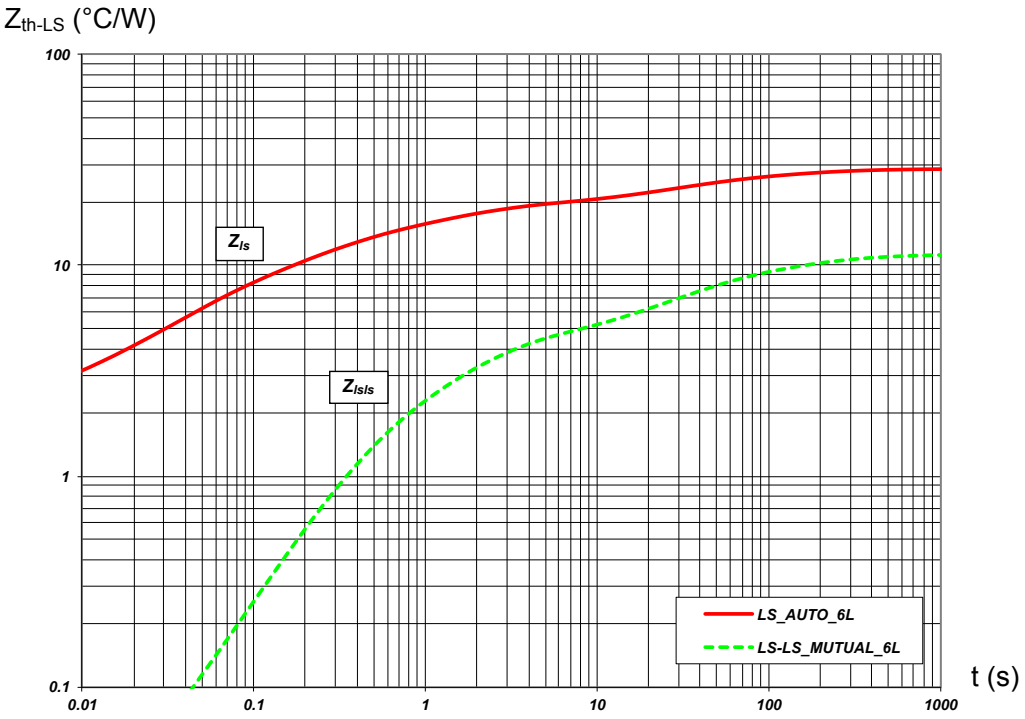
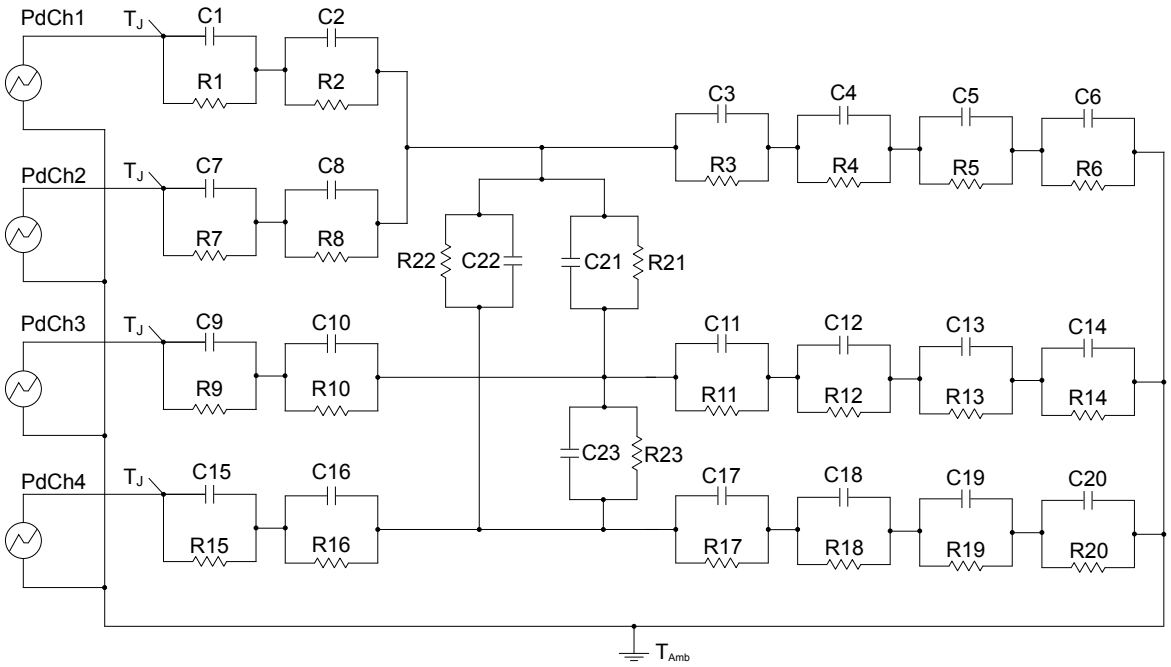


Figure 23. **Thermal fitting model**



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Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 19. **Thermal parameters**

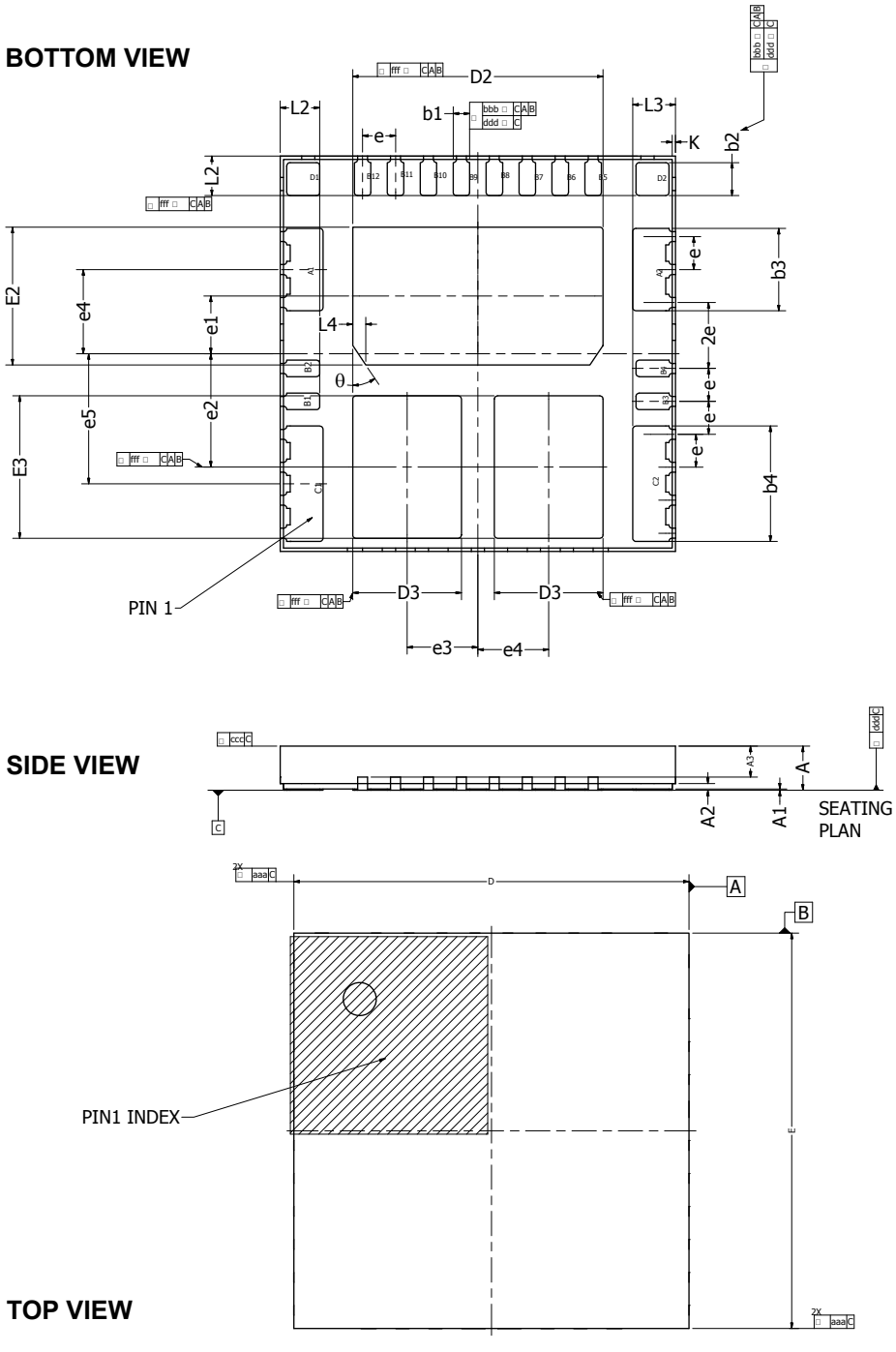
Thermal parameter	6L
R1 = R7 (°C/W)	1.55
R2 = R8 (°C/W)	2.8
R3 (°C/W)	8.5
R4 (°C/W)	8.5
R5 (°C/W)	9
R6 (°C/W)	9.5
R9 = R15 (°C/W)	1.9
R10 = R16 (°C/W)	3.3
R11 = R17 (°C/W)	7.5
R12 = R18 (°C/W)	14
R13 = R19 (°C/W)	13
R14 = R20 (°C/W)	14
R21 = R22 (°C/W)	50
R23 (°C/W)	47
C1 = C7 (W·s/°C)	0.0012
C2 = C8 (W·s/°C)	0.007
C3 (W·s/°C)	0.022
C4 (W·s/°C)	0.2
C5 (W·s/°C)	2.3
C6 (W·s/°C)	40
C9 = C15 (W·s/°C)	0.0007
C10 = C16 (W·s/°C)	0.01
C11 = C17 (W·s/°C)	0.03
C12 = C18 (W·s/°C)	0.1
C13 = C19 (W·s/°C)	2.2
C14 = C20 (W·s/°C)	8
C21 = C22 (W·s/°C)	0.0005
C23 (W·s/°C)	0.0011

11 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

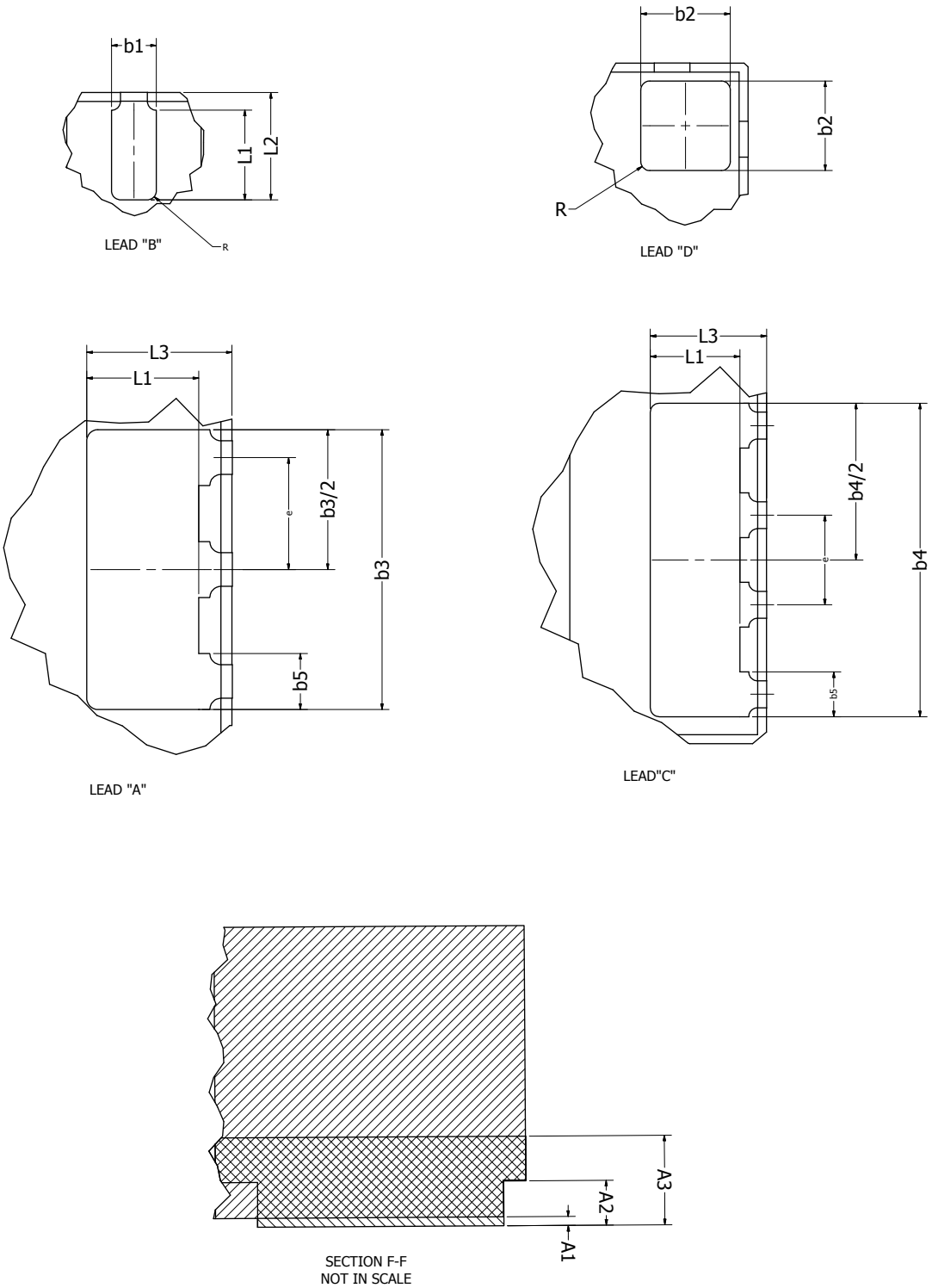
11.1 QFN 6x6 triple pad 26+2L package information

Figure 24. QFN 6x6 triple pad 26+2L package outline



DM00683589_3

Figure 25. **QFN 6x6 triple pad 26+2L package sections**



DM00683589_sections_3

Table 20. **QFN 6x6 triple pad 26+2L mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00		0.05
A2	0.10		
A3		0.20 REF.	
b1	0.20	0.25	0.30
b2	0.45	0.50	0.55
b3	1.15	1.25	1.35
b4	1.65	1.75	1.85
b5	0.20	0.25	0.30
D		6.00 BSC	
E		6.00 BSC	
D2	3.70	3.75	3.80
D3	1.55	1.60	1.65
E2	2.00	2.05	2.10
E3	2.05	2.10	2.15
e		0.50 REF	
e1		0.88 REF	
e2		1.72 REF	
e3		1.08 REF	
e4		1.28 REF	
e5		1.97 REF	
L1	0.45	0.50	0.55
L2	0.55	0.60	0.65
L3	0.65	0.70	0.75
L4	0.15	0.20	0.25
θ		34°	
N		26 + 2	
R		0.05	

Table 21. **QFN 6x6 triple pad 26+2L tolerance of form and position**

Symbol	Millimeters
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

12 Ordering information

Table 22. **Order code**

Order code	Package	Package marking	Packing
VNH9045AQTR	QFN 6x6 triple pad 26+2L	VNH9045AQ	Tape and reel

Revision history

Table 23. **Document revision history**

Date	Revision	Changes
18-Dec-2023	1	Initial release.
24-Oct-2024	2	Updated *Section Features*, *Table 4. Absolute maximum ratings*, *Table 7. Supply and supply monitoring*, *Table 9. Logic outputs (PH_OUT) open drain output*, *Table 10. Switching*, *Table 12. Multisense* and *Figure 12. PH_OUT delay time on out switch*. Added *Figure 18. V_{SENSE} vs I_{LOAD} at V_{CC} = 13 V* and *Section 10: Package and PCB thermal data*.
06-Nov-2024	3	Updated *Section 2.3: Thermal data*.
19-Dec-2024	4	Updated Section Product status link / summary.
16-Apr-2025	5	Update cover image.
15-May-2025	6	Typo correction.

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