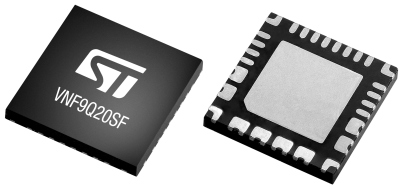
VNF9Q20SF

Datasheet

4-channel high-side driver with STi²Fuse protection for automotive power distribution applications



QFN 6x6 mm

STi²Fuse

Product summary	
Order code	VNF9Q20SFTR
Package	QFN 6x6
Packing	Tape and reel

Features

Channel	V_{CC}	R_{ON} typ.	I_{LIMH} typ.
0, 1, 2, 3	28 V	21.5 mΩ	34.5 A

- AEC-Q100 qualified
- General
  - Quad channel with 24-bit ST-SPI for full diagnostic and digital current sense feedback
  - Integrated 10-bit ADC for digital current sense
  - Integrated PWM engine with independent phase shift and frequency generation (for each channel)
  - Standby-on functionality for parking mode - I_{SOFF2} < 15 µA per channel
  - Programmable Bulb/LED mode for all channels
  - Advanced limp-home functions for robust fail-safe system
  - Very low standby current
  - Control through direct inputs and/or SPI
  - Compliant with European directive 2002/95/EC
  - Capacitive loads charging mode
  - QFN 6x6 package with wettable flanks
- Diagnostic functions
  - Digital proportional load current sense
  - Synchronous diagnostic of overload, short to GND and harness protection
  - Asynchronous diagnostic of output shorted to V_{CC} and OFF-state open-load
  - Built In Self-Test for ADC and harness protection
  - Programmable case overtemperature warning
- Protections
  - Full configurable wire harness protection (STi²Fuse)
  - Programmable shut-off current for overload
  - Fast off by DI_x
  - Load current limitation
  - Self-limiting of fast thermal transients
  - Latch-off or programmable time limited auto-restart (power limitation and overtemperature shutdown)
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load dump protected
  - Protection against loss of ground

Description

The VNF9Q20SF is a device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads directly connected to the ground.

The device is protected against voltage transients on the V_{CC} pin. Programming, control, and diagnostics are implemented via the SPI bus. A digital current sense feedback for each channel is provided through an integrated 10-bit ADC. Dedicated trimming bits allow adjusting the ADC reference current.

The device is equipped with 4 outputs controllable via SPI or 2-OTP assignable direct inputs. In whatever operating situation it is always possible to turn off channels quickly by relevant DI_x (FAST_OFF < t_{DIx_off}). Real-time diagnostic is available through the SPI bus (open-load, output short to V_{CC}, overtemperature, communication error, power limitation or latch-off). The device detects open-load in OFF-state conditions.

The VNF9Q20SF embeds the STMicroelectronics proprietary I^2t functionality, featuring an intelligent circuit breaking aimed at protecting PCB traces, connectors and wire harness from overheating, with no impact on load transients like inrush currents and capacitance charging. This function is set by two parameters called I_{NOM} and t_{NOM}: there are 3 dedicated bits, per each parameter, to set respectively I_{NOM} (nominal current) and t_{NOM} (nominal timing). The I^2t curve parameters can be individually set per each channel.

The VNF9Q20SF can limit the dissipated power to a safe level up to thermal shutdown intervention. Thermal shutdown can be configured as latched off or programmable time limited auto-restart.

The output current limitation protects the device in case of overload.

The device enters a fail-safe mode in case of communication loss with the microcontroller, reset of digital memory or watchdog monitoring time-out event. In fail-safe mode, the 4 outputs can be directly controlled by dedicated, assignable direct inputs.

It is also possible to configure the VNF9Q20SF in parallel mode (CH0//CH1 only) through a dedicated OTP bit.

The VNF9Q20SF features an operative condition called capacitive charging mode (CCM), which is available in both fail-safe and normal device states and with channels configured in bulb mode.

During the sleep mode, the device is able to support the parking mode functionality. In case one or more OUTPUT pins are pulled up to battery by an external secondary switch (for instance the L99SP08 which is delivering the requested current to the load) the device offers a very low current consumption (I_{SOFF2}). For further information refer to the application note AN6371 - Interaction of L99SP08 with dual (VNF9DxxSF) and quad (VNF9Q20SF) M09 monolithic eFuses.

1 Block diagram and pin description

Figure 1. Block diagram

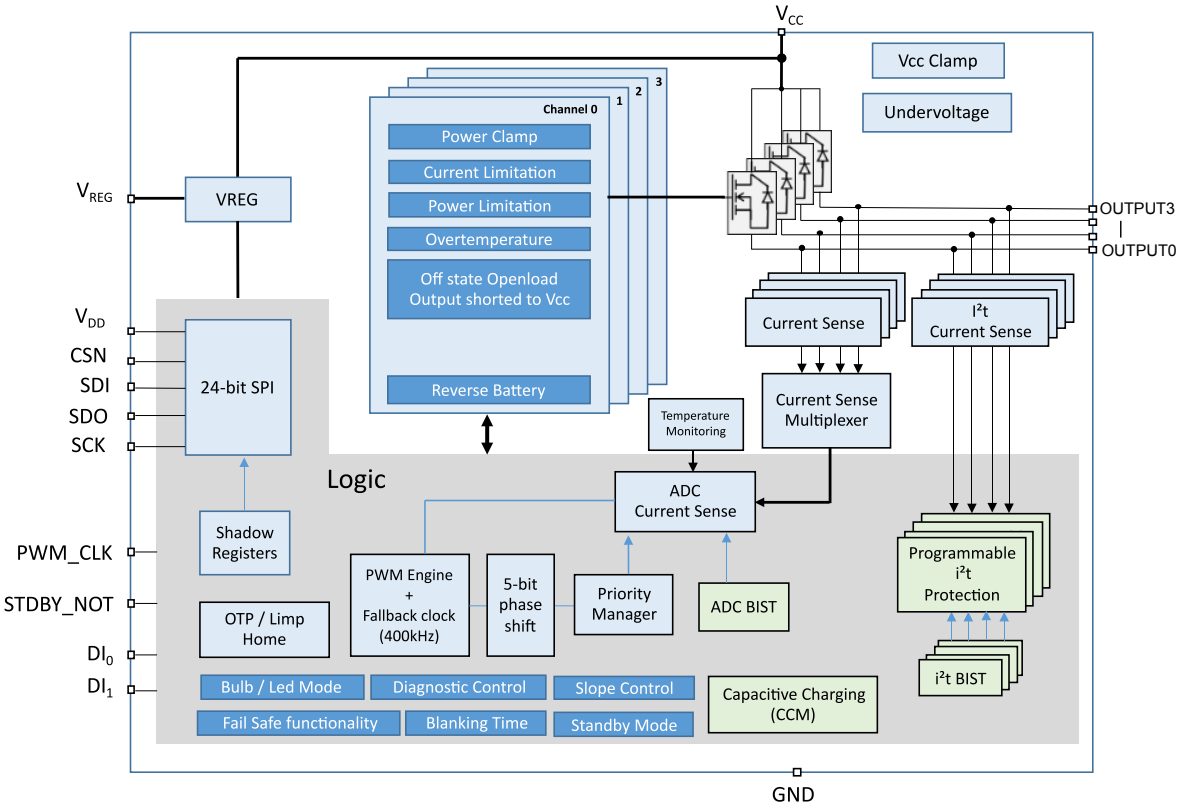
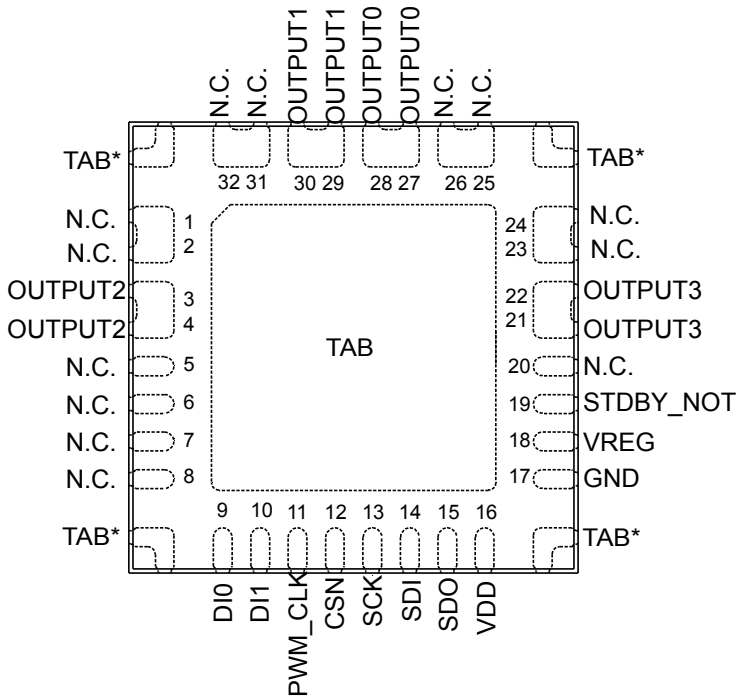


Figure 2. Connection diagram



*: Electrically connected to TAB. Those pins are intented for thermo-mechanical purpose only. They have to be soldered, but must be electrically isolated at PCB level.

Table 1. Pin functionality description

Pin #	Name	Function
TAB	VCC	Battery connection: this is the backside TAB and is the direct connection to drain Power MOSFET switches.
1, 2, 5-8, 20, 23-26, 31, 32	N.C.	Not connected pin.
3, 4	OUTPUT2	Power OUTPUT 2: direct connection to the source Power MOSFET channel 2.
9, 10	DI0, DI1	Direct input: direct control for OUTPUTx in limp-home mode. They work in AND combinationwith the relevant SPI OUTPUTx control bit in normal mode. By default, DI0 drives OUTPUT0,2 and DI1 drives OUTPUT1, 3.
11	PWM_CLK	External clock of PWM engine.
12	CSN	Chip select not (active low): it is the selection pin of the device. It is a CMOS compatible input.
13	SCK	Serial clock: it is a CMOS compatible input.
14	SDI	Serial data input: transfers data to be written serially into the device on the SCK rising edge.
15	SDO	Serial data output: transfers data serially out of the device on the SCK falling edge.
16	VDD	DC supply input for the SPI interface. 3.3 V and 5 V compatible.
17	GND	Ground connection: this pin serves as the ground connection for the logic part of the device.
18	VREG	DC output of internal preregulator (4.7 V) generated from V_{CC} to supply VREG pin and digital control circuit. Connect a low ESR capacitor (2.2 µF) in series with a resistor (120 Ω) close to this pin referenced to device ground.
19	STDBY_NOT	Standby mode enabler (active low).
21, 22	OUTPUT3	Power OUTPUT 3: direct connection to the source Power MOSFET channel 3.
27, 28	OUTPUT0	Power OUTPUT 0: direct connection to the source Power MOSFET channel 0.
29, 30	OUTPUT1	Power OUTPUT 1: direct connection to the source Power MOSFET channel 1.

2 Functional description

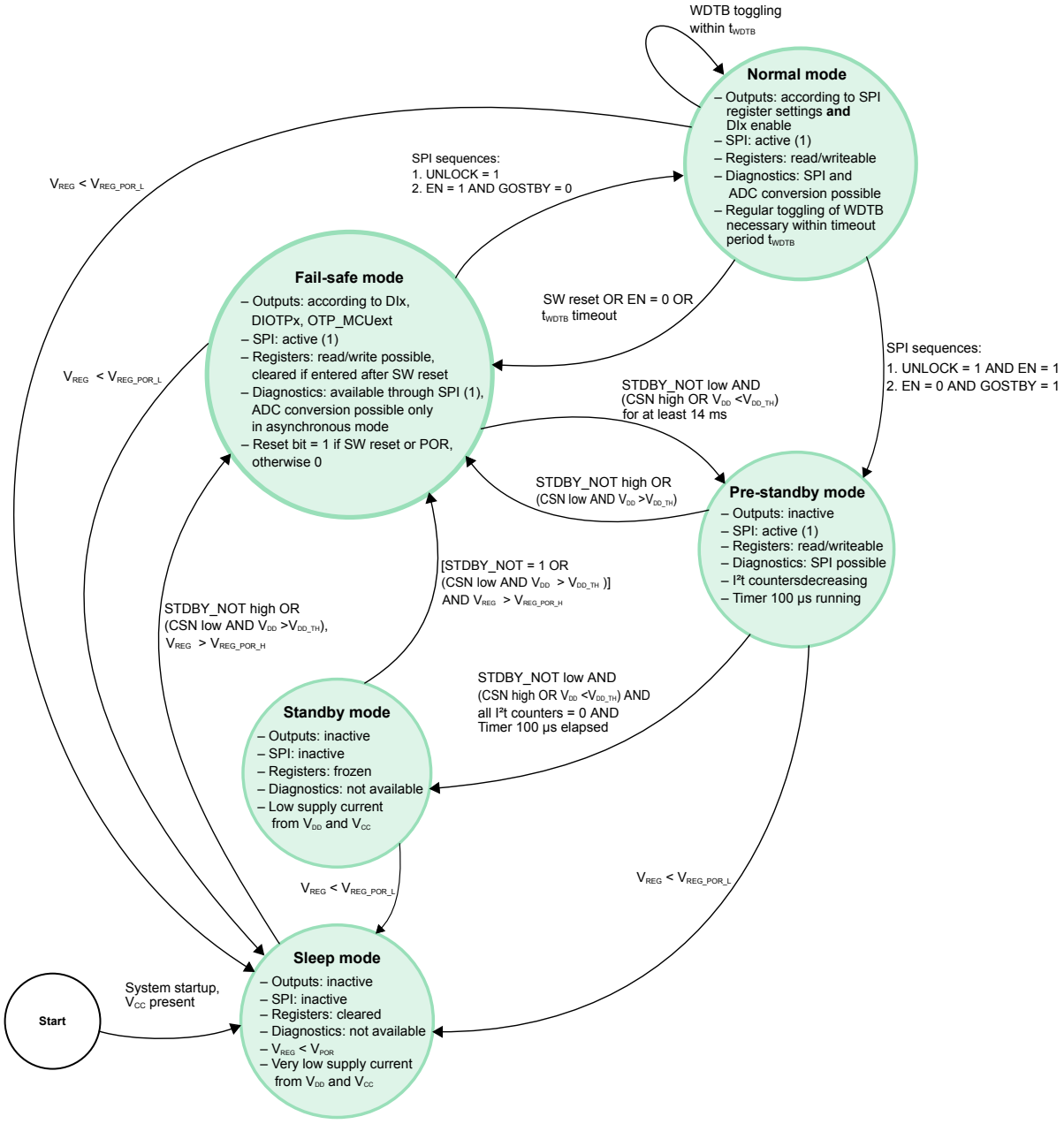
2.1 Device interfaces

- SPI: bi-directional interface, accessing RAM/ROM registers (CSN, SCK, SDI, SDO).
- PWM_CLK: PWM engine external clock.
- DIx: multipurpose pins configurable through OTP.
  - MCUext bit = 1 (default): input pins for outputs control while the device is in fail-safe mode or normal mode.
  - MCUext bit = 0: DI0 assumes digital diagnostic function while DI1 works as global I^2t protection unlatch controller (active high).
- V_{REG}: DC output of internal preregulator (4 V–6 V). DC supply input for the digital control part. A capacitor in series with a resistor should be connected between this pin and GND
- V_{DD}: DC supply of the SPI Interface. 3.3 V and 5 V compatible. A further external switchable diode (see Section 13: Application schematics) might be connected from V_{DD} pin (anode) to V_{REG} pin (cathode) to ensure a redundant supply to the digital part.
- STDBY_NOT: Standby mode enabler (active low).

2.2 State diagrams and operating modes

The device and the channel state diagrams are reported in Figure 3 and Figure 4 respectively; whilst the Table 2 shows the description of the operating modes.

Figure 3. Device state diagram



(1) SPI communication only if VDD is present.

As showed in the above figure, the device features five different operating modes:

- Standby mode
- Fail-safe mode
- Pre-standby mode
- Normal mode
- Sleep mode

The entering/leaving conditions as well as the operating modes characteristics are described in the Table 2.

Table 2. Operating modes

Operating mode	Entering conditions	Leaving conditions	Characteristics
Start: transition phase (not operating mode) where neither V_{REG} nor V_{CC} are available.	-	The device leaves this phase to enter sleep mode when: System startup, V_{CC} present	• $V_{CC} < V_{USD}$ • Outputs: OFF • SPI: inactive • Registers: reset values • Diagnostics: not available
Sleep mode: in this state, the device has very low consumption (below I_{SOFF2})	• From start phase: $V_{REG} < V_{POR}$, $V_{CC} > V_{USD}$ • From normal or fail-safe mode or pre-standby mode or standby mode: $V_{REG} < V_{REG\_POR\_L}$	The device leaves this state to enter fail-safe mode when: STDBY_NOT high OR (CSN low AND $V_{DD} > V_{DD\_TH}$), $V_{REG} > V_{REG\_POR\_H}$	• $V_{REG} < V_{REG\_POR\_H}$ • Outputs: OFF • SPI: inactive • Registers: reset values • Diagnostics: not available • Very low supply current (I_{SOFF2}) from V_{DD} and V_{CC}
Standby mode: in this state, the device has low consumption	From pre-standby mode: As soon as STDBY_NOT low AND (CSN high OR $V_{DD} < V_{DD\_TH}$) AND all I^2t counters = 0 AND t_{stdby} elapsed	The device leaves this state to enter sleep mode when: $V_{REG} < V_{REG\_POR\_L}$; The device leaves this state to enter fail-safe mode when: [STDBY_NOT = 1 OR (CSN low AND $V_{DD} > V_{DD\_TH}$)] AND $V_{REG} > V_{REG\_POR\_H}$	• $V_{REG} > V_{REG\_POR\_H}$ • Outputs: OFF • SPI: inactive • Registers: not readable • Diagnostics: not available • Low supply current from V_{DD} and V_{CC}
Fail-safe mode: (Limp-home)	• From pre-standby mode: STDBY_NOT = 1 OR (CSN low AND $V_{DD} > V_{DD\_TH}$) • From standby mode: [STDBY_NOT = 1 OR (CSN low AND $V_{DD} > V_{DD\_TH}$)] AND $V_{REG} > V_{REG\_POR\_H}$ • From normal mode: EN_bit = 0 OR WDTB timeout (t_{WDTB}) OR SW reset • From sleep mode: [STDBY_NOT = 1 OR (CSN low AND $V_{DD} > V_{DD\_TH}$)], $V_{REG} > V_{REG\_POR\_H}$	• If $V_{REG} < V_{REG\_POR\_L}$, the device enters sleep mode • If STDBY_NOT = 0 AND (CSN high OR $V_{DD} < V_{DD\_TH}$) for at least $t_{prestdby}$, the device enters pre-standby mode • If the SPI sends the following sequence, the device enters normal mode: 1st communication frame: • UNLOCK bit = 1 2nd communication frame: • EN bit = 1 AND GOSTBY bit = 0 This procedure avoids entering the normal mode unintentionally.	• $V_{REG} > V_{REG\_POR\_H}$ • Outputs: according to DIx, DIOTPx, MCUext • SPI: active • Registers: read/write possible, cleared if entered after SW reset • Diagnostics: available through SPI, ADC conversion available only in asynchronous mode • Reset bit: set to 1 if the last state is Standby mode or in case the last command is a SW reset; it is reset to 0 at the first SPI access • Protections: available. In case of over temperature or power limitation, the outputs work in auto-restart. • Harness protection: available for all channels. The channels are configured in auto-restart mode if MCUext bit = 1
Normal mode: the transition to this device state is possible ONLY from fail-safe state. DIx are enablers for the channels switching on.	• If it is in fail-safe AND the SPI sends the following sequence: 1st communication frame: • UNLOCK = 1 2nd communication frame: • GOSTBY = 0 AND EN = 1 This procedure avoids entering the normal mode unintentionally.	• If $V_{REG} < V_{REG\_POR\_L}$, the device enters the sleep mode • If the SPI clears the EN bit (EN bit = 0), the device enters the fail-safe • If WDTB is not toggled within the timeout period t_{WDTB}, the device enters fail-safe mode • If the SPI sends a SW reset, the device enters the fail-safe mode and all the registers are cleared • If the SPI sends the following sequence, the device enters the pre-standby mode:	• Outputs: according to SPI register settings AND DIx enable • SPI active • Diagnostic: available • Registers: read/write is allowed • Protections: available. The outputs can be set to “latch” or “time limited auto-restart”. In “time limited auto-restart”, the OUTPUTs are automatically switched on after an over temperature or power limitation event for a limited cumulated time duration; whilst in “latch”, the relevant status register must be cleared to switch OUTPUTs on again.

Operating mode	Entering conditions	Leaving conditions	Characteristics
		1st communication frame: • UNLOCK bit = 1 AND EN bit =1 2nd communication frame: • GOSTBY bit = 1 AND EN bit = 0 This procedure avoids entering the pre-standby mode unintentionally.	• Harness protection: available for all channels. The channels are configured in latch mode; • Reset bit = 0 • Regular toggling of WDTB is necessary within timeout period t_{WDTB}
Pre-standby mode	• If it is in fail-safe mode AND STDBY_NOT low AND (CSN high OR $V_{DD} < V_{DD\_TH}$) for a time $t > t_{prestdby}$ • If it is in normal mode AND the SPI sends the following sequence: 1st communication frame: • UNLOCK = 1 AND EN = 1 2nd communication frame: • GOSTBY = 1 AND EN = 0 (It is recommended to set also UNLOCK = 0, in this second frame). This procedure avoids entering the pre-standby mode unintentionally.	To fail-safe mode: If STDBY_NOT = 1 OR (CSN low and $V_{DD} > V_{DD\_TH}$) To standby mode: If STDBY_NOT = 0 AND (CSN high or $V_{DD} < V_{DD\_TH}$) AND all I^2t counters = 0 and tstdby elapsed To sleep mode: $V_{REG} < V_{REG\_POR\_L}$	• Outputs: OFF • SPI: active • Diagnostic: available • Registers: read/write is allowed • Protections: active • I^2t counters decreasing and t_{stdby} timer running
Capacitive charging mode (CCM): this is not device operating mode, but channel specific operating mode (see Figure 4)	From fail-safe mode: • If MCUext = 1 AND after 5 consecutive rising edges on DIx pins within t_{CCM_EN}, the corresponding channels will enter CCM, according to DIx OTP configuration. • If MCUext = 0 AND after 5 consecutive rising edges on DI1 pin within t_{CCM_EN}, according to OTP programming, relevant channels will enter CCM. From normal mode: • Set CAPCRx bit in SOCR register.	• Automatically after t_{CCM_DIS} time frame in both fail-safe and normal states. • In normal mode, also through a SPI frame, setting EXIT_CAPCRx bit in SOCR register whenever within t_{CCM_DIS} time frame	• Harness protections: disabled • LED mode: disabled • SPI: active • Latch-off delay time ($t_{D\_RESTART}$) after TSD event is disabled • Related parameters reported in Table 69
Battery undervoltage: transition phase (not device operating mode)	Any mode: $V_{CC} < V_{USD}$	If V_{DD} present AND $V_{REG} > V_{REG\_POR\_H}$	• Digital current-sense diagnostic: not available • Output stages are off regardless SPI or DIx status • SPI: active • Diagnostic: available • Registers: reading is possible • V_{CCUV} flag set, SPI registers content retained If $V_{CC} > V_{USD} + V_{USDhyst}$, the device comes back to the last mode and the V_{CCUV} flag is cleared. If $V_{REG} < V_{REG\_POR\_L}$ during V_{CC} increasing, the device is reset: the last operation mode is lost, the logic part is unpowered and the device enters sleep mode as soon as $V_{CC} > V_{USD} + V_{USDhyst}$.

Operating mode	Entering conditions	Leaving conditions	Characteristics
Battery undervoltage: transition phase (not device operating mode)	Any mode: $V_{CC} < V_{USD}$		During this case, if the DIx is changed, the operation mode is not changed and the output state will be changed accordingly after V_{CC} recovering.
		If V_{DD} NOT present AND $V_{REG} > V_{REG\_POR\_H}$	• Digital current-sense diagnostic: not available • Output Stages are off regardless SPI or DIx status • SPI: active but communication not possible • Diagnostic: NOT available • Registers: reading is not possible • V_{CCUV} flag set, SPI registers content retained. SPI register content reading always possible If $V_{CC} > V_{USD} + V_{USDhyst}$, the device comes back to the last mode and the V_{CCUV} flag is cleared. In this case, the operation mode is not changed and the output state is changed accordingly after V_{CC} recovering.
		If $V_{REG} < V_{REG\_POR\_L}$	• Digital current-sense diagnostic: not available • Output stages are off regardless SPI or DIx status The device is reset, the last operation mode is lost, the logic is unpowered and the device enters sleep mode as soon as $V_{CC} > V_{USD} + V_{USDhyst}$.

Transition to fail-safe mode from normal mode, using the SPI register

Only one frame is needed: write “CTRL” 0x0001.

Table 3. Frame 1 (write CTRL 0x0001)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	Not Used	Not Used	EN	PWM_TRIG	Not Used	Not Used
	0	0	0	0	0	0	0	0
DATA2	LOCKbit5	LOCKbit4	LOCKbit3	LOCKbit2	LOCKbit1	LOCKbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	1

Transition to fail-safe mode from normal mode by SW-reset

SPI Reset occurs by using the “read device information” command (applicable only on ROM area) at the reserved ROM address 0x3F. This is equivalent of sending a 0xFF command.

Only one frame is needed: read “ROM” 0x3F 0x--.

Table 4. Frame 1: read (ROM) 0x3F 0x--

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	1	1	1	1	1	1	1	1
DATA1	X(1)	X	X	X	X	X	X	X
	0	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X	X
	0	0	0	0	0	0	0	0

1. *X = do not care. At least one of these bits must be zero, as 0xFFFF frame is not allowed.*

The entry to the Fail Safe mode can occur due to the CSN timeout.
In this specific case, the following procedure must be executed to leave the fail-safe mode:

- Removing the cause of the CSN stuck
- Toggling the CSN pin for a min t_{SHCH} (time to release the SDO line), see parameter in Table 53
- Sending the SPI frames

If the above procedure is not respected, the first SPI frame will be rejected and the state transition will fail.

Transition from fail-safe mode to normal mode is performed by two special SPI sequences

- Frame 1: write “CTRL”0x4000
- Frame 2: write “CTRL”0x0800

Table 5. Frame 1 (write CTRL0x4000)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	Not Used	Not Used	EN	PWM_ TRIG	Not Used	Not Used
	0	1	0	0	0	0	0	0
DATA2	LOCKbit5	LOCKbit4	LOCKbit3	LOCKbit2	LOCKbit1	LOCKbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	0

Table 6. Frame 2 (write CTRL0x0800)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	Not Used	Not Used	EN	PWM_TRIG	Not Used	Not Used
	0	0	0	0	1	0	0	0
DATA2	LOCKbit5	LOCKbit4	LOCKbit3	LOCKbit2	LOCKbit1	LOCKbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	0

Transition from normal mode to pre-standby mode using SPI: two frames needed

- Frame 1: write “CTRL”0x4800
- Frame 2: write “CTRL”0x8000

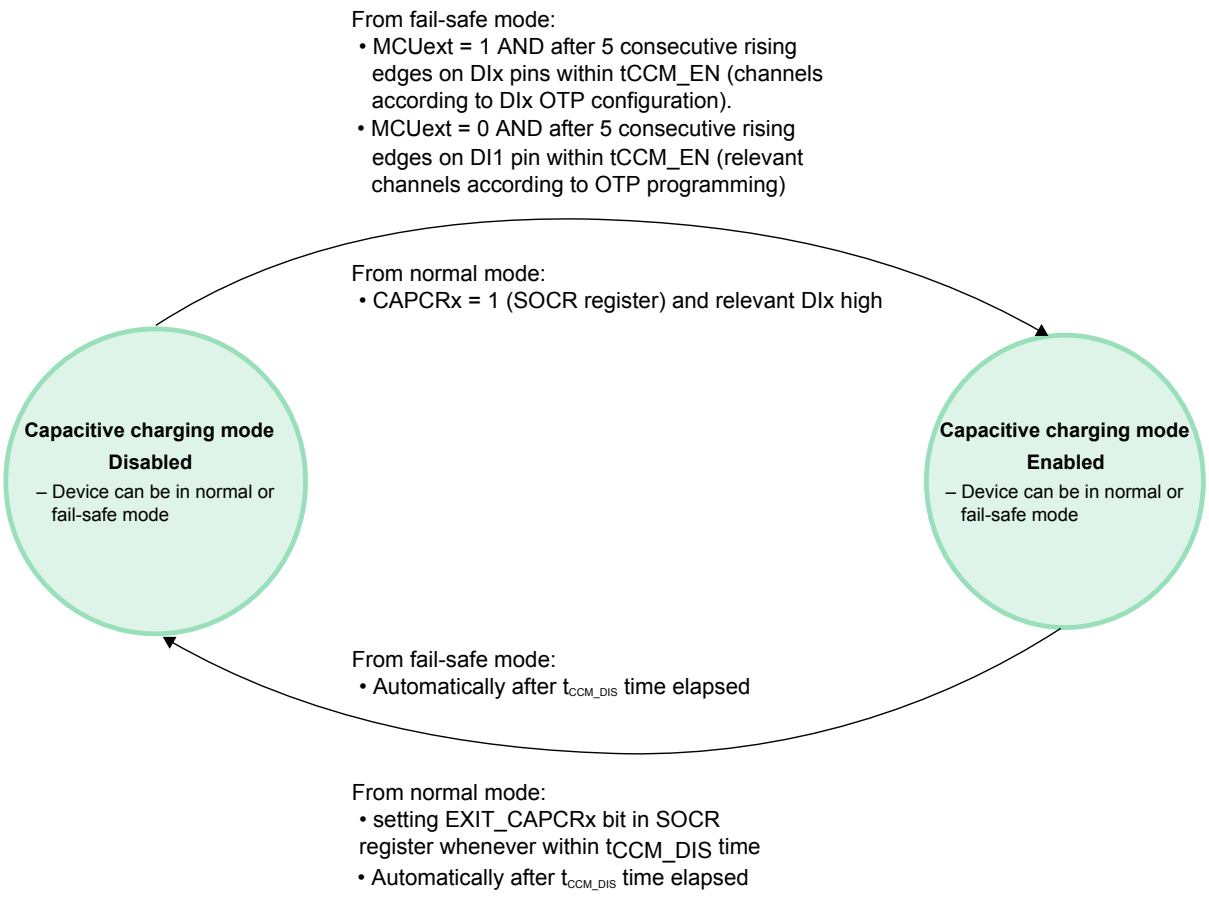
Table 7. Frame 1 (write CTRL 0x4800) - Normal mode to pre-standby mode

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	Not Used	Not Used	EN	PWM_TRIG	Not Used	Not Used
	0	1	0	0	1	0	0	0
DATA2	LOCKbit5	LOCKbit4	LOCKbit3	LOCKbit2	LOCKbit1	LOCKbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	0

Table 8. Frame 2 (write CTRL 0x8000)–Normal mode to pre-standby mode

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	1	0	1	0	0
DATA1	GOSTBY	UNLOCK	Not Used	Not Used	EN	PWM_ TRIG	Not Used	Not Used
	1	0	0	0	0	0	0	0
DATA2	LOCKbit5	LOCKbit4	LOCKbit3	LOCKbit2	LOCKbit1	LOCKbit0	PWMSYNC	Parity
	0	0	0	0	0	0	0	0

Figure 4. Channel state diagram (CCM)



3 Protections

3.1 Thermal case temperature monitoring and pre-warning

Case-temperature is constantly monitored via a 10-bit ADC converter and data is available in the dedicated status register (thermal sensor voltage register, address 0x31h).

Three different thermal warnings TW1, TW2, TW3 will be mirrored in all the OUTSRx status registers (addresses from 0x20h to 0x23h), referring to 120 ºC, 130 ºC and 140 ºC frame temperature thresholds, respectively. On top of that, the content of TW1 bit is reflected in the Global Status Byte (bit1 – T_{CASE}). This bit is set if the frame temperature is greater than the threshold (120 ºC) and can be used as a global temperature pre-warning. The bit is cleared automatically when the frame temperature drops below the case-temperature reset threshold (T_{CR1}).

3.2 Junction overtemperature (OT)

If the junction temperature of a channel rises above the shutdown temperature T_{TSD}, an overtemperature (OT) event is detected.

The channel is switched OFF and the corresponding bit (CHFBSRx Channel Feedback Status Register) is set in the Address OUTSRx register. As a consequence, the thermal shutdown bit (TSD/PL, bit 4) in the Global Status Byte and the Global Error Flag are set.

In Normal Mode, each output channel can be either set in latched OFF or time limited auto-restart operation in case of a junction over temperature event.

- In latched OFF operation: the output remains switched OFF until the junction temperature falls below the reset threshold T_R. In order to restart the channel, after elapsing of restart delay time ($t_{D\_RESTART}$), the MCU shall reset the latch-off event by refreshing the programmed value in the dedicated register (CHLOFFTCR1 or CHLOFFTCR0). The action will clear the corresponding CHLOFFSR bit in Output Status Register OUTSRx and the bit 4 (TSD/PL bit) in the Global Status Byte.
- In time limited auto-restart operation: during the programmed time, the output is switched off as described and switches on again automatically when the junction temperature falls below the reset temperature T_R and restart delay time ($t_{D\_RESTART}$) is elapsed. In order to allow asynchronous diagnostic, the status bit is latched during OFF state of the channel and it is automatically cleared when the junction temperature falls below the thermal reset temperature (T_{RS}) of OT detection. It has to be mentioned that the time limited auto-restart ($t_{BLANKING}$) and restart delay time ($t_{D\_RESTART}$) are contemporarily running, so in case $t_{BLANKING}$ is programmed with a smaller value as $t_{D\_RESTART}$ the channel will stay latched-off after the first OT intervention. After the programmed time has elapsed, the output remains switched OFF and acts as latch-off mode.

In fail-safe mode the channel works in auto-restart mode with restart delay time $t_{D\_RESTART}$ after each OT event.

Figure 5. Normal mode, short circuit - $t_{BLANKING} > t_{D\_RESTART}$

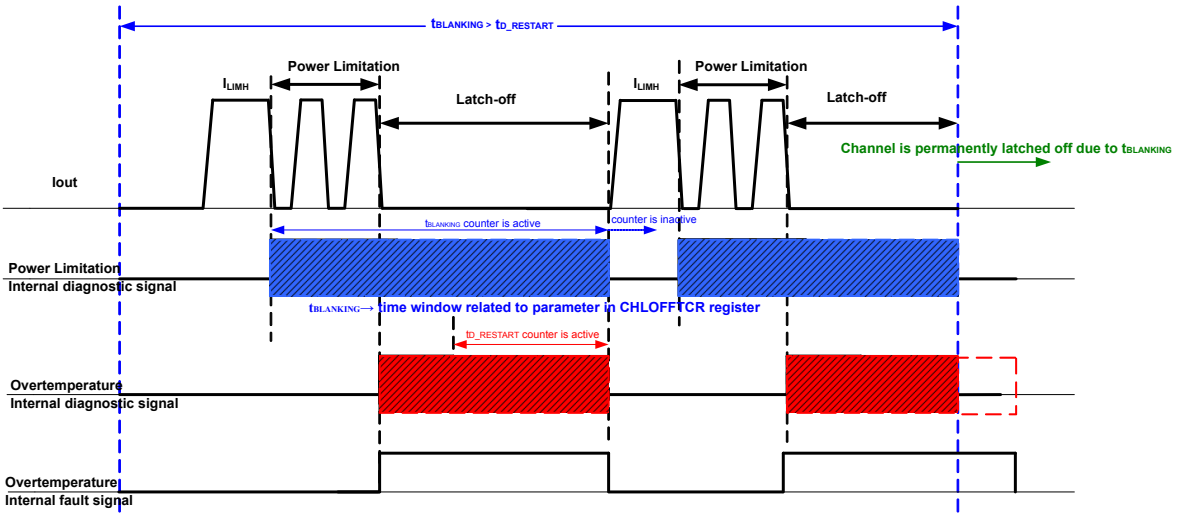
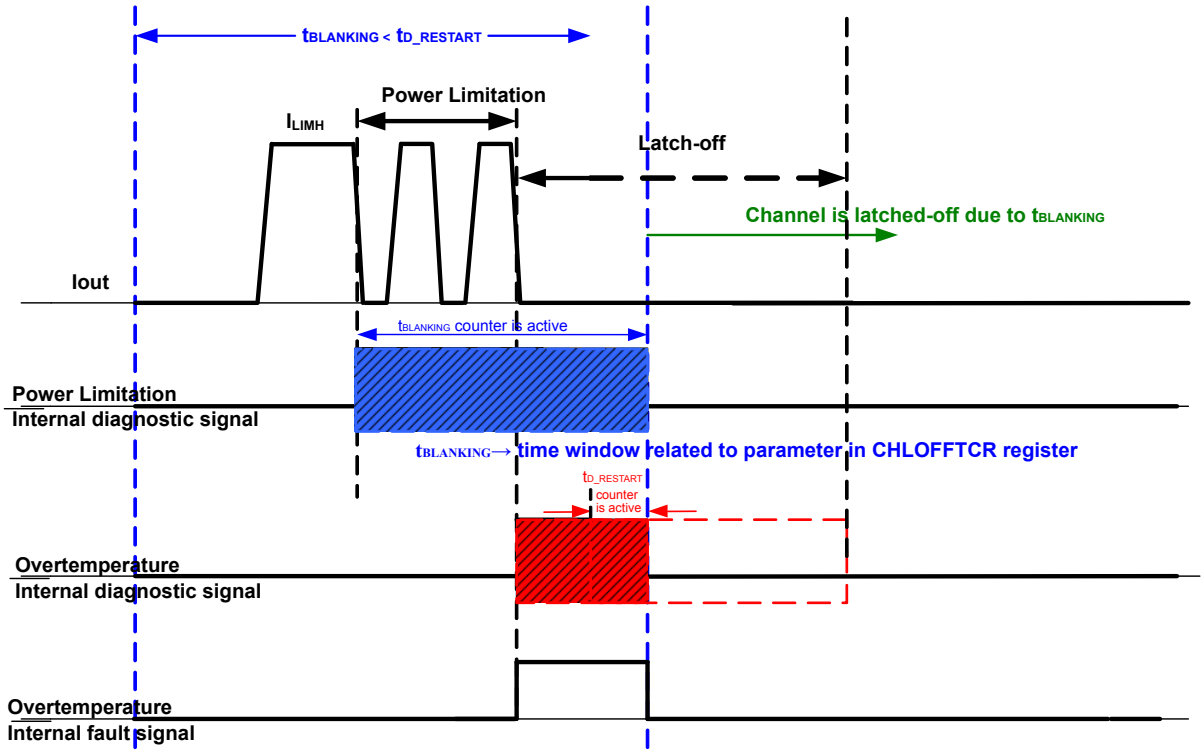


Figure 6. **Normal mode, short circuit - $t_{BLANKING} < t_{D\_RESTART}$**



3.3 Power limitation (PL)

If the difference between junction temperature and case temperature ($\Delta T = T_J - T_C$) rises above the power limitation threshold ΔT_{PLIM}, a power limitation event is detected.

The corresponding bit in the OUTSRx register - Channel Feedback Status bit (CHFBSR) - is set. The channel is switched OFF and therefore the power limitation bit (TSD/PL, bit 4) in the Global Status Byte and the Global Error Flag are set.

In normal mode, each output channel can be either set in latched OFF or time limited auto-restart operation in case of a power limitation event.

- In latched off operation: the output remains switched OFF until the difference between junction temperature and case temperature ($\Delta T = T_J - T_C$) decreases below ΔT_{PLIMR}. In order to restart the channel, the MCU shall reset the latch-off event by refreshing the programmed value in the dedicated register (CHLOFFTCR1 or CHLOFFTCR0). The action will clear the corresponding CHLOFFSR bit in the Output Status Register OUTSRx and bit 4 (TSD/PL) in the Global Status Byte.
- In time limited auto-restart: during the programmed time, the output is switched off as described and switches on again automatically when the difference between junction temperature and case temperature ($\Delta T = T_J - T_C$) decreases below Δ_{TPLIMR}. In order to allow asynchronous diagnostic, the status bit is latched during OFF-state of the channel and it is automatically cleared when the difference between junction temperature and case temperature ($\Delta T = T_J - T_C$) decreases below ΔT_{PLIMR}. After the programmed time has elapsed, the output remains switched OFF and acts as in latch-off mode.
- In Fail Safe mode the channel works in auto-restart mode.
- To improve the performances vs load compatibility test, ΔT_{PLIM} value is set at 80°C for V_{CC} < 17.5 V, whilst it is set at 55 °C for V_{CC} > 17.5 V.
- In capacitive charge mode (CCM) ΔT_{PLIM}=ΔT_{PLIM_CCM}=30°C.

3.4 Overload protection–Output current limitation (I_{LIMH})

In case of soft overload leading a channel to any output current level (including current limitation) with an output voltage above the current sense shutdown threshold, the programmed I^2t curve will be still verified by the implemented algorithm.

In the event of a hard short-circuit or heavy overload, the device immediately triggers the hardware current limitation (I_{LIMH}). During this state, the Current Sense might be disabled if $V_{OUT} < V_{OUT\_FSD}$; consequently, the digital I^2t algorithm doesn't follow the I_{OUT}, but the related counter is updated at the maximum speed when the embedded power is active (see Section 3.5). Wire harness protection is then managed exclusively by the hardware shutdown mechanism, according to the I_{LIM_LATCHx} register configuration.

On top of that, the device output current is clamped to the current limitation threshold (I_{LIMH}).

The device behavior in current limitation can be set by a dedicated OTP bit (ILIM_LATCHx) - 1x channel:

- If ILIM_LATCHx = 1: channel is switched off (after t_{FILTER_OL}) and latched. In order to restart the channel, the MCU shall reset the latch-off event by refreshing the programmed value in the dedicated register (CHLOFFTCR1 or CHLOFFTCR0). The action will clear the corresponding CHLOFFSR bit in Output Status Register OUTSRx and bit 4 in the Global Status Byte.
- If ILIM_LATCHx = 0: channel is set in auto-restart mode, allowing power limitation.

3.5 Electronic harness protection (STi²Fuse)

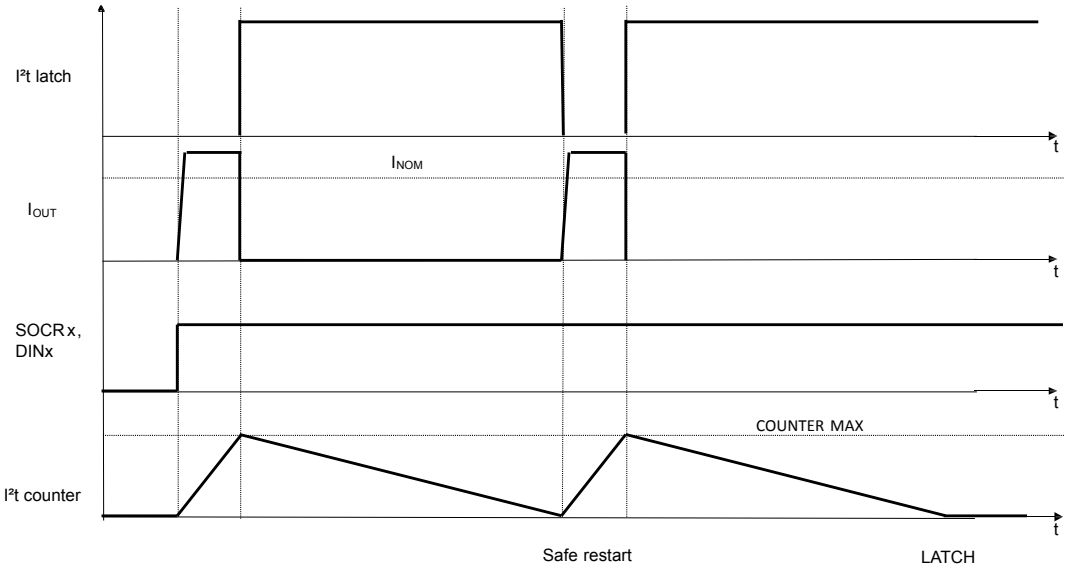
The VNF9Q20SF embeds the STMicroelectronics proprietary I²t functionality, featuring an intelligent circuit breaking aimed at protecting PCB traces, connectors and wire harness from overheating, with no impact on load transients like inrush currents and capacitance charging. The electronic wire harness protection, I²t protection, is active in all operating modes, except in:

- Standby mode when the device is in the lowest quiescent current consumption mode and all analog and digital functions are in idle mode and output stages are off. Also, when a channel is in CCM, capacitive charging mode, the I²t protection on that specific channel is disabled.
- In CCM mode the wire harness remains in any case fully protected, since CCM mode is the latest aborted after t_{CCM_DIS} with low RMS current.
- In LED mode, when the channel is operating in high R_{DSON} and low current limitation mode. In this case, the wires are protected by the intrinsic thermal I-t capability of the device.
- In reverse battery condition when outputs are automatically activated.

In all other conditions, the wire harness protection is active and works fully autonomous and in particular does not require any MCU control or supervision. The I²t protection functionality is equipped with specific safety mechanism such as built-in self-tests (BIST) for the current sense block responsible for acquiring the load current and the I²t block itself, which makes this function ASILx ready. In the ITCNTSR register the current value of the integrated I²t budget is reported and allows the application to monitor how much of the available I²t budget is actually consumed.

At each POR an internal flag Safe_Restart is set. This flag allows the device to automatically restart after first harness protection triggering, then the Safe_Restart flag is reset (see Figure 7. I²t counter: single Safe_Restart after POR with $I_{OUT} > I_{NOM}$).

Figure 7. I²t counter: single Safe_Restart after POR with $I_{OUT} > I_{NOM}$



The I²t protection is based on a continuous RMS output current calculation. The current sense for I²t calculation is sampled for each channel every $1/f_{CLK}$ with linearity ensured up to I_{LIMH}. Since the current sense block is not active in the hard short circuit condition or whenever the output voltage drops below the current sense shutdown threshold (V_{OUT_FSD}), the behavior of the channel when in current limitation is programmable (see Section 3.4: Overload protection–Output current limitation (I_{LIMH})).

In the case ILIM_LATCHx is programmed in latch-off mode, the current sense, and consequently the I²t protection function are always active when output is on (for the exceptions see above).

In case ILIM_LATCHx is programmed in auto-restart mode, the current sense, and consequently the I²t protection function are active as long as the output voltage remains above the current sense shutdown threshold (V_{OUT_FSD}). As soon as the output voltage drops below the current sense shutdown threshold (V_{OUT_FSD}), for example through a hard short circuit, the current sense is inhibited. To guarantee safety in this condition, the device triggers an emergency fail-safe: the I^2t algorithm bypasses normal current readings and increments the internal thermal counter at its maximum theoretical speed. Concurrently, the hardware power limitation mechanism restricts the RMS current to a safe minimum, ensuring effective and rapid protection for the wire harness.

The shape of the actual I²t protection curve is a staircase curve, which is determined by two configurable parameters, I_{NOM} and t_{NOM}. Both parameters are accessible through the SPI FSITCRx register, read-and writeable.

Nominal time t_{NOM}

The default t_{NOM} parameter is programmed by 3 OTP bits (TNOM0, TNOM1, TNOM2, for each channel).

Its default value is 300 s.

Table 9. Nominal time

Nominal time value	TNOM2	TNOM1	TNOM0
300 s (default)	0	0	0
257 s	0	0	1
214 s	0	1	0
172 s	0	1	1
129 s	1	0	0
86 s	1	0	1
44 s	1	1	0
1 s	1	1	1

Nominal current I_{NOM}

The default I_{NOM} parameter is programmed by 3 OTP bits (INOM0, INOM1, INOM2, for each channel).

Its default value is 6 A.

Table 10. Nominal current

Nominal current value	INOM2	INOM1	INOM0
1.5 A	0	0	1
2 A	0	1	0
2.5 A	0	1	1
3 A	1	0	0
3.5 A	1	0	1
4 A	1	1	0
5 A	1	1	1

Nominal current value	INOM2	INOM1	INOM0
6 A (default)	0	0	0

Note: In parallel mode, the I²t protection function is available. In this case, the configuration data are applied only to CH0. Effectively the I_{NOM} value is doubled.

The value of I_{NOM} represents the level of steady state current, which can be accepted for infinite time in the system consisting of IC, routing, connectors, wiring, and load. The value of t_{NOM} specifies how fast the staircase curve reaches the I_{NOM} value.

The Figure 8 depicts the I²t staircase protection curve with a configuration of I_{NOM} = 4 A and t_{NOM} = 300 s and for comparison the I-t isothermic curve of a wire with 0.13 mm^2 cross section at T_A = 85 °C heating up to 150 °C. It can be seen that the I²t staircase protection curve is always left below the wire isothermic curve, which means the I²t protection algorithm protects the wire from carrying an RMS current, which would lead to a higher temperature increase than the one of the isothermic curve.

CH0 and CH1 can be paralleled by setting a specific bit in the OTP memory map. In this case only the configuration data of channel 0 applies and the value of I_{NOM} is effectively doubled while R_{DSon} is effectively halved.

Figure 8. Protection curve with I_{NOM} = 4 A and t_{NOM} = 300 s vs a 0.13 mm^2 wire isothermic curve

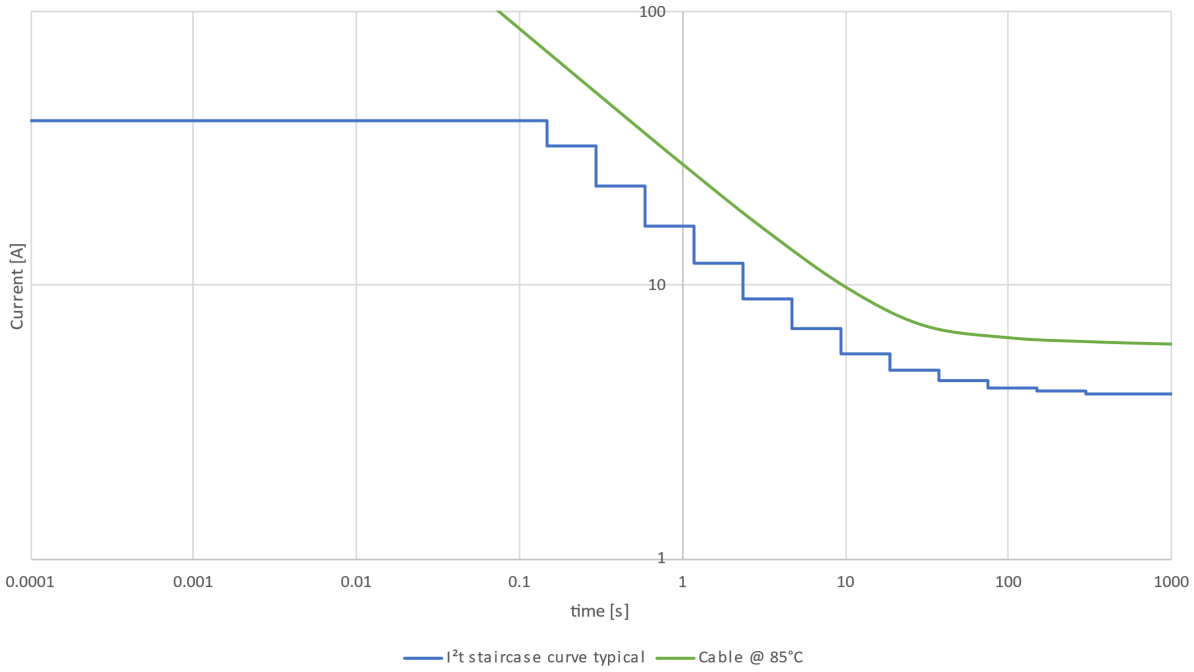
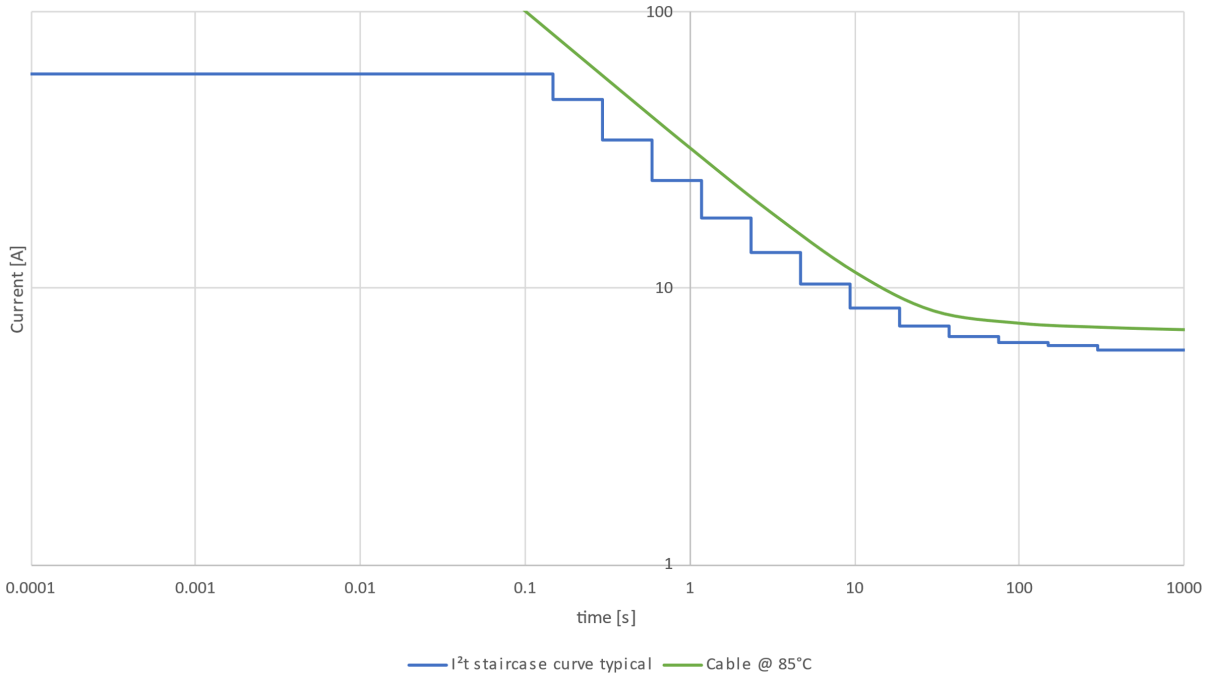
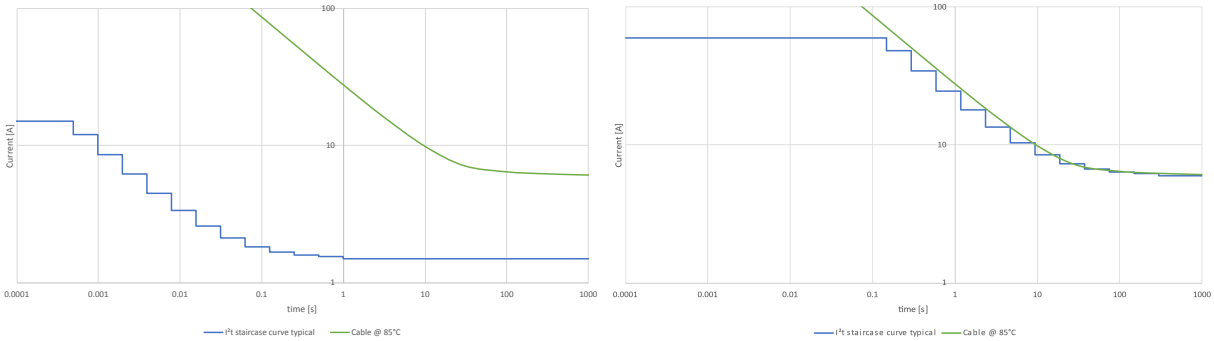


Figure 9. Protection curve in parallel mode with I_{NOM} = 6 A and t_{NOM} = 300 s vs a 0.17 mm² wire isothermic curve



The I²t protection curve can be moved in y-direction by changing the I_{NOM} value and in x-direction changing the t_{NOM} value. The following figure represents the total range of I²t the device can cover, ranging from I_{NOM_MIN} = 1.5 A with t_{NOM_MIN} = 1 s up to I_{NOM_MAX} = 6 A with t_{NOM_MAX} = 300 s.

Figure 10. Lowest I_{NOM} and t_{NOM} (left hand) and highest I_{NOM} and t_{NOM} (right hand) configuration setting



Note: In the highest configuration settings, a 0.13 mm² wire is not protected as the I²t staircase curve intersects with the isothermic curve of the wire.

The I²t protection curve consists of 13 steps, each of them corresponding to a specific current threshold. Whenever the load current exceeds a threshold, a counter is counting up. If for instance looking at the example in Figure 8, the current would exceed the value of I_{NOM} = 4 A, but stay below the current threshold of the next step, which is set at 1.03* I_{NOM} about, the counter would reach its threshold value after t_{NOM} = 300 s, the harness protection is triggered and the output channel is automatically latched off.

Diagnostic about I²t intervention is available through SPI with the ITOFFSRx bit in the OUTSRx output status register and bit 3 in the global status byte. Both bits are set when the output channel is latched off for wire harness I²t protection. An additional diagnostic indication is available, depending on the configuration of MCUext bit in the OTP memory area. The following table explains the functionality of DIx pins depending on the MCUext bit setting.

Table 11. DIx pin functionality

MCUext bit	DI0	DI1
0	Global I²t status (active low) OR combination of all channels	Global I²t unlatch pin for all channels (active high)
1 (default)	Direct input	Direct input

In case MCUext = 0, DI0 acts as an open drain global I²t status pin with an OR combination of all channels. The DI0 pin is active low, in case at least one channel has latched off for wire harness I²t protection. The I²t latch can be cleared by clearing:

- The ITOFFSRx bit through R&C command

Or

- Low to high transition on DI1 pin, it remains at high level for at least $t_{F\_UNLATCH}$, then pulls low DI1 pin. If more than one channel is latched for wire harness I²t protection, this unlatches all channels at the same time.

Consequently, bit 3 in the global status byte is cleared and the channel is restarted. The I²t counter is NOT reset, it keeps its actual value reached during down-counting while the channel was latched.

In the case MCUext = 0, both possibilities for unlatching are available in normal mode and fail-safe mode. However, ITOFFSRx bit and bit 3 in the global status byte is cleared only through the R&C command.

In case MCUext = 1, diagnostic and unlatch control is available only through SPI; however, in fail-safe mode wire harness I²t protection is in auto-restart mode, unlatching the channel when the I²t counter counted down to 0.

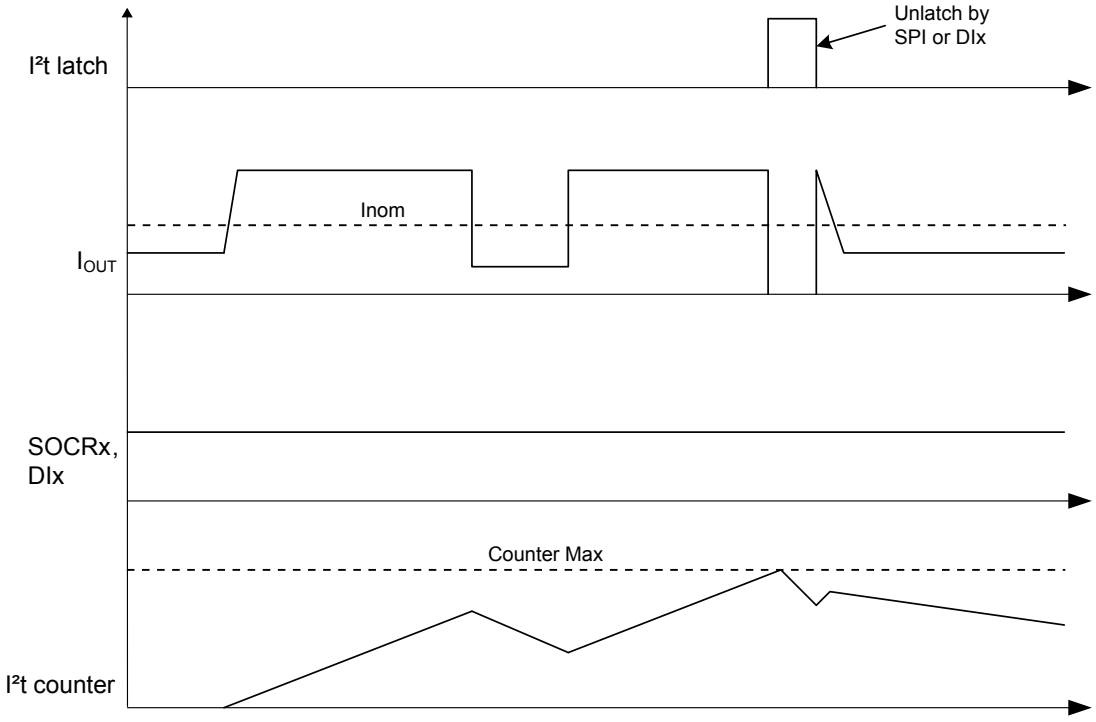
The speed of the counter up-counting (fixed drop, refer to Table 12) is increased every time the load current reaches the next staircase current threshold of the I²t curve. Every time the load current drops below the I_{NOM} threshold the counter is decreasing. The speed of the down-counting depends on how far the load current is below the I_{NOM}. This algorithm perfectly emulates a continuous RMS (root mean square) current integration, which in fact is the proper indicator to measure the losses in the wire by Joule effect, causing the temperature rise in the wire.

Table 12. FIXED_DROP table

FIXED_DROP(m)	I_{OUT} range
16	$0.25*I_{NOM} \div 0$
8	$0.5*I_{NOM} \div 0.25*I_{NOM}$
4	$0.75*I_{NOM} \div 0.5*I_{NOM}$
1	$I_{NOM} \div 0.75*I_{NOM}$

The concept of up and down-counting for RMS current control is illustrated in the figure below:

Figure 11. **I²t counter with varying I_{NOM} latch and unlatch**



The last (13th) step of the I²t protection staircase curve is equal to 10 * I_{NOM}. Whenever the load current exceeds the 13th threshold, the output channel is latched off immediately within t_{doff} + t_f, protecting the integrity of the board net power supply.
The I²t block is supplied from an internal voltage regulator supplied by V_{REG}. Therefore, as soon as V_{REG} drops below $V_{REG\_POR\_L}$, the accumulated I²t counter value is reset and the device enters in sleep mode.

Figure 12. **I²t counter after POR with I_{OUT} > I_{NOM}**

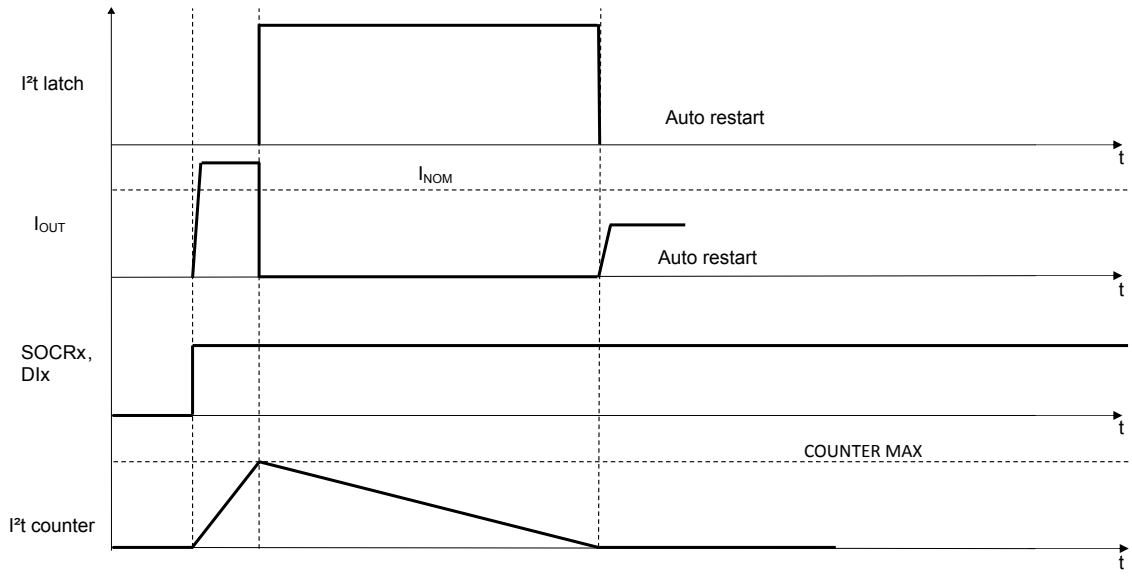
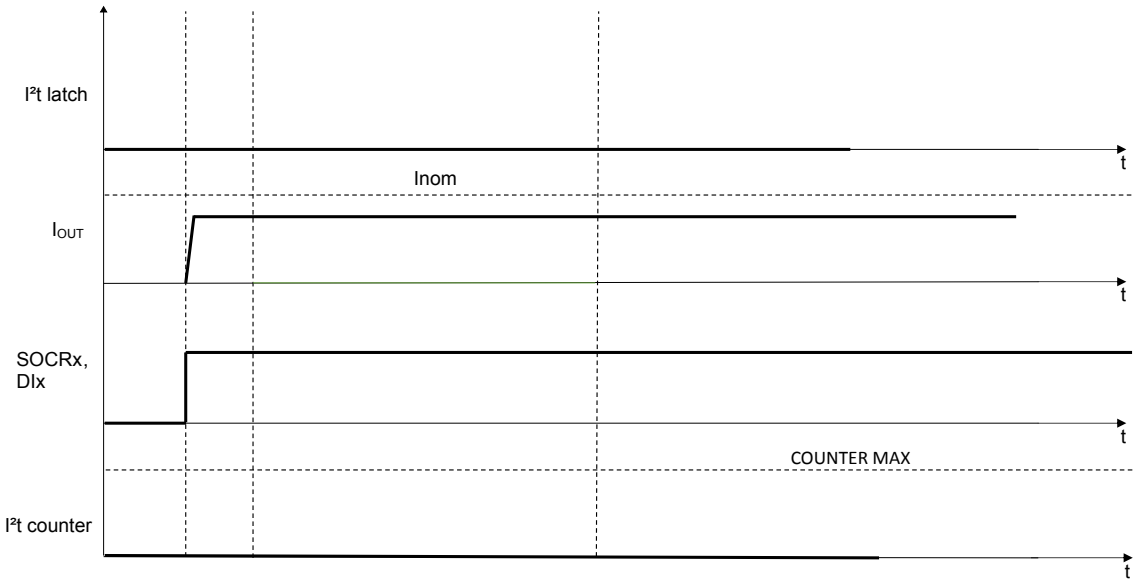
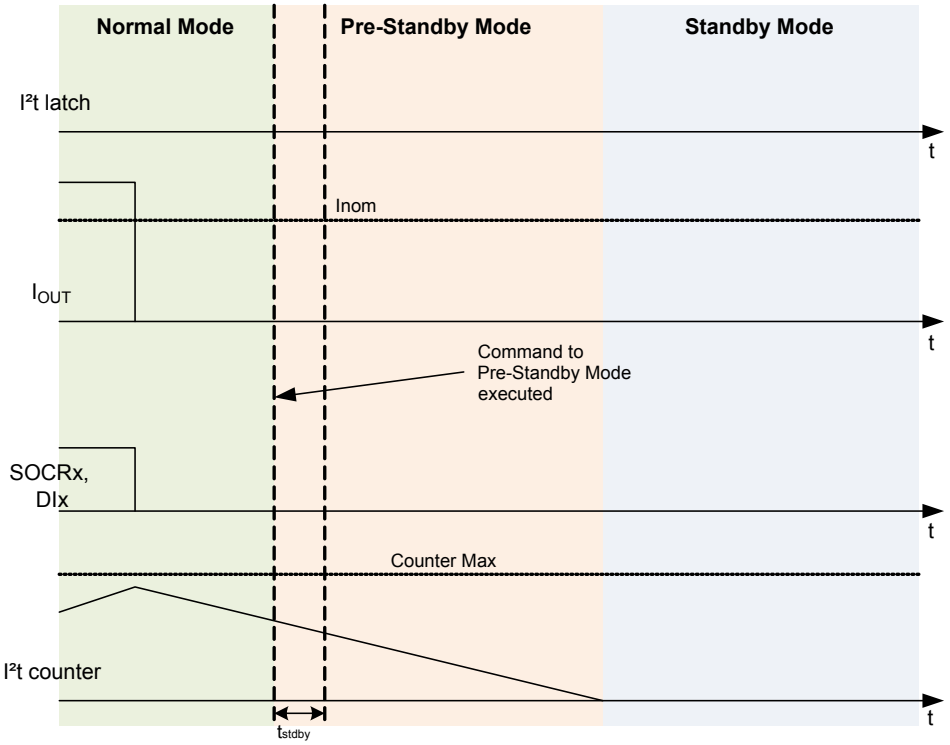


Figure 13. **I²t counter after POR with $I_{OUT} < I_{NOM}$**



The transition from pre-standby mode to standby mode requires all channels I²t counters have counted down to 0 (see Figure 14).

Figure 14. **Transition to standby mode with I²t counter running**



3.6 Programmable shut-off

A programmable shut-off current threshold is implemented to switch off the channel within 100 µs upon overcurrent detection. The seven output current thresholds are proportional to the chosen harness protection I_{NOM}, according to shut-off current threshold = M_x * I_{NOM}.

The possible threshold multiplier can be chosen between seven multiplier M_x. Changing the I_{NOM}, the selected multiplier factor does not change, but it results in a different overcurrent threshold.

The multiplier default value corresponds to a function disabled. In this case the I_SHUTOFF protection is not active. Three additional OTP bits for each channel are reserved to set the default value of the I_SHUTOFF threshold multiplier.

Table 13. OTP multiplier

Multiplier	ITHRx(2)	ITHRx(1)	ITHRx(0)
M_1	0	0	1
M_2	0	1	0
M_3	0	1	1
M_4	1	0	0
M_5	1	0	1
M_6	1	1	0
M_7	1	1	1
Disabled (default)	0	0	0

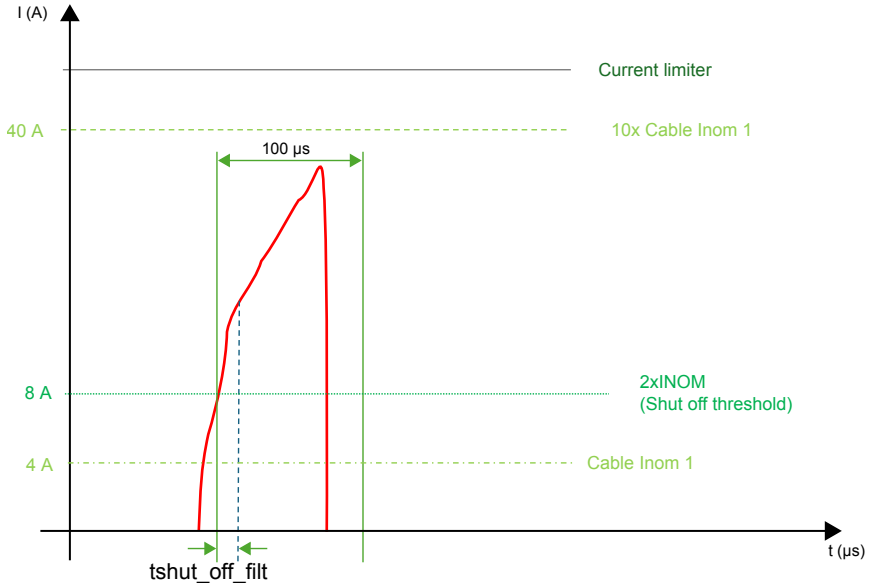
Three dedicated bits for each channel (ISHUTOFFCR2x, ISHUTOFFCR1x, ISHUTOFFCR0x) in the relevant register FSITCRx can be set for on-demand programming, to change the default configuration (valid only in normal mode, while in fail-safe mode it is reverted to the OTP settings).

Table 14. Detection threshold multiplier

Threshold multiplier	ISHUTOFFCR2x	ISHUTOFFCR1x	ISHUTOFFCR0x
M_1	0	0	1
M_2	0	1	0
M_3	0	1	1
M_4	1	0	0
M_5	1	0	1
M_6	1	1	0
M_7	1	1	1
Disabled (default)	0	0	0

Since the detection is filtered for a fixed time, the shut-off protection acts if the output current maintains a level greater or equal to the selected threshold for a minimum time "tshut_off_filt", then the channel turns off within the maximum 100 µs. The output current can evolve freely within the 100 µs time frame (see the following figure).

Figure 15. **Output current profile within 100 µs time frame**



When *Iload* > *I_shut-off current threshold* for a time greater than an internal filtering time (tshut_off_filt), the counter is set immediately to the CounterMAX value and the channel is latched off, bit ISHUTOFFSRx and bit ITOFFSRx in the relevant OUTSRx register are set high. A R&C command (the same algorithm relating to 13th level detection of harness protection) is needed on bit ITOFFSRx to unlatch the channel, and on bit ISHUTOFFSRx to reset the information.

The overcurrent detection may only be effective in case of overloads ($V_{OUT} > V_{OUT\_FSD}$). Terminal short circuit (output stuck to ground) is limited by the current limitation threshold.

The I_SHUTOFF protection diagnostic is reported also inside the GSB. The ITLOFF bit is a logical OR combination of I²t latch and programmable ISHUTOFF for each channel.

MCUext = 1 (Default)

The bit ISHUTOFFSRx (active high) and the bit ITOFFSRx (active high) in the relevant channel status register OUTSRx indicate if the programmable shut-off latch is active, or it has been activated, since the last R&C command.

When ISHUTOFFSRx is set the I²t protection is triggered too. A R&C command on the relevant OUTSRx register is sufficient to reset a latch-off condition (ITOFFSRx reset), both in normal mode and fail-safe mode.

The ISHUTOFFSRx bit is a notification bit, so the channel is able to turn on also even if it is active. A R&C command is required to reset the information.

After the ITOFFSRx bit has been cleared, the corresponding channel latch is removed, and the channel is commanded according to its setting. The counter is not reset.

MCUext = 0

The DI0 pin turns into a diagnostic output acting as an open drain pin for global diagnostics, including shut-off diagnostics. The DI1 pin is used as the F_CTRL pin to unlatch all channels at once (active high for at least 20 µs and then pulled low) from both I²t and I_SHUTOFF latches. It is not linked to the control of the latch condition for thermal events. Thermal latching event has its own dedicated reset

All protections work in parallel, so the most restrictive one intervenes independently of the others.

3.7 Reverse battery turn-on

In the reverse battery condition, the outputs are automatically activated and all protections are not active.

The self turn-on feature cannot be disabled.

4 SPI functional description

4.1 SPI communication

The SPI communication is based on a standard ST-SPI 24-bit interface, using CSN, SDI, SDO and SCK signal lines.

Input data are shifted into SDI, MSB first while output data are shifted out on SDO, MSB first.

4.1.1 Signal description

During all operations, V_{DD} must be held stable and within the specified valid range: V_{DD} min to V_{DD} max. The V_{REG} must be held stable and within the specified range, V_{REG} min to V_{REG} max, to supply the digital part.

Table 15. SPI signal description

Name	Function
Serial clock SCK	This input signal provides the timing of the serial interface. Data present at serial data input (SDI) are latched on the rising edge of the serial clock (SCK). Data on serial data output (SDO) change after the falling edge of the serial clock (SCK freq > 1 MHz).
Serial data input SDI	This input signal is used to transfer data serially into the device. It receives data to be written. Values are sampled on the rising edge of the serial clock (SCK).
Serial data output SDO	This output signal is used to transfer data serially out of the device. Data are shifted out on the falling edge of the serial clock (SCK).
Chip select CSN	When this input signal is high, the device is deselected and serial data output (SDO) is high-Z. Driving this input Low enables the communication. The communication must start on a Low level of serial clock (SCK). Data are accepted only if exactly 24 bits have been shifted in. *Note: As per the ST_SPI standard, in the case of failing communication:* • *CSN stuck at HIGH:* – *If the device is in normal mode, a WDTB timeout forces the device into fail-safe mode. The serial data out (SDO) remains in high impedance (high-Z). Any valid communication arrived after this event is accepted by the device.* • *CSN stuck at LOW:* – *In this case and whatever the mode of the device, a CSN timeout protection is activated and force the device to release the SPI bus. Then the serial data out (SDO) will go into high impedance (high-Z)* A reset of the CSN timeout (see t_{SHCH} in Table 53) is activated with a transition Low to high on the CSN pin (or with a power on reset or software reset). With this reset, the serial data out (SDO) is released and any valid communication is accepted by the device. Without this reset, the next communication is not considered by the device.

4.1.2 Connecting to the SPI bus

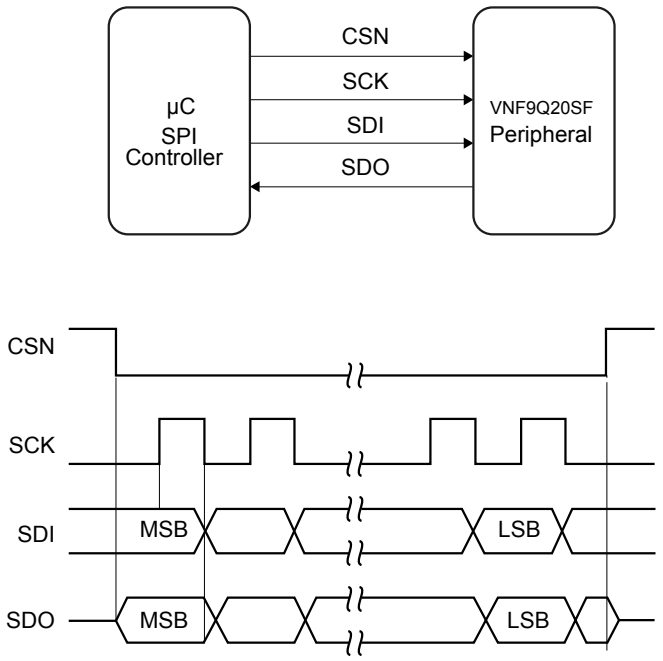
A schematic view of the architecture between the bus and devices can be seen in the Figure 17.

All input data bytes are shifted into the device, MSB first. The serial data input (SDI) is sampled on the first rising edge of the serial clock (SCK) after chip select (CSN) goes low. All output data bytes are shifted out of the device on the falling edge of SCK, MSB first on the first falling edge of the chip select (CSN).

4.1.3 SPI mode

Supported SPI mode during a communication phase can be seen in the following figure:

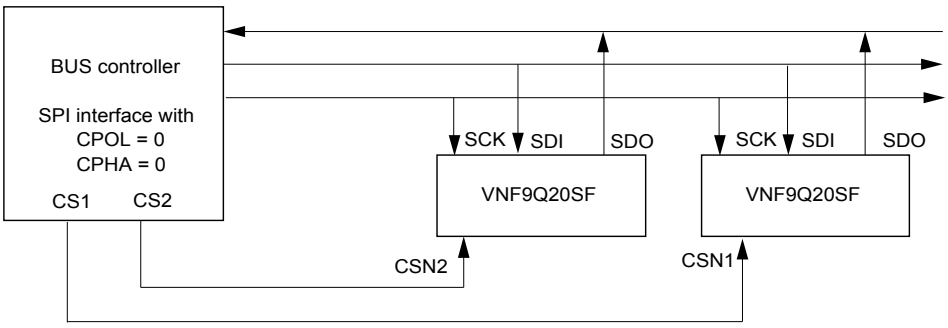
Figure 16. Supported SPI mode



This device can be driven by a microcontroller with its SPI engine running in the following mode:

- CPOL = 0, CPHA = 0

Figure 17. Bus master and two devices in a normal configuration



4.2 SPI protocol

4.2.1 SDI, SDO format

SDI format during each communication frame starts with a command byte. It begins with two bits of operating code (OC0, OC1) which specify the type of operation (read, write, read and clear status, read device information) and it is followed by a 6-bit address (A0:A5). The command byte is followed by two input data bytes (D15:D8) and (D7:D0).

Table 16. Command byte

MSB							LSB
OC1	OC0	A5	A4	A3	A2	A1	A0

Table 17. Input data byte 1

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 18. Input data byte 2

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0[1]

1. *D0 is the parity bit.*

SDO format during each communication frame starts with a specific byte called Global Status Byte (see GSB byte for more details of bit0-bit7). This byte is followed by two output data bytes (D15:D8) and (D7:D0).

Table 19. Global status byte

MSB							LSB
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

Table 20. Output data byte 1

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 21. Output data byte 2

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

4.2.2 Operating code definition

The SPI interface features four different addressing modes which are listed in Table 22:

Table 22. Operating codes

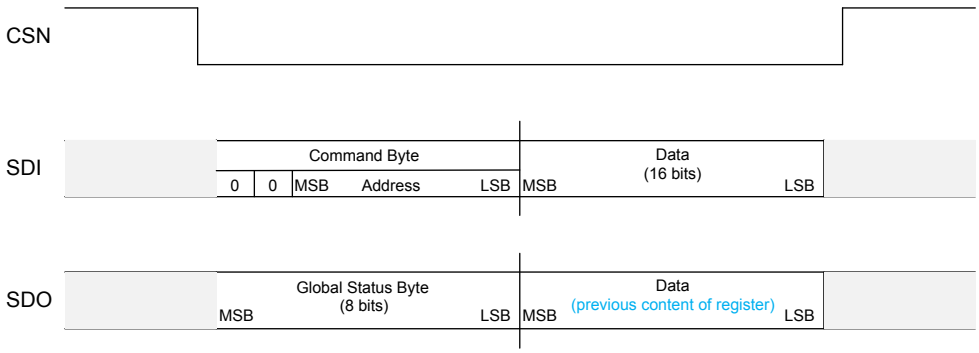
OC1	OC0	Meaning
0	0	Write operation
0	1	Read operation
1	0	Read and clear status operation
1	1	Read device information

Write mode

The write mode of the device allows to write the content of the input data byte into the addressed register (see list of registers in Table 27). Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

During the same sequence the outgoing data are shifted out MSB first on the falling edge of the CSN pin and the subsequent bits on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte and the second to the previous content of the addressed register.

Figure 18. **SPI write operation**



Read mode

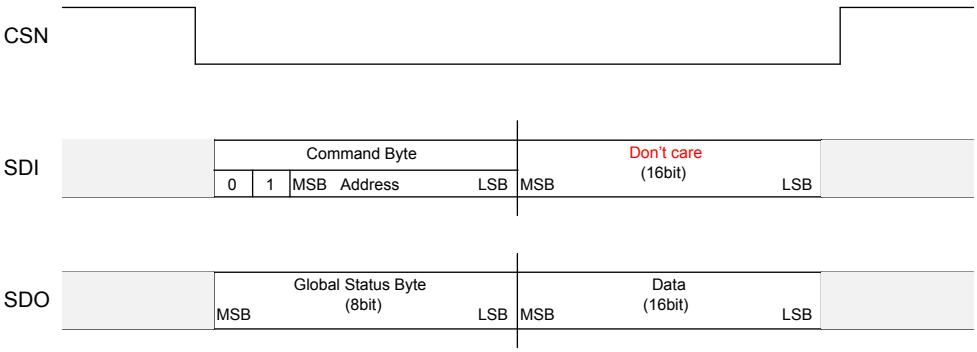
The read mode of the device allows to read and to check the state of any register. Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

The command byte allows to determine which register content is read, whilst the other two data bytes are "don't care".

In case of a read mode on an unused address, the global status/error byte on the SDO pin is followed by 0x0000 word.

In order to avoid inconsistency between the Global Status byte and the Status register, the Status register contents are frozen during the SPI communication.

Figure 19. **SPI read operation**



Read and clear status command

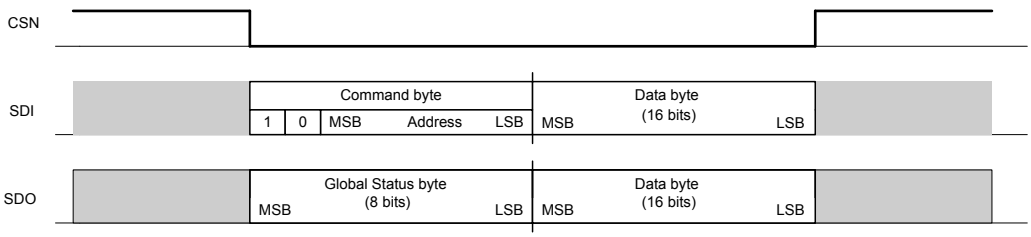
The read and clear status operation is used to clear the content of the addressed status register (see Table 27). A read and clear status operation with address 0x3Fh clears all Status registers simultaneously.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which register content is read and the payload bits set to 1 into the data byte determine the bits into the register which have to be cleared.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte and the second to the content of the addressed register.

In order to avoid inconsistency between the Global Status byte and the Status register, the Status register contents are frozen during SPI communication.

Figure 20. **SPI read and clear operation**



Read device information

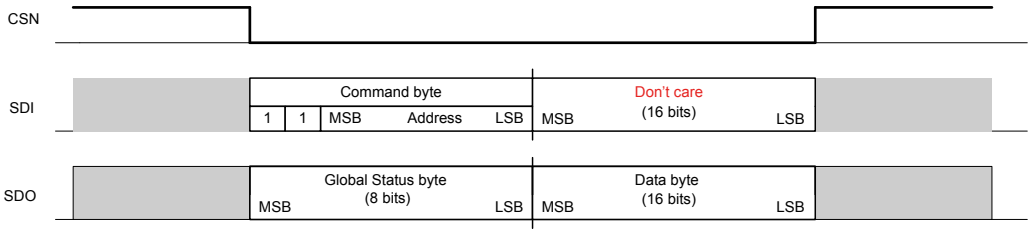
Specific information can be read but not modified during this mode. Accessible data can be seen in Table 28.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which information is read whilst the other two data bytes are "don't care".

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte and the second to the content of the addressed register and the third byte is 0x00.

Note: ROM is based on the 8-bit registers, then even if 16 bits are returned, only the second byte contains the addressed ROM register.

Figure 21. **SPI read device information**



4.2.3 Special commands

0xFF - SW Reset: set all control registers to default (ROM access)

An OpCode '11' (read device information) addressed at '111111' forces a Software Reset of the device, second and third bytes are "don't care" provided that at least one bit is zero.

Note: An OpCode '11' at address '111111' with data field equal to '1111111111111111' on the SPI frame is recognized as a frame error and SPIE bit of GSB is set.

Table 23. **0xFF: SW_Reset**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
1	1	1	1	1	1	1	1
DATA1	X	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

Note: X = do not care.

0xBF - clear all status registers (RAM access)

When an OpCode ‘10’ (read and clear operation) at address b’111111 is performed.

Table 24. Clear all status registers (RAM access)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
1	0	1	1	1	1	1	1
DATA1	X	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

Note: X = do not care.

Note: Reset value = the value of the register after a power on.
Default value = the default value of the register. Currently this is equivalent to the reset value.
Cleared register = explicitly read and clear of the register, if it is not write-protected.

4.3 Register map

The device contains a set of RAM registers used for device configuration, the device status and ROM registers for device identification. Since ST-SPI is used, Global Status byte defines the device status, containing fault information.

4.3.1 Global status byte description

The data shifted out on SDO during each communication starts with a specific byte called global status byte. This one is used to inform the microcontroller about global faults which can happen at channel-side level (that is, like thermal shutdown) or on the SPI interface (like watchdog monitoring timeout event, communication error). This specific register has the following format:

Table 25. Global Status Byte (GSB)

MSB							LSB
GSBN	RSTB	SPIE	TSD/PL	ITLOFF	LOFF	TCASE	FS

Table 26. Global Status Byte

Bit	Name	Reset	Content
7	Global status bit not (GSBN)	0	The GSBN is a logically NOR combination of Bit 0 to Bit 6. This bit can also be used as Global Status Flag without starting a complete communication frame as it is present directly after pulling CSN low.
6	Reset bit (RSTB)	1	The RSTB indicates a device reset. In case this bit is set, all internal Control Registers are set to default and kept in that state until the bit is cleared. The reset bit is automatically cleared by any valid SPI communication
5	SPI error (SPIE)	0	The SPIE is a logical OR combination of errors related to a wrong SPI communication (SCK count and SDI stuck at errors). The SPIE bit is automatically set when SDI is stuck at High or Low. The SPIE is automatically cleared by a valid SPI communication.

Bit	Name	Reset	Content
4	Thermal shutdown (TSD) or power limitation (PL)	0	This bit is set in case of thermal shutdown or power limitation.
3	I²t channel latch-off (ITLOFF)	0	Logical OR combination of STi²Fuse latch and programmable ISHUTOFF for each channel. This bit is set in case of programmable ISHUTOFF or when I²t latches OFF the channels.
2	Latch-off (LOFF)	0	The device error bit is set in case one or more channels are latched OFF
1	Case temperature bit (T_{CASE})	0	This bit is set if the frame temperature is greater than the threshold (120 °C), it can be used as a temperature pre-warning. The bit is automatically cleared when the frame temperature drops below the case-temperature reset threshold (TCR1). (It corresponds to the content of the bit TW1)
0	Fail-safe (FS)	1	The bit is set in case device operates in Fail-safe mode.

Note: The FFh or 00h combinations for the global status byte are not possible, due to the active low of global status bit (bit 7), exclusive combination exists between bit 7 and bit 0 - bit 6. Consequently, a FFh or 00h combination for the global status byte must be detected by the microcontroller as a failure (SDO stuck to GND or to VDD or loss of SCK).

4.3.2 RAM

RAM registers can be separated according to the frequency of usage:

- Init–register is read/written during the initialization phase (single shot action).
- Continuous–read/write/read and clear registers are often accessed, applying outputs control and diagnostic.
- Rare–read/read and clear status of device registers accessed on demand (in case of failure).

Table 27. RAM memory map

Address	Name	Access	Content	Access type	Reset value
Control registers					
00h	OUTCTRCR0	Read/Write	Output control configuration register channel 0	Init	0x0000
01h	OUTCTRCR1	Read/Write	Output control configuration register channel 1	Init	0x0000
02h	OUTCTRCR2	Read/Write	Output control configuration register channel 2	Init	0x0000
03h	OUTCTRCR3	Read/Write	Output control configuration register channel 3	Init	0x0000
Not used area					
08h	OUTCFGR0	Read/Write	Output configuration register 0	Init	0x0000
09h	OUTCFGR1	Read/Write	Output configuration register 1	Init	0x0000
0Ah	OUTCFGR2	Read/Write	Output configuration register 2	Init	0x0000
0Bh	OUTCFGR3	Read/Write	Output configuration register 3	Init	0x0000
Not used area					
10h	CHLOFFTCR0	Read/Write	Channel latch-off timing control register 1 (channels 2, 1, 0)	Init	0x0000
11h	CHLOFFTCR1	Read/Write	Channel latch-off timing control register 0 (Channel 3)	Init	0x0000
13h	SOCR	Read/Write	Channel control register	Init	0x0000
14h	CTRL	Read/Write	Control register	Init	0x0000
15h	FSITCR0	Read/Write	Fail-safe and I²t settings for channel 0	Init	0x0200
16h	FSITCR1	Read/Write	Fail-safe and I²t settings for channel 1	Init	0x0200

Address	Name	Access	Content	Access type	Reset value
17h	FSITCR2	Read/Write	Fail-safe and I²t settings for channel 2	Init	0x0200
18h	FSITCR3	Read/Write	Fail-safe and I²t settings for channel 3	Init	0x0200
Not used area					
STATUS REGISTERS					
20h	OUTSR0	Read/Clear	Output status register Channel 0	rare	0x0000
21h	OUTSR1	Read/Clear	Output status register Channel 1	rare	0x0000
22h	OUTSR2	Read/Clear	Output status register Channel 2	rare	0x0000
23h	OUTSR3	Read/Clear	Output status register Channel 3	rare	0x0000
Not used area					
28h	ADC0SR	Read	Digital current sense Channel 0	continuous	0x0000
29h	ADC1SR	Read	Digital current sense Channel 1	continuous	0x0000
2Ah	ADC2SR	Read	Digital current sense Channel 2	continuous	0x0000
2Bh	ADC3SR	Read	Digital current sense channel 3	continuous	0x0000
Not used area					
31h	ADC9SR	Read	Digital frame temperature sense	continuous	0x0000
32h	ADCLSR	Read/Clear	Digital current for self-test (Low Level)	Init	0x0000
33h	ADCMSR	Read/Clear	Digital Current for self-test (Medium Level)	Init	0x0000
34h	ADCHSR	Read/Clear	Digital Current for self-test (High Level)	Init	0x0000
35h	ITCNTSR	Read	I²t counter status	rare	0x0000
36h	ITSTSR	Read/Clear	I²t self-test	Init	0x0000
Not used area					
3Dh	TESTCFGR	Read/Write	Test configuration register	rare	0x0000
3Eh	TESTDATAR	Read/Write	Test data register	rare	0x0000

Note: Any command (write, read, or read and clear status) executed on a "not used" RAM register, that is, a not assigned address, does not have any effect: there is no change in the global status byte (no communication error, no error flag). The data written to this address is ignored. The data read from this address contains 00, independently of what has been written previously to this address.

A write command on "don't care" bits of an assigned RAM register address does not have any effect: There is no change on the global status byte. The data written to the "don't care bits" is ignored. The content of the "don't care bits" remains at "0" independently of the data written to these bits.

4.3.3 ROM

This memory is used for device identification.

Table 28. ROM memory map

Address	Name	Description	Access	Content
00h	Company code	STMicroelectronics company code	Read only	00H
01h	Device family	Product family (STi²Fuse) code	Read only	03H
02h	Product code 1	First product letter code (X)	Read only	58H
03h	Product code 2	Second product letter code (V)	Read only	56H
04h	Product code 3	Third product letter code (4)	Read only	4H
05h	Product code 4	Fourth product letter code (F)	Read only	46H
0Ah	Version	Silicon version	Read only	00H

Address	Name	Description	Access	Content
Not used area				
10h	SPI mode	Different modes of the SPI (see SPI mode)	Read only	A1H
11h	WD type 1	Indicates the type of watchdog used in the product	Read only	46H
13h	WD bit position 1	Indicates the address of the register containing the WD toggle bit	Read only	40H
14h	WD bit position 2	Indicates the position of the WD toggle bit	Read only	C1H
Not used area				
20h	SPI CPHA	Indicates the polarity and phase of the SPI interface	Read only	55H
3Eh	GSB options	Options of GSB byte (standard GSB definition)	Read only	00H
3Fh	Advanced op. code			

4.3.4 SPI modes

By reading out the <SPI Mode> register general information of SPI usage of the device application registers can be read.

Table 29. SPI Mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Content
BR	DL2	DL1	DL0	SPI8	0	S1	S0	A1H

SPI Burst Read

Table 30. SPI Burst Read

Bit 7	Description
0	BR disabled
1	BR enabled

The Burst Read is implemented in this product so this bit is enabled.

SPI Data Length

The SPI Data Length value indicates the length of the SCK count monitor which is running for all the accesses to the Device Application Registers. In case a communication frame with an SCK count is not equal to the reported one, the device will lead to a SPI Error and the data will be rejected.

The Frame Length is specified on 3 bits in the SPI Mode register located in the ROM part.

The 24-bit SPI communication is implemented in this product, so these bits are ‘010’.

Table 31. SPI Data Length

Bit 6	Bit 5	Bit 4	Description
DL2	DL1	DL0	
0	0	0	Invalid
0	0	1	16 bit SPI
0	1	0	24 bit SPI
...			...
1	1	1	64 bit SPI

Data Consistency Check (Parity/CRC)

For some devices a Data Consistency Check is required. Therefore, either a parity-check or for very sensitive systems a CRC may be implemented.

It is defined on 2 bits, in the SPI Mode register located in the ROM Part. A check is then applied on the incoming frame (SDI) while a calculation elaborated on one/multiple bits is done and integrated on the outgoing frame (SDO).

Table 32. SPI Data Consistency Check

Bit 1	Bit 0	Description
S1	S0	
0	0	Not used
0	1	Parity used
1	0	CRC used
1	1	Invalid

In case either the Parity or the CRC check is implemented it is always located at the end of the communication.

The device is equipped with the parity control check.

4.4 Outputs control

Depending on the actual device mode, outputs can be controlled by the SPI register or direct input DIx. Direct input DIx is a channel enabler, in whatever operating situation the device is (in fail-safe or normal mode), it is not possible to turn on the channel without the relevant DIx pulled up. Pulling down DIx, it triggers the corresponding channels FAST_OFF, within t_{DIx_off} (as in the case of faults).

The output channels can be configured to operate in Bulb or LED mode using the Channel Control Register (CCR). If the relevant bit in CCR is 0, the output is configured in Bulb mode, if it is set to 1, the output is configured in LED mode (default value is 0).

SPI register SOCR

In normal mode, the outputs can be turned ON/OFF (if relevant DIx is pulled up) by programming the dedicated bit in the SOCR register.

While SOCRx bit is set, by pulling down the relevant DIx channel is turn off FAST_OFF within t_{DIx_off}.

Procedure to turn-ON the outputs in PWM operations

The status of the output drivers is configured via the SPI output control register (SOCR), the relevant DIx pulled up and direct input enable bit “DIENCR” in the OUTCFGRx register, the PWM configuration bits (PWMFCY1 and PWMFCY0 in the OUTCFGRx register) and the channel control register (CTRL). The DIENCR selects if the OUTPUTX outputs are controlled also by the direct inputs DIx or only by the SOCR. The PWMFCY bit selects the outputs frequency in PWM mode.. Please refer to the following table for Output Control details in Normal Mode.

Table 33. Output control truth table

DIENCR (OUTCFGRx)	DIx	SOCRx	DUTYCR	OUTPUTx
1	1	X	X%	PWM
0	1	0	X%	OFF
0	1	1	X%	PWM
X	0	X	X%	OFF

Note:

- *In normal mode the outputs are driven according to the SPI register setting and DIx pins (DIx is an enabler for channels turn on) if the related DIENCR bit is set.*
- *In fail-safe mode, the outputs are controlled by the direct inputs DIx regardless of SPI commands. It is possible to apply the PWM through the DIx inputs. The PWM unit is not active in fail-safe mode, it is still possible to access the relevant registers and to configure them.*

To turn on channels, relevant DIx must be set high and information must be enter into following registers:

- Select the PWM frequency by using the two bits PWMFCYx
- Select the phase information by using the 5 bits CHPHAx
- Select the switching slope by using the two bits SLOPECRx
- Select the channels configuration Bulb/LED by using the bit CCR
- Select the duty cycle by using the 10 bits DUTYCR[9:0]
- Select the channel through the dedicated SOCRx bits in the SOCR register
- Select the PWM triggering mode by using the single bit PWM_TRIG of the CTRL register

The PWMSYNC bit in the CTRL registerwill reset the internal 12 bits clock counter. This allows to have a known time base and to synchronize different devices among each other.

The signal on the PWM_CLK is divided internally by a factor from 4096 to 512 depending on the PWMFCY1 and PWMFCY0 in the OUTCFGRx register to generate the base frequency for the output:

- PWM signal is generated by properly selecting 10 of 12 bits on the clock counter. PWM engine has a virtual 10-bit granularity except when PWM divider is set to 512, in this case only a 9-bit granularity is possible (LSB of 10bit generated PWM is fixed to zero). Duty cycle step can be modified with the granularity related to the 9-bit register.

The duty cycle of the output signal is configured for each OUTPUTX with the OUTCTRCR register using 10 bits (MSB first):

- Programming an output duty cycle at 000h will result in a 0% duty cycle, it means channel always OFF.
- Programming an output duty cycle at 3FFh will result in a 100% duty cycle (4095/4096), it means channel always ON when the SOCRx/DIx bit is set.
  - In normal mode the outputs are driven according to the SPI register setting and DIx pins (DIx is an enabler for channels turn on) if the related DIENCR bit is set.

Set PWMSYNC bit in Control Register “CTRL” (to synchronize internal PWM counter to the selected channels).

The internal PWM counter is 12 bits depth, it is active whatever the state of the channels, if $V_{DD} > V_{DD\_TH}$.

The set of PWMSYNC bit allows to reset the PWM counter.

The phase shift of the output signal is configured for each OUTPUTx by internally concatenating the CHPHAx 5 bits with '00000' in order to get 10 bits. Granularity of the phase shift is 5 bits. CHPHA = 00000b means a phase shift of 0 (internal 10bit phase shift is 0x000=0000000000b), while CHPHA = 11111b results in a maximum phase shift of 31/32 = (internal 10bit phase shift is 0x3E0 = 1111100000b). The phase shift is relative to the base frequency of the selected channel. Thus, the exact point in time when the channel switches on also depends on the operating mode of the selected channel.

Table 34. Phase shift configuration

Phase Shift (%)	CHPHA[4:0]	Internal 10-bits	Phase Shift (ms) PWM = 400 kHz Divider = 2048	Phase Shift (ms) PWM = 400 kHz Divider = 1024	Phase Shift (ms) PWM = 400 kHz Divider = 512
9.4	03h	60h	0.481	0.24	0.12
28.1	09h	120h	1.439	0.719	0.360
46.9	0Fh	1E0h	2.40	1.2	0.6
75	17h	2E0h	3.84	1.92	0.96
90	1Ch	380h	4.608	2.304	1.152

A change of phase/duty will be taken in account after the next zero crossing of the PWM counter.

Note: If the frequency on PWM_CLK is too low (f < PWMCLK), the device falls back to an internally generated PWM frequency of approximately 400 kHz. In this case the PWMCLOCKLOW bit in the OUTSRx and the global error flag are set.

4.4.1 OTP programming

A dedicated OTP manages the direct input configuration. A corresponding bit named “MCUext” is stored in a register and controls the direct input pins functionality.

The OTP bits are automatically read after transition from standby mode to fail-safe mode.

MCUext = 1 (default)

Table 35. OTP memory map - MCUext = 1

OTP Memory Map Register (3Eh)	bit 1, bit 0	bit 1, bit 0	bit 1, bit 0	bit 1, bit 0
	00	01	10	11
CH3	DI1	DI0	DI1	OFF
CH2	DI0	DI0	DI1	OFF
CH1	DI1	DI0	DI1	OFF
CH0	DI0	DI0	DI1	OFF

In fail-safe mode, the device is configured in auto-restart in case of harness protection triggering (automatic restart will occur when Counter down count will reach 0). ITOFFSRx will be set as soon as harness protection is triggered, it can be reset only by a R&C command (unlatching the channel, no counter reset).

In normal mode, device is configured in latch. As soon as ITOFFSRx is set (at harness protection triggering), a R&C command is needed for unlatch. When the unlatch command is sent, the counter will retain the value reached during down counting (no counter reset).

MCUext = 0

Table 36. OTP memory map - MCUext = 0

OTP Memory Map Register (3Eh)	bit 1, bit 0	bit 1, bit 0	bit 1, bit 0	bit 1, bit 0
	00	01	10	11
CHx	ON	ON	OFF	OFF

- DI0: configured as STATUS (Global i²t fault indication active low => OR between all channels fault flag).
- DI1: configured as F_CTRL (Unlatcher active high for all channels i²t protection at once).
- DI0 configured as STATUS and DI1 configured as F_CTRL are enabled in both Fail Safe and Normal modes.
- Harness protection latches OFF the corresponding channel. ITOFFSRx will be kept high till a R&C command is acquired. (ITOFFSRx bit remains high even if F_CTRL will unlatch all channels and even if counters reaches 0).
- Unlatch through DI1 (F_CTRL) toggling, pulled high for at least 20 µs and then set low, or R&C on ITOFFSRx. All channels will be unlatched at once. Then, the counter will retain the value reached during down counting (no counters value reset).
- F_CTRL = Low → Protection active.
- F_CTRL = High To Low → Unlatch all channels harness protection, regardless of the counter value (no counters value reset).

Further information about the OTP programming mode is provided in the dedicated user manual UM3275 (OTP programming for STi²Fuse devices).

4.4.2 Procedure to turn on the outputs with the direct input DIx

The DIx are the enabler for channel switching. In fail-safe, by applying logic level 1/0 to DIx pins, the associated OTP selected outputs are turned on/off accordingly (see Table 37). In normal mode, DIx effect is in (AND) condition with SPI configuration. When DIENCR bit = 0 the channels drive through SOCR are enabled by the relevant DIx high condition, while, when DIENCR bit is set, channels may be driven through DIx directly. In whatever operating situation it is always possible to turn off channels quickly by relevant DIx (thanks to turn off by FAST_OFF < t_{DIx_off}). Then Table 38 specifies the output state in normal mode:

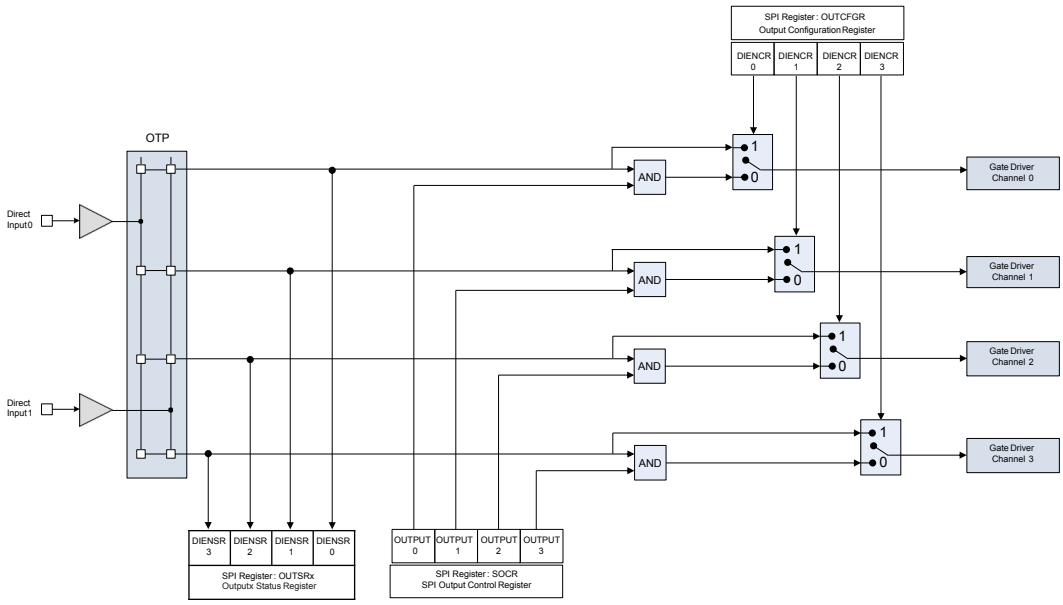
Table 37. Output driving by DIx: truth table in fail safe mode

DIENCR	DIx	SOCR	OUTx
X	L	X	OFF
X	H	X	ON (STEADY STATE)

Table 38. Output driving by DIx: truth table in normal mode

DIENCR	DIx	SOCRx	DUTYCR	OUTPUTx
0	0	X	X%	OFF
0	X	0	X%	OFF
0	1	1	X%	ON (PWM %)
1	0	X	X%	OFF
1	1	X	X%	ON (PWM %)

Figure 22. Output driving in Normal Mode



4.4.3 Output switching slopes control

Output switching slopes are set by the two bits SLOPECR1, 2 in the OUTCFGCRx register (address from 0x08h to 0x0Dh depending on the channel), as the Table 39 shows; parameter details are in the Table 62.

Table 39. Switching slopes

SLOPECRx	Channel 0–3 (V/µs)
00	Standard
01	Fast
10	Faster
11	Fastest (default)

4.5 Control registers

OUTCTRCRx

Outputs control register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	DUTYCR9	DUTYCR8	DUTYCR7	DUTYCR6	DUTYCR5	DUTYCR4	DUTYCR3	DUTYCR2	DUTYCR1	DUTYCR0	RESERVED	OLOFFCR	WDTB	PARITY
-		R/W										-	R/W		R

Address: 0x00h to 0x03h

Type: R/W

Reset: 0

Description: Outputs control register

[15:14]	-
[13:4]	Duty cycle setting value
[3]	-
[2]	OLOFFCR bit: 1: internal pull-up current generator for the corresponding channel x active 0: internal pull-up current generator for the corresponding channel x disabled
[1]	Watchdog toggle bit
[0]	Parity bit

OUTCFGRx

Output configuration register channels 0 to 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLOPECR1	SLOPECR0	RESERVED	CHPHA4	CHPHA3	CHPHA2	CHPHA1	CHPHA0	SPCR1	SPCR0	PWMFCY1	PWMFCY0	CCR	DIENCR	RESERVED	PARITY
R/W		-	R/W											-	R

Address: 0x08h to 0x0Bh

Type: R/W

Reset: C000H

Description: Output configuration register channels 0 to 3

[15:14]	Switching slope control (default: 11)
[13]	-
[12:8]	Channel phase value [4:0] 00001: resulting phase = 0/32 00010: resulting phase = 1/32 .... 11110: resulting phase = 30/32 11111: resulting phase = 31/32 Each output has a specific mode for the digital conversion of its current. This mode is defined through two dedicated bits SPCR1 and SPCR0 of OUTCFGRx registers.
[7:6]	Current Sense Sampling Point [1:0] SPCR1: 0 SPCR0: 0 STOP Mode: authorizes digital conversion to be launched at each beginning of On phase of the selected channel. SPCR1: 0 SPCR0: 1 START Mode: authorizes digital conversion to be launched just before the end of On phase of the selected channel. SPCR1: 1 SPCR0: 0 CONTINUOUS Mode: authorizes digital conversion during all On phase of the selected channel. SPCR1: 1 SPCR0: 1 FILTERED Mode: authorizes digital conversion like CONTINUOUS mode with the use of Lowpass Filter to filter datas coming from the conversion. It is useful at low level output current.
[5:4]	PWM frequency selection[1:0] Each output has a specific ratio for its PWM functionality. This mode is defined through two dedicated bits PWMFCY1 and PWMFCY0 of OUTCFGRx registers. PWMFCY1: 0 PWMFCY0: 0 PWM Freq ratio: 1024 PWMFCY1: 0 PWMFCY0: 1 = PWM Freq ratio: 2048 PWMFCY1: 1 PWMFCY0: 0 = PWM Freq ratio: 4096 PWMFCY1: 1 PWMFCY0: 1 = PWM Freq ratio: 512 When a combination will be selected, the output frequency of the selected channel will be the PWM clock input frequency divided by the defined ratio.
[3]	Set the channel configuration (Bulb/LED) 0: Bulb mode 1: Led mode Led mode internally set to ‘0’ if parallel mode is selected whatever is the logic state of this bit. Enabling LED mode both the I²t protection and the capacitive charge mode is disabled.

[2]	Direct input enable in normal mode (according to OTP mapping) Each output has an OTP programmed direct input assignment for limp-home operation. Any output can be programmed to be always OFF in limp-home, or according to DI0 pin state or according to DI1 pin state. This programmed assignment can be read from DIOTP bits of FSITCRx status register. When DIENCR bit is set, DIx pin state assigned to the output is able to turn ON/OFF the related channel with the selected PHASE/DUTYCYCLE independently on SOCR status (see Table 38). In fail-safe mode, applying logic level 1/0 to pin, the associated OTP selected outputs are turned ON/OFF.
[1]	-
[0]	Parity bit

CHLOFFTCRxx

Channel latch-off timer control register

Address: 0x10h to 0x11h

Type: R

Reset: 0

Description: Channel latch-off timer control register

In case of power limitation or thermal shutdown event, the output channel behavior is configurable (by means of 2 bits) as latch-off or time limited auto-restart ($t_{blanking}$).

By default, the latch-off mode is the set behavior.

In latch-off state, the fault must be cleared to re-enable the output channel after an overtemperature or power limitation event.

The blanking window duration ($t_{blanking}$) in case of power limitation or thermal shutdown events can be set, per channel, according to the following table:

Table 40. Programmable $t_{blanking}$ values

CHLOFFTCRx3	CHLOFFTCRx2	CHLOFFTCRx1	CHLOFFTCRx0	
0	0	0	0	latch-off (default)
0	0	0	1	16 ms
0	0	1	0	32 ms
…	…	…	…	…
1	1	1	0	224 ms
1	1	1	1	240 ms

CHLOFFTCR0

Channel latch-off timer control register 0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHLOFFTCR23	CHLOFFTCR22	CHLOFFTCR21	CHLOFFTCR20	CHLOFFTCR13	CHLOFFTCR12	CHLOFFTCR11	CHLOFFTCR10	CHLOFFTCR03	CHLOFFTCR02	CHLOFFTCR01	CHLOFFTCR00	RESERVED	RESERVED	RESERVED	PARITY
R/W												-			R

Address: 0x10h

Type: R/W

Reset: 0

Description: Channel latch-off timer control register 0

[15:12]	To configure the output behavior in case of power limitation for the corresponding channel 2
[11:8]	To configure the output behavior in case of power limitation for the corresponding channel 1
[7:4]	To configure the output behavior in case of power limitation for the corresponding channel 0
[3:1]	-
[0]	Parity bit

CHLOFFTCR1

Channel latch-off timer control register 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CHLOFFTCR33	CHLOFFTCR32	CHLOFFTCR31	CHLOFFTCR30	RESERVED	RESERVED	RESERVED	PARITY
-								R/W				-			R

Address: 0x11h

Type: R/W

Reset: 0

Description: Channel latch-off timer control register 1

[15:8]	RESERVED
[7:4]	To configure the output behavior in case of power limitation for the corresponding channel 3
[3:1]	RESERVED
[0]	Parity bit

SOCR

Channel control register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXIT_CAPCR3	EXIT_CAPCR2	EXIT_CAPCR1	EXIT_CAPCR0	SOCR3	SOCR2	SOCR1	SOCR0	I2t_BIST_TRIG	ADC_BIST_TRIG	CAPCR3	CAPCR2	CAPCR1	CAPCR0	WDTB	PARITY
R/W															R

Address: 0x13h

Type: R/W

Reset: 0

Description: Channel control register

[15]	Exit capacitive charging mode on channel 3 (active high). This bit is automatically reset.
[14]	Exit capacitive charging mode on channel 2 (active high). This bit is automatically reset.
[13]	Exit capacitive charging mode on channel 1 (active high). This bit is automatically reset.
[12]	Exit capacitive charging mode on channel 0 (active high). This bit is automatically reset.
[11]	SOCR bit controls output state of channel 3 in AND combination with related DIx logic status 1 – output enabled 0 – output disabled
[10]	SOCR bit controls output state of channel 2 in AND combination with related DIx logic status 1 – output enabled 0 – output disabled
[9]	SOCR bit controls output state of channel 1 in AND combination with related DIx logic status 1 – output enabled 0 – output disabled
[8]	SOCR bit controls output state of channel 0 in AND combination with related DIx logic status 1 – output enabled 0 – output disabled
[7]	SOCR bit controls the execution of the I2t_bist on demand 1 - I2t_BIST enabled 0 - I2t_BIST disabled
[6]	SOCR bit controls the execution of the ADC_bist on demand 1 - ADC_BIST enabled 0 - ADC_BIST disabled
[5]	Capacitive charging mode on channel 3 1 – enabled 0 – disabled This bit is automatically reset.
[4]	Capacitive charging mode on channel 2 1 – enabled 0 – disabled This bit is automatically reset.

[3]	Capacitive charging mode on channel 1 1 – enabled 0 – disabled This bit is automatically reset.
[2]	Capacitive charging mode on channel 0 1 – enabled 0 – disabled This bit is automatically reset.
[1]	Watchdog toggle bit
[0]	Parity bit

CTRL

Control register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GOSTBY	UNLOCK	RESERVED	RESERVED	EN	PWM_TRIG	RESERVED	RESERVED	LOCKEN5	LOCKEN4	LOCKEN3	LOCKEN2	LOCKEN1	LOCKEN0	PWMSYNC	PARITY
R/W		-		R/W	R/W	-		R/W						W	R

Address: 0x14h

Type: R/W

Reset: 0

Description: Control register

[15]	Go to standby. It is necessary to perform 2 write accesses to enter standby: 1. Write UNLOCK = 1 2. Write GOSTBY = 1 and EN = 0
[14]	Unlock bit. UNLOCK bit allows protected SPI transactions. It means that the next SPI communication will automatically clear this bit and prevent any change of protected data (like slope control or Bulb/Led mode for example). As a consequence, modifying a protected data requires to set UNLOCK bit in a first communication and write the protected data during the next communication.
[13:12]	-
[11]	Enter normal mode 1 - normal mode 0 - fail-safe mode To enter normal mode: • Write UNLOCK = 1 • Write EN = 1 *Note: UNLOCK bit allows protected SPI transactions. Then, the next SPI communication will automatically clear this bit and prevent any change of protected data (like slope control or Bulb/Led mode for example). As a consequence, modifying a protected data requires to set UNLOCK bit in a first communication and write the protected data with the next communication.*
[10]	PWM_TRIG: PWM triggering mode 0: PWM trigger according to the rising edge of PWM period and phase shift configuration 1: PWM trigger according to the falling edge of PWM period and phase shift configuration
[9:8]	-
[7:2]	Protected transaction mode: LOCKEN5: Lock enable for INOMx, TNOMx, and ILIM_LATCHx LOCKEN4: Lock enable for slope control SLOPECRx LOCKEN3: Lock enable for Bulb/LED mode CCRx LOCKEN2: Lock enable for phase shift CHPHAx LOCKEN1: Lock enable for configurable blanking time CHLOFFTCRx LOCKEN0: Lock enable for PWM clock synchronization When the bit is set (LOCKENx = 1), it is used to have a protected transaction: • Setting UNLOCK bit • Modify the relevant configuration register

	• LOCKENx = 0 means reset value - those configuration registers may be altered with a single frame standard Write command.
[1]	PWM clock synchronization. PWMSYNC = 1 to clear PWM internal counter. It automatically resets at next SPI communication
[0]	Parity bit

FSITCRx

Fail-safe and I²t current sense registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	ISHUTOFFCR2x	ISHUTOFFCR1x	ISHUTOFFCR0x	ILIM_LATCHx	PARAL	MCUext	DIOTP1x	DIOTP0x	INOM2x	INOM1x	INOM0x	TNOM2x	TNOM1x	TNOM0x	PARITY
-	R/W				R				R/W						R

Address: 0x15h to 0x18h

Type: R/W

Reset: 0x0200

Description: Digital I²t current sense registers

[15]	-
[14:12]	Multiplier setting for programmable I_SHUTOFF
[11]	I²t curve behavior when $V_{OUT} < V_{OUT\_FSD}$ and $I_{OUT} = I_{LIM}$ 0: to count at maximum speed 1: to latch-off the channel
[10]	Parallel mode selected for channels 0 and 1 when PARAL is ‘1’
[9]	External Micro Control Unit bit: selects if the user will have a second fail-safe MCU on board (when it is ‘0’) or if the user will drive the device in fail-safe using the main MCU (when it is ‘1’).
[8]	Associated DIx input description bit 1
[7]	Associated DIx input description bit 0
[6:4]	Nominal current setting for I²t curve
[3:1]	Nominal time setting for I²t curve
[0]	Parity bit

Note: All the bits of these registers are programmable through OTPs.

OUTSRx

Output status register channels 0 to 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIENSR	ISHUTOFFSRx	CAPCSRx	CHFBSRx	VDSHSRx	ITOFFSRx	OLPUSRx	CHLOFFSRx	RST	SPIE	PWMCLOCKLOW	VCCUV	TW3	TW2	TW1	PARITY
R	R/C	R			R/C	R		R/C			R				

Address: 0x20h to 0x23h

Type: R/C

Reset: 0

Description: Output status register channels 0 to 3

[15]	Direct input status, image of associated DI logic level according to OTP allocation
[14]	ISHUTOFFSRx is '1' when shut-off protection is active and it is switching off the channel x
[13]	Capacitive charging mode status bit
[12]	Channel feedback status. Combination of power limitation and overtemperature
[11]	VDS feedback status. VDSHSRx bit is '1' when V_{OUTx} is lower than V_{DSH_TH} (= V_{CC} - 1.5 V). If VDSHSRx is '1' in on-state (after a proper delay time depending on the capacitive load connected to the output x), this is indicative of a potential overload condition. If VDSHSRx is '0' in offstate (after a proper delay time depending on the capacitive load connected to the output x), this is indicative of a potential fault condition stuck to V_{CC}/open-load off state.
[10]	ITOFFSRx is '1' when I^2t curve protection is active and it is switching off the channel x
[9]	Output pull up generator status
[8]	Channel latch-off status. This bit is set when overload blanking time has elapse and channel is latched off. This bit must be cleared to re-enable the output channel. An SPI R&C operation on OUTSRx register will not clear this bit. This bit can be cleared only with a write operation on the corresponding CHLOFFTCRx register.
[7]	Chip reset
[6]	SPI error
[5]	PWM clock frequency too low
[4]	V_{CC} undervoltage
[3]	This bit is set if the frame temperature is greater than the threshold (140 °C) and can be used as a temperature pre-warning. The bit is cleared automatically when the frame temperature drops below the case-temperature reset threshold (TCR3).
[2]	This bit is set if the frame temperature is greater than the threshold (130 °C) and can be used as a temperature pre-warning. The bit is cleared automatically when the frame temperature drops below the case-temperature reset threshold (TCR2).
[1]	This bit is set if the frame temperature is greater than the threshold (120 °C) and can be used as a temperature pre-warning. The bit is cleared automatically when the frame temperature drops below the case-temperature reset threshold (TCR1).
[0]	Parity bit

Note: The output status register reports the status of the selected channel based on the configuration register and in case of fault condition.

ADCxSR

Digital current sense registers channels 0 to 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	ADCxSR9	ADCxSR8	ADCxSR7	ADCxSR6	ADCxSR5	ADCxSR4	ADCxSR3	ADCxSR2	ADCxSR1	ADCxSR0	RESERVED	SOCRx	UPDTSR	PARITY
-		R										-	R		

Address: 0x28h to 0x2Bh

Type: R

Reset: 0

Description: Digital current sense registers channels 0 to 3

[15:14]	-
[13:4]	10-bit register containing the digital value of OUTPUTx current
[3]	-
[2]	SOCR Bit controls output state of channel x: 1 – output Enabled 0 – output disabled
[1]	Updated status bit. This bit is set when value is updated and cleared when register is read
[0]	Parity bit

Note: The register contains the digital value of the current flowing on the selected channel. It reports the result of the digital current conversion. It is updated according to the selected modes (set by SPCR1 and SPCR0 bits) of the OUTCFGRx register.

ADC9SR

Digital case thermal sensor voltage register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	ADC9SR9	ADC9SR8	ADC9SR7	ADC9SR6	ADC9SR5	ADC9SR4	ADC9SR3	ADC9SR2	ADC9SR1	ADC9SR0	RESERVED	RESERVED	UPDTSR	PARITY
-		R										-		R	

Address: 0x31h

Type: R

Reset: 0

Description: Digital case thermal sensor voltage register

[15:14]	-
[13:4]	The 10-bit register contains the digital value of case temperature sensor voltage. ADC9SR9 (MSB) ADC9SR0 (LSB) T_{CASE} (typ.) = 401.8 °C -1.009 * ADC9SR[13:4]
[3:2]	-
[1]	Updated status bit. This bit is set when value is updated and cleared when register is read
[0]	Parity bit

Note: The register contains the result of the digital conversion of the case temperature.

ADCLSR

Digital low current value self-test

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	ADCLSR9	ADCLSR8	ADCLSR7	ADCLSR6	ADCLSR5	ADCLSR4	ADCLSR3	ADCLSR2	ADCLSR1	ADCLSR0	RESERVED	RESERVED	UPDTSR	PARITY
-		R/C										-		R	

Address: 0x32h

Type: R/C

Reset: 0

Description: Digital low current value self-test

[15:14]	-
[13:4]	The 10-bit register contains the digital value of low current level used for self-test
[3:2]	-
[1]	Updated status bit. This bit is set when value is updated and cleared when register is read
[0]	Parity bit

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address will clear all clearable bits independently of payload content.

ADCMSR

Digital medium current value self-test

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	ADCMSR9	ADCMSR8	ADCMSR7	ADCMSR6	ADCMSR5	ADCMSR4	ADCMSR3	ADCMSR2	ADCMSR1	ADCMSR0	RESERVED	RESERVED	UPDTSR	PARITY
-		R/C										-		R	

Address: 0x33h

Type: R/C

Reset: 0

Description: Digital medium current value self-test

[15:14]	-
[13:4]	The 10-bit register contains the digital value of medium current level used for self-test
[3:2]	-
[1]	Updated status bit. This bit is set when value is updated and cleared when register is read
[0]	Parity bit

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address will clear all clearable bits independently of payload content.

ADCHSR

Digital high current value self-test

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	ADCHSR9	ADCHSR8	ADCHSR7	ADCHSR6	ADCHSR5	ADCHSR4	ADCHSR3	ADCHSR2	ADCHSR1	ADCHSR0	RESERVED	RESERVED	UPDTSR	PARITY
-		R/C										-		R	

Address: 0x34h

Type: R/C

Reset: 0

Description: Digital high current value self-test

[15:14]	-
[13:4]	The 10-bit register contains the digital value of high current level used for self-test
[3:2]	-
[1]	Updated status bit. This bit is set when value is updated and cleared when register is read
[0]	Parity bit

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address will clear all clearable bits independently of payload content.

ITCNTSR

I²t counter status register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ITCNT3			ITCNT2			ITCNT1			ITCNT0			PARITY
R															

Address: 0x35h

Type: R

Reset: 0

Description: I²t counter status register

[15:13]	-
[12:10]	I²t counter status for channel 3: 000 → [0%: 12.5%] 001 → [12.5%: 25%] … 111 → [87.5%: 100%]
[9:7]	I²t counter status for channel 2: 000 → [0%: 12.5%] 001 → [12.5%: 25%] … 111 → [87.5%: 100%]
[6:4]	I²t counter status for channel 1: 000 → [0%: 12.5%] 001 → [12.5%: 25%] … 111 → [87.5%: 100%]
[3:1]	I²t counter status for channel 0: 000 → [0%: 12.5%] 001 → [12.5%: 25%] … 111 → [87.5%: 100%]
[0]	Parity bit

ITSTSR

I²t self-test status register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ITST3			ITST2			ITST1			ITST0			PARITY
-			R/C												R

Address: 0x36h

Type: R/C

Reset: 0

Description: I²t self-test status register

[15:13]	-
[12:10]	I²t self-test status for channel 3 One bit for each tested value (Low, Medium, High) → 1: PASS 0: FAIL
[9:7]	I²t self-test status for channel 2 One bit for each tested value (Low, Medium, High) → 1: PASS 0: FAIL
[6:4]	I²t self-test status for channel 1 One bit for each tested value (Low, Medium, High) → 1: PASS 0: FAIL
[3:1]	I²t self-test status for channel 0 One bit for each tested value (Low, Medium, High) → 1: PASS 0: FAIL
[0]	Parity bit

Note: Selective bitwise clear is disabled for this register. A R&C operation on this address will clear all clearable bits independently of payload content.

5 Diagnostic

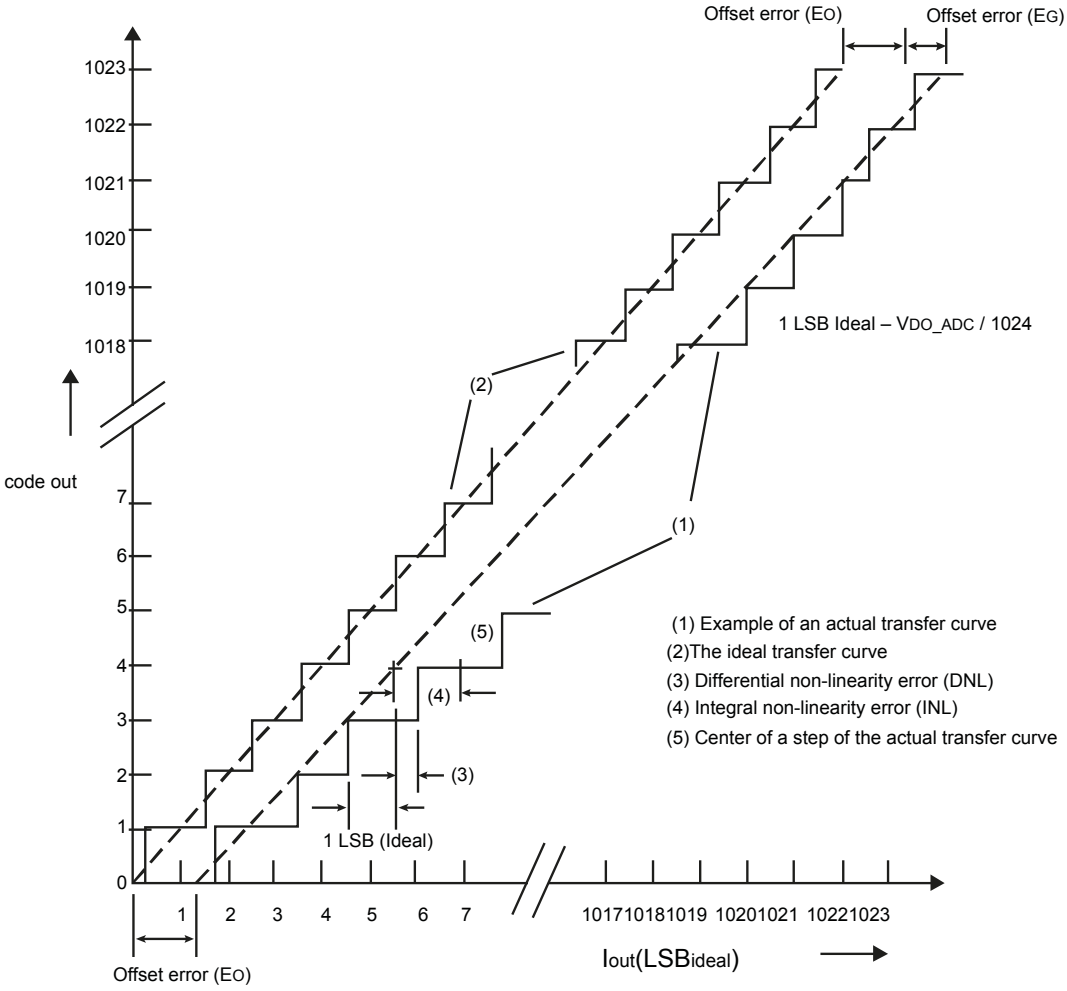
The device is capable of providing digital diagnostic information through the SPI interface.

5.1 Digital current sense diagnostic

5.1.1 ADC characteristics

Here are the “Differential Non Linearity” and “Integral Non Linearity” typical curves for the 10-bit ADC converter.

Figure 23. ADC characteristics and error definition



5.1.2 ADC operating principle

The device provides a 10-bit Successive Approximation Register (SAR) analog to digital converter. It is used to provide a digital information about the current sense feedback proportional to the output current and the temperature read by the internal sensor. An integrated LP (Progressive Average) Filter can be used to filter data coming from the ADC conversion reducing the effect of random noise coming from the analog Current Sense amplifier.

Note: The internal ADC is able to work in both Normal and Fail Safe conditions.

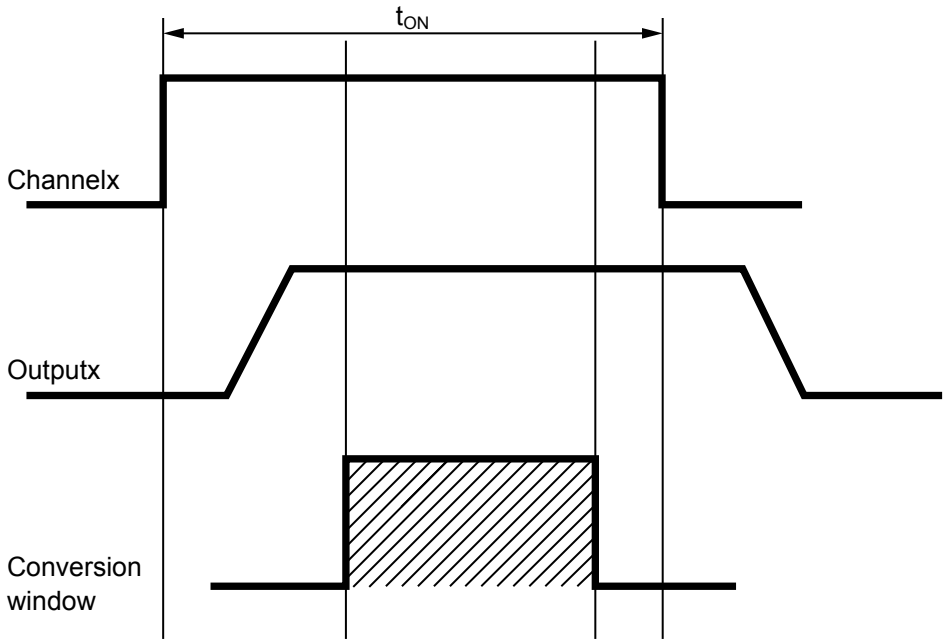
The integrated ADC control logic is designed to lead to a good 10-bit approximation of current sense/temperature feedback.

After each conversion, an updated bit “UPDTSR” is set to advise about new conversion data. This bit is reset after the Read process of the dedicated RAM register.

The data is maintained in the register until the next conversion results are available. The ADC register is refreshed at the end of each conversion and maintained during the conversion of the current sample. The data is converted on the 10-bit register, the formula is equal to: Iout_conv = data (10bit)/K. (see Table 64 and Table 68)

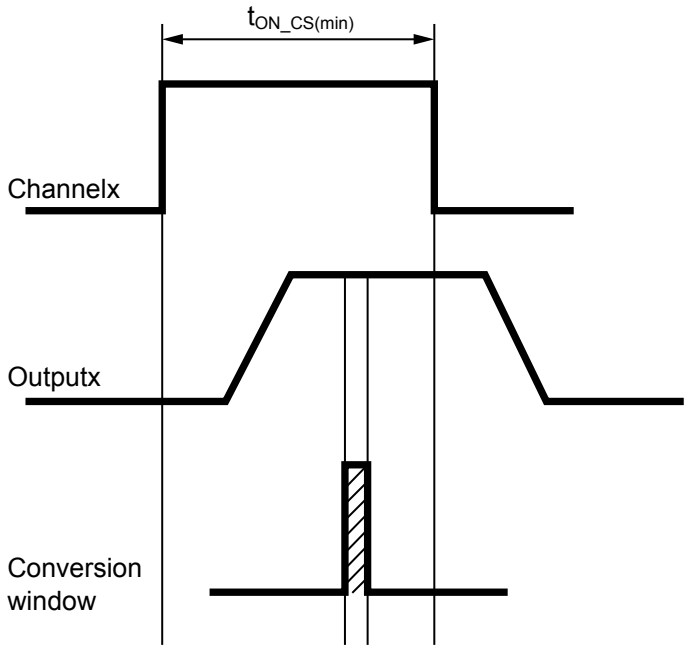
An analogue multiplexer has been implemented to connect the different channels to the amplifier and the ADC block. Due to the current sense amplifier settling time when switching from the current sense mode of one channel, to the current sense mode of another channel, a priority management is implemented to control the time when the data conversion can be done in a safe/stable way and to arbitrate the concurrent ADC sampling requests (see next figures).

Figure 24. Conversion window generation



A minimum conversion time ($t_{ON\_CS(min)}$) is defined to allow the signal stabilization at the input of the ADC converter and considering the sampling time. The user should manage the phase shift in a way that maximum two channels can be sampled in the same time window.

Figure 25. Minimum ON time for digital current sense availability

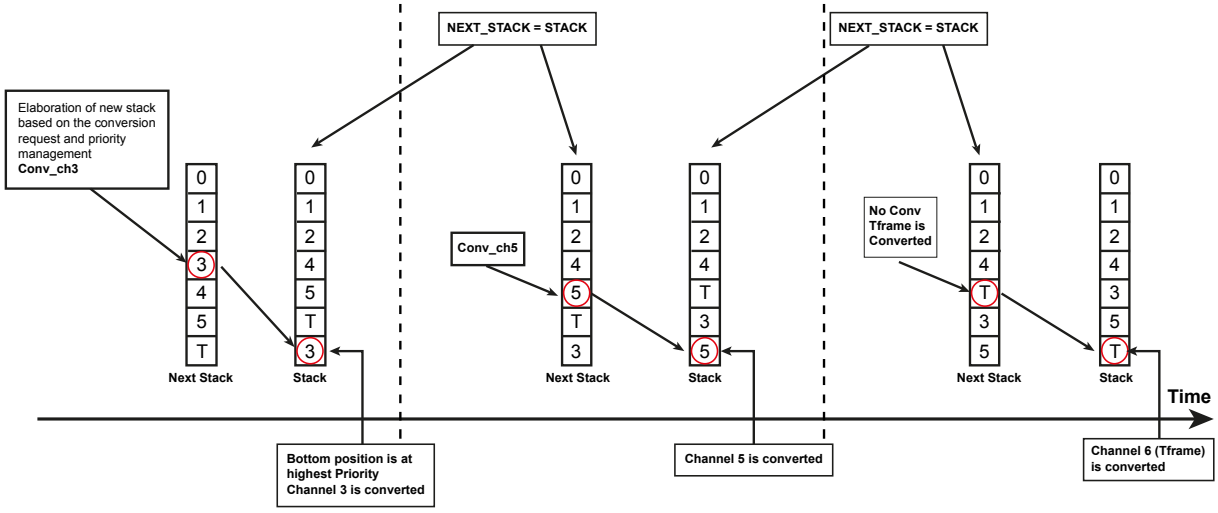


The sequence of channels to be converted is managed through an internal stack:

- Stack size is equal to the number of channels plus the frame temperature sensor.
- A conversion of selected channels is done based on the information stored at the end of the stack (see Figure 26).
- After the reset of the device or when no channels are active, the conversion of the Frame temperature sensor is done continuously.

When the conversion of a channel_x has to start, the channel_x is moved to the end of the stack while the other remaining channels are moved up.

Figure 26. Channel's sequence internal stack (6 channels example)



5.1.3 Registers

The results of the digital conversion are stored in the two dedicated registers, used for the digital conversion of the output current and case sense temperature respectively:

- **ADCxSR** (address from 28h to 2Bh) - Digital Outputx current (one register x channel).
- **ADC9SR** (address 31h) - Digital case temperature sensor voltage sense register.

Table 41. Registers

Register name	Bit 15, 14	Bit 13..4	Bit 3	Bit 2	Bit 1	Bit 0
ADCxSR 28h to 2Bh	Reserved	Digital Value of OUTx current	Reserved	SOCRx Possibility to control the Outx state (Read only)	UPDTSR Updated status bit. It is set when value is updated and cleared when register is read	Parity
ADC9SR 31h	Reserved	Digital Value of case temperature sensor voltage	Reserved	Reserved	UPDTSR Updated status bit. It is set when value is updated and cleared when register is read	Parity

5.1.4 Synchronous, asynchronous mode

Normal mode

The ADC conversion can work in 4 different sampling modes (stop, start, continuous or filtered) according to the Table 42. Two bits per channel “SPCR1” and “SPCR0” allocated in the Output Configuration Register “OUTCFGRx”, allow 4 different sampling modes:

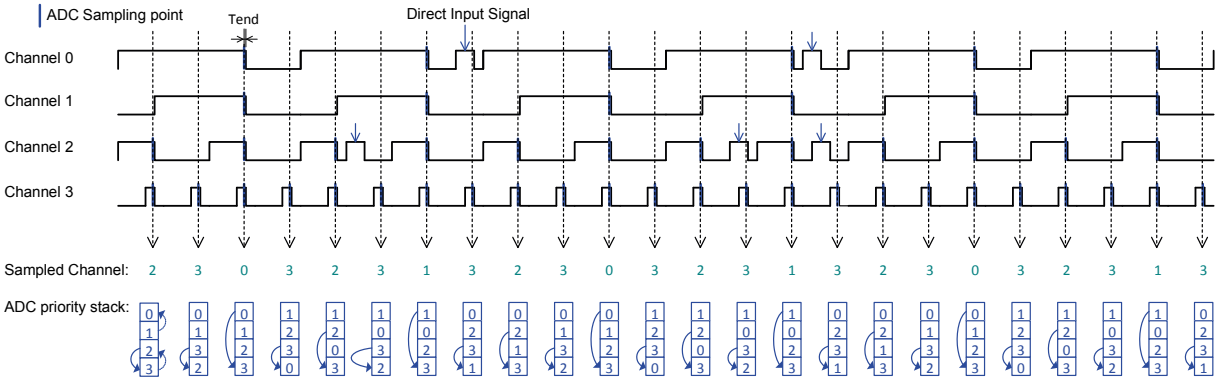
Table 42. Sampling mode

SPCRxx	Sampling mode
00	STOP mode
01	START mode
10	CONTINUOUS mode
11	FILTERED mode

Synchronous mode

- Synchronous mode in PWM condition:
  - Sampling is done according to the PWM rising and falling edge (see Figure 27). See Table 42 for more details about the registers configuration.
  - The sampling priority will be always allocated at higher priority.
- Registers configuration:
  - SPCR10 = 0h: Synchronous triggered by rising edge on internal PWM. Conversion is executed on the rising edge of the conversion window (see Figure 27).
  - The ADC real sampling is managed to trigger the sampling point with margin versus falling edge.
  - SPCR10 = 1h: Synchronous triggered by falling edge of the internal PWM signal. Conversion is executed on the falling edge of the conversion window (see Figure 27).

Figure 27. Sequence of channels



Asynchronous mode

In asynchronous mode the ADC result register is continuously refreshed, provided that the channel is commanded on through either the direct input signal or the SOCR register. Conversion is executed during the complete conversion window except the priority arbitration.

Since the ADC register is continuously refreshed, its conversion priority is always lower than the sampled channels.

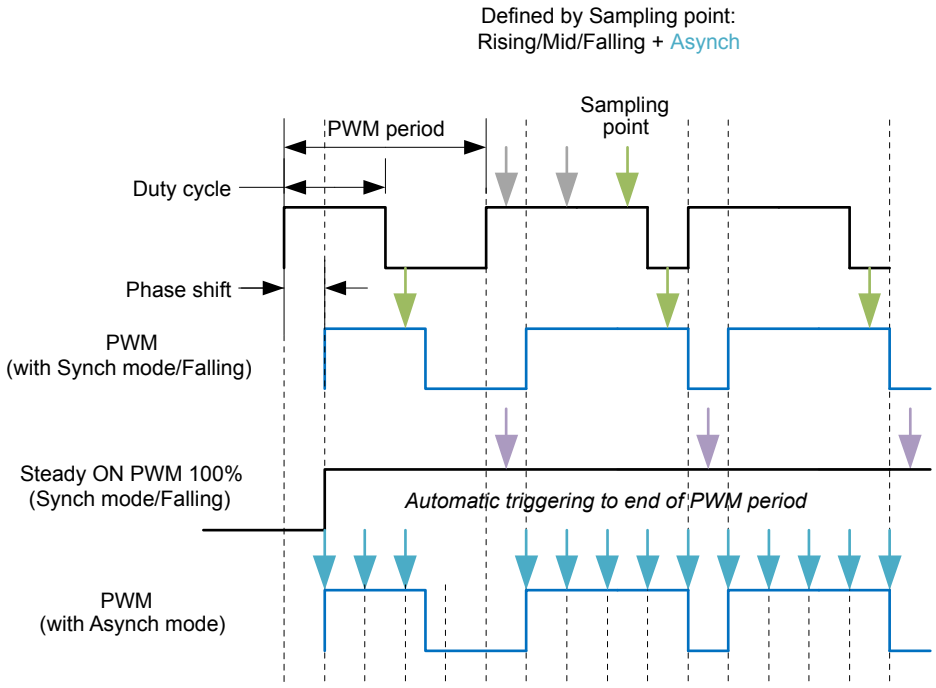
Once the PWM counter will reach a value for which synchronous diagnostic of another channel is requested, the internal MUX will switch to this channel and serve the ADC sampling request (channels in synchronous mode have higher priority compared with those in asynchronous mode). Once this sampling will be completed the MUX will switch back to the asynchronous sampling channel, provided that no higher priority sampling requests from other channels occur. If two or more channels are configured in asynchronous mode, the MUX will sequentially switch through those channels, always interrupted when higher priority synchronous sampling requests occur.

The thermal case sampling has always low priority for the ADC conversion and so can be interrupted by any channel in sample mode.

Registers configuration

- SPCR10 = 2h and SOCRx = 1: Asynchronous with continuous sampling
  Asynchronous mode, the ADC result register is continuously refreshed, provided that the channel is commanded either through the direct input signal or the SOCR register. Conversion is executed during the complete conversion window except the priority arbitration. Since the ADC register is continuously refreshed, its conversion priority is always lower than sampled channels.
- SPCR10 = 3h and SOCRx = 1: Asynchronous with continuous sampling and digital LP filter
  - The integrated LP filter is activated
  - This component will filter data coming from the ADC conversion reducing the effect of random noise coming from the analog Current Sense amplifier
- SPCR10 = 3h, SOCRx = x and DIx = High: If a channel is commanded off through SOCR, but commanded on through the Direct Input, the asynchronous sampling mode is forced
  The thermal case sampling has always low priority for the ADC conversion, and so it can be interrupted by any channel in sample mode. Thermal case conversion is always in Asynchronous continuous mode. In Fail Safe condition the ADC conversion is always in Asynchronous/Continuous Mode.
  - Conversion is executed during the complete conversion window.
  - No Priority Management is applied, channels are converted according to their position in the stack. No interruption and no priority management are possible. In case of multiple channels active at the same time, the conversion will start with the first one in the stack.

Figure 28. Asynchronous with continuous sampling



Sampling concept

- PWM mode (internal engine) → All the synchronous modes are available(start, stop, continuous or filtered).
- DC mode (internal engine) → ADC works in Continuous Mode. The conversion window follows the channel control input signal.
  - DC mode by/without DI: No difference, since this condition is equivalent to PWM with 100% of duty (the sampling will be always in continuous mode).
- PWM mode by DI (external source) → the DIx information is combined (O-red) with the channel control signal. Sampling will be executed according to the PWM mode settings.
  - With SPCRx = 2h, 3h, sampling is possible (continuous/filtered mode).

Synchronous mode in DC condition

This mode (PWM with 100% duty cycle) is equivalent to the asynchronous mode.

Table 43. ADC Configurations registers

SOCrx	DIx	DutyCrx	SPCR1, 0	Conversion Mode	Feedback type
1	X	X	00	Synchronous triggered by falling edge on the internal PWM signal	Output current
1	X	X	01	Synchronous triggered by rising edge on the internal PWM signal	Output current
1	X	X	10	Asynchronous with continuous sampling	Output current
1	X	X	11	Asynchronous with continuous sampling and digital LP filter	Output current
0	1	X	X	(Fail Safe mode) Asynchronous with continuous sampling	Output current
X	X	X	X	Tframe conversion (Always lower priority than current sampled modes)	Tframe sensor voltage

5.2 Integrated LP (progressive average) filter

In asynchronous mode, when the filtered mode is selected through the dedicated bits “SPCR1 = 1” and “SPCR0 = 1”, the integrated LP filter is activated. This component will filter the data coming from the ADC conversion reducing the effect of random noise coming from the analog Current Sense amplifier.

Features of the integrated LP filter:

- 1st order decimating filter on 16 samples.
- 1st result after 1 sample with progressive averaging of 16 successive samples.

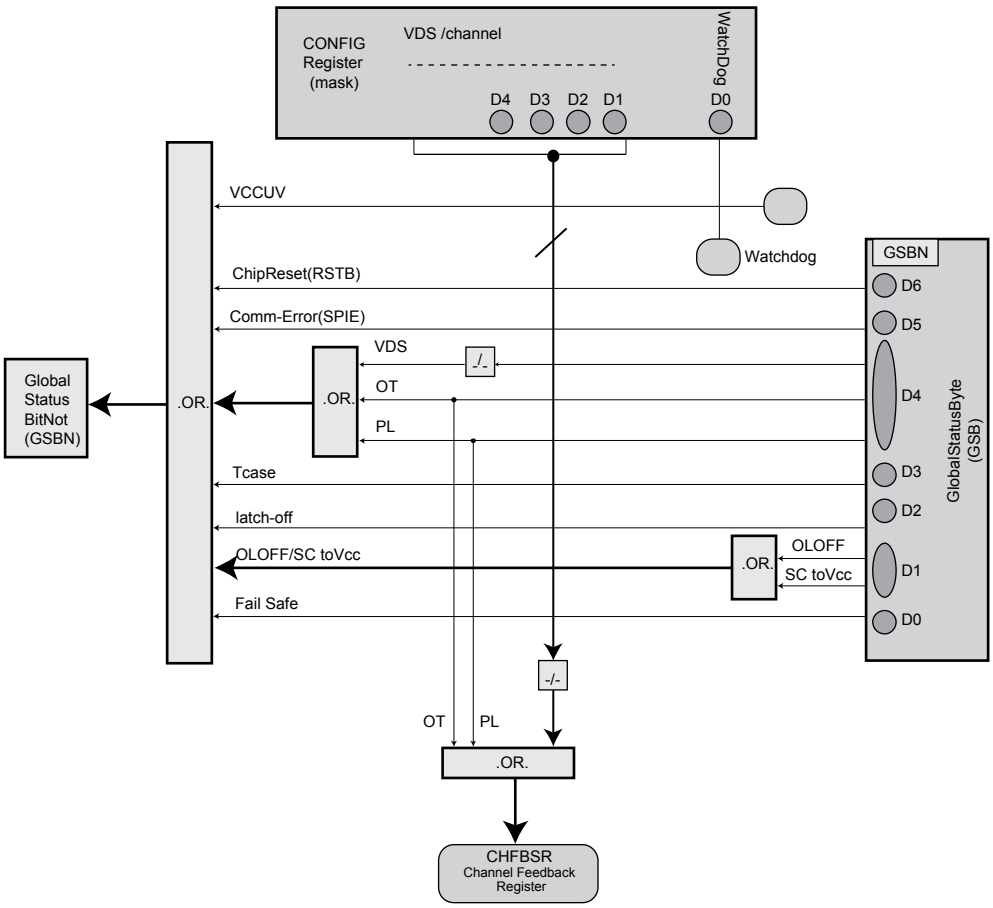
$$data(N) = \left(data(N-1)*\frac{15}{16} + data_i\right)/16 \quad (1)$$

- Continue to accumulate samples during PWM with SOCR = 1.
- Keep digitalized value when the channel is turned off.

5.3 Digital diagnostic

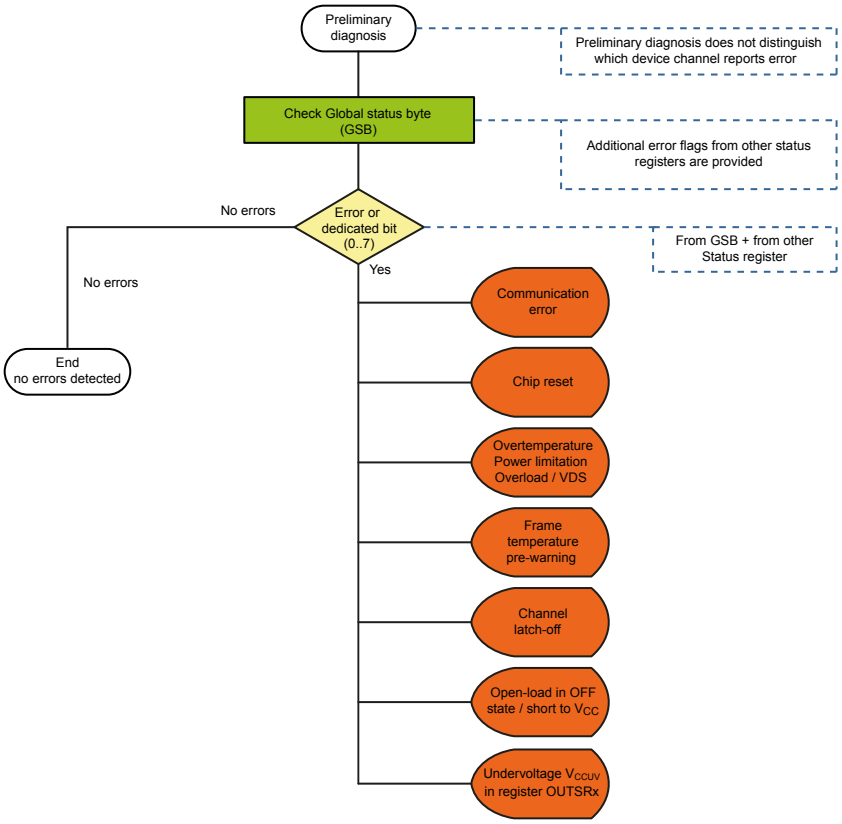
The global status byte (GSB) provides the preliminary status of the device during the SPI communication with the device. It informs about the device actual mode (normal/fail-safe).

Figure 29. Diagnostic registers



By reading the additional status registers, more detailed information is provided. Status information is stored in the status registers.

Figure 30. **Status registers**



5.3.1 Status register

Table 44. **Status register**

Address	Name	Access	Description
20h to 23h	OUTSRx	Read/Clear	Outputs status Register (see register map for detailed description).
28h to 2Bh	ADCxSR	Read	Digital current sense registers.
31h	ADC9SR	Read	Digital case temperature sensor voltage sense register.

5.4 Overload (VDS high voltage, overload - OVL)

Detection of potential overload condition can be performed monitoring the digital current sense registers (ADCxSR). On top of that, the voltage drop on the PowerMOS output stage of each channel is monitored:

- If V_{DS} (voltage across PowerMOS output stage) exceeds the threshold defined by the parameter (V_{CC} - V_{DSH_TH}), an overload condition is detected. In this case, the corresponding real time bit VDSHSRx of the OUTSRx registers (addresses from 20h to 23h) is set.
- If V_{DS} is lower than the threshold (V_{CC} - V_{DSH_TH}), this bit is automatically reset.

To avoid false fault indications, it is recommended to perform this check when the channel is in a permanent on-state condition.

5.5 Open-load on-state detection

The open-load ON-state is performed by reading the digital current sense.

5.6 Open-load off-state detection

After the channel is completely OFF, if the output voltage V_{OUT} exceeds the open-load detection threshold voltage V_{DSH_TH}, an open-load OFF-state/Stuck to V_{CC} event is detected.

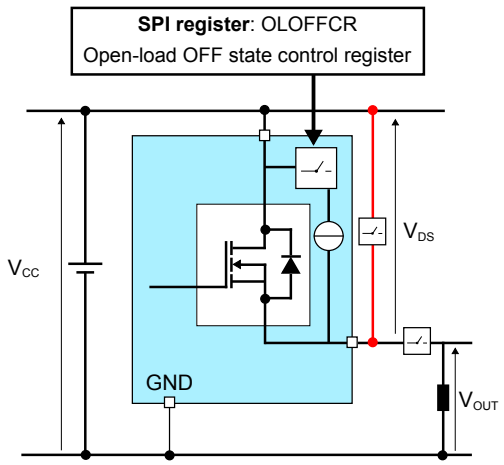
It is possible to monitor the voltage drop on the PowerMOS per each channel, checking the content of the corresponding real time bit VDSHSRx in the OUTSRx registers (addresses from 0x20h to 0x23h). When channel x is in off-state, if VDS is lower than the threshold (V_{CC} - V_{DSH_TH}), the VDSHSRx bit is low, otherwise it is in high state.

In normal operation, a low value of bit VDSHSRx in off-state must be interpreted as a potential Stuck to V_{CC} condition. However, setting OLOFFCR bit in the OUTCTRCRx register (addresses from 0x00h to 0x03h), it is possible to activate an internal pull-up current generator for the corresponding channel x. In this case a low value of bit VDSHSRx in off-state may indicate either a potential Stuck to V_{CC} or an Open load condition. In the latter case, when the internal pull-up current generator is disabled the bit VDSHSRx is high.

To avoid false fault indications, it is recommended to perform these checks when the channel is in a permanent off-state condition.

The pull-up current generators can be activated in normal, fail-safe and pre-standby modes; whilst they are switched off in standby mode. Either a HW or SW reset (V_{REG} < V_{POR} respectively FFh command byte) clears all register contents and hence the current generators are switched off.

Figure 31. Open-load OFF-state detection



GADG1004171620PS

Table 45. V_{DSHSR} state in a permanent off-state condition

Case	VDSHSR state in a permanent off-state condition	
	With internal pull-up generator	Without internal pull-up generator
Case 1: load connected	"1" / no fault condition	"1" / no fault condition
Case 2: no load	"0" / fault	"1" / no fault signal
Case 3: output shorted to V_{CC}	"0" / fault	"0" / fault

5.7 Direct input status bits in OUTSRx (DIENSR)

The DIENSR bits read back the logic level of the DIx input assigned through OTP to the specific channel.

5.8 Channel feedback status bit in OUTSRx (CHFBSR)

The CHFBSRx bit provides a logical "OR" combination of PL, OT failure flags related to OUTPUTx. If CHFBSRx bit is set, the channel OUTPUTx is failing, otherwise, NO failure is present. The bits are refreshed continuously in ON-state and latched in OFF-sate. In order to clear the bit in OFF-state, a Read&Clear command has to be performed.

5.9 Channel latch-off status bit in OUTSRx (CHLOFFSR)

The CHLOFFSR bit (one per channel) is set as soon as there is a fault condition identified as Power-limitation or over-temperature.

In case a latch-off condition occurs, the faulty channel can be reactivated after clearing the related CHLOFFSR bit through a write operation. A SW reset event clears the content of the register.

6 Programmable blanking window (PBW)

Dedicated registers (CHLOFFTCR1 and CHLOFFTCR0) per channel provide a variable and programmable blanking window ($t_{BLANKING}$) in case of power limitation or overtemperature event. During this period, the corresponding channel is in auto-restart mode and the channel is allowed to stay in power-limitation and/or overtemperature state. Once the blanking time has expired, the channel is latching off if the cause of the power limitation or overtemperature event is still present. In this case the channel latches off and the related flag in the latch-off error register (CHLOFFSR) is set. Latch-off flag is also reported in the Global Status Byte (see Global Status byte description).

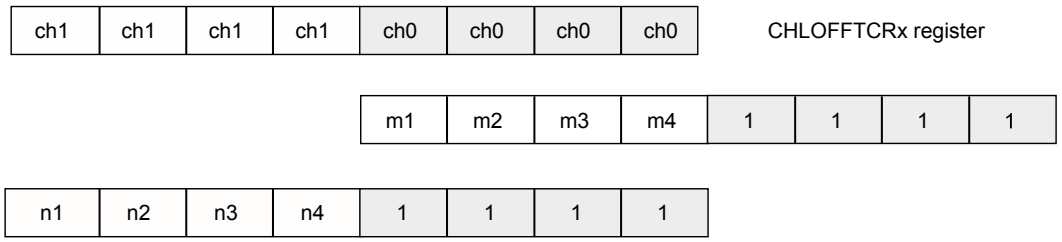
If during the blanking time the cause of power limitation and/or overtemperature event disappears, the timer stops then the rest of the blanking time will be available for another power limitation and/or overtemperature event. Therefore it is up to MCU to reset the timer by refreshing the programmed value in the dedicated register (CHLOFFTCR1 or CHLOFFTCR0).

MCU can keep the device in auto-restart forever artificially, by refreshing the programmed blanking time.

6.1 Timer

The 4-bit value per channel written in the registers CHLOFFTCR1 or CHLOFFTCR0 is translated internally into an 8-bit value. The four MSB of this 8-bit value correspond to the content of CHLOFFTCRx register, while the four LSB are filled with 0xF. The 8-bit value refers to an analogue timer value.

Figure 32. Internal timer process



The granularity of the 8-bit counter is t_{STEP}. At each power limitation or overtemperature event, the 8-bit counter is decreased by the number of steps equal to the duration of power limitation or overtemperature event. If power limitation or overtemperature phase lasts for less than t_{STEP} the counter is decreased by one step.

After each downcount of the 8-bit register, the 4 MSB bits will be transferred to the 4 bits of the corresponding CHLOFFTCRx register in order to refresh this register to the new value of the timer. The microcontroller can read only the 4 MSB bits content of the register. In consequence, the microcontroller can detect a change of every 16 steps of downcounting.

The Timer down-counts, if the flag is set as the consequence of the event of power limitation or overtemperature.

At the end of the timer’s step, the flag is checked. It will be reset if the event is not present.

The Timer stops down-counting, each time the event has disappeared, or if the channel is turned into OFF state.

This option doesn't include the one step down-counting if the flag is set for the first time.

If the event is not present, the Timer will stop down-counting and will reset the flag.

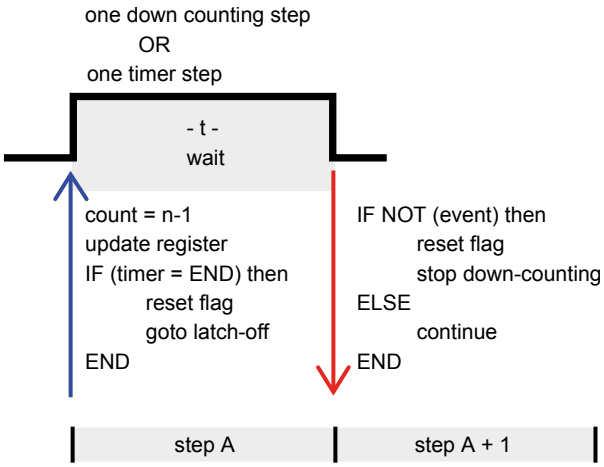
In case the Timer reaches the ZERO, the system goes to the latching off state and the related flag in the latch-off error register is set.

Downcounting is stopped and the content of the 8-bit counter is frozen, when the channel is commanded off through the Direct Input or the SOCR register. The Timer can stay with an already down-counted value for a long time. It is up to the MCU to reset it.

MCU can keep the device in auto-restart mode forever artificially, by refreshing the timer register value so not to reach Zero.

The Figure 33 is related to the one timer step. The actions are performed after the rising and falling edges.

Figure 33. **One timer step actions**



6.2 Blanking window values

The range of the configurable blanking window is shown in Table 46.

- 0x0: it configures the channel in latch-off mode in case of event without blanking time. Consequently, the channel will latch-off upon the first occurrence of power limitation or overtemperature event.
- 0x1 to 0xF: this value represents the time duration; it will be written by MCU in the register (latch-off timer register). During this time, the device is allowed to stay in power-limitation and/or over-temperature state before latching off if the “event” is still active or present.

The minimum value of the timer, known as Zero, is 0x0F. When the timer reaches this value, the latch-off action will be triggered.

The following table shows the time values written by the MCU and their real value in the Timer Register.

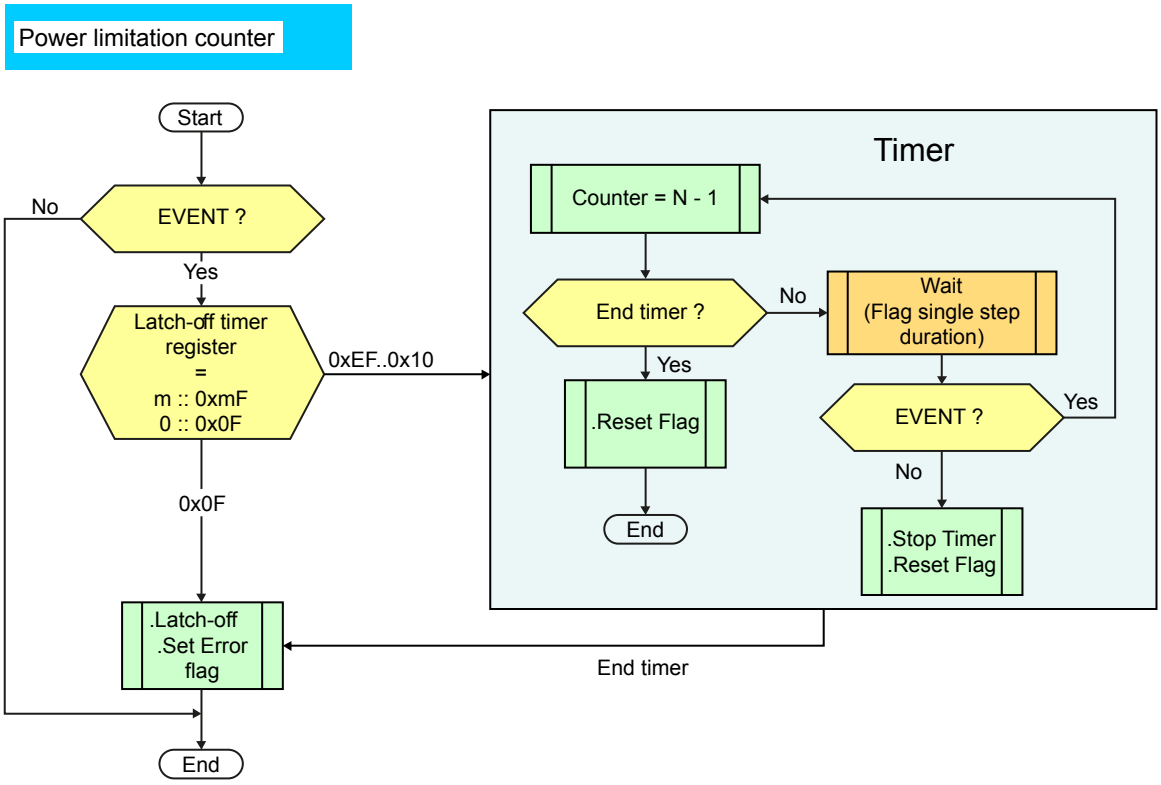
Table 46. **Blanking window values configurations**

Bit 7 or bit 3	Bit 6 or bit 2	Bit 5 or bit 1	Bit 4 or bit 0	0xm	0xmF	Typical value of $t_{blanking}$
0	0	0	0	0x0	0xF	latch-off (ZERO)
0	0	0	1	0x1	0x1F	16 ms
0	0	1	0	0x2	0x2F	32 ms
0	0	1	1	0x3	0x3F	48 ms
...				0x4	0x4F	64 ms
...				...	...	...
1	1	1	0	0xE	0xEF	224 ms
1	1	1	1	0xF	0xFF	240 ms

6.3 Power limitation counter

The flowchart below displays the flow of the events and states. It does not include the timer update by MCU.

Figure 34. Power limitation counter flowchart



6.4 Fail-safe mode

In fail-safe mode, the device is in unlimited auto-restart operation. The blanking time window has no effect on the duration of the auto-restart. The timers in the fail-safe mode are frozen and inactive.

This ensures full independence of the fail-safe mode of operation.

6.5 Registers

For more details refer to the SPI register and diagnostics.

- Address 010h - Channel latch-off Timer Control Register (CHLOFFTCR0)
- Address 011h - Channel latch-off Timer Control Register (CHLOFFTCR1)

Two 16-bit registers (latch-off timer: R/W) are used for the channel behavior configuration and the timer value setting.

For each channel 4 bits are used. The value is written by MCU from 0x0 to 0xF.

Figure 35. Example of behavior channel configuration

Dual device

ch1	ch1	ch1	ch1	ch0	ch0	ch0	ch0

Latch-off timer register access:

- Write command - store new value, read-back (during write command) old value equal to the timer down-counting.
  - Any write command will clear the flag in the latch-off flag register and reset the timer.
  - This function will be used by MCU to clear the flag in the latch-off flag register, which is a read only register.
- Read command - read currently down-counted timer value. If the channel was latched because of timer expiration, the channel is kept latched after read command.
- Channels latch-off status bit - CHLOFFSRx in OUTSRx. Each channel has one CHLOFFSR flag. In case of latch-off of a channel, this flag will be set and readable by MCU. This bit must be cleared to allow the channel to resume operation through a read/clear operation.

6.6 Digital power management

A new pin (V_{REG}) has been added, to supply the digital part. V_{DD} pin remains in charge for digital I/O and pins supplying to be compatible with system architecture. A capacitor in series with a resistance may be externally connected to V_{REG} pin (vs device GND) to sustain digital part power supply in case of fast battery interruption. The capacitor is charged at a pre-regulated voltage (4.7 V) directly from internal battery reference.

In case V_{DD} regulated voltage is supplied, an external switchable diode (see Section 13: Application schematics) may be connected between V_{DD} pin (anode) and V_{REG} pin (cathode).

7 Capacitive charging mode (CCM)

The capacitive charging mode (CCM) is an operative condition, available in both fail-safe and normal device states, with channels configured in bulb mode. The procedure to enter CCM is described below:

- Device in fail-safe mode:
  - If MCUext = 1, after 5 consecutive rising edges on DI0 and/or DI1 pins within 240 µs, the corresponding channels will enter CCM, according to DIx OTP configuration.
  - If MCUext = 0, after 5 consecutive rising edges on DI1 pin within 240 µs, according to OTP mapping, relevant channels shall enter CCM.
- Device in normal mode:
  - Set the CAPCRx bit in the SOCR register to enter CCM.

The parameters related to CCM are reported in Table 69.

During CCM, the following behaviors are applied:

- Harness protection is disabled.
- Latch-off delay time after TSD ($t_{D\_RESTART}$) is disabled.

The CCM is automatically aborted after t_{CCM_DIS} in both fail-safe and normal states. In normal mode the CCM can be aborted also through an SPI communication, setting the EXIT_CAPCRx bit in the SOCR register, whenever within the t_{CCM_DIS} time frame.

The capacitive charging mode charges capacitors with a burst of I_{CCM} pulses, provided that the total impedance is low enough to reach I_{CCM} when charging the capacitor. If I_{CCM} is not reached, the capacitor is charged with a single continuous charging pulse.

When a channel is set in capacitive charging mode and the output stage is turned on, an auto-restart procedure is started. If the ESR of the connected capacitor and the total output line impedance is low enough to let the channel reach its I_{CCM} value, the channel will turn off after the differential thermal threshold of ΔT_{PLIM_CCM} has been reached and autonomously turned on again after the differential thermal hysteresis goes below $\Delta T_{PLIM\_CCM\_HYST}$ = ΔT_{PLIMR} threshold. In this operating mode a smooth capacitor charging with low, moderate RMS current is enabled allowing to disable the I^2t wire harness protection IP in this channel operating mode. Thanks to the lower values of ΔT_{PLIM_CCM} and I_{CCM} compared to normal operating mode, capacitor charging mode is compatible with capacitors up to C_{MAX} even in high ambient temperature conditions.

8 Parallel mode

Parallel mode may be enabled by setting the corresponding OTP bit to 1 (by default, it is disabled).The CH2 and CH3 continue to work as individual channels.

During parallel mode, the CH0 and CH1 are driven by the only DIx associated to CH0 (depending on DIx assignment logic configured through OTP).

When this bit is set high, CH1 control register bits are automatically linked to CH0 values, thus CH1 is programmed exactly as CH0. This means that:

- Every control command addressed to CH0 is reflected also to CH1.
- Every control command addressed to CH1 is ignored.
- Every configuration set addressed to CH0 is reflected also to CH1.
- Every configuration set addressed to CH1 is ignored.
- LED mode is disabled for CH0 and CH1.
- Each channel protection is separated and active, and their triggering impacts both channels (for instance, a thermal shutdown event on CH1 turns off CH0 and CH1 at the same time).
- Each channel diagnostic stays separate on their own registers.
- Current sense architectures stay separate as well as ADC conversions.
- Harness protection is active, merged, and adapted to parallel mode:
  - t_{NOM} as per the one programmed for CH0.
  - I_{NOM} setting for both channels come from CH0 one (the I_{NOM} table is automatically doubled).

Parallel mode cannot ensure double energy capability due to the natural difference between the clamp structures. Thus, an external free wheeling diode is suggested when enabling this function.

When parallel mode is selected, only the bulb functionality is available (LED mode is internally disabled, whatever is the logic state of this bit).

9 Standby-on functionality for parking mode

During the sleep mode, the device is able to support the parking mode functionality. In case one or more OUTPUT pins are pulled up to battery by an external secondary switch (for instance the L99SP08 which is delivering the requested current to the load) the device offers a very low current consumption (I_{SOFF2}).

For further information refer to the application note AN6371 - Interaction of L99SP08 with dual (VNF9DxxSF) and quad (VNF9Q20SF) M09 monolithic eFuses.

The device leaves this condition when the STDBY_NOT pin and the relevant DIx pin are raised up from the external logic and the device is woken up and relevant channels are turned on (in case the requested current from the load exceeds the secondary external switch configurable threshold).

In this condition the channels switch on in less than 100 µs.

10 Safety-related functions

Two built-in self-tests (BIST) have been implemented in VNF9Q20SF to automatically check the ADC conversion and I²t comparators health along the device working life. The two BISTs are contemporarily executed, as soon as V_{CC} is present (the device leaves the start phase).

10.1 ADC BIST

At each power on reset the ADC BIST is executed after POR (V_{REG} > V_{POR}), not blocking the channels turn on. It is possible to launch the ADC BIST on demand by setting the ADC_BIST_TRIG bit in the channel control register (SOCR). It is not required to have all channels off to launch the ADC BIST, but the output current conversion is not occurred during BIST execution. During the execution of that sequence, current sense reading is disabled and a multiplexer will pass a low reference current IBIST_MIN for combination <0, 0>, a medium reference current IBIST_MID for combination <0, 1> and a high reference current IBIST_MAX for combination <1, 0>.

Table 47. ADC built in self-test

adc_bist <1>	adc_bist <0>	IBIST	Expected analog current
0	0	IBIST_MIN	50 µA
0	1	IBIST_MID	200 µA
1	0	IBIST_MAX	550 µA
1	1	IVFRAME	Dependent on frame temperature

The ADC conversion results are stored into three distinct R&C registers:

- Address 0x32h - Digital Current for self-test (Low Level) (ADCLSR)
- Address 0x33h - Digital Current for self-test (Medium Level) (ADCMSR)
- Address 0x34h - Digital Current for self-test (High Level) (ADCHSR)

The microcontroller validates the expected conversions in the fail-safe state before activating the channels.

During ADC BIST execution the channels are released and could be switched on, even if no output current sampling is executed through the ADC.

A R&C command should be sent to these registers to check for any stuck bit.

Configuration <1, 1> (default one) will end the BIST procedure by redirecting the multiplexer output current to the IVFRAME. It is kept until the next power on reset.

Table 48. ADC BIST conversion results

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
IBIST_MIN	IBIST low conversion result	ADC BIST at POR; V_{CC} =13 V;	-12%	81	12%	
IBIST_MID	IBIST mid conversion result	ADC BIST at POR; V_{CC} =13 V;	-10%	325	10%	
IBIST_MAX	IBIST high conversion result	ADC BIST at POR; V_{CC} =13 V;	-8%	890	8%	
ADC_bist_{exec}	ADC BIST execution time	ADC BIST at POR; V_{CC} =13 V;		100		µs
$I2t\_bist_{exec}$	I²t BIST execution time (channels off)			60	70	µs

10.2 I²t curve BIST

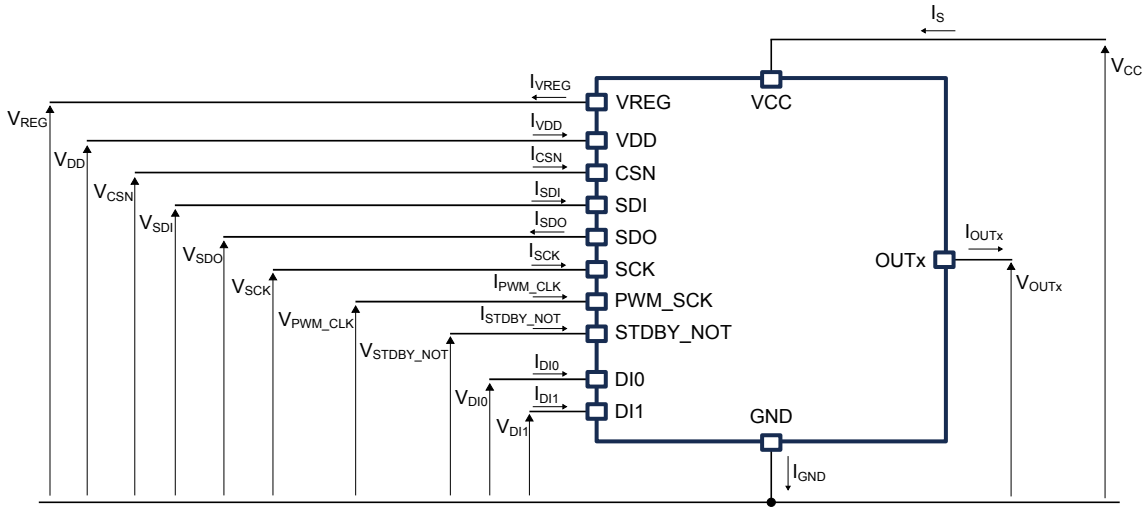
At each power on reset, the I²t BIST is executed after POR (V_{REG} > V_{POR}), not blocking channels turn on. It is possible to launch I²t BIST on demand by setting the I2t_BIST_TRIG bit in the channel control register (SOCR), but it is required to have all channels off to execute this BIST. When I2t_BIST_TRIG is set high, the I²t BIST is not executed if at least one channel is on, and the I2t_BIST_TRIG bit is automatically reset at the next clock pulse. Thus, before executing I²t BIST, it is required to check that all channels are in off state.

If the I²t BIST result is the expected one, the corresponding bit in the ITSTSR register (address 0x36h) is set high, otherwise it is set low.

During the execution of the I²t BIST on demand, all channels are disabled till the completion of the procedure. They are allowed to turn on after I²t BIST execution time (~60 µs), after standby transition.

11 Electrical specifications

Figure 36. **Current and voltage conventions**



11.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 49 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 49. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC\ LSC}$	Maximum supply voltage for full short-circuit protection	18	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
V_{CC}	DC supply voltage	35	V
$-V_{CC}$	Reverse DC supply voltage (without external components)	0.3	V
$I_{OUT0,1,2,3}$	Maximum DC output current	Internally limited	A
$-I_{OUT0,1,2,3}$	Reverse DC output current	11	A
I_{PWM_CLK}	DC PWM_CLK pin current	+3/-1	mA
V_{SDO}	DC SPI pin voltage	V_{DD} + 0.3	V
$-V_{SDO}$	Reverse DC SPI pin voltage	0.3	V
I_{SDO}	SDO pin current (as per LV124 / ISO 16750-2) t ≤ 2 min	54	mA
$I_{SDI,CSN,SCK}$	DC SPI pin current	+10/-1	mA
I_{DD}	DC VDD pin current	+10/-1	mA
	DC supply current (as per LV124 / ISO 16750-2) t ≤ 2 min	80	mA
V_{DD}	DC SPI I/O control supply	6	V
$-V_{DD}$	Reverse SPI I/O control supply	0.3	V
$I_{DI0,1}$	DC direct input current	+10/-1	mA
I_{VREG}	DC VREG pin current	-10/1(1)	mA

Symbol	Parameter		Value	Unit
V_{VREG}	DC digital control supply		6	V
$-V_{VREG}$	Reverse digital control supply		0.3	V
I_{VSTDBY_NOT}	DC STDBY_NOT pin current		+10/-1	mA
V_{STDBY_NOT}	DC STDBY_NOT pin voltage		6	V
$-V_{STDBY\_NOT}$	Reverse DC STDBY_NOT pin voltage		0.3	V
I_{LATCH_UP}	Latch up current		±20	mA
E_{MAX}	Maximum switching energy (single pulse); T_{Jstart} = 150 °C, LED mode		3	mJ
	Maximum switching energy (single pulse); T_{Jstart} = 150 °C, Bulb mode		14	
ESD	Electrostatic discharge (ANSI-ESDA-JEDEC-JS-001-2014)	$DI_{0,1}$	2000	V
		V_{DD}, V_{REG}, STDBY_NOT	2000	V
		CSN, SDI, SCK, SDO	2000	V
		$OUT_{0,1,2,3}$	4000	V
		V_{CC}	4000	V
T_J	Operating junction temperature range		-40 to 150	°C
T_{stg}	Storage temperature range		-55 to 150	°C

1. *Internally limited in operative mode.*

11.2 Thermal data

Table 50. Thermal data

Symbol	Parameter	Typ. value	Unit
R_{thJB}	Thermal resistance, junction-to-board (JEDEC JESD 51-8)	8.6	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	See Figure 48	°C/W

11.3 SPI electrical characteristics

2.7 V < V_{DD} < 5.5 V, 7 V < V_{CC} < 28 V, -40 °C < T_J < 150 °C, unless otherwise specified.

Table 51. DC characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD} and V_{REG} pins						
V_{DD}	Operating digital I/O pins supply				5	V
V_{DD_TH}	Low Voltage Detection Threshold		1.2	1.8	2.4	V
I_{VDD}	Digital I/O pins supply current in normal mode	V_{DD} = 5 V; SPI active without frame communication		11	20	µA
$I_{VDDstdby}$	Digital part supply current in standby state	V_{DD} = 5 V; T_J = 125 °C; DIx = 0 V		11	20	µA
V_{REG}	Digital Logic Supply		4.25	4.7	5.20	V
$V_{REG\_POR\_H}$	Digital Logic supply, Power-on reset threshold. Device leaves the sleep mode. Supply of digital part is reset.	V_{REG} increasing; V_{CC} > V_{USD}	1.65	2.15	2.65	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{REG\_POR\_L}$	Power-on shutdown threshold. Device enters sleep mode. Supply of digital part in shutdown.	V_{REG} decreasing; $V_{CC} > V_{USD}$	1.4	1.9	2.4	V
$V_{REG\_POR\_HYST}$	Power-on reset hysteresis			0.15		V
I_{VREG}(1)	Digital part supply current during temporary battery disconnection	SPI active without frame communication		-1.5		mA
I_{VREG_OUT}	I_{VREG} during transient external capacitor charging	V_{REG} increasing; $V_{CC} > V_{USD}$		35	55	mA
SDI, SCK, PWM_CLK pins						
I_{IL}	Low level Input current	$V_{SDI,SCK}$ = 0.3 V_{DD}	1	-	10	µA
I_{IH}	High level Input current	$V_{SDI,SCK}$ = 0.7 V_{DD}	1		10	µA
V_{IL}	Input low voltage				0.3 V_{DD}	V
V_{IH}	Input high voltage		0.7 V_{DD}			V
V_{I_HYST}	Input hysteresis voltage			0.5		V
V_{SDI_CL}	SDI clamping voltage	I_{IN} = 1 mA	6		8.2	V
V_{SDI_CL}	SDI clamping voltage	I_{IN} = -1 mA		-0.7		V
V_{SCK_CL}	SCK clamping voltage	I_{IN} = 1 mA	6		8.2	V
		I_{IN} = -1 mA		-0.7		V
V_{PWM_CLK}	PWM_CLK clamping voltage	I_{IN} = 1 mA	6		8.2	V
		I_{IN} = -1 mA		-0.7		V
SDO pin						
V_{OL}	Output low voltage	I_{SDO} = -5 mA; CSN low; fault condition			0.2 V_{DD}	V
V_{OH}	Output high voltage	I_{SDO} = 5 mA; CSN low; no fault condition	0.8 V_{DD}			V
I_{LO}	Output leakage current	V_{SDO} = 0 V or V_{DD}, CSN high	-5		5	µA
CSN pin						
I_{IL_CSN}	Low level Input current	V_{CSN} = 0.3 V_{DD}	-10			µA
I_{IH_CSN}	High level Input current	V_{CSN} = 0.7 V_{DD}			-1	µA
V_{IL_CSN}	Output low voltage				0.3 V_{DD}	V
V_{IH_CSN}	Output high voltage		0.7 V_{DD}			V
V_{HYST_CSN}	Input hysteresis voltage			0.5		V
V_{CL_CSN}	CSN clamping voltage	I_{IN} = 1 mA	6		8.2	V
		I_{IN} = -1 mA		-0.7		V

1. *Parameter evaluated by characterization, not tested in production.*

Table 52. AC characteristics (SDI, SCK, CSN, SDO)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{OUT}(1)	Output capacitance (SDO)	V_{OUT} = 0 V to 5 V	-	-	10	pF
C_{IN}(1)	Input capacitance (SDI)	V_{IN} = 0 V to 5 V	-	-	10	pF
	Input capacitance (other pins)	V_{IN} = 0 V to 5 V	-	-	20	pF

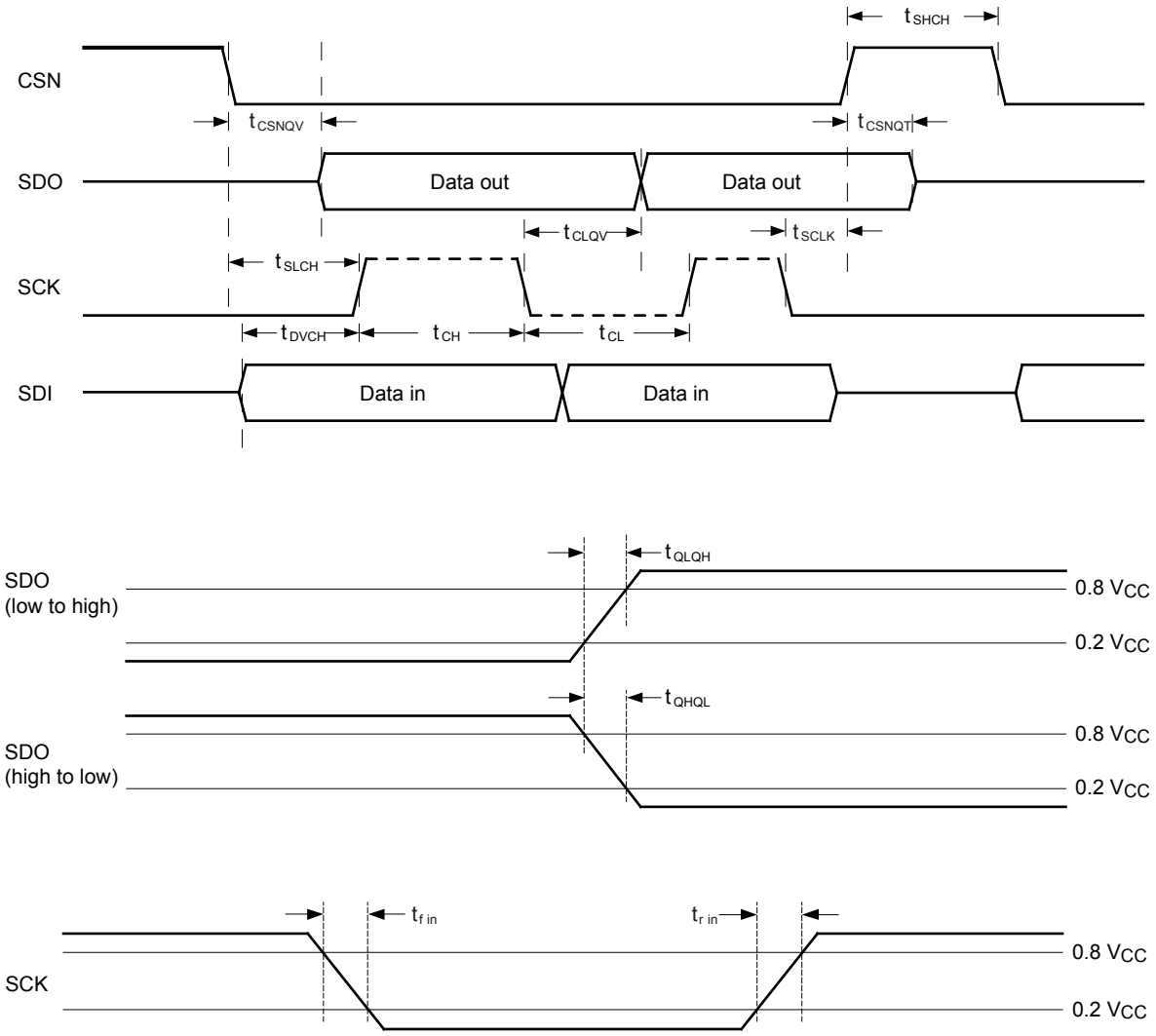
1. *Parameter specified by design, not tested in production.*

Table 53. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_C	SPI clock frequency	Duty cycle = 50%	2	4	8	MHz
t_{WHCH}	CSN timeout: time to release SDO bus		30		70	ms
t_{WDTB}	Watchdog toggle bit timeout		30	-	70	ms
t_{SLCH}(1)	CSN low setup time		60			ns
t_{SHCH}(1)	CSN high setup time		600			ns
t_{DVCH}(1)	Data in setup time		10			ns
t_{CHDX}(1)	Data in hold time		15			ns
t_{CH}(1)	Clock high time		60			ns
t_{CL}(1)	Clock low time	-	60	-	-	ns
t_{CLQV}(1)	Clock low to output valid	COUT = 1 nF		75		ns
t_{QLQH}(1)	Output rise time	COUT = 1 nF		55		ns
t_{QHQL}(1)	Output fall time	COUT = 1 nF		55		ns
t_{WU}	Rising edge of V_{REG} to first allowed communication		3		26	µs
$t_{stdby\_out\_CSN}$	Minimum time during which CSN must be toggled low to go out of STDBY mode		2	15	120	µs
$t_{stdby\_out\_STBYNOT}$	Minimum time during which STBY_NOT must be toggled high to go out of STDBY mode		2	15	120	µs
t_{SCLK}(1)	SCK setup time before CSN rising		20			ns
t_{CSNQV}(1)	CSN low to output valid				200	ns
t_{CSNQT}(1)	CSN high to output tristate				200	ns

1. *Parameter specified by design, not tested in production.*

Figure 37. **SPI dynamic characteristics**



11.4 Electrical characteristics

7 V < V_{CC} < 28 V, –40 °C < T_J < 150 °C, unless otherwise specified.

Table 54. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown	V_{CC} decreasing		2	2.7	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.1		V
$V_{USDreset}$	Undervoltage shutdown reset	V_{CC} rising			3	V
V_{clamp}	V_{CC} clamp voltage	I_{CC} = 20 mA, $I_{OUT0,1,2,3}$ = 0 A, T_J = -40 °C	35			V
		I_{CC} = 20 mA, $I_{OUT0,1,2,3}$ = 0 A, 25 °C < T_J < 150 °C	36	38	45	V
I_{SOFF}	Supply current	Sleep mode; V_{CC} = 13 V; T_J = 25 °C; V_{OUTx} = open		0.1	0.8	µA
		Sleep mode; V_{CC} = 13 V; T_J = 125 °C; V_{OUTx} = open			8	µA
I_{SOFF2}	Supply current	Sleep mode, V_{CC} = 13 V, V_{OUTx} = V_{CC} (per channel)			15	µA
I_{SON}	Supply current in active mode (device in fail-safe or normal mode)	ON-state (all channels OFF), V_{CC} = 13 V, $I_{OUT0,1,2,3}$ = 0 A		4	5.5	mA
ΔI_{Son}	Additional supply current for each output in ON state driving nominal current	ON-state (per channel), V_{CC} = 13 V, $I_{OUT0,1,2,3}$ = I_{TYP}			1.95	mA
$I_{L(off)}$	OFF-state output current	V_{OUT} = open, V_{DD} = 0 V, V_{CC} = 13 V, T_J = -40 °C (total current, channels 0,1,2,3)	0	0.01	0.8	µA
		V_{OUT} = open, V_{DD} = 0 V, V_{CC} = 13 V, T_J = 125 °C (current per channel)	0		0.7	µA
$V_{F0,1,2,3}$	Output V_{CC} diode voltage(1)	V_{CC} = 13 V, -I_{OUT} = 2.5 A, T_J = 150 °C		0.7		V

1. *For each channel.*

Table 55. Logic inputs ($DI_{0,1}$ and STDBY_NOT pins)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)0,1,2,3}$	Input hysteresis voltage		0.2			V
$V_{DI0,1\_CL}$	VDI0,1 clamp voltage	I_{IN} = 1 mA	6		8.2	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DI0,1\_CL}$	VDI0,1 clamp voltage	I_{IN} = -1 mA		-0.7		V
V_{STDBY_NOT}	V_{STDBY_NOT} clamping voltage	I_{IN} = 3 mA	9		15	V
		I_{IN} = -1 mA		-0.7		V

Table 56. Digital timings

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{STDBY}	Pre-standby mode counter	-	-	100	-	µs
$t_{PRESTDBY}$	Timing needed to enter Pre-standby from fail-safe	-	-	14	-	ms
t_{FILTER_OL}	Filtering time before channel off and latched in overload	-	-	4	-	µs
$t_{D\_RESTART}$	Restart delay time after thermal shutdown event	-	-	50	-	ms

Table 57. Protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔT_{PLIM}	Junction-case temperature difference triggering power limitation protection	V_{CC} = 16 V		80		°C
ΔT_{PLIM}	Junction-case temperature difference triggering power limitation protection	V_{CC} = 19 V		55		°C
ΔT_{PLIMR}	Junction-case temperature difference resetting power limitation protection	V_{CC} = 16 V		73		°C
ΔT_{PLIMR}	Junction-case temperature difference resetting power limitation protection	V_{CC} = 19 V		48		°C
T_{TSD}	Shutdown temperature	V_{CC} = 13 V	150	175	210	°C
	Shutdown temperature (V_{CC} decreasing)(1)	V_{CC} = 2.7 V	140			°C
	Shutdown temperature during cranking (V_{CC} decreasing)(1)	V_{CC} = 3.2 V	140			°C
T_R(1)	Reset temperature	V_{CC} = 13 V, latch-off mode disabled	T_{RS} + 1	T_{RS} + 5		°C
T_{RS}(1)	Thermal reset of OTFLTR fault detection	V_{CC} = 13 V, latch-off mode disabled	135			°C
T_{HYST}(1)	Thermal hysteresis (TTSD - TR)	V_{CC} = 13 V, latch-off flag mode disabled		10		°C
$T_{CSD0,1,2,3}$(1)	Case thermal detection pre-warning	V_{CC} = 13 V	T_{CSD} nom – 10	T_{CSD} nom	T_{CSD} nom + 10	°C
T_{CR}(1)	Case thermal detection reset	V_{CC} = 13 V		T_{CSD} nom - 10		°C
V_{DS_OVL}	V_{DS} overload detection threshold		V_{CC} - 2	V_{CC} - 1.5	V_{CC} - 1	V
$V_{DS\_OVL\_HYST}$	V_{DS} overload detection threshold Hysteresis			0.2		V
$t_{Blanking}$	Programmable blanking time	(see CHLOFFTCR0)	14.4		264	ms

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

Table 58. Open-load detection (7 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DSH_TH}	Open-load OFF-state voltage detection threshold	CHx off	V_{CC} - 2	V_{CC} - 1.5	V_{CC} - 1	V
I_{PU}	Pull-up current generator for open-load at OFF-state detection	Pull-up current generator active, V_{OUT} = V_{CC}- 1.0 V	-0.3	-0.7	-1.1	mA

11.5 PWM unit

2.7 V < V_{DD} < 5.5 V; -40 °C < T_J < 150 °C, unless otherwise specified.

Table 59. PWM unit

Symbol	Parameter	Min.	Typ.	Max.	Unit
PWM_{RES}(1)	PWM resolution			0.1	%
				0.2	%
PWM_{CLK}(1)	PWM clock range	300	400	500	kHz
PWM_{CLK_FBCK}(1)	PWM clock fallback	300	400	500	kHz
$PWM_{CLK\_FBCK\_DLY}$(1)	PWM clock fallback delay	20		40	µs

1. *Parameter specified by design, not tested in production.*

Table 60. ADC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
ASC_{RES}	ADC resolution	-	10	-	bits
ADC_{CONV}	ADC conversion rate	-	10	-	kS/s

11.6 Bulb mode

7 V < V_{CC} < 28 V, –40 °C < T_J < 150 °C, unless otherwise specified.

Table 61. Bulb–Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON}(1)	ON-state resistance	I_{OUT} = 2.5 A; T_J = 25 °C		21.5		mΩ
		I_{OUT} = 2.5 A; T_J = 150 °C			44	mΩ
		I_{OUT} = 2.5 A; V_{CC} = 4 V; V_{CC} decreasing; T_J = 25 °C			37	mΩ
R_{ON_CC}	ON-state resistance in cold crancking at 25 °C	I_{OUT} = 1 A; V_{CC} = 3.2 V; V_{CC} decreasing			215	mΩ
R_{ON_Rev}(1)	R_{DSON} in reverse battery condition	V_{CC} = 13 V, T_J = 25 °C	-	21.5	-	mΩ

1. *For each channel.*

Table 62. Bulb–Switching (V_{CC} = 13 V; Normal switch mode)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{don}(1)	Turn-on delay time $Ch_{0,1,2,3}$ at T_J = 25 °C to 150 °C	Normal mode, bulb mode, DIx high, from SPI communication to 20% V_{OUT}; R_L = 5.2 Ω; SLOPECRx = 11 (default)	15	35	55	µs
t_{doff}(1)	Turn-off delay time $Ch_{0,1,2,3}$ at T_J = 25 °C to 150 °C	Normal mode, bulb mode, from SPI communication to 80% V_{OUT}; R_L = 5.2 Ω; SLOPECRx = 11 (default)	10	25	35	µs
t_{DIx_off}	FAST OFF from DIx at T_J = 25 °C to 150 °C	Normal mode, bulb mode, from DIx falling to 80% V_{OUT}; R_L = 5.2 Ω			15	µs
t_{skew}(1)	Turn-off turn-on time $Ch_{0,1,2,3}$ at T_J = 25 °C to 150 °C	Differential Pulse skew (t_{doff} - t_{don}); R_L = 5.2 Ω; SLOPECRx = 11 (default)	-45	5	55	µs
t_{CHon}	Standard switching time from wake-up to 20%V_{OUT}	Sleep mode, STDBY_NOT = DIx = 0 V to 5 V, time for V_{OUT} to reach 20% of V_{bat} R_L = 5.2 Ω; SLOPECRx = 11 (default)			150	µs
(dVOUT/dt)on(1)	Turn-on voltage slope $Ch_{0,1,2,3}$ at T_J = 25 °C to 150 °C	V_{OUT} = 2.6 V to 7.8 V; R_L = 5.2 Ω SLOPECRx = 00	0.28	0.55	0.75	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 5.2 Ω SLOPECRx = 01	0.32	0.62	0.80	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 5.2 Ω SLOPECRx = 10	0.37	0.74	0.94	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 5.2 Ω SLOPECRx = 11	0.47	1	1.4	V/µs
(dVOUT/dt)off(1)	Turn-off voltage slope $Ch_{0,1,2,3}$ at T_J = 25 °C to 150 °C	V_{OUT} = 10.4 V to 5.2 V; R_L = 5.2 Ω SLOPECRx = 00	0.20	0.52	0.70	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 5.2 Ω SLOPECRx = 01	0.31	0.6	0.89	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 5.2 Ω SLOPECRx = 10	0.4	0.75	1.1	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 5.2 Ω SLOPECRx = 11	0.46	1.12	1.6	V/µs
W_{ON}(2)	Switching losses energy at turn-on $Ch_{0,1,2,3}$	R_L = 5.2 Ω; SLOPECRx = 11 (default)		0.17	0.4	mJ
W_{OFF}(2)	Switching losses energy at turn-off $Ch_{0,1,2,3}$	R_L = 5.2 Ω; SLOPECRx = 11 (default)		0.14	0.25	mJ

1. See *Figure 38. Switching characteristics.*
2. *Parameter specified by design and evaluated by characterization, not tested in production.*

Table 63. Bulb–Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{LIMH\_ch0,1,2,3}$(1)	DC short-circuit current	V_{CC} = 16 V, T_J = -40 °C	-15%	36.5	15%	A
		V_{CC} = 16 V, T_J = 150 °C	-15%	29	15%	A
$I_{LIMH\_ch0,1,2,3}$ at 19 V	DC short-circuit current	V_{CC} = 19 V, T_J = -40 °C	-15%	29	15%	A
		V_{CC} = 19 V, T_J = 150 °C	-15%	23	15%	
$I_{LIMH\_ch0,1,2,3}$ at 22 V	DC short-circuit current	V_{CC} = 22 V, T_J = 25 °C		12		A
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 1 A; $V_{IN0,1,2,3}$ = 0 V;	V_{CC}–36	V_{CC}–38	V_{CC}–45	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		L = 6 mH; 25 °C < T_J < 150 °C				

1. *$I_{LIMH\_ch0,1,2,3}$ ensured between 7 V and 16 V, -40 °C < T_J < 150 °C.*

Table 64. Bulb–Digital current sense (7 V < V_{CC} < 18 V, channel 0–3; T_J = -40 °C to 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_{OL}	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 90 mA	-65%	79.5	65%	1/A
K_{BULB}	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 150 mA	-35%	77.7	35%	1/A
K_0	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 0.5 A	-15%	77.7	15%	1/A
K_1	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 2.5 A	-8%	79	8%	1/A
K_2	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 7.5 A	-7%	79	7%	1/A
I_{OUT_OFFSET}(1)	Output current offset (already included in the precision of the K factors above specified)	I_{SENSE} = 000H	-45		45	mA
$I_{OUT\_SAT\_BULB}$	Output saturation current in bulb mode	I_{SENSE} = 3FFH	9.5			A
$t_{ON\_CS(min)\_Bulb}$(1)	Minimum ON time for digital current sense availability				280	µs

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

11.7 LED mode

7 V < V_{CC} < 18 V; -40 °C < T_J < 150 °C, unless otherwise specified.

Table 65. LED–Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{ON\_ch0,1,2,3}$(1)	ON-state resistance	I_{OUT} = 0.625 A; T_J = 25 °C		70		mΩ
		I_{OUT} = 0.625 A; T_J = 150 °C			176	mΩ
		I_{OUT} = 0.625 A; VCC = 4 V; T_J = 25 °C			148	mΩ
R_{ON_CC}	ON-state resistance in cold crancking at 25 °C	I_{OUT} = 310 mA; V_{CC} = 3.2 V; V_{CC} decreasing			860	mΩ

1. *For each channel.*

Table 66. LED–Switching (V_{CC} = 13 V; Normal switch mode)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{don}(1)	Turn-on delay time $Ch_{0,1,2,3}$ at T_J = 25 °C to 150 °C	Normal mode, LED mode, DIx high, from SPI communication to 20% V_{OUT}; R_L = 21 Ω; SLOPECRx = 11 (default)	5	15	25	µs
t_{doff}(1)	Turn-off delay time $Ch_{0,1,2,3}$ at T_J = 25 °C to 150 °C	Normal mode, LED mode, from SPI communication to 80% V_{OUT}; R_L = 21 Ω; SLOPECRx = 11 (default)	8	15	25	µs
t_{DIx_off}	FAST OFF form DIx at T_J = 25 °C to 150 °C	Normal mode, LED mode, from DIx falling to 80% V_{OUT} R_L = 21 Ω			15	µs
t_{skew}(1)	Turn-off, turn-on time $Ch_{0,1,2,3}$ at T_J = 25 °C to 150 °C	Differential pulse skew (t_{doff} - t_{don}); R_L = 21 Ω; SLOPECRx = 11 (default)	-32	18	68	µs
$(dV_{OUT}/dt)on$(1)	Turn-on voltage slope $Ch_{0,1,2,3}$ at T_J = 25 °C to 150 °C	V_{OUT} = 2.6 V to 7.8 V; R_L = 21 Ω; SLOPECRx = 00	0.55	1.05	1.40	V/µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$(dV_{OUT}/dt)on$[1]	Turn-on voltage slope $Ch_{0,1,2,3}$ at T_J = 25 °C to 150 °C	V_{OUT} = 2.6 V to 7.8 V; R_L = 21 Ω; SLOPECRx = 01	0.65	1.15	1.50	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 21 Ω; SLOPECRx = 10	0.80	1.4	1.80	V/µs
		V_{OUT} = 2.6 V to 7.8 V; R_L = 21 Ω; SLOPECRx = 11	0.85	1.5	2.50	V/µs
$(dV_{OUT}/dt)off$[1]	Turn-off voltage slope $Ch_{0,1,2,3}$ at T_J = 25 °C to 150 °C	V_{OUT} = 10.4 V to 5.2 V; R_L = 21 Ω; SLOPECRx = 00	0.25	0.8	1.3	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 21 Ω; SLOPECRx = 01	0.45	1	1.5	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 21 Ω; SLOPECRx = 10	0.55	1.15	1.8	V/µs
		V_{OUT} = 10.4 V to 5.2 V; R_L = 21 Ω; SLOPECRx = 11	0.6	1.4	2.5	V/µs
W_{ON}[2]	Switching losses energy at turn-on $Ch_{0,1,2,3}$	R_L = 21 Ω; SLOPECRx = 11 (default)		0.025	0.05	mJ
W_{OFF}[2]	Switching losses energy at turn-off $Ch_{0,1,2,3}$	R_L = 21 Ω; SLOPECRx = 11 (default)		0.025	0.05	mJ

1. *See Figure 38.*
2. *Parameter specified by design and evaluated by characterization, not tested in production.*

Table 67. LED–Protection and diagnosis

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{LIMH\_ch0,1,2,3}$[1]	DC short-circuit current	V_{CC} = 16 V, T_J = -40 °C	-15%	9.3	15%	A
		V_{CC} = 16 V, T_J = 150 °C	-15%	7	15%	
$I_{LIMH\_ch0,1,2,3}$ at 19 V	DC short-circuit current	V_{CC} = 19 V, T_J = -40 °C	-15%	7.2	15%	A
		V_{CC} = 19 V, T_J = 150 °C	-15%	5.6	15%	
$I_{LIMH\_ch0,1,2,3}$ at 22 V	DC short-circuit current	V_{CC} = 22 V, T_J = 25 °C	-	3	-	A

1. *$I_{LIMH\_ch0,1,2,3}$ guaranteed between 7 V and 16 V, -40 °C < T_J < 150 °C.*

Table 68. LED–Digital current sense (7 V < V_{CC} < 18 V, channel 0–3; T_J = -40 °C to 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_{OL}	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 25 mA	-65%	308.5	65%	1/A
K_{LED}	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 40 mA	-35%	303.6	35%	1/A
K_0	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 0.125 A	-15%	303.6	15%	1/A
K_1	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 0.625 A	-8%	308.2	8%	1/A
K_2	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 1.875 A	-7%	308.2	7%	1/A
I_{OUT_OFFSET}[1]	Output current offset (already included in the precision of the K factors above specified)	I_{SENSE} = 000H	-15		15	mA
$I_{OUT\_SAT\_LED}$	Output saturation current in LED mode	I_{SENSE} = 3FFH	2.5			A
$t_{ON\_CS(min)\_LED}$[1]	Minimum ON time for digital current sense availability				150	µs

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

Figure 38. **Switching characteristics**

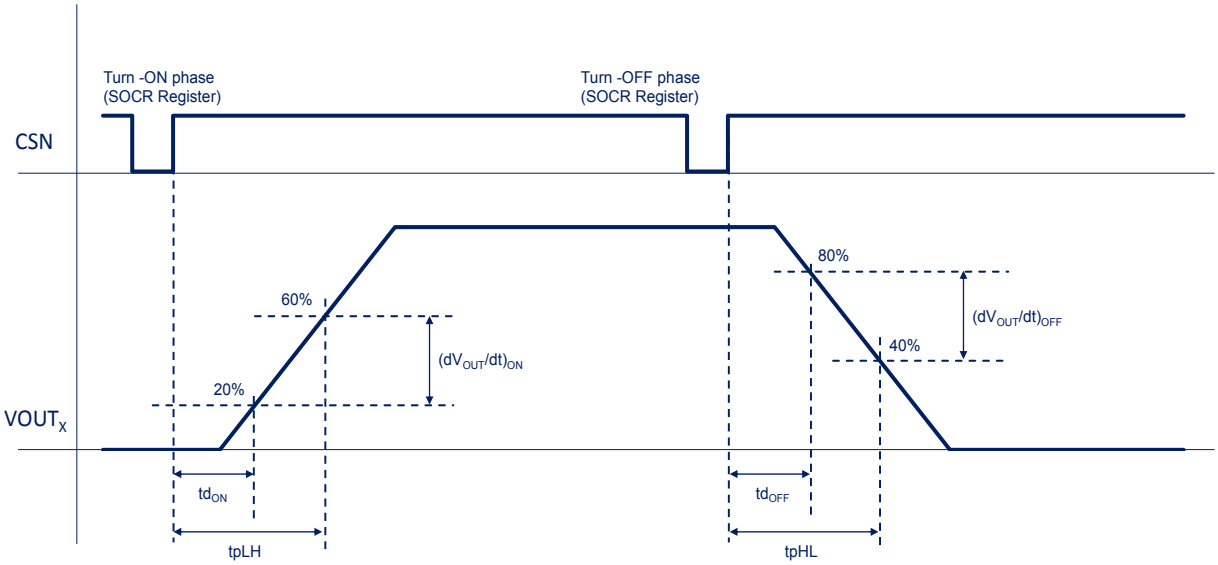


Table 69. **CCM–Capacitive loads charging mode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CCM}	Charging Current	CCM enabled Device in normal or Fail-safe mode	-	0.4*I_{LIMH}	-	A
t_{CCM_DIS}	Timing needed to leave capacitive charging mode		-	100	-	ms
t_{CCM_EN}	Timing needed to enter capacitive charging mode		-	240	-	µs
ΔT_{PLIM_CCM}	Junction-case temperature difference triggering power limitation	V_{CC} = 16 V	-	30	-	°C
C_{MAX} (1)	Max. capacitive load	V_{CC} = 16 V, T_J = 85 °C, t_{CMAX} = 50 ms, ESR = 80 mΩ	-	2.2	-	mF
		V_{CC} = 16 V, T_J = 85 °C, t_{CMAX} = 75 ms, ESR = 80 mΩ	-	2*2.2	-	

1. *Guaranteed by design and application.*

11.8 Parallel mode

7 V < V_{CC} < 28 V; -40 °C < T_J < 150 °C, unless otherwise specified

Table 70. Parallel–Power Section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R_{ON}	ON-state resistance	I_{OUT} = 5 A; T_J = 25 °C	-	10	-	mΩ
		I_{OUT} = 5 A; T_J = 150 °C	-	-	22	mΩ
		I_{OUT} = 5 A; V_{CC} = 4 V; T_J = 25 °C	-	-	18.5	mΩ
R_{ON_CC}	ON-state resistance in cold crancking at 25 °C	I_{OUT} = 2 A; V_{CC} = 3.2 V; V_{CC} decreasing	-	-	100	mΩ

Table 71. Parallel–Switching (V_{CC} = 13 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Δ_{tdon}	Turn-on delay time at T_J = 25°C to 150 °C	Fail-safe mode, parallel mode, from DIx rising to 20%V_{OUT}, R_{L0} = 5.2 Ω; R_{L1} = 5.2 Ω, SLOPECRx = 00, SLOPECRx = 01, SLOPECRx = 10, SLOPECRx = 11	-	0	-	µs
Δ_{tdoff}	Turn-off delay time at T_J = 25°C to150 °C	Fail-safe mode, parallel mode, from DIx falling to 80%V_{OUT}, R_{L0} = 5.2 Ω, R_{L1} = 5.2 Ω SLOPECRx = 00, SLOPECRx = 01, SLOPECRx = 10, SLOPECRx = 11	-	0	-	µs
Δ_{tskew}	Turn-off turn-on time at T_J = 25°C to150 °C	Differential pulse skew, R_{L0} = 5.2 Ω; R_{L1} = 5.2 Ω, SLOPECRx = 00, SLOPECRx = 01, SLOPECRx = 10, SLOPECRx = 11	-	0	-	µs
$\Delta_{(dVOUT/dt)on}$	Turn-on voltage slope at T_J = 25°C to150 °C	From V_{OUT} = 2.6 V to 7.8 V, R_{L0} = 5.2 Ω; R_{L1} = 5.2 Ω, SLOPECRx = 00, SLOPECRx = 01, SLOPECRx = 10 SLOPECRx = 11	-	0	-	V/µs
$\Delta_{(dVOUT/dt)off}$	Turn-off voltage slope at T_J = 25°C to150 °C	From V_{OUT} = 10.4 V to 5.2 V, R_{L0} = 5.2 Ω; R_{L1} = 5.2 Ω, SLOPECRx = 00, SLOPECRx = 01, SLOPECRx = 10, SLOPECRx = 11	-	0	-	V/µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ΔW_{OFF} (1)	Switching losses energy at turn-off at T_J = 25°C to 150 °C	R_{L0} = 5.2 Ω; R_{L1} = 5.2 Ω	-	0	-	mJ
ΔW_{ON} (1)	Switching losses energy at turn-on at T_J = 25°C to 150 °C	R_{L0} = 5.2 Ω; R_{L1} = 5.2 Ω	-	0	-	mJ

1. *Guaranteed by design.*

Table 72. Harness protection

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_{NOM}	I_{NOM} setting(1)	INOM2x, INOM1x, INOM0x (see FSITCRx)	000	-10%	6	10%	A
			001		1.5		
			010		2		
			011		2.5		
			100		3		
			101		3.5		
			110		4		
			111		5		
f_{CLK}	Internal time base frequency for I²t state machine				16		kHz
$t_{F\_UNLATCH}$	Minimum time for eFuse to unlatch when pulling up DI1 (FCTRL) pin when MCUext = 0				50		µs
V_{OUT_FSDx}	Fuse Current Sense - Output Voltage for Shutdown	Channelx ON			5		V
$I_{OUT\_FCS\_SATx}$(2)	Fuse current sense - Output saturation current	V_{CC} = 7 V; Channelx ON; T_J =150°C		I_{LIMH}			A
Fault diagnostic feedback							
V_{F_FAULT}	DI0 (STATUS) output voltage in fault condition when MCUext = 0	V_{CC} = 13 V; R_{STATUS_PU} = 10 kΩ; V_{STATUS_PU} = 5 V		0		300	mV
I_{F_FAULT}	DI0 (STATUS) output current in fault condition when MCUext = 0	V_{CC} = 13 V; R_{STATUS_PU} = 10 kΩ; V_{STATUS_PU} = 5 V			500		µA

1. *For each channel (in parallel mode, effectively I_{NOM} value is doubled).*
2. *Parameter evaluated by characterization, not tested in production.*

Table 73. Shut-off protection

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
$I_{shutoff}$	Shut-off current threshold $M\_x * I_{NOM}$	ISHUTOFFCR2x, ISHUTOFFCR1x, ISHUTOFFCR0x (see FSITCRx)	001	-10%	2xINOM	10%	A
			010		2.95xINOM		
			011		3.5xINOM		
			100		3.95xINOM		
			101		4.85xINOM		
			110		5.4xINOM		
			111		6.2xINOM		
			000		Disabled		
t_{shut_off}(1)	Maximum reaction time					100	µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{shut\_off\_filt}$	Minimum filter time		10	20		µs

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

12 ISO Pulse

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011(E) and ISO 16750-2:2012.

The related function performances status classification is shown in Table 74.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, with external components as shown in Figure 39.

“Status II” is defined in ISO 7637-1 Function Performed Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 74. ISO 7637-2 - Electrical transient conduction along supply line

Test pulse 2011(E)	Test pulse severity level with status II functional performance status		Minimum number of pulses or test time	Burst cycle/pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	US(1)				
1(2)	III	-112 V	500 pulses	0.5 s	5 s	2 ms, 10 Ω
2a(3)	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a(2)	IV	-220 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
4(4)	IV	-7 V	1 pulse	-	-	100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B(3)	-	+87 V	5 pulses	1 min	-	400 ms, 2 Ω

1. *US is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), see Section 5.6.*
2. *Device enters reset state and must be reinitialized.*
3. *With 35 V external suppressor referred to ground (-40 °C < T_J < 150 °C).*
4. *Test pulse in ISO7637-2:2004(E).*

13 Application schematics

Figure 39. **Application schematic**

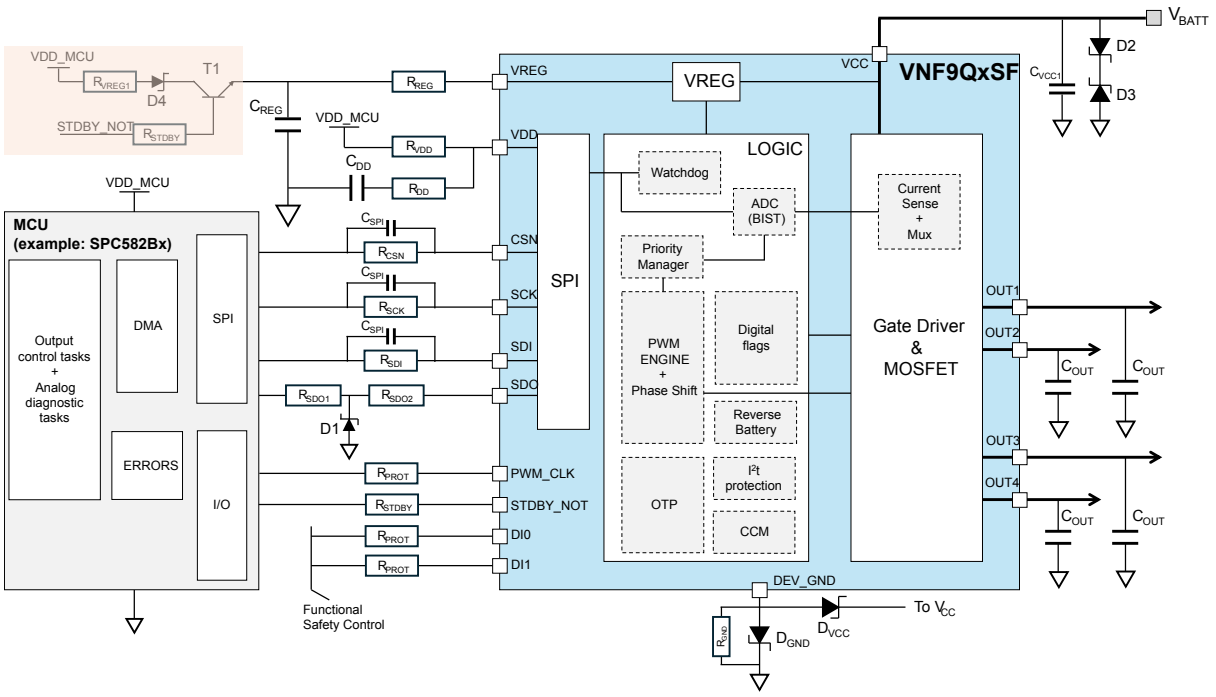


Table 75. **Component values**

Reference	Value	Comment
C_{VCC1}	100 nF	Battery voltage spikes filtering mounted close to IC
D2	SMA6F18AY	18-20 V suppressor for negative transient protection for ISO pulse 1. Place close to VCC pin
D3	Suppressor 33-36 V	33-36 V suppressor for overvoltage protection for ISO pulse 2a
D_{VCC}	1N5822 (or STPS1H100)	ISO pulse protection
D_{GND}	BAS21 (for 5 V applications) BAT54 (for 3.3 V applications)	Reverse polarity protection
R_{GND}	4.7 kΩ	
C_{OUT}	10 nF	EMC protection capacitors
R_{VDD}	330 Ω (for 5 V applications) 150 Ω (for 3.3 V applications)	Device logic protection
R_{CSN}, R_{SCK}, R_{SDI}	2.7 kΩ	Microcontroller protection during overvoltage and reverse polarity
R_{SDO2}	220 Ω	
R_{SDO1}	50 Ω	Optional protection resistor for SDO pin of the microcontroller
C_{SPI}	100 pF	Optional SPI frequency speed up capacitor
D1	BAT54	Microcontroller protection during overvoltage and reverse polarity
R_{PROT}	15 kΩ	Microcontroller protection during: overvoltage, reverse polarity, and loss of GND
R_{STDBY}	2.2 kΩ	
C_{DD}	1 nF	Capacitor acts as current source to charge MISO bus capacitance

Reference	Value	Comment
R_{DD}	100 Ω	Needed for ESD protection
C_{REG}	2.2 µF	VREG pin protection network. CREG capacitor dimension required to maintain RAM register content during ISO pulse 1/2a (1)
R_{REG}	120 Ω	
T1	BC847	
D4	BAT54	
R_{VREG}	1 kΩ	

1. *ref to ISO 7637-2:2011, with the expection of t2 ≤ 2ms (instead of 200ms) for ISO pulse 1.*

14 Maximum demagnetization energy (V_{CC} = 16 V)

Figure 40. **Maximum turn off current versus inductance – Bulb mode**

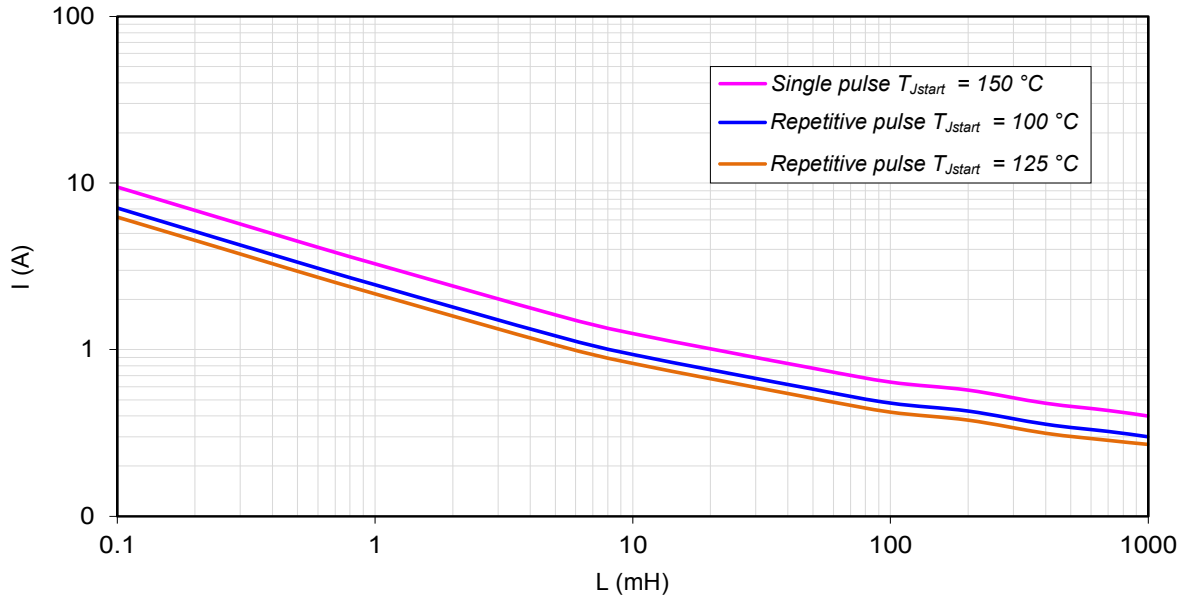


Figure 41. **Maximum turn off current versus inductance – LED mode**

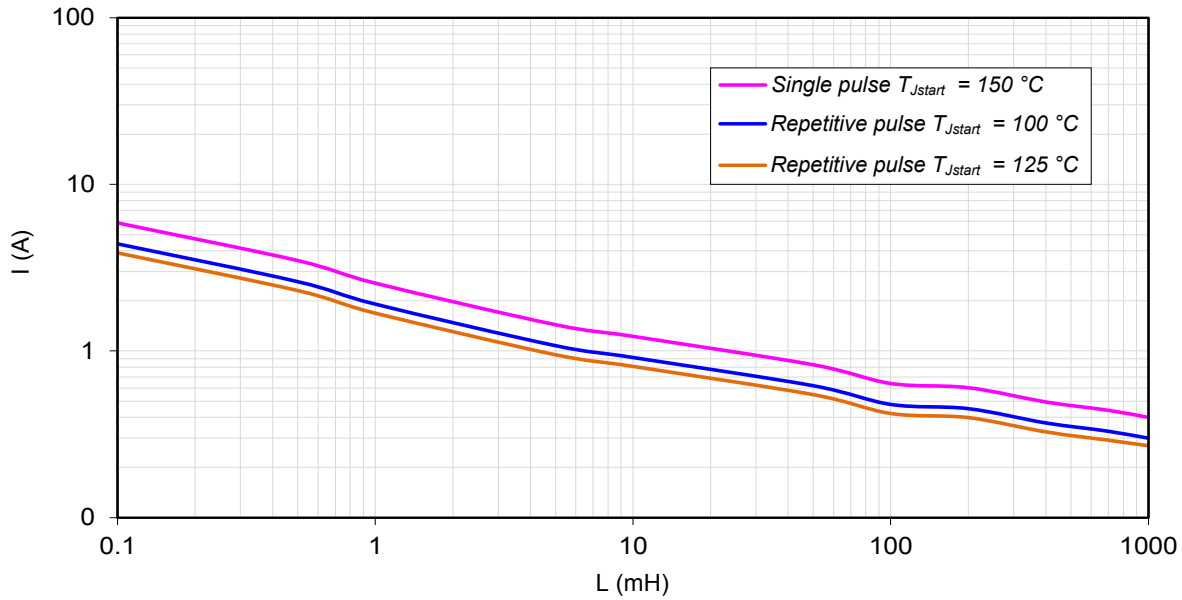


Figure 42. Maximum turn off energy versus inductance – Bulb mode

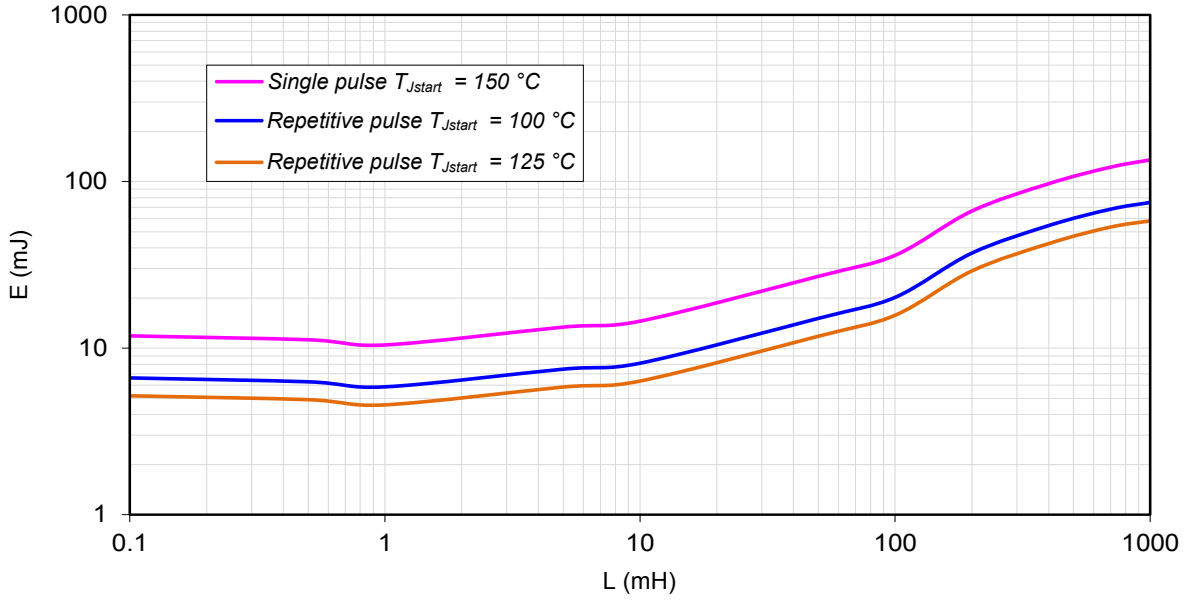
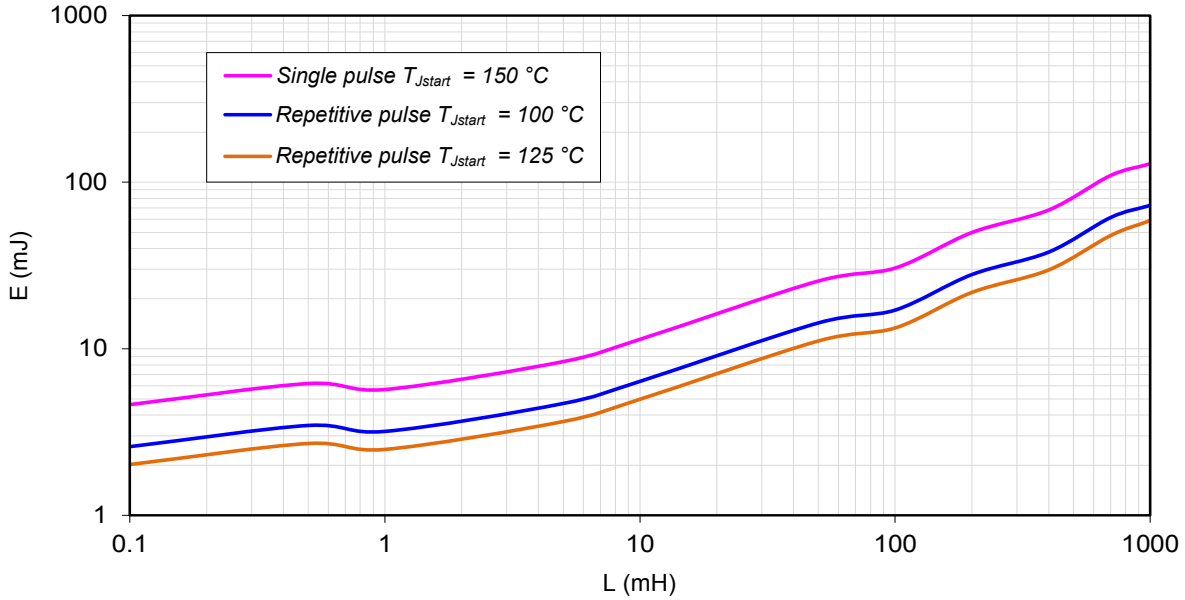


Figure 43. Maximum turn off energy versus inductance – LED mode



Note: Values are generated with R_L = 0 Ω.

In case of repetitive pulses, T_{Jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for repetitive curves.

15 Package and PCB thermal data

15.1 QFN (6x6 mm) thermal data

Figure 44. QFN (6x6 mm) PCB footprint

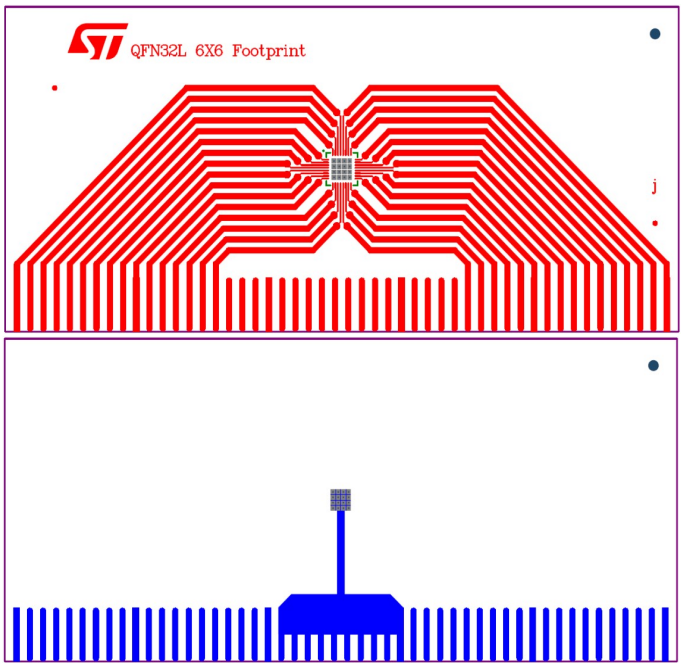


Figure 45. QFN (6x6 mm) PCB 2 cm^2

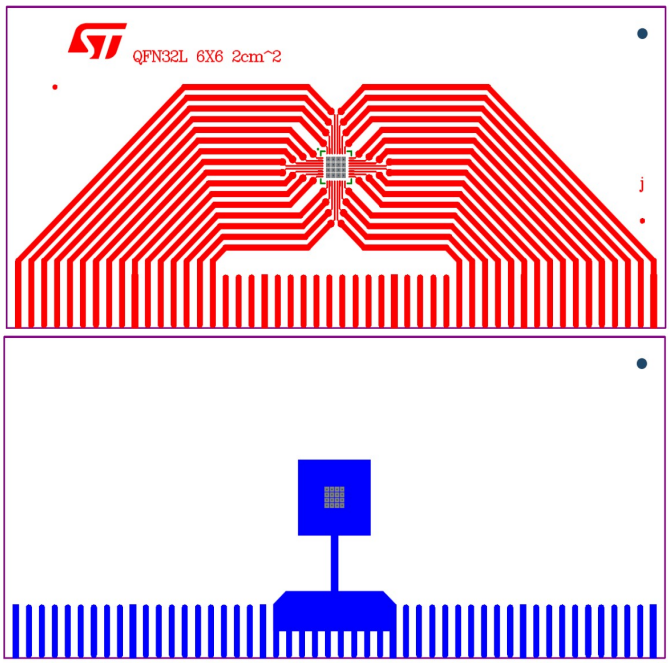


Figure 46. QFN (6x6 mm) PCB 8 cm^2

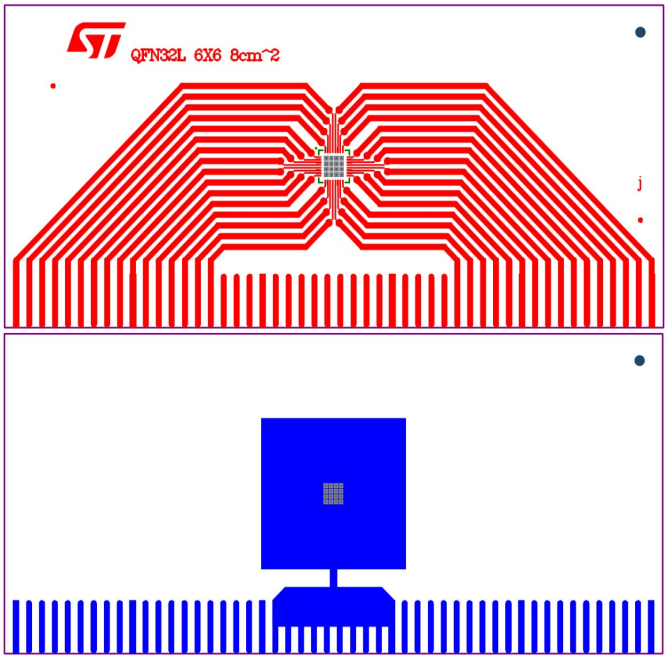


Figure 47. QFN (6x6 mm) PCB 4 layer^2

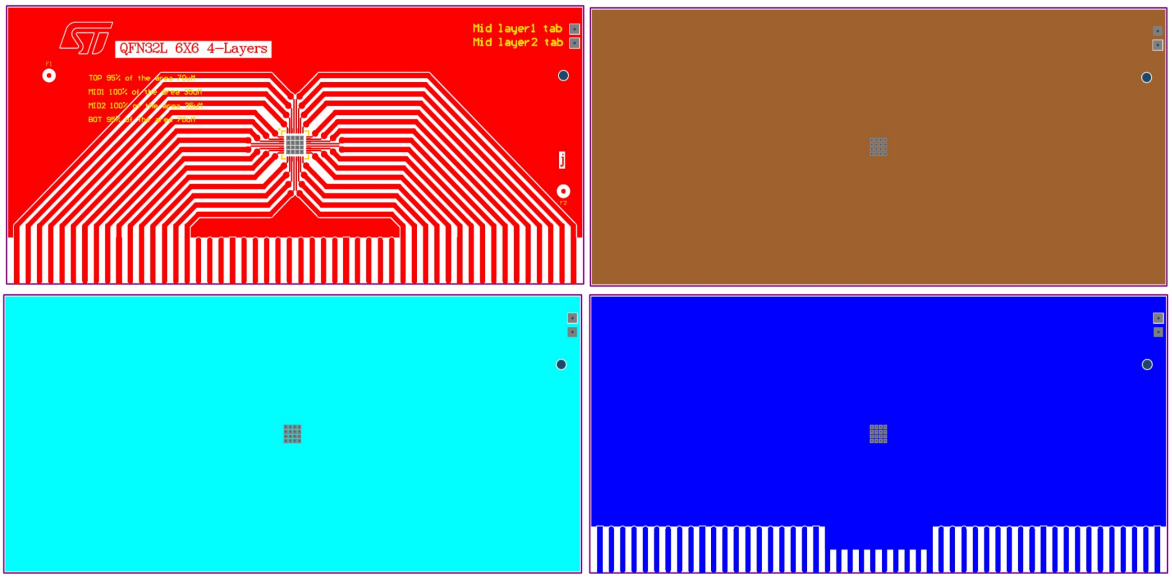
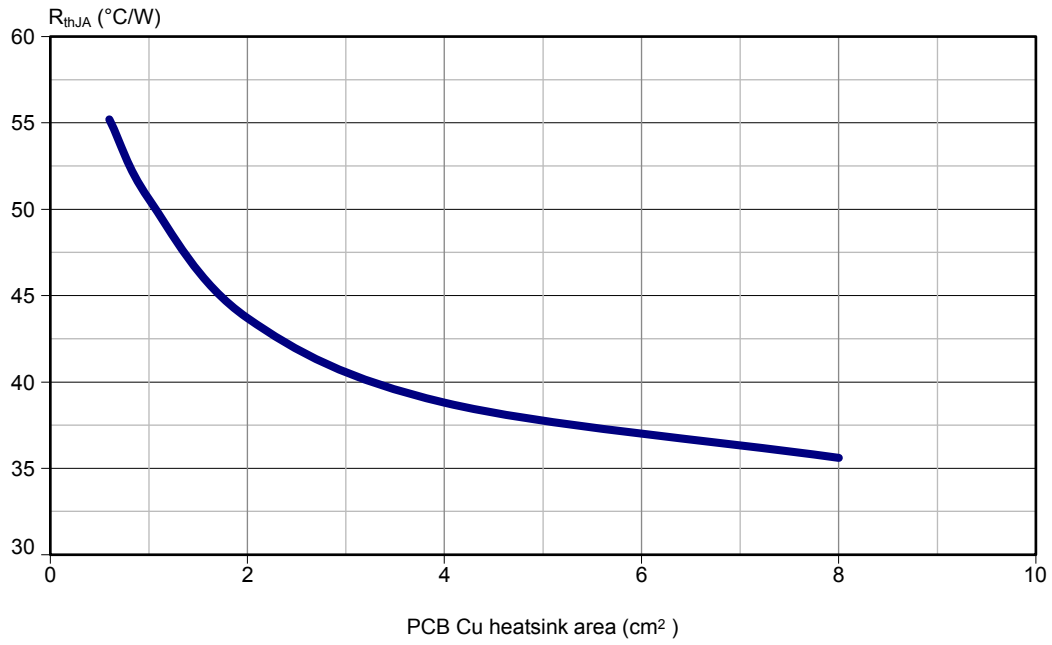


Table 76. PCB properties

Dimension	Value
Board finish thickness	1.6 mm ±10%
Board dimension	129 mm x 60 mm
Board material	FR4
Cu thickness (top and bottom layers)	0.070 mm
Cu thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal vias diameter	0.3 mm ±0.08 mm
Cu thickness on vias	0.025 mm
Footprint dimension (top layer)	6 mm x 6 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

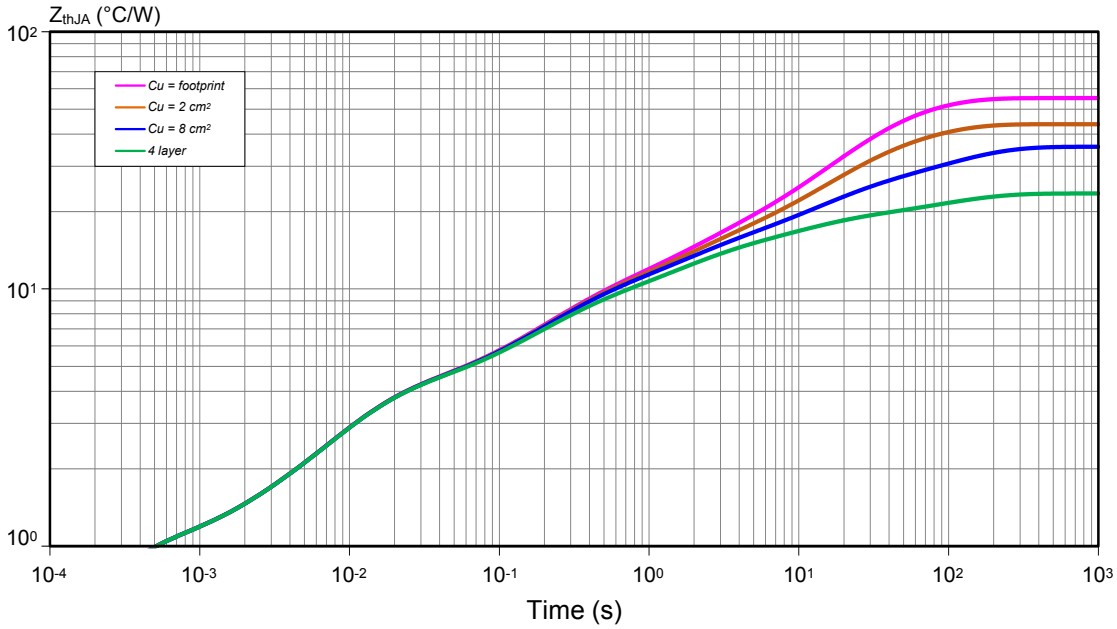
Figure 48. RthJA vs PCB copper area in open box free air conditions



R_{thJA} on 4Layers PCB: 23.5 °C/W

R_{thJB}: 8.6 °C/W

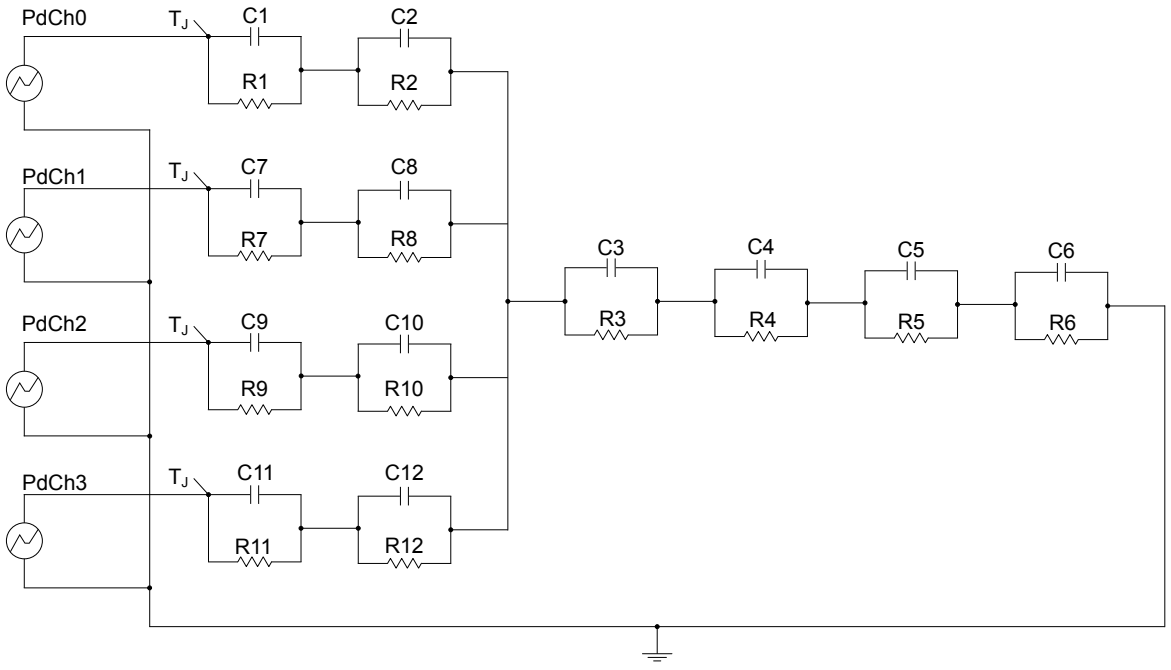
Figure 49. **QFN 6x6 thermal impedance junction ambient**



$Z_{th\delta} = R_{th} \cdot \delta + Z_{tht_p} (1 - \delta)$

where $\delta = t_P/T$

Figure 50. **Thermal fitting model**



GADG050120230849GT

Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 77. **Thermal parameters**

Thermal parameters	Area/island (cm²)			
	FP	2	8	4L
R1 = R7 = R9 = R11 (°C/W)	0.9			
R2 = R8 = R10 = R12 (°C/W)	2.8			
R3 (°C/W)	4.5	4.5	4.5	4
R4 (°C/W)	5	5	5	5
R5 (°C/W)	20	14	9.5	5.3
R6 (°C/W)	22	16.5	13	5.5
C1 = C7 = C9 = C11 (W·s/°C)	0.0002			
C2 = C8 = C10 = C12 (W·s/°C)	0.0035			
C3 (W·s/°C)	0.05			
C4 (W·s/°C)	0.3			
C5 (W·s/°C)	1	1.2	1.4	1.7
C6 (W·s/°C)	2.4	3.5	8	17

16 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

16.1 QFN (6x6 mm) package information

Figure 51. QFN (6x6 mm) package outline

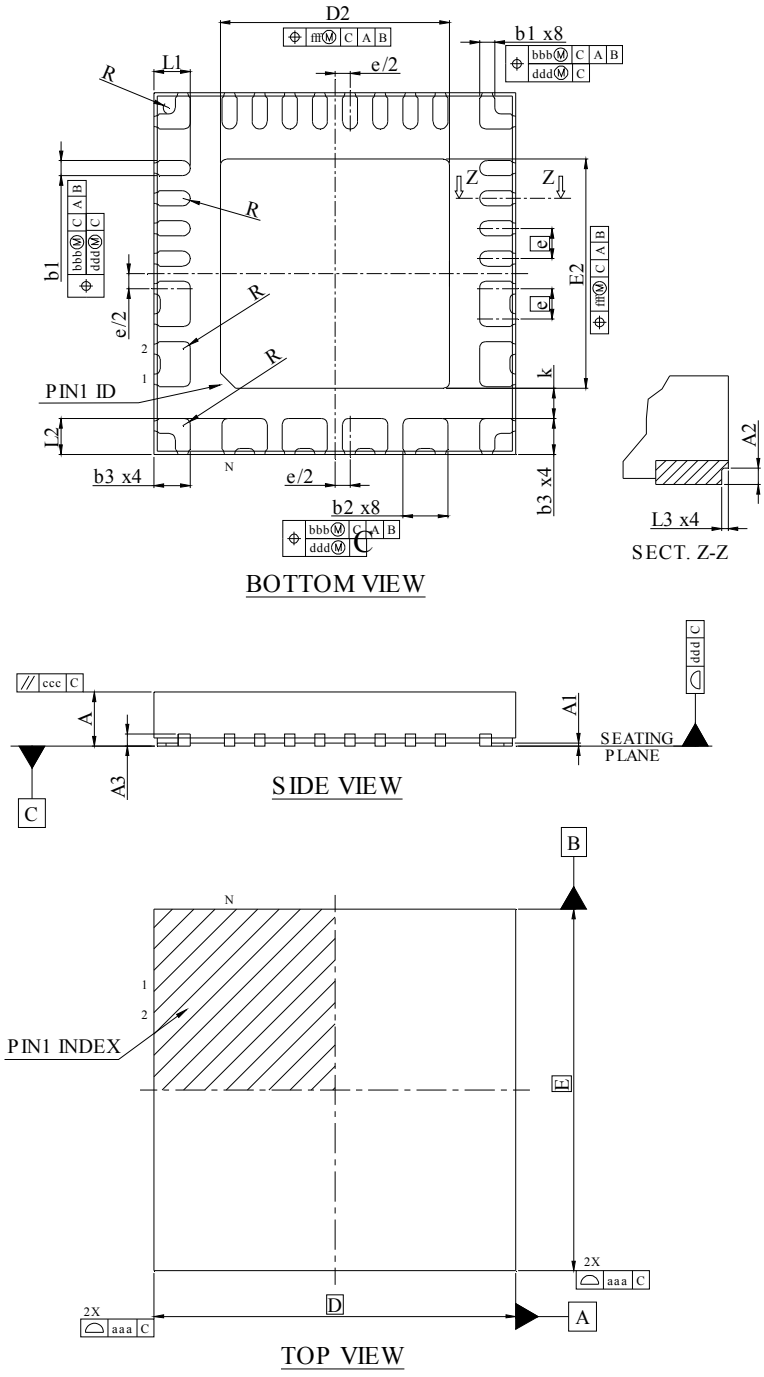


Table 78. QFN (6x6 mm) mechanical data

Dim.	Millimeters		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	-	0.05
A2	0.10	-	-
A3		0.20 REF.	
b1	0.20	0.25	0.30
b2	0.70	0.75	0.80
b3	0.50	0.60	0.70
D		6.00 BSC	
E		6.00 BSC	
e		0.50 BSC	
L1	0.50	0.60	0.70
L2	0.50	0.60	0.70
L3	-	-	0.05
k	0.45	-	-
R	-	-	0.10
N		32+4	

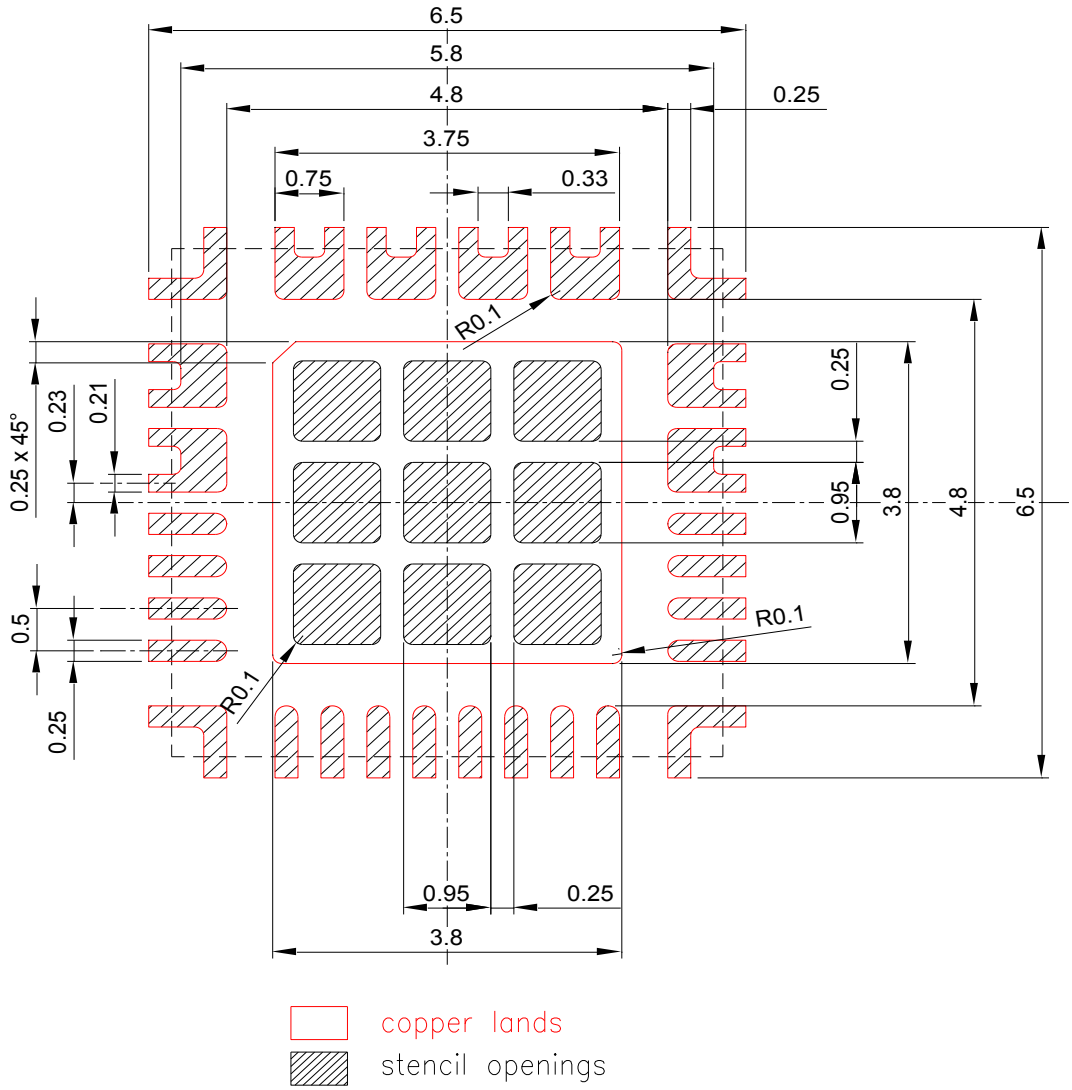
Table 79. QFN (6x6 mm) tolerance of form and position

Dim.	Millimeters
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10
NOTE	1,12
REF	-

Table 80. QFN (6x6 mm) variations

Dim.	Millimeters			OPT.
	Min.	Typ.	Max.	
D2	3.70	3.80	3.90	A
E2	3.70	3.80	3.90	

Figure 52. **QFN (6x6 mm) suggested footprint**



16.2 QFN (6x6 mm) packing information

Figure 53. **QFN (6x6 mm) reel 13"**

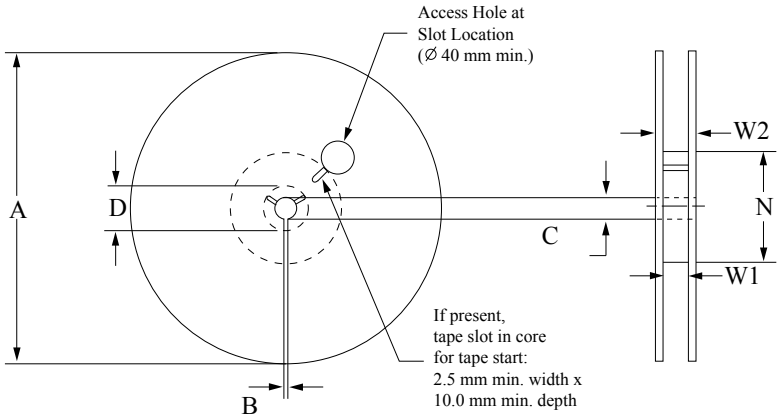


Table 81. QFN (6x6 mm) reel dimensions

Description	Value(1)
Base quantity	3000
Bulk quantity	3000
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	178
W1	146.4
W2	22.4

1. *All dimensions are in mm.*

Figure 54. QFN (6x6 mm) carrier tape

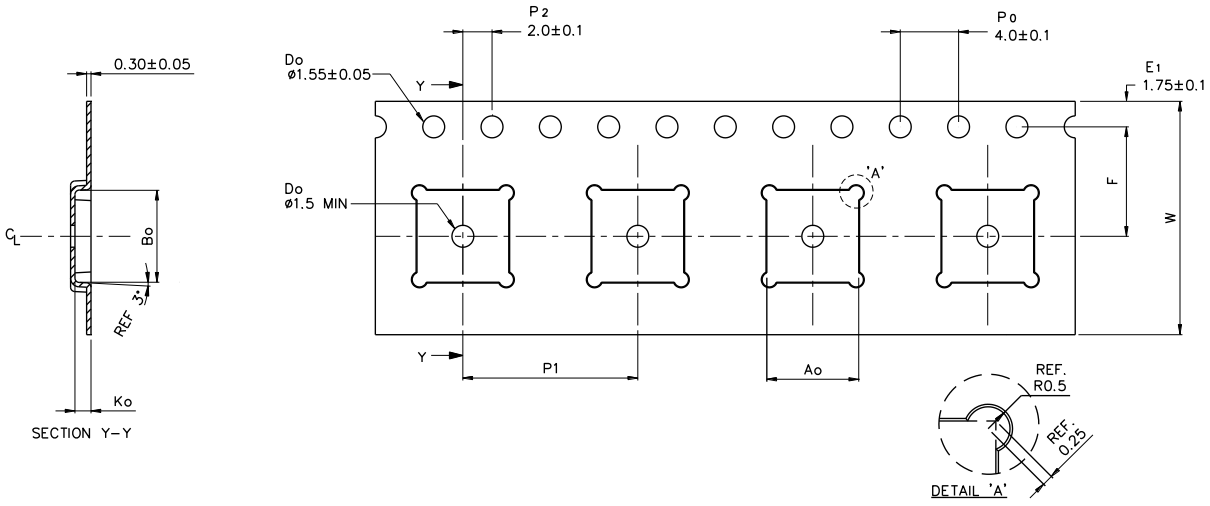


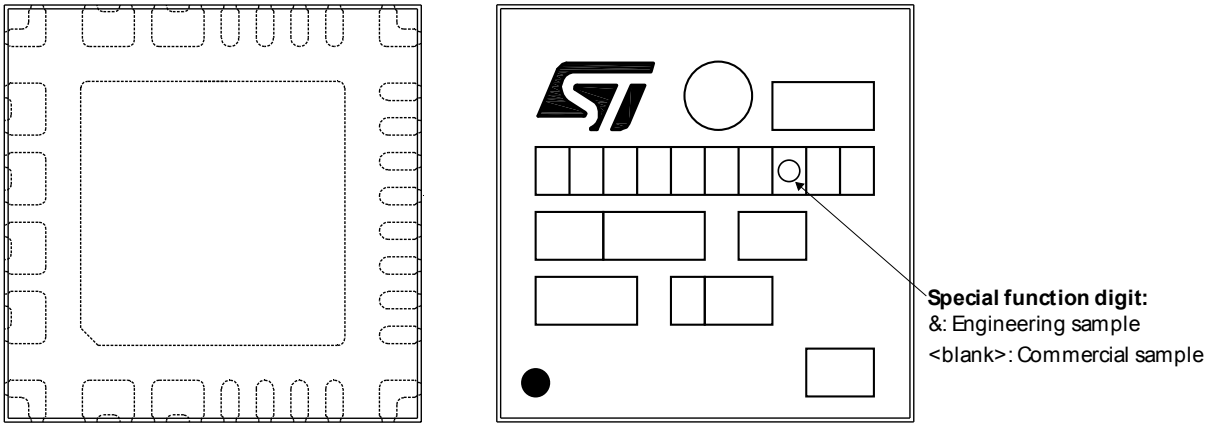
Table 82. QFN (6x6 mm) carrier tape dimensions

Description	Value(1)
A0	6.30 ± 0.1
B0	6.30 ± 0.1
K0	1.10 ± 0.1
F	7.50 ± 0.1
P1	12.00 ± 0.1
W	16.00 ± 0.3

1. *All dimensions are in mm.*

16.3 QFN (6x6 mm) marking information

Figure 55. **QFN (6x6 mm) marking information**



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17 Ordering information

Table 83. **Order code**

Order code	Package	Packing
VNF9Q20SFTR	QFN 6x6 mm	Tape and reel

Revision history

Table 84. **Document revision history**

Date	Revision	Changes
26-Jun-2024	1	Initial release.
19-Nov-2025	2	Updated Features, Description, Section 3.5, Section 4.4, Section 4.4.2, OUTCFGRx, SOCR, CTRL, Section 9, Section 11.3 (general test conditions), Section 11.6 (general test conditions), added Section 17. Updated Figure 39 and added Figure 52. Updated Table 1, Table 49, Table 27, Table 51, Table 53, Table 54, Table 55, Table 59, Table 61, Table 62, Table 63, Table 64, Table 65, Table 66, Table 67, Table 68, Table 69, Table 71, Table 73, and Table 75.
27 Mar 2026	3	Updated Features, Figure 2, Table 1, Section 2.1, Section 3.2, Section 4.4, Section 4.4.3, CHLOFFTCRxx, Section 6.6, Section 7, Table 47, Table 48, Table 57, Table 62, Table 66 and Table 73

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