VNF9D1M2Q

Datasheet

2-channel high-side driver with STi²Fuse protection for automotive power distribution applications

PQFN 7x8.5

Product status link
VNF9D1M2Q

Product summary	
Order code	VNF9D1M2QTR
Package	PQFN 7X8.5
Packing	Tape and reel

Features

Channel	V_{CC}	R_{ON} typ.	I_{PEAK} typ.
0, 1	28 V	1.2 mΩ	145 A

- AEC-Q100 qualified
- General
  - 24-bit ST-SPI for full diagnostic and digital current sense feedback
  - Integrated 10-bit ADC for digital current sense
  - Integrated 10-bit ADC for STi²Fuse digital current sense
  - Advanced limp-home functions for robust fail-safe system
  - Very low standby current for parking mode functionality
  - Control through direct inputs and/or SPI
  - Emergency stop and limp-home pins for advanced safety features
  - Capacitive loads charging mode
  - PQFN 7x8.5 package with wettable flanks
  - Compliant with European directive 2002/95/EC
- Diagnostic functions
  - Digital proportional load current sense
  - Diagnostic of overload and short to GND, harness protection
  - V_{CC} and output voltage digital feedback
  - Case temperature monitoring
  - Overtemperature shutdown, undervoltage, and overvoltage prewarning
- Protection
  - Full programmable wire harness protection (STi²Fuse)
  - Load peak current latch-off
  - Overtemperature shutdown (latch-off)
  - Overvoltage clamp
  - Load dump protected
  - Protection against loss of ground

Description

The VNF9D1M2Q is a device made using STMicroelectronics VIPower technology. It is intended for driving resistive, inductive or capacitive loads directly connected to ground.

The device is protected against voltage transient on V_{CC} pin. Programming, control and diagnostics are implemented via the SPI bus. A digital current sense feedback and an STi²Fuse digital current sense feedback for each channel are provided through two independent integrated 10-bit ADCs per channel. Dedicated trimming bits adjust the ADC reference current. The device is equipped with 2 outputs controllable via SPI and/or with two dedicated direct inputs.

Real time diagnostic is available through the SPI bus (communication error, overtemperature, harness protection, overload protection, V_{CC} and output voltage monitoring, T_C monitoring). Output overcurrent detection protects the device in overload condition. Thermal shutdown is configured as latched off.

The VNF9D1M2Q embeds the ST proprietary I²t functionality, featuring an intelligent circuit breaking aimed at protecting PCB traces, connectors and wire harness from overheating, with no impact on load transients like inrush currents and capacitance charging. This function is set by two parameters, called I_{NOM} and t_{NOM}: there are 3 dedicated bits, per each parameter, to set respectively I_{NOM} (nominal current) and t_{NOM} (nominal timing). The I²t curve parameters can be individually set per each channel. The default values of these two parameters can be programmed twice using dedicated OTPs. The selection of default I²t configuration from OTPs for all channels is defined by the I2TCFGINIT in the ITCNTSR register. Further information about the OTP programming mode is provided in the dedicated user manual UM3275 (OTP programming for STi²Fuse devices).

The device enters a limp-home mode in case of reset of digital memory, watchdog monitoring time-out event or when LH (limp-home) pin is set to high. In limp-home mode each output is controlled by dedicated direct inputs. Emergency pins allow a rapid switch-off of the output channels in case of critical events in normal operation mode bypassing SPI control.

During standby mode, the device is able to support the parking mode functionality. In case the OUTPUT pin is pulled up to battery by an external secondary switch (for instance, the L99SP08 which is delivering the requested current to the load), the device offers a very low current consumption.

For further information refer to the application note AN6025 - Interaction of L99SP08 with single (VNF9SxQ) and dual (VNF9DxQ) hybrid eFuses.

1 Block diagram and pin description

Figure 1. Block diagram

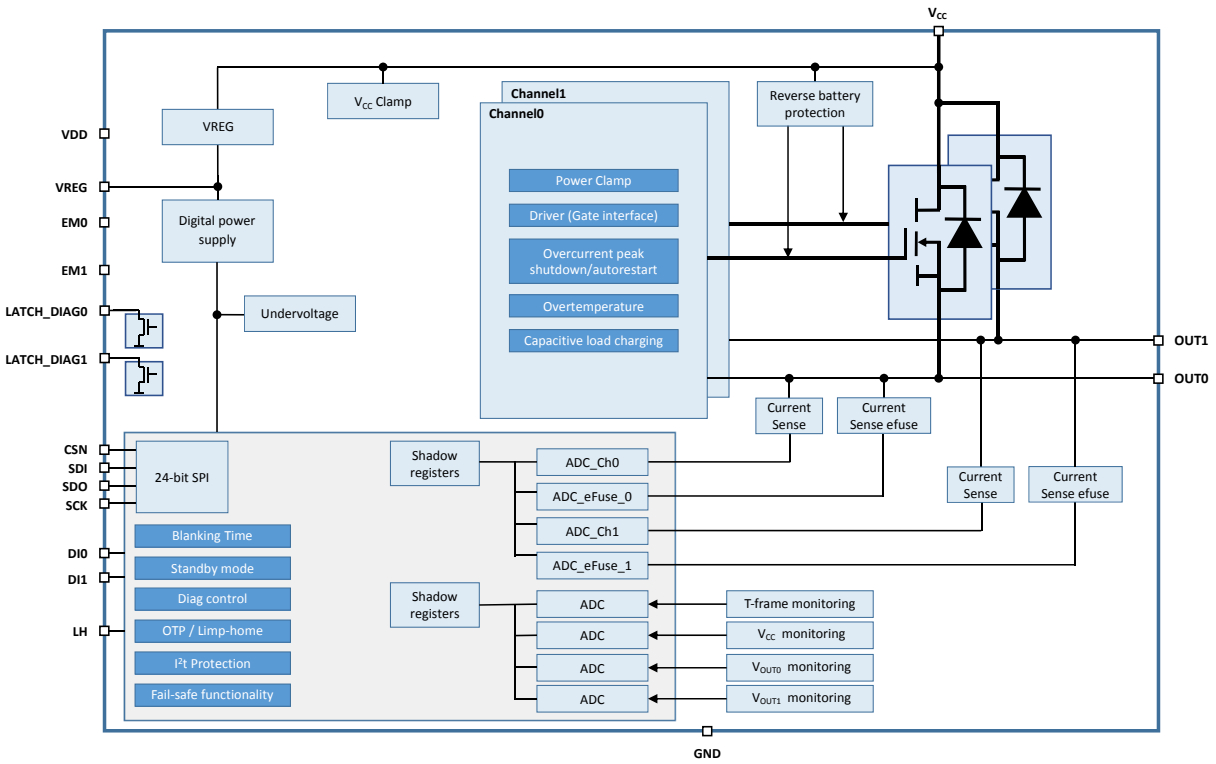

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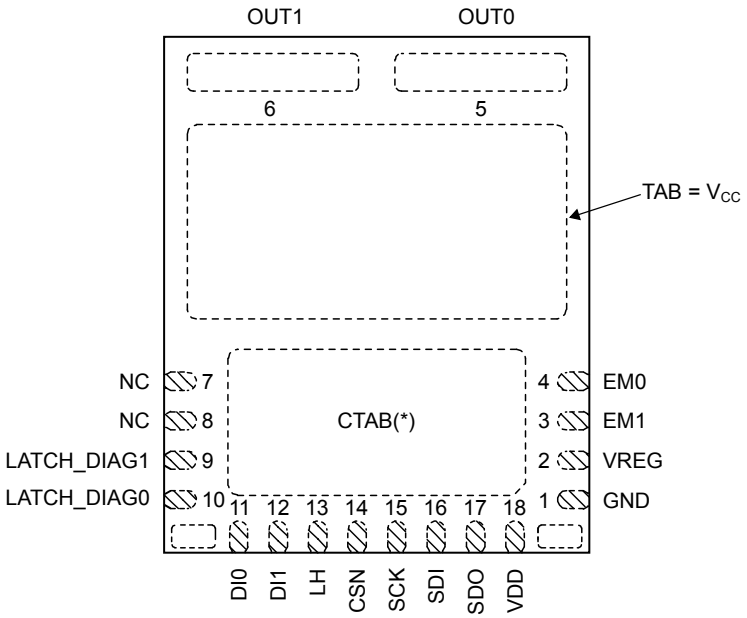
Figure 2. Connection diagram (top-through view)



(*) To be soldered but kept electrically isolated at PCB level.

Table 1. Pin functionality description

Pin #	Name	Function
TAB	V_{CC}	Battery connection: this is the backside TAB and is the direct connection to the drain of the Power MOSFET switches.
1	GND	Ground connection: This pin serves as the ground connection for the logic part of the device.
2	VREG	DC output of internal pre-regulator generated from V_{CC} to supply control circuit. To be connected to a filtering capacitor.
3	EM1	Emergency stop pins; turn off rapidly channel1 during normal operating mode.
4	EM0	Emergency stop pins; turn off rapidly channel0 during normal operating mode.
5	OUT0	Power OUTPUT0 is the direct connection to the source of the Power MOSFET switch Nº 0.
6	OUT1	Power OUTPUT1 is the direct connection to the source of the Power MOSFET switch Nº 1.
7	NC	Not connected pin.
8	NC	Not connected pin.
9	LATCH_DIAG1	Open drain diagnostic pin; active in case of latched fault on channel1. Moreover, it is active for a limited time interval soon after wake up from standby mode.
10	LATCH_DIAG0	Open drain diagnostic pin; active in case of latched fault on channel0. Moreover, it is active for a limited time interval soon after wake up from standby mode.
11	DI0	Direct Input: direct control for OUT0 in limp-home mode. Configurable as OR combination with the relevant SPI OUT0 control bit in normal mode.
12	DI1	Direct Input: direct control for OUT1 in limp-home mode. Configurable as OR combination with the relevant SPI OUT1 control bit in normal mode.
13	LH	Limp-home pin. If set high, the device goes from normal mode to fail-safe mode.
14	CSN	Chip select not (active low): It is the selection pin of the device. It is a CMOS compatible input.
15	SCK	Serial clock: It is a CMOS compatible input.
16	SDI	Serial data input: Transfers data to be written serially into the device on SCK rising edge.
17	SDO	Serial data output: Transfers data serially out of the device on SCK falling edge.
18	VDD	DC supply input for the SPI interface (3.3 V and 5 V compatible).

2 Functional description

2.1 Device interfaces

- SPI: bi-directional interface, accessing RAM/ROM registers (CSN, SCK, SDI, SDO)
- DIx: input pins for outputs control while the device is in fail-safe mode or normal mode
- V_{DD}: 5 V supply or 3.3 V supply. V_{DD} to be connected to microcontroller I/Os supply.
- EMx: emergency stop pins in normal mode operation.
- LATCH_DIAGx: open drain output pins for advanced safety diagnostic.

2.2 Operating modes

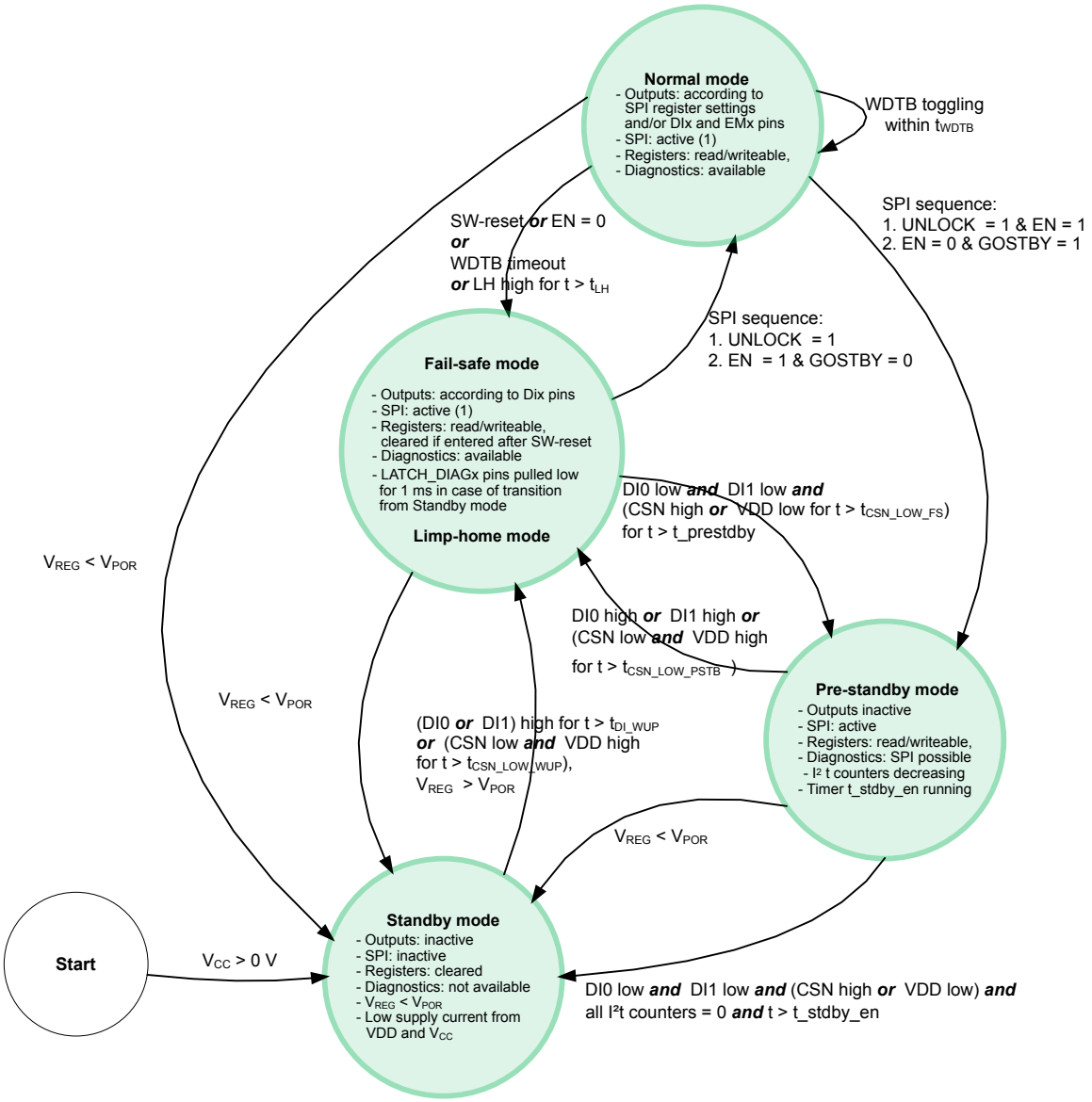
The device can operate in four different modes:

- Standby mode
- Fail-safe mode
- Normal mode
- Pre-standby mode

Table 2. Operating modes

Operating mode	Entering conditions	Leaving conditions	Characteristics
Startup transition (this is not an operating mode)		• V_{CC} > $V_{USD:}$ power on reset	• Outputs: OFF • SPI: inactive • Registers: reset values • Diagnostics: not available
Fail-safe (Limp-home mode)	• From standby mode if (DI0 or DI1) high or (CSN low and V_{DD} high), and V_{REG} > V_{POR} • From pre-standby mode if DI0 high or DI1 high or (CSN low and V_{DD} high) • From normal mode if SW reset or EN = 0 or watchdog timeout or LH high	• If V_{REG} < V_{POR}; the device enters standby mode • If DI0 low and DI1 low and (CSN high or VDD low) for t > t_prestdby, the device enters pre-standby mode • If the following SPI sequence is sent: 1. UNLOCK = 1 2. EN = 1 and GOSTBY = 0 the device enters normal mode	• Outputs: according to DIx • SPI: active • Registers: read/write possible, cleared if entered after SW reset • Diagnostics: available • The RESET is set to 1 if the last state is standby mode or in case the last command is an SW reset; it is reset to 0 at the first SPI access • Protections: available • LATCH_DIAGx pins pulled low for t_{WKUP_FDBCK}
Normal	• Fail-safe: SPI sequence 1. UNLOCK = 1 2. GOSTBY = 0 and EN = 1	• V_{REG} < V_{POR}: standby mode • SPI sequence 1. UNLOCK = 1 and EN = 1 2. GOSTBY = 1 and EN = 0: pre-standby mode • EN = 0: fail-safe mode • Watchdog time out: fail-safe mode • SW reset: fail-safe mode • LH pin is set to high for more than t_{LH}: fail-safe mode	• Outputs: according to SPI register settings and/or DIx and EMx pins • SPI: active • Registers: read/write possible • Diagnostics: available • Regular toggling of WDTB is necessary within timeout period t_{WDTB}
Standby	• Transition phase: V_{CC} > 0 • Fail-safe: V_{REG} < V_{POR} • Normal mode: V_{REG} < V_{POR} • Pre-standby: 1. V_{REG} < V_{POR} 2. DI0 low and DI1 low and (CSN high or VDD low), and all I^2t counters = 0 and t > t_stdby	• DI0 = 1 or DI1 = 1 • CSN low and V_{DD} high • VREG > VPOR	• Outputs: OFF • SPI: inactive • Registers: cleared • Diagnostics: not available • Low supply current from V_{DD} and V_{CC}
Pre-standby	• Fail-safe mode: DI0 low and DI1 low and (CSN high or VDD low) for t > t_prestdby • Normal mode: SPI sequence 1. UNLOCK = 1 and EN = 1 2. GOSTBY = 1 and EN = 0	I^2t counters and t_stdby timer are elapsed DI0 = 0 and DI1 = 0 and (CSN high or V_{DD} low)	• Outputs: OFF • I^2t counters decreasing • SPI: active • Registers: R/W possible • Diagnostics: available • Protections: active

Figure 3. Device state diagram



(1) SPI communication only if VDD is present.

2.2.1 Startup transition phase

This is not an operation mode but a transition step to standby operating mode at startup. In this phase, V_{CC} is applied.

2.2.2 Standby mode

The device is in low consumption state.

The outputs are in OFF state.

The diagnostics is not available.

The SPI communication is not active.

The registers are cleared.

The device enters standby mode under the following conditions:

- From transition phase if V_{CC} is applied
- From fail-safe mode if $V_{REG} < V_{POR}$

- From normal mode if $V_{REG} < V_{POR}$
- From pre-standby mode if:
  - $V_{REG} < V_{POR}$
  - DI0 low and DI1 low (CSN high or V_{DD} low), and all I²t counters = 0 and t_stdby_en is elapsed

The device exits standby mode under the following conditions:

- If DI0 or DI1 are set to high
- If CSN is low and VDD is applied

2.2.3 Fail-safe mode

The outputs are controlled by the direct inputs DIx.

The registers are in the read/write mode and are cleared to their reset value if fail-safe is entered through a software reset.

The RESET is 1 if the last state was standby mode or the last command was a SW reset and it is reset to 0 after the first SPI access (for more information refer to Section 4.3.1: Global status byte description).

The SPI interface is active and the diagnostics is available.

The protections are fully functional.

The device enters fail-safe mode under the following conditions:

- From standby mode if (DI0 OR DI1) high OR (CSN low AND VDD high) AND $V_{REG} > V_{POR}$
- From pre-standby mode if (DI0 OR DI1) high OR (CSN low AND VDD high)
- From normal mode if SW reset or EN = 0 or watchdog timeout or LH high for $t > t_{LH}$

The device exits fail-safe mode under the following conditions:

- If $V_{REG} < V_{POR}$, the device enters standby mode
- If (DI0 AND DI1) low AND (CSN high OR VDD low) for t > t_prestdby, the device enters pre-standby mode
- If the SPI sends the following sequence:
  - UNLOCK = 1
  - EN = 1 and GOSTBY = 0

  the device enters normal mode.

Transition to fail-safe mode from normal mode, using the SPI register

Only one frame is needed: write “CTRL” 0x0000.

Table 3. Frame 1 (write CTRL 0x0000)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	0	0	0	1	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	0	0	0	0	0	0	0	0
DATA2	Not used	Not used	Not used	Not used	LOCKEN1	LOCKEN0	Not used	Parity
	0	0	0	0	0	0	0	0

Transition to fail-safe mode from normal mode by SW-Reset

SPI reset occurs by using the “Read device information” command (applicable only on ROM area) at the reserved ROM address 0x3F. This is equivalent of sending a 0xFF command.

Only one frame is needed: **read “ROM” 0x3F**.

Table 4. Frame 1: read (ROM) 0x3F 0x--

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	1	1	1	1	1	1	1	1
DATA1	x(1)	x	x	x	x	x	x	x
	0	0	0	0	0	0	0	0
DATA2	x	x	x	x	x	x	x	x
	0	0	0	0	0	0	0	0

1. *X: do not care. At least one of these bits must be zero, as 0xFFFF frame is not allowed.*

The entry to the fail-safe mode can occur due to the CSN timeout.

In this specific case, the following procedure must be executed to leave the fail-safe mode:

- Removing the cause of the CSN stuck
- Toggling the CSN pin for a min t_{SHCH} (time to release the SDO line), see parameter in Table 38. Dynamic characteristics
- Sending the SPI frames

If the above procedure is not respected, the first SPI frame will be rejected and the state transition will be failed.

2.2.4 Normal mode

In this mode, all device functions are available. The transition to this mode is only possible from a previous fail-safe mode.

Outputs can be driven by SPI commands, EMx emergency pins and direct inputs DIx (according to DIENCRx bits).

To maintain the device in normal mode, the watchdog toggle bit in register SOCR has to be toggled within the watchdog timeout period t_{WBTB} (see Table 38. Dynamic characteristics).

Diagnostic is available through the SPI bus (digital).

The protections are fully functional. The outputs are set to latch-off mode, except for capacitive charge mode that is always set to auto-restart mode for a time t_ccm_cycle. Latched-off fault diagnostics is delivered to LATCH_DIAGx pin (open drain). Once channels are latched-off, the relevant status register has to be cleared to switch them on again.

The device enters in normal mode under one condition:

- If it is in fail-safe mode and the SPI sends the goto normal mode sequence:
  - In a first communication set bit UNLOCK = 1 – Write “CTRL” 0x4001;
  - In the consecutive communication set bit GOSTBY = 0 and bit EN = 1 – Write “CTRL” 0x0801;

Transition from fail-safe mode to normal mode is performed by two special SPI sequences

- Frame 1: Write “CTRL” 0x4001
- Frame 2: Write “CTRL” 0x0801

Table 5. Frame 1 (Write CTRL 0x4001)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	0	0	0	1	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	0	1	0	0	0	0	0	0
DATA2	Not used	Not used	Not used	Not used	Not used	LOCKEN0	Not used	Parity
	0	0	0	0	0	0	0	1

Table 6. Frame 2 (Write CTRL 0x0801)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	0	0	0	1	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	0	0	0	0	1	0	0	0
DATA2	Not used	Not used	Not used	Not used	Not used	LOCKEN0	Not used	Parity
	0	0	0	0	0	0	0	1

The device exits normal mode under the following conditions:

- If V_{REG} falls below V_{POR}, the device enters standby mode.
- If the SPI sends the goto pre-standby sequence, the device enters pre-standby mode:
  - In a first communication set bit UNLOCK = 1 and bit EN = 1
  - In the consecutive communication set bit GOSTBY = 1 and bit EN = 0

This mechanism avoids entering pre-standby mode unintentionally.

- If the SPI clears the EN bit (EN = 0), the device enters fail-safe mode.
- Watchdog timeout: if WDTB is not toggled within the monitoring timeout period t_{WDTB}, the device enters fail-safe mode.
- If the SPI sends a SW reset command (command byte = 0xFFh), all registers are cleared and the device enters fail-safe mode.
- If LH (limp-home) pin is set to high for t > t_{LH} the device enters fail-safe mode.

2.2.5 Pre-standby mode

Usually, pre-standby mode is an intermediate state towards standby mode.

The outputs are in off state.

The diagnostics is available.

The protections are active.

The SPI communication is active.

The registers are available for R/W.

Once counters elapse (I^2t counters and t_stdby_en), the device switches from pre-standby mode to standby mode if:

- (DI0 AND DI1) low AND (CSN high OR VDD low) AND $V_{REG} < V_{POR}$

The device enters pre-standby mode under the following conditions:

- From fail-safe mode if DI0 low AND DI1 low AND (CSN high OR VDD low) for t > t_prestdby
- From normal mode if the SPI sends the goto pre-standby mode sequence:
  - In a first communication set UNLOCK = 1 and EN = 1
  - In the consecutive communication set GOSTBY = 1 and EN = 0

This mechanism avoids entering pre-standby mode unintentionally.

The device exits pre-standby mode and switches back to fail-safe mode, if I^2t counters are not zero and t_stdby_en is not elapsed, under the following condition:

- (DI0 OR DI1) high OR (CSN low AND VDD high)

The device leaves pre-standby to standby mode, if I^2t counters and t_stdby_en are elapsed and:

- (DI0 AND DI1) low AND (CSN high OR VDD low)

Transition from normal mode to pre-standby mode using SPI: two frames needed.

- Frame 1: write “CTRL”0x4800
- Frame 2: write “CTRL”0x8001

Table 7. Frame 1 (write CTRL 0x4800)–Normal mode to pre-standby mode

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	0	0	0	1	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	0	1	0	0	1	0	0	0
DATA2	Not used	Not used	Not used	Not used	Not used	LOCKEN0	Not used	Parity
	0	0	0	0	0	0	0	0

Table 8. Frame 2 (write CTRL 0x8001)–Normal mode to pre-standby mode

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD	OC1	OC0	Address					
	0	0	0	0	0	0	1	0
DATA1	GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	Not used	Not used	Not used
	1	0	0	0	0	0	0	0
DATA2	Not used	Not used	Not used	Not used	Not used	LOCKEN0	Not used	Parity
	0	0	0	0	0	0	0	1

2.3 Capacitive charging mode

It is not a device state but a channel state.

When the channel is set to this mode, a specific procedure, allowing auto-restart after I_{PEAK} detection, allows to charge a capacitive load within the maximum required time (t_ccm_cycle), see Figure 4. Channel state diagram.

The device enters this specific channel mode under the following conditions:

- In normal mode, if a specific SPI frame is sent: set CAPCRx bit localized in SOCR register (position 4 and 5) to high value, the bit is automatically reset and acts as a trigger
- In fail-safe mode, after POR, if OTP bit CAPFSSRx is set
- In fail-safe mode if a specific toggling sequence to DIx pins is applied: at least 5 rising edges on DIx pins within t < t_di_mon

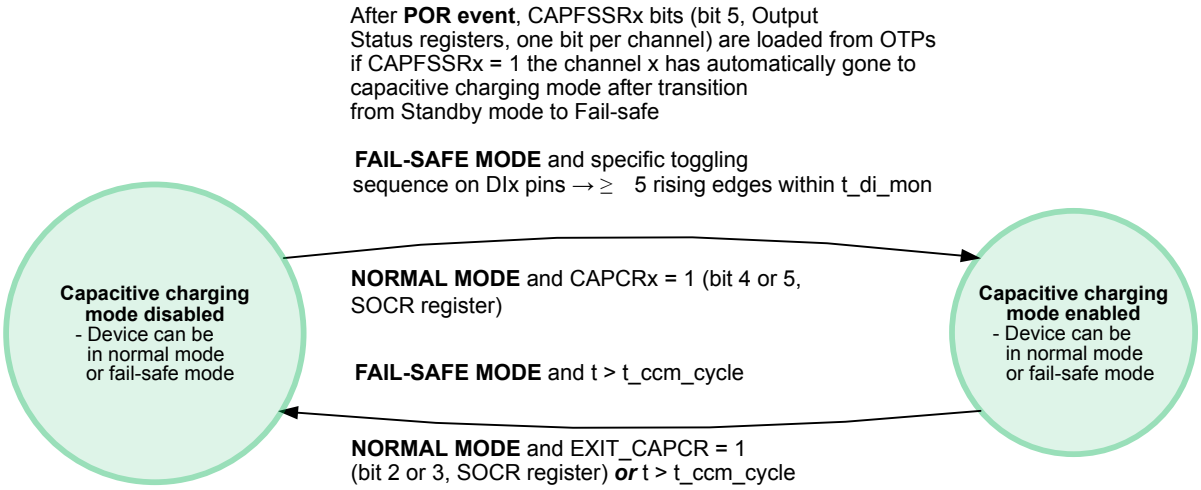
The device exits this specific channel mode under the following conditions:

- In normal mode, if a specific SPI frame is sent: set EXIT_CAPCRx bit in SOCR register (position 2 and 3) to 1
- In normal mode, if t_ccm_cycle is elapsed
- In fail-safe mode, if t_ccm_cycle is elapsed

The capacitive charging mode charges capacitors with a burst of low frequency I_{PEAK} pulses, provided that the total impedance is low enough to reach I_{PEAK} when charging the capacitor. If I_{PEAK} is not reached, the capacitor is charged with a single continuous charging pulse. In this specific channel operating mode, the device can distinguish a capacitor load from a short circuit.

When a channel is set in capacitive charging mode and the output stage is turned on, an autorestart procedure is started first in a low frequency mode. If the ESR of the connected capacitor and the total output line impedance is low enough to let the channel reach its I_{PEAK} value, the channel will turn off after t_filter_ipeak filter time elapsed and remain off for a t_{LF} period. At the end of the t_{FL} period the device samples the output voltage of the channel in capacitive charging mode. As long as the output voltage remains below VOUT_THR and the number of low frequency charging cycles remains below the MAX_COUNTER_LF threshold, the device remains in low frequency mode and will turn on its output again. The channel exits from the low frequency charging mode, as soon as VOUT_THR threshold is exceeded or MAX_COUNTER_LF is reached. In the latter case, the channel will latch off for short circuit detection and the status flag IPEAKLSRx in OUTSRx register – Channel Feedback Status bit and in the Global Status Byte will be set. Otherwise, the channel enters a high frequency charging mode (with a period equal to t_{HF}) and continues to charge the capacitor with a burst of I_{PEAK} pulses, provided that the line impedance is still low enough to let the channel reach I_{PEAK}. After each I_{PEAK} pulse, the channel will turn off after t_filter_ipeak filter time elapsed and remains off for a t_{HF} period. The process will be continued till the threshold MAX_COUNTER_LF is reached , t_ccm_cycle is elapsed or CCM is aborted through SPI command.

Figure 4. Channel state diagram



3 Protections

3.1 Thermal case temperature monitoring and pre-warning

Case-temperature is constantly monitored via a 10-bit ADC converter and data is available through T_{CASE} register (0x27h).

Case-temperature diagnostic is available through the global status byte. Temperature threshold is programmable via the control register (4 levels). T_{CASE} is cleared automatically when the case-temperature drops below the case-temperature threshold.

3.2 Junction overtemperature (OT)

If the junction temperature of one channel rises above the shutdown temperature T_{TSD}, an overtemperature event (OT) is detected.

In normal mode, the channel is switched OFF and the corresponding bit in the OUTSRx register-channel feedback status register (OTSRx) is set. Consequently, the thermal shutdown bit (bit 4) in the global status byte and the global error flag are set. LATCH_DIAGx open drain pin is set low if OTMASK = 0.

The output remains switched OFF until the junction temperature falls below T_R and the MCU resets the latch-off event by clearing the OTSRx bit in the channel status register. The bit 4 in the global status byte register is cleared and the LATCH_DIAGx pin is released.

In fail-safe mode, the channel is switched OFF and the corresponding bit in the OUTSRx register-channel feedback status bit (OTSRx) is set. Consequently, the thermal shutdown bit (bit 4) in the global status byte and the global error flag are set. LATCH_DIAGx open drain pin is set low.

The output remains switched OFF until the junction temperature falls below T_R and the latch is reset either by toggling the corresponding DIx pin or by clearing OTSRx bit by the MCU. The action clears the OTSRx bit in the channel status register and the corresponding bit 4 in the global status byte. LATCH_DIAGx pin is released.

3.3 Overcurrent protection (I_{PEAK})

In case of short circuit, the channel is protected by switching OFF if the current rises above the overcurrent threshold (I_{PEAK}) for a time longer than t_filter_ipeak. In addition, another filter (analog) is applied only after turn on (8 µs typ.).

I_{PEAK} protection is configured to operate in latched OFF mode.

In normal mode, once a fault is detected, the corresponding channel is turned OFF, both fault bits (IPEAKLSRx and ITLOFFSRx) in the channel status register (OUTSRx) are set, bits 2 and 3 in the global status byte are set, and diagnostic is delivered (if IPEAKMASK = 0 and I2TMASK = 0) to the LATCH_DIAGx pin for safety purposes. Fault can be reset by clearing the fault bits, IPEAKLSRx and ITLOFFSRx; bits 2 and 3 in the global status byte are cleared and the LATCH_DIAGx pin is released.

In fail-safe mode, once a fault is detected, the corresponding channel is turned OFF, both fault bits (IPEAKLSRx and ITLOFFSRx) in the channel status register (OUTSRx) are set, bits 2 and 3 in the global status byte are set high, and diagnostic is delivered to LATCH_DIAGx pin for safety purposes. Fault can be reset either by toggling the corresponding DIx pin or by clearing fault bits (IPEAKLSRx). Fault bit (IPEAKLSRx and ITLOFFSRx) are cleared, bits 2 and 3 in the global status byte are cleared and LATCH_DIAGx pin is released.

3.4 Electronic harness protection (STi²Fuse)

The electronic wire harness protection, I²t protection, is active in all operating modes, except in standby mode when the device is in lowest quiescent current consumption mode and all analog and digital functions are in idle mode and output stages are off. In all conditions, the wire harness protection works fully autonomous and in particular does not require any MCU control or supervision. A specific digital I²t current sense register ADCI2tSRx allows to readback the value of the current monitored by the I²t protection block at any time during on-state of the channel. In the ITCNTSR register, the current value of the integrated I²t budget is reported (ITCNTx bits) and allows the application to monitor how much of the available I²t budget is actually consumed.

The I²t protection is based on a continuous RMS output current calculation with a dedicated current sense block for each channel and linearity guaranteed up to I_{PEAK} value. Current sense for I²t calculation is sampled for each channel every t_I²t_SAMPLE. The shape of the actual I²t protection curve is a staircase curve, which is determined by two configurable parameters, I_{NOM} and t_{NOM}. Both parameters are accessible through SPI, read and writeable. Default values of I_{NOM} and t_{NOM} are stored in a user-accessible area of the OTP (one time programmable memory) with a dual programming option. The user can select any combination of the I_{NOM} and t_{NOM} values reported in the below table.

Table 9. Typical values of configurable I_{NOM}

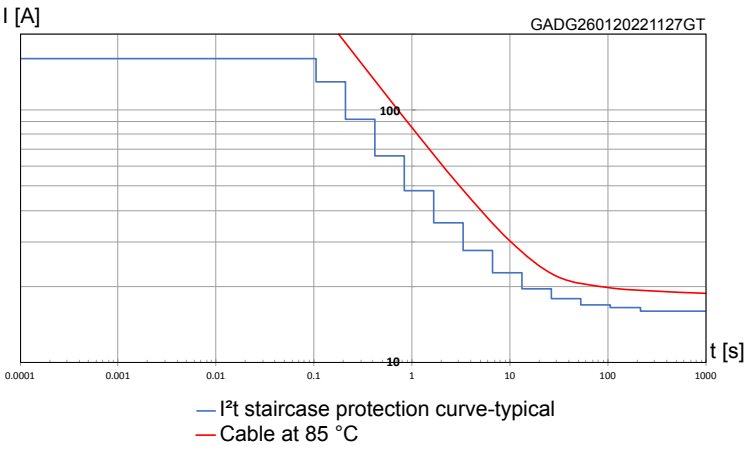
I_{NOM} [A]	INOM2	INOM1	INOM0
10 (default)	0	0	0
11	0	0	1
15	0	1	0
17.5	0	1	1
20	1	0	0
26	1	0	1
28.5	1	1	0
33.5	1	1	1

Table 10. Typical values of configurable t_{NOM}

t_{NOM} [s]	TNOM2	TNOM1	TNOM0
300 (default)	0	0	0
257	0	0	1
214	0	1	0
172	0	1	1
129	1	0	0
86	1	0	1
44	1	1	0
1	1	1	1

The value of I_{NOM} represents the level of steady state current, which can be accepted for infinite time in the system consisting of IC, routing, connectors, wiring, and load. The value of t_{NOM} specifies the speed how fast the staircase curve reaches I_{NOM} value. The following Figure 5 depicts the I²t staircase protection curve with a configuration of I_{NOM} = 15 A and t_{NOM} = 214 s and for comparison the I-t isothermic curve of a wire with 1 mm² cross-section at T_A = 85 °C heating up to 150 °C. As it can be seen, the I²t staircase protection curve is always left and below the wire isothermic curve, which means the I²t protection algorithm protects the wire from carrying an RMS current, which would lead to a higher temperature increase than the one of the isothermic curve.

Figure 5. I²t staircase protection curve



with I_{NOM} = 15 A and t_{NOM} = 214 s vs a 1 mm² wire isothermic curve

The I²t protection curve can be moved in y-direction by changing the I_{NOM} value and in x-direction changing the t_{NOM} value. The following Figure 6(1) and Figure 7(1) represent the total range of I²t the device can cover, ranging from I_{NOM_min} = 10 A with t_{NOM_min} = 1 s up to I_{NOM_max} = 33.5 A with t_{NOM_max} = 300 s.

Figure 6. Lowest I_{NOM} and t_{NOM} configuration setting

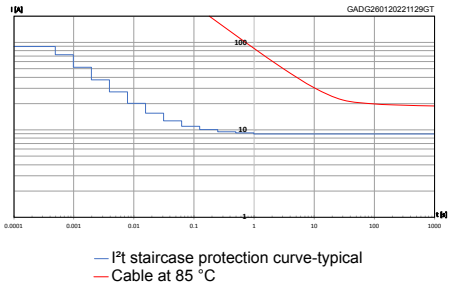
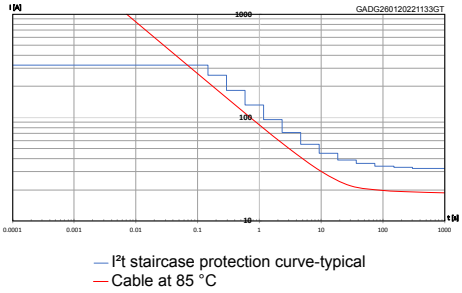


Figure 7. Highest I_{NOM} and t_{NOM} configuration setting



1. *To be intended as example of the protection behavior.*

The I²t protection curve consists of 13 steps, each of them corresponding to a specific current threshold. Whenever the load current exceeds a threshold, a counter is counting up. If for instance, looking at the example of Figure 5 the current would exceed the value of I_{NOM} = 15 A, but stay below the current threshold of the next step, which is set at 1.03*I_{NOM} about, the counter would reach its threshold value after t_{NOM} = 214 s, the harness protection is triggered and the output channel is automatically latched off. In normal mode, the ITLOFFSRx bit is set high and bit 3 in the global status byte is set. Diagnostic is also available through LATCH_DIAGx pin (I2TMASK = 0 via SPI programming). The fault can be unlatched by resetting the fault status bit, ITLOFFSRx, in the channel status register (OUTSRx). Bit 3 in the global status byte is cleared and LATCH_DIAGx pin is released after the time TF_UNLATCH.

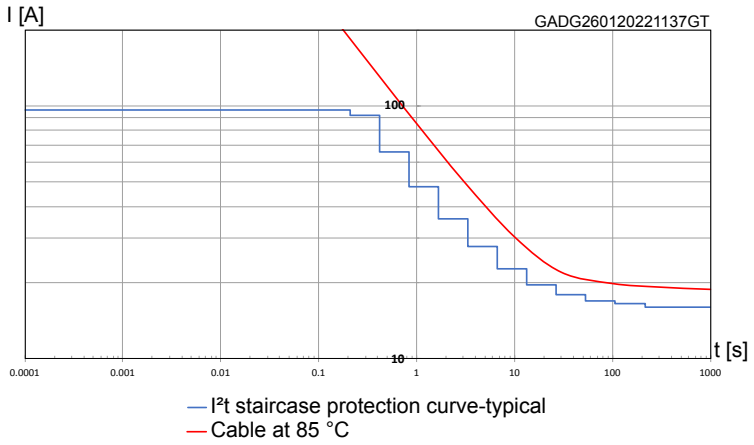
In fail-safe mode, once the harness protection is triggered the bit 3 in the global status byte is set. Diagnostic is available through LATCH_DIAGx pin (pulled down). The fault can be unlatched by toggling the corresponding DIx pin, and LATCH_DIAGx pin is released after the time TF_UNLATCH_DIx_TOGGLE. The ITLOFFSRx bit and bit 3 in the global status byte will remain set and can be clear only via SPI.

The speed of the counter is increased every time the load current reaches the next staircase current threshold of the I²t curve. Every time the load current drops below the I_{NOM} threshold the counter is decreasing. The speed of the down-counting depends on how far the load current is below the I_{NOM}. This algorithm perfectly emulates a continuous RMS–root mean square–current integration, which in fact is the proper indicator to measure the losses in the wire by the Joule effect, causing the temperature rise in the wire. The last (13^{th}) step of the I²t protection staircase curve is equal to $10*I_{NOM}$. Whenever the load current exceeds the 13^{th} threshold, the output channel is latched off immediately within $t_{doff} + t_f$, protecting the integrity of the boardnet power supply.

In case the application requires a high I_{NOM}, but at the same time a fast protection against high-transient currents is required, the highest value of the I²t staircase protection curve can be selected between $10*I_{NOM}$ and $6*I_{NOM}$. The default value can be configured in the OTP memory map through the INOMx_6X_10X bit. In normal mode, the configuration can be changed through SPI by writing to INOMx_6X_10X bit in the I²t configuration control register.

The Figure 8 shows the shape of the I²t staircase protection curve with configuration values as in the Figure 5, but with the highest threshold reduced to $6*I_{NOM}$.

Figure 8. I²t staircase protection curve



with I_{NOM} = 15 A and t_{NOM} = 214 s vs a 1 mm² wire isothermic curve with maximum threshold reduced to $6*I_{NOM}$

In case of short battery glitches an external capacitor (100 nF) connected to VREG pin supplying digital part prevents logic reset and fuse counter reset. I²t protection continues to protect efficiently the harness in these conditions.

4 SPI functional description

4.1 SPI communication

The SPI communication is based on a standard ST-SPI 24-bit interface, using CSN, SDI, SDO and SCK signal lines.

Input data are shifted into SDI, MSB first while output data are shifted out on SDO, MSB first.

4.1.1 Signal description

During all operations, V_{DD} must be held stable and within the specified valid range: V_{DD} min. to V_{DD} max.

Table 11. SPI signal description

Name	Function
Serial clock SCK	This input signal provides the timing of the serial interface. Data present at serial data input (SDI) are latched on the rising edge of serial clock (SCK). Data on serial data output (SDO) change after the falling edge of serial clock (SCK).
Serial data input SDI	This input signal is used to transfer data serially into the device. It receives data to be written. Values are sampled on the rising edge of serial clock (SCK).
Serial data output SDO	This output signal is used to transfer data serially out of the device. Data are shifted out on the falling edge of serial clock (SCK).
Chip select CSN	When this input signal is high, the device is deselected and serial data output (SDO) is high impedance. Driving this input low enables the communication. The communication must start on a low level of serial clock (SCK). Data are accepted only if exactly 24 bits have been shifted in. **Note:** as per the ST_SPI standard, in case of failing communication: • CSN stuck at high: – If the device is in normal mode, a WDTB timeout will force the device into fail-safe mode. The serial data output (SDO) will stay in high impedance (High Z). Any valid communication arrived after this event will be accepted by the device. • CSN stuck at low: – in this case and whatever the mode of the device, a CSN timeout protection will be activated and force the device to release the SPI bus. Then the serial data output (SDO) will go into high impedance (High Z) A reset of the CSN timeout (see T_{SHCH} in the Table 3) is activated with a transition low to high on CSN pin (or with a Power-on Reset or Software reset). With this reset, the serial data output (SDO) will be released and any valid communication will be accepted by the device. Without this reset, next communication will not be taken into account by the device.

4.1.2 Connecting to the SPI bus

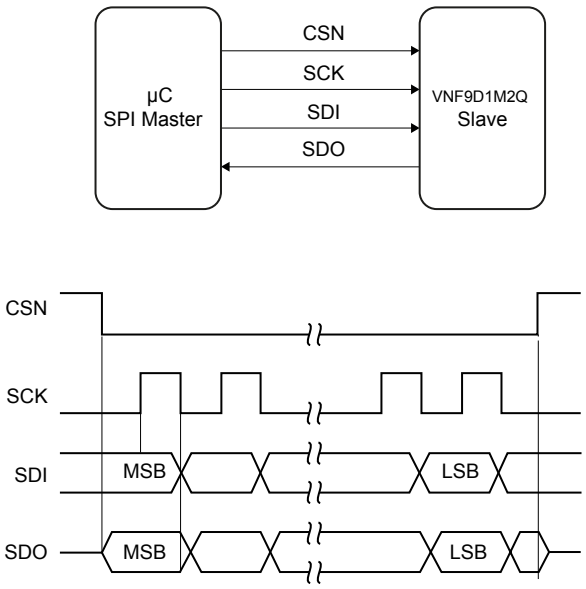
A schematic view of the architecture between the bus and devices can be seen in Figure 10.

All input data bytes are shifted into the device, MSB first. The serial data input (SDI) is sampled on the first rising edge of the serial clock (SCK) after chip select (CSN) goes low. All output data bytes are shifted out of the device on the falling edge of SCK, MSB first on the first falling edge of the chip select (CSN).

4.1.3 SPI mode

Supported SPI mode during a communication phase can be seen in the following figure:

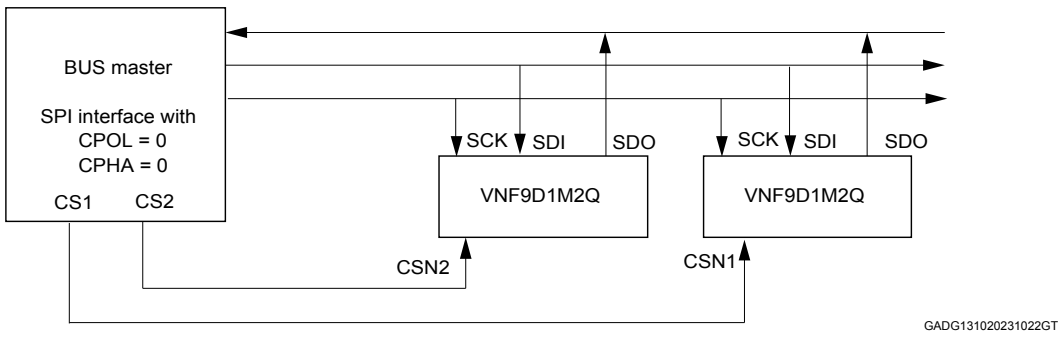
Figure 9. Supported SPI mode



This device can be driven by a micro controller with its SPI peripheral running in the following mode:

- CPOL = 0, CPHA = 0

Figure 10. Bus master and two devices in a normal configuration



4.2 SPI protocol

4.2.1 SDI, SDO format

SDI format during each communication frame starts with a command byte. It begins with two bits of operating code (OC0, OC1) which specify the type of operation (read, write, read and clear status, read device information) and it is followed by a 6-bit address (A0:A5). The command byte is followed by two input data bytes (D15:D8) and (D7:D0).

Table 12. Command byte

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
OC1	OC0	A5	A4	A3	A2	A1	A0

Table 13. Input data byte 1

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 14. Input data byte 2

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
D7	D6	D5	D4	D3	D2	D1	D0(1)

1. *D0 is the parity bit.*

SDO format during each communication frame starts with a specific byte called global status byte (see Table 15 for more details of bit0-bit7). This byte is followed by two output data bytes (D15:D8) and (D7:D0).

Table 15. Global status byte

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0

Table 16. Output data byte 1

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 17. Output data byte 2

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
D7	D6	D5	D4	D3	D2	D1	D0

4.2.2 Operating code definition

The SPI interface features four different addressing modes which are listed in Table 18. Operating codes.

Table 18. Operating codes

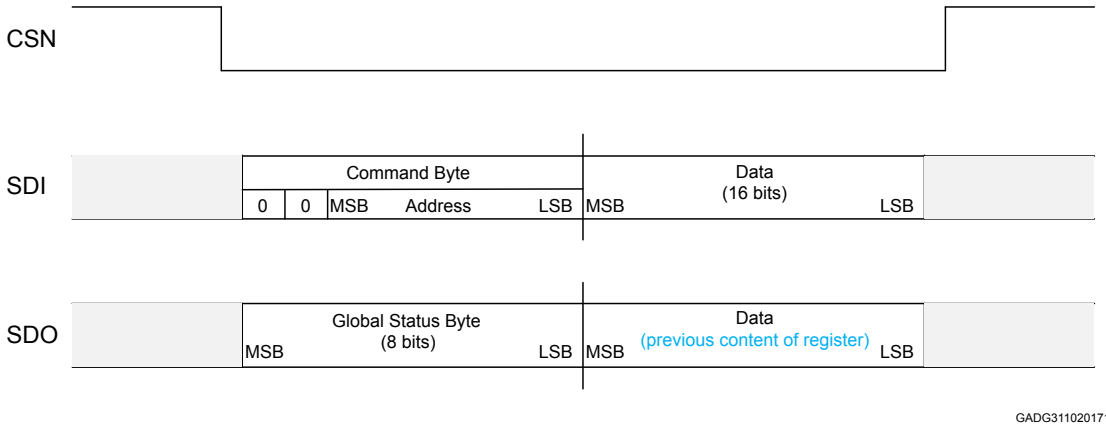
OC1	OC0	Meaning
0	0	Write operation
0	1	Read operation
1	0	Read and clear status operation
1	1	Read device information

Write mode

The write mode of the device allows to write the content of the input data byte into the addressed register (see list of registers in Table 23. RAM memory map). Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

During the same sequence the outgoing data are shifted out MSB first on the falling edge of the CSN pin and the subsequent bits on the falling edge of the serial clock (SCK). The first byte corresponds to the global status byte and the second to the previous content of the addressed register.

Figure 11. SPI write operation



Read mode

The read mode of the device allows to read and to check the state of any register.

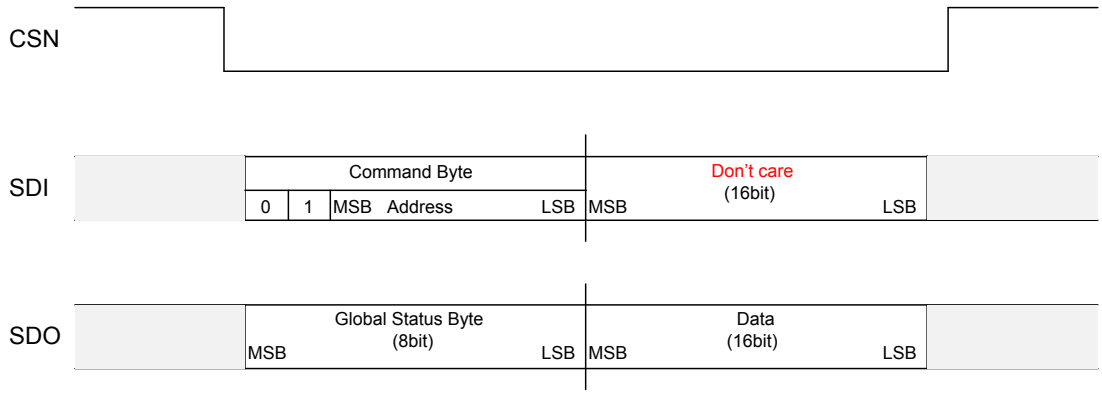
Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

The command byte allows to determine which register content is read, whilst the other two data bytes are "don't care".

In case of a read mode on an unused address, the global status/error byte on the SDO pin is followed by 0x0000 word.

In order to avoid inconsistency between the global status byte and the Status register, the Status register contents are frozen during the SPI communication.

Figure 12. **SPI read operation**



GADG311020171215MT

Read and clear status command

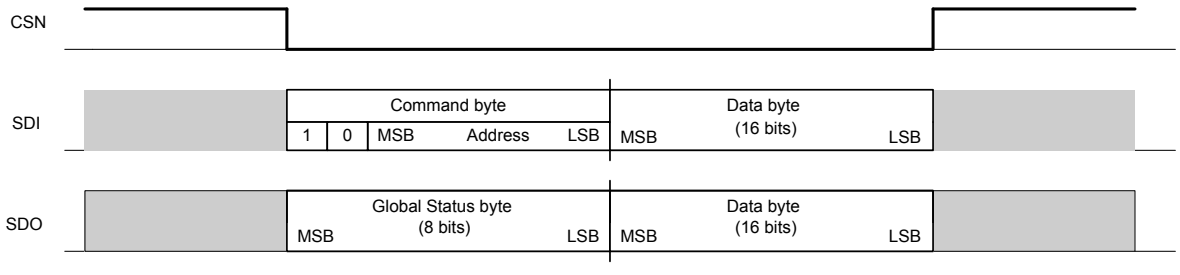
The read and clear status operation is used to clear the content of the addressed status register (see Table 23. RAM memory map). A read and clear status operation with address 0x3Fh clears all Status registers simultaneously.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which register content is read and the payload bits set to 1 into the data byte determine the bits into the register which have to be cleared.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the global status byte and the second to the content of the addressed register.

In order to avoid inconsistency between the global status byte and the Status register, the Status register contents are frozen during SPI communication.

Figure 13. **SPI read and clear operation**



GADG1010171505PS

Read device information

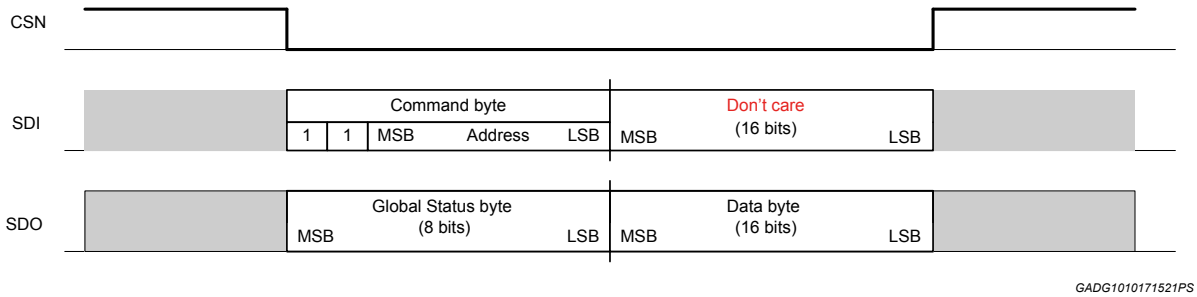
Specific information can be read but not modified during this mode. Accessible data can be seen in Section 4.3.3: ROM.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which information is read whilst the other two data bytes are "don't care".

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the global status byte and the second to the content of the addressed register and the third byte is 0x00.

Note: ROM is based on the 8-bit registers, then even if 16 bits are returned, only the second byte contains the addressed ROM register.

Figure 14. **SPI read device information**



4.2.3 Special commands

0xFF – SW-Reset: set all control registers to default

An OpCode ‘11’ (read device information) addressed at ‘111111’ forces a software reset of the device, second and third bytes are "don't care" provided that at least one bit is zero.

Note: An OpCode '11' at address '111111' with data field equal to '1111111111111111' on the SPI frame is recognized as a frame error and the SPIE bit of GSB is set.

Table 19. **0xFF: SW_Reset**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
1	1	1	1	1	1	1	1
DATA1	X(1)	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

1. *X: do not care.*

0xBF - clear all status registers (RAM access)

When an OpCode ‘10’ (read and clear operation) at address b’111111 is performed.

Table 20. **Clear all status registers (RAM access)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
1	0	1	1	1	1	1	1
DATA1	X(1)	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

1. *X: do not care.*

Note: Reset value = the value of the register after a power on.
Default value = the default value of the register. Currently this is equivalent to the reset value.
Cleared register = explicitly read and clear of the register, if it is not write protected.

4.3 Register map

The device contains a set of RAM and ROM registers. The RAM registers are used for device configuration and device status while ROM registers are used for device identification. Since ST-SPI is used, the global status byte defines the device status, containing fault information.

4.3.1 Global status byte description

The data shifted out on SDO during each communication starts with a specific byte called global status byte. This one is used to inform the microcontroller about global faults, which can happen at channel-side level (that is like thermal shutdown, OLOFF...) or on the SPI interface (like watchdog monitoring timeout event, communication error,...). This specific register has the following format:

Table 21. Global status byte (GSB)

MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	LSB
GSBN	RSTB	SPIE	TSD	ITLOFF	I_{PEAK_DETECT}	Bit1(1)	FS

1. *Bit1 in GSB is defined as T_{CASE} OR V_{CC_UV} OR V_{CC_OV}.*

Table 22. Global status byte description

Bit	Name	Reset	Content
7	Global status bit not	0	The GSBN is a logically NOR combination of bit0 to bit6. This bit can also be used as global status flag without starting a complete communication frame as it is present directly after pulling CSN low.
6	Reset bit	1	The RSTB indicates a device reset. In case this bit is set, all internal control registers are set to default and kept in that state until the bit is cleared. The reset bit is automatically cleared by any valid SPI communication
5	SPI error	0	The SPIE is a logical OR combination of errors related to a wrong SPI communication (SCK count and SDI stuck at errors). The SPIE bit is automatically set when SDI is stuck at high or Low. The SPIE is automatically cleared by a valid SPI communication.
4	Thermal shutdown (OT)	0	This bit is set in case of thermal shutdown.
3	ITLOFF	0	Logical OR combination of STi²Fuse latch for all channels.
2	I_{PEAK_DETECT}	0	Logical OR combination of I_{PEAK} detection for all channels.
1	T_{CASE} OR V_{CC_UV} OR V_{CC_OV}	0	This bit is set in case of frame temperature detection or V_{CC} undervoltage or V_{CC} overvoltage.
0	Fail-safe	1	The bit is set in case device operates in fail-safe mode. A detailed description of these root-causes and the fail-safe state itself is specified in the Section 2.2.3: Fail-safe mode

Note: The FFh or 00h combinations for the global status byte are not possible, due to the active low of global status bit (bit7), exclusive combination exists between bit7 and bit0-bit6. Consequently, a FFh or 00h combination for the global status byte must be detected by the microcontroller as a failure (SDO stuck to GND or to V_{DD} or loss of SCK).

4.3.2 RAM

RAM registers can be separated according to the frequency of usage:

- Init - register is read/written during the initialization phase (single shot action)
- Continuous - read/write / read and clear registers are often accessed, applying outputs control and diagnostic
- Rare - read/read and clear status of device registers accessed on demand (in case of failure)

Table 23. RAM memory map

Address	Name	Access	Content	Access type	Reset value
CONTROL REGISTERS					
01h	SOCR	Read/Write	Channel control register	Init	0x0000
02h	CTRL	Read/Write	Control register	Init	0x0000
03h	ITCFGCR0	Read/Write	I²t configuration control register channel0	Init	0x0000
04h	ITCFGCR1	Read/Write	I²t configuration control register channel1	Init	0x0000
... not used area					
STATUS REGISTERS					
10h	OUTSR0	Read/Clear	Output status register channel0	rare	0x0000
11h	OUTSR1	Read/Clear	Output status register channel1	rare	0x0000
... not used area					
12h	ITCNTSR	Read	I²t counter status register	rare	0x0000
20h	ADCISR0	Read	Digital current sense channel0	continuous	0x0000
21h	ADCISR1	Read	Digital current sense channel1	continuous	0x0000
22h	ADCI2TSR0	Read	Digital current sense for I²t channel0	continuous	0x0000
23h	ADCI2TSR1	Read	Digital current sense for I²t channel1	continuous	0x0000
24h	ADCVSR0	Read	Digital output voltage channel0	continuous	0x0000
25h	ADCVSR1	Read	Digital output voltage channel1	continuous	0x0000
26h	ADCVBSR	Read	Digital battery voltage	continuous	0x0000
27h	ADCVTSR	Read	Digital frame temperature sense	continuous	0x0000
3Dh	RESERVED				
3Eh	RESERVED				

Note: Any command (write, read, or read and clear status) executed on a "not used" RAM register that is a not assigned address does not have any effect: there is no change in the global status byte (no communication error, no error flag). The data written to this address is ignored. The data read from this address contains 00, independently of what has been written previously to this address.

A write command on "don't care" bits of an assigned RAM register address does not have any effect: There is no change on the global status byte. The data written to the "don't care bits" is ignored. The content of the "don't care bits" remains at "0" independently of the data written to these bits.

4.3.3 ROM

This memory is used for device identification.

Table 24. ROM memory map

Address	Name	Description	Access	Content
00h	Company code	Indicates the code of STM company	Read only	00H
01h	Device family	Indicates the product family	Read only	03H
02h	Product code 1	Indicates the first code of the product	Read only	58H
03h	Product code 2	Indicates the 2nd code of the product	Read only	56H
04h	Product code 3	Indicates the third code of the product	Read only	06H
05h	Product Code 4	Indicates the fourth code of the product	Read only	42H
0Ah	Version	Silicon version	Read only	01H
… not used area				
10h	SPI Mode	Different Modes of the SPI (see SPI mode)	Read only	A1H
11h	WD Type 1	Indicates the type of watchdog used in the product	Read only	46H
13h	WD bit position 1	Indicates the address of the register containing the WD toggle bit	Read only	40H
14h	WD bit position 2	Indicates the position of the WD toggle bit	Read only	C1H
… not used area				
20h	SPI CPHA	Indicates the polarity and phase of the SPI interface	Read only	55H
3Eh	GSB options	Options of GSB byte (standard GSB definition)	Read only	00H
3Fh	Advanced OP. Code	Access to this address results in a SW reset		

4.3.4 SPI modes

By reading out the <SPI mode> register general information of SPI usage of the device application registers can be read.

Table 25. SPI mode

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Content
BR	DL2	DL1	DL0	SPI8	0	S1	S0	A1H

SPI burst read

Table 26. SPI burst read

Bit 7	Description
0	BR disabled
1	BR enabled

The burst read is implemented in this product so this bit is enabled.

SPI data length

The SPI data length value indicates the length of the SCK count monitor, which is running for all the accesses to the device application registers. In case a communication frame with an SCK count is not equal to the reported one, the device leads to a SPI error and the data is rejected.

The frame length is specified on 3 bits in the SPI mode register located in the ROM part.

The 24-bit SPI communication is implemented in this product so these bits are ‘010’.

Table 27. **SPI data length**

Bit 6	Bit 5	Bit 4	Description
DL2	DL1	DL0	
0	0	0	Invalid
0	0	1	16-bit SPI
0	1	0	24-bit SPI
...			...
1	1	1	64-bit SPI

Data consistency check (parity/CRC)

For some devices, a data consistency check is required. Therefore, either a parity-check or for very sensitive systems a CRC may be implemented.

It is defined on 2 bits in the SPI mode register located in the ROM part. A check is then applied on the incoming frame (SDI) while a calculation elaborated on one/multiple bits is done and integrated on the outgoing frame (SDO).

Table 28. **SPI data consistency check**

Bit 61	Bit 0	Description
S1	S0	
0	0	Not used
0	1	Parity used
1	0	CRC used
1	1	Invalid

In case either the parity or the CRC check is implemented it is always located at the end of the communication.

The device is equipped with the parity control check. In the Tx device, the parity bit is calculated based on the first 23 bits: even number of "1" will set the parity bit to "1", while the odd number of "1" will set the parity bit to "0". In the Rx device, the parity bit is calculated in the same way and compared with the received one. In the case of different parity bit, the received SPI frame is considered as not valid and it is not executed.

4.4 Outputs control

Depending on the actual device mode, outputs can be controlled by the SPI register or the direct input DIx.

SPI register SOCR

In normal mode outputs can be turned ON/OFF, applying Bit[n] = 1/0

[n]: is the related channel, n = 0 for the channel 0, and n = 1 for channel 1

Example 1:

Turning ON channel 0 and 1

Table 29. Write SOCR 0x01

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
0	0	0	0	0	0	0	1
D15	**Data 1**						
Not used	Not used	Not used	Not used	DIENCR1	DIENCR0	SOCR1	SOCR0
x	x	x	x	0	0	1	1
D7	**Data 2**						
SPCR1	SPCR0	CAPCR1	CAPCR0	EXIT_CAPCR1	EXIT_CAPCR0	WDTB	Parity
x	x	x	x	x	x	1/0	0

Direct input DIx

Applying logical high/low to pin turns ON/OFF the associated output in fail-safe. In normal mode, DIx effect is OR-ed with SPI configuration in case DIENCR bit is set.

Emergency input EMx

Setting EMx = High in normal mode will turn off the Channelx.

4.5 Control registers and Status registers

SOCR

Channel control register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used	Not used	Not used	Not used	DIENCR1	DIENCR0	SOCR1	SOCR0	SPCR1	SPCR0	CAPCR1	CAPCR0	EXIT_CAPCR1	EXIT_CAPCR0	WDTB	PARITY
R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R

Address: 0x01h

Type: RW

Reset: 0

Description: Channel control register

[15:12]	Not used
[11]	Direct input signal enable in normal mode of channel 1
[10]	Direct input signal enable in normal mode of channel 0
[9]	SOCR1 bit controls output state of channel 1: 1 - output enabled 0 - output disabled
[8]	SOCR0 bit controls output state of channel 0: 1 - output enabled 0 - output disabled
[7]	Digital current sense sampling point of channel 1 (this setting is only valid for digital current sense, not for STi²Fuse digital current sense): 0 – continuous mode: it allows digital conversion during all ON phase of the selected channel 1 – filtered mode: it allows digital conversion as in continuous mode in addition to a low pass filter to filter data
[6]	Digital current sense sampling point of channel 0 (this setting is only valid for digital current sense, not for STi²Fuse digital current sense): 0 – continuous mode: it allows digital conversion during all ON phase of the selected channel 1 – filtered mode: it allows digital conversion as in continuous mode in addition to a low pass filter to filter data
[5]	Trigger for capacitive charging mode of channel 1 in normal mode: 1 – enables CCM in normal mode 0 – disabled This bit is automatically reset
[4]	Trigger for capacitive charging mode of channel 0 in normal mode: 1 – enables CCM in normal mode 0 – disabled This bit is automatically reset
[3]	Exit of capacitive charging mode of channel 1 in normal mode: 1 – Enabled 0 – disabled This bit is automatically reset

[2]	Exit of capacitive charging mode of channel 0 in normal mode: 1 – Enabled 0 – disabled This bit is automatically reset.
[1]	Watchdog toggle bit. Note: the WD timeout can be optionally disabled by a dedicated OTP.
[0]	PARITY: parity bit

CTRL

Control register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GOSTBY	UNLOCK	CTDTH1	CTDTH0	EN	OTMASK	IPEAKMASK	I2TMASK	Not used	Not used	Not used	Not used	LOCKEN1	LOCKEN0	Not used	PARITY
RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	RW	RW	R	R

Address: 0x02h

Type: RW

Reset: 0

Description: Control register

[15]	GOSTBY: Go to standby. It is necessary to perform 2 write accesses to enter standby from normal mode: 1. Write UNLOCK = 1 and EN = 1 2. Write GOSTBY = 1 and EN = 0
[14]	Unlock bit, has to be set before GOSTBY or EN can be set to 1 This bit allows protected SPI transactions. It means that the next SPI communication will automatically clear this bit and prevent any change of protected data. Therefore, modifying a protected data requires to set UNLOCK bit in a first communication and write the protected data during the next communication
[13:12]	CTDTH[1:0]: Case thermal detection threshold. These bits allow to configure the case thermal detection of the device. Three temperature thresholds are available by programming these two bits. 1. CTDTH1: 0 CTDTH0: 0 = Detection temperature: 110 °C 2. CTDTH1: 0 CTDTH0: 1 = Detection temperature: 70 °C 3. CTDTH1: 1 CTDTH0: 0 = Detection temperature: 90 °C 4. CTDTH1: 1 CTDTH0: 1 = Detection temperature: 130 °C
[11]	EN: enter normal mode 1 - normal mode 0 - fail safe mode It is necessary to perform 2 write accesses to enter normal mode from fail-safe: 1. Wrire UNLOCK = 1 2. Write EN = 1
[10]	OT fault masking bit: 0: OTx fault contributes to LATCH_DIAGx logic state 1: OTx fault contribution to LATCH_DIAGx is masked in normal mode
[9]	I_{PEAK} detection masking bit: 0: IPEAKLSRx fault contributes to LATCH_DIAGx logic state 1: IPEAKLSRx fault contribution to LATCH_DIAGx is masked in normal mode If both IPEAKLSRx and ITLOFFSRx bits are contemporaneously set and IPEAKMASKx is set as well, the contribution of ITLOFFSRx bit to LATCH_DIAGx logic state is masked, even if I2TMASKx is not set. But, if I2TMASKx=0 and both faults bits are contemporaneously cleared, the contribution of I^2t fault to LATCH_DIAG logic state will not be masked for the time interval TF_UNLATCH.
[8]	I^2t fault masking bit: 0: $ITLOFFSR_x$ fault contributes to LATCH_DIAGx logic state 1: $ITLOFFSR_x$ fault contribution to LATCH_DIAGx is masked in normal mode
[7:4]	Not used

[3]	Lock ENABLE ‘1’ means a protected transaction (first setting UNLOCK bit, then modifying the relevant configuration register) is required for changing those bits. When ‘0’ (reset value), those configuration registers may be altered with a single frame standard write command.
[2]	LOCKEN0: Lock enable for capacitive charging mode LOCKEN1: Lock enable for I²t configuration control registers
[1]	Not used
[0]	PARITY: parity bit

ITCFGCRx

I²t configuration control registers channels 0 to 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used	Not used	IPEAKxCFG	INOMSR2x	INOMSR1x	INOMSR0x	TNOMSR2x	TNOMSR1x	TNOMSR0x	Not used	Not used	Not used	Not used	Not used	Not used	PARITY
R	R	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R

Address: 0x03h to 0x04h

Type: RW

Reset: 0

Description: I²t configuration control registers channels 0 to 1

[15:14]	Not used
[13]	Configure current peak level of channel X up to 6x I_nom or 10x I_nom, according to the following settings: 1 --> 6x I_nom 0 --> 10x I_nom
[12:10]	Nominal current setting for I²t curve (see Table 9)
[9:7]	Nominal time setting for I²t curve (see Table 10)
[6:1]	Not used
[0]	PARITY: parity bit

OUTSRx

Output status registers channels 0 to 1 register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used	Not used	DIENSRx	OTSRx	Not used	CAPCSRx	IPEAKLSRx	OFFSRx	ITLOFFSRx	EMRBSR0	CAPFSSRx	Not used	Not used	Not used	Not used	PARITY
R	R	R	RC	R	R	RC	R	RC	R	R	R	R	R	R	R

Address: 0x10h to 0x11h

Type: RC

Reset: 0

Description: Output status registers channels 0 to 1 register

[15:14]	Not used
[13]	Direct input status, image of associated DIx logic level
[12]	Overtemperature feedback status bit. This bit is set when OT fault has been detected and channel is latched off. This bit must be cleared to re-enable the output of the channel.
[11]	Not used
[10]	Capacitive charging mode status bit: 1: CCM enabled 0: CCM disabled
[9]	Channel latch-off status. This bit is set when I_{PEAK} fault has been detected that is when output current reaches I_{PEAK} threshold. When this bit is set the channel is latched off. This bit must be cleared to re-enable the output of the channel.
[8]	Channel off status. This bit is used to read back the driver control signal: 1: OFF-state 0: ON-state
[7]	Channel latch-off status. This bit is set when I^2t counter time has elapsed and channel is latched off. This bit is set also in case of Ipeak_detect. In normal mode, this bit must be cleared to re-enable the output of the channel. In fail-safe mode, DIx toggling unlatches the protection but it not automatically clears this bit. This bit is set also in case output current reaches 10 x INOM, or 6 x INOM in case bit IPEAKxCFG (bit 13 of register ITCFGCRx) is set high.
[6]	Emergency read back status bit. It reflects the status of EMx pin.
[5]	Automatic startup of capacitive charging mode after POR: 1: enabled 0: disabled
[4:1]	Not used
[0]	PARITY: parity bit

ITCNTSR

I²t counter status register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used	Not used	ITCNT1			ITCNT0			I2TCFGINIT	Not used	RST	SPIE	VCCUV	VCCOV	LHIRB	PARITY
R	R	R	R	R	R	R	R	R	R	RC	RC	R	R	R	R

Address: 0x12h

Type: R

Reset: 0x40h

Description: I²t counter status register

[15:14]	Not used
[13:11]	I²t counter status for channel 1: 000 --> [0%:12.5%] 001 --> [12.5%:25%] … 111 --> [87.5%:100%]
[10:8]	I²t counter status for channel 0: 000 --> [0%:12.5%] 001 --> [12.5%:25%] … 111 --> [87.5%:100%]
[7]	Selection of default I²t configuration from OTPs for all channels: ‘0’ --> first configuration of I²t ‘1’ --> second configuration of I²t
[6]	Not used
[5]	Chip reset bit
[4]	SPI error bit
[3]	V_{CC} undervoltage status bit
[2]	V_{CC} overvoltage status bit
[1]	Limp-home pin read back bit
[0]	PARITY: parity bit

ADCISRx

Digital current sense registers channels 0 to 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used	Not used	ADCISR9 (MSB)	ADCISR8	ADCISR7	ADCISR6	ADCISR5	ADCISR4	ADCISR3	ADCISR2	ADCISR1	ADCISR0 (LSB)	Not used	SOCR	UPDTSR	PARITY
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0x20h to 0x21h

Type: R

Reset: 0

Description: Digital current sense registers channels 0 to 1

[15:14]	Not used
[13:4]	Digital value of OUTPUTx current. Output current value = ADCISRx/1023*IOUT_SAT Content is refreshed only in ON state and frozen in OFF state
[3]	Not used
[2]	Read back of SOCR bit control: 0 - output disabled 1 - output enabled
[1]	UPDTSR: updated status bit. This bit is set when ADC value is updated and cleared when register is read.
[0]	PARITY: parity bit

ADCI2TSRx

Digital I²t current sense registers channels 0 to 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used	Not used	ADCI2TSR9 (MSB)	ADCI2TSR8	ADCI2TSR7	ADCI2TSR6	ADCI2TSR5	ADCI2TSR4	ADCI2TSR3	ADCI2TSR2	ADCI2TSR1	ADCI2TSR0 (LSB)	Not used	SOCRx	UPDTSR	PARITY
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0x22h to 0x23h

Type: R

Reset: 0

Description: Digital I²t current sense registers channels 0 to 1

[15:14]	Not used
[13:4]	Digital value of OUTPUT current for I²t function. Output current value = ADCI2TSRx/1023*IOUT_SAT_FUSE Content is refreshed only in ON state and reset at OFF state
[3]	Not used
[2]	SOCR bit controls output state of the channel x: 0 - output disabled 1 - output enabled
[1]	UPDTSR: updated status bit. This bit is set when ADC value is updated and cleared when register is read.
[0]	PARITY: parity bit

ADCVSRx

Digital output voltage registers channels 0 to 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used	Not used	ADCVSR9 (MSB)	ADCVSR8	ADCVSR7	ADCVSR6	ADCVSR5	ADCVSR4	ADCVSR3	ADCVSR2	ADCVSR1	ADCVSR0 (LSB)	Not used	Not used	UPDTSR	PARITY
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0x24h to 0x25h

Type: R

Reset: 0

Description: Digital output voltage registers channels 0 to 1

[15:14]	Not used
[13:4]	Digital value of output voltage for the channel x
[3:2]	Not used
[1]	UPDTSR: updated status bit. This bit is set when ADC value is updated and cleared when register is read.
[0]	PARITY: parity bit

ADCVBSR

Digital battery voltage register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used	Not used	ADCVBSR9 (MSB)	ADCVBSR8	ADCVBSR7	ADCVBSR6	ADCVBSR5	ADCVBSR4	ADCVBSR3	ADCVBSR2	ADCVBSR1	ADCVBSR0 (LSB)	Not used	Not used	UPDTSR	PARITY
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0x26h

Type: R

Reset: 0

Description: Digital battery voltage register

[15:14]	Not used
[13:4]	Digital value of V_{CC} voltage
[3:2]	Not used
[1]	UPDTSR: updated status bit. This bit is set when ADC value is updated and cleared when register is read.
[0]	PARITY: parity bit

ADCVTSR

Digital case thermal sensor voltage register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not used	Not used	ADCVTSR9 (MSB)	ADCVTSR8	ADCVTSR7	ADCVTSR6	ADCVTSR5	ADCVTSR4	ADCVTSR3	ADCVTSR2	ADCVTSR1	ADCVTSR0 (LSB)	Not used	Not used	UPDTSR	PARITY
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 0x27h

Type: R

Reset: 0

Description: Digital case thermal sensor voltage register

[15:14]	Not used
[13:4]	Digital value of case thermal sensor voltage. T_{CASE} (typ.) = 409.13 °C - (1.0473*ADCVTSR[13:4])
[3:2]	Not used
[1]	UPDTSR: updated status bit. This bit is set when ADC value is updated and cleared when register is read.
[0]	PARITY: parity bit

5 Diagnostic

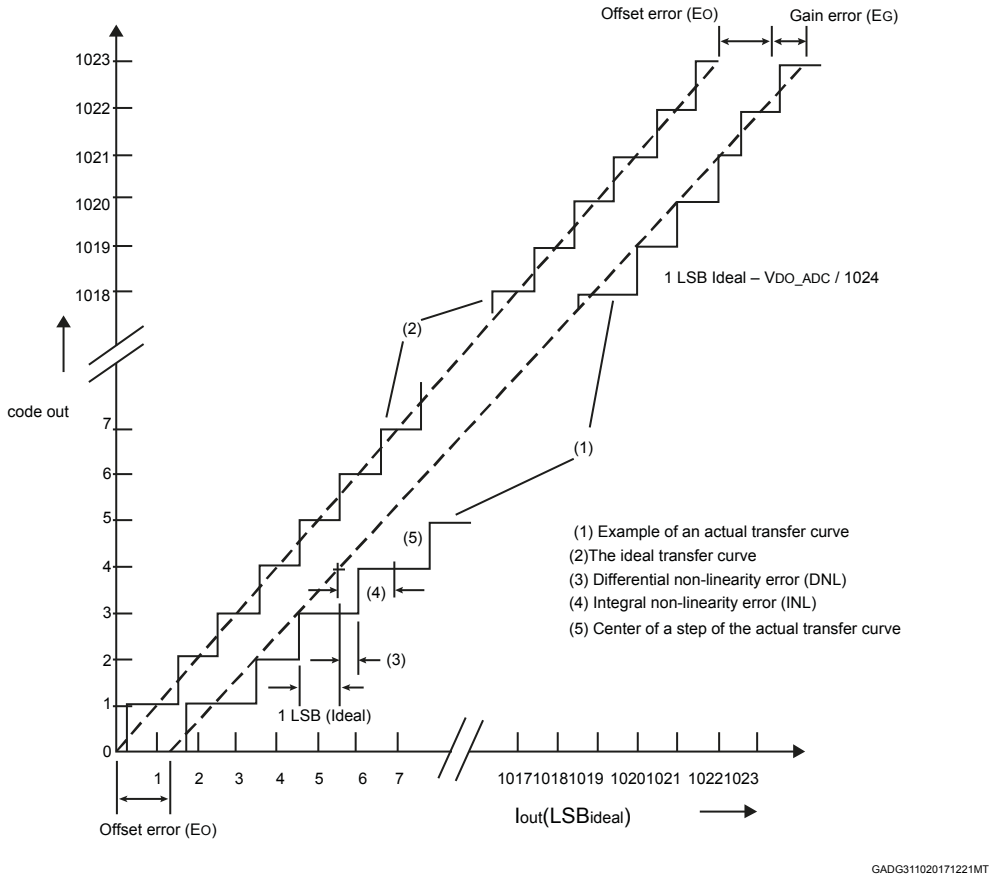
Device is capable of providing digital diagnostic information through the SPI interface.

5.1 Digital current sense diagnostic

5.1.1 ADC characteristics

Here are the “Differential non linearity” and “Integral non Linearity” typical curves for the 10-bit ADC converter.

Figure 15. ADC characteristics and error definition



5.1.2 ADC operating principle

The device provides a 10-bit successive approximation register (SAR) analog to digital converter. It is used to provide a digital information about the current sense feedback proportional to the output current. An integrated LP (progressive average) filter can be used to filter data coming from the ADC conversion reducing the effect of random noise coming from analog current sense amplifier.

Note: The internal ADC is able to work in both normal and fail-safe conditions.

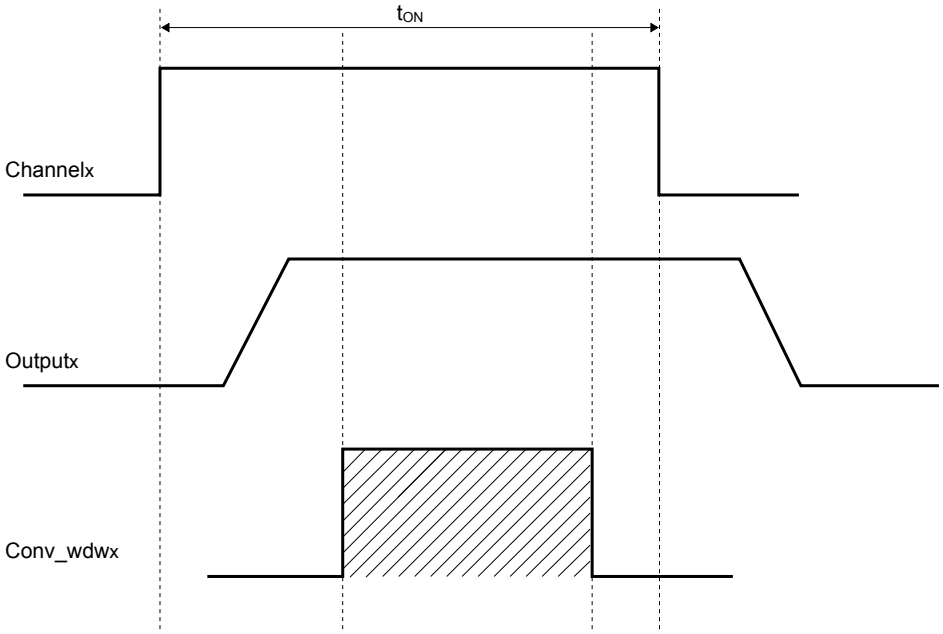
The integrated ADC control logic is designed to lead to a good 10-bit approximation of current sense/temperature feedback.

After each conversion, an updated bit “UPDTSR” is set to advise about new conversion data. This bit is reset after the read process of the dedicated RAM register.

The data is maintained in the register until the next conversion results are available. The ADC register is refreshed at the end of each conversion and maintained during the conversion of the current sample. The data is converted to the 10-bit register, the formula is equal to:

Iout_conv = data (10bit)/K;

Figure 16. **Conversion window generation**



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A minimum conversion time ($t_{ON\_CS(min)}$) is defined to allow the signal stabilization at the input of the ADC converter and considering the sampling time.

5.1.3 Registers

The results of the digital conversion are stored in the “Digital current sense registers”. Two registers are used for the digital conversion of the output current:

- ADCISRx (address from 20h to 21h) - Digital outputx current sense (one register x channel)
- ADCI2TSRx (address from 22h to 23h) - Digital Outputx current sense for I²t function (one register x channel)

Table 30. **Registers**

Register name	Bit 15, 14	Bit 13 ... 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCISRx 20h to 21h	Not used	Digital value of OUTx current. Content is refreshed only in ON state and frozen in OFF State	Not used	SOCRx Possibility to control the Outx state (read only)	UPDTSR Updated status bit. It is set when value is updated and cleared when register is read	Parity
ADCI2TSRx 22h to 23h	Not used	Digital value of OUTx current for I²t function. Content is refreshed only in ON state and reset in OFF State	Not used	SOCRx Possibility to control the Outx state (read only)	UPDTSR Updated status bit. It is set when value is updated and cleared when register is read	Parity

5.1.4 Asynchronous mode

The device is able to operate two different sampling modes, configurable by one bit per channel, SPCRx, in the channel control register, SOCR:

Table 31. Sampling mode

SPCRx	Sampling mode
0	CONTINUOUS mode
1	FILTERED mode (Digital Outputx current only)

In asynchronous mode (continuous or filtered) the ADC result register is continuously refreshed, provided the channel is commanded on either through direct input signal or through SOCR register.

Table 32. Sampling mode configuration

SPCRx	SOCRx	DIx	Sampling mode
1	1	x	Asynchronous with continuous sampling and digital LP filter (1st result after 16 samples)
0	1	x	Asynchronous with continuous sampling
x	0	1	Asynchronous with continuous sampling (fail-safe mode)

5.2 Integrated LP (progressive average) filter

In asynchronous mode, when the filtered mode is selected through the dedicated bits “SPCR1 = 1” and “SPCR0 = 1”, the integrated LP filter is activated. This component will filter the data coming from the ADC conversion reducing the effect of random noise coming from the analog current sense amplifier.

Features of the integrated LP filter:

- 1st order decimating filter on 16 samples
- 1st result after 1 sample with progressive averaging of 16 successive samples:

$$data\,(N) = \left(data\,(N-1) \cdot \frac{15}{16}\right) + data_i/16$$

- Asynchronous reset like POR reset filtered value
- Continues to accumulate samples when channel is in on-state
- Keeps digitalized value when channel is in off-state

5.3 Digital diagnostic

The global status byte (GSB) provides the preliminary status of the device during the SPI communication with the device. It informs about the device actual mode (normal/fail-safe).

By reading the additional status registers, more detailed information is provided. Status information is stored in the status registers.

5.3.1 Status registers

Table 33. Status registers

Address	Name	Access	Description
10h to 11h	OUTSRx	Read/Clear	Outputs status register (see register map for detailed description)
12h	ITCNTSR	Read	I²t counters status
20h to 21h	ADCISRx	Read	Digital current sense registers.
22h to 23h	ADCI2TSRx	Read	Digital current sense registers for I²t function
24h to 25h	ADCVSRx	Read	Digital output voltage registers
26h	ADCVBSR	Read	Digital battery voltage sense register
27h	ADCVTSRx	Read	Digital case temperature sensor voltage sense register.

5.4 Open-load ON-state detection

The open-load ON-state is performed by reading the digital current sense. In case the output is on and the reported digital current sense value is below the requested threshold, the open-load condition can be reported.

5.5 DIENSR (Direct Input Status bits in OUTSRx)

DIENSR bits read back the logic level of the DIx Input dedicated to the specific channel.

5.6 Overtemperature

The OTSRx provides an OT (overtemperature) failure flag related to OUTPUTx. If triggered, the bit is latched and keeps its status until a read and clear command on OTSRx is performed by SPI.

5.7 I_{PEAK} detection

The IPEAKLSRx provides the I_{PEAK} detection feedback for each channel. The bit is set when an I_{PEAK} event is detected, and it keeps its status until a read and clear command on IPEAKLSRx is performed by SPI.

5.8 I²t status

The ITLOFFSRx provides the I²t event feedback for each channel. The bit is set when a I²t event is detected, and it keeps its status until a read and clear command on ITLOFFSRx is performed by SPI.

6 Electrical specifications

6.1 Absolute maximum ratings

Stressing the device above the rating listed in the Table 34. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 34. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC_LSC}	Maximum supply voltage for full short-circuit protection	19	V
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
V_{CC}	DC supply voltage	35	V
$-V_{CC}$	Reverse DC supply voltage (without external components)	16	V
$-I_{GND}$	DC reverse GND pin current	200	mA
$I_{OUT0,1}$	Maximum DC output current	Internally limited	A
$-I_{OUT0,1}$	Reverse DC output current	126	A
V_{SDO}	DC SPI pin voltage	V_{DD} + 0.3	V
$-V_{SDO}$	Reverse DC SPI pin voltage	-0.3	V
$I_{SDI,CSN,SCK}$	DC SPI pin current	+10/-1	mA
I_{DD}	DC digital control supply current for SPI interface	+10/-1	mA
V_{DD}	DC digital control supply for SPI interface	6	V
$-V_{DD}$	Reverse DC digital control supply for SPI interface	-0.3	V
$I_{DIN0,1}$	DC direct input current	+10/-1	mA
$I_{EM0,1}$	DC emergency pin current	+10/-1	mA
$I_{LATCH\_DIAG0,1}$	DC LATCH_DIAG pin current	+10/-1	mA
I_{LH}	DC limp-home pin current	+10/-1	mA
I_{VREG}	DC VREG pin current	+10/-1	mA
E_{MAX}	Maximum switching energy (single pulse, T_{Jstart} = 150 °C)	130	mJ
ESD	Electrostatic discharge	(ANSI-ESDA-JEDEC-JS-001-2014)	
	DI0, DI1, EM0, EM1, LATCH_DIAG0, LATCH_DIAG1, LH, V_{REG}	2000	V
	V_{DD}	2000	
	CSN, SDI, SCK, SDO	2000	
	$OUT_{0,1}$	4000	
	V_{CC}	4000	
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_J	Junction operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C
I_{LAT}	Latch-up current	±20	mA

6.2 Thermal data

Table 35. Thermal data

Symbol	Parameter	Typ. value	Unit
R_{thJB}	Thermal resistance, junction-to-board (JEDEC JESD 51-8)	4.51	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	18.45 (see Figure 24)	°C/W

6.3 SPI electrical characteristics

2.7 V < V_{DD} < 5.5 V, 7 V < V_{CC} < 28 V, -40 °C < T_J < 150 °C, unless otherwise specified.

Table 36. DC characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VDD pin						
I_{DD}	SPI interface supply current in normal mode	V_{DD} = 5 V; SPI active without frame communication; CSN high		14	20	µA
I_{DDstd}	SPI interface supply current in standby state	V_{DD} = 5 V; T_J = 125 °C; INx = 0 V		0.05	10	µA
SDI, SCK pins						
I_{IL}	Low level Input current	$V_{SDI,SCK}$ = 0.3 V_{DD}	1		10	µA
I_{IH}	High level Input current	$V_{SDI,SCK}$ = 0.7 V_{DD}	1		10	µA
V_{IL}	Input low voltage				0.3 V_{DD}	V
V_{IH}	Input high voltage		0.7 V_{DD}			V
V_{I_HYST}	Input hysteresis voltage			0.5		V
V_{SDI_CL}	SDI clamping voltage	I_{IN} = 1 mA	6		8.2	V
		I_{IN} = -1 mA		-0.7		V
V_{SCK_CL}	SCK clamping voltage	I_{IN} = 1 mA	6		8.2	V
		I_{IN} = -1 mA		-0.7		V
SDO pin						
V_{OL}	Output low voltage	I_{SDO} = -5 mA; CSN low; fault condition			0.2 V_{DD}	V
V_{OH}	Output high voltage	I_{SDO} = 5 mA; CSN low; no fault condition	0.8 V_{DD}			V
I_{LO}	Output leakage current	V_{SDO} = 0 V or V_{DD}, CSN high	-5		5	µA
CSN pin						
I_{IL_CSN}	Low level Input current	V_{CSN} = 0.3 V_{DD}	-10			µA
I_{IH_CSN}	High level Input current	V_{CSN} = 0.7 V_{DD}			-1	µA
V_{IL_CSN}	Output low voltage				0.3 V_{DD}	V
V_{IH_CSN}	Output high voltage		0.7 V_{DD}			V
V_{HYST_CSN}	Input hysteresis voltage			0.5		V
V_{CL_CSN}	CSN clamping voltage	I_{IN} = 1 mA	6		8.2	V
		I_{IN} = -1 mA		-0.7		V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{CSN\_LOW\_WUP}$	CSN low filtering time at standby		10	25	55	µs

Table 37. AC characteristics (SDI, SCK, CSN, SDO)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{OUT}	Output capacitance (SDO)	V_{OUT} = 0 V to 5 V	-	-	20	pF
C_{IN}	Input capacitance (SDI)	V_{IN} = 0 V to 5 V	-	-	20	pF
	Input capacitance (other pins)	V_{IN} = 0 V to 5 V	-	-	20	pF

Table 38. Dynamic characteristics

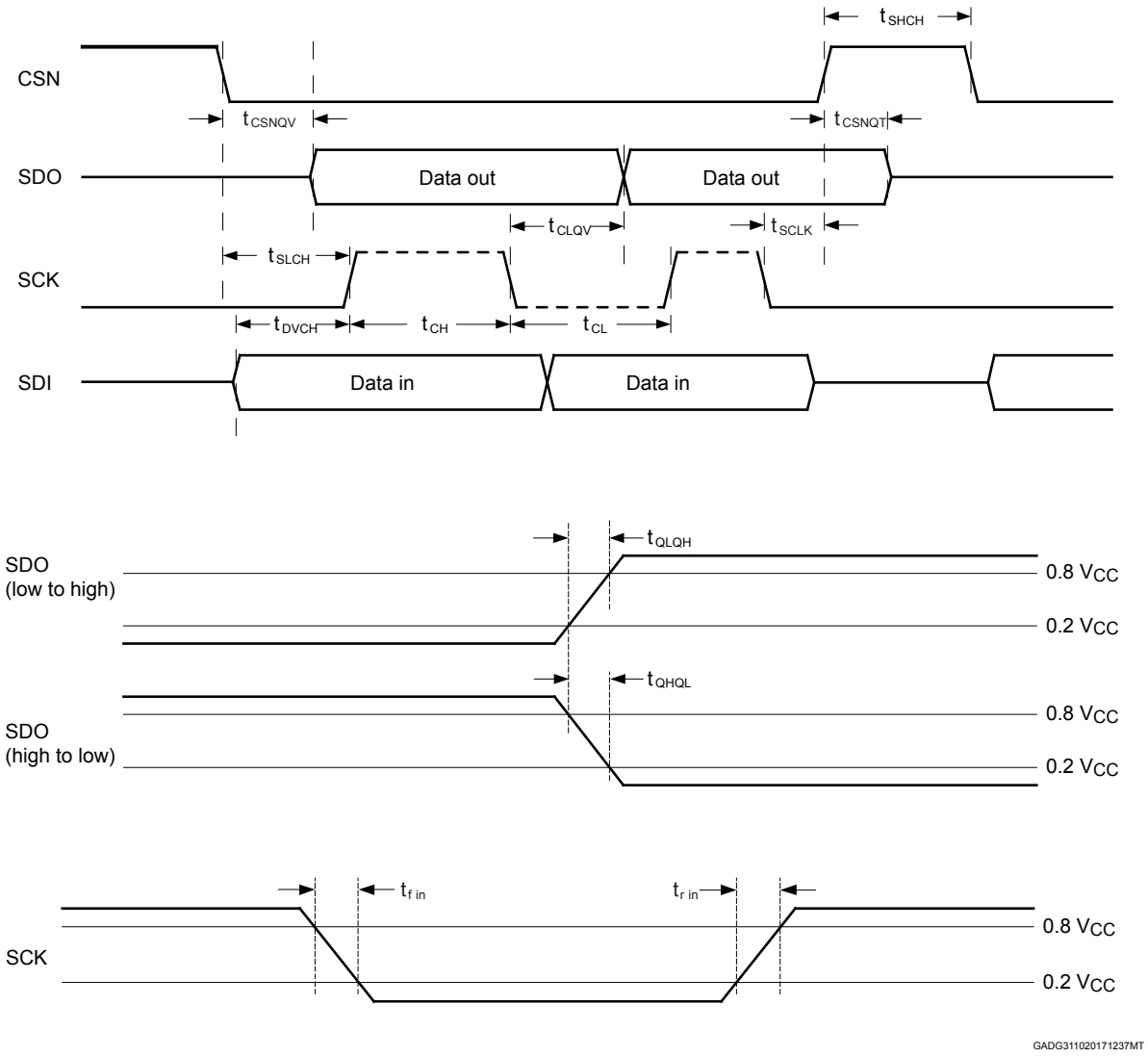
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_C	SPI clock frequency	Duty cycle = 50%			8	MHz
t_{SLCH}	CSN low setup time		60			ns
t_{SHCH}	CSN high setup time		600			ns
t_{DVCH}	Data in setup time		10			ns
t_{CHDX}	Data in hold time		15			ns
t_{CH}	Clock high time		60			ns
t_{CL}	Clock low time		60			ns
t_{CLQV}	Clock low to output valid	C_{OUT} = 1 nF		75		ns
t_{QLQH}	Output rise time	C_{OUT} = 1 nF		55		ns
t_{QHQL}	Output fall time	C_{OUT} = 1 nF		55		ns
t_{SCLK} (1)	SCK setup time before CSN rising		20			ns
t_{CSNQV}(1)	CSN low to output valid				200	ns
t_{CSNQT}(1)	CSN high to output tristate				200	ns

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

Table 39. Digital timings

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_ccm_cycle	Time to exit from capacitive charging mode		200	250	300	ms
t_di_mon	Time window to enter in capacitive charging mode in fail-safe		198	300	402	µs
t_prestdby	Time to go to pre-standby		11	14	16	ms
t_stdby_en	Minimum time from pre-standby to standby mode		90	100	110	µs
t_filter_ipeak	Filtering time of I_{PEAK} detection		0.95	1.2	1.45	µs
t_{LF}	Period for low frequency charging mode		3.4	4	4.6	ms
t_{HF}	Period for high frequency charging mode		0.85	1	1.15	ms
MAX_COUNTER_LF	Maximum number of autorestart pulses allowed in short-circuit				30	
t_{WKUP_FDBCK}	Wake-up feedback timing after power-on reset	After power-on, $LATCH\_DIAG_x$ pins are pulled low for t_{WKUP_FDBCK} delay. The parameter is measured between 10% of falling and rising edges of $LATCH\_DIAG_x$ pins.	0.8	1.0	1.2	ms
t_{LH}	Limp-home pin symmetrical filtering time		20	25	30	µs
$t_{CSN\_LOW\_FS}$	Filtering time of CSN_LOW signal in Fail-safe mode		0.8	1	1.2	µs
$t_{CSN\_LOW\_PSTB}$	Filtering time of CSN_LOW signal in pre-standby mode		20	25	30	µs
t_{WHCH}	CSN timeout: time to release SDO bus		80		140	ms
t_{WDTB}	Watchdog toggle bit timeout		80		140	ms
$i\_time\_tol\_t$	I-t tolerance on time step		0.9*(t - 32)		1.1*(t + 125)	µs
$t_{F\_UNLATCH}$	Minimum time for I^2t protection on channel x to unlatch after a R&C of the $ITLOFFSR_x$ bit				70	µs
$t_{F\_UNLATCH\_DIx\_TOGGLE}$	Minimum time for I^2t protection on channelx to unlatch after a toggling of DIx pin in Failsafe Mode		15		95	µs
t_{DIx_TOGGLE}	Filtering time for DIx toggling, to unlatch channelx in case of fault in Failsafe Mode		15		25	µs
t_{HSHT_DELAY}	Intervention delay of the I^2t protection at 10xINOM/6xINOM				40	µs
t_{BLANK_CS}	Blanking time for digital current sense after rising edge of command signal		125	150	175	µs

Figure 17. **SPI dynamic characteristics**



6.4 Electrical characteristics

7 V < V_{CC} < 28 V, –40 °C < T_J < 150 °C, unless otherwise specified.

Table 40. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4	13	28	V
V_{USD}	Undervoltage shutdown	V_{CC} decreasing			3.4	V
V_{POR}	Undervoltage shutdown on V_{REG}	V_{REG} decreasing	1.5		1.9	V
V_{POR_HYST}	Undervoltage shutdown on V_{REG} hysteresis			0.15		V
R_{ON}	On-state resistance(1)	I_{OUT} = 30 A, T_J = 25 °C		1.2		mΩ
		I_{OUT} = 30 A, T_J = 150 °C			2.4	
		I_{OUT} = 30 A, V_{CC} = 4 V, T_J = 25 °C			2.2	
		I_{OUT} = 30 A, V_{CC} = 3.4 V, T_J = 25 °C			12.5	
R_{ON_Rev}	R_{DSON} in reverse battery condition(1)	I_{OUT} = 30 A, V_{CC} = 13 V, T_J = 25 °C		1.2		mΩ
V_{clamp}	V_{CC} clamp voltage	I_{CC} = 20 mA, $I_{OUT0,1}$ = 0 A, T_J = -40 °C	35			V
		I_{CC} = 20 mA, $I_{OUT0,1}$ = 0 A, 25 °C < T_J < 150 °C	36	38	45	
I_S	Supply current	Standby mode, DIx = 0 V, V_{DD} = 0 V, V_{CC} = 13 V, T_J = 25 °C		0.025	0.4	µA
		Standby mode, DIx = 0 V, V_{DD} = 0 V, V_{CC} = 13 V, T_J = 85 °C		0.3	0.8	µA
		Standby mode, DIx = 0 V, V_{DD} = 0 V, V_{CC} = 13 V, T_J = 125 °C		2.3	10	µA
I_{Son}	Supply current in active mode (fail-safe or normal mode)	ON-state (all channels OFF), V_{CC} = 13 V, V_{DD} = 5 V, $I_{OUT0,1}$ = 0 A		5.5	7	mA
ΔI_{Son}	Additional supply current for each output in ON state driving nominal current	ON-state (per channel), V_{CC} = 13 V, V_{DD} = 5 V, $I_{OUT0,1}$ = A			4	mA
$I_{L(off)}$	OFF-state output current	V_{DI} = 0 V, V_{OUT} = 0 V, V_{CC} = 13 V, T_J = 25 °C	0	0.01	0.8	µA
		V_{DI} = 0 V, V_{OUT} = 0 V, V_{CC} = 13 V, T_J = 125 °C, Ch0,1 (per channel)	0		10	µA
$I_{L(off)2}$	OFF-state output current at V_{OUT} = V_{CC}	No standby, V_{DI} = 0 V, V_{OUT} = 13 V, V_{CC} = 13 V			100	µA
		Standby, V_{DI} = 0 V, V_{OUT} = 13 V, V_{DD} = 0 V, V_{CC} = 13 V			5	
$V_{F0,1}$	Output V_{CC} diode voltage	V_{CC} = 13 V, I_{OUT} = 30 A, T_J = 150 °C			0.7	V

1. *For each channel.*

Table 41. Switching (V_{CC} = 13 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{don} (1)	Turn-on delay time Ch0,1 at T_J = 25 °C to 150 °C	Fail-safe mode, from DIx rising to 20%V_{OUT}, R_L = 0.43 Ω	1.8	3.6	4.8	µs
t_{doff} (1)	Turn-off delay time Ch0,1 at T_J = 25 °C to 150 °C	Fail-safe mode, from DIx falling to 80%V_{OUT}, R_L = 0.43 Ω	2.9	4.5	7.7	µs
t_{stdby_out}	Time required for a complete transition from Standby Mode to Fail Safe Mode, defined from the rising edge of the signal DIx, up to the falling edge of Latch_Diagx	C_{VREG} = 100 nF	15.5	27	40	µs
$t_{stbdy\_out\_efuse\_on}$	Time interval from the rising edge of DIx in Standby Mode to 70% V_{OUT} (V_{OUT} = 70% V_{CC})	C_{VREG} = 100 nF			95	µs
$(dV_{OUT}/dt)_{on}$ (1)	Turn-on voltage slope at T_J = 25 °C to 150 °C	R_L = 0.43 Ω	0.1	0.38	1.1	V/µs
$(dV_{OUT}/dt)_{off}$ (1)	Turn-off voltage slope at T_J = 25 °C to 150 °C	R_L = 0.43 Ω	1.0	6.5	15.5	V/µs
W_{ON} (2)	Switching energy losses at turn-on	R_L = 0.43 Ω		5.1	13	mJ
W_{OFF} (2)	Switching energy losses at turn-off	R_L = 0.43 Ω		0.45	0.7	mJ

1. See *Figure 18. Switching characteristics*.
2. *Parameter guaranteed by design and characterization.*

Table 42. Logic inputs ($DI_{0,1}$, $EM_{0,1}$, LH pins)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	V_{DIN} = 0.9 V	1			µA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	V_{DIN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.2			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	6.0		8.2	V
		I_{IN} = -1 mA		-0.7		V
t_{DI_WUP}	Filtering time at standby		0.8	1.5	2.7	µs

Table 43. Fault diagnostic feedback (LATCH_DIAG0,1 pins)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{LD\_FAULT0,1}$	LATCH_DIAG output voltage in fault condition	I_{LATCH_DIAG} = -1 mA			0.5	V
$V_{LD\_FAULT0,1}$	LATCH_DIAG clamp voltage	I_{LATCH_DIAG} = 1 mA	6		8.2	V
		I_{LATCH_DIAG} = -1 mA		-0.7		V

Table 44. Voltage regulator (V_{REG})

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{REG_OUT}	Pre-regulator output voltage	V_{CC} = 13 V, T_J = 25 °C	4	4.9	6	V
V_{REG_DROP}	Maximum V_{CC} – V_{REG} drop at low V_{CC}	V_{CC} = 4 V, Channel ON		0.25	0.7	V
V_{VREG_CL}	V_{REG} clamp voltage	I_{EN} = 1 mA	6		8.2	V
		I_{EN} = -1 mA		-0.7		V

Table 45. Protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Shutdown temperature		150	175	215	°C
T_{RS}	Thermal reset of OTSR fault detection(1)	V_{CC} = 13 V	135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_{RS})(1)	V_{CC} = 13 V		10		°C
T_{CSD}(1)	Case thermal detection pre-warning	V_{CC} = 13 V (see CTRL)	$T_{CSD\ nom}$ -10	$T_{CSD\ nom}$	$T_{CSD\ nom}$ +10	°C
T_{CR}	Case thermal detection reset(1)	V_{CC} = 13 V	$T_{CR\ nom}$ -10	$T_{CR\ nom}$	$T_{CR\ nom}$ +10	°C

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

6.5 ADC

Table 46. ADC

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ADC_INL	Integral non-linearity error	-	-	-	2	LSB
ADC_DNL	Differential non-linearity error	-	-	-	1	LSB

Table 47. Protection and diagnostic (7 < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{PEAK}(1)	Short-circuit current	V_{DD} = 5 V, V_{CC} = 16 V, L_L = 5 µH, R_L = 50 mΩ, T_J = -40°C	100		160	A
		V_{DD} = 5 V, V_{CC} = 16 V, L_L = 5 µH, R_L = 50 mΩ, T_J = 150°C	145		205	A
$t_{\_blank\_ipeak}$	Blanking time for Ipeak detection after rising edge of command signal			8		µs
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A, $V_{IN0,1}$ = 0 V, L = 6 mH, 25 °C < T_J < 150 °C	V_{CC} -35	V_{CC} - 38	V_{CC} - 45	V

1. *I_{PEAK}, ensured between 7 V and 16 V, -40 °C < T_J < 150 °C.*

Table 48. Digital current sense (7 V < V_{CC} < 18 V, T_J = -40 °C to 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
ADC_{SM_Time}	Sample rate				10	µs
K_0	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 1.2 A	-38%	25.4	38%	1/A
dK_0/K_0 (1)(2)	Digital current sense gain drift	I_{OUT} = 1.2 A	-28		28	%
K_1	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 6 A	-12%	25.4	12%	1/A
dK_1/K_1 (1)(2)	Digital current sense gain drift	I_{OUT} = 6 A	-9		9	%
K_2	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 30 A	-7%	25.4	7%	1/A
dK_2/K_2 (1)(2)	Digital current sense gain drift	I_{OUT} = 30 A	-4		4	%
I_{OUT_OFFSET} (1)	Output current offset	I_{SENSE} = 000H	150		150	mA
I_{OUT_SAT}	Output saturation current	I_{SENSE} = 3FFH	34.3	40.3		A
$V_{OUT\_CD\_SD}$	Current sense minimum output voltage	Output voltage for CS shutdown			6.5	V
$t_{ON\_CS(min)}$	Minimum ON time for digital current sense availability		125	150	175	µs
$t_{ON\_CS(min)}$	Minimum ON time for stable digital CS availability, from rising edge of command signal up to 90% of analog CS signal	T_J = 25 °C to 150 °C		240	450	µs

1. *Parameter specified by design and evaluated by characterization, not tested in production.*
2. *All values refer to V_{CC} = 13 V; T_J = 25°C, unless otherwise specified.*

Table 49. STi²Fuse digital current sense (7 V < V_{CC} < 18 V, T_J = -40 °C to 150 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$ADCf_{SM\_Time}$	Sample rate				10	µs
K_{F0}	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 9 A	-12%	6.3	12%	1/A
dK_{F0}/K_{F0} (1)(2)	Digital current sense gain drift	I_{OUT} = 9 A	-15		15	%
K_{F1}	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 32 A	-7%	6.3	7%	1/A
dK_{F1}/K_{F1} (1)(2)	Digital current sense gain drift	I_{OUT} = 32 A	-4		4	%
K_{F2}	Digital current sense gain: ADC_{OUT}/I_{OUT}	I_{OUT} = 120 A	-7%	6.3	7%	1/A
dK_{F2}/K_{F2} (1)(2)	Digital current sense gain drift	I_{OUT} = 120 A	-4		4	%
$I_{OUT\_OFFSET\_Fuse}$ (1)	Fuse output current offset	I_{SENSE} = 000H	-590		590	mA
$I_{OUT\_SAT\_Fuse}$	Fuse output saturation current	I_{SENSE} = 3FFH	138.5	161		A
V_{OUT_FSD}	Fuse sense minimum output voltage	Output voltage for fuse CS shutdown			6.5	V

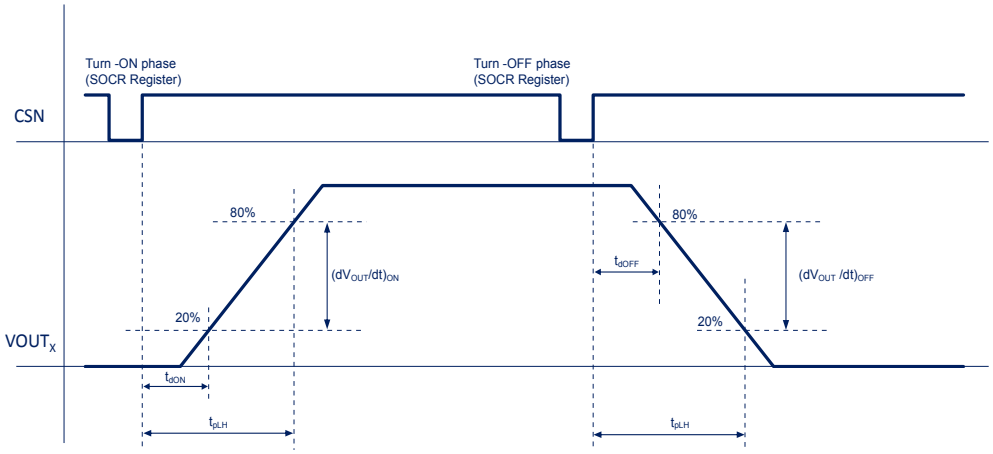
1. *Parameter specified by design and evaluated by characterization, not tested in production.*
2. *All values refer to V_{CC} = 13 V; T_J = 25°C, unless otherwise specified.*

Table 50. Digital monitoring (7 < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$ADC_{V_{CC}\_SM\_Time}$	Sample rate				150	µs
$V_{CC\_digital}$	Digital V_{CC} voltage feedback	3.4 V < V_{CC} < 24 V	-8%	1023* V_{CC}/25V	8%	
$V_{OUT\_digital}$	Digital output voltage feedback	2.4 V < V_{OUT} < 3.4 V	-9%	1023* V_{OUT_x}/25V	9%	
		3.4 V < V_{OUT} < 24 V	-8%	1023* V_{OUT_x}/25V	8%	
$T_{CASE\_digital}$(1)	Digital case temperature feedback	T_{CASE} = 125 °C	-10	See CTRL(2)	10	°C
V_{CCUV_TH}	V_{CC} undervoltage threshold		-8%	8	+8%	V
V_{CCUV_HYS}	V_{CC} undervoltage threshold hysteresis			0.5		V
V_{CCOV_TH}	V_{CC} overvoltage threshold		-8%	25	+8%	V
V_{CCOV_HYS}	V_{CC} overvoltage threshold hysteresis			0.5		V
V_{OUT_THR}	V_{OUT} threshold for capacitive charging mode		-9%	3	+9%	V
C_{max}	Max. capacitive load	V_{CC} = 16 V, T_J = 85 °C, t_{Cmax} = t_ccm_cycle, ESR = 80 mΩ		10		mF

1. *Garanteed by characterization from 70 °C to 130 °C*
2. *Refer to the bit 12 and bit 13 in the CTRL register.*

Figure 18. Switching characteristics



GADG200320230817GT

7 ISO Pulse

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the VCC pin, is tested in accordance with ISO7637-2:2011(E) and ISO 16750-2:2010.

The related function performances status classification is shown in the Table 51. ISO 7637-2 - electrical transient conduction along supply line.

Test pulses are applied directly to DUT (device under test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, with external components, as shown in Figure 1.

“Status II” is defined in ISO 7637-1 Function Performed Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 51. ISO 7637-2 - electrical transient conduction along supply line

Test pulse 2011(E)	Test pulse severity level with status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	Us(1)				
1(2)	III	-112 V	500 pulses	0.5 s	5 s	2 ms, 10 Ω
2a (3)	III	+55 V	500 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	IV	-220 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
3b	IV	+150 V	1 h	90 ms	100 ms	0.1 µs, 50 Ω
4(4)	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B(3)		+87 V	5 pulses	1 min		400 ms, 2 Ω

1. *US is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.*
2. *With -18 V external suppressor referred to ground (from -40 °C to 150 °C).*
3. *With 35 V external suppressor referred to ground (-40 °C < T_J < 150 °C).*
4. *Test pulse in ISO 7637-2:2004(E).*

8 Application schematic

Figure 19. **Application schematic**

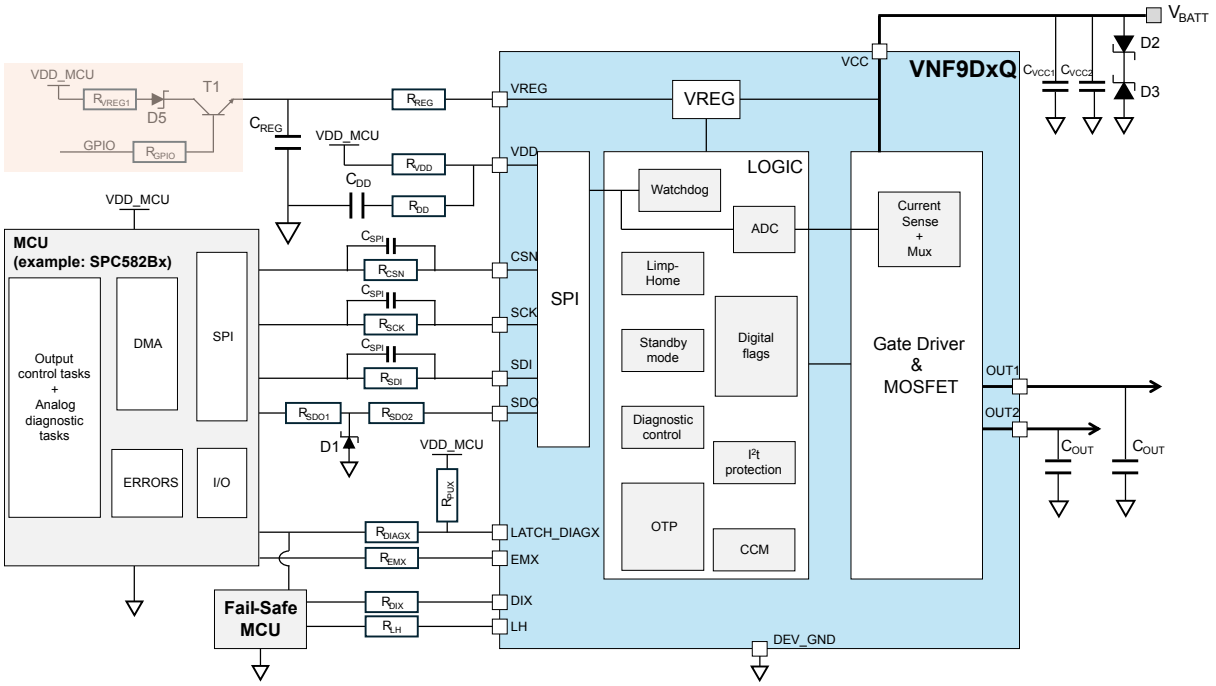


Table 52. Component values

Reference	Value	Comment
CV_{CC1}	100 nF	Battery voltage spikes filtering mounted close to IC
CV_{CC2}	2.2 µF	
D2	Suppressor 18-20 V (for example SMA6F18AY)	Negative transient protection for ISO pulse 1 Transil diode close to V_{CC} pin
D3	Suppressor 33-36 V (for example SMA6F33AY)	Overvoltage protection for ISO pulse 2a
R_{CSN}, R_{SCK}, R_{SDI}	2.7 kΩ	Microcontroller protection during overvoltage and reverse polarity
C_{SPI}	100 pF	Optional SPI frequency speed up capacitor
R_{SDO2}	220 Ω	Microcontroller protection during overvoltage and reverse polarity
R_{SDO1}	50 Ω	Optional
D1	BAT54	Microcontroller protection during overvoltage and reverse polarity
R_{EMX}, R_{DIX} R_{L_DIAGX}, R_{LH}	15 kΩ	Microcontroller protection during: overvoltage, reverse polarity, and loss of GND
R_{PUX}	4.7 kΩ	Pull-up resistor of open-drain active low diagnostic pins
RV_{DD}	330 Ω for V_{DD} = 5 V 150 Ω for V_{DD} = 3.3 V	Device logic protection
C_{DD}	1 nF	Capacitor acts as current source to charge MISO bus capacitance
R_{DD}	100 Ω	Needed for ESD protection
C_{REG}	100 nF	VREG pin protection network C_{REG} dimension required to maintain RAM register content during ISO pulse 1a
R_{REG}	120 Ω	
T1	BC847	
D5	BAT54	
R_{VREG}	1 kΩ	
R_{GPIO}	4.7 kΩ	

9 Maximum demagnetization energy (V_{CC} = 16 V)

Figure 20. Maximum turn off current versus inductance

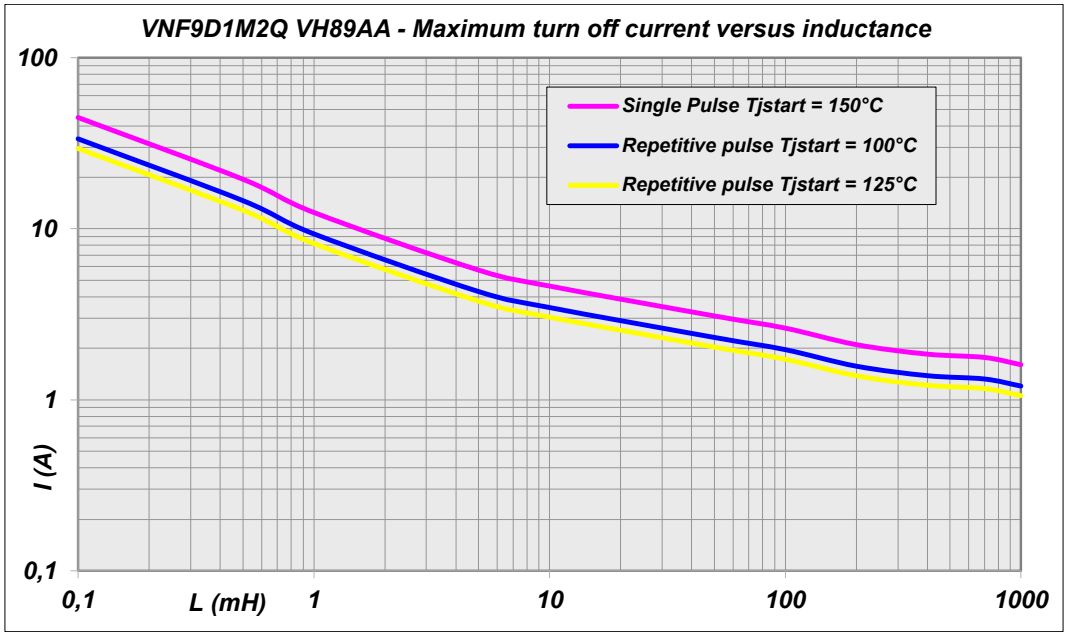
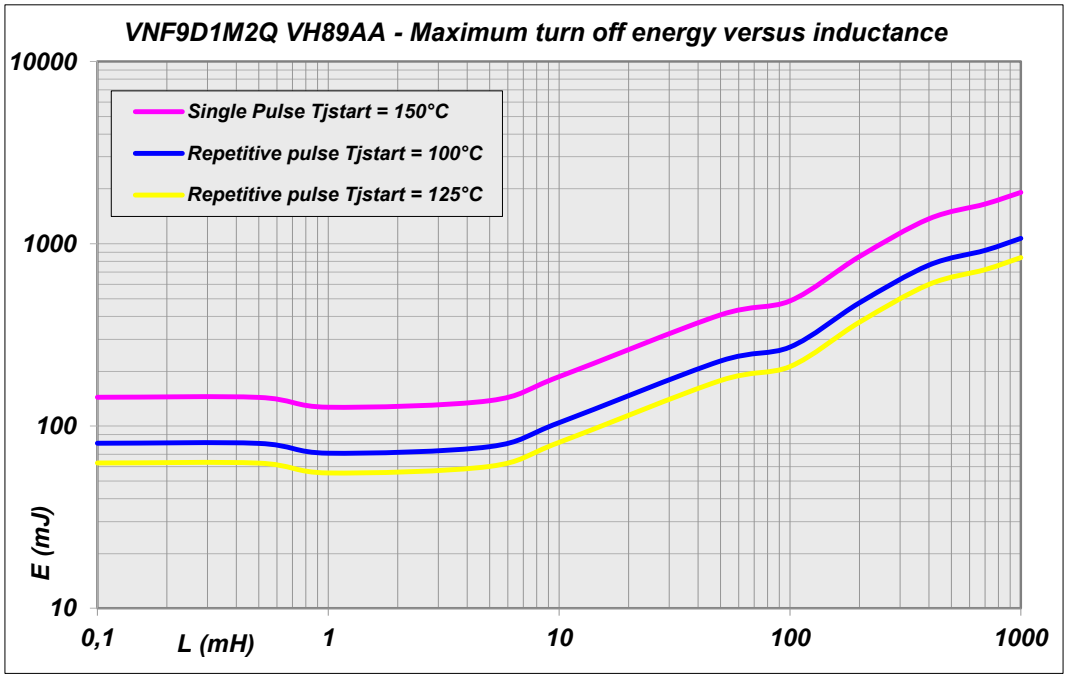


Figure 21. Maximum turn off energy versus inductance



10 Package and PCB thermal data

10.1 PQFN (7x8.5 mm) thermal data

Figure 22. PQFN (7x8.5 mm) PCB footprint, 2 cm^2 and 8 cm^2

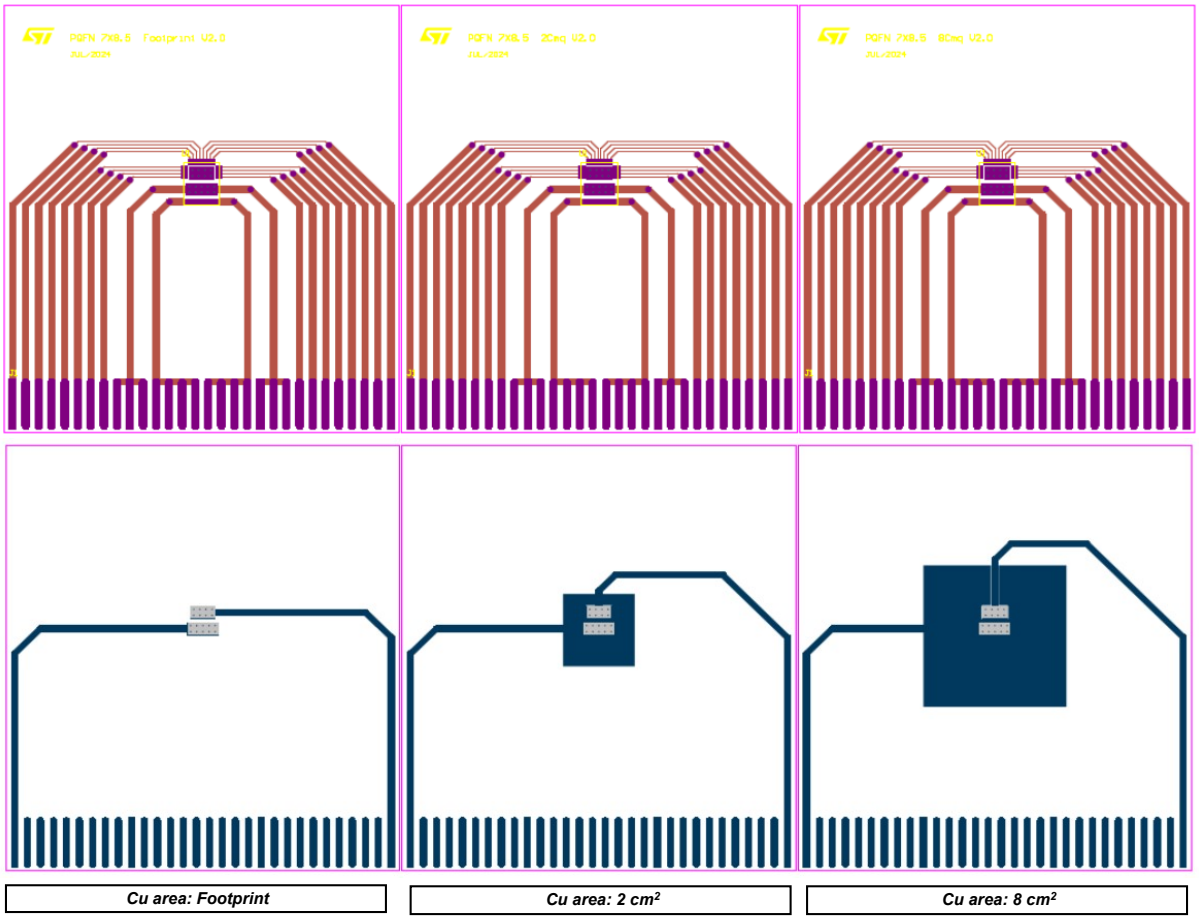
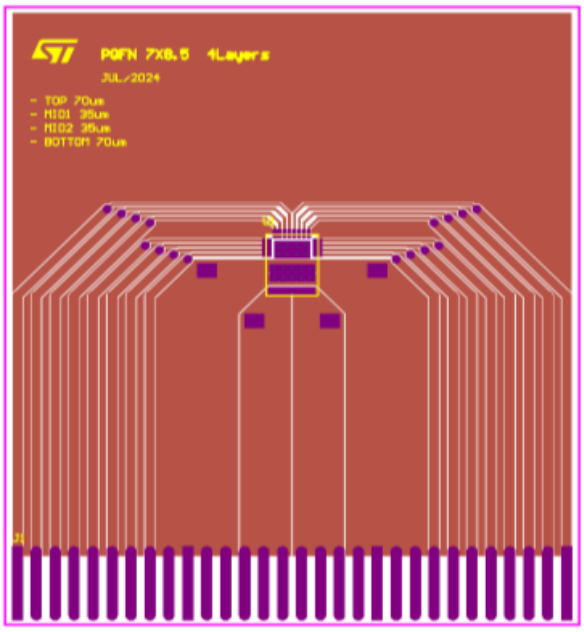
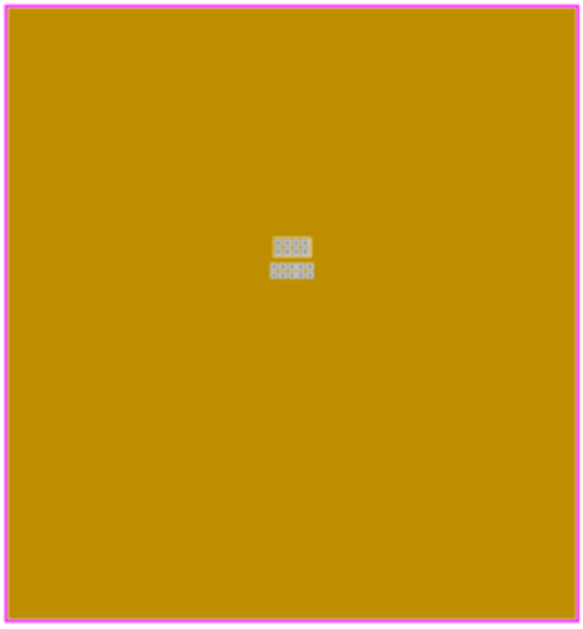


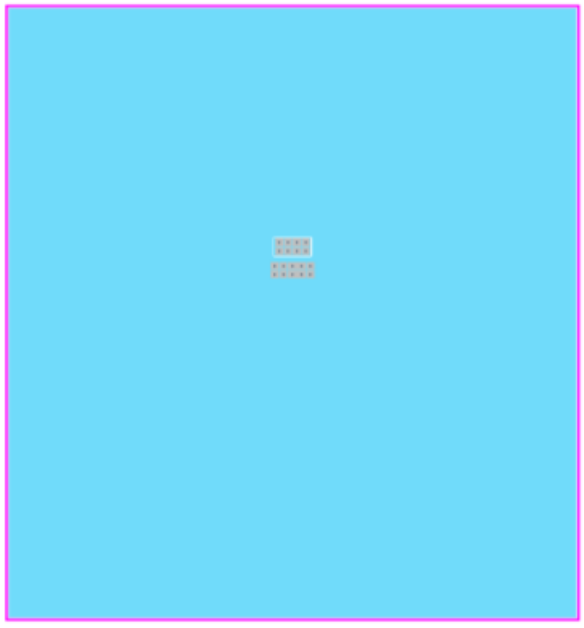
Figure 23. **PQFN (7x8.5 mm) PCB 4 layers**



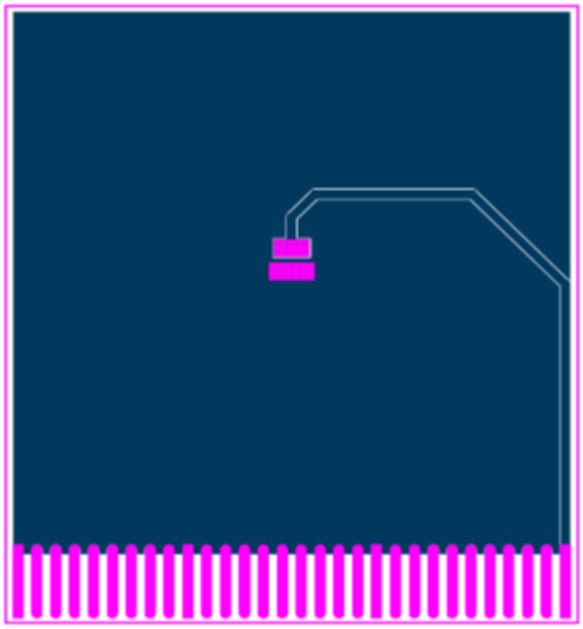
Cu coverage on top layer: 90%



Cu on mid1 layer: full coverage



Cu on mid2 layer: full coverage

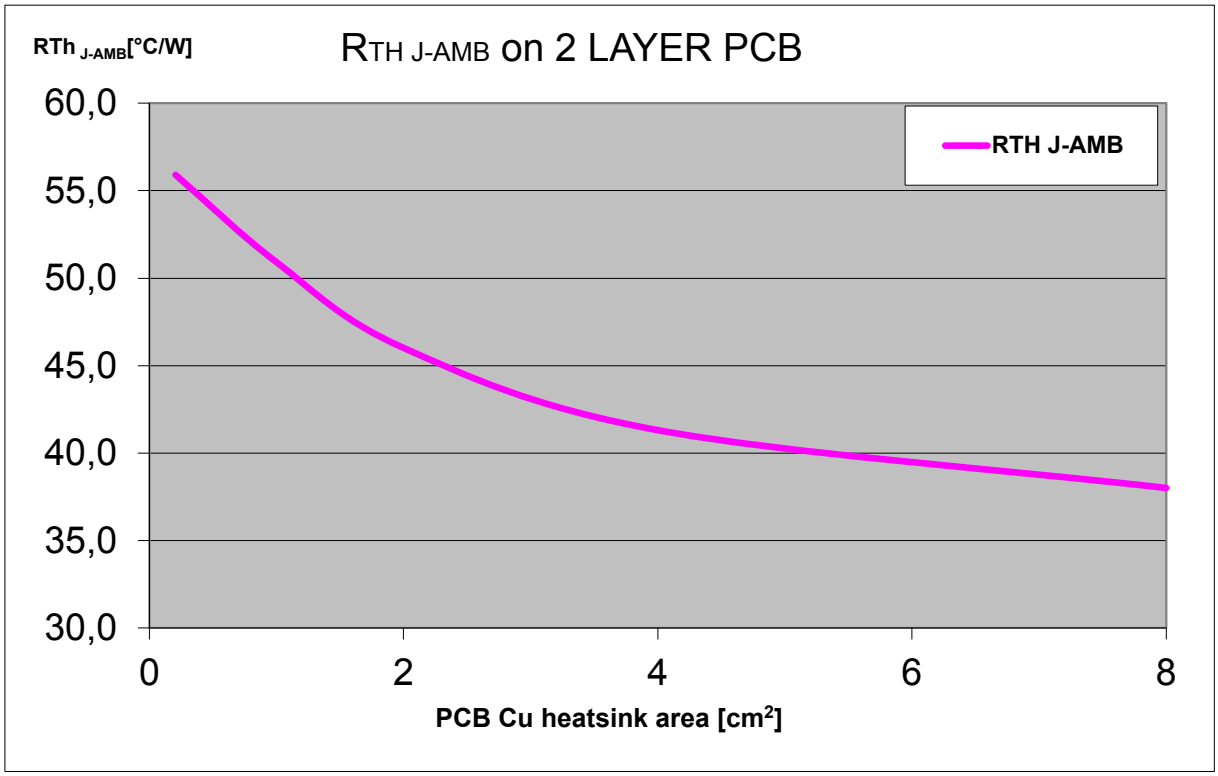


Cu coverage on bottom layer: 90%

Table 53. **PCB properties**

Dimension	Value
Board finish thickness	1.6 mm ±10%
Board dimension	77 mm x 86 mm
Board material	FR4
Cu thickness (top and bottom layers)	0.070 mm
Cu thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal vias diameter	0.3 mm ±0.08 mm
Cu thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm^2 or 8 cm^2

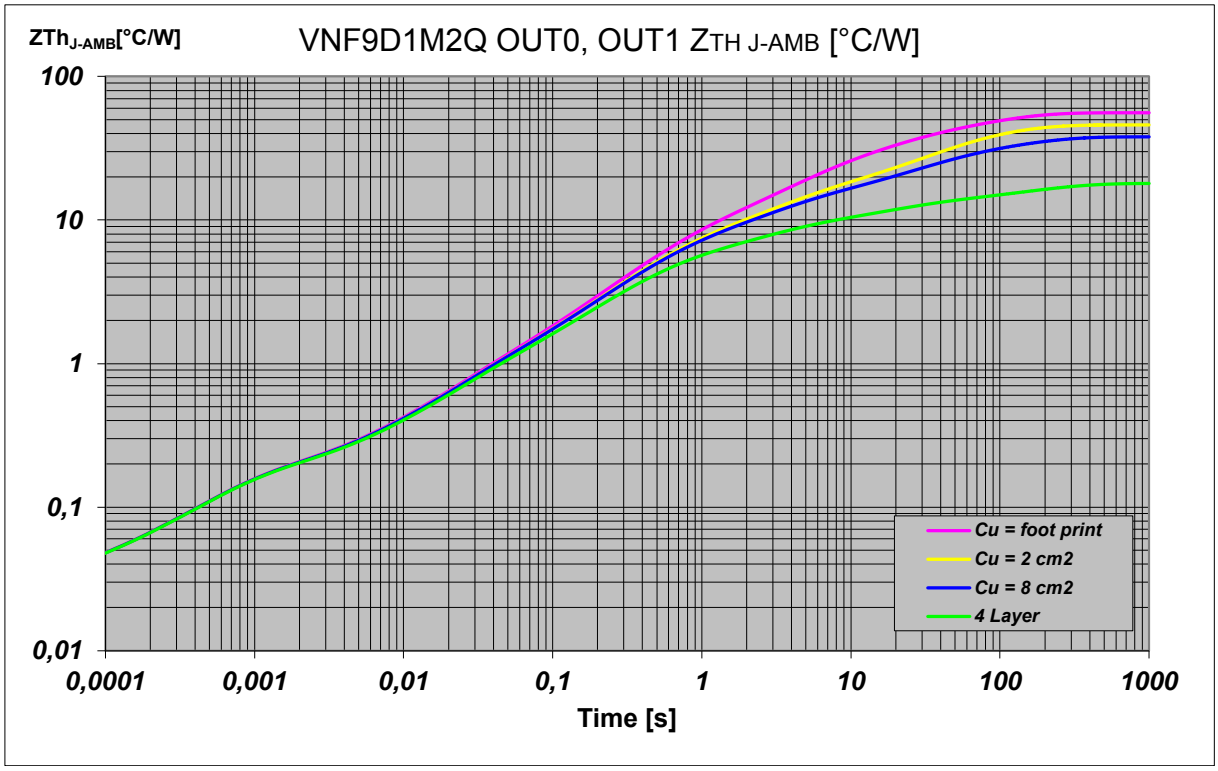
Figure 24. R_{thJA} **vs PCB copper area in open box free air conditions**



R_{thJA} on 4 layers PCB: 18 °C/W

R_{thJB} on 4 layers PCB: 4.37 °C/W

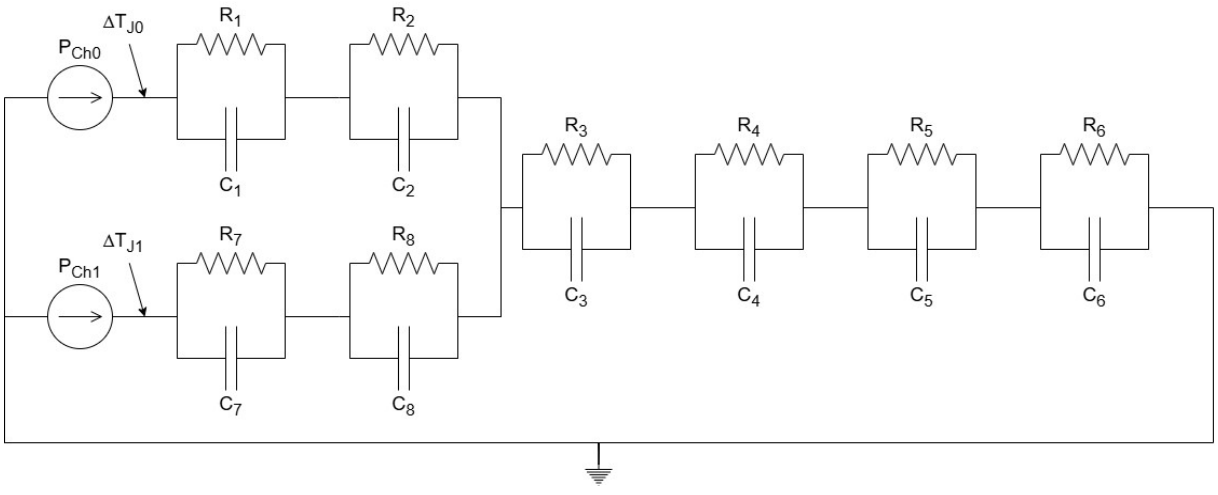
Figure 25. **PQFN (7x8.5 mm) thermal impedance junction ambient**



$Z_{th\delta} = R_{th} \cdot \delta + Z_{tht_p} (1 - \delta)$

where $\delta = t_P/T$

Figure 26. **Thermal fitting model**



Note: The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 54. **Thermal parameters**

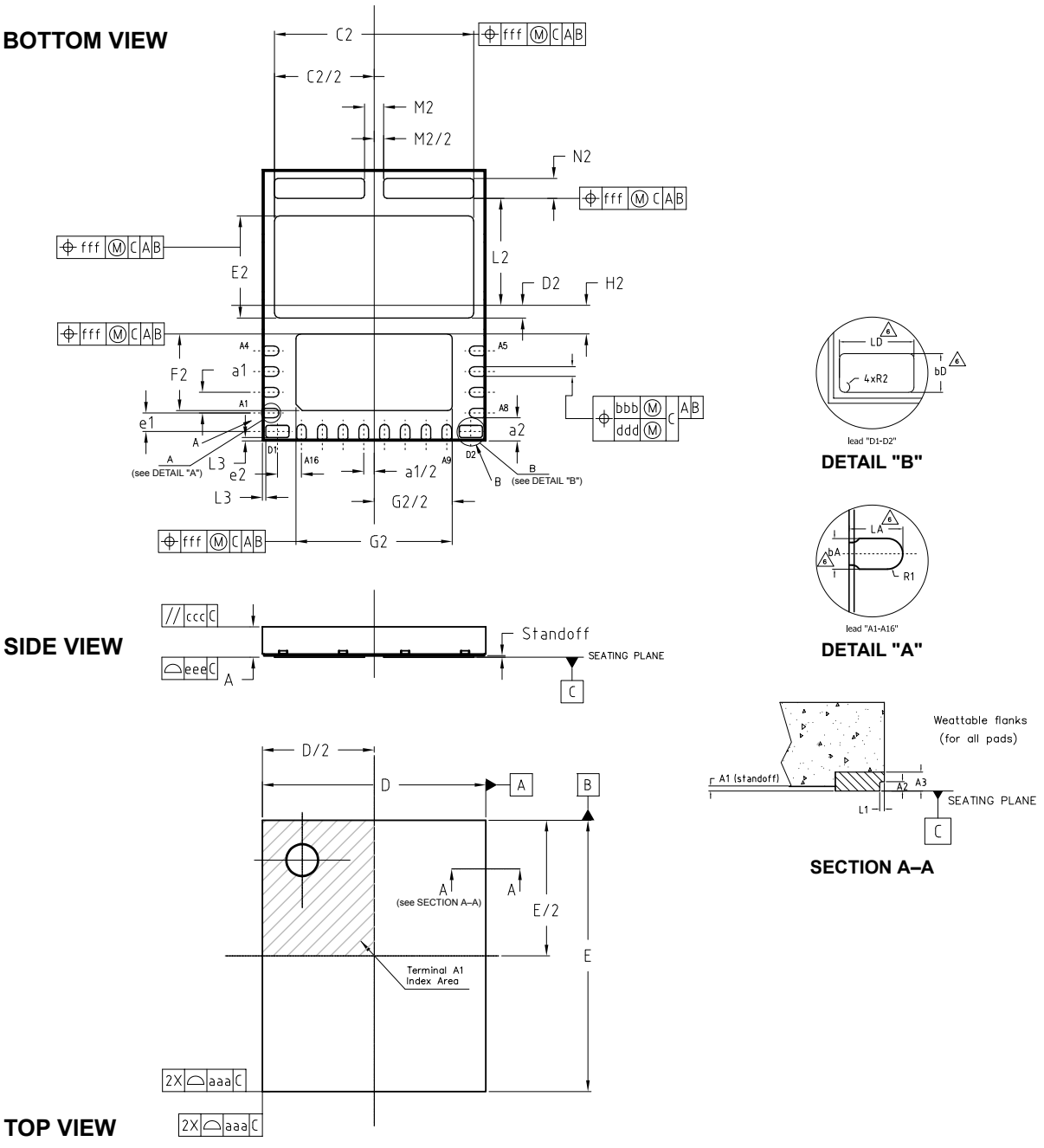
Thermal parameters	Area/island (cm²)			
	2 layers PCB			4 layers PCB
	FP	2	8	4L
R1 = R7 (°C/W)	0.15	0.15	0.15	0.15
R2 = R8 (°C/W)	0.4	0.4	0.4	0.4
R3 (°C/W)	5.35	4.75	4.55	3.75
R4 (°C/W)	11	8	7.2	4
R5 (°C/W)	16	15	12	4.2
R6 (°C/W)	23	17.7	13.7	5.5
C1 = C7 (W·s/°C)	4m	4m	4m	4m
C2 = C8 (W·s/°C)	60m	60m	60m	60m
C3 (W·s/°C)	0.1	0.1	0.1	0.1
C4 (W·s/°C)	0.4	0.4	0.4	0.6
C5 (W·s/°C)	1	2.4	2.4	4
C6 (W·s/°C)	3.5	5	9	30

11 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 PQFN 7x8.5 package information

Figure 27. PQFN 7x8.5 package outline



DM00824009_2

Table 55. **PQFN 7x8.5 mechanical data**

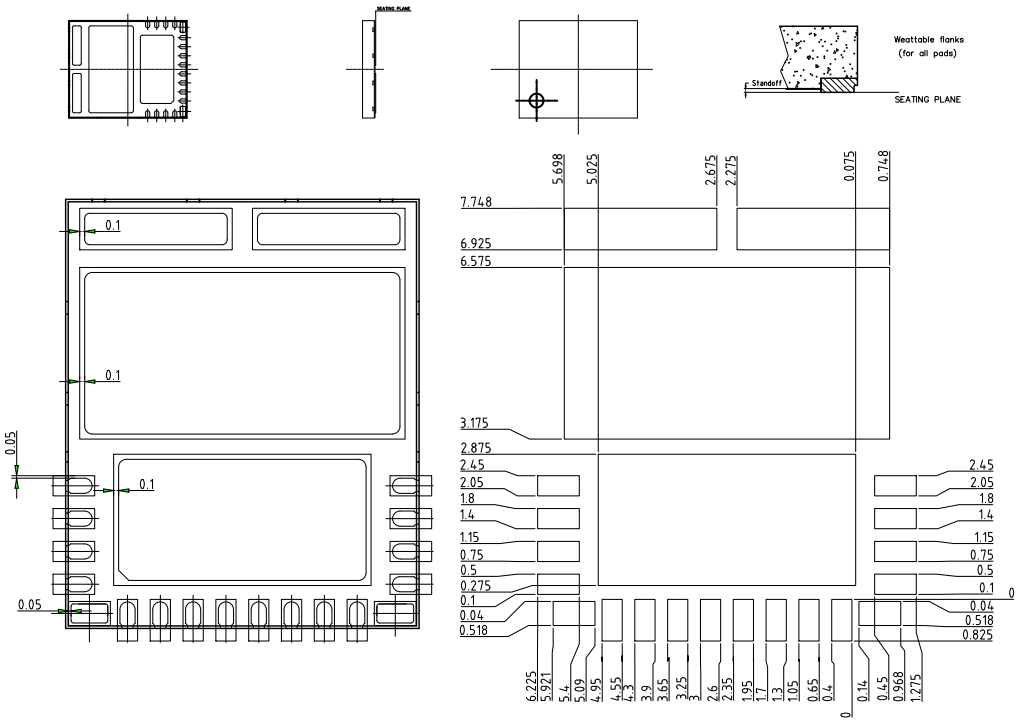
Symbol	Millimeters		
	Min.	Typ.	Max.
A	0.85	0.95	1.05
A1	0.00		0.05
A2	0.10		
A3		0.203 REF.	
bA1-16	0.25		0.35
bD1-2	0.328		0.428
C2	6.195		6.295
D2		0.40 BSC	
E2	3.15		3.25
F2	2.35		2.45
G2	4.85		4.95
H2		0.90 BSC	
L1	0.00		0.05
L2		3.35 BSC	
L3	0.058		0.158
M2		0.60 BSC	
N2	0.57		0.67
D		7.00 BSC	
E		8.50 BSC	
a1		0.65 BSC	
a2	0.675		0.775
e1		0.579 BSC	
e2		0.754 BSC	
LA1-16	0.475		0.575
LD1-2	0.678		0.778
L	0.475		0.575
R1		0.15	
R2	0.03		0.07

Table 56. **PQFN 7x8.5 tolerance of form and position**

Symbol	Millimeters
aaa	0.15
bbb	0.10
ccc	0.10
ddd	0.05
eee	0.08
fff	0.10

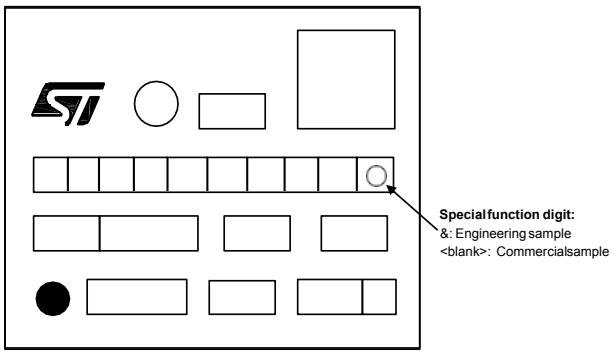
11.2 PQFN (7x8.5 mm) suggested footprint

Figure 28. **PQFN (7x8.5 mm) suggested footprint**



11.3 PQFN (7x8.5 mm) marking information

Figure 29. **PQFN (7x8.5 mm) marking information**



Parts marked as '&' are not yet qualified and therefore not approved for use in production. STMicroelectronics is not responsible for any consequences resulting from such use. In no event will STMicroelectronics be liable for the customer using any of these engineering samples in production. STMicroelectronics's quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

12 Ordering information

Table 57. **Order codes**

Order code	Package	Package marking	Packaging
VNF9D1M5QTR	PQFN 7X8.5	VFD12VH89	Tape and reel

Revision history

Table 58. **Document revision history**

Date	Revision	Changes
04-Dec-2023	1	Initial release.
17-Feb-2025	2	Updated Features and Description on cover page. Updated Table 24. ROM memory map, SOCR, OUTSRx, ITCNTSR, ADCISRx, ADCI2TSRx, ADCVSRx, ADCVBSR, and ADCVTSR. Updated Section 5.1.3: Registers, and Section 5.3.1: Status registers. Updated Table 36. DC characteristics, Table 38. Dynamic characteristics, Table 39. Digital timings, Table 40. Power section, Table 45. Protection, Table 46. ADC, Table 47. Protection and diagnostic ($7 < V_{CC} < 18$ V), Table 48. Digital current sense ($7 V < V_{CC} < 18$ V, T_J = -40 °C to 150 °C), Table 49. STi²Fuse digital current sense ($7 V < V_{CC} < 18$ V, T_J = -40 °C to 150 °C), and Table 50. Digital monitoring ($7 < V_{CC} < 18$ V). Added Section 8: Application schematic.
17-Nov-2025	3	Updated Section Cover image, Features, Description, Section 3.3, Section 3.4, ITCNTSR, ADCVTSR, Section 8, Section 9, Section 10; added Section 11.2 and Section 12. Updated Table 24, Table 34, Table 42, Table 44, Table 47.

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