VNF1248F

Datasheet

High-side switch controller with intelligent fuse protection for 12 V, 24 V and 48 V automotive applications

QFN32L 5X5 mm

Product status
VNF1248F

Product summary	
Order code	VNF1248FTR
Package	QFN32L
Packing	Tape and reel

Features

Maximum transient supply voltage	VS	70 V
Operating voltage range	VS	6 V to 60 V
Operating voltage range (extended)	VS	6 V to 70 V
Standby current (max.)	IS_Q	75 µA
SPI I/O supply voltage	VSPI	3 V to 5.5 V
SPI standby current (max.)	I_STBY	5 µA

- AEC-Q100 qualified
- General
  - High-side switch control IC with e-fuse protection for automotive 12 V, 24 V and 48 V applications
  - 32-bit ST-SPI interface compatible with 3.3 V and 5 V CMOS level
  - 2-stage charge pump
  - Gate drive for an external MOSFET in high-side configuration
  - High precision uni-directional current sense through an external high side shunt resistor
  - Input for a NTC resistor to monitor the external MOSFET temperature
  - Very low standby current
  - Device configuration lock out by a dedicated digital input pin
  - Integrated ADC for TJ, VNTC, VOUT, VSENSE conversion
  - Fast ADC for VDS, VSENSE conversion
  - CCM: capacitive charging mode
  - Few times programmable non-volatile memory (FTP NVM) embedded for customer sector program/erase/read
  - Direct input pin for hardware control of external MOSFET gate pin
  - Package QFN32L 5x5 package with wettable flanks
- Protections
  - Battery undervoltage shut-down
  - External MOSFET desaturation shutdown configurable via SPI
  - Hard short circuit latch-off configurable via SPI
  - Current vs time latch-off configurable via SPI (fuse-emulation)
  - Device overtemperature shutdown
  - External MOSFET overtemperature shutdown
  - Reverse battery
  - Loss of GND

Application

- Specially intended for Automotive power distribution applications
- Intelligent high current fuse replacement for automotive applications

Description

The device is an advanced controller for a Power MOSFET in high-side configuration, designed for the implementation of an intelligent high-side switch for 12 V, 24 V, and 48 V automotive applications. The control IC is interfaced to a host microcontroller through a 3.3 V and 5 V CMOS-compatible SPI interface and provides protection and diagnostics to the system.

1 Block diagram and pin description

Figure 1. Block diagram

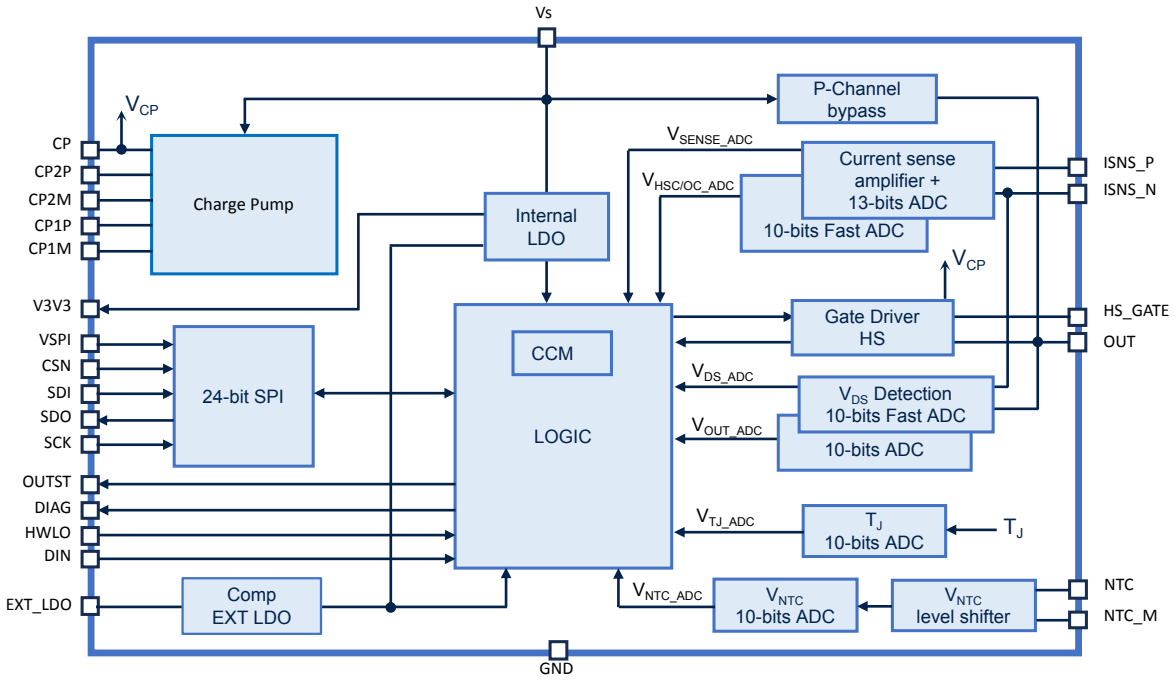
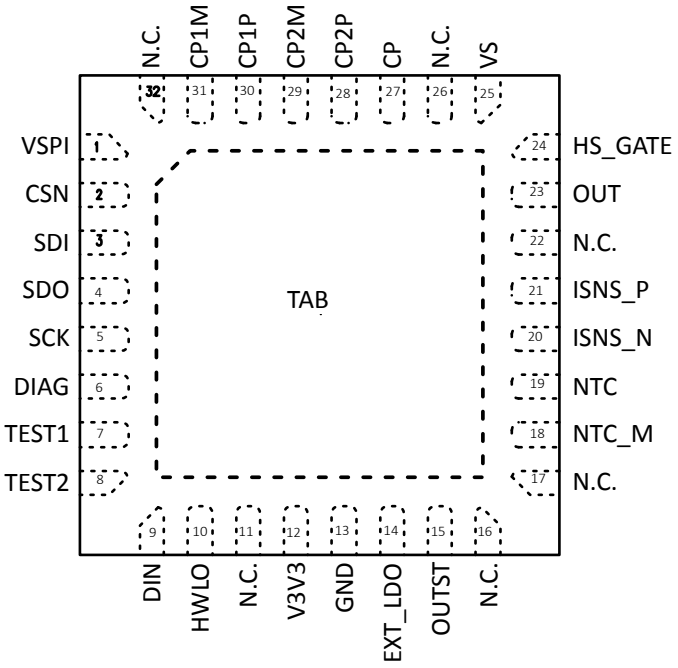


Figure 2. Configuration diagram (top through view)



Note: TAB connection must be to the ground. TAB is not intended as the device reference ground (a dedicated pin shall be used).

Table 1. Pin functions

Pin #	Name	Function
TAB		GND
1	VSPI	DC supply input for the SPI interface. 3.3 V and 5 V are compatible.
2	CSN	Chip select (active low) for SPI communication. It is the selection pin of the device. CMOS compatible input.
3	SDI	Serial data input for SPI communication. Data is transferred serially into the device and sampled on SCK rising edge.
4	SDO	Serial data output for SPI communication. Data is transferred serially out of the device on the SCK falling edge.
5	SCK	Serial clock for SPI communication. It is a CMOS compatible input.
6	DIAG	Open drain logic output. Diagnostic feedback. DIAG = '0' if ((SR1.FAILSAFE_ST='1' or (CR1.AUTO_ON_DIS='1') and BYPASS_SAT='1') or (GSB.DIAGS = '1') or (GSB.DE = '1') or "internal oscillator fault event" else '1'
7	TEST1	Test mode pin 1 - It must be connected to the ground through 1 kΩ resistor.
8	TEST2	Test mode pin 2 - It must be connected to the ground through 1 kΩ resistor.
9	DIN	Direct input to wake-up device from standby and to control directly gate turn-on/turn-off. If not used, must be connected to the ground through 1 kΩ resistor.
10	HWLO	Active high input pin compatible with 3.3 V and 5 V CMOS. If not used, must be connected to the ground through 1 kΩ resistor.
11, 16, 17, 22, 26, 32	N.C	Not connected.
12	V3V3	Output of the 3.3 V internal LDO voltage regulator (logic and I/O supply). Connect a low ESR capacitor (1 µF) close to this pin.
13	GND	Ground connection.
14	EXT_LDO	External V3V3 supply. If not used, must be connected to the ground through 1 kΩ resistor.
15	OUTST	Gate status monitor.
18	NTC_M	Negative input pin for external NTC resistor.
19	NTC	Positive input pin for external NTC resistor.
20	ISNS_N	Current sense amplifier negative input.
21	ISNS_P	Current sense amplifier positive input.
23	OUT	External FET source connection.
24	HS_GATE	Output of the gate driver for the external FET.
25	VS	Input supply pin. Connect to the 12 V, 24 V, 48 V battery voltage.
27	CP	Charge pump output.
28	CP2P	Charge pump–Positive terminal of the flying capacitor C_{P2}.
29	CP2M	Charge pump–Negative terminal of the flying capacitor C_{P2}.
30	CP1P	Charge pump–Positive terminal of the flying capacitor C_{P1}.
31	CP1M	Charge pump–Negative terminal of the flying capacitor C_{P1}.

2 Electrical specification

2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 2 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect device reliability.

Table 2. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 70	V
$-I_{GND}$	DC reverse ground pin current	200	mA
V_{SPI}	DC input voltage	-0.3 to 6.5	V
V_{3V3}	DC Output voltage	-0.3 to 4.6	V
V_{EXT_LDO}	External V3V3 supply	-0.3 to 4.6	V
V_{CSN}, V_{SDI}, V_{SCK}	SPI pins DC input voltage	-0.3 to 6.5	V
V_{SDO}	SPI pins DC output voltage	-0.3 to V_{SPI} + 0.3	V
V_{HWLO}	DC input voltage	-0.3 to 70	V
V_{DIAG}	DC output voltage	-0.3 to V3V3 + 0.3 < 4.6	V
I_{DIAG}	DC input current	Internally limited	mA
V_{ISNS_P}	DC input voltage	-15 to 70	V
V_{ISNS_N}			
ΔV_{ISNS}	Differential DC input voltage (V_{ISNS_P} - V_{ISNS_N})	< 3.3	V
V_{HS_GATE}	DC output voltage	-15 to V_{out} + 20	V
V_{OUT}	DC output voltage	-15 to V_S + 3	V
V_{NTC}	DC input voltage	-15 to I_{SNS_P} + 0.3	V
V_{NTC_M}	DC input voltage	-15 to I_{SNS_P} + 0.3	V
V_{CP}	DC input voltage	V_S - 0.3 to V_S + 20	V
V_{CP1P}	DC input voltage	V_S - 0.3 to V_S + 20	V
V_{CP2P}	DC input voltage	V_S - 0.6 to V_S + 20	V
V_{CP1M}, V_{CP2M}	DC input voltage	-0.3 to V_S + 0.3	V
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F)	2000	V
		4000(1)	
	Charge device model (CDM-AEC-Q100-011)	±500(2)	
		±750(3)	
OUTST	Open drain active high. Gate status monitor.	-0.3 to V3V3 + 0.3 < 4.6	V
DIN	Direct input	-0.3 to 70	V
T_J	Junction operating temperature	-40 to 150	°C

Symbol	Parameter	Value	Unit
T_{stg}	Storage temperature	-55 to 150	°C
N_{FTP}	Maximum number of few time programmable non-volatile memory (FTP NVM) programming cycles	1000	

1. *Only for pin: VS, OUT, DIN.*
2. *All pins except corners.*
3. *Corner pins.*

2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Typ. value	Unit
R_{thJA}	Thermal resistance, junction-to-ambient (JEDEC JESD 51-2, -7)(1)	56	°C/W
	Thermal resistance, junction-to-ambient (JEDEC JESD 51-2, -5)(2)	26	

1. *Device mounted on two-layer 2s0p PCB with 2 cm² heatsink copper trace.*
2. *Device mounted on four-layer 2s2p PCB.*

Note: Board finish thickness 1.6 mm ±10%; Board double layer and four layers; board dimension 129x60; board material FR4; Cu thickness 0.070 mm (outer layers), Cu thickness 0.035 mm (inner layers); Thermal vias separation 1.2 mm, Thermal vias diameter 0.3 mm ±0.08 mm, Cu thickness on vias 0.025 mm; footprint dimension 3.5 mm x 3.5 mm.

2.3 Main electrical characteristics

6 V < V_S < 60 V; -40 °C < T_J < 150 °C, unless otherwise specified.

All typical values refer to V_S = 48 V; T_J = 25 °C, unless otherwise specified.

Table 4. Supply specification

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_S	Operating supply voltage		6	48	60	V
V_{S_EXT}	Extended operating supply voltage	100 ms max. duration	6	-	70	V
$V_{EXT\_LDO\_L}$	Low level voltage EXT_LDO		2.6	2.8	3	V
$V_{EXT\_LDO\_H}$	High level voltage EXT_LDO		2.8	3	3.2	V
$I_{EXT\_LDO\_H}$	Current consumption from EXT_LDO in supplier mode	V_{EXT_LDO} > $V_{EXT\_LDO\_H}$	3.5	5	6	mA
$I_{EXT\_LDO\_L}$	Current consumption from EXT_LDO	V_{EXT_LDO} < $V_{EXT\_LDO\_L}$	6	10	16	µA
V_{S_USD1}	Undervoltage shutdown(1)		3.8	4	4.2	V
V_{S_USD2}			12	13	14	
V_{S_USD3}			22	24	25	
$V_{S\_USD\_RES1}$	Undervoltage shutdown reset		4.3	4.5	4.8	V
$V_{S\_USD\_RES2}$			13	14	15	
$V_{S\_USD\_RES3}$			24	27	29	
$V_{S\_USD\_HYS1}$	Undervoltage shutdown hysteresis		-	0.5	-	V
$V_{S\_USD\_HYS2}$	Undervoltage shutdown hysteresis		-	1	-	V
$V_{S\_USD\_HYS3}$	Undervoltage shutdown hysteresis		-	3	-	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{VS_USD}	Undervoltage shutdown filtering time.		-	33	-	µs
VSPI_UV	Undervoltage shutdown on VSPI		1.5	1.6	1.8	V
VSPI_UV_RESET	Undervoltage shutdown reset on VSPI		2	2.1	2.2	V
I_{SPI}	SPI supply current during frame communication		-	-	3	mA
I_{SPI_STBY}	SPI supply current in standby state		-	-	5	µA
$I_{S(ON)}$	Supply current on VS pin (includes logic)	f_{PWM} = 1 Hz, $V_{EXT\_LDO} < V_{EXT\_LDO\_L}$ V_S = 13 V, OUT = V_S Gate ON, R_{GATE} = 47 kΩ	-	8.6	-	mA
		f_{PWM} = 1 Hz, $V_{EXT\_LDO} < V_{EXT\_LDO\_L}$ V_S = 48 V, OUT = V_S Gate ON, R_{GATE} = 47 kΩ	-	7.9	-	mA
		f_{PWM} = 1 Hz, $V_{EXT\_LDO} < V_{EXT\_LDO\_L}$ V_S = 48 V, OUT = V_S (2)	4.5	7.2	8.5	mA
		f_{PWM} = 1 Hz, $V_{EXT\_LDO} > V_{EXT\_LDO\_H}$, V_S = 13 V, OUT = V_S Gate ON, R_{GATE} = 47 kΩ	-	4	-	mA
		f_{PWM} = 1 Hz, $V_{EXT\_LDO} > V_{EXT\_LDO\_H}$, V_S = 48 V, OUT = V_S Gate ON, R_{GATE} = 47 kΩ	-	3.1	-	mA
I_{OUT_STDBY}	Output current standby mode	V_S = 13 V, standby mode, OUT = GND	1.5	3	5	µA
		V_S = 48 V, standby mode, OUT = GND	1	3	5	µA
I_{OUT_ON}	Output current unlocked mode	V_S = 13 V, unlocked mode, OUT=GND	140	185	230	µA
		V_S = 48 V, unlocked mode, OUT = GND	210	250	320	µA
I_{S_Q}	V_S quiescent current (includes logic)– independently from bypass switch condition	V_S = 48 V, T_J = 25 °C, OUT = V_S	45	60	70	µA
		V_S = 48 V, T_J = 25 °C, OUT = GND	50	60	75	µA
		V_S = 13 V, T_J = 25 °C, OUT = V_S	30	48	57	µA
$V_{S\_POR\_ON}$	Power-on reset the threshold. The device leaves the reset mode		2.4	2.5	2.65	V
$V_{S\_POR\_OFF}$	Power-on shutdown threshold. Device enters reset mode		2.2	2.3	2.45	V
$V_{S\_POR\_HYST}$	Power-on reset hysteresis		-	0.2	-	V
t_{PWON}	Time from power-on to standby	$V_S > V_{S\_POR\_ON}$,	-	-	500	µs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
		V3V3 external capacitor 1 µF				

1. See *Table 51. CR#3: control register 3 (read/write); address 03h.*
2. *Measured in test mode with the charge pump off.*

Table 5. SPI logic inputs (CSN, SCK, and SDI) specification

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low level input current (SCK and SDI)	V_{IL} = 1.5 V	1.7	-	4	µA
	Low level input current (CSN)		-2.9	-	-2	µA
I_{IH}	High level input current (SCK and SDI)	V_{IH} = 2.1 V	-13	-	-3	µA
	High level input current (CSN)		-18	-	-10	µA
V_{IL}	Low level input voltage		-	-	1.5	V
V_{IH}	High level input voltage		2.1	-	-	V
V_{I_HYST}	Input hysteresis voltage		-	0.4	-	V

Table 6. SPI logic output (SDO) specification

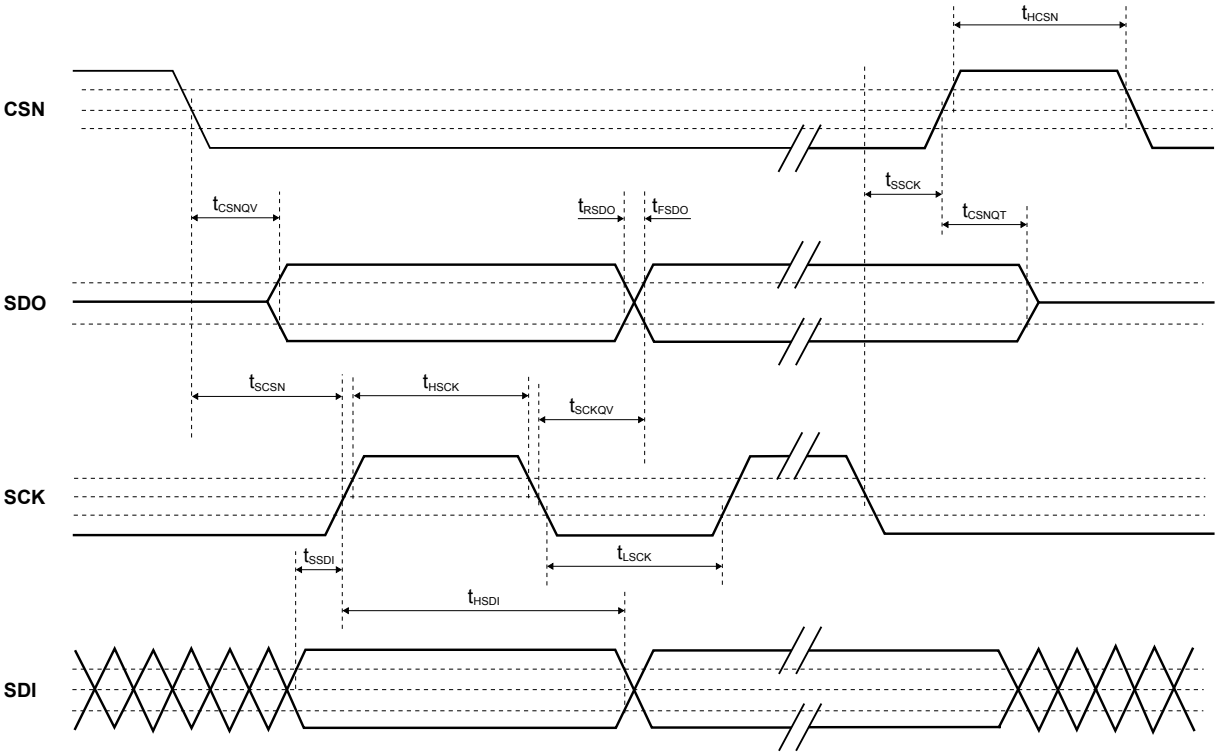
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Low level output voltage		-	-	0.3 * V_{SPI}	V
V_{OH}	High level output voltage		0.7 * V_{SPI}	-	-	V
ISDO_Ilow	Low level output current	VSDO = 1 V, VSPI = 5 V	45	-	96	mA
ISDO_Ihigh	High level output current	VSDO = 4 V, VSPI = 5 V	15	-	32	mA
I_{LO}	Output leakage current		-1	-	1	µA

Table 7. SPI timing specification

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
f_{SCK}	SPI clock frequency			-	-	8	MHz
t_{HSCK}	SCK high time			55	-	-	ns
t_{LSCK}	SCK low time			55	-	-	ns
t_{HCSN}	CSN high time			1	-	-	µs
t_{SCSN}	CSN setup time–CSN low before SCK rising edge			100	-	-	ns
t_{SSCK}	SCK setup time–SCK low before CSN rising edge			100	-	-	ns
t_{SSDI}	SDI setup time before SCK rising edge			25	-	-	ns
t_{HSDI}	SDI hold time			20	-	-	ns
t_{CSNQV}	CSN falling edge until SDO valid			-	-	70	ns
t_{CSNQT}	CSN rising edge until SDO tristate			-	220	-	ns
t_{SCKQV}	SCK falling edge until SDO valid			-	-	50	ns
t_{RSDO}	SDO rise time			-	-	25	ns
t_{FSDO}	SDO fall time			-	-	25	ns
t_{WHCH}	CSN low timeout			-10%	50	+10%	ms
t_{WDTB}	Watchdog toggle bit timeout	WD_TIME configuration:	00	-10%	50	+10%	ms
			01		100		

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
t_{WDTB}	Watchdog toggle bit timeout	WD_TIME configuration:	10	-10%	150	+10%	ms
			11		200		
t_{STBY_OUT}	Minimum time during which CSN must be toggled low to the wake-up device from standby state	Device in standby state		2	4	6	µs

Figure 3. SPI specification: timing waveforms



t_{HCSN} : CSN high time
t_{CSNQV} : CSN falling until SDO valid
t_{RSDO} : SDO fall time
t_{FSDO} : SDO rise time
t_{SSCK} : SCK setup time before CSN rising
t_{CSNQT} : CSN rising until SDO tristate
t_{SCSN} : CSN setup time before SCK rising
t_{HSCK} : SCK high time
t_{SCKQV} : SCK falling until SDO valid
t_{SSDI} : SDI setup time before SCK rising
t_{HSDI} : SDI hold time
t_{LSCK} : SCK low time

Table 8. HWLO logic input pin specification

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low level input current	V_{IL} = 1.5 V	0.5	-	2.5	µA
I_{IH}	High level input current	V_{IH} = 2.1 V	1.6	-	3.5	µA
V_{IL}	Low level input voltage		-	-	1.5	V
V_{IH}	High level input voltage		2.1	-	-	V
V_{I_HYST}	Input hysteresis voltage		-	0.4	-	V
t_{HWLO}	HWLO filtering time		-10%	33	10%	µs

Table 9. DIAG logic output pin specification

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DIAG_PD}	DIAG pin open-drain pull-down voltage	I_{DIAG_PD} = 1 mA	-	-	0.2	V
I_{DIAG_PD}	DIAG pin open-drain input current	$V_{DIAG} = V_{DIAG\_PD}$	-	-	1	mA
I_{DIAG_LKG}	DIAG pin open-drain leakage current	$V_{DIAG} = V_{V3V3}$ = 4.6 V	0	-	1	µA

Table 10. Device thermal shutdown

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
T_{TSD}	Junction temperature thermal shutdown threshold		160	175	190	°C
T_{TSD_HYS}	Junction temperature thermal shutdown hysteresis		-	15	-	°C
$T_{J\_ADC\_CONV}$	Junction temperature ADC full-scale range resolution (1)		0	-	1023	-
$T_{J\_ADC\_RATE}$	Junction temperature ADC sample rate		-	10	-	kSample/s

1. T_{J_ADC} (°C) = T_{J_ADC} [9:0]/3 - 72

Table 11. DIN logic input pin specification

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{IL}	Low level input current	V_{IL} = 1.5	1.5	-	5	µA
I_{IH}	High level input current	V_{IH} = 2.1	-12	-	-2	µA
V_{IL}	Low level input voltage		1.48	1.59	1.73	V
V_{IH}	High level input voltage		2.01	2.05	2.10	V
V_{I_HYST}	Input hysteresis voltage		-	0.4	-	V
t_{DIN_WAKEUP}	Filtering time on DIN rise edge for device wakeup		-	4	-	µs
$t_{DIN\_DEGLITCH}$	De-glitch filtering time on DIN rise/fall edges		-	1	-	µs
$t_{DIN\_RISE\_FILTER}$	Filtering time on DIN rise edge for DIN direct control of external FET in fail-safe state		-	10	-	µs
$t_{DIN\_TOGGLE\_TOUT}$	DIN toggling timeout		-	20	-	µs

Table 12. OUTST logic output pin specification

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OUTST_PU}	OUTST pin open-drain pull-up voltage	I_{OUTST_PU} = 1 mA	3.15	-	-	V
I_{OUTST_PU}	OUTST pin open-drain output current		-	-	1	mA
I_{OUTST_LKG}		V_{OUTST} = 4.6 V	0	-	16	µA

Table 13. Charge pump specification

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CP_6V}	Charge pump output voltage	V_S = 6 V	V_S + 7	V_S + 11	-	V
V_{CP_10V}	Charge pump output voltage	V_S > 10 V	V_S + 13.5	V_S + 14.5	V_S + 15.5	V
$V_{CP\_LOW\_H}$	Charge pump output under voltage high threshold	Ramp up on V_{CP}	V_S + 5.5	V_S + 6	V_S + 6.5	V
$V_{CP\_LOW\_L}$	Charge pump output undervoltage low threshold	Ramp down on V_{CP}	V_S + 5.1	V_S + 5.6	V_S + 6.2	V
$V_{CP\_LOW\_hyst}$	Charge pump output undervoltage hysteresis		-	0.4	-	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f_{CP}	Charge pump frequency		-5%	400	+5%	kHz
t_{CP_RISE}	Charge pump low (CP_LOW diagnostic) rising edge filtering time		-5%	60	5%	µs
t_{CP_FALL}	Charge pump low (CP_LOW diagnostic) falling edge filtering time		-10%	2.3	10%	µs

Table 14. External FET gate driver specification

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{GSON_6V}	Gate-on voltage	V_S = 6 V, I_G = 50 µA	6	-	-	V
V_{GSON_10V}	Gate-on voltage	V_S > 10 V, I_G = 50 µA	11.5	-	15	V
V_{GSOFF}	Gate-off voltage		-	-	0.5	V
V_{GSMAX}	Maximum gate voltage (internally limited)		-	-	20	V
t_{ON}	Gate turn-on	V_{GS} = 0.5 V to V_{GS} = 10 V, C_{GATE} = 80 nF	-	-	3	µs
t_{OFF}	Gate turn-off	Full V_{GS} to V_{GS} < 0.5, C_{GATE} = 80 nF	-	-	10	µs
$V_{GS\_UVLO\_6V}$	Gate undervoltage lockout	V_S = 6 V	3.5	-		V
$V_{GS\_UVLO\_10V}$	Gate undervoltage lockout	V_S > 10 V, C_{GATE_max} = 30 nF	7	-	-	V
$V_{G\_UVLO\_BLK}$	Gate undervoltage lockout blanking	Enable at charge pump startup if external FET turn-on is required, and applied after CP_LOW expiration (falling edge)	-5%	100	5%	µs
$V_{G\_UVLO\_DEGLITCH}$	Gate undervoltage lockout de-glitch filtering time		-15%	8	15%	µs

Table 15. Current sense amplifier

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SENSE_CM}	Common-mode input voltage range		CS_UV	-	VS	V
V_{SENSE_FSR}	Differential input voltage full-scale range		0	-	160	mV
I_{SNS_P}	CSA positive input current	V_S = 12 V	1.1	1.3	1.5	mA
I_{SNS_N}	CSA negative input current	I_{sense_P} = 12 V I_{sense_N} = 11.9 V Gate ON	100	200	300	µA

Table 16. Integrated VSENSE 13-bit ADC

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SENSE\_ADC\_CONV}$	Current sense ADC full-scale range resolution	V_{SENSE_ADC}[12:0] = min((V_{SENSE}/160 * 8192), 8191)	0	-	8191	-
$V_{SENSE\_REFRESH}$	Current sense ADC sample rate		-	2.4	-	kSample/s
$V_{SENSE\_ACC\_6mV}$	Digital current sense accuracy	6 mV < V_{SENSE_DIFF} < 10 mV	-10	-	+10	%
$V_{SENSE\_ACC\_10mV}$		10 mV < V_{SENSE_DIFF} < 20 mV	-5	-	+5	%
$V_{SENSE\_ACC\_20mV}$		V_{SENSE_DIFF} > 20 mV	-3	-	+3	%
$V_{SENSE\_ACC\_3mV}$		3 mV < V_{SENSE_DIFF} < 6 mV	-17	-	+17	%
$V_{SENSE\_ACC\_1.8mV}$		1.8 mV < V_{SENSE_DIFF} < 3 mV	-0.5	-	+0.5	mV

Note: The accuracies showed in the Table 16 are referred to the sigma delta converter at 13-bit, while the hard short and overcurrent protections are related to the 10-bit SAR converter as reported in the Table 18.

Table 17. External FET VDS protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DS\_THRS\_RANGE}$	V_{DS} monitor threshold range 31 steps programmable through SPI		300	-	1800	mV
$V_{DS\_THRS\_STEP}$	V_{DS} monitor threshold step		-	50	-	mV
$V_{DS\_THRS\_0}$	V_{DS} monitor thresholds		-	300	-	mV
$V_{DS\_THRS\_1}$			-	350	-	
$V_{DS\_THRS\_2}$			-	400	-	
$V_{DS\_THRS\_3}$			-	450	-	
$V_{DS\_THRS\_4}$			-	500	-	
$V_{DS\_THRS\_5}$			-	550	-	
$V_{DS\_THRS\_6}$			-	600	-	
$V_{DS\_THRS\_7}$			-	650	-	
$V_{DS\_THRS\_8}$			-	700	-	
$V_{DS\_THRS\_9}$			-	750	-	
$V_{DS\_THRS\_10}$			-	800	-	
$V_{DS\_THRS\_11}$			-	850	-	
$V_{DS\_THRS\_12}$			-	900	-	
$V_{DS\_THRS\_13}$			-	950	-	
$V_{DS\_THRS\_14}$			-	1000	-	
$V_{DS\_THRS\_15}$			-	1050	-	
$V_{DS\_THRS\_16}$			-	1100	-	
$V_{DS\_THRS\_17}$			-	1150	-	
$V_{DS\_THRS\_18}$			-	1200	-	
$V_{DS\_THRS\_19}$			-	1250	-	
$V_{DS\_THRS\_20}$			-	1300	-	
$V_{DS\_THRS\_21}$			-	1350	-	
$V_{DS\_THRS\_22}$			-	1400	-	
$V_{DS\_THRS\_23}$			-	1450	-	
$V_{DS\_THRS\_24}$			-	1500	-	
$V_{DS\_THRS\_25}$			-	1550	-	
$V_{DS\_THRS\_26}$			-	1600	-	
$V_{DS\_THRS\_27}$			-	1650	-	
$V_{DS\_THRS\_28}$			-	1700	-	
$V_{DS\_THRS\_29}$			-	1750	-	
$V_{DS\_THRS\_30}$			-	1800	-	
$V_{DS\_THRS\_ACC}$	V_{DS} monitor threshold accuracy		-5	-	5	%

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DS\_DEGLITCH}$	V_{DS} monitor shut-off deglitch time		-20%	5	+20%	µs
V_{DS_DELAY}	V_{DS} monitor shut-off delay time	C_{GATE} = 30 nF, T = 105 °C	-	-	5	µs
V_{DS_BLK}	V_{DS} monitor shut-off blanking time	At high-side external FET startup	-10%	960	+10%	µs
$V_{DS\_ADC\_CONV\_RES}$	VDS monitor ADC full-scale range solution (1)		0	-	1023	Bit
$V_{DS\_ADC\_CONV}$	V_{DS} monitor ADC full-scale voltage range		-0.05	-	1.87	V
$V_{DS\_ADC\_RATE}$	V_{DS} monitor ADC sample rate		-	0.9	-	MSample/s

1. *V_{DS} (V) = V_{DS_ADC} [9:0] * 2.4 /1280 - 0.05*

Table 18. Hard short circuit protection with integrated 10-bit ADC

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{HSC\_THRS\_RANGE}$	Hard short circuit protection threshold range 16 steps programmable via SPI		20	-	160	mV
$V_{HSC\_THRS\_0}$	Hard short circuit protection thresholds		-	20	-	mV
$V_{HSC\_THRS\_1}$			-	23	-	
$V_{HSC\_THRS\_2}$			-	26.4	-	
$V_{HSC\_THRS\_3}$			-	30.3	-	
$V_{HSC\_THRS\_4}$			-	34.8	-	
$V_{HSC\_THRS\_5}$			-	40	-	
$V_{HSC\_THRS\_6}$			-	45.9	-	
$V_{HSC\_THRS\_7}$			-	52.8	-	
$V_{HSC\_THRS\_8}$			-	60.6	-	
$V_{HSC\_THRS\_9}$			-	69.6	-	
$V_{HSC\_THRS\_10}$			-	80	-	
$V_{HSC\_THRS\_11}$			-	91.9	-	
$V_{HSC\_THRS\_12}$			-	105.6	-	
$V_{HSC\_THRS\_13}$			-	121.3	-	
$V_{HSC\_THRS\_14}$			-	139.3	-	
$V_{HSC\_THRS\_15}$			-	160	-	
$V_{HSC\_THRS\_ACC}$	Hard short circuit protection threshold accuracy		-5	-	5	%
V_{HSC_DELAY}	Hard short circuit protection delay time	C_{GATE} = 30 nF, T = 105 °C	-	-	5	µs
$V_{HSC\_ADC\_CONV}$	Hard short circuit protection ADC full range resolution(1)		0	-	1023	-
$V_{HSC\_ADC\_RATE}$	Hard short circuit ADC sample rate		-	0.9	-	MSample/s

1. *V_{SENSE} (mV) = V_{SENSE_ADC} [9:0] * 160 / 1024.*

Table 19. Overcurrent protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OC\_THRS\_RANGE}$	Overcurrent protection first threshold range 32 steps programmable via SPI		6	-	90	mV
$V_{OC\_THRS\_0}$	Overcurrent protection thresholds		-12%	6	+12%	mV
$V_{OC\_THRS\_1}$				7.2		
$V_{OC\_THRS\_2}$				8.7		
$V_{OC\_THRS\_3}$			-7%	10.4	7%	
$V_{OC\_THRS\_4}$				11.8		
$V_{OC\_THRS\_5}$				13		
$V_{OC\_THRS\_6}$				13.8		
$V_{OC\_THRS\_7}$				14.8		
$V_{OC\_THRS\_8}$				15.8		
$V_{OC\_THRS\_9}$				16.8		
$V_{OC\_THRS\_10}$				17.9		
$V_{OC\_THRS\_11}$				19.1		
$V_{OC\_THRS\_12}$				20.4		
$V_{OC\_THRS\_13}$			-5%	21.8	5%	
$V_{OC\_THRS\_14}$				23.3		
$V_{OC\_THRS\_15}$				24.8		
$V_{OC\_THRS\_16}$				26.5		
$V_{OC\_THRS\_17}$				28.2		
$V_{OC\_THRS\_18}$				30.1		
$V_{OC\_THRS\_19}$				32.2		
$V_{OC\_THRS\_20}$				34.3		
$V_{OC\_THRS\_21}$				36.6		
$V_{OC\_THRS\_22}$				39.1		
$V_{OC\_THRS\_23}$				41.7		
$V_{OC\_THRS\_24}$				44.5		
$V_{OC\_THRS\_25}$				47.5		
$V_{OC\_THRS\_26}$				50.6		
$V_{OC\_THRS\_27}$				54		
$V_{OC\_THRS\_28}$				61.3		
$V_{OC\_THRS\_29}$				69.5		
$V_{OC\_THRS\_30}$				78.8		
$V_{OC\_THRS\_31}$				89.3		
i-time_tol_t	I-t tolerance on time step (y axis)		(t-10%) - 32	-	(t+10%) + 32	µs
$t_{I\_SAMPLING}$	I^2t algorithm sampling time		-10%	61	10%	µs

Note: Overcurrent protection is based on the same 10-bit ADC used for hard short protection.

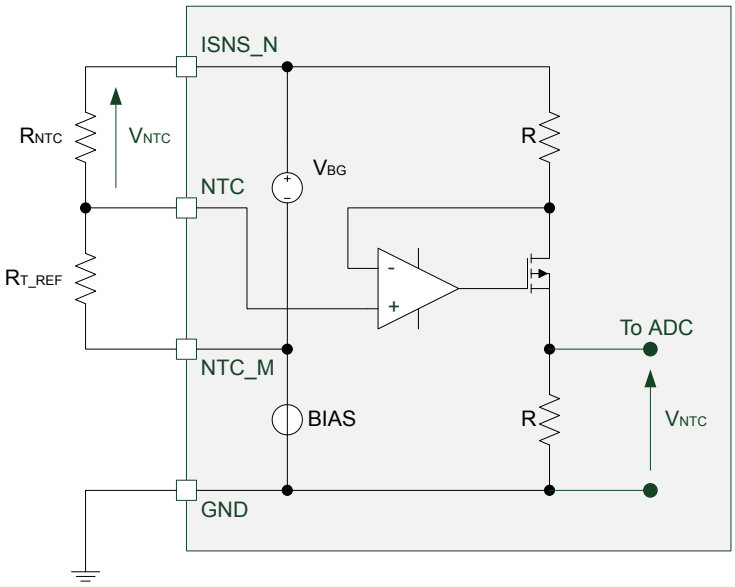
Table 20. External FET thermal shutdown via NTC input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{NTC_FSR}	NTC input voltage full-scale range		VSENSE_N - 1.2	-	VSENSE_N	V
V_{NTC_M}	NTC_M output voltage		-	VSENSE_N - 1.2	-	V
V_{NTC_ACC}	NTC input voltage threshold accuracy		-5	-	5	mV
$V_{NTC\_THRS\_0}$	External FET thermal shutdown NTC input voltage thresholds		-	110.92	-	mV
$V_{NTC\_THRS\_1}$			-	98.76	-	
$V_{NTC\_THRS\_2}$			-	88.07	-	
$V_{NTC\_THRS\_3}$			-	78.66	-	
$V_{NTC\_THRS\_4}$			-	70.38	-	
$V_{NTC\_THRS\_5}$			-	63.08	-	
$V_{NTC\_THRS\_6}$			-	56.64	-	
$V_{NTC\_THRS\_7}$			-	50.95	-	
$V_{NTC\_THRS\_8}$			-	45.92	-	
$V_{NTC\_THRS\_9}$			-	41.46	-	
$V_{NTC\_THRS\_10}$			-	37.50	-	
$V_{NTC\_THRS\_11}$			-	37.50	-	
$V_{NTC\_THRS\_12}$			-	37.50	-	
$V_{NTC\_THRS\_13}$			-	37.50	-	
$V_{NTC\_THRS\_14}$			-	37.50	-	
$V_{NTC\_THRS\_15}$			-	37.50	-	
$V_{NTC\_DEGLITCH}$	External FET thermal shutdown deglitch time		10	-	500	µs
$V_{NTC\_ADC\_CONV}$	External FET thermal shutdown ADC full range resolution(1)		0	-	1023	
$V_{NTC\_ADC\_RATE}$	External FET thermal shutdown ADC sample rate		-	4.9	-	kSample/s

1. V_{NTC} (V) = V_{NTC_ADC} [9:0] * 1.2 / 1024

   $R_{NTC}(\Omega) = V_{NTC} * R_{T\_REF} / (V_{BG} - V_{NTC})$.

Figure 4. **NTC bridge**



Note:

- V_{NTC} *(V) =* V_{NTC_ADC} *[9:0] * 1.2 / 1024*
- R_{NTC}*(Ω) =* $V_{NTC} * R_{T\_REF} / (V_{BG} - V_{NTC})$.
- R_{NTC} *= B57232V5103F360 (10 kΩ at 25 °C)*
- R_{T_REF} *= 10 kΩ ±1%*
- V_{BG} *= 1.2 V*

Table 21. **Bypass switch**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DS\_BYPASS\_SAT}$	Bypass switch VDS saturation protection threshold		1	-	2	V
I_{BYPASS_SAT}	Bypass switch saturation current	$V_S - V_{OUT} = V_{DS\_BYPASS\_SAT}$	297	572	900	mA
$R_{DS(ON)\_BYPASS}$	Bypass switch on state resistance		1	2	4.5	Ω
t_{ON_BYPOFF}	Output turn-on time on bypass-shutting off		-	-	100	µs
$t_{BYPASS\_SAT\_DEGLITCH}$	Bypass switch saturation diagnostic de-glitch filtering time	Standby state	-20%	5	+20%	µs

Table 22. V_{OUT} **A-to-D conversion**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{OUT\_ADC\_CONV}$	V_{OUT} ADC full range resolution(1)		0	-	1023	
$V_{OUT\_ADC\_RATE}$	V_{OUT} ADC sample rate		-	4.9	-	kSample/s
$V_{OUT\_ACC\_1V}$	Output voltage accuracy	$1 < V_{OUT} \leq 2$ V	-18	-	18	%
$V_{OUT\_ACC\_2V}$	Output voltage accuracy	$2 V < V_{OUT} \leq 3$ V	-9	-	9	%
$V_{OUT\_ACC\_3V}$	Output voltage accuracy	$3 V < V_{OUT} \leq 12$ V	-6	-	6	%
$V_{OUT\_ACC\_12V}$	Output voltage accuracy	$12 V < V_{OUT} \leq 60$ V	-3	-	3	%

1. V_{OUT} *(mV) =* V_{OUT_ADC} *[9:0] * 1.2 * 51 / 1024.*

Table 23. **Self-test timing**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{S\_T\_ACTIVE}$	Self-test execution time		-10%	5	+10%	µs
$t_{S\_T\_WAIT}$	Self-test wait time		-10%	5	+10%	µs

3 eFuse function

Protection of wire harness and PCB can be performed by defining an ideal time to fuse curve as a result of a maximum power dissipation over the time in the wire or copper PCB traces themselves. This function can ensure that the insulation of wires and PCB are subject to a limited temperature and time budget that is below the reliability specified values. Not respecting such specified limits can lead to the formation of a conducting path by carbonization across the organic insulation materials and therefore local hot spot can conduct to sparking and fire ignition.

The VNF1248F embeds the ST proprietary eFuse functionality for the implementation of a robust and flexible overcurrent protection mechanism. The eFuse functionality features an intelligent circuit breaking aimed at protecting PCB traces, connectors and wire harness from overheating, with no impact on load transients like inrush currents and capacitance charging.

This function is set by two parameters called I_{NOM} and t_{NOM}. The value of I_{NOM} corresponds to the maximum continuous current while t_{NOM} will determine a current versus time-to-fuse curve when load current is higher than I_{NOM}. The expression of current versus time-to-fuse is approximated by an optimized stepwise function, which can be adjusted in a range between the wire I^2-t limit on one side and load transient characteristics on the other side. The value of t_{NOM} corresponds to the first step up of the curve. The current time curve is always active in combination with very fast overcurrent protection that will be triggered when the current reaches a defined threshold for hard short circuit condition.

When the current in the load is pulse wide modulated the eFuse function calculates the mean square root of the current. Mean square root of the current is also calculated when switching on/off the power switch during normal operation or after a switch off due to short circuit/overload condition. So, if for example the circuit is broken due to an overload and after a while the circuit is activated again, the eFuse keeps in memory the previous condition and still avoids that maximum I_{RMS} is higher than I_{NOM}.

VIP-Fuse is programmed via SPI as follows:

- VOC_THRS sets I_{NOM} = VOC_THRS/Rsense
- VHSC_THRS sets hard short circuit current = VHSC_THRS/Rsense
- T_NOM sets t_{NOM} from 1 to 511 s

No intervention occurs for VSENSE < VOC_THRS, whilst an immediate shut-off occurs for VSENSE > VHSC_THRS.

The eFuse functionality operating range is defined between VOC_THRS and VHSC_THRS. In that range, the circuit breaking profile is defined by the stepwise function reported in Figure 5. The number of steps is consequential to the selection of VOC_THRS and VHSC_THRS, the maximum being 15, when VOC_THRS = 6 mV and VHSC_THRS = 160 mV. This corresponds to a 1:26.67 ratio between the maximum allowed continuous current and hard short circuit.

The Figure 6 shows the I^2-t curve when VOC_THRS = 26.5 mV and VHSC_THRS = 105.60 mV. The number of steps is reduced to 9 accordingly.

Figure 5. eFuse I^2-t typical curve (VOC_thrs minimum - VHSC_thrs maximum)

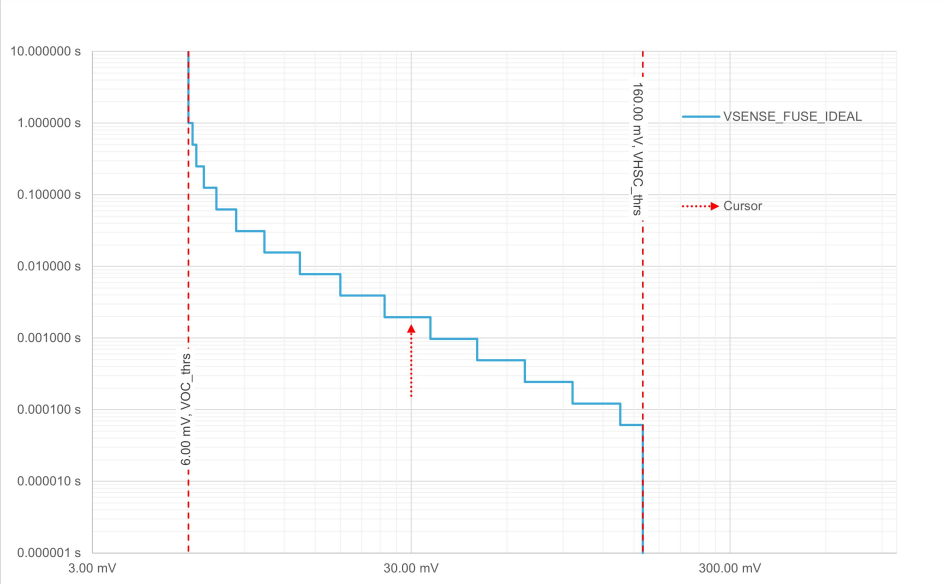
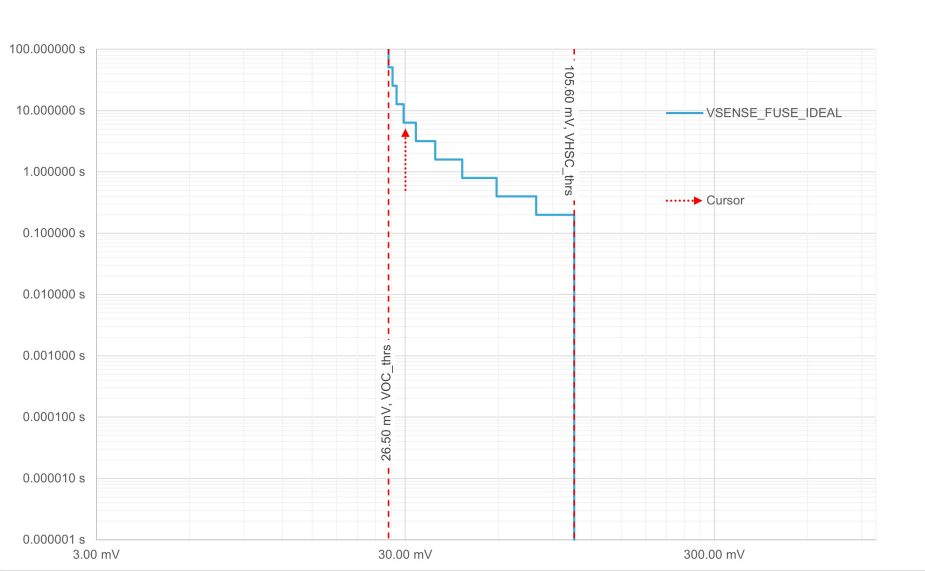


Figure 6. eFuse I^2-t typical curve (generic thresholds)



4 Self-test

The following sections describe how the device supports the execution of the in-application tests needed to verify the proper behavior of the hardware diagnostic verification during product lifetime. Configuration, control, and check for each of the tests is performed in close relationship with the microcontroller, through SPI interface communication.

Activities related to self-test are possible in a specific device state (self-test) to distinguish it from operating modes (standby, wake-up, unlocked, and locked modes), allowing to manage differently diagnostic faults according to the hardware feature under test.

Self-test control interface

The initialization of the self-test sequence (selection of the self-test, start, and stop command) is done through the control register 1 (CR#1). Results are accessible through the status register 5 (SR#5), status register 6 (SR#6) and status register 7 (SR#7).

4.1 Current sense self-test

The purpose of the current sense self-test is to verify the proper behavior of the full current sense chain, from the analog input to the digital output.

Starting from the unlocked state, the current sense self-test is activated through a dedicated SPI frame. The duration of this test is defined by $t_{S\_T\_ACTIVE}$ + $t_{S\_T\_WAIT}$ (10 µs); first $t_{S\_T\_ACTIVE}$ period is intended for measure and A/D conversion execution, while $t_{S\_T\_WAIT}$ period is needed to allow transients expiration.

Once the self-test is started, an internal current generator provides a current sink able to produce an additional voltage drop of 100 mV at the input pin of the internal comparator.

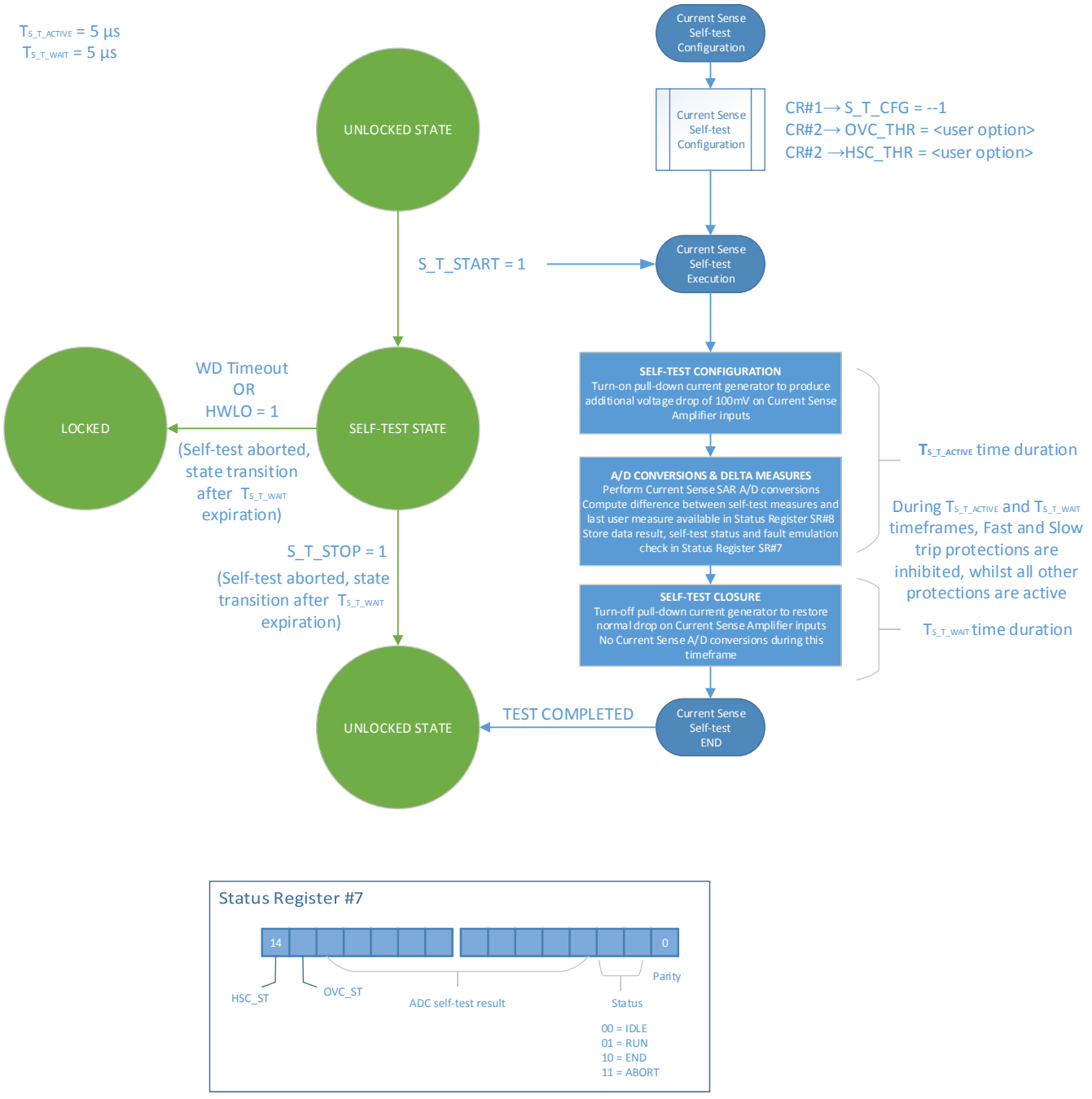
The result of the self-test is the difference between this converted value and the value already stored in SR#8 (HSC field), corresponding to the normal measurement performed during operation; such result is stored in SR#7 together with the self-test status.

The transition from self-test state to unlocked state is automatically ensured after the test is completed (around 10 µs) or if the test is stopped through S_T_STOP = 1 (self-test aborted).

The transition from the self-test state to the locked state occurs in case of watchdog timeout or HWLO = 1 (self-test aborted).

When the self-test is in execution if bypass and ext_fet are ON, this state is kept.

Figure 7. Current sense self-test flow sequence



4.2 External FET V_{DS} detection self-test

The purpose of the external FET V_{DS} detection self-test is to verify the proper behavior of the complete V_{DS} monitor chain (sense/process/detection), from the analog input to the digital output.

Starting from the unlocked state, the V_{DS} detection self-test is activated through a dedicated SPI frame. The duration of this test is defined by $t_{S\_T\_ACTIVE}$ + $t_{S\_T\_WAIT}$ (10 µs); first $t_{S\_T\_ACTIVE}$ period is intended to convert the value of the voltage across the drain and source terminals of the external FET, while $t_{S\_T\_WAIT}$ period is needed to bring back the analog circuitry to normal configuration.

Once the self-test is started, an internal current generator provides a current sink able to produce an additional voltage offset of 100 mV on V_{DS} monitor circuit inputs, to distinguish self-test execution from normal operation. In order to ensure proper data conversions, special care must be taken to avoid V_{DS} ADC saturation by keeping the overall V_{DS} sensed by the monitor circuit below the maximum scale range (V_{DS}_ADC_CONV).

V_{DS} detection self-test result is the difference between the converted value obtained during self-test execution and the value already stored in SR#4 (V_{DS} field), corresponding to the normal measurement performed during operation; such delta measure result is stored in SR#5 (S_T_VDS field) together with the self-test status.

During self-test execution it is also possible to emulate the external FET V_{DS} fault condition by playing with programmable thresholds available through register CR#2 (VDS_THRS field) ; fault emulation result is stored in SR#5 (S_T_VDS_MAX1 bit field).

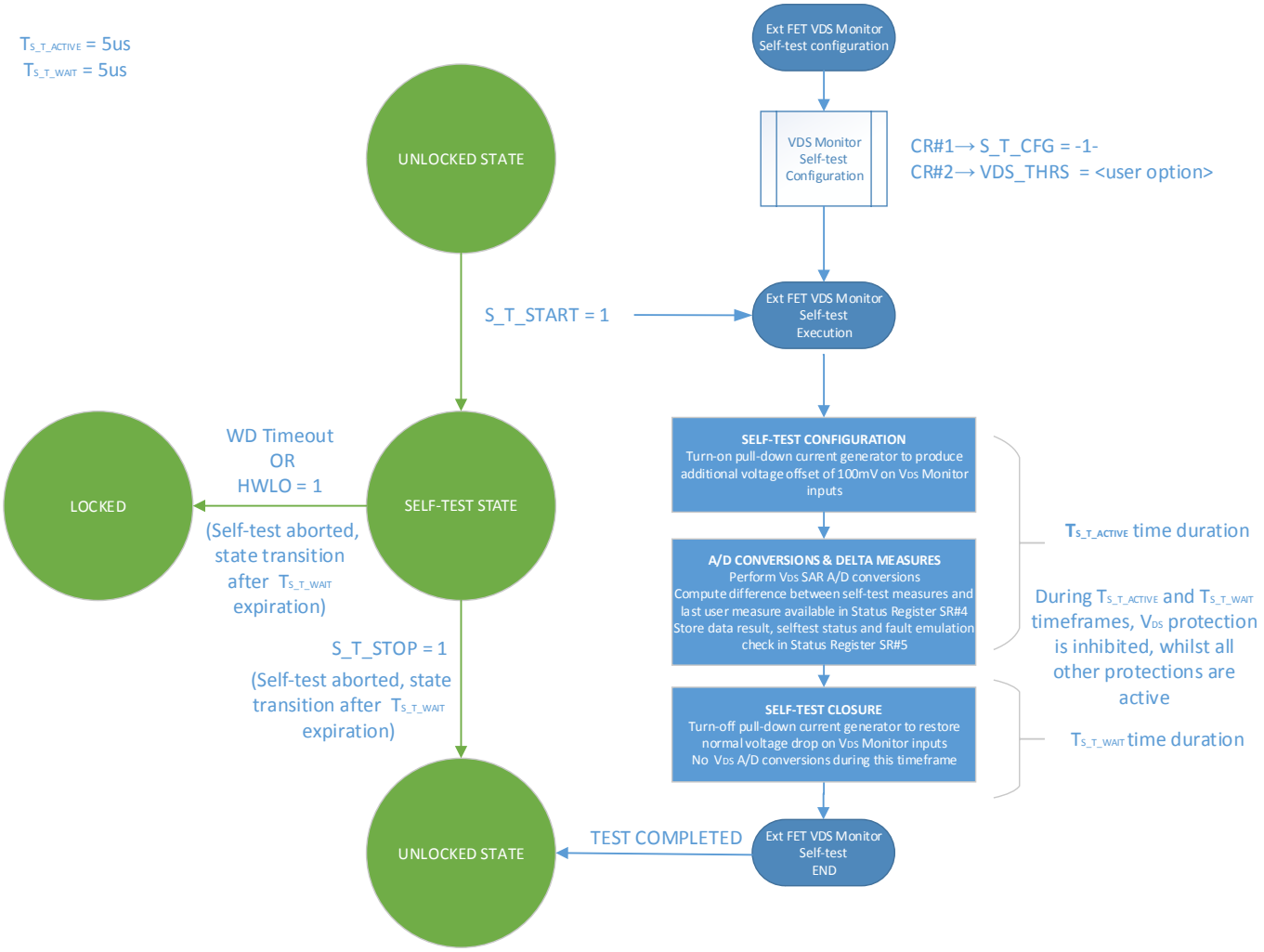
To be noted that diagnostic fault for normal operation (VDS_MAX, SR#1) is inhibited during execution, while all the others are kept enabled.

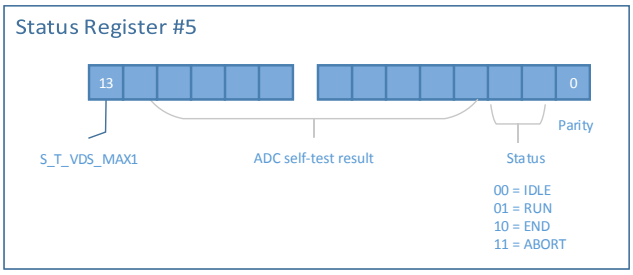
The transition from self-test state to unlocked state is automatically ensured after the test is completed (around 10 µs) or if the test is stopped through S_T_STOP = 1 (self-test aborted).

The transition from the self-test state to the locked state can occur in case of watchdog timeout or HWLO = 1 (self-test aborted).

When the self test is in execution if bypass and ext_fet are ON, this state is kept.

Figure 8. VDS monitor self-test flow sequence





4.3 External FET stuck-on self-test

The goal of this self-test is to verify the proper turn-off of the external power switch, by monitoring its V_{DS} behavior in time.

Starting from the unlocked State, the external FET stuck-on self-test is activated through a dedicated SPI frame (CR#1, S_T_START and S_T_CFG fields).

At execution start the external FET is automatically turned-off, regardless of its status during previous operations, then continuous AtoD conversions of V_{DS} voltage, sensed across external power switch terminals, are performed in order to allow the user to monitor V_{DS} evolution in time.

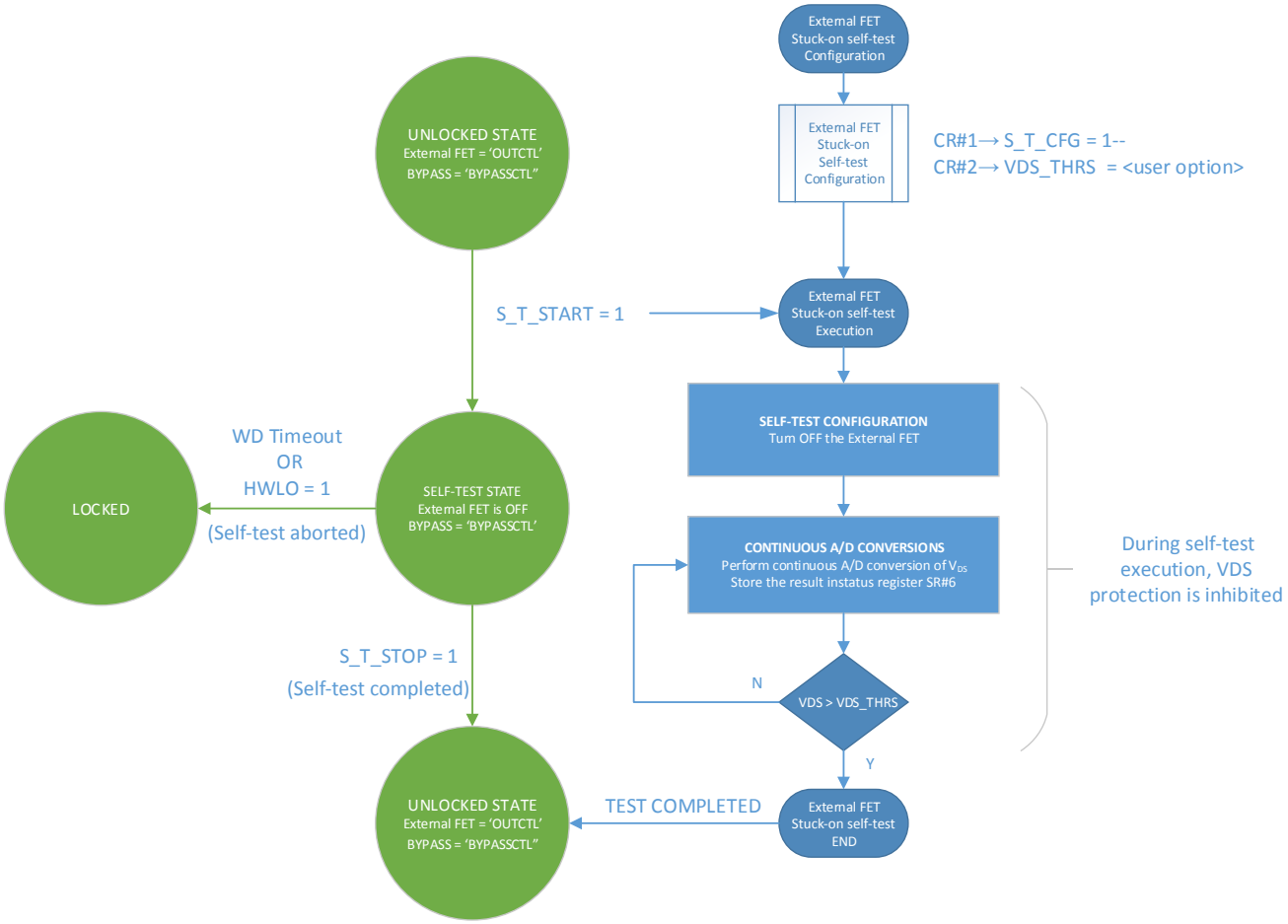
Data conversion values are made available through dedicated register SR#6 (S_T_STUCK field); in addition, a specific bit informs the user if the data have been updated with a new measure or are still relative to the previous one (UPDT_S_T_STUCK bit). Status of self-test execution is available in the same register.

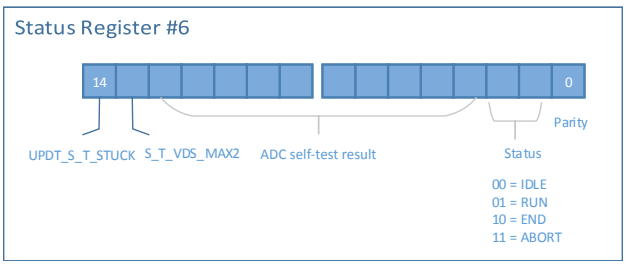
Self-test completion can be controlled directly by sending the S_T_STOP command (CR#1, bit 8) or by setting the programmable V_{DS} threshold (CR#2, VDS_THRS field) : in this case, self-test is stopped automatically as soon as the external FET V_{DS} overcomes the previously mentioned threshold and a specific bit is set to flag this situation (SR#6, S_T_VDS_MAX2 bit). In both cases, device FSM performs the transition from self-test to unlocked state.

To be noted that the diagnostic fault for normal operation (VDS_MAX, SR#1) is inhibited during execution, while all the others are kept enabled; bypass switch control is left to the user.

The transition from the self-test state to the LOCKED state can occur in case of watchdog timeout or HWLO = 1 (self-test aborted).

Figure 9. External FET stuck-on self-test flow sequence for entry





5 VSPI pin undervoltage monitor

The device implements a monitor of VSPI pin voltage in order to detect SPI interface supply below expected value; this is required to avoid unexpected device wakeup from standby state caused by CSN pin driven low by VSPI drop or shutoff (uC in standby condition).

When VSPI voltage is lower than VSPI_UV threshold (refer to Table 4), device wake up from standby state through CSN pin is inhibited.

6 DIN input management

The device allows external FET control directly by hardware, through a dedicated input pin (DIN), in addition to software control by the SPI interface. Through this pin, it is possible to turn-on/turn-off directly the power switch, providing an alternative to application host management, as requested by safety requirements and by application use cases in which the device could operate without the SPI interface being active. Clearly, DIN control is superseded by faults occurrence.

On top of this functionality, DIN input is also used as an additional device wake up source from standby state and as enable for capacitive charging mode functionality, if properly driven.

To fulfill different application requirements, DIN management can be configured by dedicated programmable register fields to achieve distinct behaviors in the three main device active states (unlocked, locked, and fail-safe).

6.1 Standby state

As mentioned, a pulse on the DIN input, with duration > t_{DIN_WAKEUP}, triggers the device wake-up (apart from the FS_MODE = "01" configuration, where the DIN wake-up feature is disabled), allowing to move to the fail-safe state with all relevant circuits enabled to allow external FET driving. No other DIN functions are available in this state.

6.2 Unlocked state

In this state, DIN behavior is defined by the following control register fields:

- DIN_CTRL_EN (CR#1): this bit enables the use of DIN input for output control; access to this control field is managed by unlock sequence;
  - DIN_CTRL_EN = ‘0’ → DIN input not effective, output directly controlled only by OUTCTL bit
  - DIN_CTRL_EN = ‘1’ → DIN input control enabled
- DIN_CTRL_OPT (CR#1): this bit defines the functional combination of DIN input with the correspondent SPI-driven control bit (OUTCTL, CR#1); access to this control field is managed by the unlock sequence;
  - DIN_CTRL_OPT = ‘0’ → to turn ON external FET regardless of OUTCTL bit status; so-called OR mode behavior, for example useful for quasi-synch turn-on in case of application with multiple controllers and power switches sharing the same load
  - DIN_CTRL_OPT = ‘1’ → to turn OFF external FET regardless of OUTCTL bit status; so-called AND mode behavior, for example useful for quasi-synch turn-off in case of application with multiple controllers sharing the same load)

The table below shows possible combinations of DIN input with SPI-driven controls, depending on DIN control bit configuration, and their effects on device outputs (power switch and diagnostic output) and internal blocks (bypass switch); in case of bypass saturation detection (BYPASS_SAT fault), the power switch is automatically turned on and bypass switched off, regardless of DIN/OUTCTL/BYPASSCTL status, to ensure proper driving of load.

Table 24. Unlocked state - DIN control behavior

BYPASS_SAT bit	DIN_CTRL_EN bit	DIN_CTRL_OPT bit	DIN input	OUTCTL bit	BYPASSCTL bit	OUTPUT	BYPASS
1	x	x	x	x	x	On	Off
0	0	x	x	0/1	0/1	Off/On	Off/On
	1	0	0				
	1	0	1	x		On	
	1	1	0	x		Off	
	1	1	1	0/1		Off/On	

In this state, internal bypass switch control is independent from DIN setting, only BYPASSCTL bit defines its status; in case of user setting (DIN_CTRL_EN = '1', DIN_CTRL_OPT = '1'), AND mode configuration, where DIN is used to fast turn-off external power switch, it is recommended to set BYPASSCTL=0 accordingly, to avoid BYPASS_SAT fault generation and, consequently, power switch automatically turned on again (overriding DIN action).

6.3 Locked state

Output and bypass behavior according to DIN are the same as in unlocked state but, depending on device configuration, DIN_CTRL_EN and DIN_CTRL_OPT settings are taken from:

- Default configuration stored into NVM memory, if NVM_DEF_CFG_EN = 1
- RAM configuration register fields, if NVM_DEF_CFG_EN = 0.

6.4 Fail-safe state

In this state DIN behavior is conditioned by the following programmable control register field:

- FS_MODE[1:0] (CR#1): it defines three different modes for output channel and bypass switch management in fail-safe; access to this control field is managed by unlock sequence;
  - FS_MODE = '00'/'01': output directly controlled by DIN; in this configuration, DIN_CTRL_EN control field is accessible, through unlock sequence, to allow keeping DIN control active after fail-safe → unlocked transition, avoiding holes in driving power switch
  - FS_MODE = '10': last output state from unlocked/locked kept (same for bypass)
  - FS_MODE = '11': output and bypass turned off

Table 25. Fail-safe state

BYPASS_SAT bit	FS_MODE [1:0]	DIN input	OUTCTL bit	BYPASSCTL bit	Output	Bypass	DIAG
1	xx	x	x	x	On	Off	Low
0	0x	1	x	x	On	Refer to the Table 26	High/Low
		0	x	x	Off		High/Low
	10	x	x	x	Last state maintained	Last state maintained	High/Low
	11	x	x	x	Off	Off	Low

6.5 DIN toggling

As mentioned above, DIN can be used to enable capacitive charging mode functionality (described in the following section of this document), when device is in fail-safe state. To do that, a specific toggling sequence on this input shall be executed, consisting of, 4 DIN pulses rising edges within a maximum time of $t_{DIN\_TOGGLE\_TOUT}$, after which sequence need to be restarted. Each pulse duration shall be $t_{DIN\_DEGLITCH} < t < t_{DIN\_RISE\_FILTER}$, where $t_{DIN\_RISE\_FILTER}$ represents the time interval after which DIN pulse is considered valid for driving directly the external FET (capacitive charging mode not started).

The Table 11 reports timings of different DIN functionalities.

7 Bypass control management

Bypass switch control and status is determined by the following device settings:

- BYPASSCTL (CR#1): dedicated programmable control bit in RAM register map.
- BYPASS_CTL_DEF: bit belonging to NVM default configuration, available if NVM_DEF_CFG_EN is set to '1' (see Section 10.1: NVM – Programmable default configuration), used to define bypass status in standby and fail-safe states.
- BYPASS_SAT: bypass switch dedicated protection.
- FS_MODE (CR#1): fail-safe programmable output behavior.
- DIN: in fail-safe state, with DIN-controlled configuration (FS_MODE = '0x') and BYPASS_CTL_DEF = '1', first falling edge of DIN will cause bypass turn-off too; this to let DIN having full control on external FET and avoiding automatic turn-on due BYPASS_SAT protection intervention (that would occur if bypass is kept on).

The Table 26 provides bypass switch behavior, according to aforementioned setting and correspondent device states:

Table 26. Bypass switch control vs FSM

<table>
<tr><th>To state →
From state ↓</th><th>Locked</th><th>Fail-safe</th><th>Self-test</th><th>Power-on</th><th>Standby</th><th>Unlocked</th></tr>
<tr><td>Power-on</td><td rowspan="3">Not allowed</td><td>Not allowed</td><td rowspan="3">Not allowed</td><td rowspan="6">OFF</td><td>If NVM_DEF_CFG_EN = '0'
→ OFF
If NVM_DEF_CFG_EN = '1'
→ BYPASS_DEF</td><td>Not allowed</td></tr>
<tr><td>Standby</td><td>if BYPASS_SAT = '1' → OFF
if FS_MODE = '11' → OFF
if FS_MODE = '10' → HOLD LAST STATE
if FS_MODE = '0x'
→ OFF if NVM_DEF_CFG_EN = '0'
→ BYPASS_CTL_DEF if NVM_DEF_CFG_EN = '1'</td><td rowspan="3">If NVM_DEF_CFG_EN = '0'
→ BYPASS_CTL
If NVM_DEF_CFG_EN = '1'
→ BYPASS_DEF</td><td rowspan="2">BYPASS_CTL</td></tr>
<tr><td>Fail-safe</td><td>if BYPASS_SAT = '1' → OFF
if FS_MODE = '11' → OFF
if FS_MODE = '10' → HOLD LAST STATE
if FS_MODE = '0x'
→ OFF if NVM_DEF_CFG_EN = '0'
→ BYPASS_CTL_DEF if NVM_DEF_CFG_EN = '1'
→ OFF if DIN falling edge</td></tr>
<tr><td>Unlocked</td><td>BYPASS_CTL</td><td rowspan="3">if FS_MODE = '11' → OFF
if FS_MODE = '10' → HOLD LAST STATE
if FS_MODE = '0x'
→ OFF if NVM_DEF_CFG_EN = '0'
→ BYPASS_CTL_DEF if NVM_DEF_CFG_EN = '1'</td><td>BYPASS_CTL</td><td>If BYPASS_SAT=1
→ OFF
If BYPASS_SAT=0
→ BYPASS_CTL</td></tr>
<tr><td>Locked</td><td>if BYPASS_SAT = '1'
→ OFF else BYPASS_CTL</td><td>Not allowed</td><td rowspan="2">BYPASS_CTL</td></tr>
<tr><td>Self-test</td><td>Not allowed</td><td>BYPASS_CTL</td><td>Not allowed</td></tr>
</table>

8 External LDO

An external power supply can be used to power the device and reduce the consumption of the VS pin in normal mode. If the voltage $V_{EXT\_LDO} > V_{EXT\_LDO\_H}$, the device is automatically powered by the external regulator, and the current is supplied by the external LDO, thus reducing battery consumption. The EXT_REG_ON bit is latched to "1". Instead, if the voltage $V_{EXT\_LDO} < V_{EXT\_LDO\_L}$, the device is automatically powered by the internal LDO, and the current is supplied through the VS pin.

9 Capacitive charging mode–CCM

Digital logic implements a PWM-based control of high-side driver to allow charging a capacitive load through the off-chip power MOSFET driven by the device.

Load charging is split in two phases:

- Start charging: in this phase the load is charged with a slower PWM period, to check for possible short circuit on output; a maximum number of PWM pulses is allowed to reach a minimum V_{OUT} value, otherwise CCM is aborted
- Standard charging: in this phase the load is charged with a nominal PWM period until V_{DS} reaches an internally defined threshold (100 mV), or timeout limit is reached

Burst mode control is configured by the following programmable parameters:

- PWM period (CR#5 - CCM_PWM_T): PWM period (T_{on} + T_{off}) set during standard charging phase
- PWM T_{on} time (CR#5 - CCM_PWM_TON): PWM interval time with high-side driver turned on
- PWM T_{on} Multiplying Factor (CR#3 - CCM_PWM_TON_MF): to multiply by 1/2/4/8 T_{on} time defined by CCM_PWM_TON setting, for duty cycle configuration
- PWM start period (CR#5 - CCM_PWM_SC_T): PWM period (T_{on} + T_{off}) set during starting phase (short circuit check)
- PWM start pulses max number (CR#5 - CCM_PWM_SC_T_NB): Max number of PWM pulses during starting phase (short circuit check)
- CCM timeout (CR#5 – CCM_PWM_TIMEOUT): Maximum time allowed to charging phase
- V_{OUT} threshold (CR#3 – CCM_VOUT_THR): V_{OUT} limit to overcome to switch form starting phase to standard charging phase

According to parameter settings, PWM frequency and duty cycle allowed ranges are:

- PWM standard frequency = 1/CCM_PWM_T → [250 Hz : 20 kHz]
- PWM standard duty cycle = CCM_PWM_TON_MF*CCM_PWM_TON/CCM_PWM_T
  - CCM_PWM_T = 50 µs (min.) → CCM_PWM_TON_MF x [2 : 100]%
  - CCM_PWM_T = 4 ms (max.) → CCM_PWM_TON_MF x [0.025 : 1.25]%
- PWM start frequency = 1/CCM_PWM_SC_T → [250 Hz : 500 Hz]
- PWM start duty cycle = CCM_PWM_TON_MF*CCM_PWM_TON/CCM_PWM_SC_T
  - CCM_PWM_SC_T = 2 ms (min.) → CCM_PWM_TON_MF x [0.05: 2.5]%
  - CCM_PWM_SC_T = 4 ms (max.) → CCM_PWM_TON_MF x [0.025 : 1.25]%

Burst mode control can be activated in two different ways.

- Control registers: two trigger bits (CR#1 - CCM_CTRL_ON, CCM_CTRL_OFF) are available to, respectively, turn-on or turn-off CCM burst mode when the device is in unlocked/locked state
- DIN input: specific toggling sequence on this pin (at least 4 rising edges within $t_{DIN\_TOGGLE\_TOUT}$) allows to turn-on CCM burst mode when the device is in fail-safe state; DIN must be kept high during CCM, as DIN is driven low load charging is stopped and the device exits from CCM burst mode

CCM operation status is accessible through a specific field in SR#1 register (CCM_STATUS), encoding the following information:

- IDLE: CCM operation not started
- RUN: CCM operation started, running
- CHARGED: CCM operation completed successfully (V_{DS} fixed threshold reached)
- CHARGE INCOMPLETE: CCM operation aborted (timeout or short-circuit condition) or stopped (CCM switched off while running)

Table 27. CCM PWM T_{on} setting

CCM_PWM_TON			
Register field value	PWM T_{on} value [µs]	Register field value	PWM T_{on} value [µs]
0x00	T_{on} stopped by protection	0x20	**23**
0x01	1	0x21	24
0x02	1.5	0x22	25
0x03	2	0x23	26
0x04	2.5	0x24	27
0x05	3	0x25	28
0x06	3.5	0x26	29
0x07	4	0x27	30
0x08	4.5	0x28	31
0x09	5	0x29	32
0x0A	5.5	0x2A	33
0x0B	6	0x2B	34
0x0C	6.5	0x2C	35
0x0D	7	0x2D	36
0x0E	7.5	0x2E	37
0x0F	8	0x2F	38
0x10	8.5	0x30	39
0x11	9	0x31	40
0x12	9.5	0x32	41
0x13	10	0x33	42
0x14	11	0x34	43
0x15	12	0x35	44
0x16	13	0x36	45
0x17	14	0x37	46
0x18	15	0x38	47
0x19	16	0x39	48
0x1A	17	0x3A	49
0x1B	18	0x3B	50
0x1C	19	0x3C	50
0x1D	20	0x3D	50
0x1E	21	0x3E	50
0x1F	22	0x3F	50

Table 28. **CCM PWM max. start pulses number setting**

CCM_PWM_SC_T_NB			
Register field value	Number of PWM low frequency pulses	Register field value	Number of PWM low frequency pulses
0x00	5	0x10	22
0x01	6	0x11	24
0x02	7	0x12	26
0x03	8	0x13	28
0x04	9	0x14	30
0x05	10	0x15	32
0x06	11	0x16	34
0x07	12	0x17	36
0x08	13	0x18	38
0x09	14	0x19	40
0x0A	15	0x1A	42
0x0B	16	0x1B	44
0x0C	17	0x1C	46
0x0D	18	0x1D	48
0x0E	19	0x1E	50
0x0F	20	0x1F	50

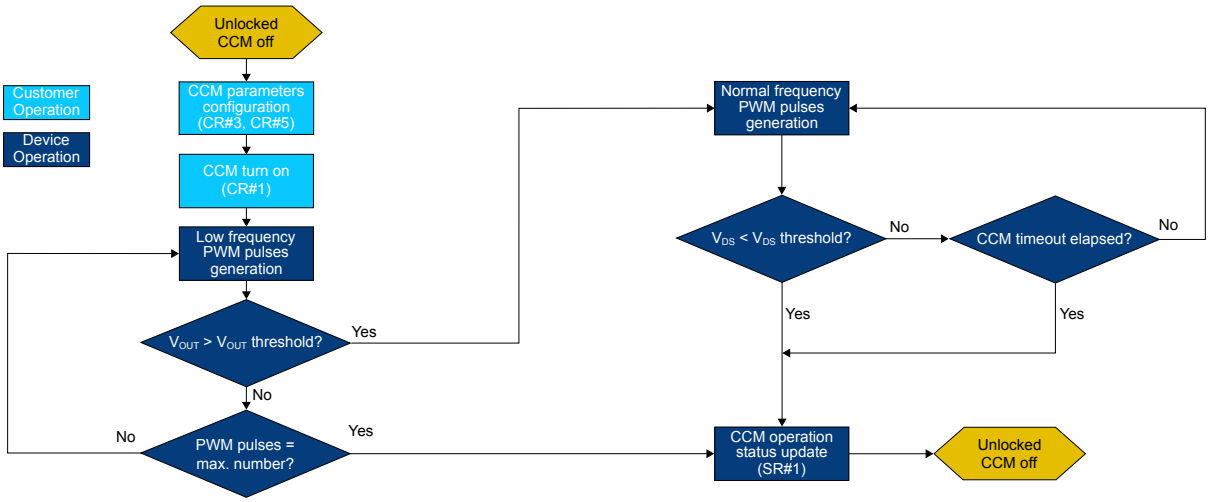
Table 29. **CCM PWM standard period setting**

CCM_PWM_T			
Register field value	PWM standard period duration [µs]	Register field value	PWM standard period duration [µs]
0x00	50	0x20	3100
0x01	100	0x21	3200
0x02	150	0x22	3300
0x03	200	0x23	3400
0x04	300	0x24	3500
0x05	400	0x25	3600
0x06	500	0x26	3700
0x07	600	0x27	3800
0x08	700	0x28	3900
0x09	800	0x29	4000
0x0A	900	0x2A	4000
0x0B	1000	0x2B	4000
0x0C	1100	0x2C	4000
0x0D	1200	0x2D	4000
0x0E	1300	0x2E	4000
0x0F	1400	0x2F	4000
0x10	1500	0x30	4000
0x11	1600	0x31	4000
0x12	1700	0x32	4000
0x13	1800	0x33	4000
0x14	1900	0x34	4000
0x15	2000	0x35	4000
0x16	2100	0x36	4000
0x17	2200	0x37	4000
0x18	2300	0x38	4000
0x19	2400	0x39	4000
0x1A	2500	0x3A	4000
0x1B	2600	0x3B	4000
0x1C	2700	0x3C	4000
0x1D	2800	0x3D	4000
0x1E	2900	0x3E	4000
0x1F	3000	0x3F	4000

9.1 Control algorithm

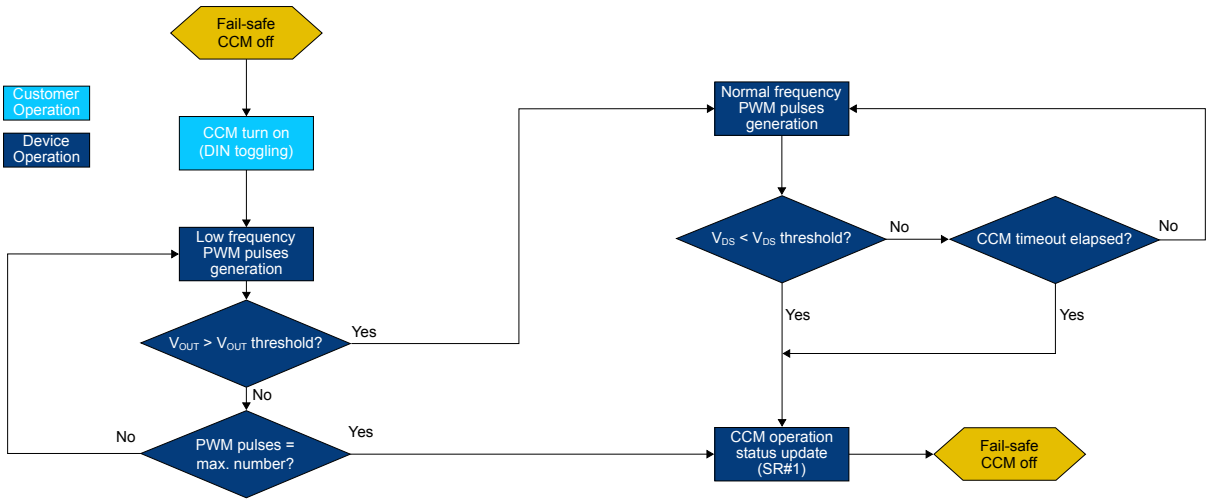
The following flow charts show the sequence of operations foreseen by CCM control algorithm, for those device states in which load charging is allowed.

Figure 10. CCM in unlocked state (1)



Note: (1) Same flow chart in locked mode but it is not possible to perform the first step, CCM parameter configuration (CR#3, CR#5). In this case it needs to configure before enter in the locked state.

Figure 11. CCM in fail-safe state



10 Non-volatile memory (NVM) customer programming

The control logic unit enables the capability to program, by the user, part of the NVM memory embedded in the device, to test and store the specific settings for some of the key parameters, to be used during the operations.

Specifically, one sector (sector 5) of the six available can be write/read by the customer, after having entered a proper command sequence, needed to ensure a secure and safe access to this functionality, avoiding unexpected write operations could corrupt NVM content.

To perform write/read operations, digital control exploits RAM register fields dedicated to the mentioned parameters as source (for write) or destination (for read) of NVM data to be stored, or read; a specific logic map register field into the NVM sector, preparing the 120-bit word that the NVM interface IP writes serially to the memory; opposite mapping is performed by the same logic during read operation.

User access to NVM Write/Read functionalities is enabled by the following sequence:

1. SPI write frame to set UNLOCK bit to 1 (CR#3)
2. SPI write frame to write customer access key (CR#4)

The above steps shall be performed sequentially, not interleaved by any other command, otherwise user access is not unlocked.

After having properly completed the sequence, register CR#4 makes available the following fields to control NVM Write/Read operations:

- NVM_ADDR: address of the NVM sector to be read/written
- NVM_WR_EN: NVM operation type (1 --> write, 0 --> read)
- NVM_OP_START: trigger bit to start the selected NVM operation

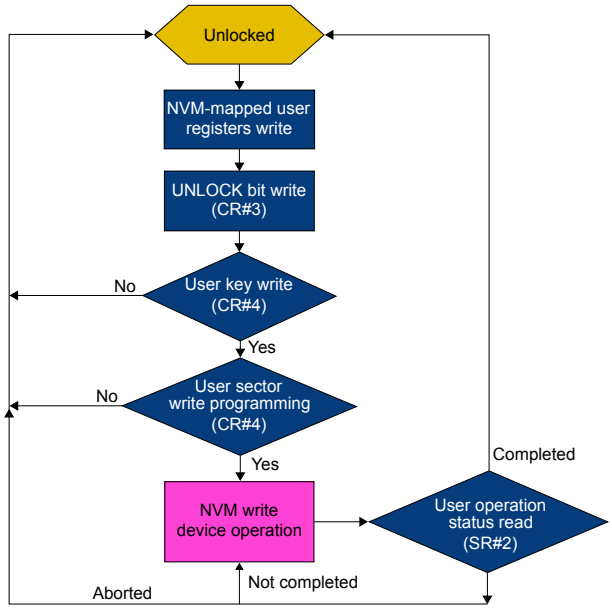
The steps for Programming/Write execution are the following:

1. The user writes through SPI those RAM registers fields related to parameters target of NVM programming
2. The user writes through SPI the required 2-steps access sequence
3. The user writes through SPI sector address, access type and start command in the unlocked dedicated register (CR#4)
4. Digital control logic maps RAM register fields into the equivalent NVM sector
5. Digital control logic provides control, address, and data to NVM interface IP
6. NVM IP interface handles NVM memory IP programming procedure
7. NVM IP interface notifies programming phase completion to digital logic
8. User reads (and clear) through SPI RAM register field reporting NVM operation status

Note: During NVM write execution, correspondent RAM register fields shall be kept constant, considering they are direct sources of data stored into the NVM sector (no intermediate buffering).

In case of the customer NVM write involving only a subset of allowed programmable parameters (partial write), it is mandatory to run first an NVM read operation, to fill the RAM register fields of those parameters that is not be affected by the changes, avoiding overwriting their NVM locations with unwanted values (NVM write operation consider all RAM register fields belonging to NVM target sector).

Figure 12. **NVM write operation**

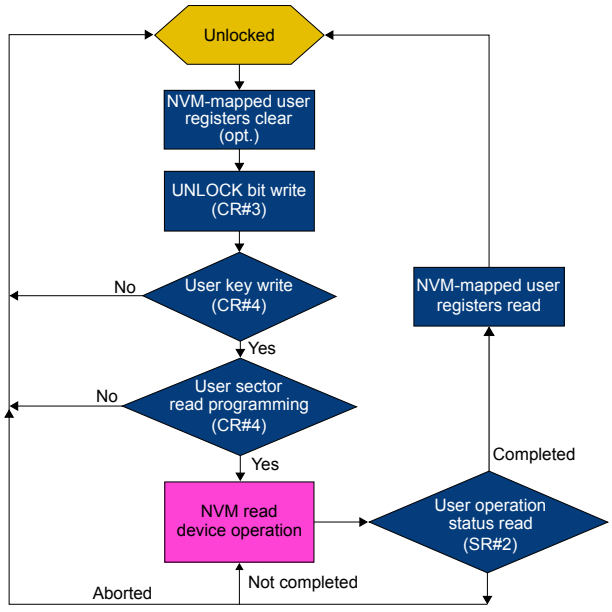


For what concerns NVM read execution, the steps are the following:

1. User reset (by writing 0) target RAM register fields (optional)
2. The user writes, through SPI, the required 2-steps access sequence
3. User writes, through SPI, sector address, access type and start command in the unlocked dedicated register (CR#4)
4. Digital control logic provides controls and address to NVM interface IP
5. NVM IP interface handles NVM memory IP reading procedure
6. NVM IP interface notifies reading phase completion to digital logic
7. Digital control logic maps sector data output to respective RAM register fields
8. User reads (and clear), through SPI, RAM register field reporting NVM operation status

The user reads through SPI, RAM register fields corresponding to addressed device parameters.

Figure 13. **NVM read operation**



10.1 NVM – Programmable default configuration

As mentioned previously, the device foresees the possibility to store, inside the NVM memory, a default configuration for some key device parameters, critical from an operational/safety viewpoint, to be loaded only when the device switches to fail-safe or locked states, to ensure a well-known, and not modifiable behavior in such states; as soon as the device exits from them, parameter values are set back to the current setting stored inside programmable RAM configuration registers, restoring the latest user configuration.

Loading of default settings is configurable by a specific bit (NVM_DEF_CFG_EN), accessible through CR#1, and stored into NVM; modification of this bit shall be performed during device configuration by the user, while defining the proper default setting, it is not recommended to do that during device operation in the application.

The following table summarizes the key device parameters equipped with NVM default configuration and stored into correspondent memory sector #5:

Table 30. NVM mapped configuration parameters

Name	Description	Register field	Use
DIN_CTRL_EN_DEF	Direct input control enable	CR#1→DIN_CTRL_EN	Locked
DIN_CTRL_OPT_DEF	Direct input control behavior selection (AND/OR modes)	CR#1→DIN_CTRL_OPT	Locked
BYPASS_CTL_DEF	Internal bypass control	CR#1→BYPASS_CTL	Fail-safe/Standby
FS_MODE_DEF	Output behavior configuration in fail-safe	CR#1→FS_MODE	Fail-safe
NVM_DEF_CFG_EN	Fail-safe default configuration enable	CR#1→NVM_DEF_CFG_EN	Fail-safe/Locked
T_NOM_FS_DEF	I2t fuse emulation nominal timescale	CR#2→TNOM	Fail-safe/Locked
OVC_THR_FS_DEF	I2t fuse emulation nominal overcurrent protection threshold selection	CR#2→OVC_THR	Fail-safe/Locked
HSC_THR_FS_DEF	Hard short protection threshold selection	CR#2 →HSC_THR	Fail-safe/Locked
VDS_THRS_FS_DEF	V_{DS} protection threshold selection	CR#2→VDS_THRS	Fail-safe/Locked
NTC_THR_FS_DEF	NTC thermal protection threshold selection	CR#3→NTC_THR	Fail-safe/Locked
WD_TIME_DEF	Watchdog monitor timeout selection	CR#3→WD_TIME	Fail-safe/Locked
UV_THR_DEF	Vs undervoltage threshold selection	CR#3→UV_THR	Fail-safe/Locked
CS_UV_RETRY_T_DEF	Current sense undervoltage protection retry time	CR#3→CS_UV_RETRY_T	Fail-safe/Locked
CCM_VOUT_THR_DEF	Capacitive load charge (burst mode) V_{OUT} threshold selection	CR#3→CCM_VOUT_THR	Fail-safe/Locked
CCM_PWM_TON_MF_DEF	Capacitive load charge (burst mode) PWM ton multiplying factor	CR#3→CCM_PWM_TON_MF	Fail-safe/Locked
CCM_PWM_TON_DEF	Capacitive load charge (burst mode) PWM ton setting	CR#5→CCM_PWM_TON	Fail-safe/Locked
CCM_PWM_T_DEF	Capacitive load charge (burst mode) PWM period	CR#5→CCM_PWM_T	Fail-safe/Locked
CCM_PWM_SC_T_DEF	Capacitive load charge (burst mode) PWM period for short circuit check at start	CR#5→CCM_PWM_SC_T	Fail-safe/Locked
CCM_PWM_SC_T_NB_DEF	Capacitive load charge (burst mode) max number of PWM pulses for short circuit check at start	CR#5→CCM_PWM_SC_T_NB	Fail-safe/Locked
CCM_TIMEOUT_DEF	Capacitive load charge (burst mode) maximum time duration	CR#5→CCM_TIMEOUT	Fail-safe/Locked

The default configuration is available in fail-safe/locked states for almost all parameters, with the following exceptions:

- BYPASS_CTL_DEF: it is used for setting bypass switch status in fail-safe and standby states, when NVM_DEF_CFG_EN is set (not in locked state).
- FS_MODE_DEF: it is used for setting output control configuration in fail-safe state only (not in locked state).
- DIN_CTRL_EN, DIN_CTRL_OPT: they are used to configure DIN use and its combination with software control in the locked state only (not in the fail-safe state).

10.1.1 NVM default configuration and output control mode in fail-safe

Considering the three different operation modes available in fail-safe, the availability of default configuration is meaningful in the cases shown by the following table:

Table 31. Device and output configuration options

Output control mode	RAM-based configuration FS_DEF_CFG_EN = 0	NVM-based configuration FS_DEF_CFG_EN = 1
OUTPUT DIN CONTROLLED (FS_MODE = 00/01)	YES	YES
OUTPUT LAST STATUS (FS_MODE = 10)	YES	YES
OUTPUT OFF (FS_MODE = 11)	YES	NO

10.1.2 NVM default configuration and RAM registers in fail-safe

If default configuration into NVM is enabled, by NVM_DEF_CFG_EN dedicated bit in NVM, and FS_MODE = 00/01 (DIN control on output), user write access to RAM registers is allowed in the fail-safe state, especially for programming configuration fields of Table 30. NVM mapped configuration parameters, to let the preparing device configuration for the unlocked state; those settings are stored but not effective until the fail-safe to unlocked transition occurs.

User write is not effective for the register field NVM_DEF_CFG_EN that is used only for related NVM bit setting during the NVM programming phase.

With FS_MODE = 10/11, all RAM registers are locked to write access, except for the following control bits:

- CR#→ EN
- CR#1→ GOSTBY
- CR#1→ FS_CFG_UPLOAD (not effective with NVM_DEF_CFG_EN = ‘0’)
- CR#3→ UNLOCK

10.1.3 NVM default configuration and RAM registers in locked

If default configuration into NVM is enabled, (NVM_DEF_CFG_EN = ‘1’), in the locked state the device is configured with fixed configuration parameters stored into NVM; user writes to RAM configuration registers fields of Table 30. NVM mapped configuration parameters is allowed, considering those settings are stored but is not effective until the locked to unlocked transition occurs. The other RAM control register fields not belonging to the NVM default configuration, mainly dedicated to output control, features activation triggering and specific device controls, is write accessible, giving the freedom to have full output control with fixed parameter settings. These registers fields are reported in the Table 32:

Table 32. Control register fields (not NVM mapped)

Register field	Description	Use
CR#1→OUTCTL	Output channel (external power switch) control	
CR#1→BYPASSCTL	Internal bypass switch control	
CR#1→S_T_START	Self-test start trigger	Effective only in the unlocked/self-test states
CR#1→S_T_STOP	Self-test stop trigger	
CR#1→S_T_CFG	Self-test type selection	
CR#1→EN	Unlocked state transition control	
CR#1→GOSTBY	Standby state transition control	
CR#1→CCM_CTRL_ON	Capacitive charge mode start trigger	
CR#1→CCM_CTRL_OFF	Capacitive charge mode stop trigger	
CR#1→locked_MODE_EN	Locked mode enable	
CR#1→FS_CFG_UPLOAD	NVM configuration upload to RAM registers	
CR#3→UNLOCK	Unlock access for specific control register fields	
CR#1,2,3,4,5→WD_TRIG	Watchdog monitor trigger	

If the NVM default configuration is not used (NVM_DEF_CFG_EN = '0'), the RAM configuration registers for NVM (Table 30. NVM mapped configuration parameters) is locked to prevent any unsafe changes to the device configuration while it is in a locked state. However, write access to the RAM control register fields in the device and output configuration options table is still allowed.

10.1.4 Default configuration upload to RAM

It is possible to upload default configuration from internal registers into correspondent RAM configuration registers, through a specific programmable control bit (NVM_DEF_CFG_UPLOAD, CR#1), to allow read access by the SPI interface of parameters default settings; the current content of RAM configuration registers is overwritten with default values stored internally.

This feature enables to:

- Configure the device in an unlocked state with a well-known, defined set of parameters, without the need to do that by a sequence of SPI frames.
- Monitor periodically the default configuration applied to the device while in fail-safe/locked states, to verify expected parameters settings have not been corrupted (safety purpose).

11 Protections

11.1 Battery undervoltage shutdown

The device is able to operate down to V_S = 6 V, with the charge pump still active. If the battery supply voltage V_S falls below the programmable undervoltage shutdown threshold, the device enters in battery undervoltage mode. The current sense diagnostic is not available. The charge pump, the output stage and the bypass switch are off regardless of the SPI status.

If V_S rises above the threshold (V_{S_USD} + $V_{S\_USD\_hys}$) the device returns to the last mode.

An undervoltage flag is set in the SPI register when $V_S < V_{S\_USD}$, and automatically reset when $V_S > V_{S\_USD} + V_{S\_USD\_hys}$.

11.2 Device overtemperature shutdown

The device temperature is internally monitored. An overtemperature shut-down of the device occurs when T_J exceeds T_{TSD}. The charge pump, the output stage and the bypass switch are off. A fault indication is given via SPI.

The device restarts when T_J decreases below T_{TSD} - T_{TSD_HYS}.

V_{TJ} is converted by a dedicated ADC converter. The converted result is stored in the Status register and can be read via SPI.

11.3 External MOSFET overtemperature shutdown

The external MOSFET temperature is monitored through a 10 kΩ NTC thermistor with one terminal connected to the Drain of the MOSFET, in order to allow optimal component placement.

R_{NTC} is part of a V_{BG} (V_{BG}= (V_{sense}N - VNTC_M); typ. 1.2 V) voltage divider through NTC and NTC_M pins:

$$V_{NTC} = \frac{V_{BG} \times R_{NTC}}{R_{T\_REF} + R_{NTC}} \quad (1)$$

V_{NTC} is converted by a dedicated ADC converter. The converted result is stored in the Status register and can be read via SPI.

An overtemperature shutdown of the MOSFET occurs when V_{NTC} voltage decreases under a preset threshold, see Table 20. The threshold can be set via SPI in the range from 100 °C to 150 °C in steps of 5 °C. In this case both output stages and bypass switch are turned off.

The MOSFET and the bypass switch are re-armed via SPI by clearing latched fault NTC_OVT bit.

This protection is not active in case of external MOSFET in OFF state.

11.4 External MOSFET desaturation shutdown

The external MOSFET drain-source voltage is monitored by the control IC. A desaturation shutdown of the MOSFET occurs when the V_{DS} exceeds the preset threshold. In this case both output stage and bypass switch are turned off. The threshold can be set via SPI in the range 0.3 V to 1.80 V in steps of 50 mV (default = 300 mV), see Table 17.

The MOSFET and bypass switch are re-armed via SPI by clearing latched fault VDS_MAX bit.

V_{DS} is converted by a dedicated ADC converter. The converted result is stored in the status register and can be read via SPI.

This protection is not active in case of external MOSFET in off state.

11.5 Hard short circuit latch-off

The external MOSFET drain-source current is monitored by the control IC through the current sense amplifier, which reads the voltage drop across a high-side shunt resistor. A hard short circuit shutdown of the MOSFET occurs when the current sense voltage exceeds the preset threshold. In this case, both output stage and bypass switch are turned off. The threshold can be set via SPI in the range from 20 mV to 160 mV, see Table 18 (the parameters showed in the table are referred to the SAR converter at 10 bit).

The MOSFET is re-armed via SPI by clearing the HSC latched fault bit.

V_{HSC} is converted by a dedicated ADC converter. The converted result is stored in the status register and can be read via SPI.

This protection is not active in case the external MOSFET is in OFF state.

11.6 I^2t vs time latch-off

The external MOSFET drain-source current is monitored by the control IC through the current sense amplifier, which reads the voltage drop across a high-side shunt resistor. The overload detection circuitry emulates the response of a traditional fuse. An overcurrent shutdown of the MOSFET occurs when the current sense voltage exceeds the preset threshold for longer than the preset time. In this case, both output stages and bypass switch are turned off. The threshold can be set via SPI in the range 6 mV to 90 mV, see the Table 19 (the parameters showed in the table are referred to the SAR converter at 10-bit), while the nominal trip time can be programmed in the range from 1 s to 511 s, (see timing: Table 50).

The MOSFET is re-armed via SPI by clearing the FUSE_LATCH latched fault bit. This protection is not active in case the external MOSFET is in OFF state.

In case of hard short protection event occurrence, reported by the HSC flag bit, the FUSE_LATCH bit is set as well.

11.7 Low current bypass desaturation shutdown

Internal bypass switch VDS voltage (VS - VOUT) is monitored by the IC, to protect the switch from load current sink changes.

A desaturation shutdown of the bypass occurs when its VDS exceeds a fixed threshold (VDS_BYPASS_SAT); in this situation, the bypass switch is turned off while the external FET is turned on through the HS_GATE output, directly by the hardware, regardless of their software controlled bit status, to protect the bypass and provide the requested current capability to the connected load.

This represents the so-called AUTO-ON event and it is flagged by bit #4 (AUTOON) of the global status byte that corresponds to the BYPASS_SAT flag of the Table 54. SR#1: status register 1; address 11h.

The bypass switch can be re-armed through SPI control by clearing the BYPASS_SAT fault latched bit.

This protection is not active in case the bypass switch is in the OFF state.

A particular case is represented by standby wake-up event occurrence. The FSM passes from the Standby state to the fail-safe state due to the bypass switch desaturation. In this situation, in addition to the shutdown of the bypass switch and the turn on of the external FET, the DIAG pin of the device is driven low. This, to advise the system of the autonomous woken up of the device, due to an hardware event (load current increase caused by the desaturation of the bypass switch).

It is important to notice that the bypass switch cannot be used to charge any type of load, even those requesting small currents capability. On the contrary, it shall be used to keep powered application loads, previously charged by external FET, when they switch to low-power consumption modes (that is, standby).

11.8 Current sense undervoltage (shutdown)

Voltage level of ISNS_P pin is monitored by the IC in order to detect an undervoltage condition due to battery drop. In this situation, IC is still able to work (if V_S is decoupled from V_{bat} by external components) but external FET monitoring circuitry could be affected if ISNS_P voltage falls below an internally defined threshold.

Thresholds voltage is derived by a configurable resistive divider.

Table 33. **Current sense undervoltage thresholds**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
CS_UV	Current sense undervoltage TH1 L2H	CS_UV = 00	2.78	2.87	3	V
	Current sense undervoltage TH1 H2L	CS_UV = 00	2.98	3.08	3.18	
$t_{CS\_UV\_DEGLITCH}$	Current sense fault deglitch filtering	HS_GATE ON	-10%	10	10%	µs
$t_{CS\_UV\_RETRY\_TIME}$	Current sense fault clear autoretry time	CR#3[23:22] = 00	-5%	100	5%	µs
		CR#3[23:22] = 01	-5%	250	5%	µs
		CR#3[23:22] = 10	-5%	500	5%	µs
		CR#3[23:22] = 11	-5%	1000	5%	µs

In case of fault detection, after a de-glitch filtering time of 10 µs , VNF1248F switches off the output, sets to 1 the proper status flag in SR#1 → CS_UV register bit (visible also by SPI GSB.DIAGS bit) and waits for a time, defined by CR#3→CS_UV_RETRY_T register field, before clearing the fault (status flag set to 0) and trying to restart again the output. If the fault is not detected (after another 10 µs filtering time elapse), output channel is kept on and device behaves as before fault occurrence, otherwise output channel is turned off again, fault is latched (SR#1 → CS_UV flag set, DIAG pin driven low) and VNF1248F waits for external intervention (by SPI command or DIN input) to clear fault and restart driving the external FET.

Protection is active when external FET is turned on.

11.9 Reverse battery and loss of ground

For 12 V applications, the external MOSFET is either switched off or remains off and the device protects itself in the event of a reverse battery connection or loss of ground (GND).

Note that an external component is required for reverse battery protection, as detailed in Table 63.

12 SPI functional description

12.1 SPI communication

The SPI communication is based on the “ST-SPI Specification”.

The device operates in slave mode on a bus configuration through CSN, SDI, SDO and SCK signal lines, with 32 bits SPI frames.

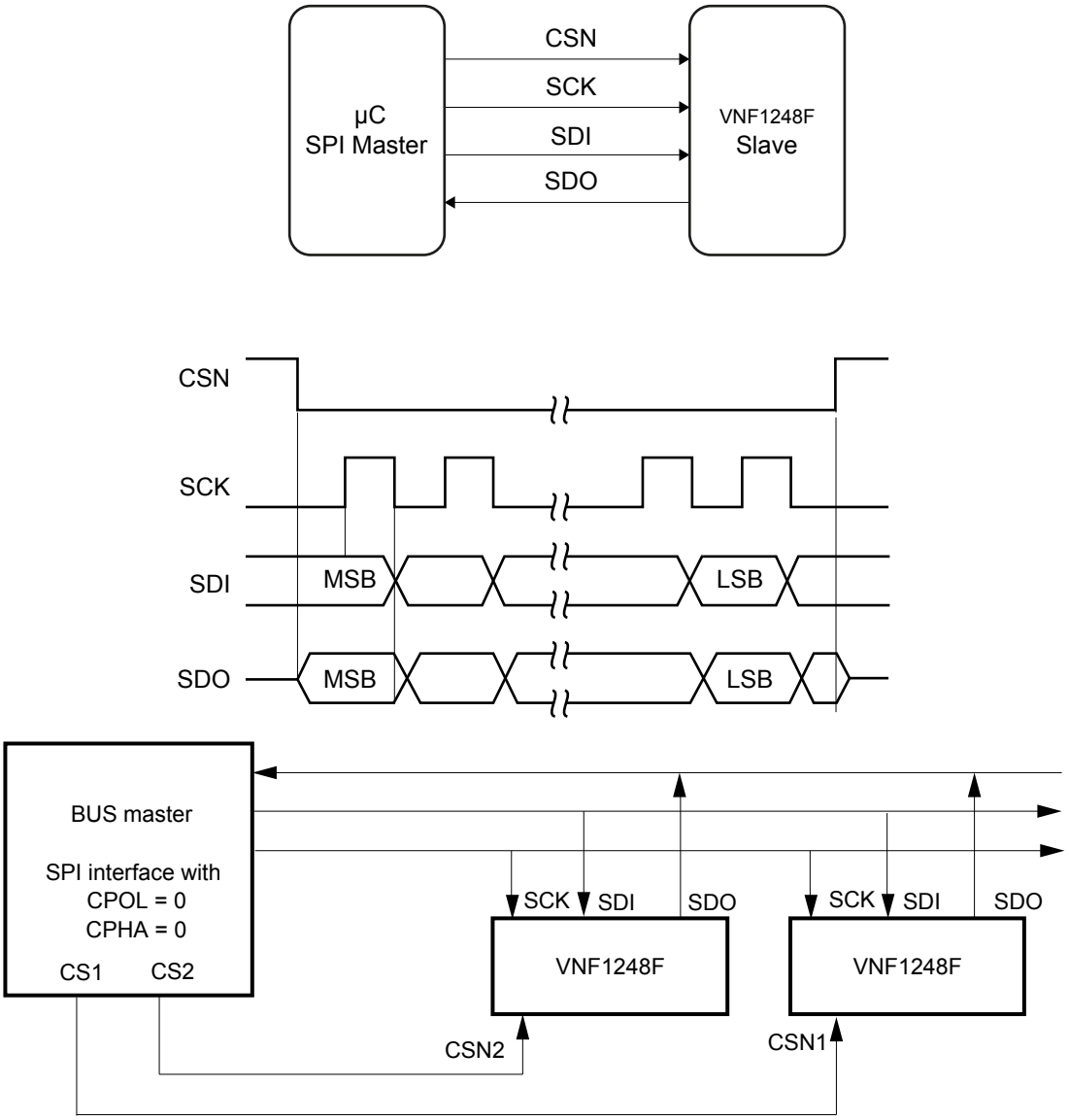
A SPI master device (host microcontroller) initiates the communication.

The SPI master device must be configured in the following mode:

CPOL = 0, CPHA = 0

Input data are shifted into SDI, MSB first while output data are shifted out on SDO, MSB first.

Figure 14. SPI functional diagram



12.2 Signal description

Serial clock SCK

This input signal provides the timing of the serial interface. Data present at Serial Data Input (SDI) are latched on the rising edge of Serial Clock (SCK). Data on Serial Data Output (SDO) change after the falling edge of Serial Clock (SCK).

Serial data input SDI

This input signal is used to transfer data serially into the device. It receives data to be written. Values are sampled on the rising edge of Serial Clock (SCK).

Serial data output SDO

This output signal is used to transfer data serially out of the device. Data are shifted out on the falling edge of Serial Clock (SCK).

Chip select CSN

The communication interface is deselected, when this input signal is logically high. A falling edge on CSN enables and starts the communication while a rising edge finishes the communication and the sent command is executed when a valid frame was sent. During communication start and stop the Serial Clock (SCK) has to be logically low.

12.3 SPI protocol

SDI format during each communication frame starts with a command byte. It begins with two bits of operating code (OC1, OC0) which specify the type of operation (read, write, read and clear status, read device information) and it is followed by a 6-bit address (A5:A0). The command byte is followed by three input data bytes: (D23:D16), (D15:D8) and (D7:D0).

Table 34. Command byte

MSB							LSB
OC1	OC0	A5	A4	A3	A2	A1	A0

Table 35. Input data byte 1

MSB							LSB
D23	D22	D21	D20	D19	D18	D17	D16

Table 36. Input data byte 2

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 37. Input data byte 3

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

Table 38. Global status byte

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

SDO format during each communication frame starts with a specific byte called Global Status Byte (see GSB byte for more details on bit0–bit7). This byte is followed by three output data bytes (D23:D16), (D15:D8) and (D7:D0).

Table 39. **Output data byte 1**

MSB							LSB
D23	D22	D21	D20	D19	D18	D17	D16

Table 40. **Output data byte 2**

MSB							LSB
D15	D14	D13	D12	D11	D10	D9	D8

Table 41. **Output data byte 3**

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

12.4 Operating code definition

The SPI interface features four different addressing modes which are listed in Table 42.

Table 42. **Operating codes**

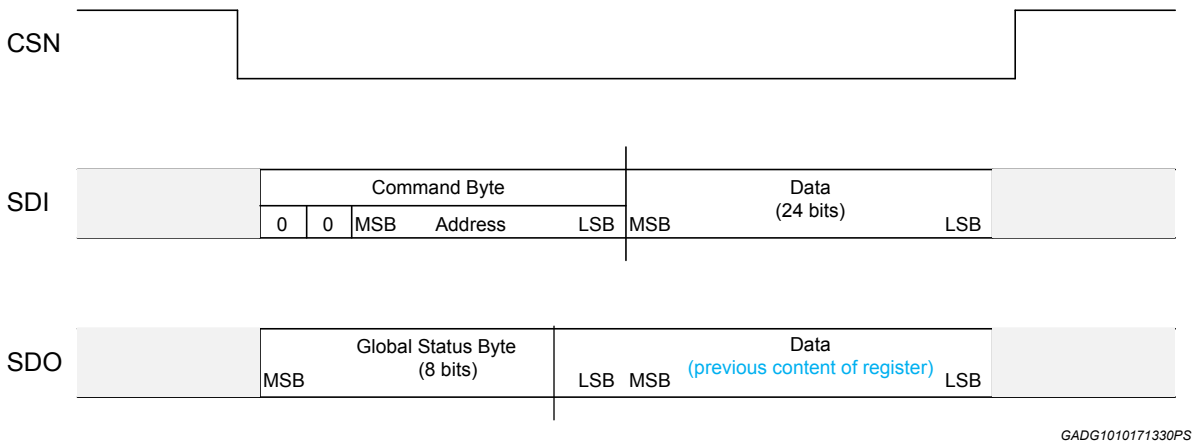
OC1	OC0	Meaning
0	0	Write operation
0	1	Read operation
1	0	Read and clear status operation
1	1	Read device information

12.5 Write mode

The write mode of the device allows writing the content of the input data byte into the addressed register (see list of the registers in Table 47. RAM memory map). The incoming datum is sampled on the rising edge of the serial clock (SCK), MSB first.

During the same sequence, the outgoing datum is shifted out MSB first on the falling edge of the CSN pin and subsequent bits on the falling edge of the serial clock (SCK). The first byte corresponds to the global status byte, the second, third and forth bytes to the previous content of the addressed register. Unused bits are always read as 0.

Figure 15. **SPI write operation**



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12.6 Read mode

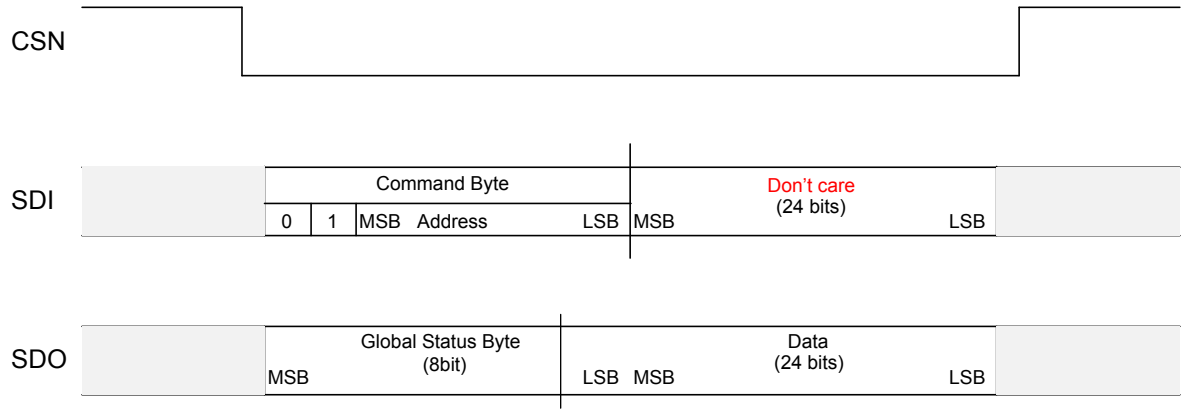
The read mode of the device allows to read and to check the state of any registers.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status Byte, second, third and forth byte to the content of the addressed register.Unused bits will be always read as 0.

In order to avoid inconsistency between the Global Status byte and the Status register, the Status register contents are frozen during SPI communication.

Figure 16. SPI read operation



12.7 Read and clear status command

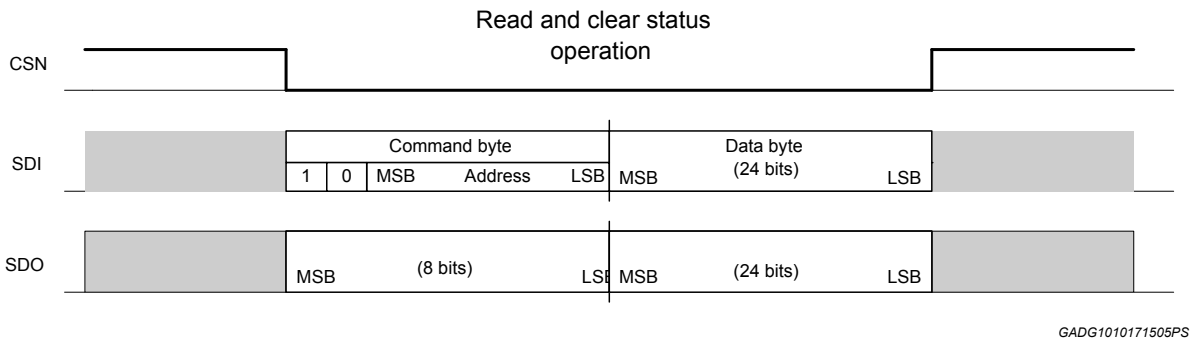
The read and clear status operation is used to clear the content of the addressed status register (see Table 47. RAM memory map). A read and clear status operation with address 0x3Fh clears all Status registers simultaneously.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which register content is read and the payload bits set to 1 into the data byte determine the bits into the register which have to be cleared.

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte, second, third and forth byte to the content of the addressed register. Unused bits will be always read as 0.

In order to avoid inconsistency between the Global Status byte and the Status register, the Status register contents are frozen during SPI communication.

Figure 17. SPI read and clear operation



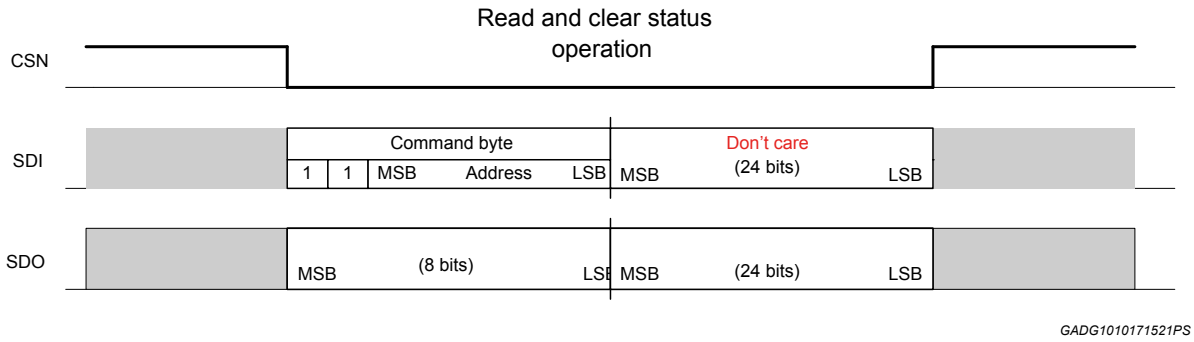
12.8 SPI device information

Specific information can be read but not modified during this mode.

Incoming data are sampled on the rising edge of the serial clock (SCK), MSB first. The command byte allows to determine which information is read, whilst the other three data bytes are "don't care".

Outgoing data are shifted out MSB first on the falling edge of the CSN pin and others on the falling edge of the serial clock (SCK). The first byte corresponds to the Global Status byte, second byte to the content of the addressed register, third and forth bytes are 0x00.

Figure 18. SPI read device information



12.9 Special commands

0xFF - SWReset: sets all control registers to default and clears all status register

An Opcode '11' (read device information) addressed at '111111' forces a Software Reset of the device, second, third and forth bytes are "don't care" provided that at least one bit is zero.

Note: In the case of an OpCode '11' at address '111111' with data field equal to '1111111111111111' the SPI frame is recognized as a frame error and SPIE bit of GSB is set.

Table 43. 0xFF: (SW_Reset)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
1	1	1	1	1	1	1	1
DATA1	X(1)	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA3	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

1. *X: do not care*

0xBF - Clear all status registers (RAM access)

When an OpCode '10' (read and clear operation) at address b'111111 is performed.

Table 44. Clear all status registers (RAM access)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command							
OC1	OC0	Address					
1	0	1	1	1	1	1	1
DATA1	X(1)	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA2	X	X	X	X	X	X	X
	0	0	0	0	0	0	0
DATA3	X	X	X	X	X	X	X
	0	0	0	0	0	0	0

1. *X: do not care*

12.10 Global status byte

As per the ST SPI 4.1 specification, the device features an in-frame response mechanism.

A global status byte is transmitted to the SPI master on the SDO line while the command byte is received on the SDI line.

The global status byte reports the global status of the device:

Table 45. Global status byte

MSB	30	29	28	27	26	25	LSB
GSBN	RSTB	SPIE	AUTOON	DIAGS	DE	OVC	FS

Table 46. Global status byte - Bit description

Bit #	Name	Description
31	GSBN	**Global status bit NOT** This bit is a NOR combination of the remaining bits of this register: GSBN = NOT (RSTB or SPIE or AUTOON or DIAGS or DE or OVC or FS) This bit can also be used as the global status flag without starting a complete communication frame as it is present directly after pulling CSN low.
30	RSTB	**Reset bit** The RSTB indicates a device hardware reset. This bit is set in power-on mode. All internal control registers are set to default and kept in that state until the bit is automatically cleared by the first valid SPI communication.
29	SPIE	**SPI error** The SPIE is a logical OR combination of errors related to a wrong SPI communication: SDI stuck-at fault, SPI frame length ≠ 32 bit (wrong number of clock pulses while CSN is low), parity check error
28	AUTOON	**AUTOON** The AUTOON indicates the automatic turn-on of the external FET due to low current bypass desaturation (BYPASS_SAT = 1) when its V_{DS} exceeds a fixed threshold (VDS_BYPASS_SAT). AUTOON = BYPASS_SAT
27	DIAGS	**Diagnostic signal bit** The DIAGS is a logical OR combination of all faults, which cause the external FET to be switched off DIAGS = VS_UV or HSC or VDS_MAX or FUSE_LATCH or DEV_OVT or NTC_OVT or VGS_LOW or DIS_OUT_FAULT or CS_UV
26	DE	**Device error bit**

Bit #	Name	Description
		The DE is a logical OR combination of errors related to device specific blocks: charge pump output undervoltage, NVM download failure. DE = CP_LOW or NVM_FAIL
25	OVC	**Overcurrent bit** The OVC is a 'real-time' bit indicating an overcurrent event (programmed $V_{OC\_THRS\_X}$ overcome)
24	FS	**Fail-safe** If the FS bit is set, the device was forced into a safe state. This bit is set in the fail-safe state (SR#1.FAILSAFE_ST = 1) FS = FAILSAFE_ST

12.11 RAM memory map

Table 47. RAM memory map

Address	Name	Access	Content
01h	Control register 1	R/W	CR#1: 1st control register (CONTROLS)
02h	Control register 2	R/W	CR#2: 2nd control register (CONFIG 1)
03h	Control register 3	R/W	CR#3: 3rd control register (CONFIG 2)
04h	Control register 4	R/W	CR#4: 4th control register (NVM Programming)
05h	Control register 5	R/W	CR#5: 5th control register (CCM Configuration)
06h : 10h	...	R	Reserved
11h	Status register 1	R/C	SR#1: 1st status register (DIAGNOSTICS + PROTECTIONS)
12h	Status register 2	R	SR#2: 2nd status register (CURRENT SENSE + NVM PROGRAMMING STATUS)
13h	Status register 3	R	SR#3: 3rd status register (NTC + TJ)
14h	Status register 4	R	SR#4: 4th status register (VOUT + VDS)
15h	Status register 5	R/C	SR#5: 5th status register (SELFTEST VDS)
16h	Status register 6	R/C	SR#6: 6th status register (SELFTEST STUCK ON)
17h	Status register 7	R/C	SR#7: 7th status register (SELFTEST CURRENT SENSE)
18h	Status register 8	R	SR#8: 8th status register (HSC)
19h	...	R	Reserved
Reserved			
3Fh	Advanced Operation Code	C	A R&C operation to this address causes all status registers to be cleared

12.12 ROM memory map

Table 48. **ROM memory map**

Address	Name	Access	Content (hex)	Description
00h	Company code	R	00h	Indicates the code of STMicroelectronics company
01h	Device family	R	01h	Indicates the product family
02h	Device N. 1	R	55h	Indicates the first code of the product
03h	Device N. 2	R	52h	Indicates the second code of the product
04h	Device N. 3	R	07h	Indicates the third code of the product
05h	Device N. 4	R	4Ah	Indicates the fourth code of the product
0Ah	Silicon version	R	02h	Related silicon version
10h	SPI mode	R	31h	Bit7 = 0, burst read is disabled SPI data length = 32 bits Bit6, DL2 = 0 Bit5, DL1 = 1 Bit4, DL0 = 1 Bit3, SPI8 = 0: 8-bit frame option not available Bit2 = 0 Parity check is used Bit1, S1= 0 Bit0, S0 = 1
11h	WD type 1	R	4Ah	A WD is implemented Bit7, WD1 = 0 Bit6, WD0 = 1 WD period 50 ms = 10*5ms -> WT[5:0] = 0xA Bit5, WT5 = 0 Bit4, WT4 = 0 Bit3, WT3 = 1 Bit2, WT2 = 0 Bit1, WT1 = 1 Bit0, WT0 = 0
13h	WD bit pos. 1	R	43h	Bit7,WB1 = 0 Bit6,WB2 = 1 WBA[5-0], Bit[5-0] = address of the config. register, where the WD bit is located = 03h = 000011b
14h	WD bit pos. 2	R	C1h	Bit7,WB1 = 1 Bit6,WB0 = 1 Bit position of the WD bit within the corresponding configuration register = 01d = 000001b
3Fh	Advanced operation code	R	00h	Access to this address triggers a SW reset (all control registers are set to their default values; in addition, all status registers are cleared too).(1)

1. *Data field should not be “all ones”, otherwise an “SDI stuck at” error occurs.*

12.13 Control registers

Table 49. **CR#1: control register 1 (read/write); address 01h**

Bit	Default	Name	Description
23	0	AUTO_ON_DIS	Control bit to disable external FET automatic turn-on in case of bypass switch saturation fault; in this case the DIAG pin will be driven low. Specific for customer application test mode ('Hot plug-in'). Access to this field is allowed after the UNLOCK bit set to 1.
22:21		Unused	
20	0	LOCKED_MODE_EN	Control bit needed to: - Enable locked state entry in case of HWLO = 1 or EN = 0 events occurrence in unlocked state - Enable/Disable write access to control register fields in the locked state
19	0	CCM_CTRL_OFF	Trigger to stop CCM burst mode in unlocked/locked state
18	0	CCM_CTRL_ON	Trigger bit to start CCM burst mode in unlocked/locked state
17	0	NVM_DEF_CFG_UPLOAD	Trigger bit to upload NVM default configuration into correspondent RAM configuration register fields (RAM overwrite)
16	0	NVM_DEF_CFG_EN	Control bit to allow reading/writing of correspondent NVM bit (through NVM access procedure) for NVM default configuration enabling in fail-safe/locked states NVM bit = 1: fail-safe/locked parameters setting depending on values stored into the NVM NVM bit = 0: fail-safe/locked parameters setting depending on values stored into RAM registers Access to this bit is allowed after UNLOCK bit set to 1
15:14	0x0	FS_MODE	Fail-safe state behavior configuration (see Section 6.4: Fail-safe state) Access to this field is allowed after the UNLOCK bit set to 1
13	0	DIN_CTRL_OPT	Unlocked state DIN control behavior configuration (see Section 6.2: Unlocked state) Access to this bit is allowed after UNLOCK bit set to 1
12	0	DIN_CTRL_EN	Unlocked state DIN control enable Access to this bit is allowed after UNLOCK bit set to 1
11	0	GOSTBY	GOSTBY can be set to 1 only if UNLOCK = 1; in other words, trying to set this bit to 1 when UNLOCK = 0 will have no effects and it maintains its previous value. GOSTBY can be reset to 0 also when UNLOCK = 0. To set standby mode it is necessary to send two consecutive SPI frames, as follows: 1st SPI write operation to set UNLOCK bit to 1 2nd SPI write operation to set GOSTBY bit to 1 and EN bit to 0
10	0	EN	EN can be set to 1 only if UNLOCK = 1; in other words, trying to set this bit to 1 when UNLOCK = 0 will have no effects and it maintains its previous value. EN can be reset to 0 also when UNLOCK = 0. To set the EN bit and move the device from fail-safe/locked to unlocked state, it is necessary to send two consecutive SPI frames as follows: 1st SPI write operation to set UNLOCK bit to 1 2nd SPI write operation to set GOSTBY bit to 0 and EN bit to 1
9	0	S_T_START	When it is set to 1, starts selected-test.

Bit	Default	Name	Description
			If the current state is unlocked and S_T_CFG is not 000, then setting this bit causes a transition to -test state. This bit is automatically reset.
8	0	S_T_STOP	When it is set to 1, stops execution of the selected-test (when it is applicable). This bit is automatically reset.
7:5	0x0	S_T_CFG	Test selection: 000: No selection 001: Current sense 010: VDS detection 100: Power switch stuck-on 011: Current sense + VDS detection 101: Current sense + power switch stuck-on 110: VDS detection + power switch stuckon 111: Current sense + VDS detection + power switch stuck-on Others: Reserved
4	0	OUTCTL	Enables high-side through SPI [1]: HS gate driver commanded on [0]: HS gate driver commanded off
3	0	BYPASSCTL	Enables low current bypass through SPI: [1]: LCB commanded on [0]: LCB commanded off
2	0	Reserved	
1	0	WD_TRIG	Mirror of WD_TRIG bit
0	1	Parity bit	Odd parity bit check

Table 50. CR#2: control register 2 (read/write); address 02h

Bit	Default	Name	Description
23 ÷ 16	00000000	T_NOM	Configures the value of nominal time required for the fuse emulation: t_{NOM} (s) = b{T_NOM(7:0), 1} T_NOM_{min} = 00000000 → t_{NOM} (s) = b000000001 = 1 s T_NOM_{max} = 11111111 → t_{NOM} (s) = b111111111 = 511 s The nominal time corresponds to the trip time obtained when the current is equal to the nominal overcurrent threshold (OVC_THR).
15 ÷ 11	00000	OVC _THR	Configures the value of the nominal overcurrent threshold. The threshold can be set in the range 6 mV to 90 mV See Table 19. Overcurrent protection.
10 ÷ 7	0000	HSC_THR	Configures a threshold for hard short circuit latch-off. The threshold can be set in the range from 20 mV to 160 mV. See Table 18. Hard short circuit protection with integrated 10-bit ADC.
6 ÷ 2	00000	VDS_THRS	Configures a threshold for external MOSFET desaturation shut-down. The threshold can be set in the range from 0.3 V to 1.80 V in steps of 50 mV (default = 300 mV). Configuration 0x1F is reserved.
1	0	WD_TRIG	Mirror of WD_TRIG bit
0		Parity bit	Odd parity bit check

Table 51. CR#3: control register 3 (read/write); address 03h

Bit	Default	Name	Description
23:22	0x0	CS_UV_RETRY_T	Current sense undervoltage fault clear auto retry time (only once) 00: 100 µs 01: 250 µs 10: 500 µs 11: 1 ms
21:20	0x0	Reserved	
19:18	0x0	CCM_PWM_TON_MF	Capacitive charge mode PWM ton multiplying factor 00: T_{on} x1 01: T_{on} x2 10: T_{on} x4 11: T_{on} x8
17	0x0	Reserved	
16:14	0x0	CCM_VOUT_THR	Capacitive charge mode V_{OUT} threshold selection 000: 1 V 001: 2 V 010: 3 V 011: 4 V 1xx: 5 V
13:12	0x0	Reserved	
11:10	0x0	UV_THR	V_S supply undervoltage threshold selection 0x: V_{S_USD1} 10: V_{S_USD2} 11: V_{S_USD3}
9	0	UNLOCK	[0]: bits GOSTBY, EN cannot be set to 1 but can be reset; [1]: bits GOSTBY, EN can be set to 1, but only with the next valid SPI frame. When UNLOCK = 1, it is automatically reset with the next valid SPI frame.
8:5	0x0	NTC_THR	Configures a threshold for external MOSFET overtemperature shutdown. The threshold can be set in the range [110.92 : 37.50] mV.
4:3	0x0	WD_TIME	00: t_{WD} = 50 ms 01: t_{WD} = 100 ms 10: t_{WD} = 150 ms 11: t_{WD} = 200 ms
2	0	Reserved	
1	0	WD_TRIG	To keep the device in the unlocked state, this bit must be cyclically toggled within a period equal to t_{WD} to refresh the watchdog.
0	1	Parity bit	Odd parity bit check

Table 52. CR#4: control register 4 (read/write); address 04h

Bit	Default	Name	Description
Register function 1			
23:2	0x0	NVM_CTM_ACCESS_KEY	A specific word (0x105B96) to be written to have access to NVM programming control bits

Bit	Default	Name	Description
			Access to this field is allowed only after the UNLOCK bit is set to ‘1’
1	0	WD_TRIG	Mirror of WD_TRIG bit
0	1	Parity bit	Odd parity bit check
Register function 2: the following fields are enabled only if function 1 has been executed successfully			
23:12	0x0	Reserved	
11:8	0x0	NVM_ADDR	Address of NVM sector to be accessed. Only address 0x5 is available to customer access.
7:4	0x0	Reserved	
3	0	NVM_WR_EN	NVM operation type: 1: NVM sector data programming/write 0: NVM sector data read
2	0	NVM_OP_START	Trigger bit to start NVM operation Write-only, read always 0
1	0	WD_TRIG	Mirror of WD_TRIG bit
0	1	Parity bit	Odd parity bit check

Table 53. CR#5: control register 5 (read/write); address 05h

Bit	Default	Name	Description
23:22	0x0	CCM_TIMEOUT	Capacitive load charge (burst mode) maximum time duration: 00: 200 ms 01: 250 ms 10: 300 ms 11: 400 ms
21:17	0x0	CCM_PWM_SC_T_NB	Capacitive load charge (burst mode) maximum number of lower frequency PWM pulses for short circuit check (start phase) Range: 5 to 50 pulses, variable step (refer to the Table 28.)
16:14	0x0	CCM_PWM_SC_T	Capacitive load charge (burst mode) time duration of PWM period during short circuit check (start phase) 000: 2.0 ms 001: 2.5 ms 010: 3.0 ms 011: 3.5 ms 1 - -: 4.0 ms
13:8	0x0	CCM_PWM_TON	Capacitive load charge (burst mode) PWM Ton setting Range: 1 to 50 µs, variable step (refer to the Table 27) 0x0 configuration: high-side driver controlled by protection only (hard short, fuse latch)
7:2	0x0	CCM_PWM_T	Capacitive load charge (burst mode) PWM period during standard phase Range: 50 to 4000 µs (refer to the Table 29)
1	0	WD_TRIG	Mirror of WD_TRIG bit
0	1	Parity bit	Odd parity bit check

12.14 Status registers

Table 54. SR#1: status register 1; address 11h

Bit	Default	Name	Description	Access
23:22	0x0	CCM_STATUS	Capacitive load charge burst mode operation status: 00 → IDLE: CCM operation not started 01 → RUN: CCM operation started running 10 → CHARGED: CCM operation completed successfully 11 → CHARGE INCOMPLETE: CCM operation aborted (timeout/short circuit)	R/C
21	0	CS_UV	Current sense (ISense_P) undervoltage bit Set if I_{sense_P} voltage falls below the internally configured current sense undervoltage threshold. It is reset: 1. in Fail-safe state if FS_MODE = `00'/`01' AND DIN falling edge occur. 2. in Unlocked/Locked state if DIN_CTRL_EN = 1 AND DIN falling edge occur.	R/C
20	0	EXT_REG_ON	The EXT_REG_ON bit is "0" by default; it is latched to `1' if the V_{EXT_LDO} > $V_{EXT\_LDO\_H}$, (the device is automatically powered by the external regulator) and reset when a power-on or a standby state occurs (internal supply node powered by internal LDO regulator).	R
19	0	DIN_ST	DIN input status flag bit	R
18	0	DIS_OUT_FAULT	Disable output fault: this bit is set during a transition to fail-safe state when CR#1_FS_MODE = “11”. When it is set, both the high-side and bypass are switched off.	R/C
17	0	SELFTEST_STATE	FSM SELF-TEST state flag bit	R
16	0	OUT_ST	High-side gate driver status bit [1]: HS gate driver turned on [0]: HS gate driver turned off	R
15	0	BYPASS_ST	Low current bypass status bit [1]: LCB turned on [0]: LCB turned off	R
14	0	LOCKED_STATE	FSM LOCKED state flag bit	R
13	0	FAILSAFE_STATE	FSM fail-safe state flag bit	R
12	0	HWLO_ST	HWLO mirror bit	R
11	0	VS_UV	VS undervoltage “real-time” bit [0] VS > V_{S,UV_H} [1] VS ≤ V_{S,UV_L} If the battery supply voltage VS falls below the undervoltage shutdown threshold, then the HS gate driver, bypass, and charge pump are switched off.	R
10	0	HSC	Hard short circuit latch-off: a hard short circuit shut-down of the MOSFET (HSC = 1) occurs when the current sense voltage exceeds the preset threshold. When it happens, the bypass is switched off as well. The MOSFET is re via SPI.	R/C
9	0	VDS_MAX	External MOSFET desaturation shut-down: a desaturation shut down of the MOSFET (V_{DS_MAX} = 1) occurs if the VDS exceeds the preset threshold when HS is in on-state after a preset blanking time. When it happens, the bypass is switched off as well. The MOSFET is rearmed via SPI.	R/C

Bit	Default	Name	Description	Access
			It is reset: 1. in Fail-safe state if FS_MODE = `00'/`01' AND DIN falling edge occur. 2. in Unlocked/Locked state if DIN_CTRL_EN = 1 AND DIN falling edge occur.	
8	0	BYPASS_SAT	Low current bypass desaturation shut-down: a desaturation shut down of the low current bypass (BYPASS_SAT = 1) occurs if the VDS exceeds the preset threshold when HS is in off-state and the bypass is in on-state. When BYPASS_SAT = 1 external MOSFET is automatically commanded on, independently on OUTCTL. This bit is reset if a DIN rising edge occurs. The low current bypass is re-armed via SPI. This bit is also set to 1 correspondingly to the transition from wake-up to unlocked mode.	R/C
7	0	FUSE_LATCH	Current vs time latch-off: an overcurrent shut down of the MOSFET (FUSE_LATCH = 1) occurs when the current sense voltage exceeds the preset threshold for longer than the preset time (I^2-t curve emulating a traditional fuse). When it happens, the bypass is switched off as well. The MOSFET is rearmed via SPI. It is reset: 1. in Fail-safe state if FS_MODE = `00'/`01' AND DIN falling edge occur. 2. in Unlocked/Locked state if DIN_CTRL_EN = 1 AND DIN falling edge occur.	R/C
6	0	OVC	Overcurrent warning: an overcurrent warning (OVC = 1) occurs even when the current sense voltage exceeds the preset threshold for a time not longer than the preset time. This is a “real-time” bit.	R
5	0	DEV_OVT	Overtemperature shut-down (“real-time” bit). When it is set to 1, the high side, bypass, and charge pump are switched off.	R
4	0	NTC_OVT	External MOS overtemperature: this bit is set when NTC is lower than NTC_THR for more than a certain deglitch time. When it happens, the bypass is switched off as well. The MOSFET is rearmed via SPI. It is reset: 1. in Fail-safe state if FS_MODE = `00'/`01' AND DIN falling edge occur. 2. in Unlocked/Locked state if DIN_CTRL_EN = 1 AND DIN falling edge occur.	R/C
3	0	VGS_LOW	This bit is set in on-state when V_{GS} falls below $V_{GS\_UVLO\_*V}$ for more than $V_{G\_UVLO\_DEGLITCH}$ time (8us typ). When this bit is set, the external FET is switched off. It is reset: 1. in Fail-safe state if FS_MODE = `00'/`01' AND DIN falling edge occur. 2. in Unlocked/Locked state if DIN_CTRL_EN = 1 AND DIN falling edge occur.	R/C
2	0	CP_LOW	This bit is set when VCP falls below V_{CP_low} threshold (V_S + 5 V) for more than t_{CP_RISE} (60us typ). When this bit is set, the external FET driver is disabled. This is a “real-time” bit.	R
1	0	WD_FAIL	Watchdog failure bit: [0]: watchdog OK; [1]: watchdog failure in unlocked/locked/self-test state When this bit is set, the device moves to the fail-safe state.	R/C
0		Parity bit	ODD parity bit check	

Table 55. SR#2: status register 2; address 12h

Bit	Default	Name	Description	Access
23	0	Unused		R
22÷17	0x0	NVM_FAIL	Status of NVM download into RAM and internal registers bit = '1' --> correspondent NVM row download failed (parity err.) bit = '0' --> correspondent NVM row downloaded correctly	R/C
16÷15	0x0	NVM_OP_STATUS	NVM Read/Write operation status 00 --> IDLE: NVM operation not started 01 --> RUN: NVM operation started running 10 --> END: NVM operation completed successfully 11 --> ABORT: NVM operation aborted (wrong sector access)	R/C
14÷2	0x000	CURR_SENSE	13-bit ADC conversion related to current sense amplifier, ranging from 0V to 160 mV; unidirectional current through an external sense resistor.	R
1	0	UPDT_CURR	Updated status bit. This bit is set when the value is updated and cleared when the register is read.	R
0	1	Parity bit	ODD parity bit check	

Table 56. SR#3: status register 3; address 13h

Bit	Default	Name	Description	Access
23		Unused		
22 ÷ 13	0000000000	TJ	10-bit ADC conversion related to TJ (device temperature)	R
12	0	UPDT_TJ	Updated status bit. This bit is set when the value is updated and cleared when the register is read.	R
11 ÷ 2	0000000000	NTC	10-bit ADC conversion related to NTC (External MOSFET temperature sensing through an external NTC resistor)	R
1	0	UPDT_NTC	Updated status bit. This bit is set when the value is updated and cleared when the register is read.	R
0		Parity bit	ODD parity bit check	

Table 57. SR#4: status register 4; address 14h

Bit	Default	Name	Description	Access
23 ÷ 12		Unused		
22 ÷ 13	0000000000	VDS	10-bit ADC conversion of the voltage across the HS switch (VS-OUT). This register is not refreshed during VDS self-test execution.	R
12	0	UPDT_VDS	Updated status bit. This bit is set when the value is updated and cleared when the register is read.	R
11 ÷ 2	0000000000	VOUT	10-bit ADC conversion of the OUT pin	R
1	0	UPDT_VOUT	Updated status bit. This bit is set when the value is updated and cleared when the register is read.	R
0		Parity bit	ODD parity bit check	

Table 58. SR#5: status register 5; address 15h

Bit	Default	Name	Description	Access
23 ÷ 14		Unused		
13		S_T_VDS_MAX1	This bit is set if VDS_THRS is reached during VDS self-test.	R/C

Bit	Default	Name	Description	Access
12 ÷ 3	0000000000	S_T_VDS	Difference between 10-bit ADC conversion of the VDS, performed during VDS self-test and content of the VDS register latched during self-test execution.	R/C
2 ÷ 1	00	S_T_VDS_STATUS	Status of VDS self-test 00: IDLE: Self-test not started 01: RUN: Self-test execution in progress 10: END: Self-test completed successfully (consistent data available on dedicated registers) 11: ABORT: Self-test aborted (watchdog timeout, HWLO, S_T_STOP when not required)	R/C
0		Parity bit	ODD parity bit check	

Table 59. SR#6: status register 6; address 16h

Bit	Default	Name	Description	Access
23 ÷ 15		Unused		
14	0	UPDT_S_T_STUCK	Updated status bit. This bit is set when the value is updated and cleared when the register is read.	R/C
13	0	S_T_VDS _MAX2	This bit is set if VDS_THRS is reached during STUCK ON self-test.	R/C
12 ÷ 3	0000000000	S_T_STUCK	10-bit ADC conversion of the VDS, performed during STUCK ON self-test	R/C
2 ÷ 1	00	S_T_STUCK_STATUS	Status of STUCK _ON self-test 00: IDLE: Self-test not started 01: RUN: Self-test execution in progress 10: END: Self-test completed successfully (consistent data available on dedicated registers) 11: ABORT: Self-test aborted (watchdog timeout, HWLO, S_T_STOP when not required)	R/C
0		Parity bit	ODD parity bit check	

Table 60. SR#7: status register 7; address 17h

Bit	Default	Name	Description	Access
23 ÷ 15		Unused		
14	0	S_T_HSC	This bit is set if HSC_THR is reached during the CURRENT SENSE self-test.	R/C
13	0	S_T_OVC	This bit is set if OVC_THR is reached during the CURRENT SENSE self-test.	R/C
12 ÷ 3	0000000000	S_T_CURR	Difference between 10-bit ADC conversion of the CURRENT SENSE, performed during CURRENT SENSE self-test and content of the HSC_SAR register latched during self-test execution.	R/C
2 ÷ 1	00	S_T_CURR_STATUS	Status of current sense self-test 00: IDLE: Self-test not started 01: RUN: Self-test execution in progress 10: END: Self-test completed successfully (consistent data available on dedicated registers) 11: ABORT: Self-test aborted (watchdog timeout, HWLO, S_T_STOP when not required)	R/C
0		Parity bit	ODD parity bit check	

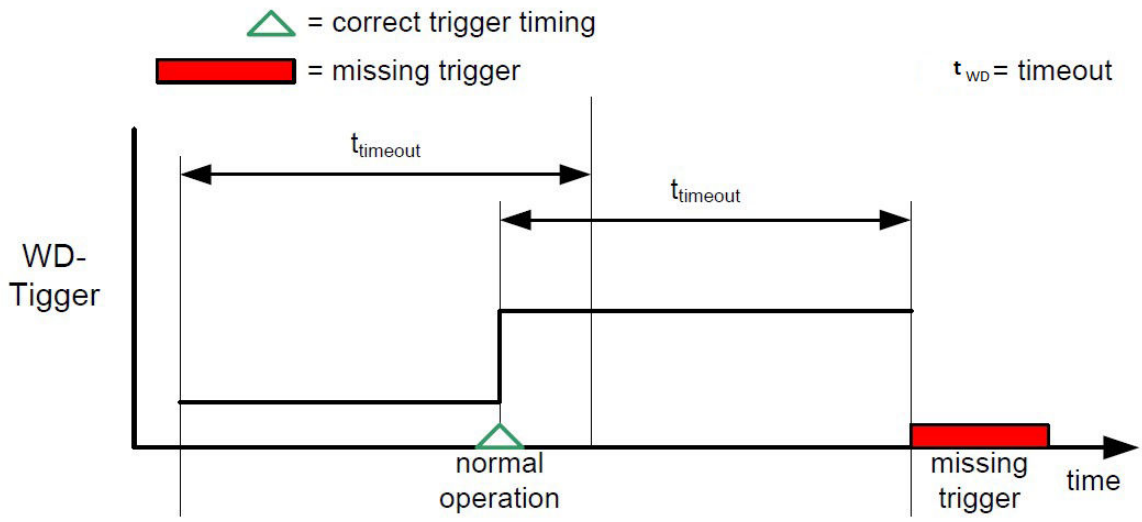
Table 61. SR#8: status register 8; address 18h

Bit	Default	Name	Description	Access
23:22	0x0	Unused		R
21:12	0x0	NVM_PROG_CNT	Total number of programming cycles performed on NVM customer dedicated sector	R
11:2	0x000	HSC_SAR	10-bit ADC SAR conversion related to the current sense amplifier, ranging from 0 V to 160 mV; unidirectional current through an external sense resistor.	R
1	0	UPDT_HSC	Updated status bit. This bit is set when the value is updated and cleared when the register is read.	R
0	1	Parity bit	ODD parity bit check	R

12.15 Watchdog timeout

In order to serve the timeout watchdog, the relevant WD_TRIG bit (Watchdog Trigger bit) must be toggled within a given timeout window.

Figure 19. Timeout watchdog



13 Functional description

This functionality is managed by the 6-states based FSM, to distinguish between initial phase, after power-on reset, low power status, active status (user full control), locked status (user output control, device configuration locked), safe (limp-home) status, and autodiagnostic phase. Main control supports three different wake-up sources from low power state and automatic FET turn-on (active standby feature).

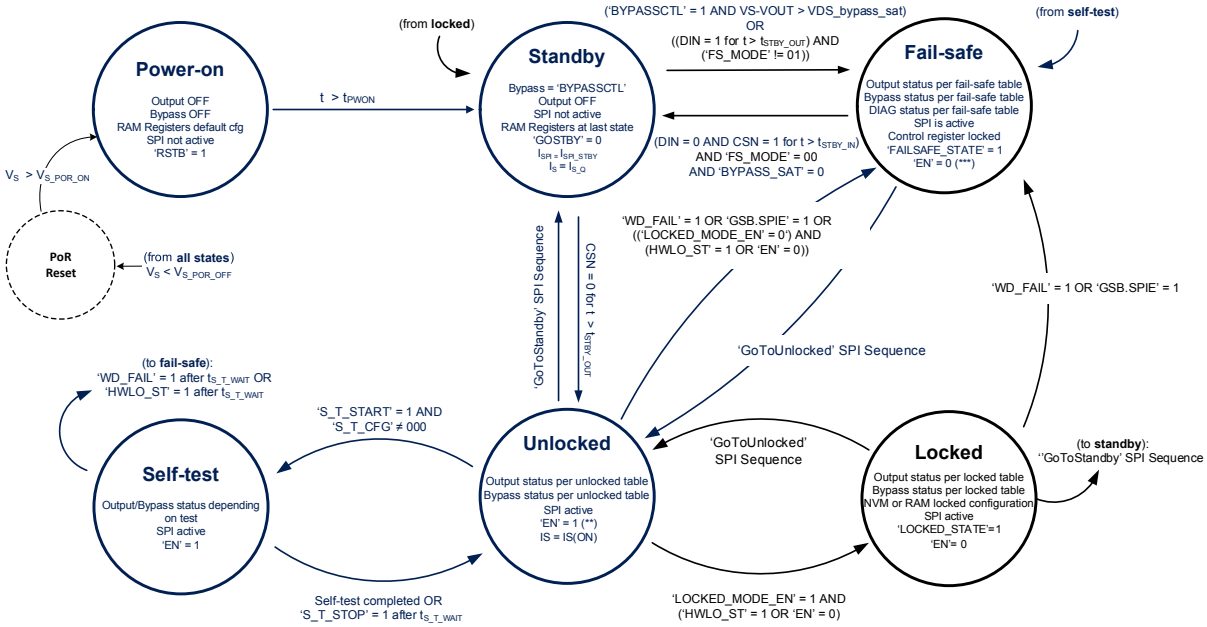
The device state diagram is shown in the next figure.

13.1 Operating modes

The device can operate in the following different modes:

- Power-on mode
- Standby mode
- Fail-safe mode
- Unlocked mode
- Locked mode
- Self-test mode

Figure 20. State diagram



Notes:

(*) Transition to fail-safe sets 'BYPASS_SAT'status bit to 1 only if BYPASSCTL = 1 and VS-VOUT > $V_{DS\_bypass\_sat}$.

(**) Transition to unlocked sets 'EN' bit to 1.

(***) Transition to fail-safe resets 'EN' bit to 0.

t_{STBY_OUT} = 4 µs

t_{STBY_IN} = 80 ms

$t_{S\_T\_WAIT}$ = 5 µs

13.2 Power-on state

The power-on state is the device reset state at power-on-reset and device startup.

- As soon as the internal oscillator is ready, nonvolatile memory content is downloaded into the corresponding RAM registers
- External MOSFET and internal bypass are kept OFF
- The SPI interface is not active
- SPI global status byte RSTB bit is set to 1 to notify PoR event occurrence
- Transition to the standby state is automatically triggered after the end of the NVM download phase

13.3 Standby state

In the standby state, the device is in quiescent power consumption and operates under the following conditions:

- External FET off with all related internal power circuitry (charge pump)
- Internal oscillator turned off, with registers frozen to last values before standby entry (powered without clock)
- Low current bypass can be ON or OFF according to the 'BYPASS_CTL' control bit/BYPASS_CTL_DEF NVM bit
- Protections are disabled apart bypass V_{DS} monitoring, in case the bypass is in ON state, to detect saturation and consequently wake-up the device
- SPI interface is not active (watchdog monitor disabled)
- DIAG pin kept high, unless device internal malfunction (NVM download failure after power-on)

The device can reach this state (standby entry) from:

- Power-on state, after NVM download completion
- Unlocked or locked state, through a well-defined SPI frame sequence
- Fail-safe state (with FS_MODE = 00 configuration), if BYPASS_SAT=0 (no bypass fault) and DIN=0 for t > t_{STBY_IN}, without any activity on the SPI interface during this interval.

The device can leave this state (wake-up) to:

- Unlocked state, if CSN pin is kept low (by direct CSN control of SPI frame) for t > $t_{STANDBY\_OUT}$
- Fail-safe state, if one of the following conditions is met:
  1. Internal bypass ON and bypass saturation detected (V_S - V_{OUT} > $V_{DS\_BYBASS\_SAT}$)
  2. DIN pin set to 1 for t > $t_{STANDBY\_OUT}$, with FS_MODE configurations 00/10/11 (with configuration 01, the device remains in standby)

13.4 Fail-safe state

In this state the device is in a safe operating mode, with limitations on software control and the following properties:

- External FET can be automatically turned-on (due to bypass fault during active standby) or DIN-controlled/ driven off/maintained with last unlocked status, depending on selected configuration (FS_MODE control register field)
- Bypass can be driven with NVM default/driven off/maintained with last unlocked status, depending on the selected configuration (FS_MODE)
- Channel protections enabled according to external FET and bypass status
- Device protections enabled
- The SPI interface is active
- RAM control registers can be written but modifications are not effective or can be only readable (with some exceptions detailed below), depending on device configuration (FS_DEF_CFG_EN control register field)
- Capacitive load burst charging mode functionality is available if enabled by proper DIN toggling sequence
- Watchdog monitor disabled

The fail-safe state can be reached from:

- Standby state (see above)

- Unlocked state, if one of the following conditions is met:
  1. Watchdog fail
  2. SPI communication error detected
  3. HWLO external pin set high if LOCKED_MODE_EN bit (CR#1) set to '0'
  4. ‘EN’ bit set to ‘0’ by SPI frame, if LOCKED_MODE_EN bit (CR#1) set to '0'
- Locked state, if watchdog fails or SPI communication errors are detected
- Self-test state, if watchdog fails or HWLO pin is set high

The device can leave the fail-safe state to:

- Standby state (see above)
- Unlocked state, by well-defined SPI frame sequence

13.5 Unlocked state

In this state the device functionalities are fully operative and controllable by hardware and software:

- External FET controllable by SPI interface or DIN (if enabled)
- Internal bypass controllable by SPI interface
- Channel protection is enabled according to external FET and bypass status
- Device protections enabled
- SPI interface active (watchdog monitoring enabled)
- RAM registers fully accessible
- CCM capacitive charging mode functionality is available if enabled by a dedicated control bit

The unlocked state can be reached from

- Standby and fail-safe states (refer to previous sections)
- Locked state, by well-defined SPI frame sequence
- Self-test state, at the end of self-test execution or if the SPI self-test stop command is received

The device can leave this state to

- Standby and fail-safe states (refer to previous sections)
- Locked state, if one of the following conditions is met:
- 1. HWLO external pin set high, if LOCKED_MODE_EN it (CR#1) set to '1'
  2. 'EN' bit set to '0' by SPI frame, if LOCKED_MODE_EN bit (CR#1) set to '1'
- Self-test state, if a specific self-test has been selected and its execution has been triggered

13.6 Locked state

In this state the device configuration cannot be changed, while user still has software/hardware turn-on/off control of external FET and bypass switch:

- External FET controllable by SPI interface combined with DIN input (if enabled)
- Internal bypass controllable by SPI interface
- Channel protection enabled according to external FET and bypass status
- Device protections enabled
- SPI interface active (watchdog monitoring enabled)
- RAM registers fully accessible if NVM_DEF_CFG_EN = 1 (device configuration from NVM) otherwise locked
- Capacitive load burst charging mode functionality available if enabled either by dedicated control bit

The device can reach this state only from unlocked and leave it to standby, fail-safe, or unlocked as described previously in this document.

13.7 Self-test mode

This state is dedicated to execution of in-application checks performed by device on some key functionality. For details, refer to dedicated section in this document.

The following figure summarizes main device functions status depending on device control states.

Table 62. Device functionalities status vs device states

Device functionalities	Device states					
	Power-on	Stand-by	Unlocked	Locked	Self-test	Fail-safe
Output	Off	Off	See Table 24	See Table 24	See Table 24(1)	See Table 25
Bypass	Off	Off/On	See Table 24	See Table 24	See Table 24	See Table 25
V3V3	Internal LDO	Internal PRE-REG	Internal LDO or external regulator	Internal LDO or external regulator	Internal LDO or external regulator	Internal LDO or external regulator
Device configuration	POR Default	RAM (frozen)	RAM	NVM or RAM(2)	RAM	NVM or RAM(2)
RAM REGs access	No access	No access	R/W/C	Control: R/W Config.: R/W(3) Status: R/C	R/W/C	Control: R/W(4) Config.: R/W(4) Status: R/C
SPI I/F	Inactive	Inactive	Active	Active	Active	Active
Channel protections	Inactive	Inactive(5)	Active	Active	Active(6)	Active
Device protections	Active	Inactive	Active	Active	Active	Active
Diag	Low/High	High	Low/High	Low/High	Low/High	Low/High
Cap. charge	Disabled	Disabled	Enabled	Enabled	Disabled	Enabled/Disabled(4)

1. *Output off in case of stuck-on self-test execution.*
2. *Defined by dedicated option bit in the NVM.*
3. *Writable if NVM is used, otherwise is read-only.*
4. *Depending on fail-safe mode configuration.*
5. *Bypass fault protection active if bypass is on.*
6. *Specific protection inactive, depending on which self-test is executed.*

14 Application information

Figure 21. **Application diagram (MCU 3.3 V)**

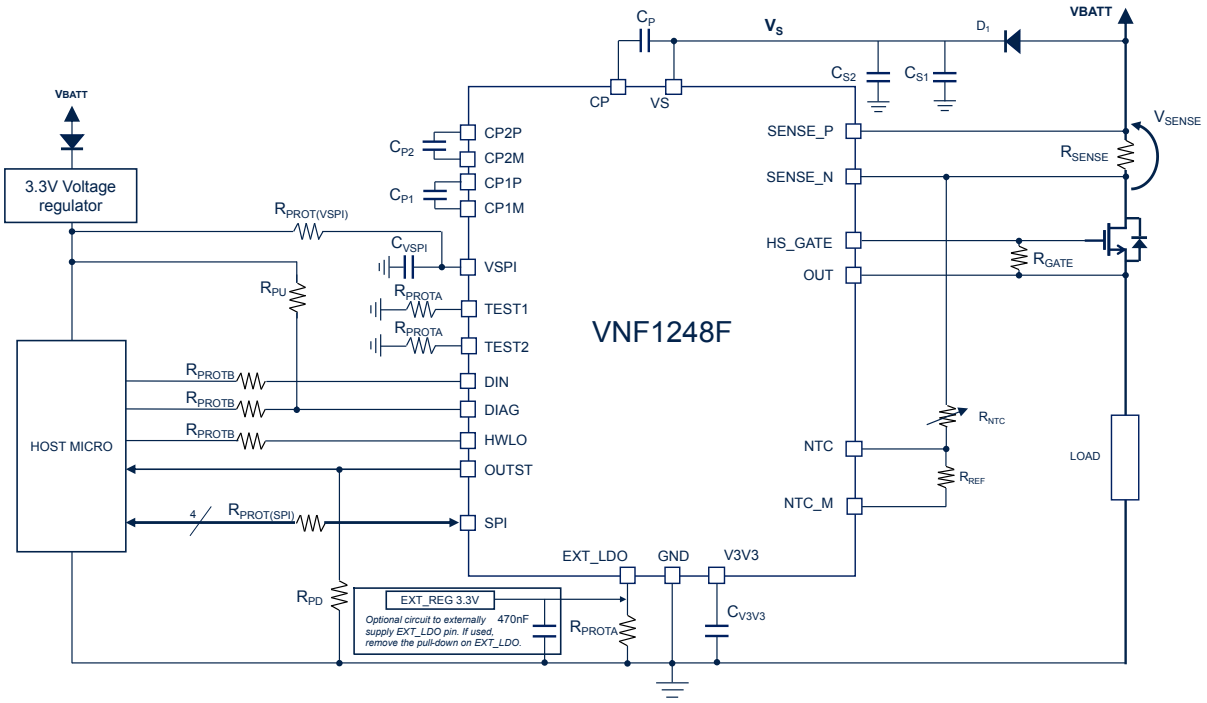


Figure 22. **Application diagram (MCU 5 V)**

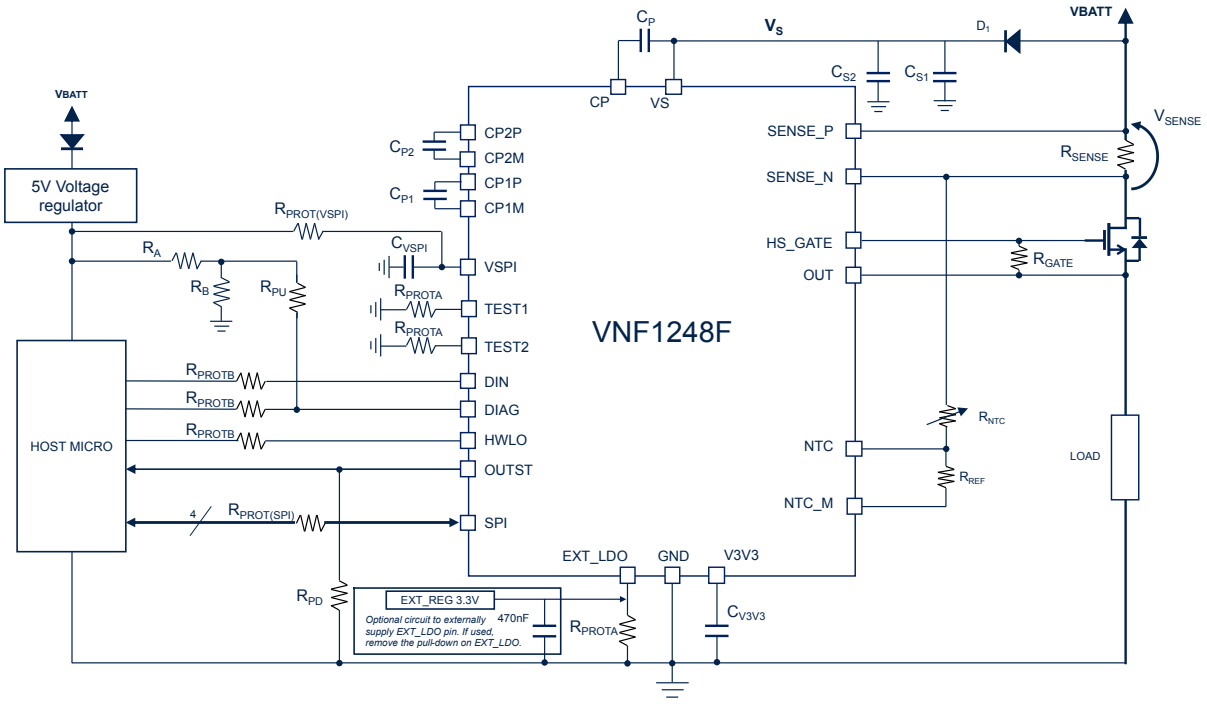


Table 63. Component value

Reference		Value
C_{S1}		22 µF (1) 2x22 µF (2)
C_{S2}		100 nF
C_{P1}, C_{P2}		220 nF
C_P		390 nF
C_{VSPI}		330 nF
C_{V3V3}		1 µF
R_{PU}		4.7 kΩ
R_{PD}		8.2 kΩ
R_A (only for application with MCU 5 V)		8.2 kΩ
R_B (only for application with MCU 5 V)		15 kΩ
$R_{(VSPI)}$		300 Ω
R_{PROTA}		1 kΩ
R_{PROTB}		2.2 kΩ
$R_{PROT(SPI)}$	R_{CS}	50 mΩ
	R_{CLK}	50 mΩ
	R_{SDI}	50 mΩ
	R_{SDO}	100 Ω
R_{GATE}		47 kΩ
R_{REF}		12 kΩ ±1%
R_{SENSE}		1 mΩ
R_{NTC}		B57232V5103F360
D_1		STPS2L60-Y Reverse battery protection

1. *In case of usage of device at 48 V.*
2. *In case of usage at 12 V, in order to withstand the severe cold start pulse test defined by the VW80000 LV124 E-11 without turning OFF the OUT.*

15 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

15.1 QFN32L Epad (5.0x5.0x1.0 mm) package information

Figure 23. QFN32L Epad (5.0x5.0x1.0 mm) package outline

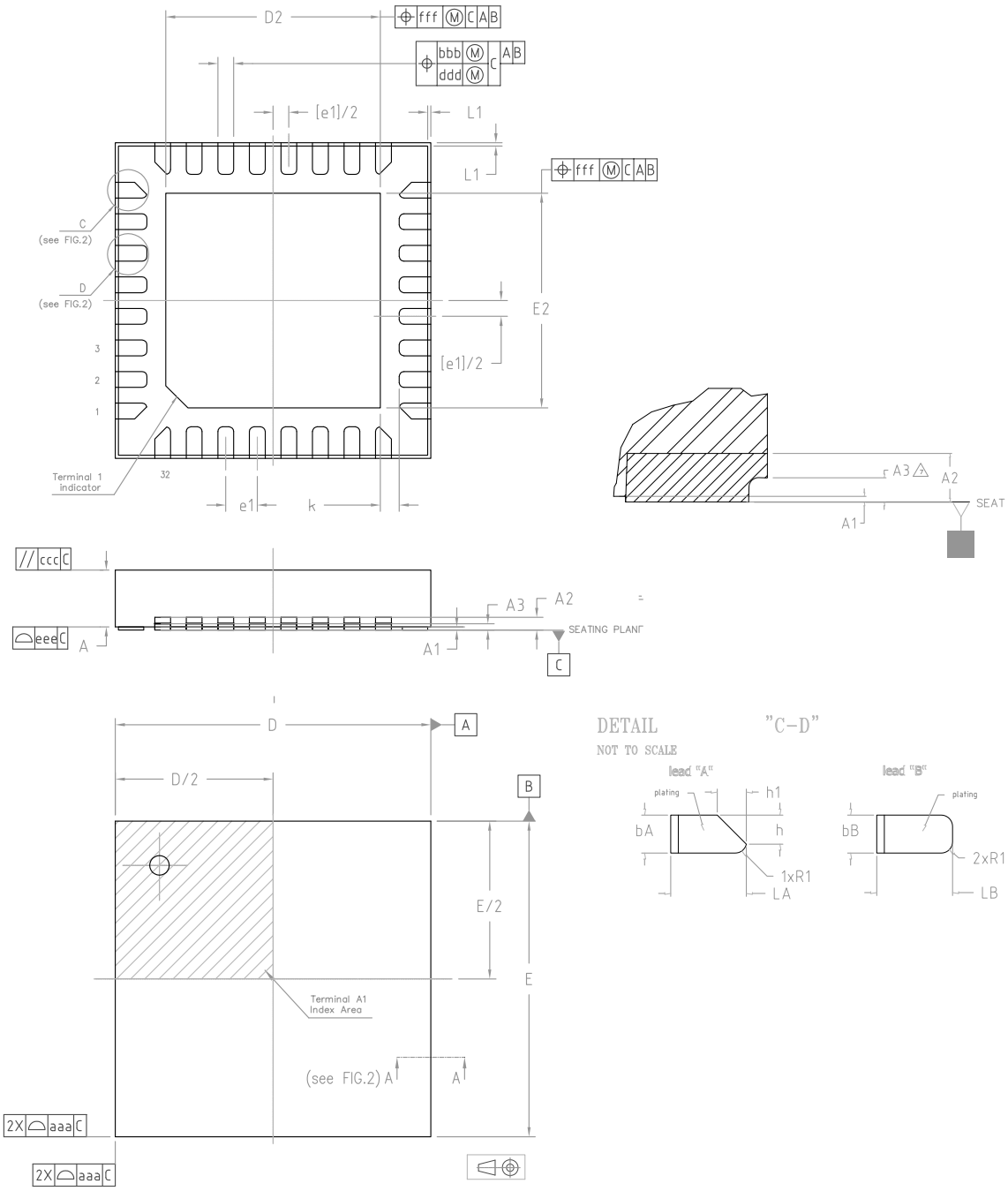
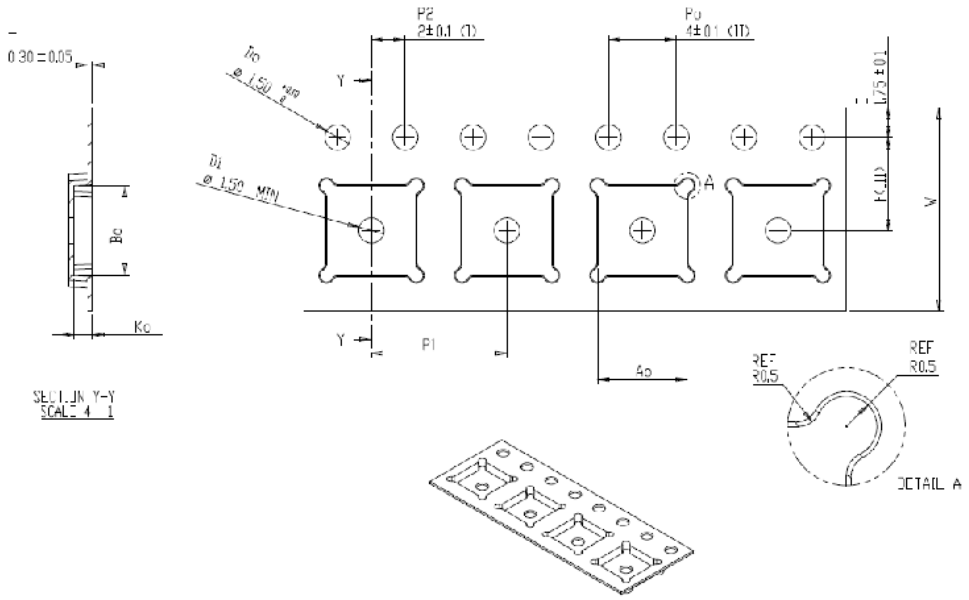


Table 64. **QFN32L Epad (5.0x5.0x1.0 mm) package mechanical data**

Symbol	Dimension in mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0		0.05
A2		0.2 REF	
A3	0.1		
D		5.00 BSC	
D2	3.40	3.50	3.60
E		5.00 BSC	
E2	3.40	3.50	3.60
e1		0.5 BSC	
k	0.20		
L1			0.05
La	0.40	0.50	0.60
bA	0.20	0.25	0.30
h		0.19 REF	
h1		0.19 REF	
LB	0.45	0.50	0.55
bB	0.20	0.25	0.30
N		32	
R1			0.1
Tolerance of form and position			
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

15.2 QFN32L Epad 5x5 mm packing information

Figure 24. **QFN32L Epad 5x5 mm carrier tape**



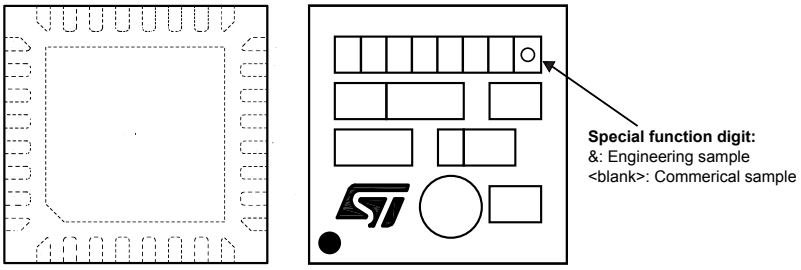
Note: (I) (III) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of sprocket holes is ± 020.

Table 65. **QFN32L Epad 5x5 mm carrier tape**

Description	Value [mm]
A0	5.30 ± 0.1
B0	5.30 ± 0.1
K0	1.10 ± 0.1
F	5.50 ± 0.1
P1	8.00 ± 0.1
W	12.00 ± 0.1

15.3 QFN32L Epad 5x5 marking information

Figure 25. **QFN32L Epad 5x5 marking information**



Parts marked as '&' are not yet qualified and therefore not approved for use in production. STMicroelectronics is not responsible for any consequences resulting from such use. In no event will STMicroelectronics be liable for the customer using any of these engineering samples in production. STMicroelectronics's quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

16 Ordering information

Table 66. **Ordering information**

Order code	Package	Packing
VNF1248FTR	QFN32L	Tape and reel

Revision history

Table 67. **Document revision history**

Date	Revision	Changes
20-Dec-2022	1	Initial release.
07-Nov-2023	2	Updated *Section Features on cover page.* Updated *Section 1 Block diagram and pin description, Table 2. Absolute maximum rating, Section 2.3 Main electrical characteristics, Figure 4. eFuse I2-t typical curve (VOC_thrs minimum - VHSC_thrs maximum), Figure 5. eFuse I2-t typical curve (generic thresholds), Figure 6. Current sense self-test flow sequence, Figure 8. External FET stuck-on self-test - flow sequence for entry, Section 6 DIN input management, Section 9 Capacitive charging mode - CCM, Section 10.1 NVM-Programmable default configuration, Table 45. RAM memory map, Table 46. ROM memory map (ID12.2), Section 12.13 Control registers, Section 13 Functional description, Figure 23. Device functionalities status vs device states and Section 14 Application information.* Added *Section 7 Bypass control management, Section 8 Ext LDO, Section 11.8 Current sense under voltage (CS_UV) and Section 13.1 Operating modes, Section 5 VSPI_UV.*
18-Mar-2024	3	Updated *Figure 1. Block diagram*, *Table 4. Supply specification*, *Table 5. SPI logic inputs (CSN, SCK, and SDI) specification*, *Table 20. Bypass switch*, *Section 6.4: Fail-safe state*, *Section 6.2: Unlocked state*, *Table 6. SPI logic output (SDO) specification*, *Table 11. DIN logic input pin specification*, *Table 12. OUTST logic output pin specification*, *Table 16. External FET VDS protection*, *Table 28. External LDO voltage and current*, *Section 10.1.2: NVM default configuration and RAM registers in fail-safe*, *Table 35. Current sense undervoltage thresholds* and *Figure 21. Application diagram.* Added *Section 6.3: Locked state*, *Section 9: Capacitive charging mode–CCM* and *Section 10.1.4: Default configuration upload to RAM.* Minor text changes.
02-Jul-2024	4	Updated Features on cover page. Updated Table 1. Pin functions, Table 2. Absolute maximum rating, Table 4. Supply specification, Table 5. SPI logic inputs (CSN, SCK, and SDI) specification, Table 7. SPI timing specification, Figure 3. SPI specification: timing waveforms, Table 8. HWLO logic input pin specification, Table 12. OUTST logic output pin specification, Table 14. External FET gate driver specification, Table 15. Current sense amplifier , Table 17. External FET VDS protection, Table 18. Hard short circuit protection with integrated 10-bit ADC, Table 19. Overcurrent protection, and Table 22. V_{OUT} A-to-D conversion. Updated title of *Table 11. Voltage and current thresholds of DIN PIN* to Table 11. DIN logic input pin specification, and *Table 12. Voltage and current thresholds of OUTST PIN* to Table 12. OUTST logic output pin specification. Updated Figure 7. Current sense self-test flow sequence, Figure 8. VDS monitor self-test flow sequence, and Figure 9. External FET stuck-on self-test flow sequence for entry. Updated Section 6.1: Standby state, replaced *Figure 10. UNLOCKED state – DIN control behavior* with Table 24. Unlocked state - DIN control behavior, and *Figure 11. FAILSAFE state* with Table 25. Fail-safe state. Removed *Table 25. Voltage and current thresholds of DIN PIN*. Updated Table 26. Bypass switch control vs FSM. Updated Section 9: Capacitive charging mode–CCM, Table 29. CCM PWM standard period setting, Figure 10. CCM in unlocked state (1), and Figure 11. CCM in fail-safe state. Updated Table 46. Global status byte - Bit description, Table 47. RAM memory map, Table 49. CR#1: control register 1 (read/write); address 01h, Table 50. CR#2: control register 2 (read/write); address 02h , Table 51. CR#3: control register 3 (read/write); address 03h, Table 52. CR#4: control register 4 (read/write); address 04h, Table 53. CR#5: control register 5 (read/write); address 05h, Table 49. CR#1: control register 1 (read/write); address 01h, and removed *Table 51. S_T_CFG self test selection*. Updated Figure 20. State diagram, Section 13.3: Standby state, Section 13.4: Fail-safe state, Section 13.5: Unlocked state, Section 13.6: Locked state, and replaced *Figure 23. Device functionalities status vs device states* with Table 62. Device functionalities status vs device states. Updated Section 14: Application information. Minor text changes.

Date	Revision	Changes
10-Jul-2025	5	Updated Features on cover page, Section 5, Section 8, and added Section 11.9. Updated Table 1, Table 2, Table 4, Table 5, Table 6, Table 7, Table 8, Table 10, Table 11, Table 12, Table 14, Table 15 (splitted in Table 15 and Table 16), Table 17, Table 18 (and title), Table 19, Table 20, Table 21, Table 22, Table 26Table 63. Updated Figure 1, Figure 3, Figure 21, and added Figure 22. Updated Note below Figure 4, and added Note of Figure 10. Replaced HSHT with HSC, VDS_THR with VDS_THRS and, BYPASS_DEF with BYPASS_CTL_DEF.
18-Jul-2025	6	Updated Features on cover page, Section 8. Updated Table 4, Table 5, Table 12, Table 33, and Table 54.
01-Aug-2025	7	Updated Table 1, Table 11 (moved data timing from Section 6.5), Table 54, and Figure 1. Added Section 15.2.

Contents

List of tables

List of figures

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