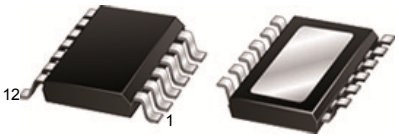
# VND5HV100AJ-E

Datasheet

# Double channel high-side driver with analog current sense for 48 V automotive applications




**PowerSSO-12**

| Product status link |
|---|
| VND5HV100AJ-E |

| Product summary | |
|---|---|
| **Order code** | **VND5HV100AJTR-E** |
| **Package** | PowerSSO-12 |
| **Packing** | Tape and reel |

## Features

| Description | Parameter | Value |
|---|---|---|
| Max. transient supply voltage | $V_{CC}$ | 60 V |
| Operating voltage range | $V_{CC}$ | 8 to 54 V |
| Typ. on-state resistance (per channel) | $R_{ON}$ | 100 mΩ |
| Current limitation (typ.) | $I_{LIM}$ | 22 A |
| Off-state supply current | $I_S$ | 55 µA[1] |

1. *Typical value with all loads connected.*

- AEC-Q100 qualified
- General
  - Very low standby current
  - 3.0 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - Compliant with European directive 2002/95/EC
  - Fault reset standby pin (FR_Stby)
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide range currents
  - Off-state open-load detection
  - Output short to $V_{CC}$ detection
  - Overload and short to ground latch-off
  - Thermal shutdown latch-off
  - Very low current sense leakage
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of $V_{CC}$
  - Thermal shutdown
  - Electrostatic discharge protection

## Applications

- All types of resistive, inductive and capacitive loads

## Description

The VND5HV100AJ-E is a monolithic device made using STMicroelectronics VIPower technology, intended for driving resistive or inductive loads with one side connected to the ground. Active $V_{CC}$ pin voltage clamp protects the device against low energy spikes.

The device integrates an analog current sense, which delivers a current proportional to the load current.

Fault conditions such as overload, overtemperature, or short to $V_{CC}$ are reported via the current sense pin.

Output current limitation protects the device in overload conditions. The device latches off in case of overload or thermal shutdown.

The device is reset by a low level pass on the fault reset standby pin.

A permanent low level on the inputs and on the fault reset standby pins disables all outputs and sets the device in standby mode.

# 1 Block diagram and pin description

**Figure 1. Block diagram**

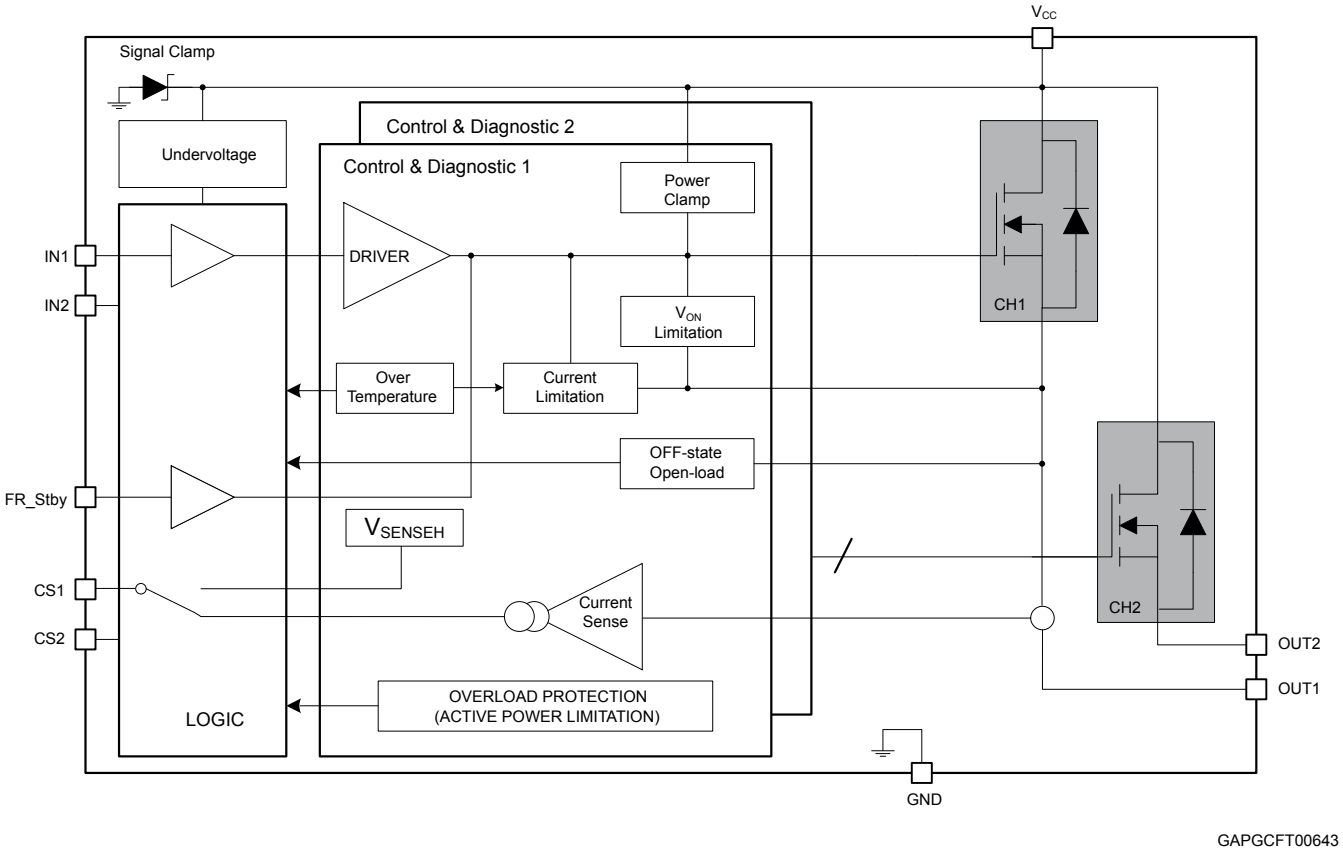



**Table 1. Pin function**

| Name | Function |
|---|---|
| $V_{CC}$ | Battery connection. |
| OUT1, 2 | Power outputs. |
| GND | Ground connection. |
| IN1, 2 | Voltage controlled input pins with hysteresis, CMOS compatible. They control output switch state. |
| CS1, 2 | Analog current sense pins, they deliver a current proportional to the load current. |
| FR_Stby | In case of latch-off for overtemperature/overcurrent condition, a low pulse on the FR_Stby pin is needed to reset the channel.<br>The device enters in standby mode if all inputs and the FR_Stby pin are low. |

**Figure 2. Configuration diagram PowerSSO-12 (top view)**

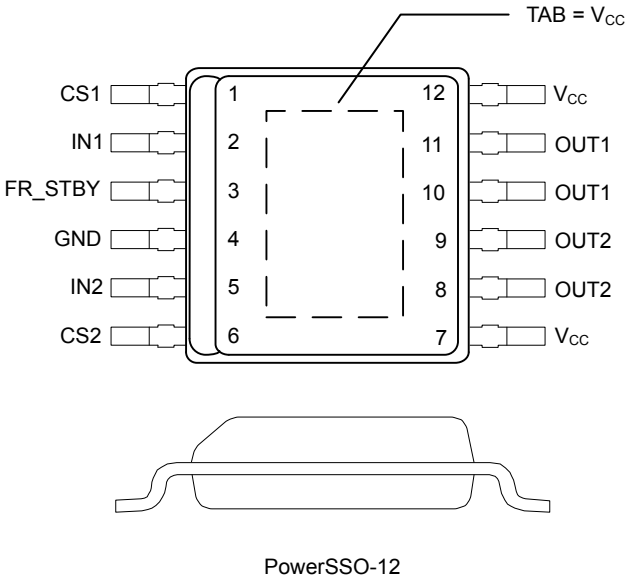


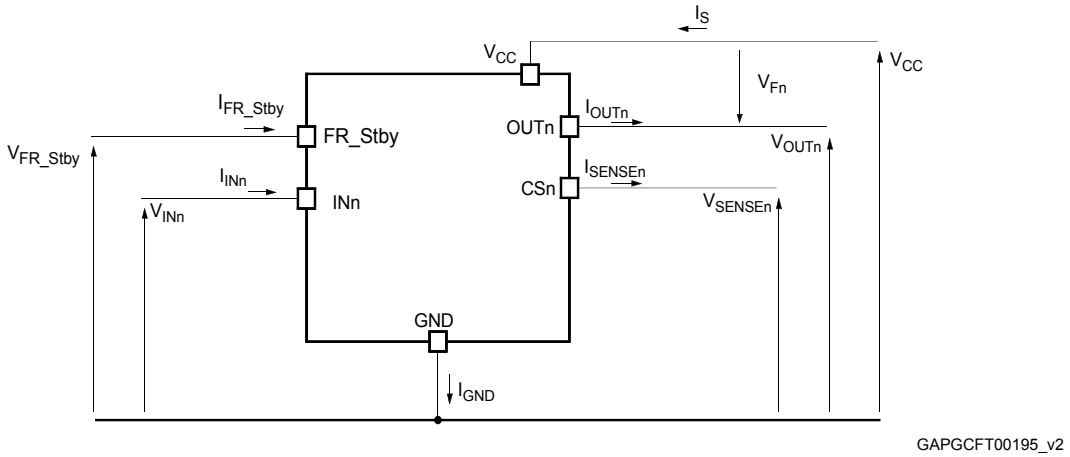

**Table 2. Suggested connections for unused and not connected pins**

| Connection/pin | CurrentSense | NC | Output | Input | FR_Stby |
|---|---|---|---|---|---|
| Floating | Not allowed | X[(1)] | X | X | X |
| To ground | Through 10 kΩ resistor | X | Not allowed | Through 15 kΩ resistor | Through 15 kΩ resistor |

1. *X: do not care.*

# 2 Electrical specification

**Figure 3. Current and voltage conventions**




## 2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the Table 3 may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | 60 | V |
| $I_{OUT}$ | DC output current | | Internally limited | A |
| $I_{IN}$ | DC input current | | 0 to 10 | mA |
| $I_{FR_Stby}$ | Fault reset standby DC input current | | 0 to 1.5 | mA |
| $V_{CSENSE}$ | Current sense maximum voltage | | ($V_{CC}$ - 60) to $V_{CC}$ | V |
| $E_{MAX}$ | Maximum switching energy ($T_{Jstart}$ = 150 °C; $I_{OUT}$ = $I_{limL\ (typ.)}$) | | 70 | mJ |
| $L_{smax}$ | Maximum stray inductance in short circuit condition<br>$R_L$ = 300 mΩ, $V_{BAT}$ = 54 V, $T_{Jstart}$ = 150 °C, $I_{OUT}$ = $I_{limH\ (max.)}$ | | 10 | µH |
| $V_{ESD}$ | Electrostatic discharge (human body model: R = 1.5 kΩ, C = 100 pF) | IN1, 2 | 4000 | V |
| | | CS1, 2 | 2000 | |
| | | FR_Stby | 4000 | |
| | | OUT1, 2 | 5000 | |
| | | $V_{CC}$ | 5000 | |
| | Charge device model (CDM-AEC-Q100-011) | | 750 | |
| $T_J$ | Operating junction temperature range | | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature range | | -55 to 150 | °C |

## 2.2 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thJC}$ | Thermal resistance, junction-to-case (with one channel ON) | 6 | °C/W |
| $R_{thJA}$ | Thermal resistance, junction-to-ambient | See Figure 15 | °C/W |

## 2.3 Electrical characteristics

8 V < $V_{CC}$ < 54 V, -40 °C < $T_J$ < 150 °C, unless otherwise specified.

**Table 5. Power section**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating supply voltage | | 8 | 48 | 54 | V |
| $V_{USD}$ | Undervoltage shutdown | | | 3.5 | 5 | V |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.5 | | V |
| $R_{ON}$ | On-state resistance(1) | $I_{OUT}$ = 1.5 A, $T_J$ = 25 °C | | 100 | | mΩ |
| | | $I_{OUT}$ = 1.5 A, $T_J$ = 150 °C | | | 200 | |
| $V_{clamp}$ | Clamp voltage | $I_S$ = 20 mA | 60 | 64 | 70 | V |
| $I_S$ | Supply current | Off-state, $V_{CC}$ = 48 V, $T_J$ = 25 °C, $V_{IN}$ = $V_{OUT}$ = $V_{SENSE}$ = 0 V, $V_{FR_Stby}$ = 0 V | | 55(2) | 85(2) | µA |
| | | On-state, $V_{CC}$ = 48 V, $T_J$ = 25 °C, $V_{IN}$ = 5 V, $I_{OUT}$ = 0 A | | 5.8 | 7.5 | mA |
| $I_{L(off)}$ | Off-state output current | $V_{IN}$ = $V_{OUT}$ = 0 V, $V_{CC}$ = 48 V, $T_J$ = 25 °C | 0 | 0.01 | 3 | µA |
| | | $V_{IN}$ = $V_{OUT}$ = 0 V, $V_{CC}$ = 48 V, $T_J$ = 125 °C | 0 | | 5 | |
| $V_F$ | Output - $V_{CC}$ diode voltage | $-I_{OUT}$ = 1.5 A, $T_J$ = 150 °C | | | 0.7 | V |

1. *For each channel.*
2. *Power MOSFET leakage included.*

**Table 6. Switching ($V_{CC}$ = 48 V, $T_J$ = 25 °C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $R_L$ = 32 Ω | | 25 | | µs |
| $t_{d(off)}$ | Turn-off delay time | $R_L$ = 32 Ω | | 43 | | µs |
| $(dV_{OUT}/dt)_{(on)}$ | Turn-on voltage slope | $R_L$ = 32 Ω | | 2 | | V/µs |
| $(dV_{OUT}/dt)_{(off)}$ | Turn-off voltage slope | $R_L$ = 32 Ω | | 2.2 | | V/µs |
| $W_{ON}$(1) | Switching energy losses during $t_{won}$ | $R_L$ = 32 Ω | | 0.41 | | mJ |
| $W_{OFF}$(1) | Switching energy losses during $t_{woff}$ | $R_L$ = 32 Ω | | 0.34 | | mJ |

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

**Table 7. Logic inputs**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage | | | - | 0.9 | V |
| $I_{IL}$ | Low level input current | $V_{IN}$ = 0.9 V | 1 | - | | µA |
| $V_{IH}$ | Input high level voltage | | 2.1 | - | | V |
| $I_{IH}$ | High level input current | $V_{IN}$ = 2.1 V | | - | 10 | µA |
| $V_{I(hyst)}$ | Input hysteresis voltage | | 0.25 | - | | V |
| $V_{ICL}$ | Input clamp voltage | $I_{IN}$ = 1 mA, $V_{CC}$ = 48 V | 5.5 | - | 7 | V |
| $V_{FR_Stby_L}$ | Fault_reset_standby low level voltage | | | - | 0.9 | V |
| $I_{FR_Stby_L}$ | Low level fault_reset_standby current | $V_{FR_Stby}$ = 0.9 V | 1 | - | | µA |
| $V_{FR_Stby_H}$ | Fault_reset_standby high level voltage | | 2.1 | - | | V |
| $I_{FR_Stby_H}$ | High level fault_reset_standby current | $V_{FR_Stby}$ = 2.1 V | | - | 10 | µA |
| $V_{FR_Stby(hyst)}$ | Fault_reset_standby hysteresis voltage | | 0.25 | - | | V |
| $V_{FR_Stby_CL}$ | Fault_reset_standby clamp voltage | $I_{FR_Stby}$ = 15 mA (t < 10 ms), $V_{CC}$ = 48 V | 11 | - | 15 | V |
| $t_{reset}$[(1)] | Overload latch-off reset time | See Figure 4 | 2 | - | 24 | µs |
| $t_{stby}$ | Standby delay | See Figure 5 | 120 | - | 1200 | µs |

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

**Figure 4. $t_{reset}$ definition**

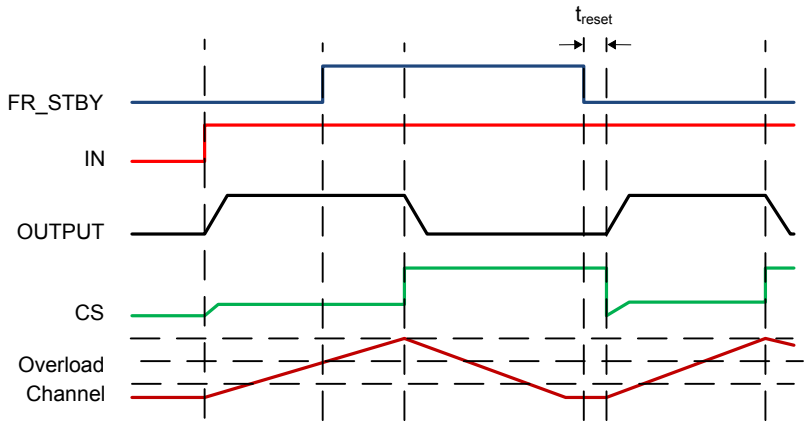



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**Figure 5. $t_{stby}$ definition**

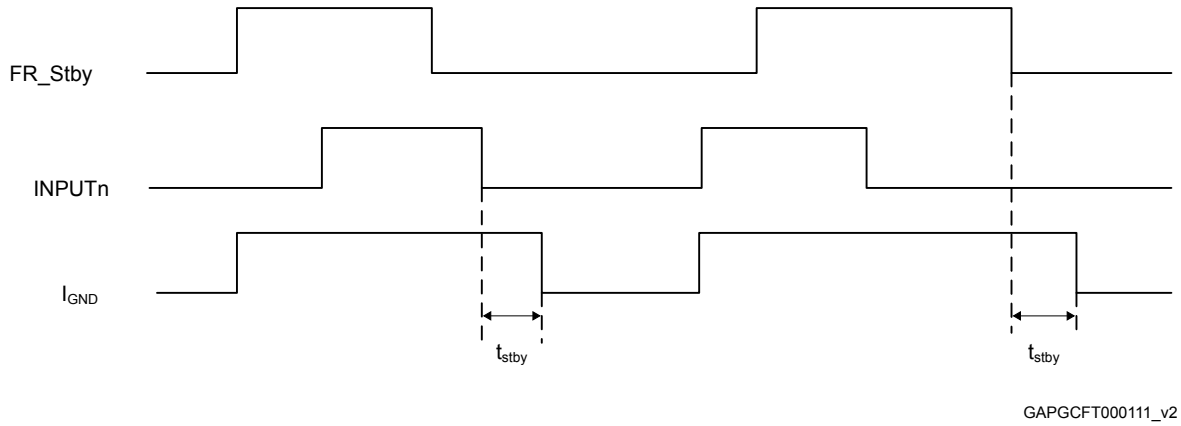


**Table 8. Protections and diagnostics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{limH}$ | DC short circuit current | $V_{CC}$ = 48 V | 16 | 22 | 30 | A |
| | | 5 V < $V_{CC}$ < 54 V | | | 30 | |
| $I_{limL}$ | Short circuit current during thermal cycling | $V_{CC}$ = 48 V, $T_R$ < $T_J$ < $T_{TSD}$ | | 6 | | A |
| $T_{TSD}$(1) | Shutdown temperature | | 150 | 175 | 200 | °C |
| $T_R$(1) | Reset temperature | | $T_{RS}$ + 1 | $T_{RS}$ + 5 | | °C |
| $T_{RS}$(1) | Thermal reset of status | | 135 | | | °C |
| $T_{HYST}$(1) | Thermal hysteresis ($T_{TSD}$ - $T_R$) | | | 7 | | °C |
| $V_{DEMAG}$ | Turn-off output voltage clamp | $I_{OUT}$ = 1.5 A, $V_{IN}$ = 0 V, L = 6 mH | $V_{CC}$ - 58 | $V_{CC}$ - 64 | $V_{CC}$ - 70 | V |
| $V_{ON}$ | Output voltage drop limitation | $I_{OUT}$ = 50 mA, $T_J$ = -40 °C to 150 °C | | 25 | | mV |

1. *Parameter specified by design and evaluated by characterization, not tested in production.*

**Table 9. Current sense (8 V < $V_{CC}$ < 54 V)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $K_1$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 350 mA, $V_{SENSE}$ = 1 V, $T_J$ = -40 °C to 150 °C | 930 | 1547 | 2185 | |
| | | $I_{OUT}$ = 350 mA, $V_{SENSE}$ = 1 V, $T_J$ = 25 °C to 150 °C | 1050 | | 2020 | |
| $dK_1/K_1$(1) | Current sense ratio drift | $I_{OUT}$ = 350 mA, $V_{SENSE}$ = 1 V, $T_J$ = -40 °C to 150 °C | -15 | | 15 | % |
| $K_2$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.8 A, $V_{SENSE}$ = 2 V, $T_J$ = -40 °C to 150 °C | 1225 | 1528 | 1835 | |
| | | $I_{OUT}$ = 0.8 A, $V_{SENSE}$ = 2 V, $T_J$ = 25 °C to 150 °C | 1310 | | 1745 | |
| $dK_2/K_2$(1) | Current sense ratio drift | $I_{OUT}$ = 0.8 A, $V_{SENSE}$ = 2 V, $T_J$ = -40 °C to 150 °C | -12 | | 12 | % |
| $K_3$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 1.5 A, $V_{SENSE}$ = 2 V, $T_J$ = -40 °C to 150 °C | 1340 | 1525 | 1715 | |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $K_3$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 1.5 A, $V_{SENSE}$ = 2 V, $T_J$ = 25 °C to 150 °C | 1405 | 1525 | 1655 | |
| $dK_3/K_3$[1] | Current sense ratio drift | $I_{OUT}$ = 1.5 A, $V_{SENSE}$ = 2 V, $T_J$ = -40 °C to 150 °C | -8 | | 8 | % |
| $K_4$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 6 A, $V_{SENSE}$ = 4 V, $T_J$ = -40 °C to 150 °C | 1450 | 1522 | 1600 | |
| | | $I_{OUT}$ = 6 A, $V_{SENSE}$ = 4 V, $T_J$ = 25 °C to 150 °C | 1475 | | 1560 | |
| $dK_4/K_4$[1] | Current sense ratio drift | $I_{OUT}$ = 6 A, $V_{SENSE}$ = 4 V, $T_J$ = -40 °C to 150 °C | -5 | | 5 | % |
| $I_{SENSE0}$ | Analog sense leakage current | $I_{OUT}$ = 0 A, $V_{SENSE}$ = 0 V, $V_{IN}$ = 0 V, $V_{CC}$ = 48 V, $T_J$ = -40 °C to 150 °C | 0 | | 6 | µA |
| | | $I_{OUT}$ = 0 A, $V_{SENSE}$ = 0 V, $V_{IN}$ = 5 V, $V_{CC}$ = 48 V, $T_J$ = -40 °C to 150 °C | 0 | | 6 | |
| $V_{SENSE}$ | Max. analog sense output voltage | $I_{OUT}$ = 6 A, $R_{SENSE}$ = 3.9 kΩ | 5 | | | V |
| $V_{SENSEH}$ | Analog sense output voltage in fault condition[2] | $V_{CC}$ = 48 V, $R_{SENSE}$ = 3.9 kΩ | 7.5 | 8.5 | 9.5 | V |
| $I_{SENSEH}$ | Analog sense output current in fault condition[2] | $V_{CC}$ = 48 V, $V_{SENSE}$ = 5 V | 4.9 | 9 | 12 | mA |
| $t_{DSENSE2H}$ | Delay response time from rising edge of INPUT pins | $V_{SENSE}$ < 4 V, 0.07 A < $I_{OUT}$ < 1.5 A, $I_{SENSE}$ = 90% of $I_{SENSEMAX}$, (see Figure 6) | | 100 | 200 | µs |
| $\Delta t_{DSENSE2H}$ | Delay response time between rising edge of output current and rising edge of current sense | $V_{SENSE}$ < 4 V, $I_{SENSE}$ = 90 % of $I_{SENSEMAX}$, $I_{OUT}$ = 90 % of $I_{OUTMAX}$, $I_{OUTMAX}$ = 1.5 A (see Figure 10) | | | 150 | µs |
| $t_{DSENSE2L}$ | Delay response time from falling edge of INPUT pins | $V_{SENSE}$ < 4 V, 0.07 A < $I_{OUT}$ < 1.5 A, $I_{SENSE}$ = 10% of $I_{SENSEMAX}$ (see Figure 6) | | 5 | 20 | µs |

1. *Specified by design, not tested in production.*
2. *Fault condition includes: power limitation, overtemperature and open-load in off-state condition.*

**Table 10. Open-load detection ($V_{FR_Stby}$ = 5 V)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Open-load off-state voltage detection threshold | $V_{IN}$ = 0 V, 8 V < $V_{CC}$ < 54 V, $V_{FR_Stby}$ = 5 V | 2.2 | - | 4.2 | V |
| $t_{DSTKON}$ | Output short circuit to $V_{CC}$ detection delay at turn off | $V_{FR_Stby}$ = 5 V (see Figure 7) | 180 | - | 1800 | µs |
| $I_{L(off2)}$ | Off-state output current at $V_{OUT}$ = 4.2 V | $V_{IN}$ = 0 V, $V_{SENSE}$ = 0 V, $V_{OUT}$ rising from 0 V to 4.2 V, $V_{FR_Stby}$ = 5 V, $V_{CC}$ = 48 V | -120 | - | 0 | µA |
| $t_{d_vol}$ | Delay response from output rising edge to $V_{SENSE}$ rising edge in open-load | $V_{OUT}$ = 4.2 V, $V_{IN}$ = 0 V, $V_{SENSE}$ = 90 % of $V_{SENSEH}$, $R_{SENSE}$ = 3.9 kΩ, $V_{FR_Stby}$ = 5 V | | - | 20 | µs |
| $t_{DFRSTK_ON}$ | Output short circuit to $V_{CC}$ detection delay at FR_Stby activation | Input1, 2 = low (see Figure 9) | | - | 50 | µs |

**Figure 6. Current sense delay characteristics**

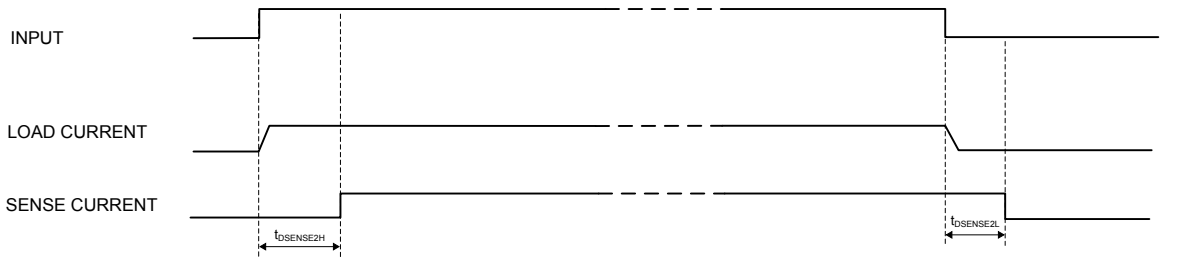


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**Figure 7. Open-load off-state delay timing**

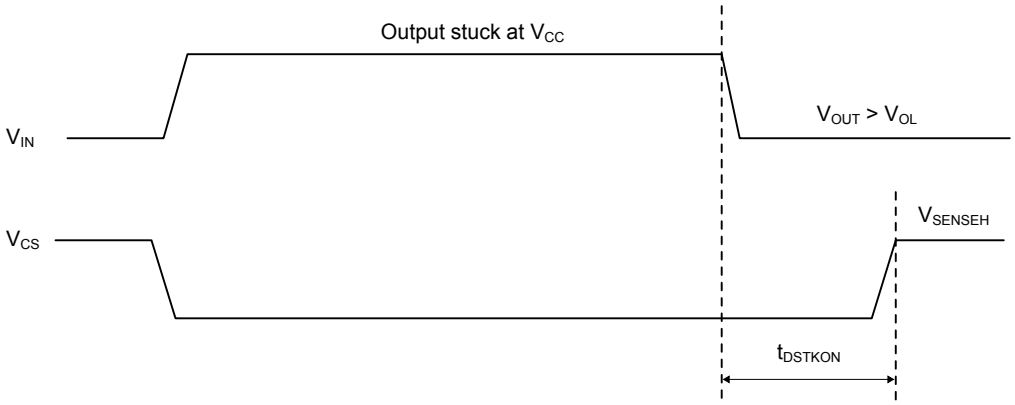


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**Figure 8. Switching characteristics**

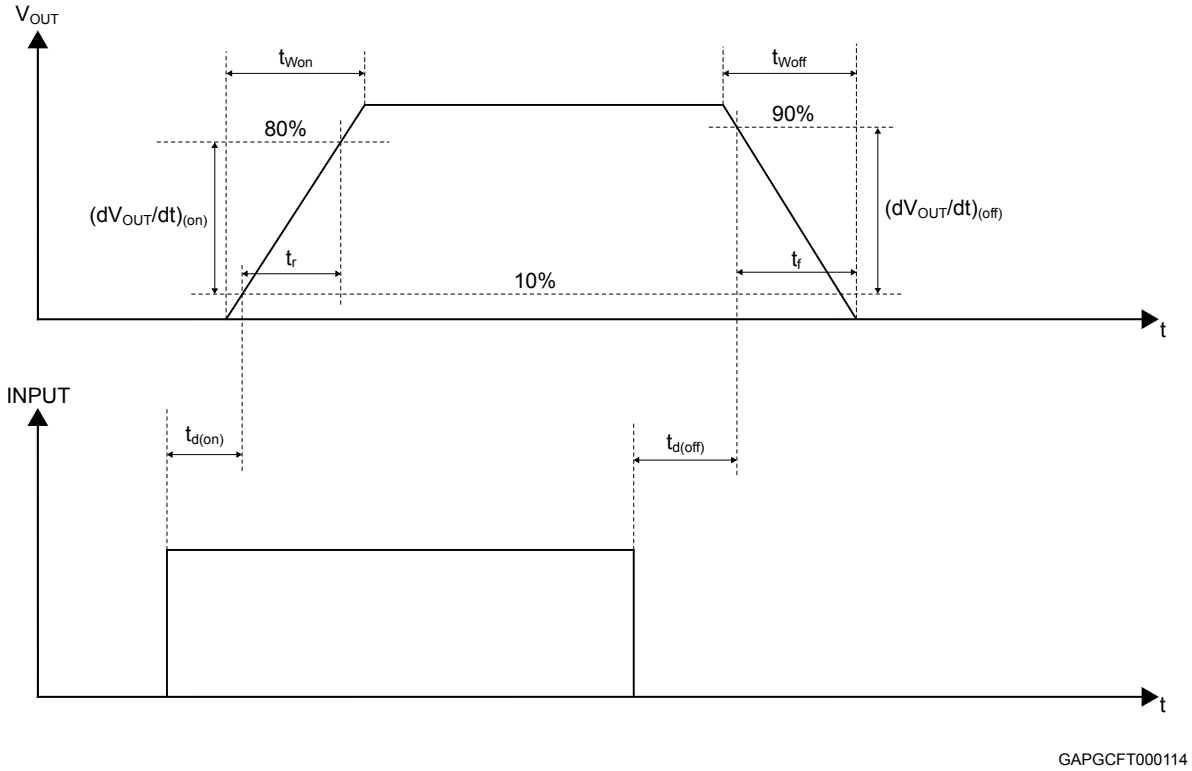



**Figure 9. Output stuck to $V_{CC}$ detection delay time at FR_Stby activation**

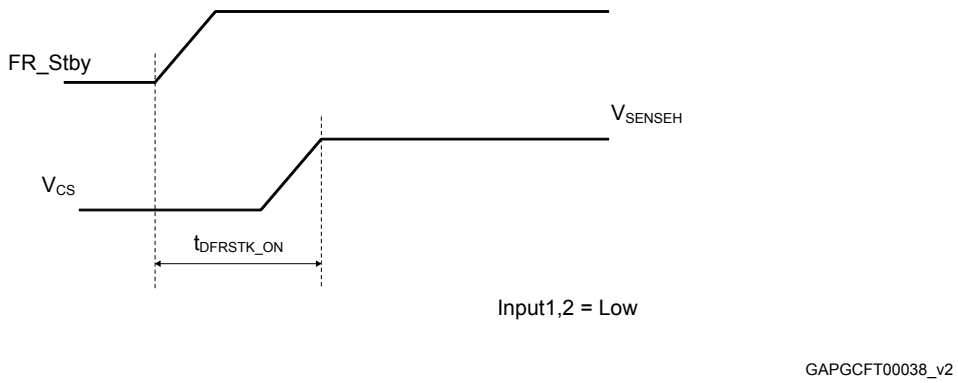


**Figure 10. Delay response time between rising edge of ouput current and rising edge of current sense**

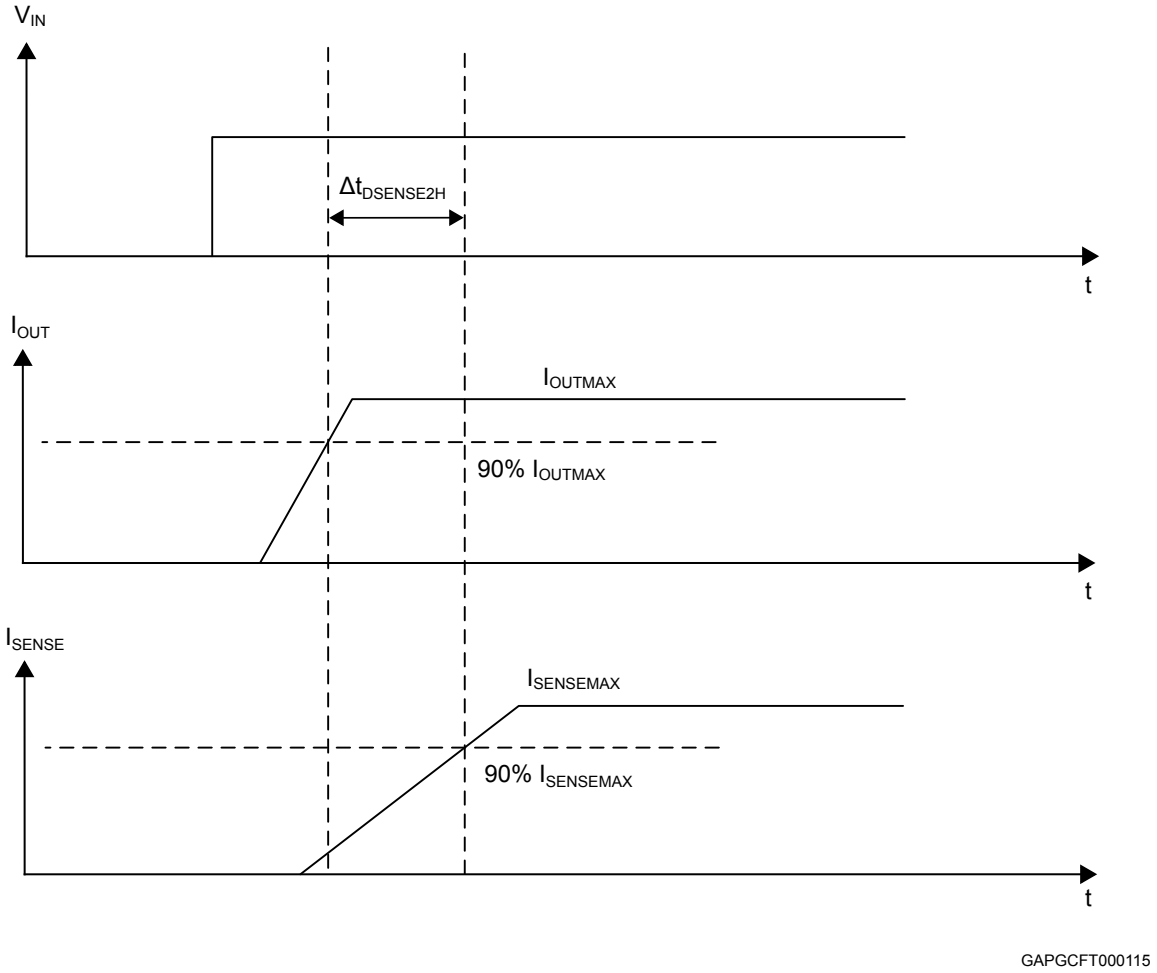



**Figure 11. Output voltage drop limitation**

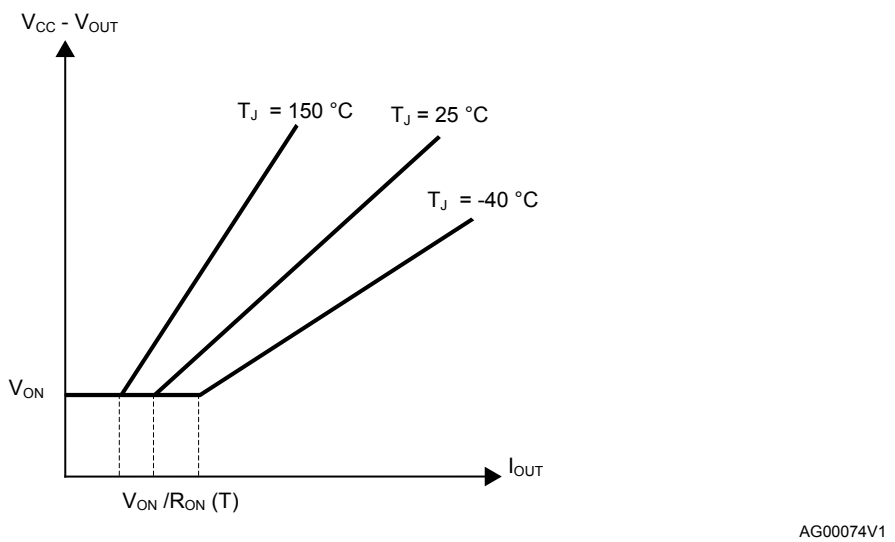
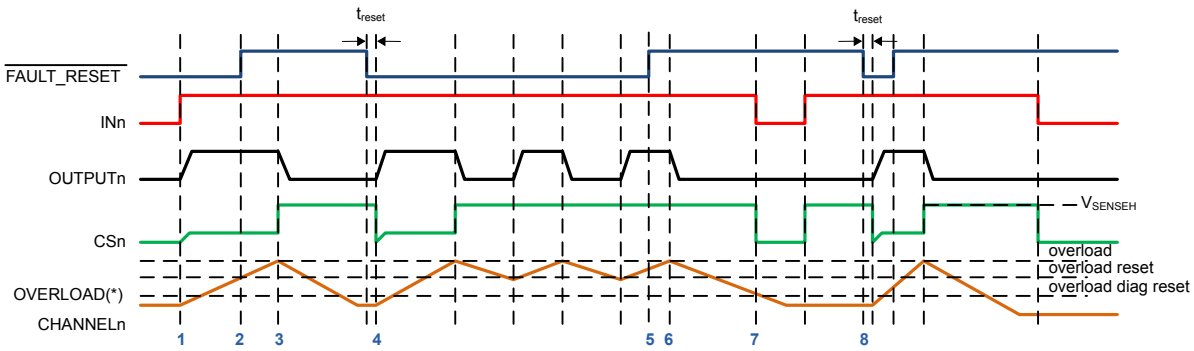


**Figure 12. Device behavior in overload condition**




1: OUTPUTn and CSn controlled by INn
2: FAULT_RESET from '0' to '1' → no action on CSn pin
3: overload latch-off. INn high → CSn high
4: FAULT_RESET low AND Temp channeln < overload_reset → overload latch reset after t_reset
4 to 5: FAULT_RESET low AND INn high → thermal cycling, CSn high
5: FAULT_RESET high → latch-off reset disabled
6 to 7: overload event and FAULT_RESET high → latch-off, no thermal cycling
7 to 8: overload diagnostic disabled/enabled by the input
8: overload latch-off reset by FAULT_RESET

(*) OVERLOAD = thermal shutdown OR power limitation

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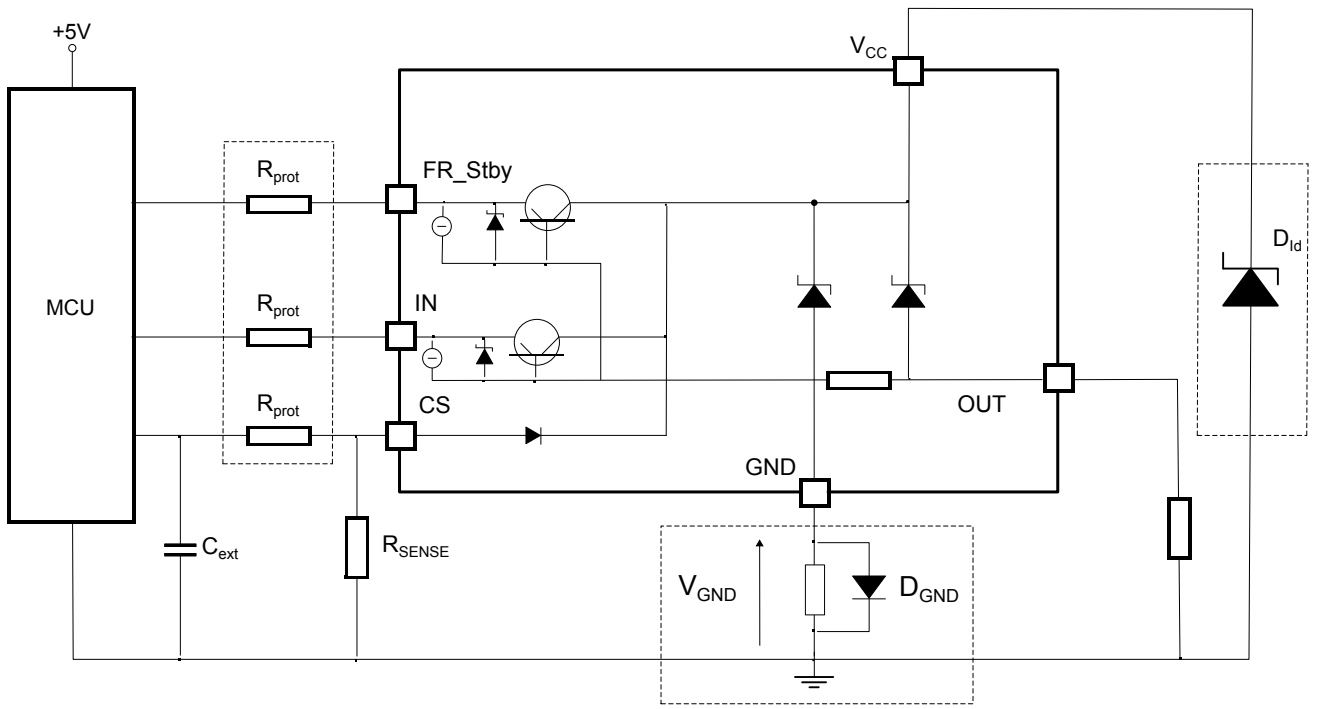
**Table 11. Truth table**

| Conditions | Fault reset standby | Input | Output | Sense |
|---|---|---|---|---|
| Standby | L | L | L | 0 |
| Normal operation | X | L | L | 0 |
| | X | H | H | Nominal |
| Overload | X | L | L | 0 |
| | X | H | H | > Nominal |
| Overtemperature/short to ground | X | L | L | 0 |
| | L | H | Cycling | $V_{SENSEH}$ |
| | H | H | Latched | $V_{SENSEH}$ |
| Undervoltage | X | X | L | 0 |
| Short to $V_{BAT}$ | L | L | H | 0 |
| | H | L | H | $V_{SENSEH}$ |
| | X | H | H | < Nominal |
| Open-load off-state (with pull-up) | L | L | H | 0 |
| | H | L | H | $V_{SENSEH}$ |
| | X | H | H | 0 |
| Negative output voltage clamp | X | L | Negative | 0 |

# 3 Application information

Figure 13. Application schematic




## 3.1 GND protection network against reverse battery

### 3.1.1 Solution 1: resistor in the ground line ($R_{GND}$ only)

This solution can be used with any load type.

The following is an indication on how to dimension the $R_{GND}$ resistor.

1. $R_{GND} \leq 600$ mV / ($I_{S(on)max.}$)
2. $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

Where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power dissipation in $R_{GND}$ (when $V_{CC} < 0$ V: during reverse battery situations) is:

$P_D = (-V_{CC})^2 / R_{GND}$

This resistor can be shared among several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max.}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the $R_{GND}$ produces a shift ($I_{S(on)max.} * R_{GND}$) in the input thresholds and the status output values. This shift varies depending on how many devices are ON in the case of several high side drivers sharing the same $R_{GND}$.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor, then ST suggests solution 2 is used (see below).

### 3.1.2 Solution 2: diode ($D_{GND}$) in the ground line

A resistor ($R_{GND}$ = 4.7 kΩ) should be inserted in parallel to $D_{GND}$ if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values, if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

## 3.2 MCU I/Os protection

If a ground protection network is used and negative transient is present on the $V_{CC}$ line, the control pins are pulled negative. ST suggests that a resistor ($R_{prot}$) has to be inserted in line to prevent the microcontroller I/Os pins from latching-up.

The value of these resistors is a compromise between the leakage current of the microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

**Equation: $R_{prot}$ range calculation**

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH} - V_{GND}) / I_{IHmax}$

**Calculation example:**

For $V_{CCpeak}$ = -600 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

30 kΩ ≤ $R_{prot}$ ≤ 180 kΩ.

Recommended value: $R_{prot}$ = 60 kΩ.

# 4 Package and PCB thermal data

## 4.1 PowerSSO-12 thermal data

Figure 14. PowerSSO-12 PCB

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Layout condition of $R_{th}$ and $Z_{th}$ measurements (board finish thickness 1.6 mm ±10%; board double layer; board dimension 77 mm x 86 mm; board material FR4; Cu thickness 0.070 mm (front and back side); thermal vias separation 1.2 mm; thermal via diameter 0.3 mm ±0.08 mm; Cu thickness on vias 0.025 mm; footprint dimension 4.1 mm x 6.5 mm).

Figure 15. $R_{thJA}$ vs PCB copper area in open box free air condition (one channel ON)

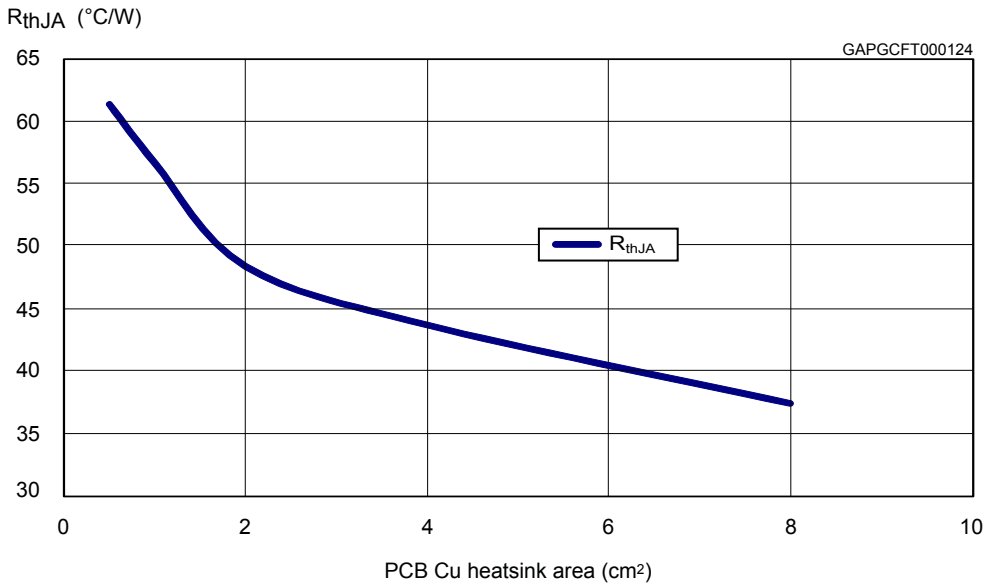


**Figure 16. PowerSSO-12 thermal impedance junction ambient single pulse (one channel ON)**

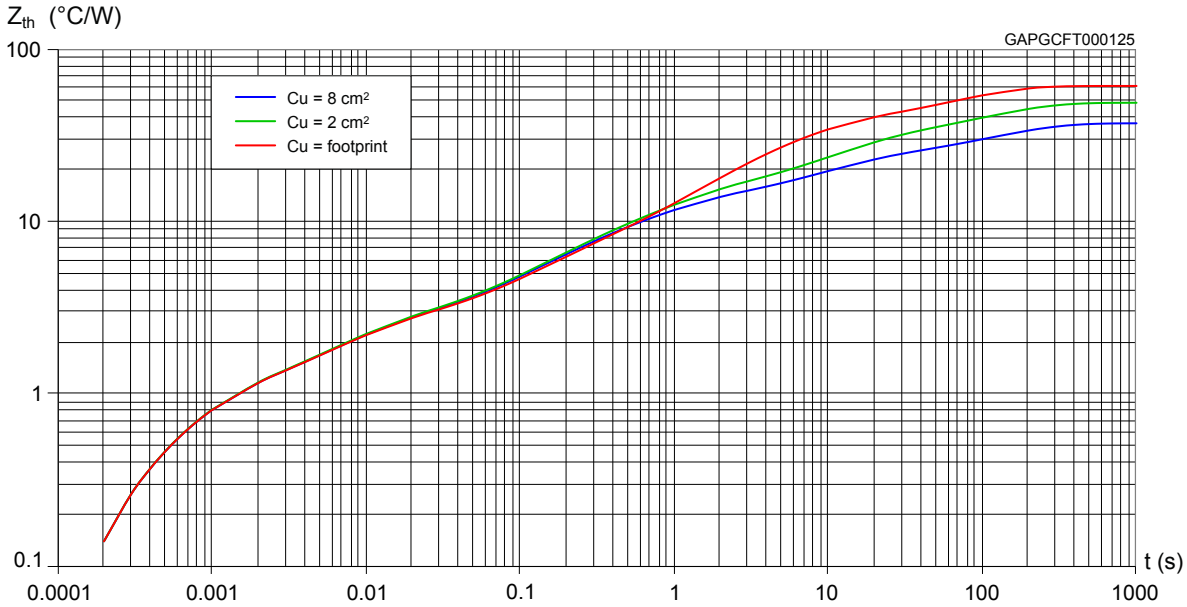
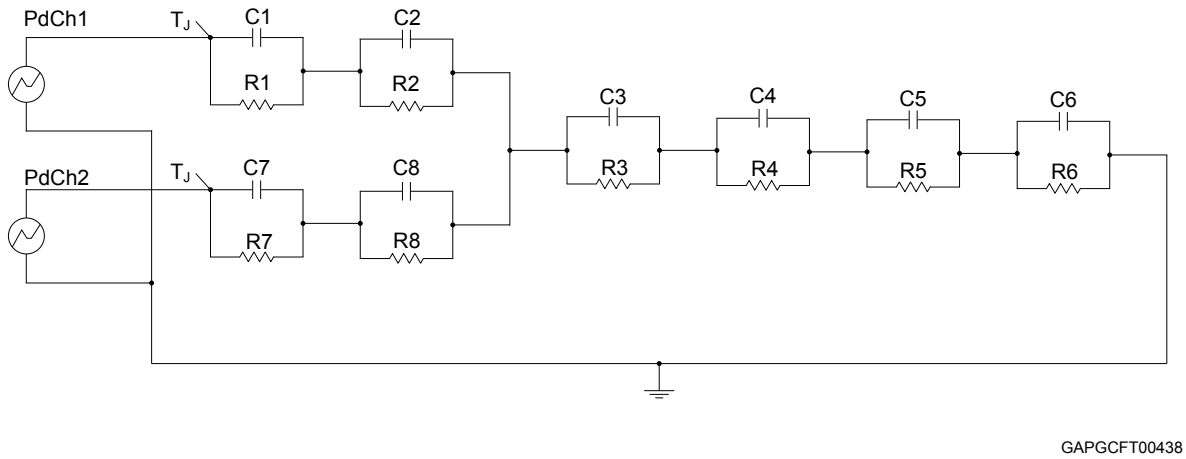



**Figure 17. Thermal fitting model of a double channel HSD in PowerSSO-12**




The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

**Equation: pulse calculation formula**

$Z_{th\delta} = R_{th} \cdot \delta + Z_{thtp} (1 - \delta)$

Where $\delta = t_P/T$

**Table 12. Thermal parameters**

| Area/island ($cm^2$) | Footprint | 2 | 8 |
|---|---|---|---|
| R1 = R7 (°C/W) | 0.8 | | |
| R2 = R8 (°C/W) | 1.5 | | |
| R3 (°C/W) | 3 | | |
| R4 (°C/W) | 8 | 8 | 7 |
| R5 (°C/W) | 22 | 15 | 10 |
| R6 (°C/W) | 26 | 20 | 15 |
| C1 = C7 (W.s/°C) | 0.0008 | | |
| C2 = C8 (W.s/°C) | 0.005 | | |
| C3 (W.s/°C) | 0.05 | | |
| C4 (W.s/°C) | 0.2 | 0.1 | 0.1 |
| C5 (W.s/°C) | 0.27 | 0.8 | 1 |
| C6 (W.s/°C) | 3 | 6 | 9 |

# 5 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

## 5.1 PowerSSO-12 package information

**Figure 18. PowerSSO-12 package dimensions**

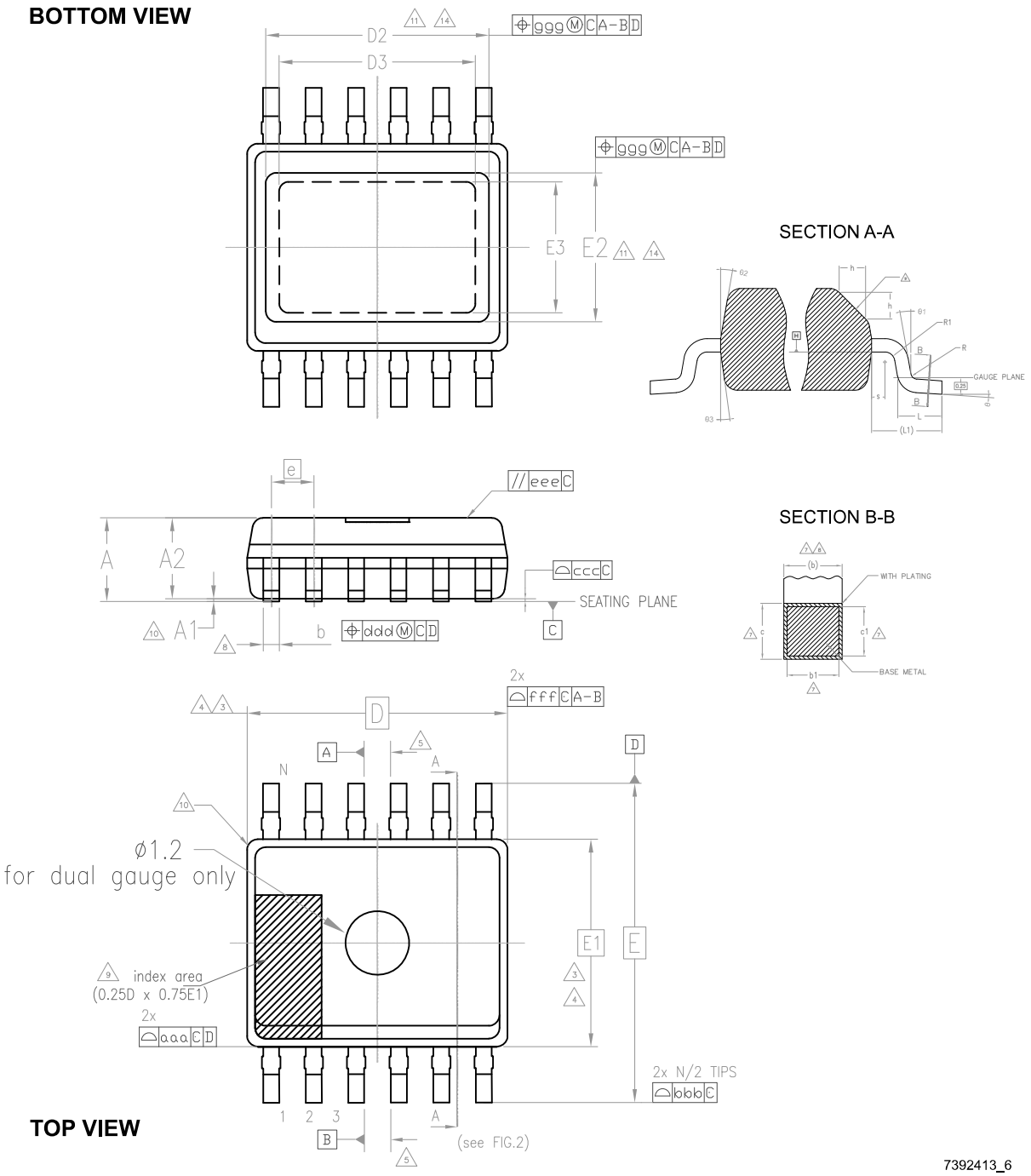


**Table 13. PowerSSO-12 mechanical data**

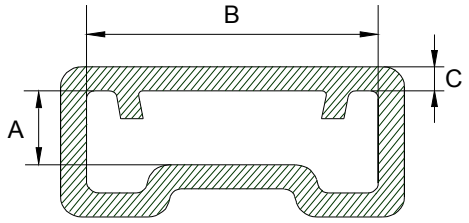
| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| θ | 0° | | 8° |
| θ1 | 0° | | |
| θ2 | 5° | | 15° |
| θ3 | 5° | | 15° |
| A | 1.25 | | 1.70 |
| A1 | 0.00 | | 0.10 |
| A2 | 1.10 | | 1.60 |
| b | 0.23 | | 0.41 |
| b1 | 0.20 | 0.25 | 0.39 |
| c | 0.19 | | 0.25 |
| c1 | 0.19 | 0.20 | 0.23 |
| D | 4.90 BSC | | |
| D2 | 3.60 | | 4.20 |
| D3 | 2.90 | | |
| e | 0.80 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| E2 | 1.90 | | 2.50 |
| E3 | 1.20 | | |
| h | 0.25 | | 0.50 |
| L | 0.40 | | 1.27 |
| L1 | 1.00 REF | | |
| N | 12 | | |
| R | 0.07 | | |
| R1 | 0.07 | | |
| S | 0.20 | | |

**Table 14. PowerSSO-12 tolerance of form and position**

| Symbol | Millimeters |
|---|---|
| aaa | 0.10 |
| bbb | 0.10 |
| ccc | 0.10 |
| ddd | 0.08 |
| eee | 0.10 |
| fff | 0.10 |
| ggg | 0.15 |

## 5.2 PowerSSO-12 packing information

**Figure 19. PowerSSO-12 tube shipment (no suffix)**




All dimensions are in mm.

| | |
|---|---|
| Base q.ty | 100 |
| Bulk q.ty | 2000 |
| Tube length ( ±0.5) | 532 |
| A | 1.85 |
| B | 6.75 |
| C ( ±0.1) | 0.6 |

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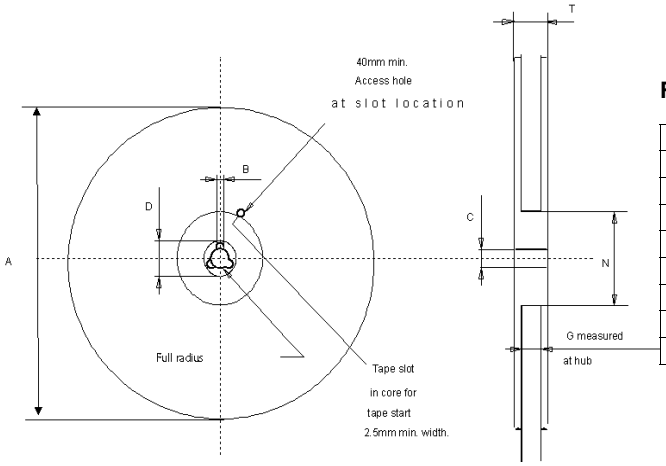
**Figure 20. PowerSSO-12 tape and reel shipment (suffix “TR”)**



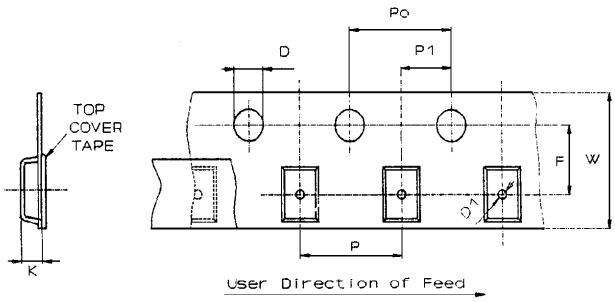

**Reel dimensions**

| | |
|---|---|
| Base q.ty | 2500 |
| Bulk q.ty | 2500 |
| A (max) | 330 |
| B (min) | 1.5 |
| C ( ±0.2) | 13 |
| F | 20.2 |
| G (+ 2 / -0) | 12.4 |
| N (min) | 60 |
| T (max) | 18.4 |

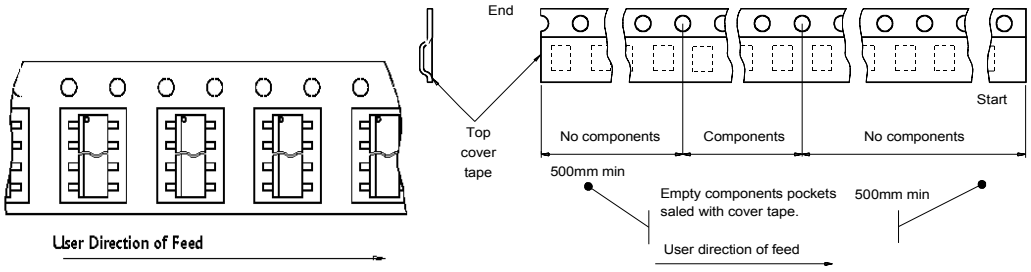
**Tape dimensions**

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

| | | |
|---|---|---|
| Tape width | W | 12 |
| Tape hole spacing | P0 (± 0.1) | 4 |
| Component spacing | P | 8 |
| Hole diameter | D ( ±0.05) | 1.5 |
| Hole diameter | D1 (min) | 1.5 |
| Hole position | F ( ±0.1) | 5.5 |
| Compartment depth | K (max) | 4.5 |
| Hole spacing | P1 ( ±0.1) | 2 |




All dimensions are in mm.



## Revision history

**Table 15. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 28-Aug-2023 | 1 | Initial release. |
| 15-Sep-2023 | 2 | Updated *Table 9. Current sense (8 V < $V_{CC}$ < 54 V)*. |
| 05-Oct-2023 | 3 | Updated *Table 5. Power section*, *Table 6. Switching ($V_{CC}$ = 48 V, $T_J$ = 25 °C)*, *Table 7. Logic inputs*, *Table 8. Protections and diagnostics*, *Table 9. Current sense (8 V < $V_{CC}$ < 54 V)* and *Table 10. Open-load detection ($V_{FR_Stby}$ = 5 V)*. |
| 06-Sep-2024 | 5 | Product classification changed from ST restricted to public. |

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