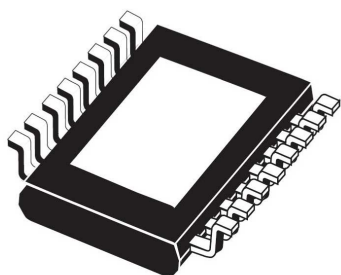


Single channel high-side driver with current sense analog feedback for automotive applications


PowerSSO-16

Features

Max transient supply voltage	V_{CC}	36 V
Operating voltage range	V_{CC}	4 to 28 V
Typ. on-state resistance (per channel)	R_{ON}	8 m Ω
Programmable current limitation (typ.)	I_{LIMH}	$I_{LIMH1} = 28$ A (default)
		$I_{LIMH2} = 42$ A
Standby current (max.)	I_{STBY}	0.5 μ A



- AEC-Q100 qualified
- Extreme low voltage operation for deep cold cranking applications (compliant with LV124, revision 2013)
- General
 - Single channel smart high-side driver with current sense analog feedback
 - Very low standby current
 - Compatible with 3 V and 5 V CMOS outputs
- Current sense diagnostic functions
 - Multiplexed analog feedback of load current with high precision proportional current mirror
 - Overload and short to ground (power limitation) indication
 - Thermal shutdown indication
 - OFF-state open-load detection (with external pull-up)
 - Output short to V_{CC} detection
- Sense enable/disable
 - Fast switch off/on
 - CCM: capacitive charging mode
 - Compatibility with companion chip L99SP08 to support STDBY_ON (parking mode)
- Protections
 - Undervoltage shutdown
 - Overvoltage clamp
 - Programmable current limitation
 - Self-limiting of fast thermal transients
 - Configurable latch-off on overtemperature or power limitation with dedicated fault reset pin
 - Loss of ground and loss of V_{CC}
 - Reverse battery through self turn-on
 - Electrostatic discharge protection

Product status link

[VN9008CAJ](#)

Product summary

Order code	VN9008CAJTR
Package	PowerSSO-16
Packing	Tape and reel

Applications

- Smart power distribution, heating systems, relay replacement and high power resistive, inductive and capacitors loads
- Protected supply for ADAS systems: radars and sensors

Description

The **VN9008CAJ** is a single channel high-side driver manufactured using ST proprietary VIPower M0-9 technology and housed in a PowerSSO-16 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS-compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as programmable current limitation, overload active management by power limitation and overtemperature shutdown with configurable latch-off and fast switch off.

A $\overline{\text{FaultRST}}$ pin unlatches the output in case of fault or disables the latch-off functionality.

A dedicated multifunction multiplexed analog output pin delivers sophisticated diagnostic functions including high precision proportional load current sense, supply voltage feedback and chip temperature sense, in addition to the detection of overload and short circuit to ground, short to V_{CC} and OFF-state open-load.

This device implements new features, as capacitive charging mode (CCM) and the compatibility with companion chip L99SP08 to support STDBY_ON functionality.

1 Block diagram and pin description

Figure 1. Block diagram

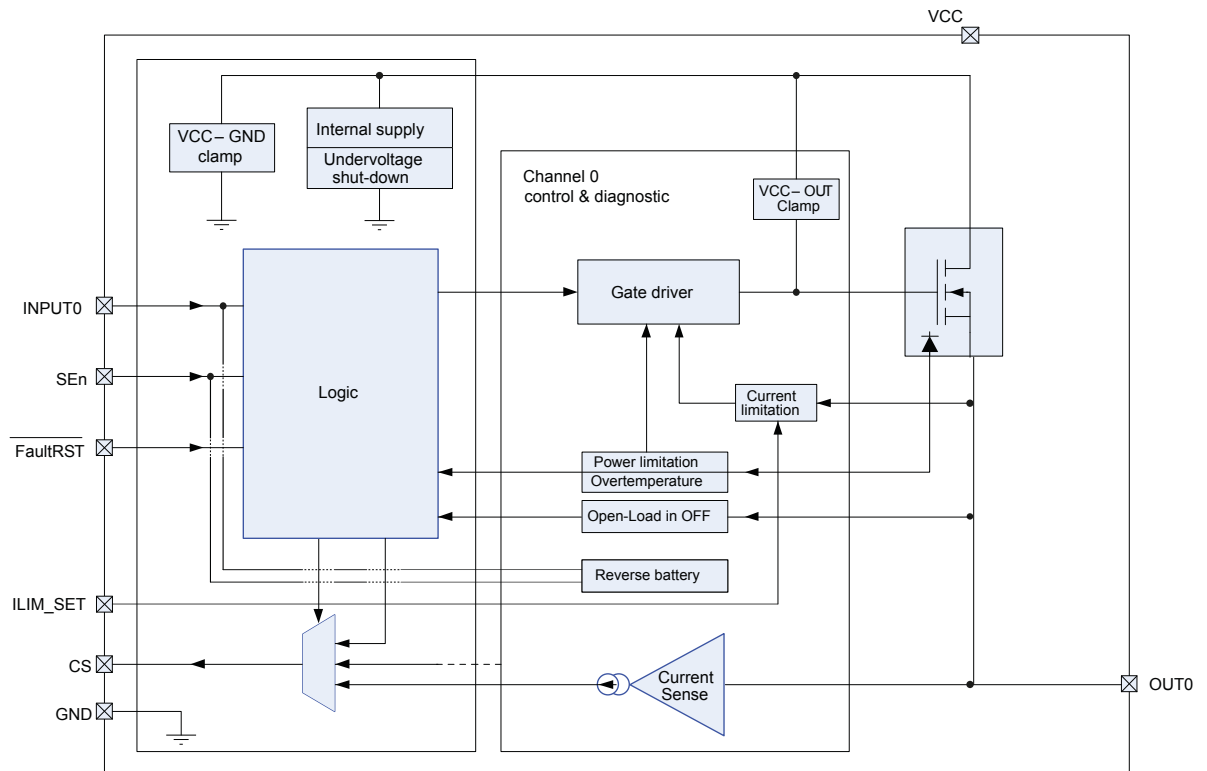
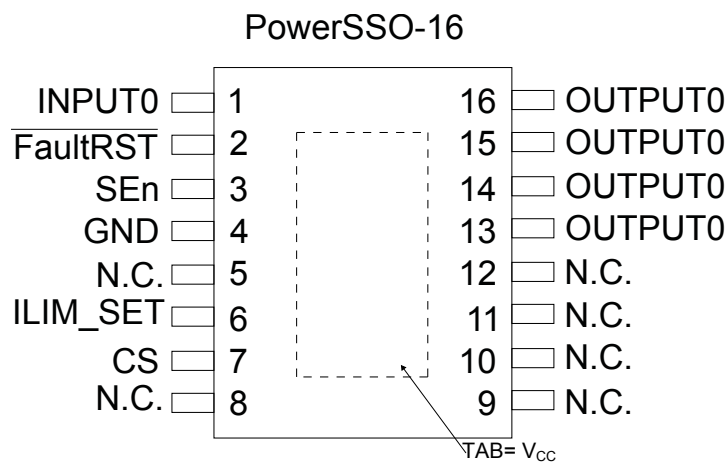


Table 1. Pin functions

Name	Function
V _{CC}	Battery connection.
OUTPUT ₀	Power outputs.
GND	Ground connection. Must be reverse battery protected by an external diode / resistor network.
INPUT ₀	Voltage controlled input pin with hysteresis, compatible with 3 V and 5 V CMOS outputs. It controls output switch state.
CS	Multiplexed analog sense output pin; it delivers a current proportional to the selected load current.
SEn	Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the CS diagnostic pin.
FaultRST	Active low compatible with 3 V and 5 V CMOS outputs pin; it unlatches the output in case of fault; If kept low, it sets the outputs in auto-restart mode.
ILIM_SET	Compatible with 3 V and 5 V CMOS outputs pin; it is used for setting the two different limitation currents: with ILIM_SET = 0 V, ILIMH = ILIMH1 (default); with ILIM_SET = 5 V, ILIMH = ILIMH2.

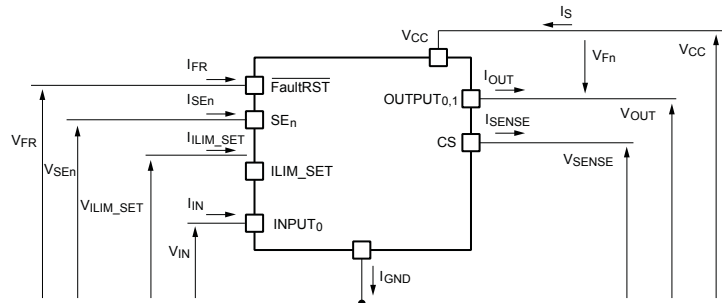
Figure 2. Configuration diagram (top view)

Table 2. Suggested connections for unused and not connected pins

Connection / pin	CS	NC	Output	Input, ILIM_SET	SEn, $\overline{\text{FaultRST}}$
Floating	Not allowed	X	X ⁽¹⁾	X	X
To ground	Through 1 k Ω resistor	X	Not allowed	Through 15 k Ω resistor	Through 15 k Ω resistor

1. X: do not care.

2 Electrical specification

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in Table 3. **Absolute maximum ratings** may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in the table below for extended periods may affect the device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	36	V
$-V_{CC}$	Reverse DC supply voltage	0.3	
V_{CCJS}	Maximum jump start voltage for single pulse short circuit protection	28	V
$-I_{GND}$	DC reverse ground pin current	200	mA
I_{OUT}	OUTPUT ₀ DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	15	
ILIM_SET	ILIM_SET DC input current	-1 to 10	mA
I_{IN}	INPUT ₀ DC input current	-1 to 10	mA
I_{SEN}	SEn DC input current	-1 to 3	
I_{FR}	FaultRST DC input current	-1 to 10	
I_{SENSE}	CS pin DC output current ($V_{GND} = V_{CC}$ and $V_{SENSE} < 0$ V)	10	mA
	CS pin DC output current in reverse ($V_{CC} < 0$ V)	-20	
E_{MAX}	Maximum switching energy (single pulse) ($T_{jstart} = 150$ °C)	32	mJ
V_{ESD}	Electrostatic discharge (JEDEC 22A-114F)	2000	V
	• INPUT ₀ , ILIM_SET	2000	V
	• CS	2000	V
	• SEn, FaultRST	4000	V
	• OUTPUT ₀	4000	V
	• VCC	4000	V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj-board}$	Thermal resistance junction-board (JEDEC JESD 51-8) ⁽¹⁾	6.8	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-2) ⁽²⁾	52.5	
$R_{thj-amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-2) ⁽¹⁾	19.9	

1. Device mounted on a four-layer 2s2p PCB

2. Device mounted on a two-layer 2s0p PCB with 2 cm² heat sink copper trace

2.3 Main electrical characteristics

7 V < V_{CC} < 28 V; -40°C < T_j < 150°C, unless otherwise specified.

All typical values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC}	Operating supply voltage		4	13	28	V
V _{USD}	Undervoltage shutdown			2.1	2.7	V
V _{USDReset}	Undervoltage shutdown reset				4.5	V
V _{USDhyst}	Undervoltage shutdown hysteresis			0.15		V
R _{ON}	On-state resistance	I _{OUT} = 7 A; T _j = 25°C		8		mΩ
		I _{OUT} = 7 A; T _j = 150°C			17.6	
		I _{OUT} = 7 A; V _{CC} = 4 V; T _j = 25°C			13.6	
		I _{OUT} = 1 A; V _{CC} = 2.7 V; V _{CC} decreasing			48	
R _{ON_ReV}	R _{DS(on)} in reverse battery condition	V _{CC} = -13 V; I _{OUT} = 7 A; T _j = 25°C		8		
V _{clamp}	Clamp voltage	I _S = 20 mA; 25°C < T _j < 150°C	36	38	45	V
		I _S = 20 mA; T _j = -40°C	36			V
I _{STBY}	Supply current in standby at V _{CC} = 13 V ⁽¹⁾	V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{FR} = V _{SEn} = 0 V; T _j = 25°C; V _{ILIM_SET} = 0 V			0.5	μA
		V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{FR} = V _{SEn} = 0 V; T _j = 85°C; V _{ILIM_SET} = 0 V ⁽²⁾			0.5	
		V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{FR} = V _{SEn} = 0 V; T _j = 125°C; V _{ILIM_SET} = 0 V			3	
I _{STBY_ON}		V _{CC} = 13 V, V _{IN} = V _{FR} = V _{SEn} = V _{ILIM_SET} = 0 V, V _{OUT} = V _{CC} , T _j = 25°C		2	15	
t _{D_STBY}	Standby mode blanking time	V _{CC} = 13 V; V _{IN} = V _{OUT} = V _{FR} = 0 V; V _{SEn} = 5 V to 0 V; V _{ILIM_SET} = 0 V	60	260	550	μs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{S(ON)}$	Supply current	$V_{CC} = 13\text{ V}$; $V_{SEn} = 0\text{ V} = V_{FR} = 0\text{ V}$; $V_{IN0} = 5\text{ V}$; $I_{OUT0} = 0\text{ A}$; $V_{ILIM_SET} = 0\text{ V}$		3.5	4.5	mA
$I_{GND(ON)}$	Control stage current consumption in ON-state. All channels active.	$V_{CC} = 13\text{ V}$; $V_{SEn} = 5\text{ V}$; $V_{FR} = V_{IN0} = 5\text{ V}$; $I_{OUT0} = 7\text{ A}$			6	mA
$I_{L(off)}$	Off-state output current at $V_{CC} = 13\text{ V}$	$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_J = 25^\circ\text{C}$	0	0.01	0.5	μA
		$V_{IN} = V_{OUT} = 0\text{ V}$; $V_{CC} = 13\text{ V}$; $T_J = 125^\circ\text{C}$	0		3	
V_F	Output - V_{CC} diode voltage	$I_{OUT} = -7\text{ A}$; $T_J = 150^\circ\text{C}$			0.7	V

1. PowerMOS leakage included.
2. Parameter specified by design; not subject to production test.

Table 6. Switching

$V_{CC} = 13\text{ V}$; $-40^\circ\text{C} < T_J < 150^\circ\text{C}$, unless otherwise specified						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}^{(1)}$	Turn-on delay time at $T_J = 25^\circ\text{C}$	$R_L = 1.85\ \Omega$	10	25	110	μs
$t_{d(off)}^{(1)}$	Turn-off delay time at $T_J = 25^\circ\text{C}$		0.1	2	15	
$(dV_{OUT}/dt)_{on}^{(1)}$	Turn-on voltage slope at $T_J = 25^\circ\text{C}$	$R_L = 1.85\ \Omega$	0.3	0.45	0.9	V/ μs
$(dV_{OUT}/dt)_{off}^{(1)}$	Turn-off voltage slope at $T_J = 25^\circ\text{C}$		0.9	4	7.5	
W_{ON}	Switching energy losses at turn-on (t_{won})	$R_L = 1.85\ \Omega$	—	0.6	1.6 ⁽²⁾	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	$R_L = 1.85\ \Omega$	—	0.08	0.25 ⁽²⁾	mJ
$t_{SKEW}^{(1)}$	Differential Pulse skew ($t_{PHL} - t_{PLH}$)	$R_L = 1.85\ \Omega$	-90	-40	10	μs
$t_{WAKE-UP}$	Turn-on delay time at $T_J = 25^\circ\text{C}$ (exit from stby)	$R_L = 1.85\ \Omega$			100	μs
t_{switch_off}	Turn-off time at $T_J = 25^\circ\text{C}$	$R_L = 1.85\ \Omega$	0.1		50	μs

1. See Figure 4. Switching time and pulse skew.
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 7. Logic inputs

$7\text{ V} < V_{CC} < 28\text{ V}$; $-40^\circ\text{C} < T_J < 150^\circ\text{C}$						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
INPUT characteristics						
V_{IL}	Input low level voltage				0.9	V
I_{IL}	Low level input current	$V_{IN} = 0.9\text{ V}$	1			μA
V_{IH}	Input high level voltage		2.1			V
I_{IH}	High level input current	$V_{IN} = 2.1\text{ V}$			10	μA

7 V < V _{CC} < 28 V; -40°C < T _J < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{I(hyst)}	Input hysteresis voltage		0.2			V
V _{ICL}	Input clamp voltage	I _{IN} = 1 mA	6		8.5	V
		I _{IN} = -1 mA		-0.7		
FaultRST characteristics						
V _{FRL}	Input low level voltage				0.9	V
I _{FRL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{FRH}	Input high level voltage		2.1			V
I _{FRH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{FR(hyst)}	Input hysteresis voltage		0.2			V
V _{FRCL}	Input clamp voltage	I _{IN} = 1 mA	6		8.5	V
		I _{IN} = -1 mA		-0.7		
SEn characteristics (7 V < V _{CC} < 18 V)						
V _{SEnL}	Input low level voltage				0.9	V
I _{SEnL}	Low level input current	V _{IN} = 0.9 V	1			μA
V _{SEnH}	Input high level voltage		2.1			V
I _{SEnH}	High level input current	V _{IN} = 2.1 V			10	μA
V _{SEn(hyst)}	Input hysteresis voltage		0.2			V
V _{SEnCL}	Input clamp voltage	I _{IN} = 1 mA	9		12	V
		I _{IN} = -1 mA		-0.7		
ILIM_SET characteristics (7 V < V _{CC} < 18 V)						
V _{LILIM_SET}	ILIM_SET low level voltage				0.9	V
I _{LILIM_SET}	Low level ILIM_SET current	V _{IN} = 0.9 V	1			μA
V _{HILIM_SET}	ILIM_SET high level voltage		2.1			V
I _{HILIM_SET}	High level ILIM_SET current	V _{IN} = 2.1 V			10	μA
V _{ILIM_SET(hyst)}	ILIM_SET hysteresis voltage	I _{IN} = 1 mA	0.2			
V _{CLILIM_SET}	ILIM_SET clamp voltage	I _{IN} = -1 mA	6		8.5	V
				-0.7		

Table 8. Protections

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{LIMH} ⁽¹⁾	DC short-circuit current	V _{CC} = 16 V; T _J = -40°C; VLIM_SET = 0 V	-15%	32	15%	A
		V _{CC} = 16 V; T _J = -40°C; VLIM_SET = 5 V	-15%	48	15%	
		V _{CC} = 16 V; T _J = +150°C; VLIM_SET = 0 V	-15%	22.5	15%	
		V _{CC} = 16 V; T _J = +150°C; VLIM_SET = 5 V	-15%	33.5	15%	

7 V < V _{CC} < 18 V; -40°C < T _J < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{LIMH} at 22 V	DC short-circuit current at 22 V	V _{CC} > 20 V; T _J = 25°C		28		A
T _{TSD}	Shutdown temperature		150	175	210	°C
	Shutdown temperature (V _{CC} decreasing)	V _{CC} = 2.7 V	140			
T _{RS}	Thermal reset of fault diagnostic indication	V _{FR} = 0 V; V _{SEn} = 5 V	135			
T _{HYST}	Thermal hysteresis (T _{TSD} - T _{RS}) ⁽²⁾			7		
ΔT _{J_SD}	Dynamic temperature			35		K
t _{LATCH_RST}	Fault reset time for output unlatch ⁽²⁾	V _{FR} = 5 V to 0 V; V _{SEn} = 5 V V _{IN0} = 5 V	3	10	20	μs
t _{D_Restart}	Latch-OFF delay time before automatic restart			50	75	ms
V _{DEMAG}	Turn-off output voltage clamp	I _{OUT} = 1 A; L = 6 mH; T _J = -40°C	V _{CC} - 36			V
		I _{OUT} = 1 A; L = 6 mH; T _J = 25°C to 150°C	V _{CC} - 36	V _{CC} - 38	V _{CC} - 45	V

1. I_{LIMH}, guaranteed between 7 V and 16 V, -40°C < T_J < 150°C
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 9. CCM - Capacitive loads charging mode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{MAX}	Max capacitive load ⁽¹⁾	V _{CC} = 16 V, T _J = 85 °C, t _{CMAX} = 50 ms, ESR = 40mΩ	-	8	-	mF

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 10. Current Sense

7 V < V _{CC} < 18 V; -40°C < T _J < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{SENSE_CL}	CS clamp voltage	V _{SEn} = 0 V; I _{SENSE} = 1 mA	-9	-8	-7	V
		V _{SEn} = 0 V; I _{SENSE} = -1 mA		7		
CurrentSense characteristics						
K _{LED}	I _{OUT} /I _{SENSE}	I _{OUT} = 100 mA; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-35%	14800	+35%	
dK _{LED} /K _{LED} ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 100 mA; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-25		25	%
K ₀	I _{OUT} /I _{SENSE}	I _{OUT} = 0.7 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-25%	14800	25%	
dK ₀ /K ₀ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 0.7 A; V _{SENSE} = 0.5 V; V _{SEn} = 5 V	-20		20	%

7 V < V _{CC} < 18 V; -40°C < T _J < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K ₁	I _{OUT} /I _{SENSE}	I _{OUT} = 1.4 A; V _{SENSE} = 3.5 V; V _{SEn} = 5 V	-15%	14800	15%	
dK ₁ /K ₁ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 1.4 A; V _{SENSE} = 3.5 V; V _{SEn} = 5 V	-10		10	%
K ₂	I _{OUT} /I _{SENSE}	I _{OUT} = 7 A; V _{SENSE} = 3.5 V; V _{SEn} = 5 V	-7%	14800	7%	
dK ₂ /K ₂ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 7 A; V _{SENSE} = 3.5 V; V _{SEn} = 5 V	-7		7	%
K ₃	I _{OUT} /I _{SENSE}	I _{OUT} = 21 A; V _{SENSE} = 3.5 V; V _{SEn} = 5 V; V _{LIM_SET} = 5V	-7%	14800	7%	
		I _{OUT} = 18 A; V _{SENSE} = 3.5 V; V _{SEn} = 5 V; V _{LIM_SET} = 0V	-7%	14800	7%	
dK ₃ /K ₃ ^{(1) (2)}	Current sense ratio drift	I _{OUT} = 21 A; V _{SENSE} = 3.5 V; V _{SEn} = 5 V	-5		5	%
I _{SENSE0}	CurrentSense leakage current	CS disabled: V _{SEn} = 0 V	0		0.5	μA
		CS disabled: -1 V < V _{SENSE} < 5 V ⁽¹⁾	-1		1	
		CS enabled: V _{SEn} = 5 V; Channel ON; V _{IN0} = 5 V; I _{OUT0} = 0 A;	0		3	
		CS enabled: V _{SEn} = 5 V; Channel OFF; V _{IN0} = 0 V; I _{OUT0} = 0 A	0		1	
V _{OUT_MSD} ⁽¹⁾	Output voltage for CS shutdown	V _{SEn} = 5 V; R _{SENSE} = 2.7 kΩ; E.g. Ch ₀ : V _{IN0} = 5 V; I _{OUT0} = 7 A		5		V
V _{SENSE_SAT}	Current sense saturation voltage	V _{CC} = 7 V; R _{SENSE} = 10 kΩ; V _{SEn} = 5 V; V _{IN0} = 5 V; I _{OUT0} = 21 A; T _J = -40°C; V _{LIM_SET} = 5V	4.8			V
		V _{CC} = 7 V; R _{SENSE} = 10 kΩ; V _{SEn} = 5 V; V _{IN0} = 5 V; I _{OUT0} = 18 A; T _J = -40°C; V _{LIM_SET} = 0V	4.8			V
I _{SENSE_SAT} ⁽¹⁾	CS saturation current	V _{CC} = 7 V; V _{SENSE} = 3.5 V; V _{IN0} = 5 V; V _{SEn} = 5 V; T _J = 150°C	2			mA
I _{OUT_SAT} ⁽¹⁾	Output saturation current	V _{CC} = 7 V; V _{SENSE} = 3.5 V; V _{IN0} = 5 V; V _{SEn} = 5 V; T _J = 150°C	19			A
OFF-state diagnostic						
V _{OL}	OFF-state open-load voltage detection threshold	V _{SEn} = 5 V; Ch OFF; V _{IN0} = 0 V;	2	3	4	V
I _{L(off2)}	OFF-state output sink current	V _{IN} = 0 V; V _{OUT} = V _{OL} ; T _J = -40°C to 125°C	-150	-40	-5	μA
t _{DSTKON}	OFF-state diagnostic delay time from falling edge of INPUT (see Figure 6. T _{DSTKON})	V _{SEn} = 5 V; Ch ON to OFF transition; V _{IN0} = 5 V to 0 V; I _{OUT0} = 0 A; V _{OUT} = 4 V	150	260	400	μs
t _{D_OL_V}	Settling time for valid OFF-state open load diagnostic indication from rising edge of SE _n	V _{IN} = 0 V; V _{FR} = 0 V; V _{OUT0} = 4 V; V _{SEn} = 0 V to 5 V			60	μs

7 V < V _{CC} < 18 V; -40°C < T _j < 150°C						
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{D_VOL}	OFF-state diagnostic delay time from rising edge of V _{OUT}	V _{SEn} = 5 V; Ch OFF; V _{IN0} = 0 V; V _{OUT} = 0 V to 4 V		5	30	μs
Fault diagnostic feedback (see Table 11. Truth table)						
V _{SENSEH}	MultiSense output voltage in fault condition	13 V < V _{CC} < 18 V; Ch0 in open load; R _{SENSE} = 0.7 kΩ; V _{IN0} = 0 V; V _{SEn} = 5 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V	5		7.5	V
		V _{CC} = 7 V; Ch0 in open load; R _{SENSE} = 0.7 kΩ; V _{IN0} = 0 V; V _{SEn} = 5 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V	4.3			
I _{SENSEH}	CurrentSense output current in fault condition	13 V < V _{CC} < 18 V; V _{SENSE} = 5 V; Ch0 in open load; V _{IN0} = 0 V; V _{SEn} = 5 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V	7	8.6	12	mA
		V _{CC} = 7 V; V _{SENSE} = 5 V; Ch0 in open load; V _{IN0} = 0 V; V _{SEn} = 5 V; I _{OUT0} = 0 A; V _{OUT0} = 4 V	4.4			
CurrentSense timings (current sense mode - see Figure 5. Current sense timings (current sense mode)) ⁽³⁾						
t _{DSENSE1H}	Current sense settling time from rising edge of SEn	V _{IN} = 5 V; V _{SEn} = 0 V to 5 V; R _{SENSE} = 1 kΩ; R _L = 1.85 Ω			60	μs
t _{DSENSE1L}	Current sense disable delay time from falling edge of SEn	V _{IN} = 5 V; V _{SEn} = 5 V to 0 V; R _{SENSE} = 1 kΩ; R _L = 1.85 Ω		5	20	μs
t _{DSENSE2H}	Current sense settling time from rising edge of INPUT	V _{IN} = 0 V to 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 1.85 Ω		100	250	μs
Δt _{DSENSE2H}	Current sense settling time from rising edge of I _{OUT} (dynamic response to a step change of I _{OUT})	V _{IN} = 5 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; I _{SENSE} = 90 % of I _{SENSEMAX} ; R _L = 1.85 Ω			100	μs
t _{DSENSE2L}	Current sense turn-off delay time from falling edge of INPUT	V _{IN} = 5 V to 0 V; V _{SEn} = 5 V; R _{SENSE} = 1 kΩ; R _L = 1.85 Ω		70	250	μs
t _{DSENSE3H}	Current sense latch-OFF filtering time		1.4	2.0	2.6	ms

1. Parameter specified by design; not subject to production test.
2. All values refer to V_{CC} = 13 V; T_j = 25°C, unless otherwise specified.
3. Transition delay is measured up to +/- 10% of final conditions.

Figure 4. Switching time and pulse skew

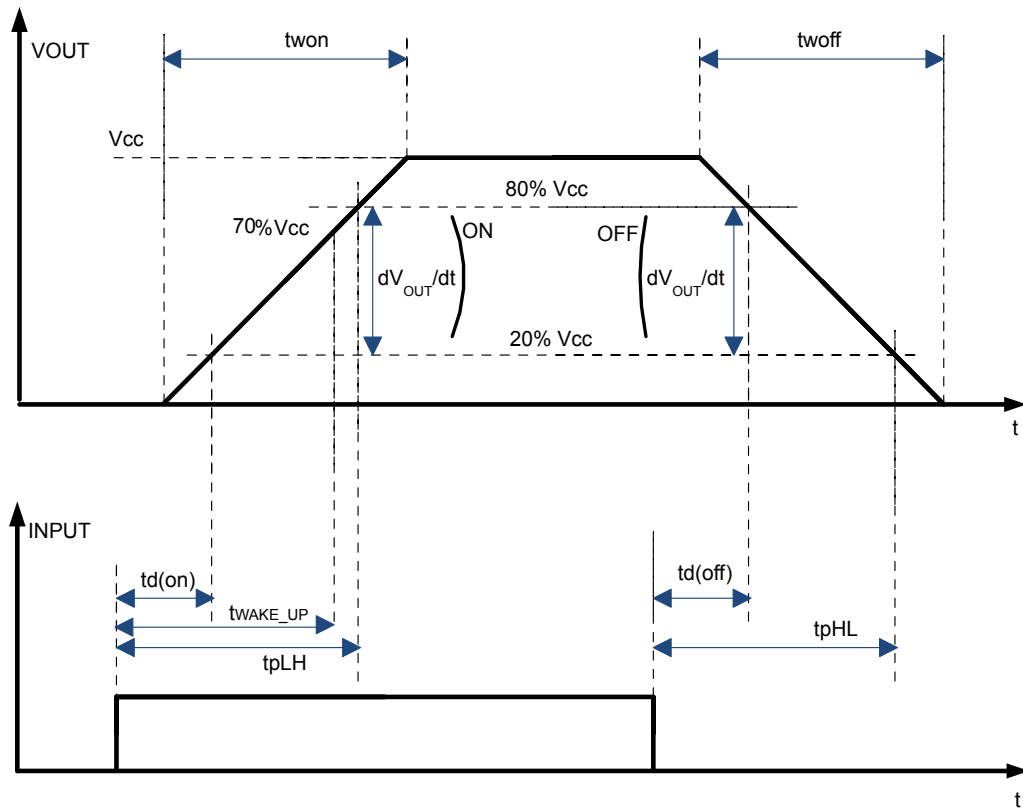
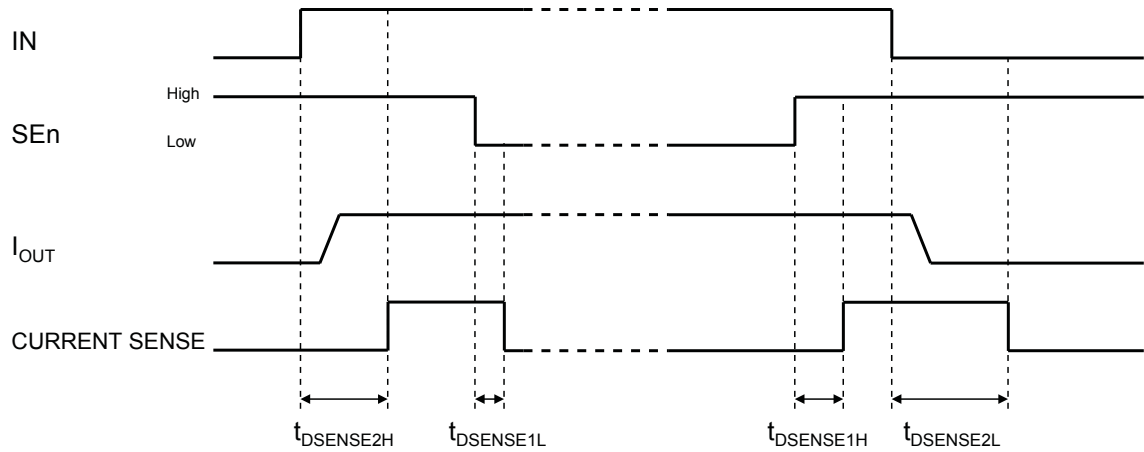
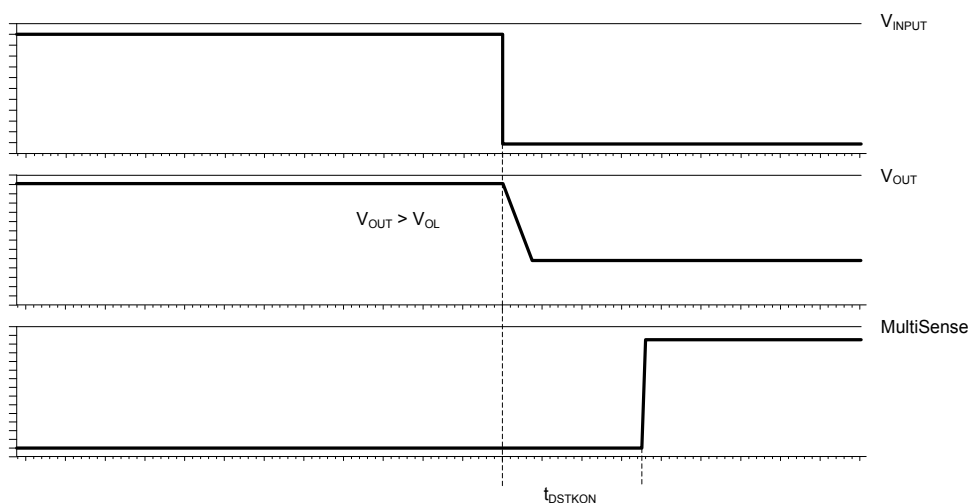


Figure 5. Current sense timings (current sense mode)



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Figure 6. T_{DSTKON}


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Table 11. Truth table

Mode	Conditions	IN _x	FR	SEn	OUT _x	CS	ILIM_SET	Comments
Standby	All logic inputs low	L	L	L	L	Hi-Z	L	Low quiescent current consumption
Normal	Nominal load connected; $T_j < 150\text{ }^{\circ}\text{C}$	L	X	See ⁽¹⁾	L	See ⁽¹⁾	X	
		H	L		H	See ⁽¹⁾	X	Outputs configured for auto-restart
		H	H		H	See ⁽¹⁾	X	Outputs configured for latch-off Section 2.3 Main electrical characteristics
Overload	Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j_SD}$	L	X	See ⁽¹⁾	L	See ⁽¹⁾	X	
		H	L		H	See ⁽¹⁾	X	Output cycles with temperature hysteresis
		H	H		L	See ⁽¹⁾	X	Output latches-off Section 2.3 Main electrical characteristics
Undervoltage	$V_{CC} < V_{USD}$ (falling)	X	X	X	L L	Hi-Z Hi-Z	X	Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising)
OFF-state diagnostics	Short to V_{CC}	L	X	See ⁽¹⁾	H	See ⁽¹⁾	X	
	Open-load	L	X		H	See ⁽¹⁾	X	External pull-up
Negative output voltage	Inductive loads turn-off	L	X	See ⁽¹⁾	$< 0\text{ V}$	See ⁽¹⁾	X	

 1. Refer to [Table 12. Current Sense multiplexer addressing](#)
Table 12. Current Sense multiplexer addressing

SEn	MUX channel	MultiSense output			
		Normal mode	Overload	OFF-state diag.	Negative output
L	N.A.	Hi-Z			
H	Channel 0 diagnostic	$I_{SENSE} = 1/K * I_{OUT0}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z

2.4 Waveforms

Figure 7. Latch-off mode - Intermittent short circuit

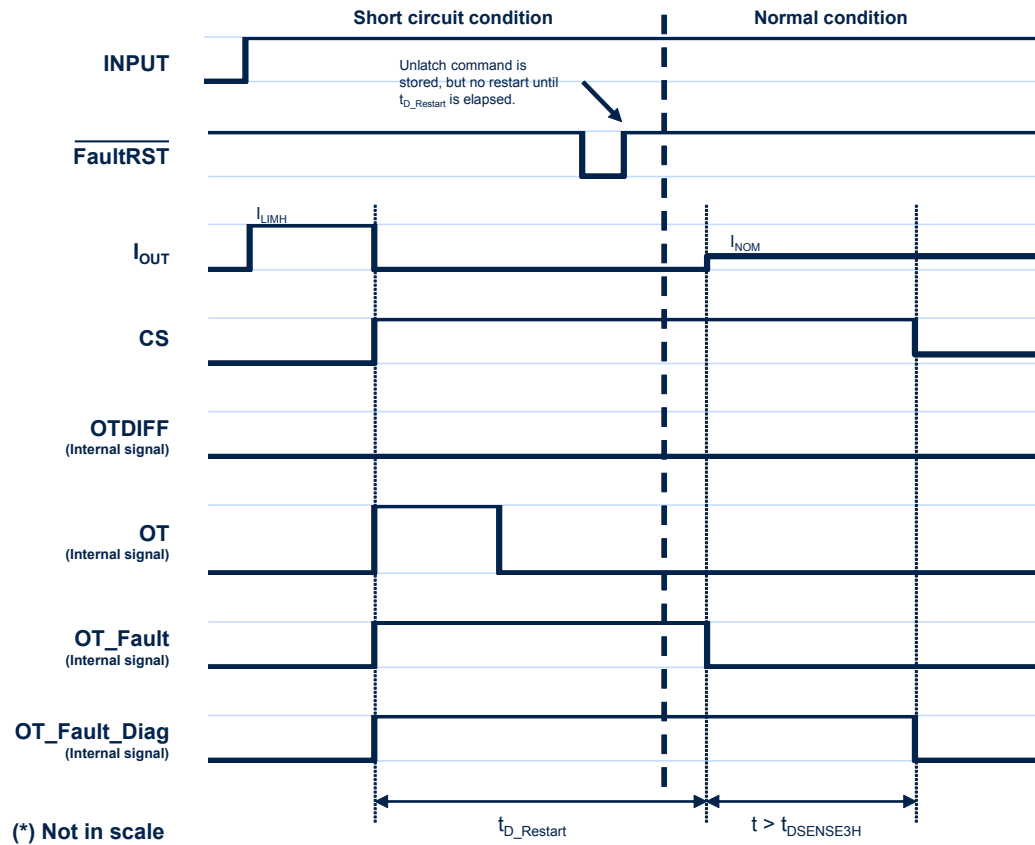


Figure 8. Auto-restart mode - Intermittent short circuit

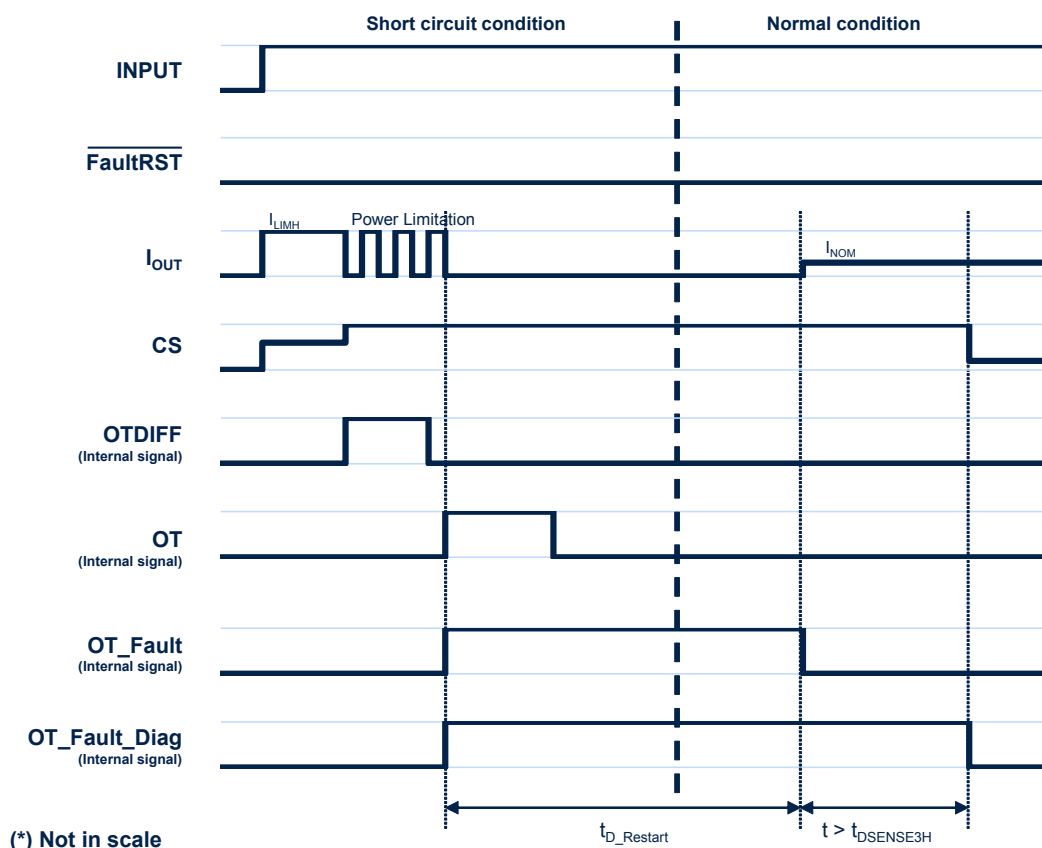


Figure 9. Auto-restart mode - Permanent short circuit

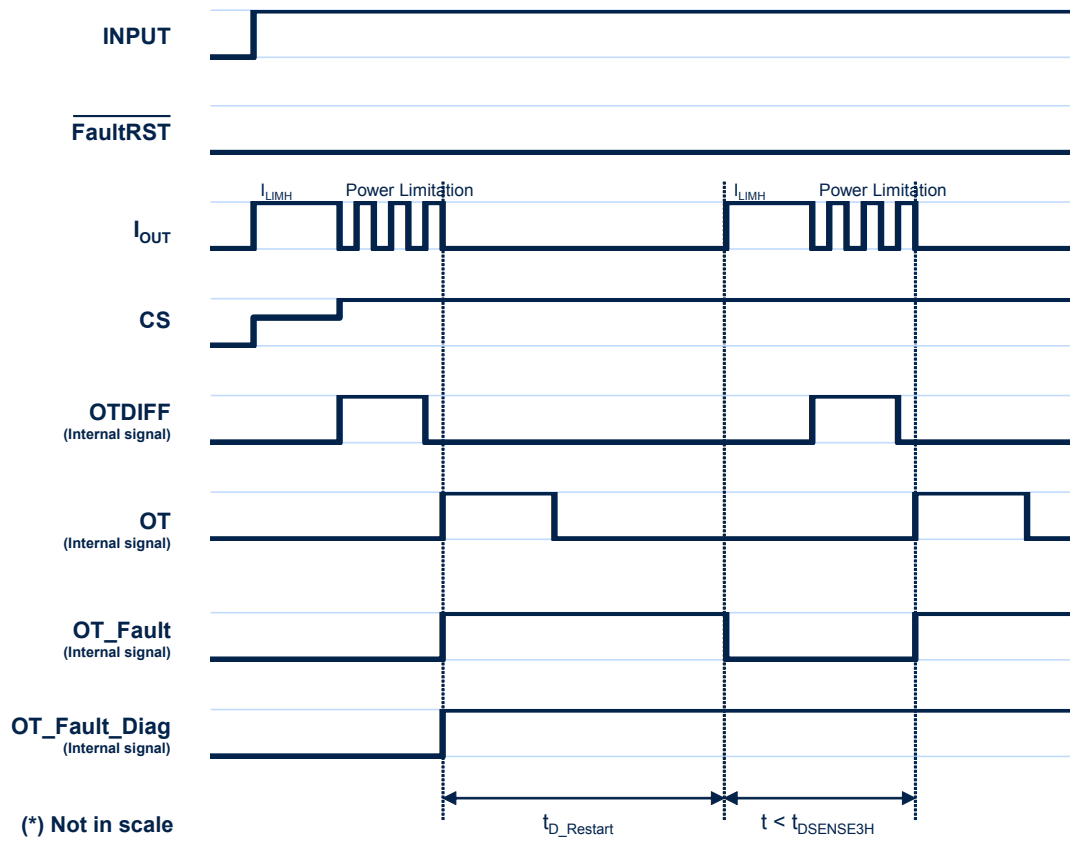


Figure 10. Standby mode activation

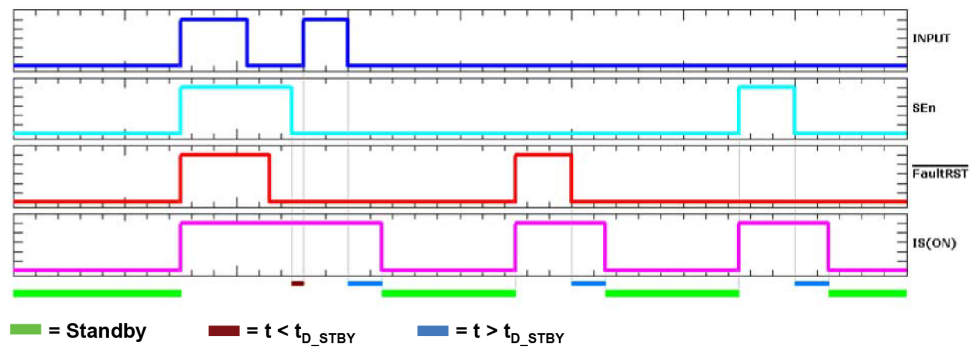
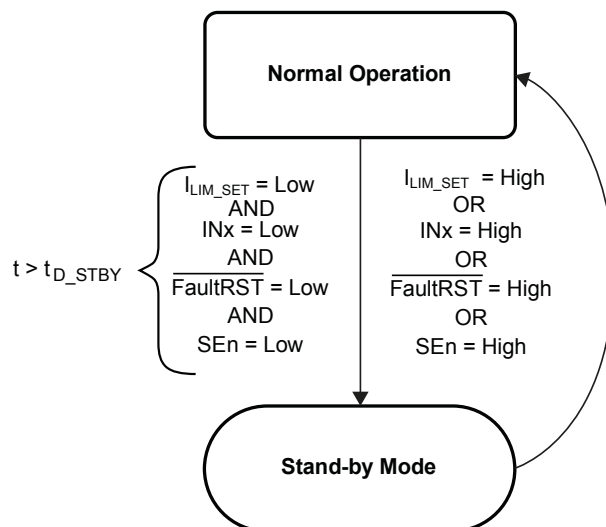


Figure 11. Standby state diagram



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3 Protections

3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing ΔT_J through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as ΔT_J exceeds the safety level of ΔT_{J_SD} . According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled ($\overline{\text{FaultRST}} = \text{Low}$) or remain off ($\overline{\text{FaultRST}} = \text{High}$). The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175 °C), it automatically switches off and the diagnostic indication is triggered. According to the voltage level on the $\overline{\text{FaultRST}}$ pin, the device switches on again as soon as its junction temperature drops to T_R ($\overline{\text{FaultRST}} = \text{Low}$) or remains off ($\overline{\text{FaultRST}} = \text{High}$).

3.3 Current limitation

The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (for example bonding wires, wiring harness, connectors, loads, etc.) from excessive current flow. Consequently, in case of short-circuit, overload or during load power-up, the output current is clamped to a safety level, I_{LIMH} , by operating the output power MOSFET in the active region.

3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches a negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, V_{DEMag} , allowing the inductor energy to be dissipated without damaging the device.

4 Capacitive charging mode (CCM)

The capacitive charging mode (CCM) is an operative condition, available in normal operation (channel in on state).

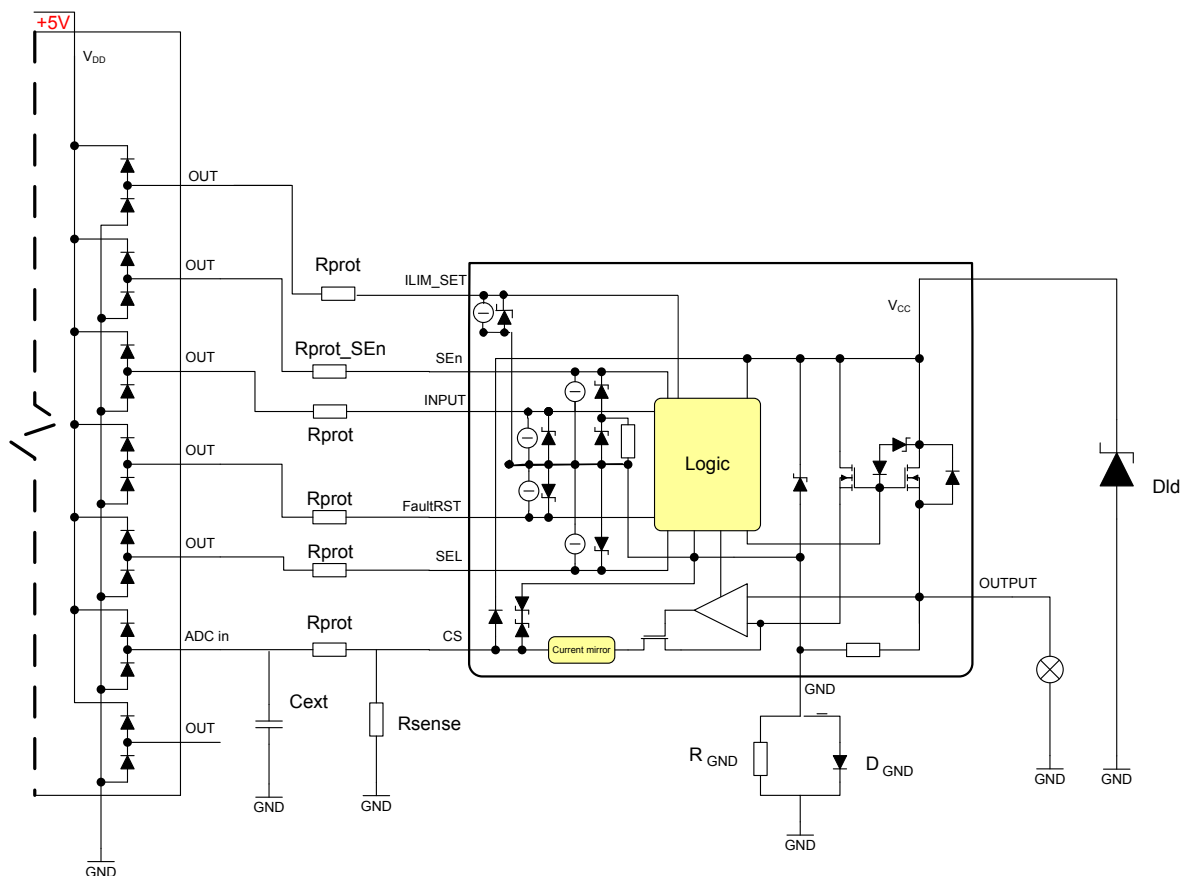
The capacitive charging mode charges capacitors with a burst of ILIMH pulses, provided that the total impedance is low enough to reach ILIMH when charging the capacitor. If ILIMH is not reached, the capacitor is charged with a single continuous charging pulse.

If the ESR of the connected capacitor and the total output line impedance is low enough to let the channel reach its ILIMH value, the channel will turn off after the differential thermal threshold of DTJ_SD has been reached and autonomously turned on again after the differential thermal hysteresis goes below a certain threshold.

Thanks to the lower values of ΔT_{J_SD} and I_{LIMH} , compared to standard M0-9 HSD devices which don't implement this feature, all the devices with CCM can sustain the loading of capacitors up to C_{MAX} even in high ambient temperature conditions.

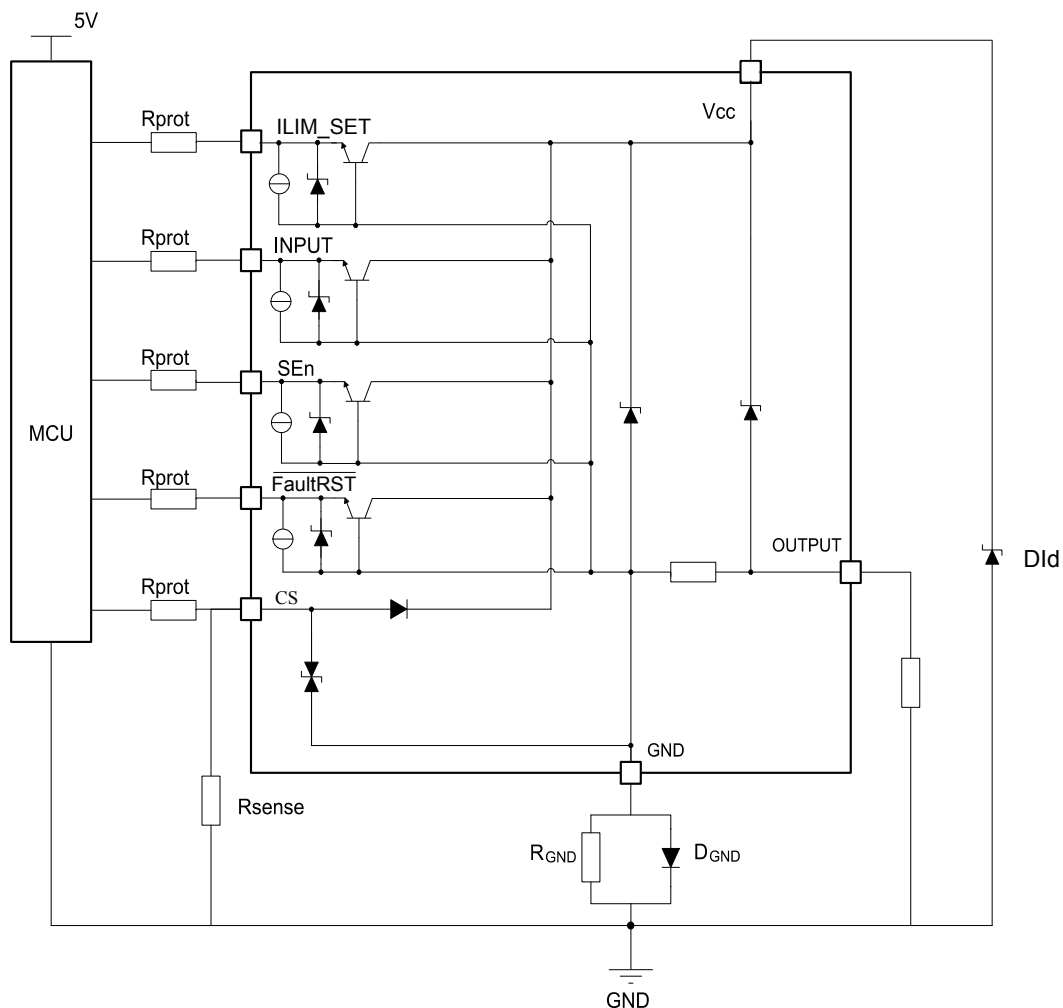
5

Figure 12. Application diagram



5.1 GND protection network against reverse battery

Figure 13. Simplified internal structure



5.1.1 Diode (DGND) in the ground line

A resistor (typ. $R_{GND} = 4.7 \text{ k}\Omega$) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift ($\approx 600 \text{ mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

5.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the V_{CC} pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in [Table 13. ISO 7637-2 - electrical transient conduction along supply line](#).

Test pulses are applied directly to DUT (device under test) both in ON and OFF state and in accordance to ISO 7637-2:2011(E), chapter 4.

The DUT is intended as the current device only, with external components as shown in [Figure 14. M0-9 application schematic](#).

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: "The function does not perform as designed during the test but returns automatically to normal operation after the test".

Table 13. ISO 7637-2 - electrical transient conduction along supply line

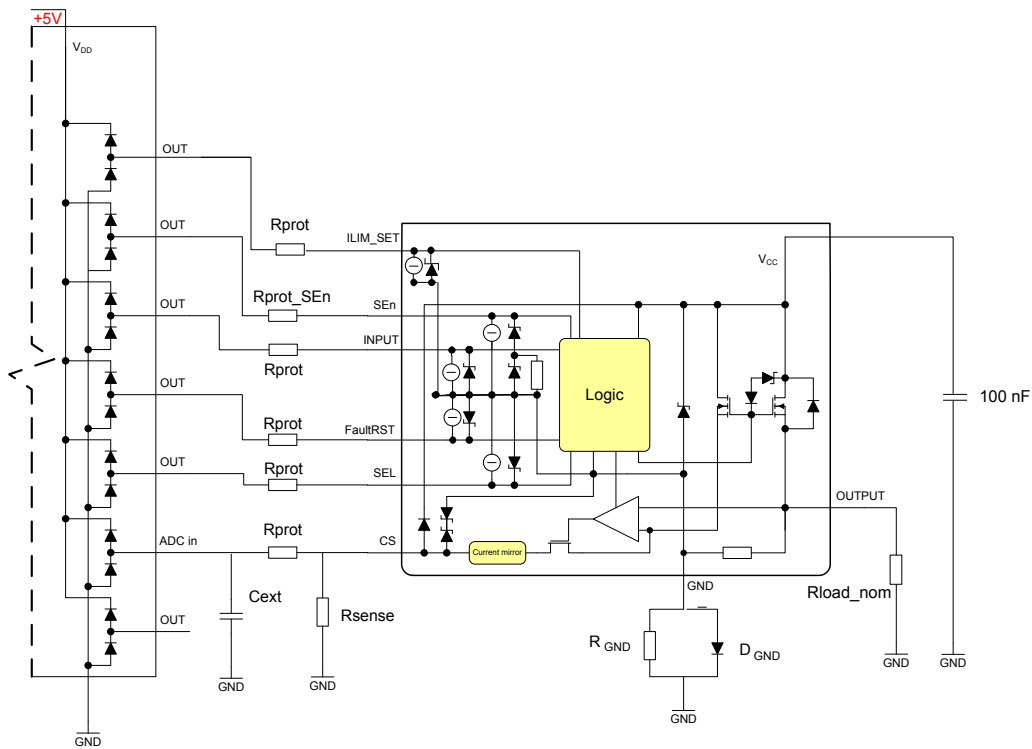
Test Pulse 2011(E)	Test pulse severity level with Status II functional performance status		Minimum number of pulses or test time	Burst cycle / pulse repetition time		Pulse duration and pulse generator internal impedance
	Level	$U_S^{(1)}$		min	max	
1	III	-112 V	500 pulses	0.5 s		2 ms, 10 Ω
2a	III	+55 V	500 pulses	0.2 s	5 s	50 μs , 2 Ω
3a	IV	-220 V	1h	90 ms	100 ms	0.1 μs , 50 Ω
3b	IV	+150 V	1h	90 ms	100 ms	0.1 μs , 50 Ω
4 ⁽²⁾	IV	-7 V	1 pulse			100 ms, 0.01 Ω
Load dump according to ISO 16750-2:2010						
Test B ⁽³⁾		35 V	5 pulses	1 min		400 ms, 2 Ω

1. U_S is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.

2. Test pulse from ISO 7637-2:2004(E).

3. With 35 V external suppressor referred to ground ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$).

Figure 14. M0-9 application schematic



5.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation

$$\frac{V_{ccpeak}}{I_{latchup}} \leq R_{prot} \leq \frac{(V_{OH\mu C} - V_{IH} - V_{GND})}{I_{IHmax}} \quad (1)$$

Calculation example:

For $V_{CCpeak} = -150 \text{ V}$; $I_{latchup} \geq 20 \text{ mA}$; $V_{OH\mu C} \geq 4.5 \text{ V}$

$7.5 \text{ k}\Omega \leq R_{prot} \leq 140 \text{ k}\Omega$.

Recommended values: $R_{prot} = 15 \text{ k}\Omega$

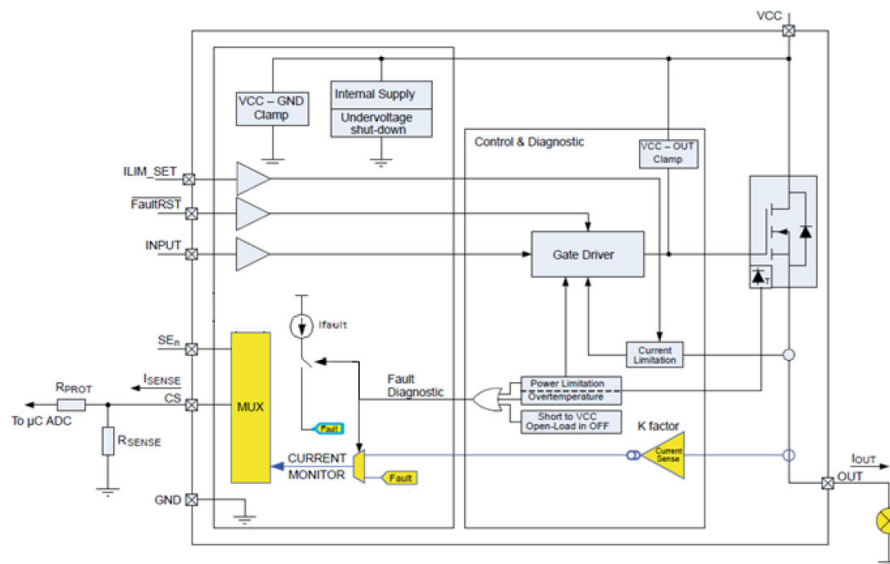
5.4 CS - analog current sense

Diagnostic information on device and load status is provided by an analog output pin (CS) delivering the following signals:

- Current monitor: current mirror of channel output current

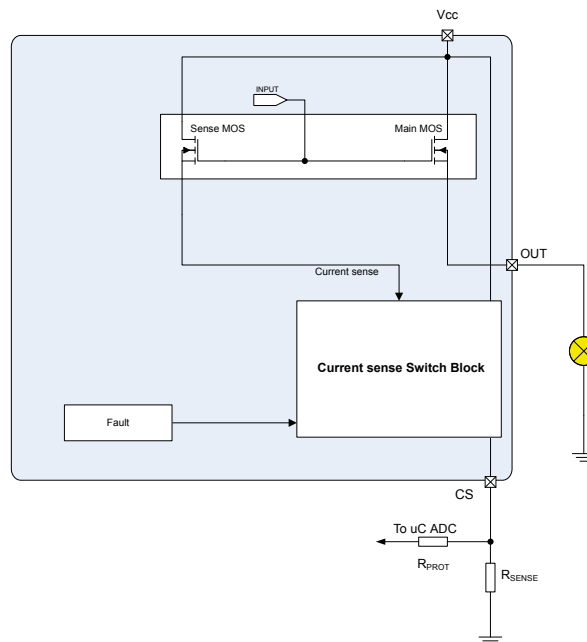
Those signals are routed through an analog multiplexer which is configured and controlled by means of SE_n pins, according to the address map in [Table 12. Current Sense multiplexer addressing](#).

Figure 15. Current Sense and diagnostic – block diagram



5.4.1 Principle of current sense signal generation

Figure 16. Current sense block diagram



Current sense

The output is capable of providing:

- Current mirror proportional to the load current in normal operation, delivering current proportional to the load according to a known ratio named K
- Diagnostics flag in fault conditions delivering a current I_{SENSEH} converted to a voltage (V_{SENSEH}) by using an external sense resistor in case of:
 - Power limitation, overtemperature in on-state.
 - Short to VCC / open-load in off-state (with external pull-up resistor) condition.

The current delivered by the current sense circuit, I_{SENSE} , can be easily converted into a voltage V_{SENSE} by using an external sense resistor, R_{SENSE} , allowing continuous load monitoring and abnormal condition detection.

Normal operation (channel ON, no fault, SEN active)

While the device is operating in normal conditions (no fault intervention), V_{SENSE} calculation can be done using simple equations.

Current provided by MultiSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on R_{SENSE} : $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where:

- V_{SENSE} is the voltage measurable on the R_{SENSE} resistor
- I_{SENSE} is the current provided from CurrentSense pin in current output mode
- I_{OUT} is the current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying the ratio between I_{OUT} and I_{SENSE} .

Failure flag indication

When the device is in ON state, whenever a protection is triggered and the device is in current mode, the internal logic sets the CurrentSense output in fault mode, disabling the current monitor circuit and providing a particular internal signal which activates a current generator (see [Figure 15](#)). In Fault condition the CS pin supplies a current I_{SENSEH} (typically 8 mA), that can be easily converted into a voltage by using an external sense resistor R_{SENSE} (V_{SENSEH} = R_{SENSE} * I_{SENSEH})

In any case, the current sourced by the CurrentSense in this condition is limited to I_{SENSEH} .

The typical behavior in case of overload or hard short-circuit is shown in Waveforms.

Figure 17. Analog HSD – open-load detection in off-state

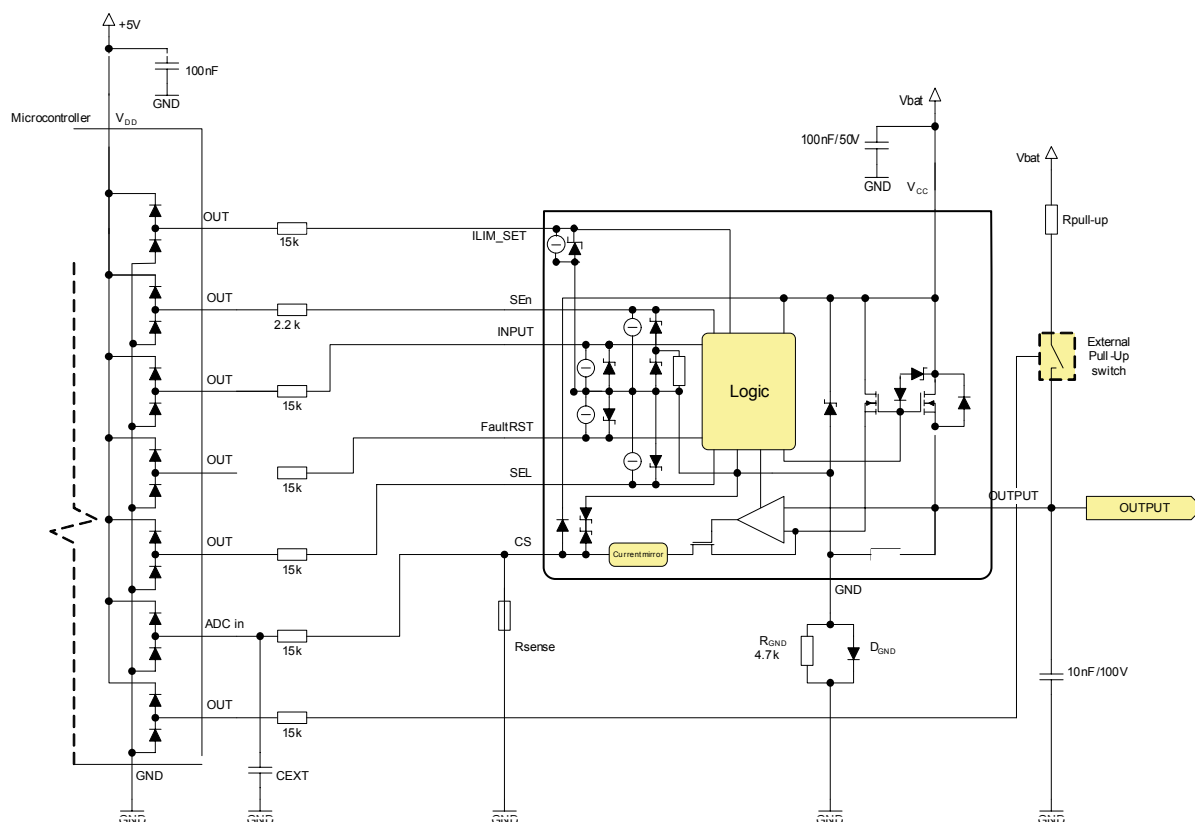
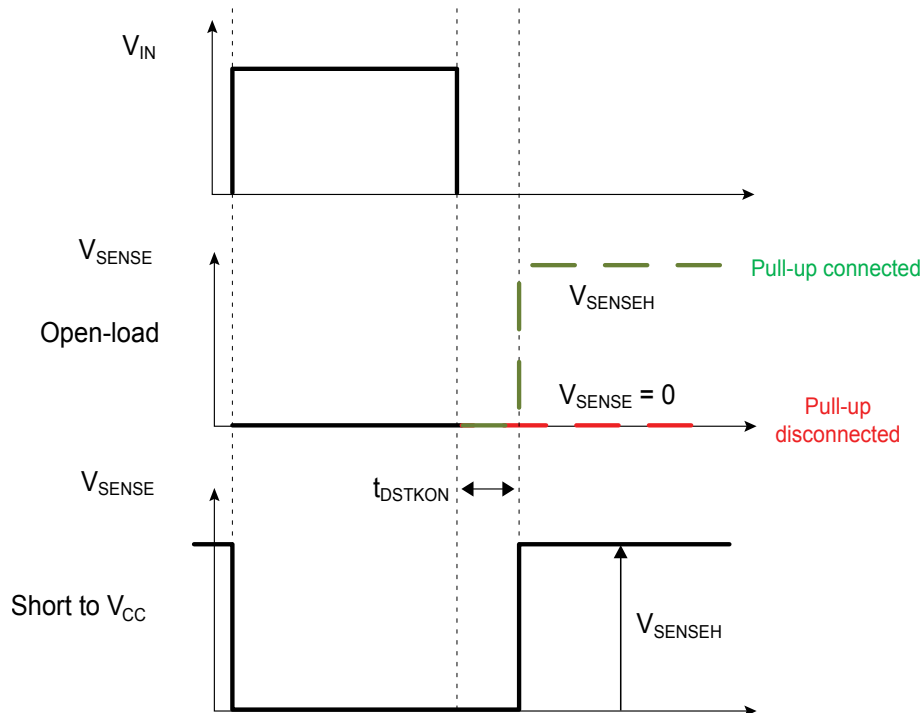


Figure 18. Open-load / short to V_{CC} condition

Table 14. CS pin levels in off-state

Condition	Output	CS	SEn
Open-load	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H
Short to V _{CC}	$V_{OUT} > V_{OL}$	Hi-Z	L
		V_{SENSEH}	H
Nominal	$V_{OUT} < V_{OL}$	Hi-Z	L
		0	H

5.4.2 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short-circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable that V_{PU} is switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

R_{PU} must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min@4V}} \quad (2)$$

6 Maximum demagnetization energy ($V_{CC} = 16\text{ V}$)

Figure 19. Maximum turn off current versus inductance

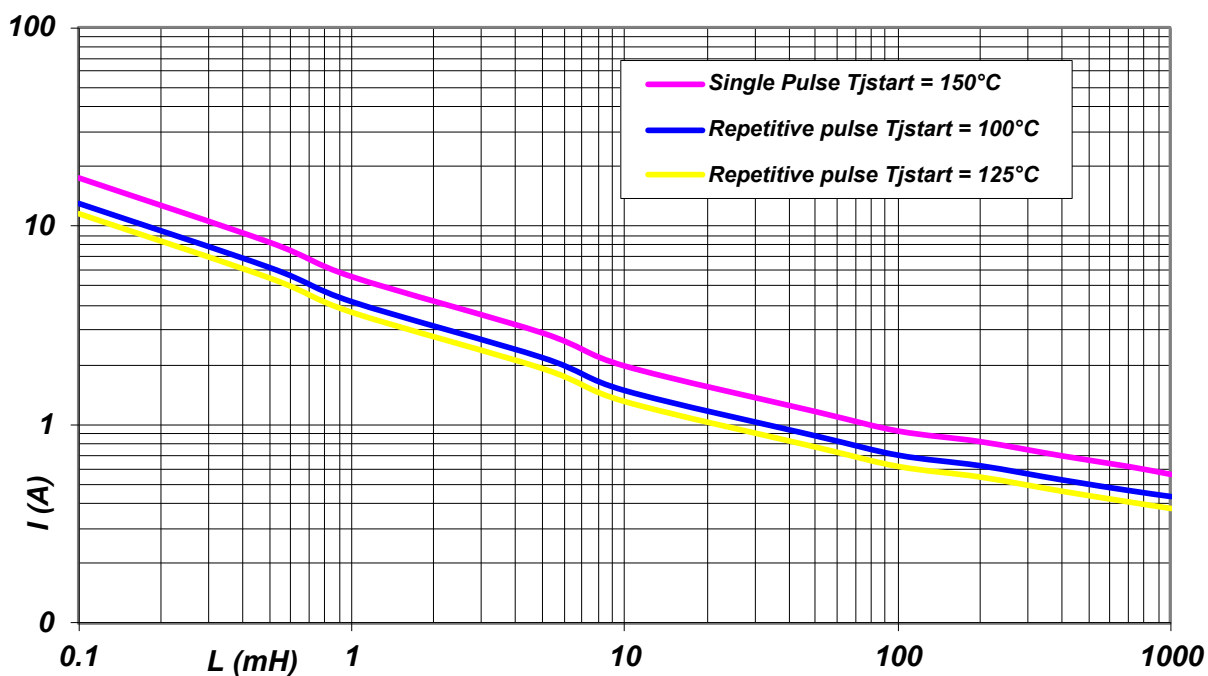
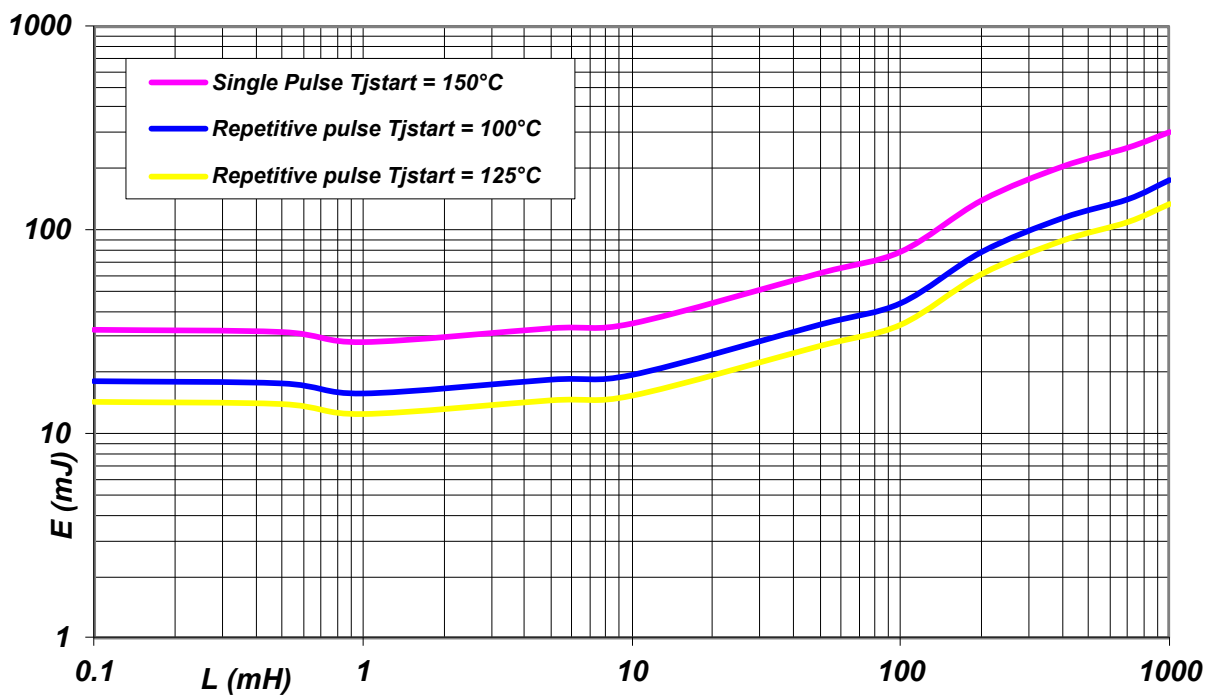


Figure 20. Maximum turn off energy versus inductance



7 PowerSSO-16 thermal data

Figure 21. PowerSSO-16 on two-layer PCB (2s0p to JEDEC JESD 51-5)

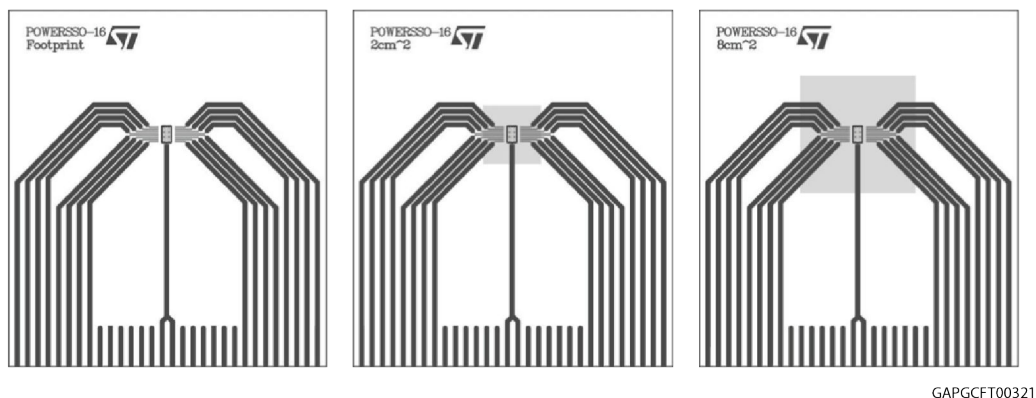


Figure 22. PowerSSO-16 on four-layer PCB (2s2p to JEDEC JESD 51-7)

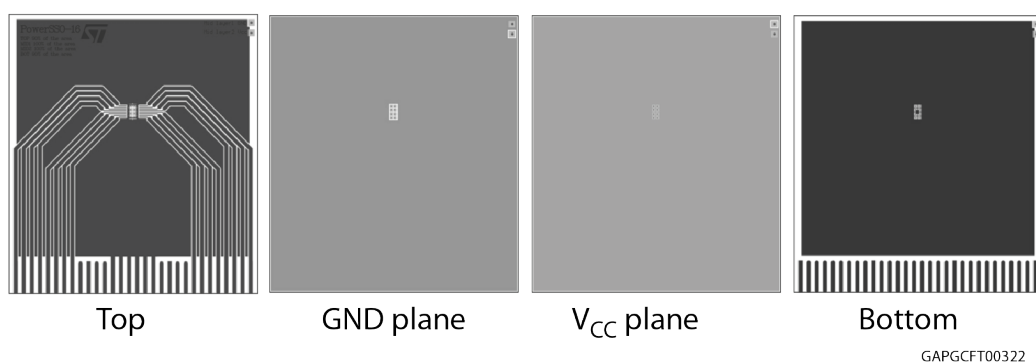


Table 15. PCB properties

Dimension	Value
Board finish thickness	1.6 mm +/- 10%
Board dimension	77 mm x 86 mm
Board Material	FR4
Copper thickness (top and bottom layers)	0.070 mm
Copper thickness (inner layers)	0.035 mm
Thermal vias separation	1.2 mm
Thermal via diameter	0.3 mm +/- 0.08 mm
Copper thickness on vias	0.025 mm
Footprint dimension (top layer)	2.2 mm x 3.9 mm
Heatsink copper area dimension (bottom layer)	Footprint, 2 cm ² or 8 cm ²

Figure 23. $R_{thj-amb}$ vs PCB copper area in open box free air condition (one channel on)

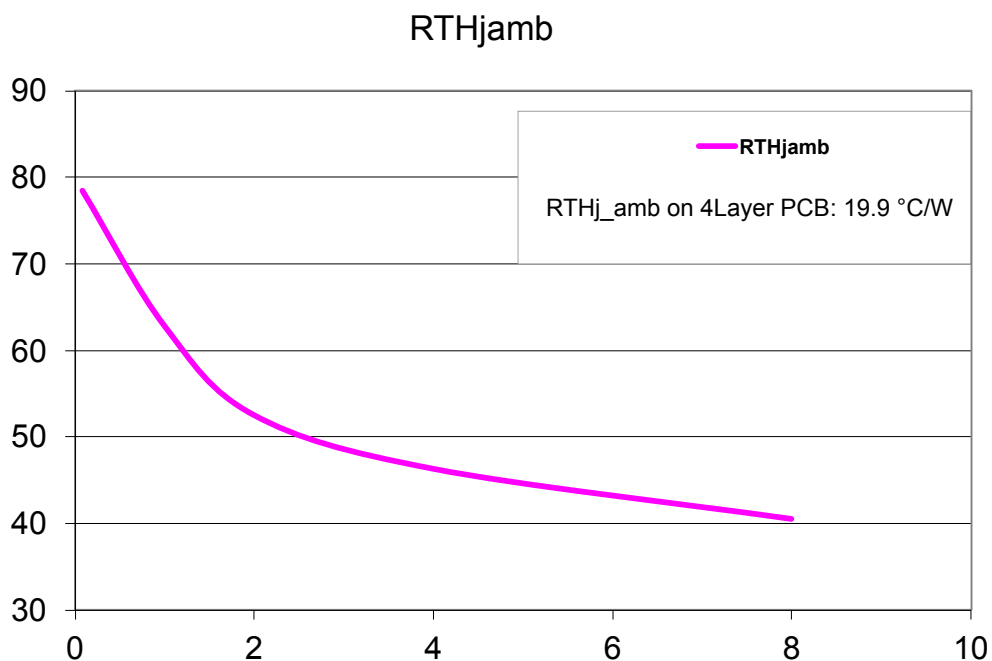
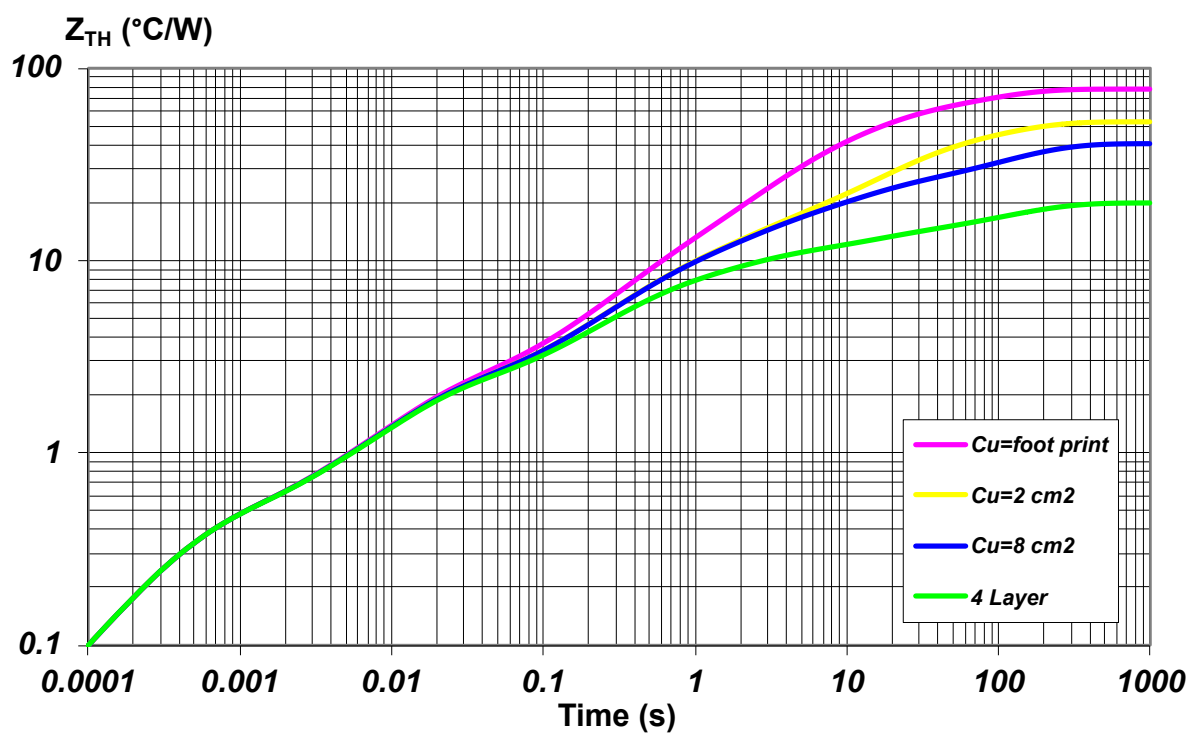


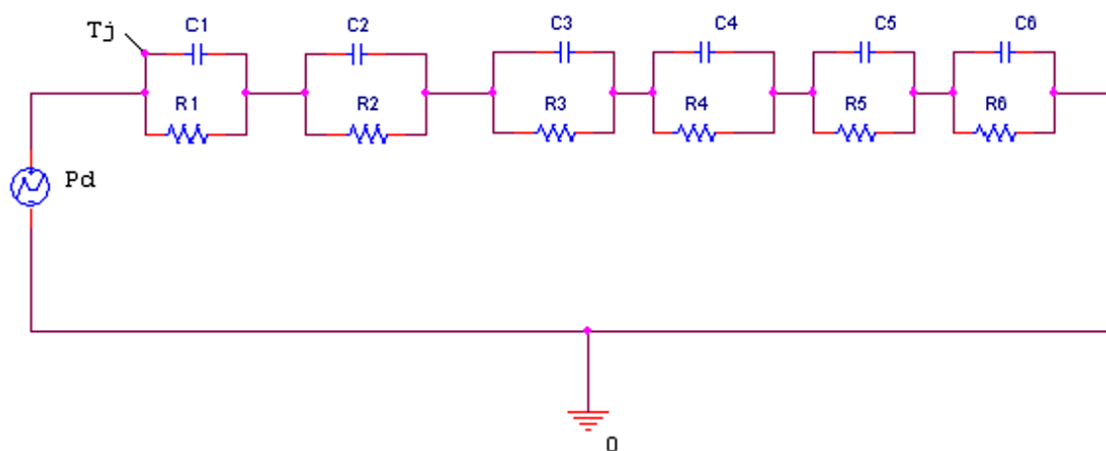
Figure 24. PowerSSO-16 thermal impedance junction ambient single pulse (one channel on)



Equation: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THip} (1 - \delta)$$

where $\delta = t_p/T$

Figure 25. Thermal fitting model of a double-channel HSD in PowerSSO-16


Note: the fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Table 16. Thermal parameters

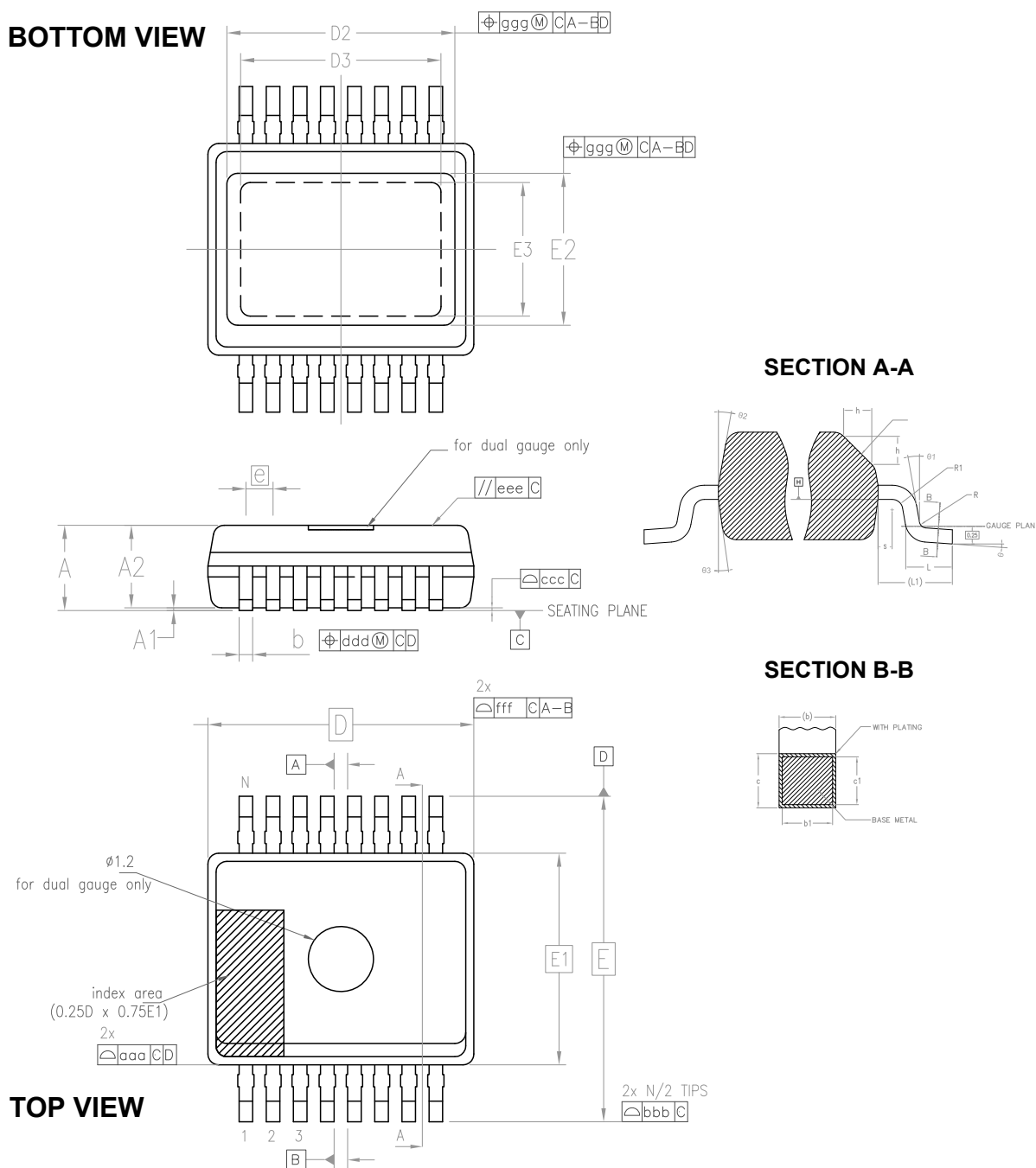
Area/island (cm ²)	FP	2	8	4L
R1 (°C/W)	0.37			
R2 (°C/W)	1.5			
R3 (°C/W)	4.6	4.6	4.6	4
R4 (°C/W)	16	6	6	4
R5 (°C/W)	30	20	10	3
R6 (°C/W)	26	20	18	7
C1 (W·s/°C)	0.001			
C2 (W·s/°C)	0.008			
C3 (W·s/°C)	0.08			
C4 (W·s/°C)	0.2	0.3	0.3	0.4
C5 (W·s/°C)	0.4	1	1	4
C6 (W·s/°C)	3	5	7	18

8 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 PowerSSO-16 package information

Figure 26. PowerSSO-16 package outline



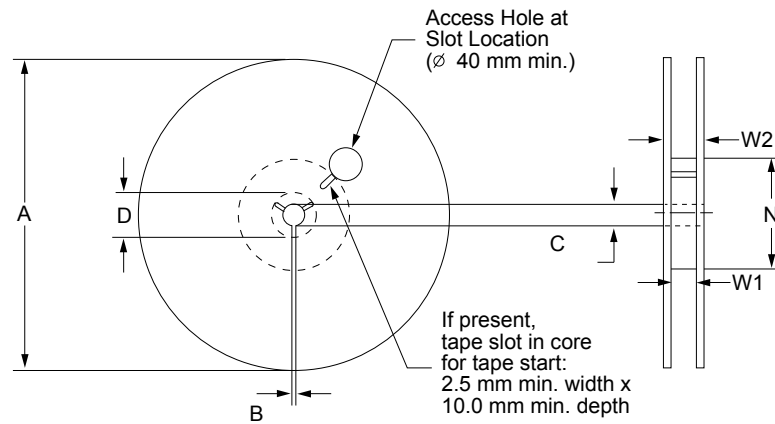
8017965_10_D

Table 17. PowerSSO-16 package mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
Θ	0°		8°
$\Theta 1$	0°		
$\Theta 2$	5°		15°
$\Theta 3$	5°		15°
A			1.70
A1	0.00		0.10
A2	1.10		1.60
b	0.20		0.30
b1	0.20	0.25	0.28
c	0.19		0.25
c1	0.19	0.20	0.23
D	4.9 BSC		
D2	3.60		4.20
D3	2.90		
e	0.50 BSC		
E	6.00 BSC		
E1	3.90 BSC		
E2	2.50		3.10
E3	1.80		
h	0.25		0.50
L	0.40	0.60	0.85
L1	1.00 REF		
N	16		
R	0.07		
R1	0.07		
S	0.20		
Tolerance of form and position			
aaa	0.10		
bbb	0.10		
ccc	0.08		
ddd	0.08		
eee	0.10		
fff	0.10		
ggg	0.15		

8.2 PowerSSO-16 packing information

Figure 27. PowerSSO-16 reel 13"



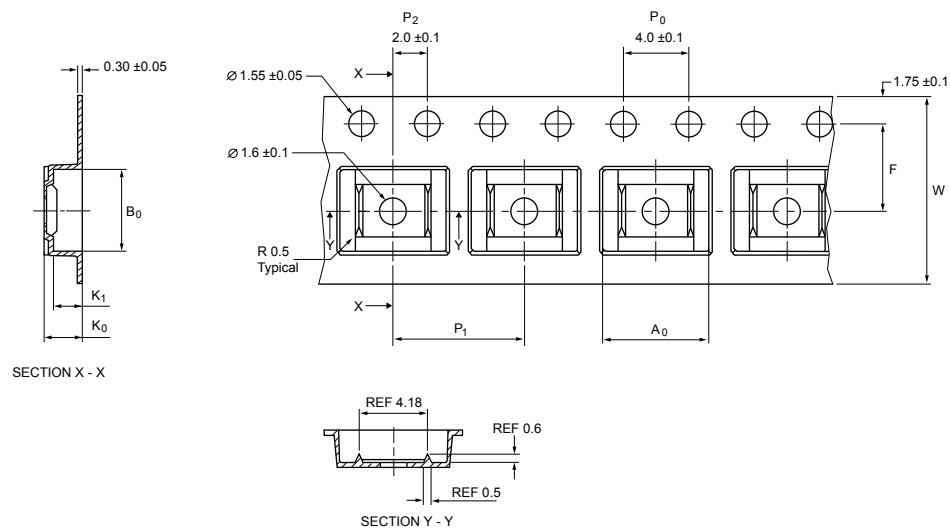
TAPG2004151655CFT

Table 18. Reel dimensions

Description	Value ⁽¹⁾
Base quantity	2500
Bulk quantity	2500
A (max)	330
B (min)	1.5
C (+0.5, -0.2)	13
D (min)	20.2
N	100
W1 (+2 /-0)	12.4
W2 (max)	18.4

1. All dimensions are in mm.

Figure 28. PowerSSO-16 carrier tape

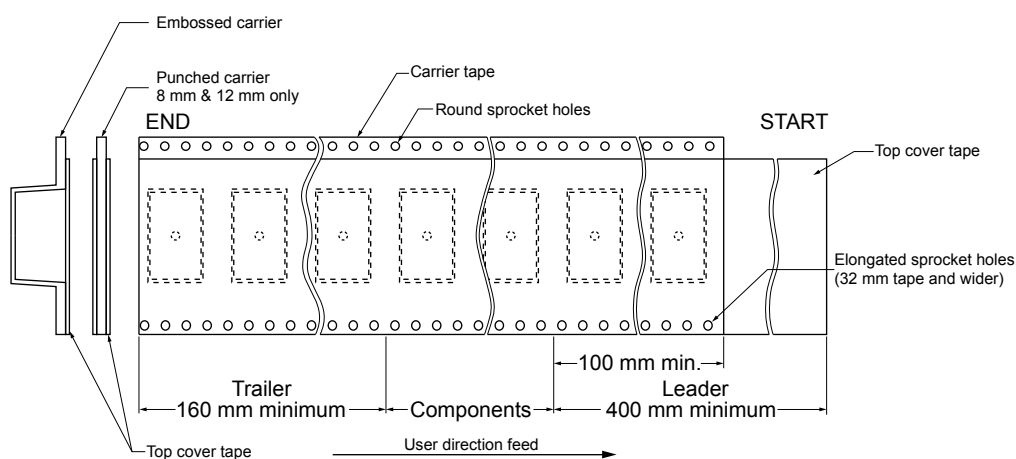


GAPG2204151242CFT

Table 19. PowerSSO-16 carrier tape dimensions

Description	Value ⁽¹⁾
A_0	6.50 ± 0.1
B_0	5.25 ± 0.1
K_0	2.10 ± 0.1
K_1	1.80 ± 0.1
F	5.50 ± 0.1
P_1	8.00 ± 0.1
W	12.00 ± 0.3

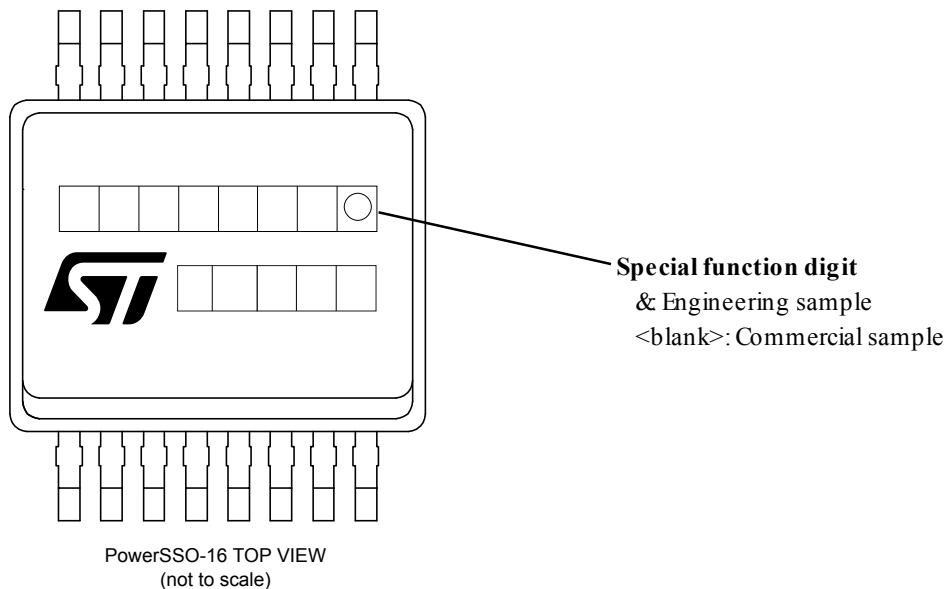
1. All dimensions are in mm.

Figure 29. PowerSSO-16 schematic drawing of leader and trailer tape


GAPG2004151511CFT

8.3 PowerSSO-16 marking information

Figure 30. PowerSSO-16 marking information



GADG0310161234SMD

Parts marked as '&' are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

Revision history

Table 20. Document revision history

Date	Version	Changes
19-Jun-2024	1	First release.
20-Sep-2024	2	Updated Table 3. Absolute maximum ratings, Table 5. Power section, Table 6. Switching, Table 8. Protections and Table 10. Current Sense. Minor text changes.
13-Jan-2025	3	Updated Table 6. Switching, Table 9, and Table 10. Current Sense.
28-Oct-2025	4	Updateds in Table 5. Power section, Table 10. Current Sense, Section 4: Capacitive charging mode (CCM) and Figure 15. Current Sense and diagnostic – block diagram
11-Nov-2025	5	Minor changes in Table 6. Switching and Table 9. CCM - Capacitive loads charging mode

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