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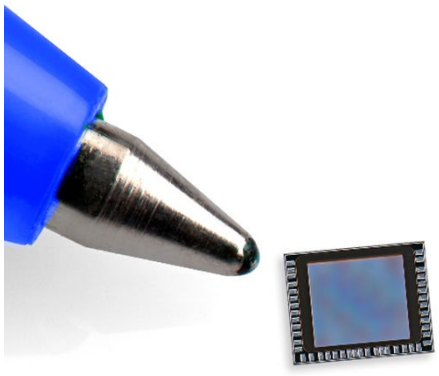
VD55G1

Datasheet

Tiny, clever, low power, 0.56-megapixel, monochrome global shutter image sensor



ST Bright Sense

Order code	Description
VD55G1CCB0/RW	Monochrome, die as reconstructed wafer

Features

- Tiny sensor, which can fit everywhere:
  - World's first 2.16 µm global shutter pixel for optimum compactness
  - Footprint of only 2.73 x 2.16 mm²
  - Small optical format of 1/9 inch (800 x 700) and 1/10 inch (600 x 600)
- Ultralow power solution with:
  - Smart auto wake-up feature, with ultralow power sleepy mode, and smart wake up when an event is detected
  - Low power operation of ≤ 2 mW in auto wake-up mode
  - Power consumption scaling with features, frame rate, and software standby
- Optimized image quality straight out of the sensor with:
  - Cutting-edge performance of ST proprietary pixels combining global shutter, BSI, CDTI, and 3D stacking
  - High sensitivity and sharpness in both visible and NIR
  - Various on-chip features to optimize image quality, such as autoexposure, noise reduction, or defect correction
- Seamless integration into embedded systems:
  - 1-lane MIPI CSI-2 output
  - I²C and I3C control interface
  - Effortless integration with VD55G1 development kit, camera modules, with drivers available from st.com

Application

- AR/VR and gaming
- PC and personal electronics
- Robotics and drones
- Biometrics
- Barcode reading and logistics
- Security
- Machine vision

Description

The VD55G1 is a unique ultracompact and low-power image sensor in the ST BrightSense portfolio. It has been developed to enable the next generation of smart and power-efficient systems. Leveraging the world's first 2.16 µm global shutter pixel, the sensor highlights maximum compactness. It has a tiny 2.73 x 2.16 mm² footprint that fits into the most size-constrained devices such as AR/VR glasses or personal electronics.

With its well-thought-out design, the VD55G1 maintains low power consumption even when pushed at the highest frame rates, making it ideal for battery-powered devices. In addition to this low operating power, the sensor embeds an auto wake-up feature. This enables the sensor to operate in an ultralow power sleepy mode when no change or event is detected. As soon as an event is detected, the sensor automatically sends a trigger to its host processor to switch into full streaming mode to capture the corresponding event. Thanks to this clever feature, vision system makers can finally get rid of the power-hungry, ineffective 24/7 operation of systems such as security cameras, auto-ID, or in-line product inspection.

Besides auto wake-up, the VD55G1 embeds a complete toolbox of on-chip features for optimizing image quality, adjusting frame rate, or improving data efficiency. Autoexposure, noise reduction, and various image corrections help to get stunning images directly from the sensor. This sensor can perform background removal for more efficient face ID, or capture event frames in an event-like mode, enabling the output of event information in a synchronous manner.

Combining a small form factor, power efficiency, and a full range of clever features, the VD55G1 is the ideal vision extension for the next generation of smart embedded systems. Its single-lane MIPI CSI-2 output and I²C or I3C control interface makes it natively compatible with the broadest range of processing units. To facilitate further integration, the sensor is provided along with development kits, camera modules, and drivers. All can be found on st.com.

Figure 1. VD55G1 key features

1 Acronyms and abbreviations

Table 1. Acronyms and abbreviations

Acronym/abbreviation	Definition
ADC	analog to digital converter
AWU	auto wake-up
BSI	backside illumination
CCI	camera control interface
CDM	charge device model
CDTI	capacitive deep trench isolation
CRA	chief ray angle
CSI	camera serial interface
DL	data lane
FoV	field of view
fps	frames per second
GPIO	general-purpose input/output
HBM	human body model
I²C/I3C	inter-integrated circuit (bus)
ISP	image signal processor
LUT	look-up-table
MCU	microcontroller unit
MIPI	mobile industry processor interface
MTF	modulation transfer function
NIR	near infra-red
OIF	output interface
OTP	one-time programmable
POW	power on reset
PWL	piece-wise linear
PWM	pulse-width modulation
QE	quantum efficiency
ROM	read-only memory
STBY	standby
SW	software

2 Product overview

2.1 Function description summary

The VD55G1 is a compact global shutter image sensor featuring a matrix of 804 x 704 pixels. With its global shutter operation, all pixels are synchronized to capture light at the same time. This feature gets rid of the motion blur that can affect rolling shutter image sensors when capturing changing or moving scenes.

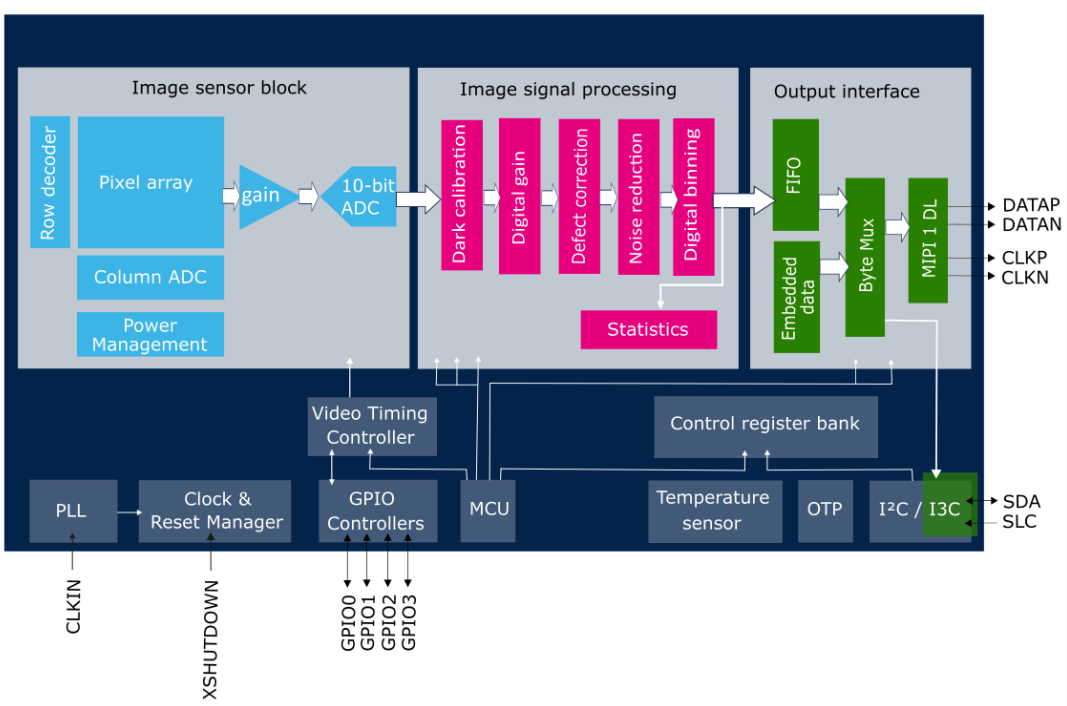
Once the exposure is finished, each pixel information is transferred in a storage node, before being read and digitized one pixel row after the other. The image data are digitized using internal 10-bit ADCs. Additional gains can be applied before ADC stage (for example, analog gain) or after ADC stage (for example, digital gain). Following the digital conversion, various image preprocessing and correction algorithms can be applied into the sensor before data output, such as autoexposure or binning.

The image data are output as frames of RAW8 or RAW10 data through a MIPI CSI-2 interface. The sensor operates on the single MIPI CSI-2 lane.

The VD55G1 is synchronized to the rest of the system by means of an external clock, triggers, and general-purpose input/output (GPIO) signals, which enable synchronization of several sensor exposure starts or to control strobe light sources during exposure time.

The device is fully configurable through the I²C or I3C serial interfaces and provides flexible frame-to-frame parameter configuration changes via the use of programmable contexts. It also embeds a one-time programmable (OTP) nonvolatile memory. It should be written with 32-bit words for traceability and customer data. The dedicated space reserved for the user is at least 1 Kbit.

Figure 2. Functional block diagram



2.2 Technical specifications summary

Table 2. Technical specifications

Category	Parameter	VD55G1 specifications
Resolution	Resolution	0.56 MP
	Pixel array [H x V]	804 x 704
	Aspect ratio	Close to 1: 1
Pixel	Shutter type	Global shutter
	Illumination type	BSI
	Pixel size	2.16 µm
Color	Color option	Monochrome
Frame rates (maximum)	Full resolution VGA resolution QVGA resolution	194 fps 271 fps 480 fps
Optical characteristics	Pixel array size [H x V]	1.74 mm x 1.52 mm
	Optical format	1/9 inch (2.3 mm)
	CRA	30° linear
Mechanical characteristics	Die footprint [H x V]	2.73 mm x 2.16 mm
	Die pinout	43 pins
	Operating temperature range	-30 to 85°C
Electronic characteristics	Sensor data interface	MIPI CSI-2, 1 lane | I3C
	Sensor control interface	I²C, up to 1MHz | I3C, up to 12.5 MHz
	Output format	RAW8, RAW10
	Supply voltages	2.8 V–1.8 V or 1.2 V–1.10 V
	External clock frequency	6-27 MHz
	Power consumption	35 mW (60 fps typical) 1-2 mW (auto wake-up) 0.5 mW (standby)
Embedded features	Image quality optimization	• Autoexposure • Automatic dark calibration • Noise reduction • Gamma correction • Defective pixel correction • Analog and digital gains
	Power and data optimization	• Auto wake-up • Background removal • Event-like mode • Cropping • Binning • Subsampling • Context management with up to 4 contexts
	Other	• Mirror/Flip • Test pattern generation • Temperature sensor • GPIOs x4

3 Functional description

3.1 Interfaces

3.1.1 Inter-integrated circuit (I²C)

The VD55G1 is configured and controlled via an I²C interface. It operates in either fast mode (up to 400 kHz) or fast+ mode (up to 1 MHz) at 1.8 V or 1.2 V. After the CPU boot sequence, the default I²C configuration is fast mode plus with a sink capability set to 20 mA. Drive capability can be decreased to 4 mA (fast mode) by writing a dedicated register once the system has booted.

Device addressing uses a CCI protocol as per the I²C-bus specification and user manual (UM3224).

3.1.2 MIPI I3C^{SM} client interface

In addition to the CSI interface, the VD55G1 I3C can be used to output the image. The I3C allows the use of a host in cases where CSI is not supported, or when the CSI interface is already used by another device.

Note: It is not possible to use CSI and I3C simultaneously to stream images.

Depending on the I3C host, the theoretical maximum frame rates are the following:

Table 3. Theoretical maximum frame rates

Frame rate	Resolution
>5 fps	400 x 700
17 fps	200 x 400
41 fps	100 x 200

In the case of the I3C image output, the host must be in real time to ensure that the data are read at a consistent data rate.

The device interface includes a MIPI I3C^{SM} SDR. Refer to the MIPI - I3C specification v1.0.

3.1.3 Camera serial interface (CSI)

Refer to:

- MIPI CSI-2 version 1.3 with I3C CCI (as defined in CSI-2 v4.0.1).
- MIPI D-PHY specification v 1.1.

3.2 Power supplies

The power supplies required by the sensor are:

- 2.8 V for the analog blocks
- 1.8 V or 1.2 V for the digital I/Os
- 1.10 V for the core digital logic and MIPI CSI-2 output drivers

The pixel array requires different positive and negative voltages, all internally generated by charge pumps and regulators. Two voltage references, internally generated, need external decoupling capacitors.

The internal MCU handles the entire power management of the sensor to guarantee the lowest power consumption at any given time.

3.3 Clock

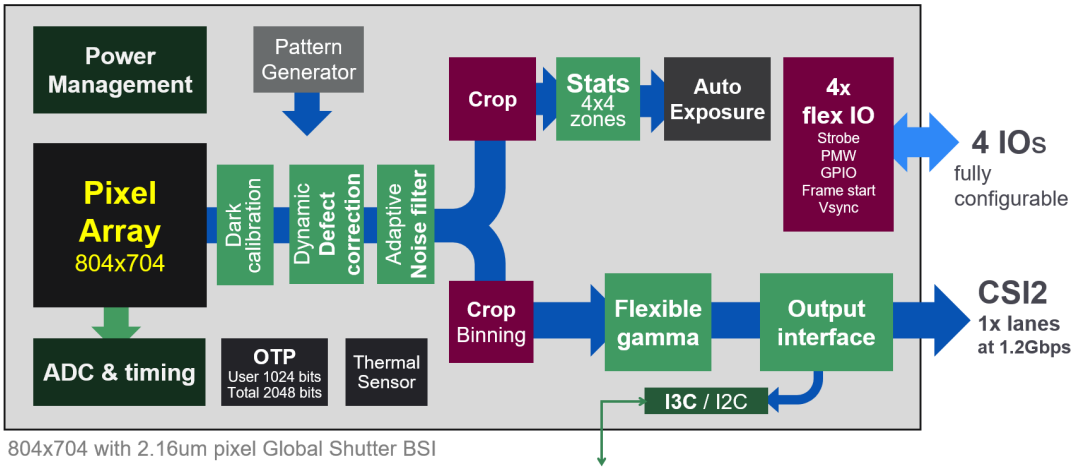
An input clock is required from an external digital clock source in the range of 6 MHz to 27 MHz.

3.4 Video pipe

The video pipe performs several features designed to ensure an image of high quality. These features include:

- Analog subsampling
- Pattern generation
- Dynamic defective pixel correction
- Dark calibration
- Autoexposure
- Digital binning
- Embedded status lines
- Output interface
- Context management
- Cropping
- Flexible PWL gamma

Figure 3. VD55G1 image signal processor schematic



3.4.1 Analog subsampling

The device supports x2, x4, and x8 subsampling, which reduces overall image size and keeps the same FoV. Subsampling is applied vertically and horizontally during the ADC readout. Every two, every four, or every eight pixels are read. When subsampling is used, the frame rate can be increased by decreasing the frame length.

Binning and subsampling are mutually exclusive.

3.4.2 Pattern generation

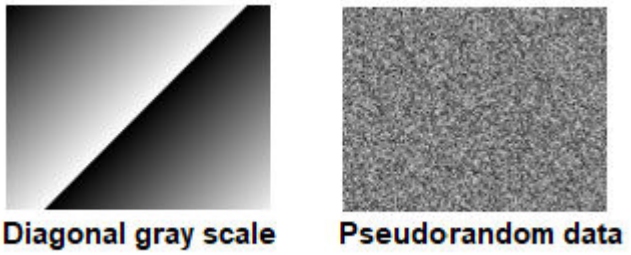
The pattern generation allows the insertion of digital patterns in the output frame for test and debug. Either:

- Whole or part of the active data is replaced with a pattern
- Dark lines are kept untouched

The available patterns are:

- Diagonal gray scale
- Pseudorandom data

Figure 4. Available patterns



3.4.3 Defective pixel correction

Active pixels are corrected automatically by a dynamic algorithm embedded in the sensor ISP. This enables defect-free images straight out of the sensor without further algorithm development or processing resources. The advanced correction algorithm can correct singlet and couplet of defects and take into account local spatial gradients.

The correction strength evolves automatically with exposure time.

3.4.4 Dark calibration

The pixel matrix has dedicated lines with shielded pixels that dynamically retrieve the dark level and subtract it from the active image. Temperature, exposure time, or gain changes are compensated. Temporal smoothing and fractional bit dithering are applied to avoid a sudden one-code step. This block also embeds a programmable digital gain control feature with a granularity of 1/256 followed by a configurable pedestal to offset the dark level along the ISP pipe.

3.4.5 Autoexposure

The sensor integrates an autoexposure module to compute statistics on a given part of the active image. This module allows the exposure parameter to be changed accordingly.

The sensor can enable two concurrent autoexposure processing algorithms. They can be split over the four contexts. It continues computing statistics over frames whether the autoexposure feature is enabled or not.

Stable behavior of the autoexposure module requires that AE ROI, exposure conditions, and active scene illumination in contexts are homogeneous.

3.4.6 Digital binning

The digital binning process reduces the image resolution by a factor of 2 or 4 in each direction. Central and neighboring pixels are weighted to produce the digital binned image, avoiding special phase shifts and artifacts that may occur on the output image. Digital binning and subsampling are mutually exclusive.

3.4.7 Embedded status lines

The MCU has access to a bank of status registers. They are refreshed at each frame. They provide detailed information on the current state of the sensor. For example:

- Clock settings
- Cropping and orientation parameters
- Analog and digital gains
- Integration time
- Frame counter index
- Thermal sensor value

The embedded status lines content is a copy of this information. The OIF generates an embedded status line, which allows metadata to be sent through the MIPI image data interface. There are 512 bytes transmitted at the beginning of each frame. The length of the embedded status line can be stretched to equal the active line packet size. Transmission of the embedded data lines can be disabled by configuring a static register during SW_STANDBY state before streaming. The embeded data lines have their own programmable "data types" and "virtual channels".

3.4.8 Output interface (OIF)

The OIF embeds a single data lane MIPI D-PHY interface. It supports up to 1.2 Gb/s of data. RAW10 and RAW8 data formats are supported over the CSI2-OIF.

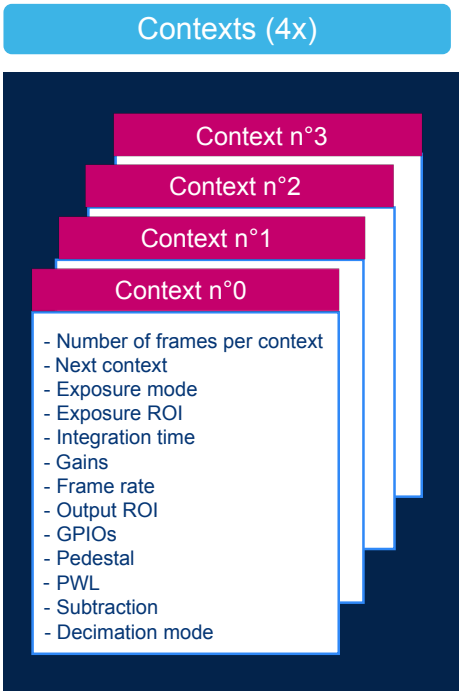
The OIF can output a combination of the following:

- Intelligent status lines
- Frame data

3.4.9 Context management

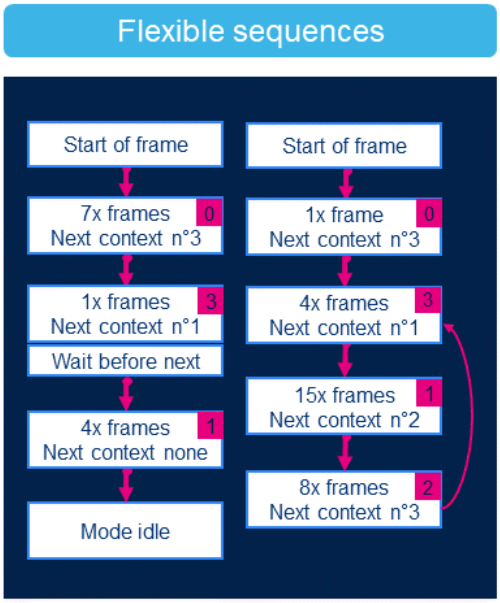
The sensor allows the configuration of up to four different rolling contexts (or frame setups). Parameters that can be specifically defined in a context are listed in the figure below.

Figure 5. Context parameters



Contexts can be chained one to another in an ending or non-ending sequence.

Figure 6. **Example of ending and non-ending multicontext sequence**



3.4.10 Cropping

The host can accurately choose which area of the whole pixel array it receives. This reduces traffic on the CSI interface and saves processing time.

3.5 Synchronization modes

The sensor has multiple synchronization modes:

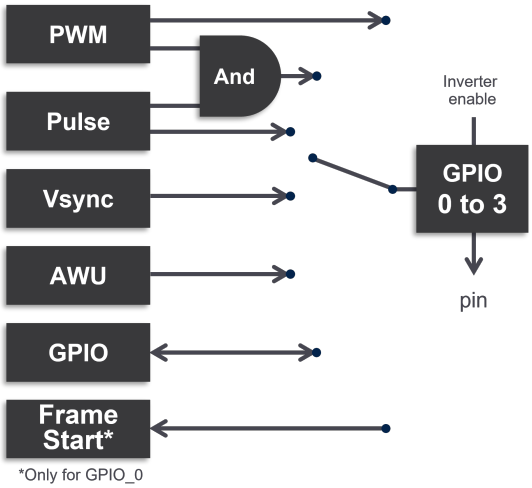
1. Leader mode
   - Image streaming starts right after the execution of a streaming initialization command sent over the I²C bus.
2. Follower mode
   - Using GPIO pulses
   - Using I²C and I3C triggering commands

3.6 General purpose input/outputs (GPIOs)

The sensor provides four GPIOs:

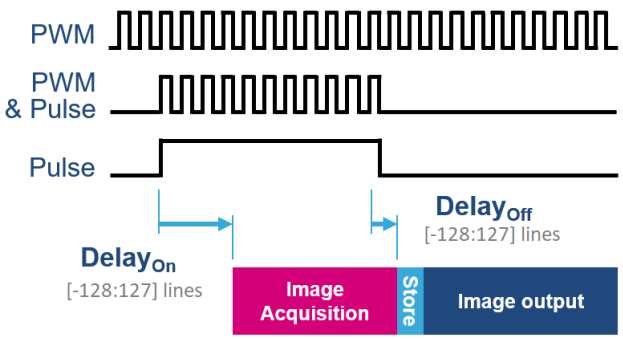
- GPIO0 is used as a frame start synchronization signal or as a generic GPIO if not used for this function
- GPIO[1-3] are used as strobe output, PWM output, VSYNC or as a generic GPIO as per the configuration

Figure 7. GPIO modes



All GPIO settings are fully configurable for the four context setups. Each output signal can be mapped to one or several of the GPIOs. All GPIOs have configurable polarity.

Figure 8. PWM and pulse overview



3.7 Use case examples

Data of Table 4. Example of functional use cases are provided for an integration time of 1 ms.

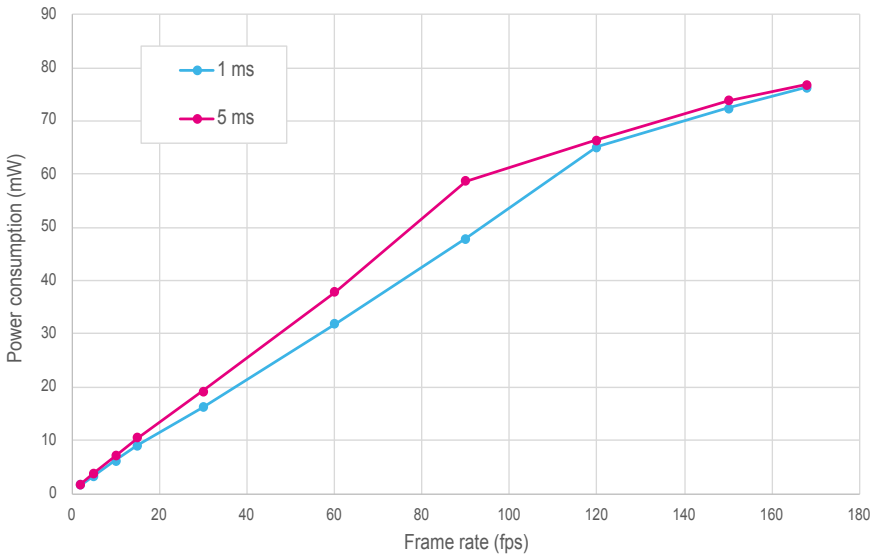
Table 4. Example of functional use cases

Resolution	fps at 9 bits	Typical power consumption at 9 bits	fps at 10 bits	Typical power consumption at 10 bits
800 x 700	194	75.8	168	76.9
600 x 600	224	70.9	194	68.7
640 x 480	271	72.7	235	71.6
320 x 240	480	62.3	408	61.9

3.7.1 Low power consumption

The figure below describes the variation of the power consumption as a function of the frame rate, at full resolution, and at different integration times.

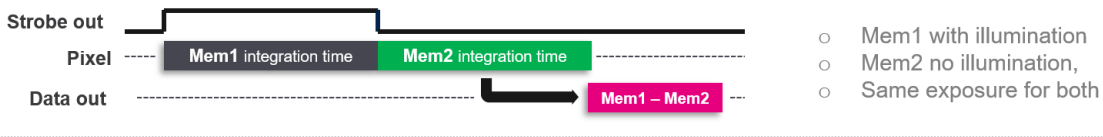
Figure 9. VD55G1 power consumption vs frame rate



3.7.2 Background removal

The VD55G1 includes the ability for in-sensor background removal. Using the pixel combined with the read-out ensures there is no delay between the two exposures.

Figure 10. Background removal



3.7.3 Differential mode

The VD55G1 embeds a disruptive streaming mode, where each pixel value is the difference between two times.

It can be used to measure motion, with a single frame, so with ultra-low latency (single frame) and no impact on power consumption.

This mode is done directly at pixel level with ultrashort timings so cannot be emulated by the host.

There is no host processing needed as the image is natively differential.

Output can be considered as event-like but still compatible with standard processing.

Differential value is signed, where the zero can be positioned anywhere in the range [0:1023], which is useful for motion estimation.

These differential frames can be interlaced with standard images. It is typically useful to combine both object detection (hands, eyes...) and motion estimation.

Figure 11. Differential mode

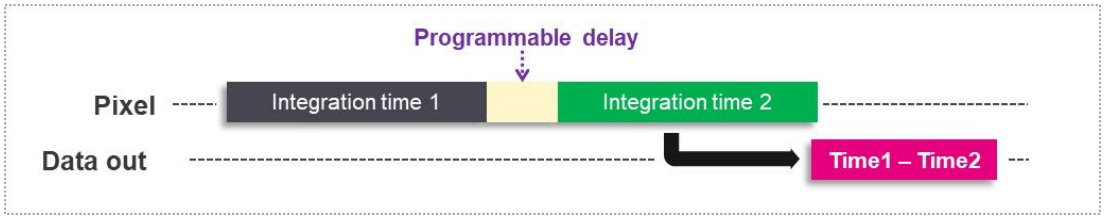
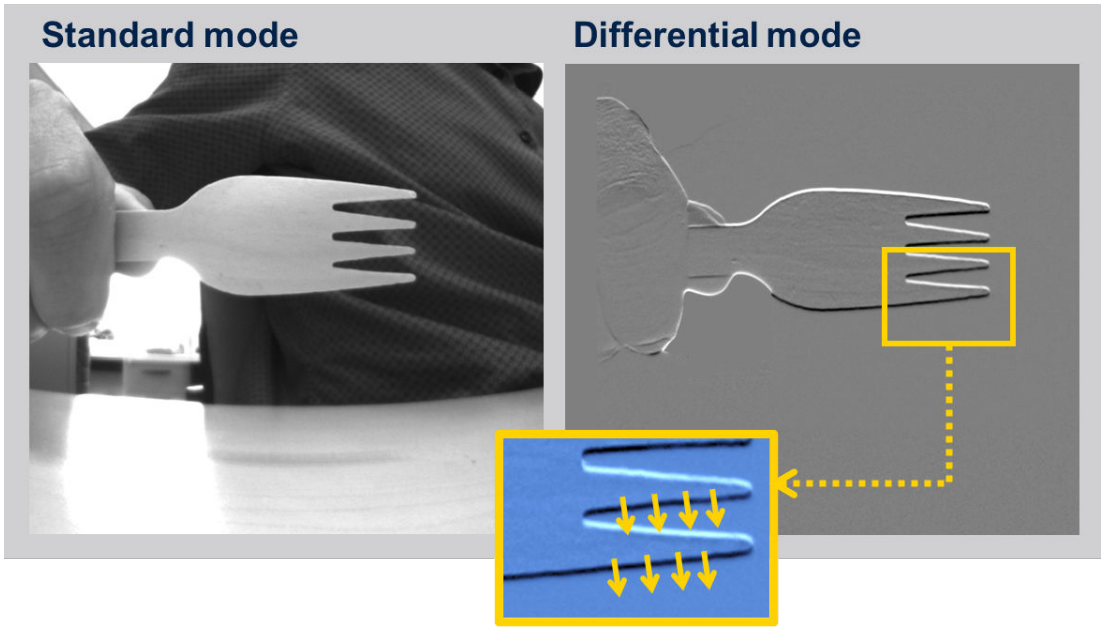


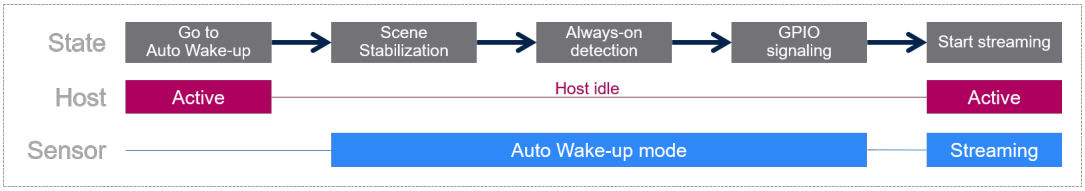
Figure 12. Differential mode illustration



3.7.4 Auto wake-up

The VD55G1 includes an autonomous mode, which ensures power saving. It allows sensing the scene in lower power mode, without image output. When there is a significant change in the image, the sensor triggers a GPIO. Then the host can enable normal streaming and analyze the scene.

Figure 13. Auto wake-up



3.7.5 Spatial HDR

The VD55G1 supports an HDR feature, requiring a single frame, so with no impact on power and latency.

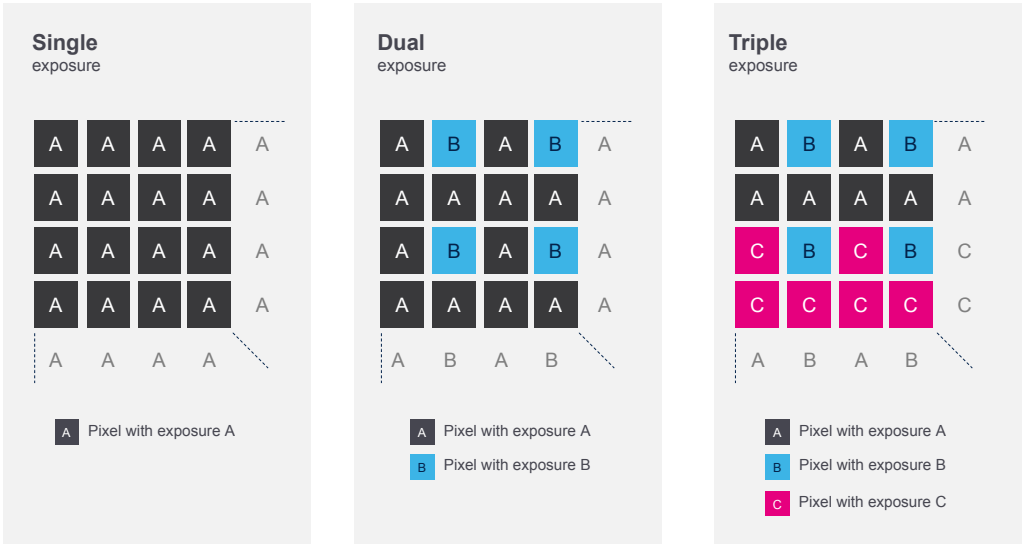
There are three categories of pixels; each group has its own integration time.

The VD55G1 outputs the raw image without recombining the HDR.

There are two options for the host:

- Compute an HDR image by recombining the pixels with different exposure.s
- Directly apply computer vision on the raw image.

Figure 14. Spatial HDR

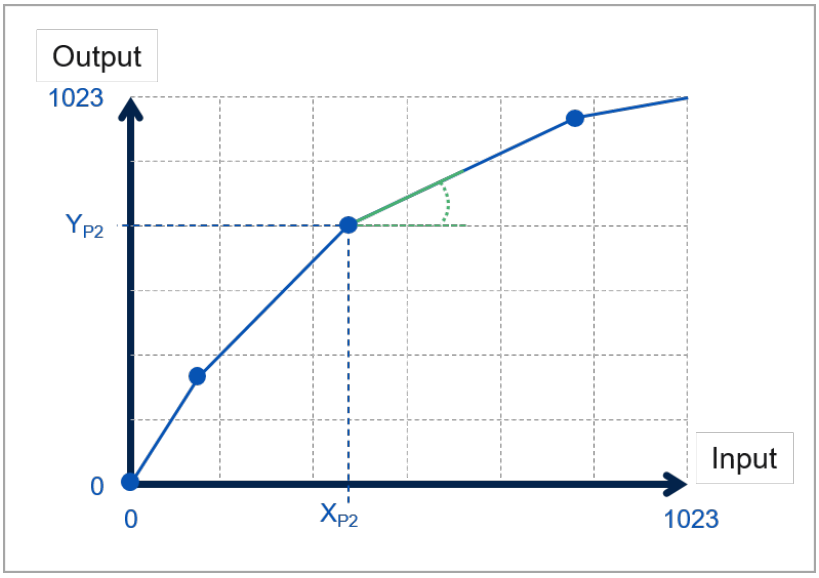


3.7.6 Flexible PWL gamma

The VD55G1 embeds a flexible piece-wise linear (PWL) look-up-table (LUT).

The LUT is defined by four points. Each point is positioned by X and Y values, as well as the slope to the next point.

Figure 15. **VG55G1 LUT**



4 Die specifications

In the table below, the die dimensions are after sawing. The optical center is with the die center as reference.

Table 5. Die size after sawing

Description	Min. (µm)	Typ. (µm)	Max. (µm)
X die (after sawing)	2720	2730	2740
Y die (after sawing)	2153	2163	2173
Die thickness		150 µm	

Table 6. Optical center

Description	X	Y
Optical center	0.0	36.4

Figure 16. Die mechanical dimensions (µm)

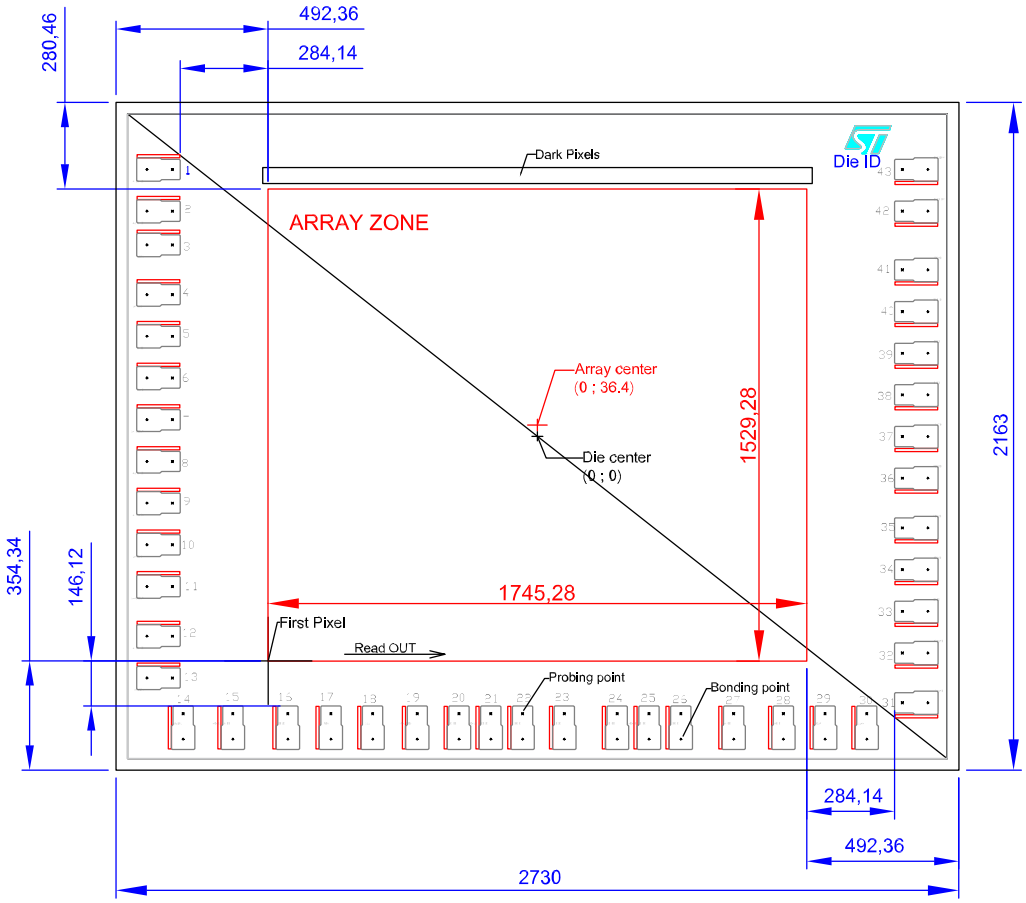


Figure 17. **Pad details**

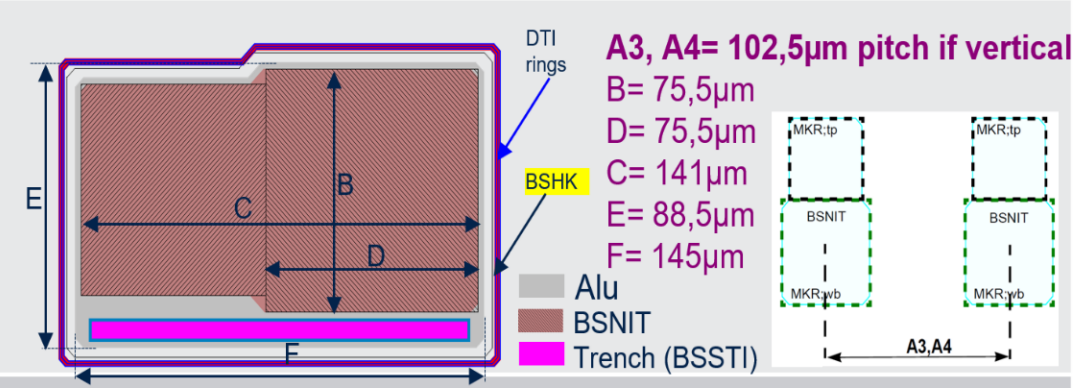
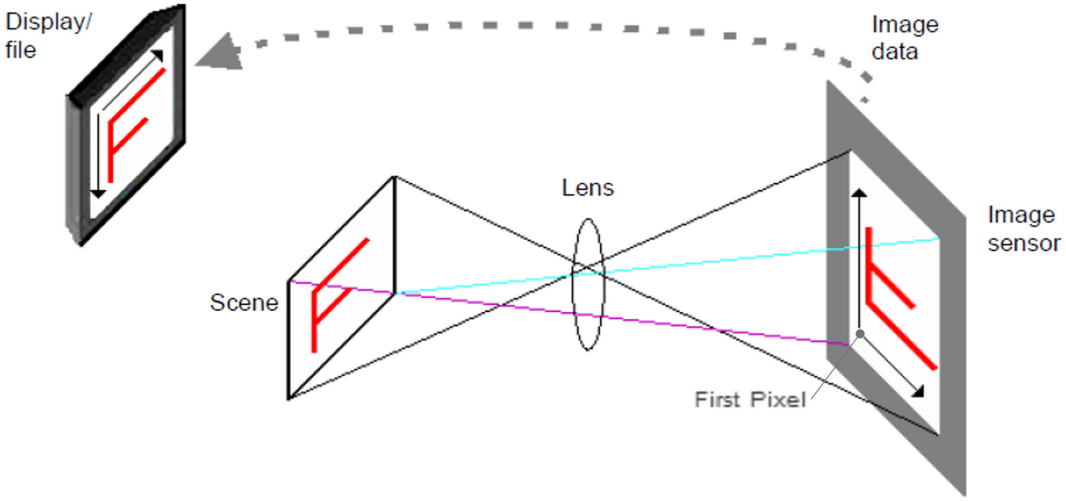


Figure 18. **Display**



5 Pad description

Table 7. Pad description table

Ball name	Type	Description	Reset state	Reference supply
Power supply				
VCORE	PWR	1.10 V power supply for the digital core		1.10 V
VDDIO		1.8 V or 1.2 V power supply for the IOs		1.8 V or 1.2 V
VANA		2.8 V analog power supply		2.8 V
DGND		Digital ground		VDDIO
AGND		Analog ground		VANA
Reference				
VCPNEG_IN	REF	Must be connected to VCPNEG_OUT		VANA
VCPNEG_OUT		Must be connected to VCPNEG_IN		
VCPPOS_IN		Must be connected to VCPPOS_OUT		
VCCPOS_OUT		Must be connected to VCPPOS_IN		
CSI-2 interface				
DATA1P, DATA1N	MIPI DPHY	CSI-2 data lane 1, positive and negative	Low	VCORE
CLKP, CLKN		CSI-2 clock, positive and negative		
Host interface				
XSHUTDOWN	I	Reset active low		VDDIO
SDA	IO	I²C/I3C data		
SCL	I	I²C/I3C clock		
GPIO0	IO	General purpose I/O and strobe light control	Low	
GPIO1				
GPIO2				
GPIO3				
CLKIN	I	Input clock		
Other pins				
NC		Not connected		

Table 8. Pad coordinates

The pad coordinates (0, 0) are the die center

Pad number	Net name	Bonding point X coordinate	Bonding point Y coordinate
1	VANA	-1260.030	863.920
2	AGND	-1260.030	728.840
3	NC	-1260.030	619.730
4	CPNEGIN	-1260.030	458.700
5	VCORE	-1260.030	323.630
6	DGND	-1260.030	188.560
7	CPNEGOUT	-1260.030	53.490
8	AGND	-1260.030	-81.590
9	AGND	-1260.030	-216.660

Pad number	Net name	Bonding point X coordinate	Bonding point Y coordinate
10	CPPOS	-1260.030	-351.730
11	CPPOS	-1260.030	-486.800
12	VANA	-1260.030	-647.830
13	NC	-1260.030	-782.900
14	NC	-1147.420	-976.530
15	NC	-986.390	-976.530
16	VDDIO	-808.350	-976.530
17	SDA	-668.750	-976.530
18	SCL	-533.670	-976.530
19	XSHUTDOWN	-389.150	-976.530
20	VCORE	-254.080	-976.530
21	NC	-151.010	-976.530
22	DGND	-47.950	-976.530
23	DGND	87.130	-976.530
24	VCORE	258.370	-976.530
25	NC	361.430	-976.530
26	DGND	464.500	-976.530
27	VANA	635.740	-976.530
28	AGND	796.760	-976.530
29	CLKN	931.840	-976.530
30	CLKP	1066.900	-976.530
31	DATA1N	1260.030	-863.290
32	DATA1P	1260.030	-702.260
33	VDDIO	1260.030	-567.190
34	GPIO0	1260.030	-432.120
35	GPIO1	1260.030	-297.050
36	GPIO2	1260.030	-136.020
37	CLKIN	1260.030	-0.950
38	DGND	1260.030	134.130
39	VCORE	1260.030	268.570
40	DGND	1260.030	403.640
41	GPIO3	1260.030	538.710
42	AGND	1260.030	728.850
43	VANA	1260.030	863.920

6 Application schematic

6.1 Additional components

Dedicated additional capacitors are required to complete the circuit. These are listed in Table 9. Capacitor needs. Capacitor needs below. The capacitors should be selected to maintain their capacitance value within the indicated tolerance over the full range of maximum voltages, operating temperatures, and aging.

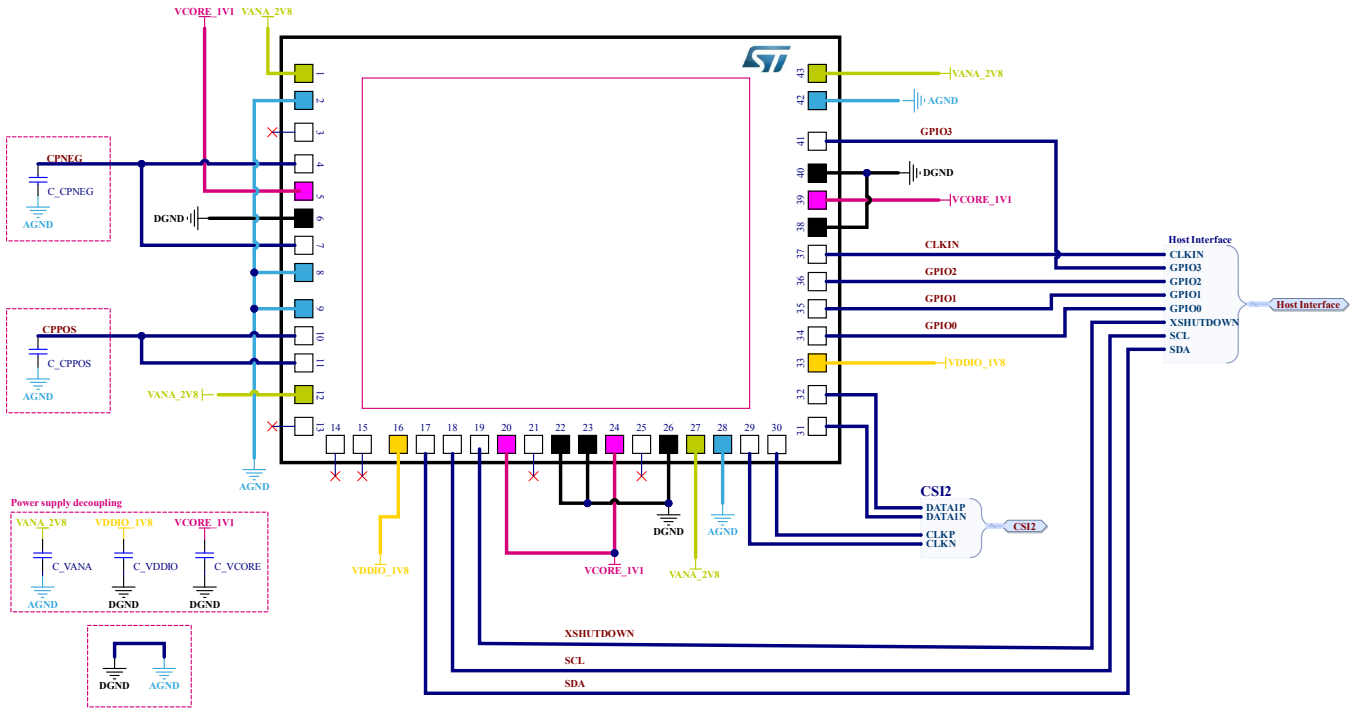
Capacitor values are based on capacitor positions (embedded in the camera module or external to the camera module).

External capacitors are required to properly filter out supply noise. Optimal reference in terms of value and size is subject to application board architecture and topology. The external capacitor values provided in the table below may be increased to compensate real supply noise.

Table 9. Capacitor needs

Associated pad name	Typical voltage	Capacitor position	Minimum capacitance	Typical capacitance	Maximum capacitance	Operating frequencies	Capacitor ground	Purpose
CPPOS_IN, CPPOS_OUT	3.55 V	Embedded	330 nF	470 nF	564 nF	350 to 450 MHz	AGND	CP tank capacitor
CPNEG_IN, CPNEG_OUT	-2.0 V	Embedded	650 nF	0.88 µF	1.04 µF	350 to 450 MHz	AGND	CP tank capacitor
VDDIO	1.8 V or 1.2 V	External	1 µF			1 MHz (I²C) 12.5 MHz (I3C)	DGND	Supply decoupling
VCORE	1.10 V	Embedded	470 nF			800 MHz (RCC) 0.4 GHz as min. value - 1.2 GHz (MIPI DPHY) 150 MHz (ISP)	DGND	Supply decoupling
		External	10 µF			Pulse of current of 2 µs	DGND	Supply decoupling
VANA	2.8 V	Embedded	100 nF			350 to 450 MHz (CPPOS)	AGND	Supply decoupling
		External	10 µF				AGND	Supply decoupling
Capacitor position	Embedded in the camera module or external to the camera module							

Figure 19. **Application schematic**



6.2 Layout guidelines

For good PCB design practice, observe the following image sensor layout:

- Use power and ground planes to supply power to the sensor.
- Join grounds i.e. join AGND and DGND into one single, solid GND plane underneath the sensor.
- Connect this GND plane to the sensor pads with one via per GND pad.
- To minimize risk of emissions, shield all vias and tracks attached to supplies by their respective GND nets.
- Maximize copper fill on the power planes near the sensor and use vias to improve heat transfer from the sensor. Consider including additional heatsinks close to the sensor if it is to be used at high temperatures.
- Route the high-speed signal pairs of the MIPI CSI-2 interface with balanced and controlled impedance differential traces (50 Ω single-ended impedance, 100 Ω differential impedance). This is a requirement for high-speed signaling. Route each pair together and match them in length to target a maximum 10 ps skew.

CPNEG_IN and CPNEG_OUT must be connected together with a short track. The required decoupling capacitor shall be placed on this path and not on an isolated track.

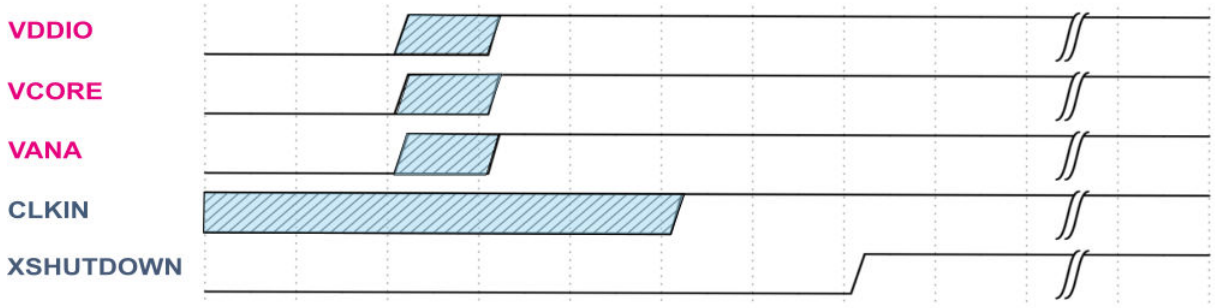
CPPOS_IN and CPPOS_OUT must be connected together with a short track. The required decoupling capacitor shall be placed on this path and not on an isolated track.

6.3 Device power up sequence

The power on sequence must be done as follows:

1. Provide all the external supplies (VDDIO, VCORE, VANA) according to the device characteristics described in Section 8: Electrical characteristics. As long as XSHUTDOWN is low, the device is in HW_STANDBY state.
2. External supplies can be switched on in any order, as well as CLKIN.
3. Set XSHUTDOWN to high.

Figure 20. Power up sequence



The device has power-on-reset (POR) detection cells with hysteresis on VCORE and VDDIO power supplies. POR is released after a typical delay of 20 µs on the rising edge.

Bursts with a duration of less than 2 µs (typical) are ignored.

Table 10. POR threshold

Supply	POR max threshold rising edge (V)	POR min threshold falling edge (V)
VCORE	0.746	0.502
VDDIO	0.686	0.622

6.4 Device power down sequence

The power down sequence must be done as follows:

1. If the sensor is in STREAMING state, then set it to SW_STANDBY state and wait for the command to complete.
2. Set XSHUTDOWN to low.
3. External supplies can be switched off in any order, as well as CLKIN.

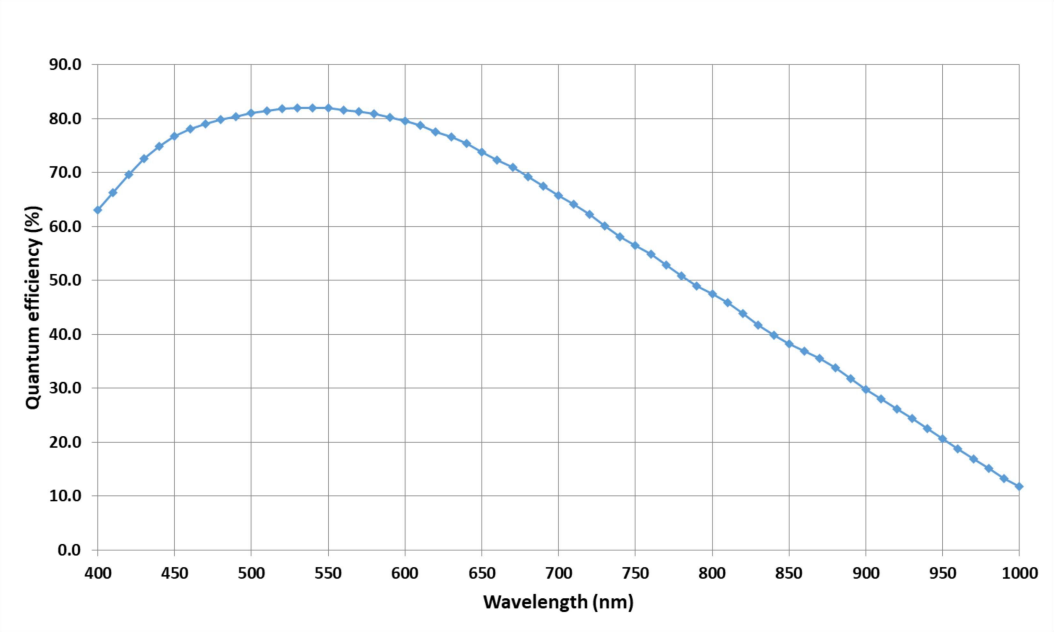
7 Pixel performance

7.1 Quantum efficiency

Quantum efficiency (QE) is the percentage of incident photons converted into electrons, representing the sensitivity of the pixels.

QE graph is measured at Tj=60°C.

Figure 21. Quantum efficiency



7.2 MTF

The modulation transfer function (or MTF) measures the ability of the device to differentiate spatial frequencies. The MTF value represents the contrast restitution for the corresponding spatial frequency, hence describes the contrast attenuation. It is a sharpness indicator that quantifies to what extent the image sensor can capture and discriminate tiny detailed contrast of an object in the field of view.

The figure below presents the on-axis MTF, measured in a 100x100 pixels ROI with the slanted-edge method. Note that the Ny is the spatial Nyquist frequency. This describes the MTF properties of the sensor itself (without a lens).

MTF is measured at ambient temperature.

Figure 22. **On axis vertical and horizontal pixel MTF @ 534 nm**

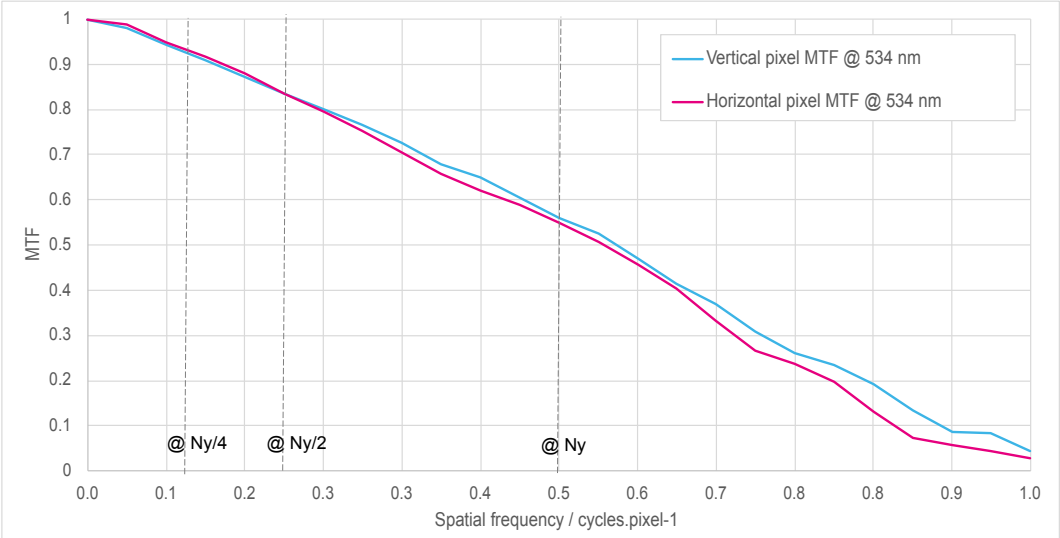
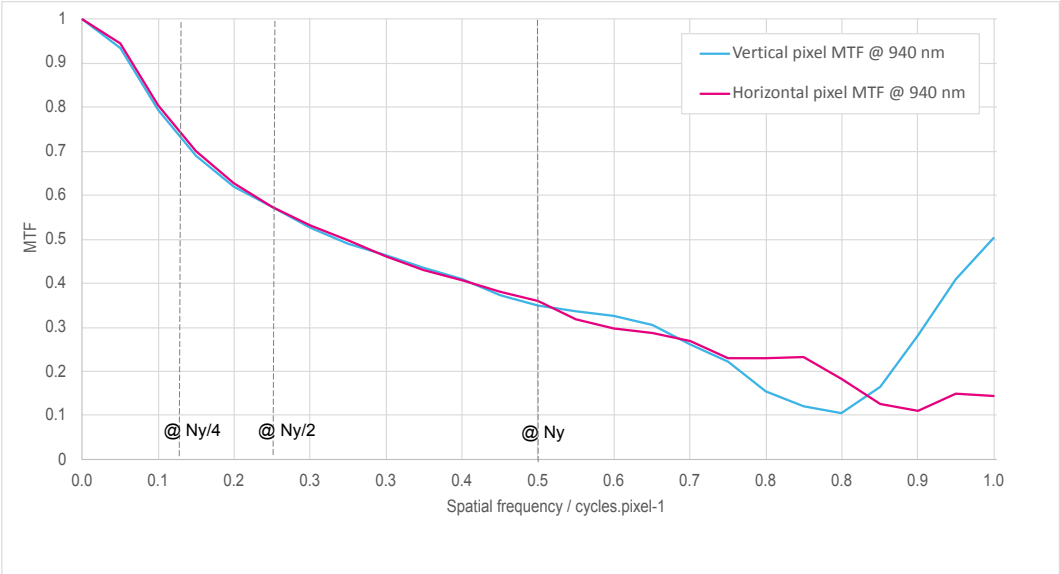


Figure 23. **On axis vertical and horizontal pixel MTF @ 940 nm**



7.3 Microlenses and CRA matching

Each pixel of the matrix has its own micro lens covering it.

The purpose of the microlens is to concentrate and optimize photon capture passing through the module lens down to the photodiode.

The light beam has an incidence angle change when passing through the module lens, increasing from center to periphery. This is the chief ray angle (CRA).

To compensate the change of CRA over the matrix, the microlens position over the pixels progressively shifts from matrix center to matrix borders.

The design of the sensor microlens shift is optimized for matching a lens with CRA of 30° at the corners, and follows a linear shift shape.

It is recommended to match the CRA of the lens with the CRA of the image sensor to maximize image quality. Featuring advanced BSI pixel technology, the VD55G1 provides high relative illumination (RI) uniformity up to the image corners, which enables users to select lenses with different CRA with limited impact.

The following figure presents the CRA tolerance range in lens selection for maintaining RI uniformity over 90% across the image.

Figure 24. Guideline for lens CRA matching at 520 nm

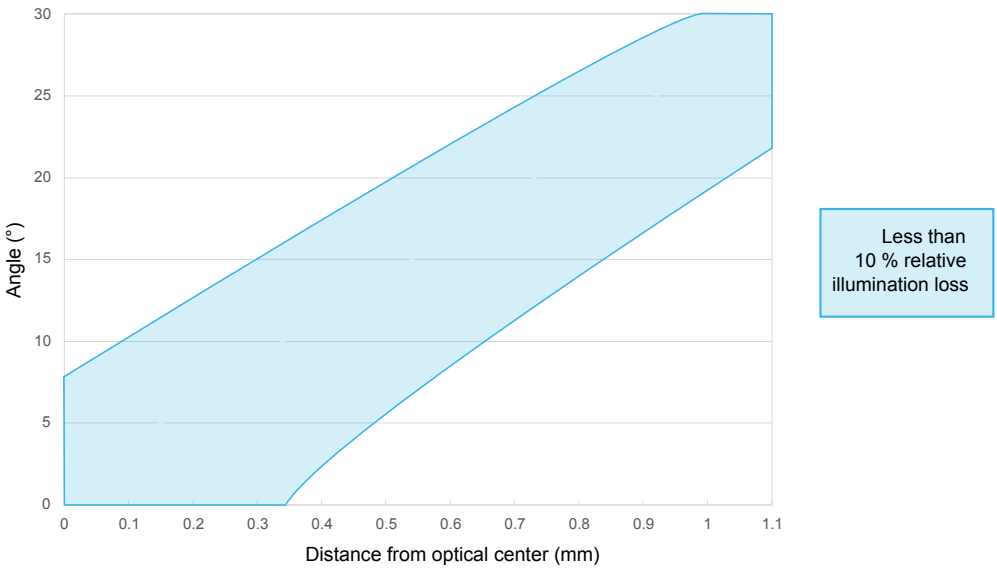


Table 11. CRA examples

Distance from optical center (mm)	Chief ray angle (°)
0.00	0
0.12	3
0.23	6
0.35	9
0.46	12
0.58	15
0.70	18
0.81	21
0.93	24
1.04	27
1.16	30

8 Electrical characteristics

The electrical characteristics have been measured under the following conditions:

- Full resolution (804x704 pixels)
- Nominal power supply levels and nominal voltage
- External clock at 12 MHz
- Full speed (168 fps)
- 1.2 Gbit/second on MIPI
- Junction temperature at 60°C
- Integration time = 376 µs

8.1 Absolute maximum ratings

Caution: Stresses above those listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 12. Absolute maximum ratings

Symbol	Parameter	Maximum	Unit
VDDIO	Digital IO power supply	2.88	V
VANA	Analog power supply	3.99	V
VCORE	Digital core power supply	1.89	V
VESD, electrostatic discharge model	Human body model (HBM)	±2	kV
	Charge device model (CDM)	±500	V

8.2 Operating conditions

Table 13. Operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDIO	Digital IO power supply	1.62	1.8	1.92	V
		1.08	1.2	1.32	
VANA	Analog power supply	2.7	2.8	2.9	V
VCORE	Digital core power supply	1.05	1.10	1.26	V
Temperature					
T JF	Junction temperature (functional operation)	-30	—	85	°C

8.3 Power consumption

Values below are measured for the conditions listed in Section 8: Electrical characteristics, but they also include process variability.

Table 14. Typical and maximum power consumptions for VDDIO = 1.8 V

State	VDDIO		VCORE		VANA		Unit	Total power		Unit
	Typ	Max	Typ	Max	Typ	Max		Typ	Max	
Reset	0.006	0.01	0.5	2	0.002	0.01	mA	0.6	2.2	mW
SW standby	0.006	0.01	0.75	2.1	0.002	0.01		0.8	2.4	
Streaming 168 fps	0.006	0.01	33.2	37.0	13.5	15.0		74.3	82.7	
Streaming 30 fps	0.006	0.01	9.7	11.5	3.6	4.0		20.8	23.9	

The values in Table 15. Maximum supply consumption are measured for the worst conditions of process, voltage, and junction temperature (85°C). They are evaluated on a limited number of devices.

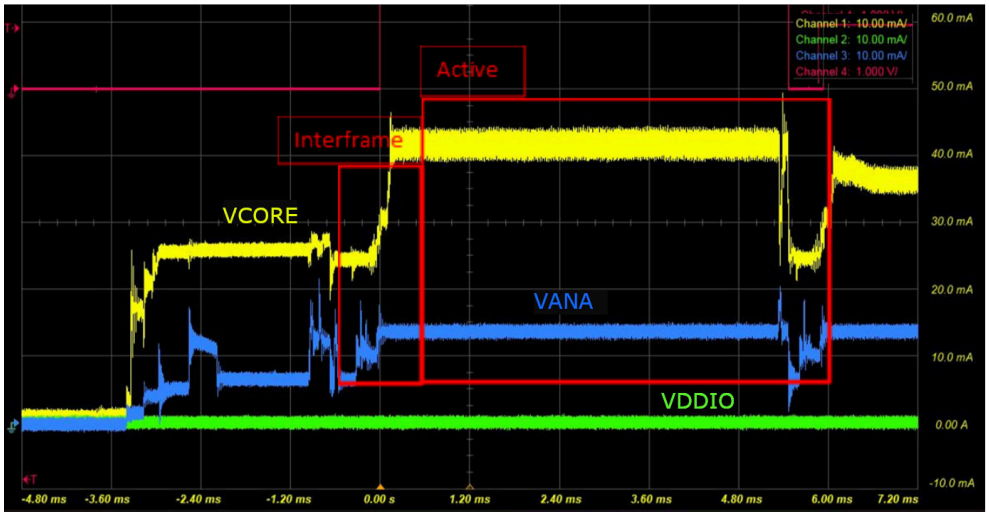
Table 15. Maximum supply consumption

State	VDDIO (mA)	VCORE (mA)	VANA (mA)
SW_STANDBY	0.01	4	0.01
Streaming image 168 fps	0.01	50	15

8.4 Current profile

It is evaluated on one device.

Figure 25. Start streaming and first frame of typical current profile (mA) over time (ms)

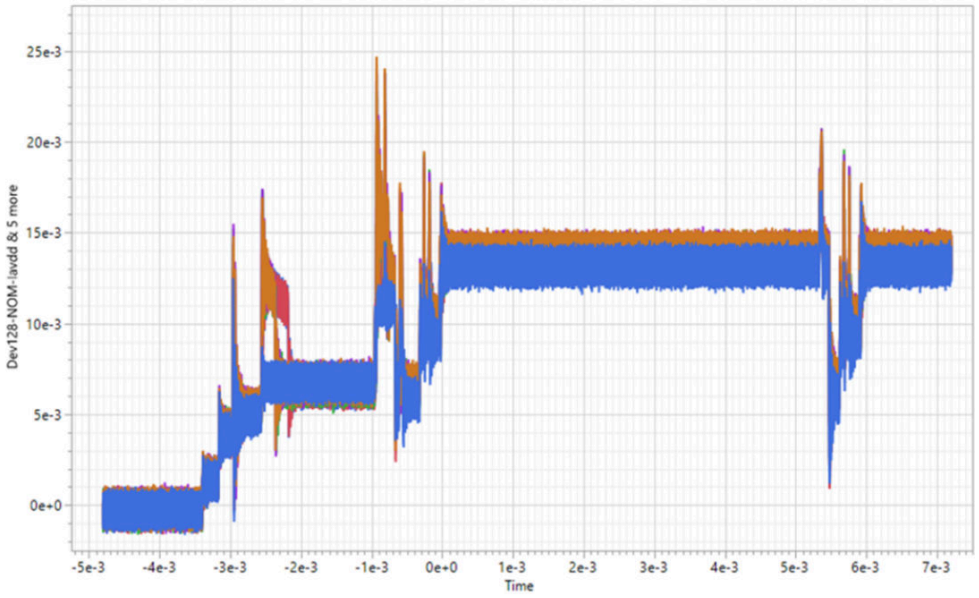


Note: In the figure above, start streaming and first frame of typical current profile (mA) over time (ms) is captured at maximum temperature and voltage.

The curves on the graph below cover different devices tested over different voltage conditions (nominal or maximum).

It is evaluated on a limited number of devices.

Figure 26. **Detail of VANA first transient pulse energy**



8.5 AC ripples

Image sensors require stable power to ensure high-quality image capture, because fluctuations in power can lead to noise in the images. To ensure optimal performance of image sensors, it is important to provide a power supply that has a minimum spurious voltage.

The AC ripple parameter pertains to the sensor's external power sources. It applies to the voltage regulators powering the sensor. The table below defines the limits for permissible residual ripple.

These parameters are specified by design.

Table 16. **AC ripples**

Supply	AC ripples (mV peak to peak)	Frequency range
VANA	10	Up to 10 MHz
VCORE	20	

8.6 CLKIN input

The CLKIN input is for all voltage and temperature conditions.

Table 17. **Typical CLKIN input**

V_{CLKINL}, V_{CKLINH}, f_{CLKIN}, C to Cjitter and duty cycle are evaluated on a limited number of devices.

Symbol	Parameter	Min	Max	Unit
V_{CLKINL}	DC-coupled square wave low-level input	-0.5	0.15 x VDDIO	V
V_{CLKINH}	DC-coupled square wave high-level input	0.85 x VDDIO	VDDIO + 0.5	
f_{CLKIN}	Clock input frequency	6	27	MHz
C to Cjitter	Clock maximum cycle to cycle jitter	—	200	ps
Duty cycle	Clock duty cycle	40	60	%
I_{CLKIN}	Input leakage current	—	10	µA

8.7 Digital inputs

The digital inputs are over process variations at 60°C.

Table 18. Digital inputs over process variations at 60°C

VIL and VIH are evaluated on a limited number of devices.

Symbol	Parameter	Min	Max	Unit
V_{IL}	Low-level input voltage	-0.3	0.3 x VDDIO	V
V_{IH}	High-level input voltage	0.7 x VDDIO	VDDIO + 0.3	
I_{Leak}	Input leakage current (1)	—	10	µA

1. *For 0 ≤ VI ≤ VDDIO*

8.8 Digital outputs

The digital outputs are over process variations at 60°C.

Table 19. Digital outputs

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Low-level output voltage	IOL = -4 mA	—	0.4	V
V_{OH}	High-level output voltage	IOH = 4 mA VDDIO=1.2 V	0.7	—	
		IOH = 4 mA VDDIO=1.8 V	1.4	—	
I_{max}	Maximum current	—	—	4	mA

8.9 I²C interface - SDA, SCL

I²C timing and voltage conform with the norm: UM10204-I2C-bus specification and user manual, Rev. 6, 4 April 2014.

It is evaluated on a limited number of devices.

8.10 I3C interface

I3C timing and voltage conform with the norm :MIPI alliance Errata 02 for MIPI I3C Specification version 1.1.1, 10 March 2022.

It is evaluated on a limited number of devices.

8.11 CSI-2 interface

The CSI-2 interface conforms with the MIPI DPHY specification v1.1.

It is evaluated on a limited number of devices.

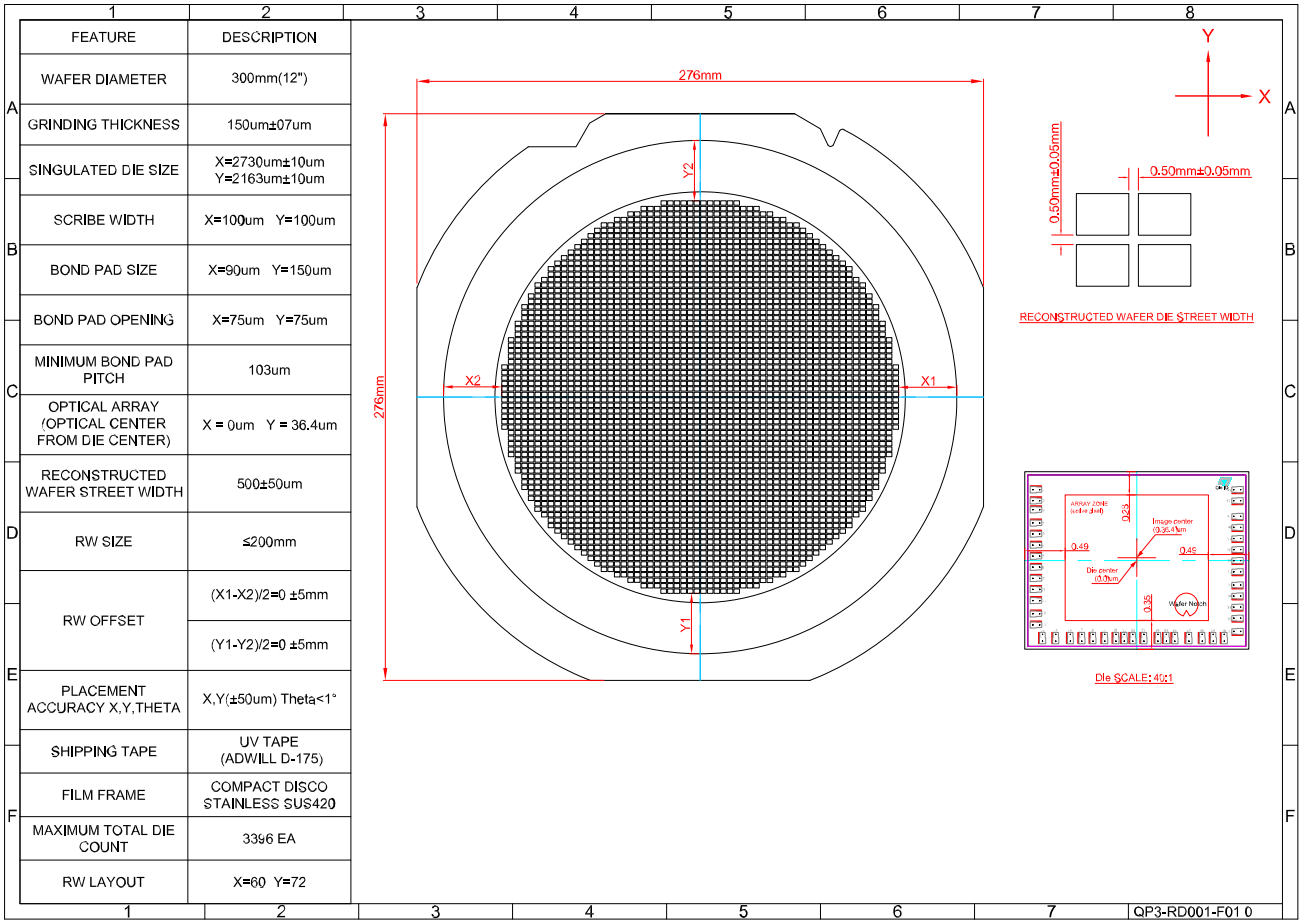
9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

9.1 Packing

Tested dice are delivered as sawn dice, which are reconstructed into a wafer format on UV-tape, and delivered on a metallic ring (see figure below). The frames are packed in plastic containers, each including a maximum of 13 double-spaced reconstructed wafer rings. A mapping information file is also provided for localizing dice that may have been damaged during wafer reconstruction on sticking foil.

Figure 27. Reconstructed wafer information



FEATURE	DESCRIPTION
WAFER DIAMETER	300mm(12")
GRINDING THICKNESS	150um±07um
SINGULATED DIE SIZE	X=2730um±10um Y=2163um±10um
SCRIBE WIDTH	X=100um Y=100um
BOND PAD SIZE	X=90um Y=150um
BOND PAD OPENING	X=75um Y=75um
MINIMUM BOND PAD PITCH	103um
OPTICAL ARRAY (OPTICAL CENTER FROM DIE CENTER)	X = 0um Y = 36.4um
RECONSTRUCTED WAFER STREET WIDTH	500±50um
RW SIZE	≤200mm
RW OFFSET	(X1-X2)/2=0 ±5mm
	(Y1-Y2)/2=0 ±5mm
PLACEMENT ACCURACY X,Y,THETA	X,Y(±50um) Theta<1°
SHIPPING TAPE	UV TAPE (ADWILL D-175)
FILM FRAME	COMPACT DISCO STAINLESS SUS420
MAXIMUM TOTAL DIE COUNT	3396 EA
RW LAYOUT	X=60 Y=72

9.2 Storage information

Store all packing material in an appropriate indoor area. This is to prevent any dust and/or damage from the sun, external light, and physical shocks.

Keep the temperature between 15ºC and 35ºC.

Keep the relative humidity range between 10% and 70% maximum.

Store the reconstructed wafers under vacuum, in their original supplied sealed packing until they are used.

After the packing seal is broken, store the reconstructed wafers under nitrogen (N2) within dedicated closed shelves until they are processed.

Use the trace code to count the storage time. It is written on the package label.

The maximum storage time of the reconstructed wafer is:

- Six months from the trace code date. This is when the wafer is kept in the original sealed packing.
- One week from the trace code date. This is when the original packing seal is open.

The maximum storage time defines the maximum time that can be waited for reconstructed wafer processing. Processing may be for picking and placing, and module integration. If the maximum storage time is not respected, safe processing is not guaranteed.

Note: For further information on reconstructed wafer specifications for visual inspection and packing, refer to the technical note TN1497.

Revision history

Table 20. **Document revision history**

Date	Version	Changes
27-Feb-2023	1	Initial release
27-Jun-2024	2	Updated the document title, cover image, product summary table, "Features", and "Description". Added the ST BrightSense subbrand and "Applications". Reorganized Section 2: Product overview. Added information to Section 2.1: Function description summary and updated Figure 2. Functional block diagram. Updated Table 2. Technical specifications. Updated Section 3.1.1: Inter-integrated circuit (I²C). Updated Section 3.1.2: MIPI I3C^{SM} client interface. Updated Section 3.1.3: Camera serial interface (CSI). Updated wording in Section 3.4: Video pipe. Updated Section 3.4.3: Defective pixel correction. Updated Section 3.4.4: Dark calibration. Updated Section 3.4.5: Autoexposure. Modified binning to digital binning and updated Section 3.4.6: Digital binning. Updated Section 3.4.7: Embedded status lines. Updated Section 3.4.9: Context management. Updated Section 3.4.1: Analog subsampling. Updated Section 3.5: Synchronization modes. Updated Section 3.6: General purpose input/outputs (GPIOs). Updated Table 4. Example of functional use cases. Updated Section 3.7.1: Low power consumption. Added Section 3.7.3: Differential mode. Added Section 3.7.5: Spatial HDR. Updated Figure 16. Die mechanical dimensions (µm) and Figure 17. Pad details. Added Table 7. Pad description table. Updated some net names in Table 8. Pad coordinates and modified term pin to pad. Updated Section 6.1: Additional components. Updated Section 6.3: Device power up sequence. Added Section 7.1: Quantum efficiency. Added Section 7.2: MTF. Renamed CRA section to Section 7.3: Microlenses and CRA matching and updated. Updated Section 8: Electrical characteristics. Added Section 8.1: Absolute maximum ratings. Updated Table 13. Operating conditions. Updated Section 8.3: Power consumption. Added Section 8.4: Current profile. Updated Section 8.5: AC ripples. Renamed EXTCLK input section to Section 8.6: CLKIN input and updated.

Date	Version	Changes
27-Jun-2024	2 continued	Seperated Digital inputs and outputs into two seperate sections and updated values in Table 18. Digital inputs over process variations at 60°C and Table 19. Digital outputs. Updated Section 8.9: I²C interface - SDA, SCL. Added Section 8.10: I3C interface. Updated Section 8.11: CSI-2 interface. Modified title Sawn die information to Section 9.1: Packing and updated description. Added Section 9.2: Storage information.
30-Jul-2024	3	Modified the voltage value for the core digital logic and MIPI CSI-2 output drivers in Section 2.2: Technical specifications summary, Section 3.2: Power supplies, and Table 7. Pad description table. Updated Figure 24. Guideline for lens CRA matching at 520 nm.

Contents

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