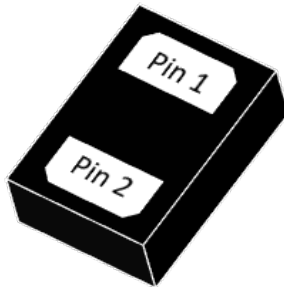
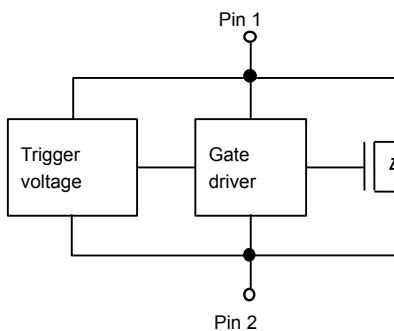


22 V, 16 A unidirectional self-controlled TVS in SOD882 (0402)



SOD882 (0402) package



Pin configuration

Features

- Low flat clamping voltage
- Unidirectional diode
- Low leakage current
- SOD882 (0402) package
- ECOPACK2 compliant component
- Exceeds the IEC 61000-4-2 level 4 standard:
 - ± 8 kV (contact discharge)
 - ± 30 kV (air discharge)

Application

Where transient over voltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones, and accessories
- Tablets and notebooks
- Portable multimedia devices and accessories
- Wearable, home automation, healthcare
- Highly integrated systems
- USB Type-C V_{BUS}

Description

The TVS221SC-1T2 is a unidirectional single line TVS diode designed to protect the power line or other low speed I/O against ESD and small surge transients. These self-controlled TVS offer benefits such as a flat clamping voltage over the temperature range and over the current range. Thanks to an extremely low R_{DS_ON} the quasi constant clamping voltage remains much smaller than for a conventional TVS diode.

The device is ideal for applications where board space saving is required

Product status link

[TVS221SC-1T2](#)

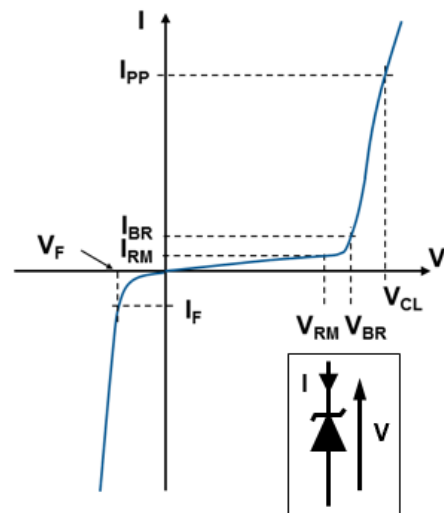
1 Characteristics

Table 1. Absolute maximum ratings ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Parameter		Value	Unit
V_{pp}	Peak pulse voltage	IEC 61000-4-2 contact discharge	± 8	kV
		IEC 61000-4-2 air discharge	± 30	
		HBM JESD22-A114D, level 2	± 2	
P_{pp}	Peak pulse power (8/20 μs)		440	W
I_{pp}	Peak pulse current (8/20 μs)		16	A
T_{op}	Operating junction temperature range		-40 to 125	$^{\circ}\text{C}$
T_{stg}	Storage junction temperature range		-55 to 150	$^{\circ}\text{C}$
T_L	Maximum lead temperature for soldering during 10 s		260	$^{\circ}\text{C}$

Figure 1. Electrical characteristics (definitions)

- V_{RM} Maximum stand-off voltage
- I_{RM} Maximum leakage current @ V_{RM}
- V_R Stand-off voltage
- I_R Leakage current @ V_R
- V_{BR} Breakdown voltage @ I_{BR}
- I_{BR} Breakdown current
- V_{CL} Clamping voltage @ I_{PP}
- I_{PP} Peak pulse current
- R_D Dynamic resistance
- V_F Forward voltage drop @ I_F
- I_F Forward current


Table 2. Electrical characteristics (values) ($T_{amb} = 25\text{ }^{\circ}\text{C}$)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{RM}	Stand-off voltage			22	V
I_{RM}	Leakage current		$V_{RM} = 22\text{ V}$	200	nA
V_{BR}	Breakdown voltage		$I_R = 1\text{ mA}$	27	V
V_{CL}	Reverse clamping voltage		$I_{PP} = 16\text{ A } 8/20\text{ }\mu\text{s}$, (pin 1 to pin 2)	27.4	V
	Forward clamping voltage		$I_{PP} = 16\text{ A } 8/20\text{ }\mu\text{s}$, (pin 2 to pin 1)	1.28	
R_D	Dynamic resistance		8/20 μs waveform (from $I_{PP} = 2\text{ A}$ to $I_{PP} = 16\text{ A}$)	16	m Ω
C_{LINE}	Line capacitance		$V_{LINE} = 22\text{ V}$, $F = 1\text{ MHz}$	75	pF
V_F	Forward voltage		$I_F = 10\text{ mA}$, (pin 2 to pin 1)	0.55	V

1.1 Characteristics (curves)

Figure 2. IEC61000-4-5 (+16 A)

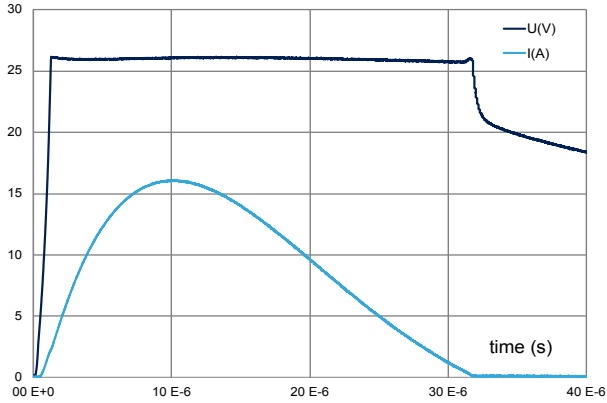


Figure 3. Breakdown voltage versus junction temperature

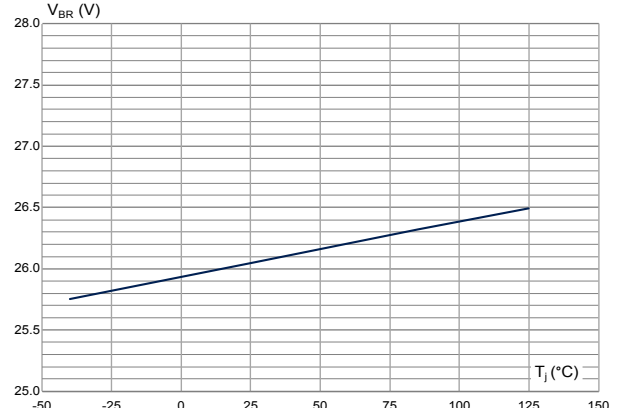


Figure 4. Junction capacitance versus reverse applied voltage

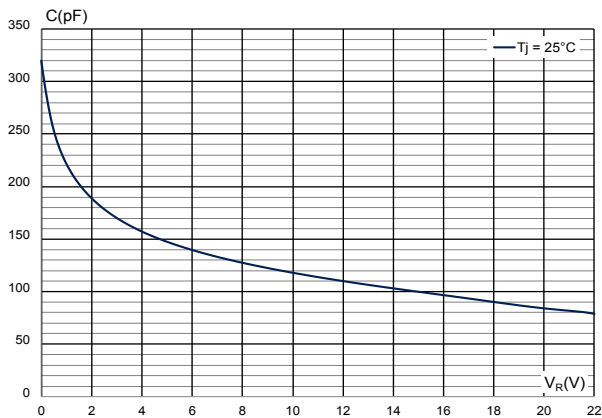


Figure 5. Peak pulse current versus initial junction temperature

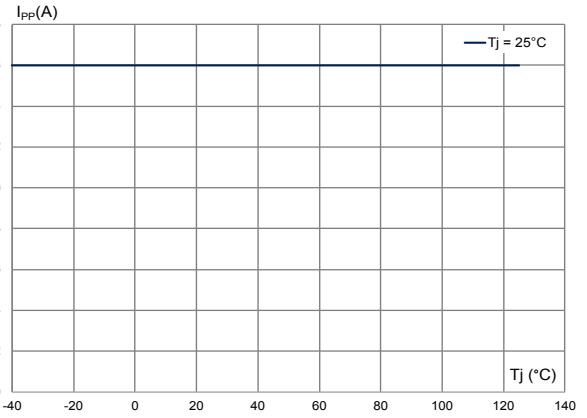


Figure 6. Clamping voltage versus peak pulse current

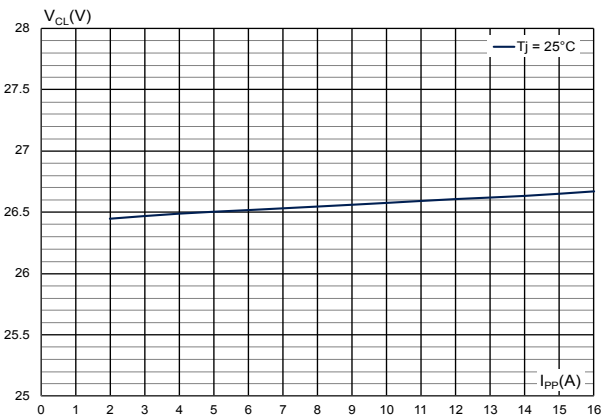


Figure 7. Leakage current versus junction temperature

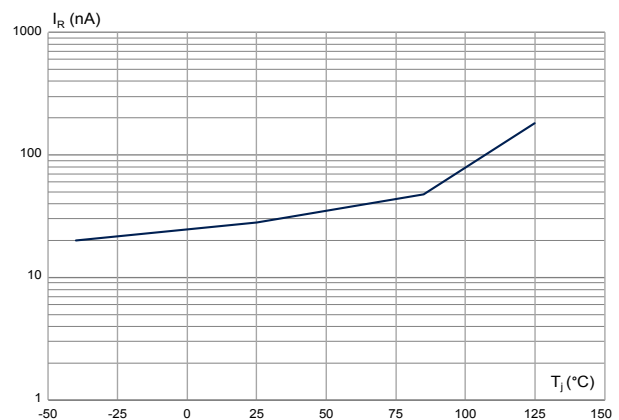


Figure 8. Clamping voltage at I_{PP} max versus junction temperature

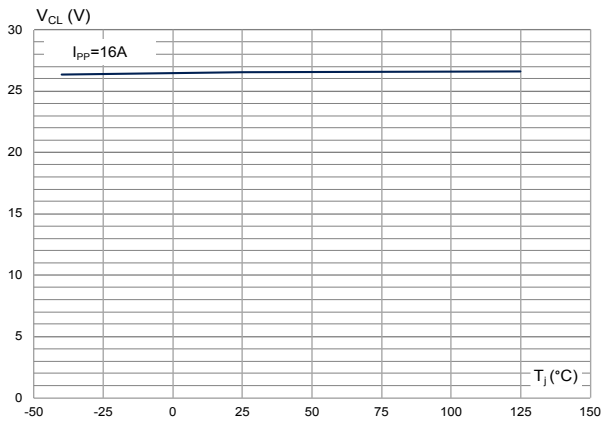


Figure 9. Dynamic leakage vs Signal Slew Rate

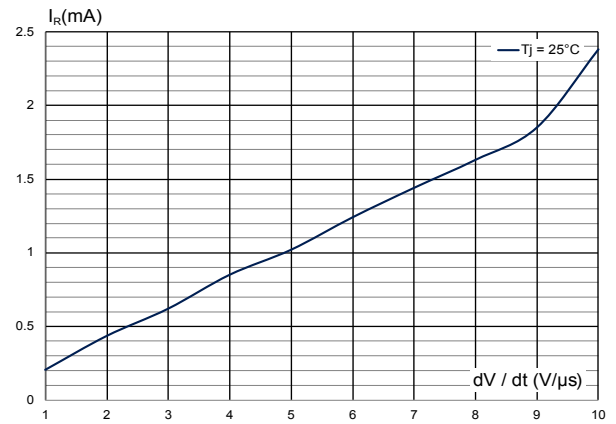


Figure 10. ESD response to IEC 61000-4-2 (+8 kV contact discharge)

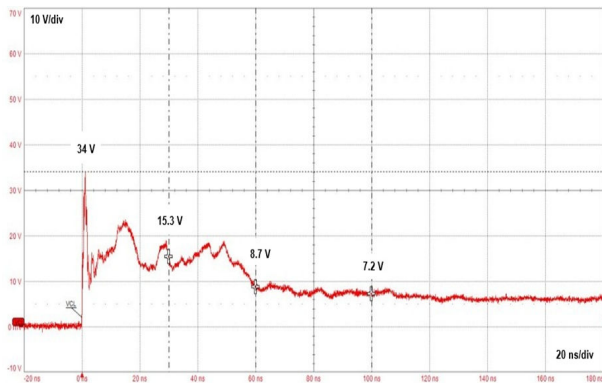
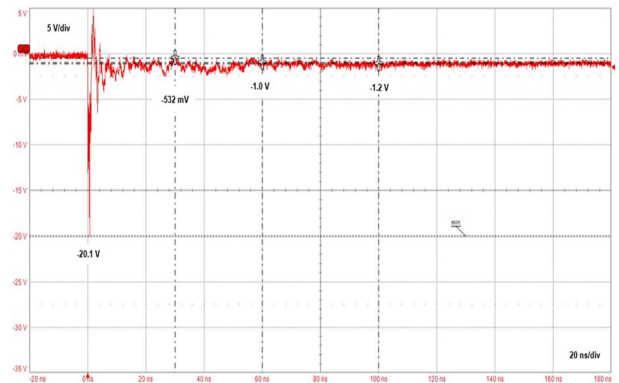


Figure 11. ESD response to IEC 61000-4-2 (-8 kV contact discharge)

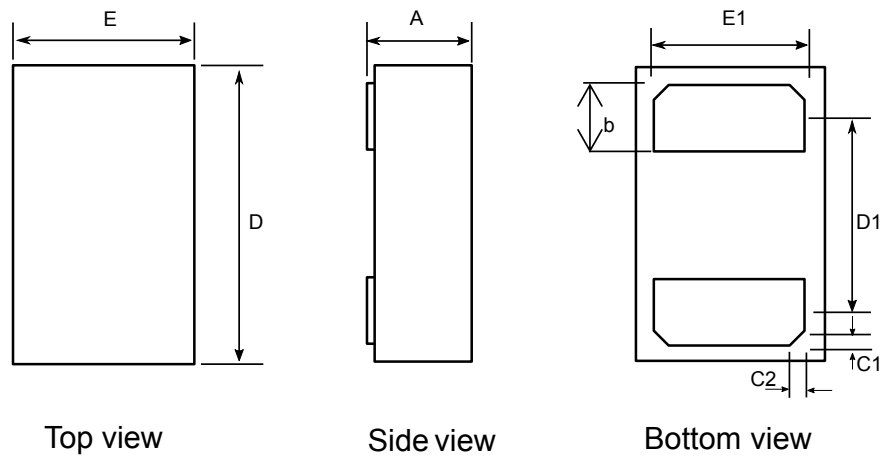


2 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 SOD882 (0402) package-information

Figure 12. SOD882 (0402) package outline



DM00337698_optionH_rev14

Table 3. SOD882 (0402) mechanical data

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.250	0.280	0.310
b	0.205	0.235	0.265
D	0.990	1.020	1.050
E	0.580	0.610	0.640
D1		0.650	
E1	0.445	0.475	0.505
C1		0.052	
C2		0.052	

Figure 13. Marking

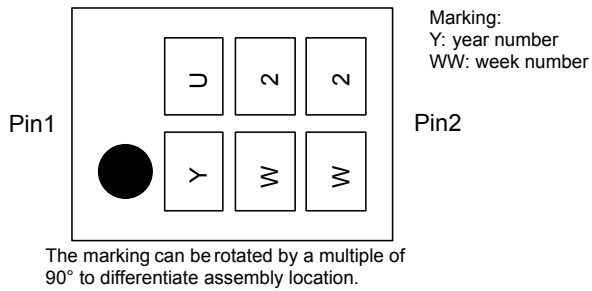


Figure 14. Package orientation in reel

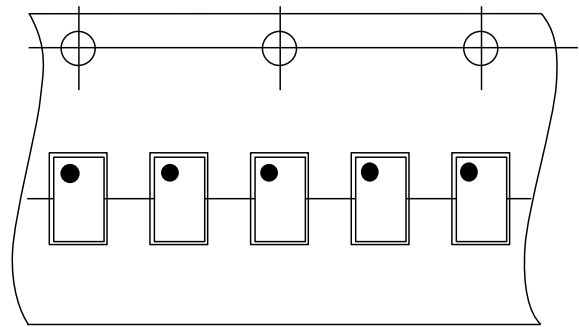


Figure 15. Tape outline

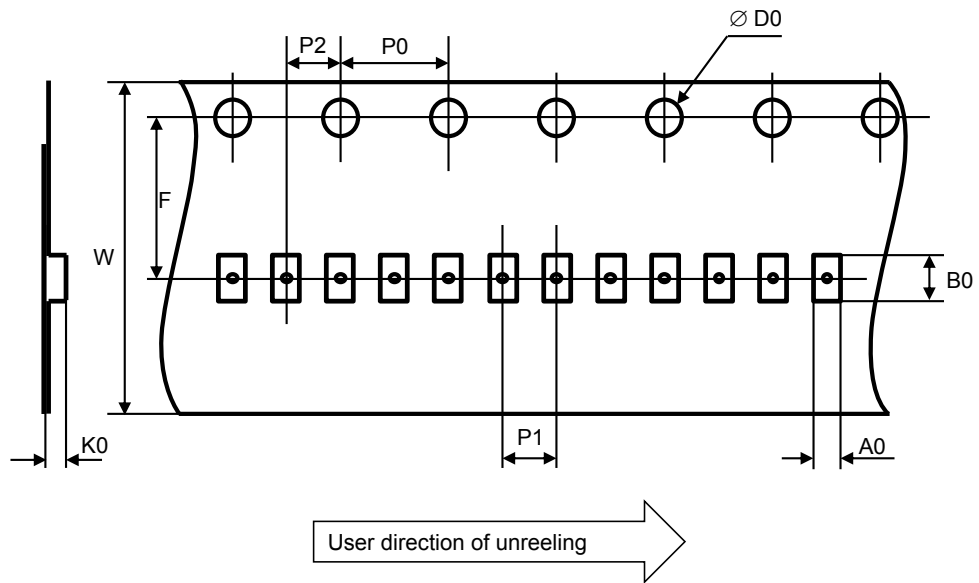


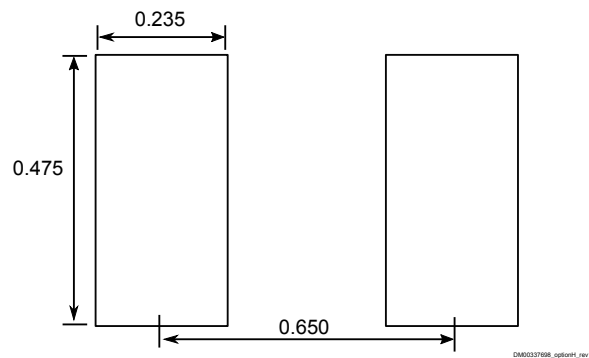
Table 4. Tape dimension values

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A0	0.68	0.71	0.74
B0	1.09	1.12	1.15
D0	1.40	1.50	1.60
F	3.45	3.50	3.55
K0	0.32	0.35	0.38
P0	3.9	4.00	4.10
P1	1.95	2.00	2.05
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

3 PCB assembly recommendations

3.1 Recommended footprint

Figure 16. Recommended footprint in mm

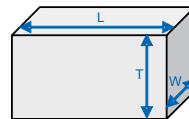


Note: Non Solder Mask Defined / Solder Mask Defined (SMD) recommended

3.2 Stencil opening design

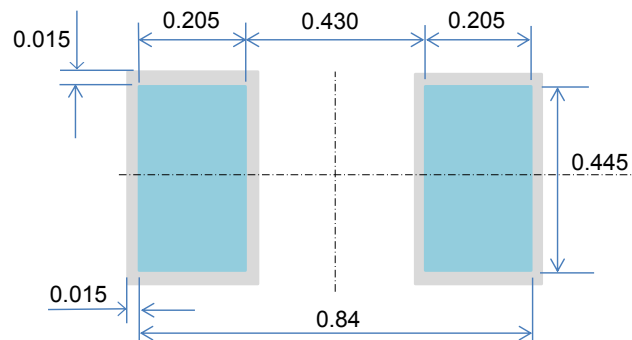
1. General recommendation on stencil opening design
 - a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).

Figure 17. Stencil opening recommendation



- b. General design rule
 - Stencil thickness (T) = 75 ~ 125 μm
 - $\frac{W}{T} \geq 1.5$
 - $\frac{L \times W}{2T(L + W)} \geq 0.66$
1. Reference design
 - a. Stencil opening thickness: 100 μm
 - b. Stencil opening for leads: Opening to footprint ratio is 90 %

Figure 18. Recommended stencil window position in mm



3.3 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. "No clean" solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Use solder paste with fine particles: powder particle size 20-45 μm .

3.4 Placement

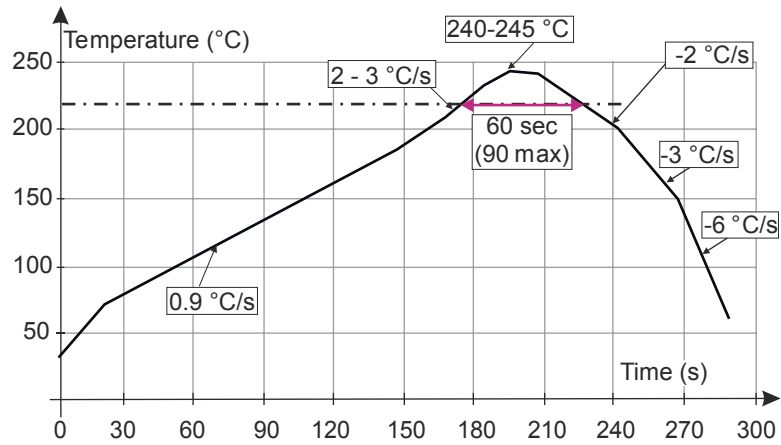
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.6 Reflow profile

Figure 19. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TVS221SC-1T2	See Figure 13.	SOD882 (0402)	0.425 mg	15000	Tape and reel

1. The marking can be rotated by multiples of 90° to differentiate assemble location.

Revision history

Table 6. Document revision history

Date	Revision	Changes
05-Jun-2026	1	Initial release.
23-Jun-2026	2	Updated confidentiality level to public.

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