TSV7742

Datasheet

Automotive grade, high bandwidth (20 MHz) low offset (150 µV), high CMR rail-to-rail 5 V op amp



TSV7742
MiniSO8

Maturity status link
TSV7742

Product status link	Channel	Automotive	Package
TSV7742IST	2		MiniSO8
TSV7742IYST	2	•	MiniSO8

Related products	
TSV7722	Low rail 22 MHz amplifier
TSV772	Rail-to-rail 20 MHz amplifier

Features

- Automotive grade qualification
- Gain bandwidth product 20 MHz, unity gain stable
- Low input offset voltage 40 µV typ., 150 µV max.
- Outstanding common-mode voltage rejection 120 dB
- Rail-to-rail input and output
- Wide supply voltage range: 2.0 V to 5.5 V
- Low noise: 7 nV/√Hz, low distortion
- Benefits:
  - Accuracy of measurement is virtually unaffected by input common-mode
  - Signal conditioning for high frequencies

Applications

- Precision sensor signal conditioning
- Biomedical and patient-monitoring instrumentation
- Industrial measurement and process control
- Data acquisition and ADC input buffering
- Instrumentation amplification

Description

The TSV7742 is dual amplifiers that have 20 MHz-bandwidth and unity-gain stability. It features a rail-to-rail input stage and a maximum input offset voltage of 150 µV, which allows for accurate amplification of small-amplitude input signals. Its unique architecture also provides exceptional rejection of common-mode voltage and virtually zero distortion of the input signal versus the variations of the common-mode. The TSV7742 can operate from a single supply of 2.0 V to 5.5 V and is fully characterized for an output capacitor of 47 pF, making it an easy-to-use input buffer for A/D converters.

1 Pin description

1.1 TSV7742 dual operational amplifier: MiniSO8

Figure 1. **Pin connections MiniSO8 (top view)**

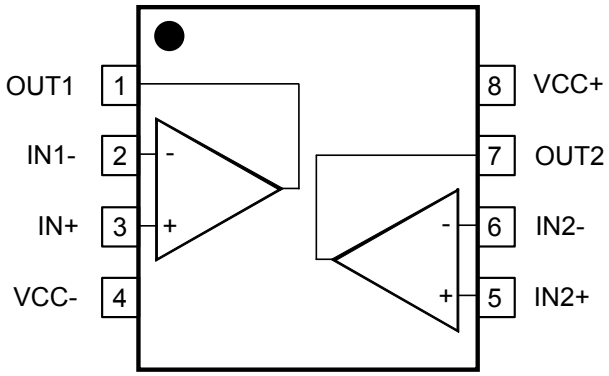


Table 1. **Pin description**

Pin n°	Pin name	Description
1	OUT1	Output channel 1
2	IN1-	Inverting input channel 1
3	IN1+	Non-inverting input channel 1
4	VCC-	Negative supply voltage
5	IN2+	Non-inverting input channel 2
6	IN2-	Inverting input channel 2
7	OUT2	Output channel 2
8	VCC+	Positive supply voltage

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter [1]	Value	Unit
V_{CC}	Supply voltage	-0.3 to 6	V
V_{id}	Input voltage differential (V_{IN+} - V_{IN-}) [2]	$\pm V_{CC}$	V
V_{in}	Input pins voltage	(V_{CC-}) - 0.3 to (V_{CC+}) + 0.3	V
I_{in}	Input current	±10	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{th-ja} [3]	Thermal resistance junction-to-ambient		°C / W
	MiniSO8	190	
T_j	Maximum junction temperature	150	°C
ESD	HBM: human body model [4]	2	kV
	CDM: charged device model [5]	1	kV

1. *All voltage values are with respect to the VCC- pin, unless otherwise specified.*
2. *The maximum input voltage differential value may be extended to the condition that the input current is limited to ±10 mA.*
3. *R_{th-ja} is a typical value obtained with PCB according to JEDEC 2s2p without vias.*
4. *Human body model: the test HBM is done in accordance with the standards ESDA-JS-001-2017 and Q100-002.*
5. *Charged device model: the test CDM is done in accordance with the standards ESDA-JS-002-2018 and Q100-011.*

Table 3. Operating conditions

Symbol	Parameter	Value
V_{CC}	Supply voltage	2.0 V to 5.5 V
V_{icm}	Common-mode input voltage range	V_{CC-} – 0.1 V to V_{CC+} + 0.1 V
T_{oper}	Operating free air temperature range	-40 °C to +125 °C

3 Electrical characteristics

Table 4. Electrical characteristics at V_{CC} = 5 V, V_{icm} = V_{OUT} = V_{CC} / 2, T = 25 °C, R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 47 pF (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		40	± 150	µV
		-40 °C ≤ T ≤ 125 °C			± 650	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift (1)	-40 °C ≤ T ≤ 125 °C			± 5	µV/°C
I_{ib}	Input bias current for channel 2 (IN2+ and IN2- pins) (2)	T = 25 °C		0.5	2	pA
		-40 °C ≤ T ≤ 125 °C			50	
	Input bias current for channel 1 (IN1+ and IN1- pins) (2)	T = 25 °C		0.5	2	
		-40 °C ≤ T ≤ 125 °C			800	
I_{io}	Input offset current for channel 2 (IN2+ and IN2- pins) (2)	T = 25 °C		0.01	1	pA
		-40 °C ≤ T ≤ 125 °C			5	
	Input offset current for channel 1 (IN1+ and IN1- pins) (2)	T = 25 °C		0.01	1	
		-40 °C ≤ T ≤ 125 °C			200	
A_{VD}	Open loop gain	V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, T = 25 °C	110			dB
		V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, -40 °C ≤ T ≤ 125 °C	100			
		R_L = 2 kΩ, T = 25 °C, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV	105			
		R_L = 2 kΩ, -40 °C ≤ T ≤ 125 °C, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV	96			
CMR	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} - 0.1 V ≤ V_{icm} ≤ V_{CC+} + 0.1 V, T = 25 °C	100	120		dB
		V_{CC-} - 0.1 V ≤ V_{icm} ≤ V_{CC+} + 0.1 V, - 40 °C ≤ T ≤ 125 °C	96			
SVR	Supply-voltage rejection ratio 20.log($\Delta V_{io}/\Delta_{CC}V_{CC}$)	2.0 V ≤ V_{CC} ≤ 5.5 V, T = 25 °C, V_{icm} = 0 V	90	110		dB
		2.0 V ≤ V_{CC} ≤ 5.5 V, V_{icm} = 0 V, -40 °C ≤ T ≤ 125 °C	90			
V_{OH}	High-level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
V_{OL}	Low-level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
I_{OUT}	I_{SINK} (R_L connected to V_{CC+})	T = 25 °C	45	65		mA
		-40 °C ≤ T ≤ 125 °C	30			
	I_{SOURCE} (R_L connected to V_{CC-})	T = 25 °C	45	60		
		-40 °C ≤ T ≤ 125 °C	30			
I_{CC}	Supply current (by operational amplifier)	T = 25 °C		2.1	2.2	mA
		-40 °C ≤ T ≤ 125 °C			2.2	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AC performance						
GBP	Gain bandwidth product		16	20		MHz
SR	Slew rate	A_V = 1 V/V, 10% to 90% (3)	11	15		V/µs
t_S	Settling time	R_L = 4.7 kΩ, A_V = -1 V/V, to 0.1%, V_{in} = 2 Vp-p		240		ns
		R_L = 4.7 kΩ, A_V = -1 V/V, to 0.01%, V_{in} = 2 Vp-p (4)		440		
t_{rec}	Overload recovery time	V_{OUT} = 50 mV from initial value, A_V = +1		80		
CR	Crosstalk	V_{OUT} = 4 V_{pp}, A_V = +101 V/V, f = 1 kHz		120		dB
Φm	Phase margin			40		degrees
GM	Gain margin			8		dB
en	Input voltage noise density	f = 1 kHz		10		nV/√Hz
		f = 10 kHz		7		
en p-p	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		4		$µV_{pp}$
C_{in}	Differential input capacitance			2.2		pF
	Common-mode input capacitance			0.8		

1. *See 4.2 input offset voltage drift over the temperature.*
2. *Guaranteed by design and characterization on a sample of parts, not tested in production.*
3. *The slew rate value is the average of rising and falling values.*
4. *Settling time at 0.01% is guaranteed by design.*

Table 5. Electrical characteristics at V_{CC} = 3.3 V, V_{icm} = V_{OUT} = V_{CC} / 2, T = 25 °C, R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 47 pF (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		40	± 150	µV
		-40 °C ≤ T ≤ 125 °C			± 650	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift (1)	-40 °C ≤ T ≤ 125 °C			± 5	µV/°C
I_{ib}	Input bias current for channel 2 (IN2+ and IN2- pins) (2)	T = 25 °C		0.5	2	pA
		-40 °C ≤ T ≤ 125 °C			50	
	Input bias current for channel 1 (IN1+ and IN1- pins) (2)	T = 25 °C		0.5	2	
		-40 °C ≤ T ≤ 125 °C			800	
I_{io}	Input offset current for channel 2 (IN2+ and IN2- pins) (2)	T = 25 °C		0.01	1	pA
		-40 °C ≤ T ≤ 125 °C			5	
	Input offset current for channel 1 (IN1+ and IN1- pins) (2)	T = 25 °C		0.01	1	
		-40 °C ≤ T ≤ 125 °C			200	
A_{VD}	Open loop gain	V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, T = 25 °C	106			dB
		V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, -40 °C ≤ T ≤ 125 °C	96			
		R_L = 2 kΩ, T = 25 °C, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV	101			
		R_L = 2 kΩ, -40 °C ≤ T ≤ 125 °C, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV	92			
CMR	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} - 0.1 V ≤ V_{icm} ≤ V_{CC+} + 0.1 V, T = 25 °C	95	107		dB
		V_{CC-} - 0.1 V ≤ V_{icm} ≤ V_{CC+} + 0.1 V, - 40 °C ≤ T ≤ 125 °C	92			
V_{OH}	High-level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
V_{OL}	Low-level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
I_{OUT}	I_{SINK} (R_L connected to V_{CC+})	T = 25 °C	45	60		mA
		-40 °C ≤ T ≤ 125 °C	30			
	I_{SOURCE} (R_L connected to V_{CC-})	T = 25 °C	45	55		
		-40 °C ≤ T ≤ 125 °C	30			
I_{CC}	Supply current (by operational amplifier)	T = 25 °C		1.9	2.2	mA
		-40 °C ≤ T ≤ 125 °C			2.2	
AC performance						
GBP	Gain bandwidth product		16	20		MHz
SR	Slew rate	A_V = 1 V/V, 10% to 90% (3)	11	13		V/µs
t_S	Settling time	R_L = 4.7 kΩ, A_V = -1 V/V, to 0.1%, V_{in} = 1 Vp-p		220		ns
		R_L = 4.7 kΩ, A_V = -1 V/V, to 0.01%, V_{in} = 1 Vp-p (4)		260		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{rec}	Overload recovery time	V_{OUT} = 50 mV from initial value, A_V = +1		80		ns
Φm	Phase margin			38		degrees
GM	Gain margin			8		dB
en	Input voltage noise density	f = 1 kHz		10		nV/√Hz
		f = 10 kHz		7		
en p-p	Input noise voltage	0.1 Hz ≤ f ≤ 10 Hz		4		μV_{pp}
C_{in}	Differential input capacitance			2.2		pF
	Common-mode input capacitance			0.8		

1. *See 4.2 input offset voltage drift over the temperature.*
2. *Guaranteed by design and characterization on a sample of parts, not tested in production.*
3. *The slew rate value is the average of rising and falling values.*
4. *Settling time at 0.01% is guaranteed by design.*

Table 6. Electrical characteristics at V_{CC} = 2.5 V, V_{icm} = V_{OUT} = V_{CC} / 2, T = 25 °C, R_L = 10 kΩ connected to V_{CC} / 2 and C_L = 47 pF (unless otherwise specified).

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T = 25 °C		40	± 150	µV
		-40 °C ≤ T ≤ 125 °C			± 650	
$\Delta V_{io}/\Delta T$	Input offset voltage temperature drift (1)	-40 °C ≤ T ≤ 125 °C			± 5	µV/°C
I_{ib}	Input bias current for channel 2 (IN2+ and IN2- pins) (2)	T = 25 °C		0.5	2	pA
		-40 °C ≤ T ≤ 125 °C			50	
	Input bias current for channel 1 (IN1+ and IN1- pins) (2)	T = 25 °C		0.5	2	
		-40 °C ≤ T ≤ 125 °C			800	
I_{io}	Input offset current for channel 2 (IN2+ and IN2- pins) (2)	T = 25 °C		0.01	1	pA
		-40 °C ≤ T ≤ 125 °C			5	
	Input offset current for channel 1 (IN1+ and IN1- pins) (2)	T = 25 °C		0.01	1	
		-40 °C ≤ T ≤ 125 °C			200	
A_{VD}	Open loop gain	V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, T = 25 °C	102			dB
		V_{CC-} + 100 mV ≤ V_{OUT} ≤ V_{CC+} - 100 mV, -40 °C ≤ T ≤ 125 °C	92			
		R_L = 2 kΩ, T = 25 °C, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV	97			
		R_L = 2 kΩ, -40 °C ≤ T ≤ 125 °C, V_{CC-} + 200 mV ≤ V_{OUT} ≤ V_{CC+} - 200 mV	88			
CMR	Common-mode rejection ratio 20.log ($\Delta V_{io}/\Delta V_{icm}$)	V_{CC-} - 0.1 V ≤ V_{icm} ≤ V_{CC+} + 0.1 V, T = 25 °C	92	107		dB
		V_{CC-} - 0.1 V ≤ V_{icm} ≤ V_{CC+} + 0.1 V, - 40 °C ≤ T ≤ 125 °C	84			
V_{OH}	High-level output voltage drop (V_{OH} = V_{CC+} - V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
V_{OL}	Low-level output voltage drop (V_{OL} = V_{OUT})	T = 25 °C			10	mV
		-40 °C ≤ T ≤ 125 °C			20	
I_{OUT}	I_{SINK} (R_L connected to V_{CC+})	T = 25 °C	45	60		mA
		-40 °C ≤ T ≤ 125 °C	30			
	I_{SOURCE} (R_L connected to V_{CC-})	T = 25 °C	45	55		
		-40 °C ≤ T ≤ 125 °C	30			
I_{CC}	Supply current (by operational amplifier)	T = 25 °C		1.8	2.2	mA
		-40 °C ≤ T ≤ 125 °C			2.2	
AC performance						
GBP	Gain bandwidth product		16	20		MHz
SR	Slew rate	A_V = 1 V/V, 10% to 90% (3)	9	12		V/µs
t_S	Settling time	R_L = 4.7 kΩ, A_V = -1 V/V, to 0.1%, V_{in} = 1 Vp-p		220		ns
		R_L = 4.7 kΩ, A_V = -1 V/V, to 0.01%, V_{in} = 1 Vp-p (4)		260		

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{rec}	Overload recovery time	V_{OUT} = 50 mV from initial value, A_V = +1		100		ns
Φm	Phase margin			37		degrees
GM	Gain margin			8		dB
en	Input voltage noise density	f = 1 kHz		10		nV/√Hz
		f = 10 kHz		7		
en p-p	Input noise voltage	0.1 Hz ≤ f ≤ 10 kHz		4		µVpp
C_{in}	Differential input capacitance			2.2		pF
	Common-mode input capacitance			0.8		

1. *See 4.2 input offset voltage drift over the temperature.*
2. *Guaranteed by design and characterization on a sample of parts, not tested in production.*
3. *The slew rate value is the average of rising and falling values.*
4. *Settling time at 0.01% is guaranteed by design.*

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 MiniSO8 package information

Figure 2. MiniSO8 package outline

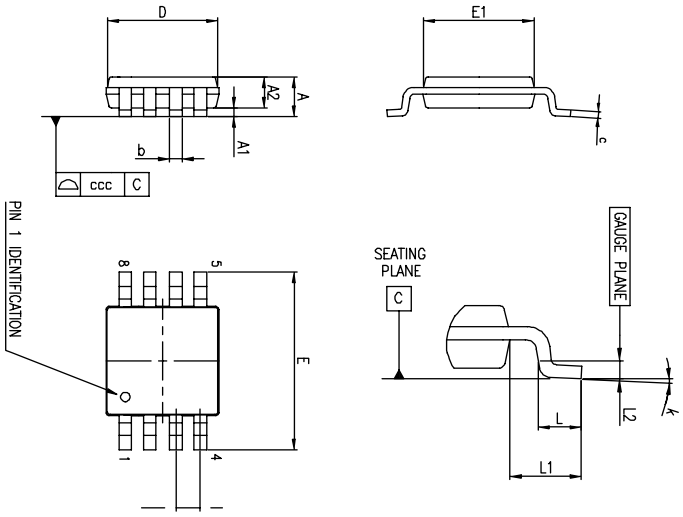


Table 7. MiniSO8 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.0006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.22		0.40	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.80	3.00	3.20	0.11	0.118	0.126
E	4.65	4.90	5.15	0.183	0.193	0.203
E1	2.80	3.00	3.10	0.11	0.118	0.122
e		0.65			0.026	
L	0.40	0.60	0.80	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.010	
k	0°		8°	0°		8°
ccc			0.10			0.004

5 Ordering information

Table 8. Order code

Order code	Channel	Automotive	Package	Marking
TSV7742IST	1		MiniSO8	K257
TSV7742IYST	1	• (1)	MiniSO8	K258

1. *Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent. For qualification status detail, check " Maturity Status Link " on first page (" Quality & Reliability " tab on www.st.com).*

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
18-Nov-2026	1	Initial release.

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