TS3002

Datasheet

High-speed, push-pull dual comparator with rail-to-rail inputs



MiniSO8



DFN8 2x2 mm
(Automotive version with wettable flanks)

Features

- Automotive qualification AEC-Q100
- Fast propagation delay: 2 ns typ.
- Max. toggle frequency 375 MHz or 750 Mbps
- Rail-to-rail inputs
- Push-pull outputs
- Wide supply voltage 2.4 V to 5.5 V
- High ESD tolerance: 4 kV HBM
- Wide temperature range: -40 to +125 °C
- Safety capable: Documentation available to aid functional safety system design

Applications

- Industrial
- Automotive
- LiDAR
- Time-of-flight
- Crystal oscillator for high-speed ADCs, ethernet, radar and satellite communication systems
- Communication equipment

Product status link
TS3002

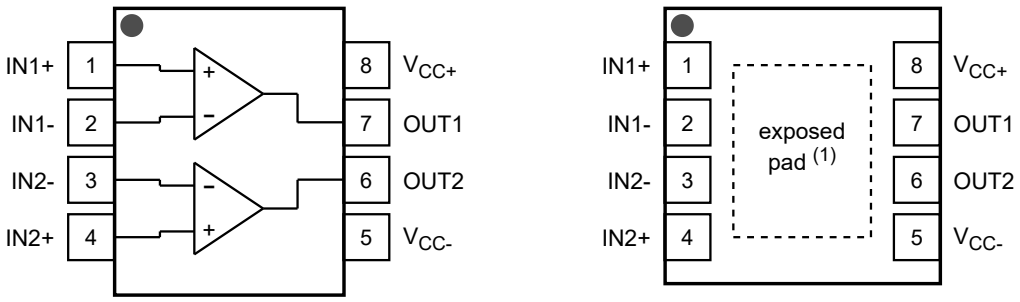
Related products	
TSV792	50 MHz op amp

Description

The TS3002 automotive dual comparator has excellent response time ideally suited for laser control and communication equipment. It is specified for supply voltages from 2.4 to 5.5 V. The device operates over a wide temperature range from -40 °C to 125 °C making it ideal for industrial and automotive applications with the associated qualification. Thanks to its small package size, the TS3002 can be used in applications where space on the board is limited.

1 Pin description

Figure 1. **Pin connection TS3002 (top view)**



MiniSO8 **DFN8 2 x 2 mm**

Table 1. **Pin description**

Pin	Pin name	Description
1	IN1 +	Positive input voltage
2	IN1 -	Negative input voltage
3	IN2 -	Negative input voltage
4	IN2 +	Positive input voltage
5	V_{CC-}	Negative supply voltage
6	OUT2	Output voltage
7	OUT1	Output voltage
8	V_{CC+}	Positive supply voltage
	ep	exposed pad(1)

1. *Exposed pad can be left floating or connected to Vcc-.*

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	6	V
V_{ID}	Differential input voltage (2)	± V_{CC}	V
V_{IN}	Input voltage range	(V_{CC}-) - 0.3 to (V_{CC}+) + 0.3	V
I_{IN}	Input current (3)	10	mA
V_{OUT}	Output voltage (4)	(V_{CC}-) - 0.3 to (V_{CC}+) + 0.3	V
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
R_{TH-JA}	Thermal resistance junction to ambient (5) (6) MiniSO8 DFN8 2x2 exposed pad	 127 57	°C/W
ESD	Human body model (HBM) (7)	4	kV
	Charged device model (CDM) (8)	1.5	

1. *All voltage values, except differential voltages, are referenced to V_{CC}-. V_{CC} is defined as the difference between V_{CC}+ and V_{CC}-.*
2. *The magnitude of input and output voltages must never exceed the supply rail ±0.3 V.*
3. *Input current must be limited by a resistor in series with the inputs.*
4. *Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.3 V beyond the supply rails must be current-limited to 50 mA or less.*
5. *Rth are typical values.*
6. *Short-circuits can cause excessive heating. These values are typical.*
7. *According to JEDEC standard JESD22-A114F.*
8. *According to ANSI/ESD STM5.3.1.*

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.4 to 5.5	V
V_{IN}	Input voltage	V_{CC-} -0.2 to V_{CC+} + 0.2	V
V_{OUT}	Output voltage	V_{CC-} to V_{CC+}	V
T_{oper}	Operating temperature range	-40 to +125	°C

3 Electrical characteristics

Table 4. Electrical characteristics, V_{CC} = 5 V, V_{icm} = V_{CC-} + 300 mV, C_L = 5 pF, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage (1)	T_{amb} = + 25 °C	-7		+7	mV
		T_{min} < T_{amb} < T_{max}	-9		9	
$\lvert\Delta V_{IO}/\Delta T\rvert$	Input offset voltage drift			3		µV/°C
V_{HYST}	Input hysteresis voltage (2)	T_{amb} = + 25 °C	2	6	15	mV
		T_{min} < T_{amb} < T_{max}	1.5		20	
$\lvert I_{IB}\rvert$	Input bias current (3)	T_{amb} = + 25 °C		5	50	pA
		T_{min} < T_{amb} < T_{max}			200	
$\lvert I_{IO}\rvert$	Input offset current (3)	T_{amb} = + 25 °C		1	25	
		T_{min} < T_{amb} < T_{max}			100	
C_{IN}	Input capacitance (3)			1		pF
CMRR	Common mode rejection ration	V_{CC-} ≤ V_{icm} ≤ V_{CC+}		72		dB
SVR	Supply voltage rejection ration	ΔV_{CC} = 2.4 V to 5 V, T_{amb} = + 25 °C		86		
V_{OL}	Low level output voltage from V_{CC-}	I_{sink} = 1 mA, T_{amb} = + 25 °C		44	60	mV
		T_{min} < T_{amb} < T_{max}			100	
V_{OH}	High level output voltage from V_{CC+}	I_{source} = 1 mA, T_{amb} = + 25 °C		56	60	
		T_{min} < T_{amb} < T_{max}			100	
I_{out}	Short circuit sink current	T_{amb} = + 25 °C	30	40		mA
		T_{min} < T_{amb} < T_{max}	25			
	Short circuit source current	T_{amb} = + 25 °C	30	40		
		T_{min} < T_{amb} < T_{max}	25			
I_{CC}	Supply current per channel, output high	T_{amb} = + 25 °C	4.4	7	10	mA
		T_{min} < T_{amb} < T_{max}			11	
	Supply current per channel, output low	T_{amb} = + 25 °C	3.9	6	9	
		T_{min} < T_{amb} < T_{max}			9	
AC performance						
T_{PLH}	Propagation delay (4) (low to high) (3) (5)	f = 1 kHz, C_L = 5 pF, overdrive = 50 mV, T_{amb} = + 25 °C		2.0	3.0	ns
		T_{min} < T_{amb} < T_{max}			4.0	
T_{PHL}	Propagation delay (6) (high to low) (3) (5)	f = 1 kHz, C_L = 5 pF, overdrive = 50 mV, T_{amb} = + 25 °C		2.0	3.0	
		T_{min} < T_{amb} < T_{max}			4.0	
T_R	Rise time (10% to 90%)	10% to 90%		0.70		ns
T_F	Fall time (90% to 10%)	90% to 10%		0.70		
t_{JITTER}	RMS Jitter	V_{IN} = 100 mVpp, f_{IN} = 100 MHz, Jitter BW = 10 Hz to 50 MHz		8		ps

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{SKEW}	Channel-to-channel propagation delay skew	V_{IN} = 100 mVpp, f_{IN} = 100 MHz max. between Δt_{PHL} or Δt_{PLH}		35		ps
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mVpp sine wave, when output reaches 10% or 90% of V_{CC-} to V_{CC+}		375		MHz
Pulse width	Minimum input pulse width	$V_{overdrive}$ = 50 mV, PW_{out} = 90% of PW_{IN}		1.25		ns

1. *The offset is defined as the average value of positive and negative trip points (input voltage differences requested to change the output state in each direction).*
2. *The hysteresis is a built-in feature. It is defined as the voltage difference between the trip points.*
3. *Guaranteed by design.*
4. *T_{PLH} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting input voltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} - 100 mV to V_{ICM} + overdrive*
5. *Ensured by characterization.*
6. *T_{PHL} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting input voltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} + 100 mV to V_{ICM} - overdrive*

Table 5. Electrical characteristics, V_{CC} = 3.3 V, V_{icm} = V_{CC-} + 300 mV, C_L = 5 pF, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage (1)	T_{amb} = + 25 °C	-7		+7	mV
		$T_{min} < T_{amb} < T_{max}$	-9		9	
$\lvert\Delta V_{IO}/\Delta T\rvert$	Input offset voltage drift			3		µV/°C
V_{HYST}	Input hysteresis voltage (2)	T_{amb} = + 25 °C	2	6	15	mV
		$T_{min} < T_{amb} < T_{max}$	1.5		20	
$\lvert I_{IB}\rvert$	Input bias current (3)	T_{amb} = + 25 °C		5	50	pA
		$T_{min} < T_{amb} < T_{max}$			200	
$\lvert I_{IO}\rvert$	Input offset current (3)	T_{amb} = + 25 °C		1	25	
		$T_{min} < T_{amb} < T_{max}$			100	
C_{IN}	Input capacitance (3)			1		pF
CMRR	Common mode rejection ration	$V_{CC-} \le V_{icm} \le V_{CC+}$		68		dB
V_{OL}	Low level output voltage from V_{CC-}	I_{sink} = 1 mA, T_{amb} = + 25 °C		45	80	mV
		$T_{min} < T_{amb} < T_{max}$			100	
V_{OH}	High level output voltage from V_{CC+}	I_{source} = 1 mA, T_{amb} = + 25 °C		60	80	
		$T_{min} < T_{amb} < T_{max}$			100	
I_{out}	Short circuit sink current	T_{amb} = + 25 °C	18	24		mA
		$T_{min} < T_{amb} < T_{max}$	15			
	Short circuit source current	T_{amb} = + 25 °C	16	21		
		$T_{min} < T_{amb} < T_{max}$	13			
I_{CC}	Supply current per channel, output high	T_{amb} = + 25 °C	3.7	7	9.5	mA
		$T_{min} < T_{amb} < T_{max}$			10	
	Supply current per channel, output low	T_{amb} = + 25 °C	3.1	6	8	
		$T_{min} < T_{amb} < T_{max}$			8.5	
AC performance						
T_{PLH}	Propagation delay (4) (low to high) (3) (5)	f = 1 kHz, C_L = 5 pF, overdrive = 50 mV, T_{amb} = + 25 °C		2.0	3.0	ns
		$T_{min} < T_{amb} < T_{max}$			4.0	
T_{PHL}	Propagation delay (6) (high to low) (3) (5)	f = 1 kHz, C_L = 5 pF, overdrive = 50 mV, T_{amb} = + 25 °C		2.0	3.0	
		$T_{min} < T_{amb} < T_{max}$			4.0	
T_R	Rise time (10% to 90%)	10% to 90%		0.70		ns
T_F	Fall time (90% to 10%)	90% to 10%		0.70		
t_{JITTER}	RMS Jitter	V_{IN} = 100 mVpp, f_{IN} = 100 MHz, Jitter BW = 10 Hz to 50 MHz		8		ps
t_{SKEW}	Channel-to-channel propagation delay skew	V_{IN} = 100 mVpp, f_{IN} = 100 MHz max. between Δt_{PHL} or Δt_{PLH}		35		ps
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mVpp sine wave, when output reaches 10% or 90% of V_{CC-} to V_{CC+}		350		MHz

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Pulse width	Minimum input pulse width	$V_{overdrive}$ = 50 mV, PW_{out} = 90% of PW_{IN}		1.25		ns

1. *The offset is defined as the average value of positive and negative trip points (input voltage differences requested to change the output state in each direction).*
2. *The hysteresis is a built-in feature. It is defined as the voltage difference between the trip points.*
3. *Guaranteed by design.*
4. *T_{PLH} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting input voltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} - 100 mV to V_{ICM} + overdrive*
5. *Ensured by characterization.*
6. *T_{PHL} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting input voltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} + 100 mV to V_{ICM} - overdrive*

Table 6. Electrical characteristics, V_{CC} = 2.5 V, V_{icm} = V_{CC-} + 300 mV, C_L = 5 pF, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{IO}	Input offset voltage (1)	T_{amb} = + 25 °C	-7		+7	mV
		$T_{min} < T_{amb} < T_{max}$	-9		9	
$\lvert\Delta V_{IO}/\Delta T\rvert$	Input offset voltage drift			3		µV/°C
V_{HYST}	Input hysteresis voltage (2)	T_{amb} = + 25 °C	2	6	15	mV
		$T_{min} < T_{amb} < T_{max}$	1.5		20	
$\lvert I_{IB}\rvert$	Input bias current (3)	T_{amb} = + 25 °C		5	50	pA
		$T_{min} < T_{amb} < T_{max}$			200	
$\lvert I_{IO}\rvert$	Input offset current (3)	T_{amb} = + 25 °C		1	25	
		$T_{min} < T_{amb} < T_{max}$			100	
C_{IN}	Input capacitance (3)			1		pF
CMRR	Common mode rejection ration	$V_{CC-} \le V_{icm} \le V_{CC+}$		66		dB
V_{OL}	Low level output voltage from V_{CC-}	I_{sink} = 1 mA, T_{amb} = + 25 °C		50	95	mV
		$T_{min} < T_{amb} < T_{max}$			115	
V_{OH}	High level output voltage from V_{CC+}	I_{source} = 1 mA, T_{amb} = + 25 °C		80	95	
		$T_{min} < T_{amb} < T_{max}$			115	
I_{out}	Short circuit sink current	T_{amb} = + 25 °C	10	14		mA
		$T_{min} < T_{amb} < T_{max}$	10			
	Short circuit source current	T_{amb} = + 25 °C	9	11		
		$T_{min} < T_{amb} < T_{max}$	8			
I_{CC}	Supply current per channel, output high	T_{amb} = + 25 °C	3.4	6	8	mA
		$T_{min} < T_{amb} < T_{max}$			9	
	Supply current per channel, output low	T_{amb} = + 25 °C	2.9	5	7	
		$T_{min} < T_{amb} < T_{max}$			7.5	
AC performance						
T_{PLH}	Propagation delay (4) (low to high) (3) (5)	f = 1 kHz, C_L = 5 pF, overdrive = 50 mV, T_{amb} = + 25 °C		2.6	3.5	ns
		$T_{min} < T_{amb} < T_{max}$			4.0	
T_{PHL}	Propagation delay (6) (high to low) (3) (5)	f = 1 kHz, C_L = 5 pF, overdrive = 50 mV, T_{amb} = + 25 °C		2.6	3.5	
		$T_{min} < T_{amb} < T_{max}$			4.0	
T_R	Rise time (10% to 90%)	10% to 90%		0.70		ns
T_F	Fall time (90% to 10%)	90% to 10%		0.70		
t_{JITTER}	RMS Jitter	V_{IN} = 100 mVpp, f_{IN} = 100 MHz, Jitter BW = 10 Hz to 50 MHz		8		ps
t_{SKEW}	Channel-to-channel propagation delay skew	V_{IN} = 100 mVpp, f_{IN} = 100 MHz max. between Δt_{PHL} or Δt_{PLH}		35		ps
f_{TOGGLE}	Input toggle frequency	V_{IN} = 200 mVpp sine wave, when output reaches 10% or 90% of V_{CC-} to V_{CC+}		325		MHz

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Pulse width	Minimum input pulse width	$V_{overdrive}$ = 50 mV, PW_{out} = 90% of PW_{IN}		1.25		ns

1. *The offset is defined as the average value of positive and negative trip points (input voltage differences requested to change the output state in each direction).*
2. *The hysteresis is a built-in feature. It is defined as the voltage difference between the trip points.*
3. *Guaranteed by design.*
4. *T_{PLH} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting input voltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} - 100 mV to V_{ICM} + overdrive.*
5. *Ensured by characterization.*
6. *T_{PHL} is measured when the output signal crosses a voltage level at 50% of V_{CC} with the following conditions: inverting input voltage (IN-) = V_{ICM} and non-inverting input voltage (IN+) moving from V_{ICM} + 100 mV to V_{ICM} - overdrive.*

4 Typical performance characteristics

Figure 2. Supply current vs. supply voltage at V_{ICM} = 300 mV, output high

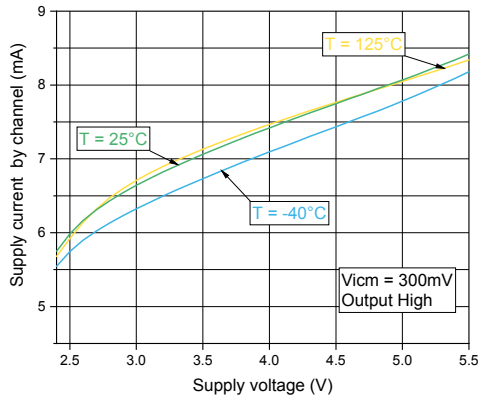


Figure 3. Supply current vs. supply voltage at V_{ICM} = 300 mV, output low

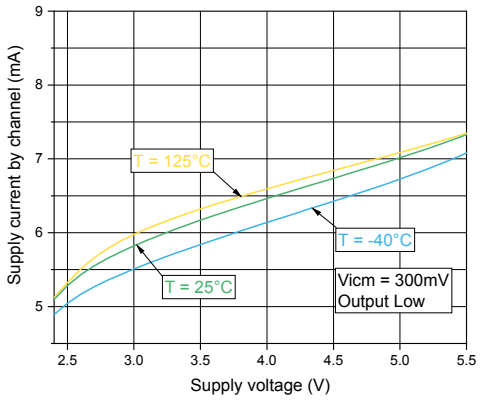


Figure 4. Supply current vs. input common-mode voltage at V_{CC} = 2.5 V, output high

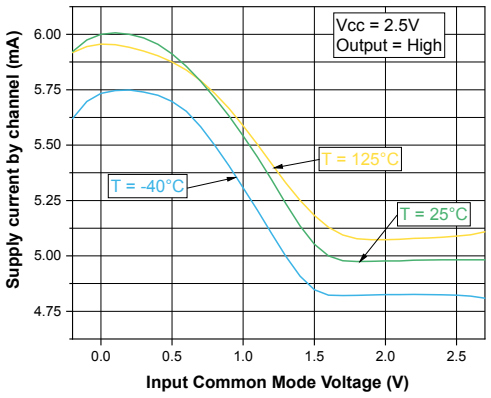


Figure 5. Supply current vs. input common-mode voltage at V_{CC} = 3.3 V, output high

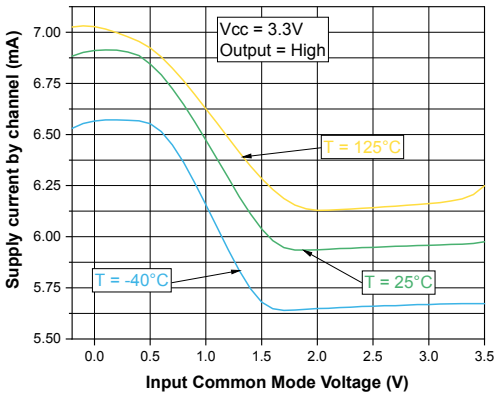


Figure 6. Supply current vs. input common-mode voltage at V_{CC} = 5 V, output high

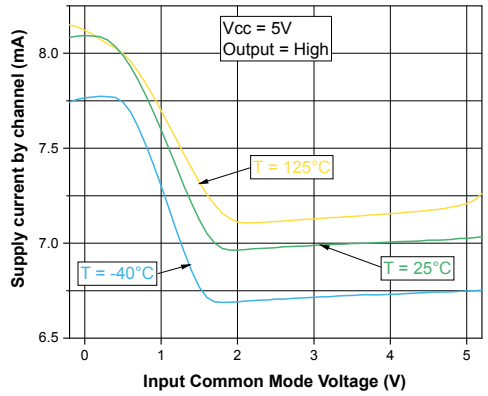


Figure 7. Supply current vs. input common-mode voltage at V_{CC} = 2.5 V, output low

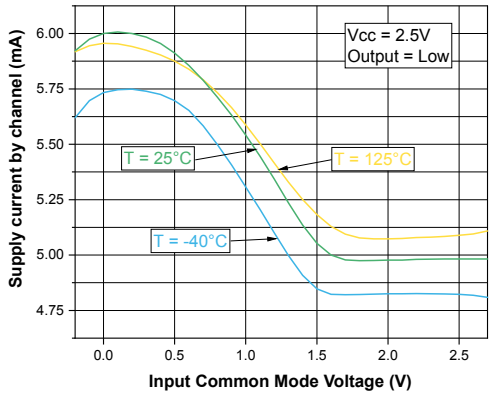


Figure 8. Supply current vs. input common-mode voltage at V_{CC} = 3.3 V, output low

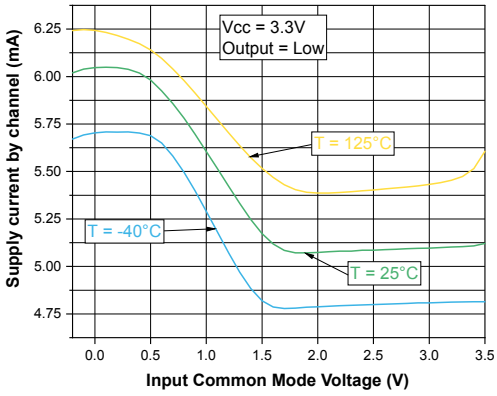


Figure 9. Supply current vs. input common-mode voltage at V_{CC} = 5 V, output low

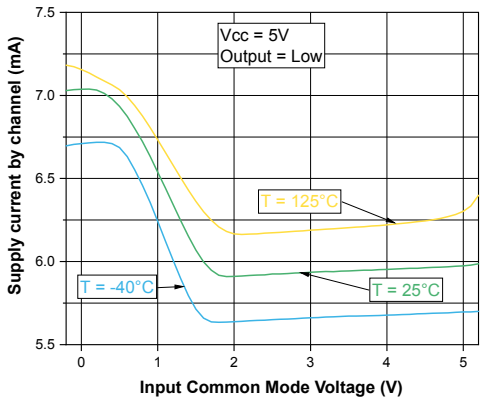


Figure 10. Input offset voltage distribution V_{CC} = 2.5 V

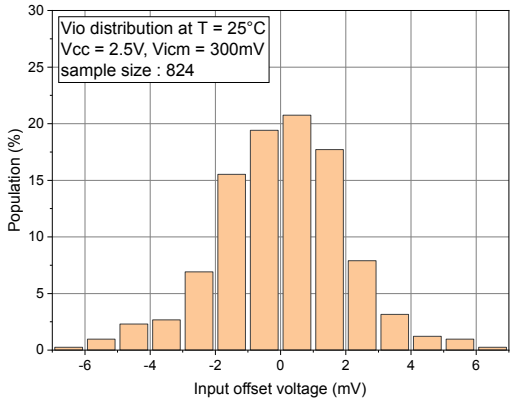


Figure 11. Input offset voltage distribution V_{CC} = 3.3 V

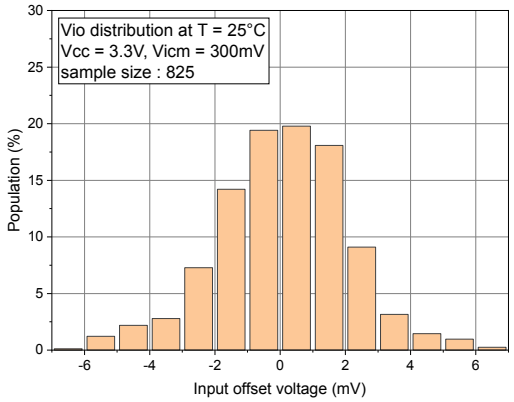


Figure 12. Input offset voltage distribution V_{CC} = 5 V

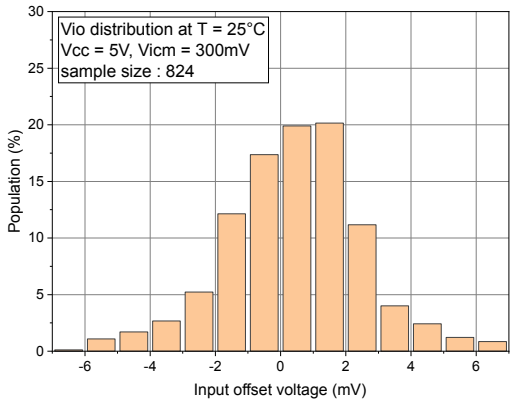


Figure 13. Input offset voltage vs. input common-mode voltage at V_{CC} = 2.5 V

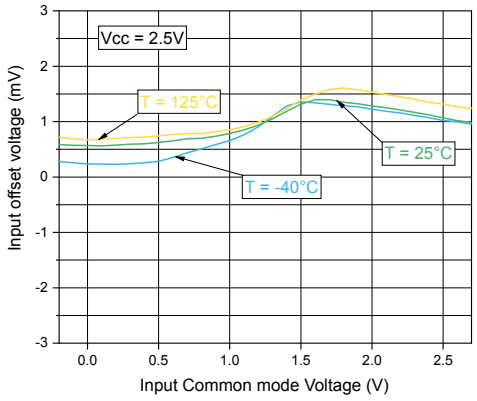


Figure 14. Input offset voltage vs. input common-mode voltage at V_{CC} = 3.3 V

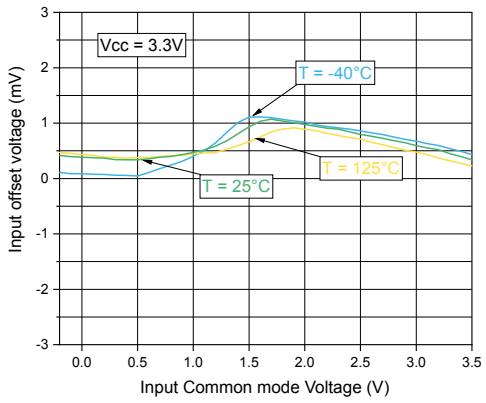


Figure 15. Input offset voltage vs. input common-mode voltage at V_{CC} = 5 V

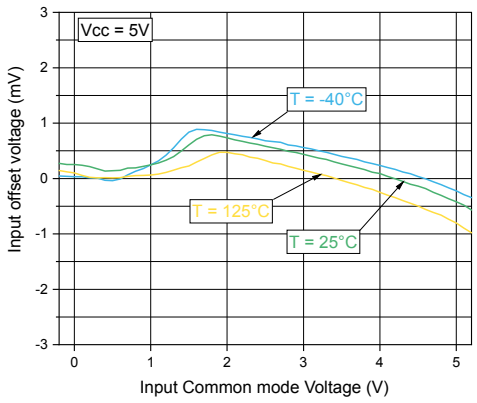


Figure 16. Input offset voltage vs. temperature at V_{CC} = 2.5 V

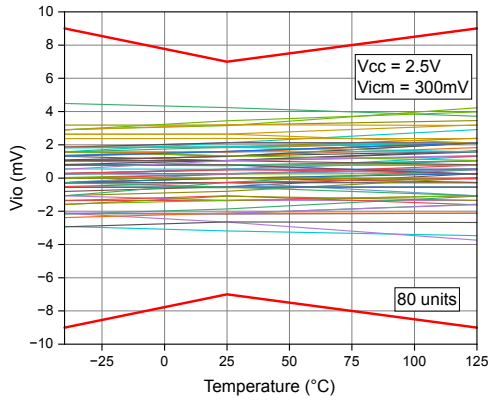


Figure 17. Input offset voltage vs. temperature at V_{CC} = 3.3 V

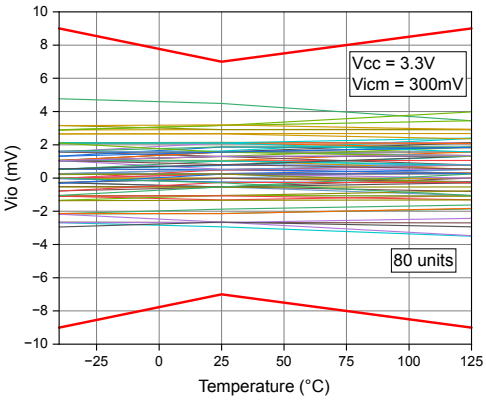


Figure 18. Input offset voltage vs. temperature at V_{CC} = 5 V

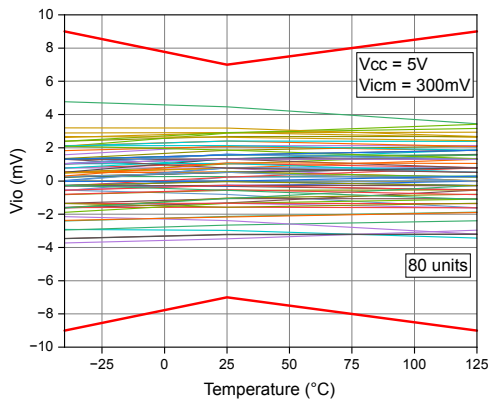


Figure 19. Input bias current vs. input common mode voltage at V_{CC} = 2.5 V

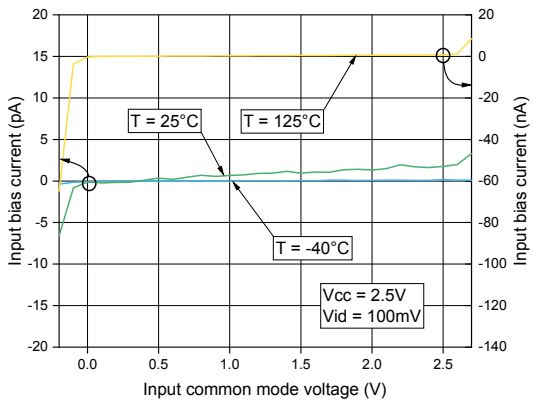


Figure 20. Input bias current vs. input common mode voltage at V_{CC} = 3.3 V

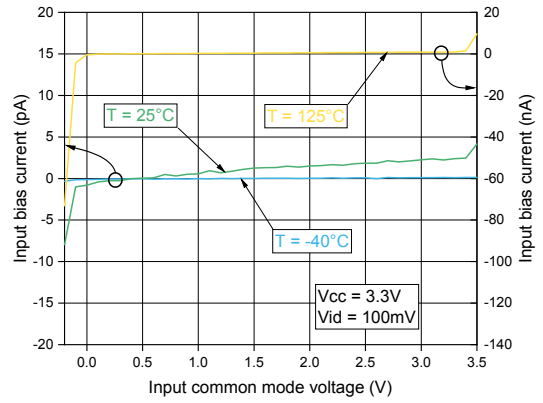


Figure 21. Input bias current vs. input common mode voltage at V_{CC} = 5 V

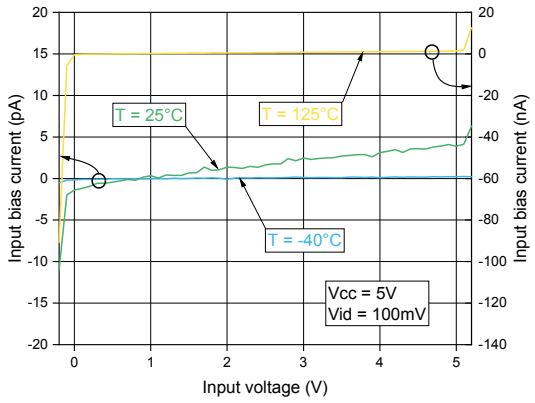


Figure 22. Output drop voltage vs. output sink current at V_{CC} = 2.5 V

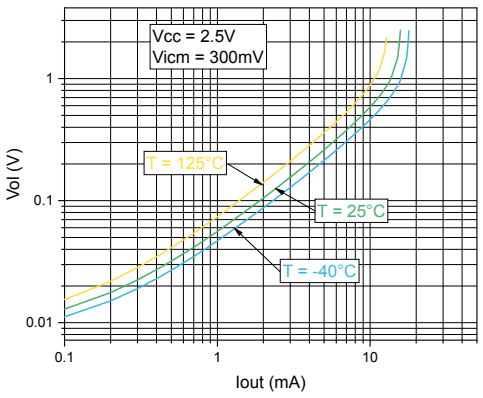


Figure 23. Output drop voltage vs. output sink current at V_{CC} = 3.3 V

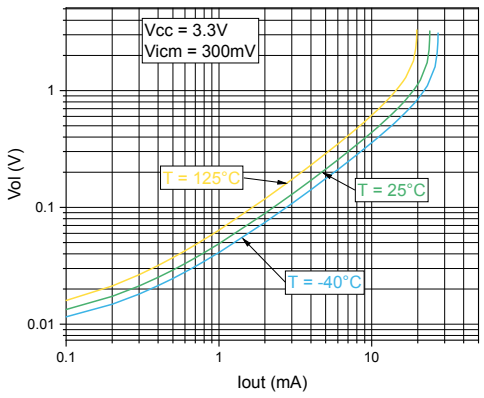


Figure 24. Output drop voltage vs. output sink current at V_{CC} = 5 V

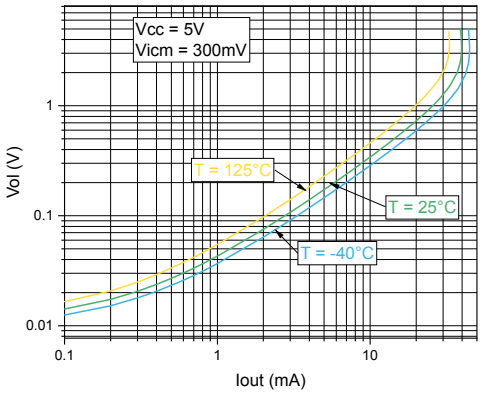


Figure 25. Output drop voltage vs. output source current at V_{CC} = 2.5 V

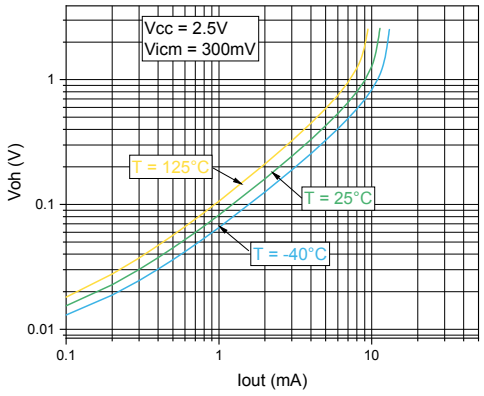


Figure 26. Output drop voltage vs. output source current at V_{CC} = 3.3 V

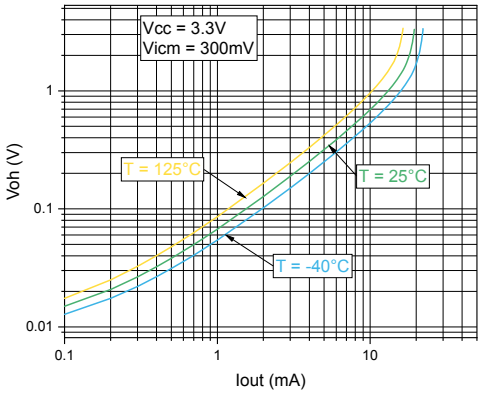


Figure 27. Output drop voltage vs. output source current at V_{CC} = 5 V

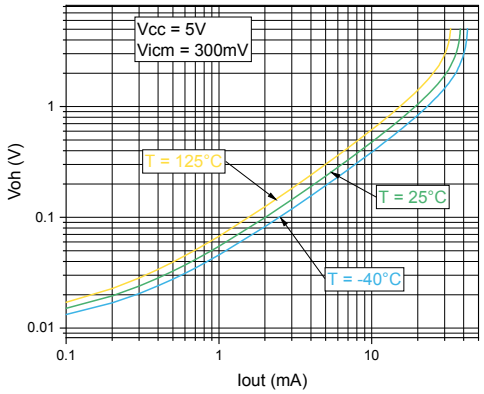


Figure 28. Sinking current vs V_{CC} at V_{ICM} = 300 mV

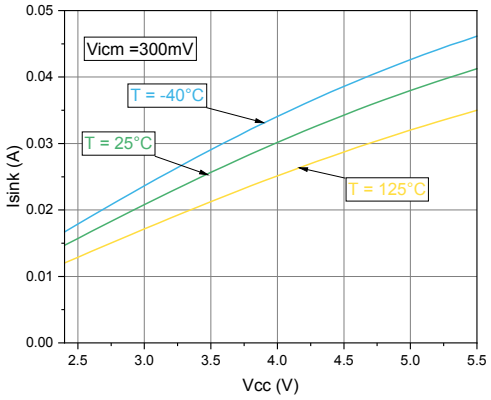


Figure 29. Sourcing current vs V_{CC} at V_{ICM} = 300 mV

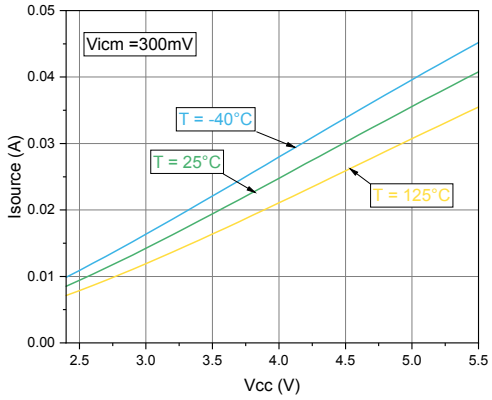


Figure 30. High-to-low propagation delay vs. overdrive at V_{CC} = 2.5 V, V_{ICM} = 300 mV

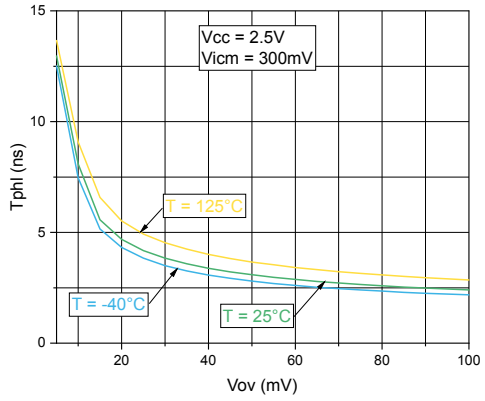


Figure 31. High-to-low propagation delay vs. overdrive at V_{CC} = 3.3 V, V_{ICM} = 300 mV

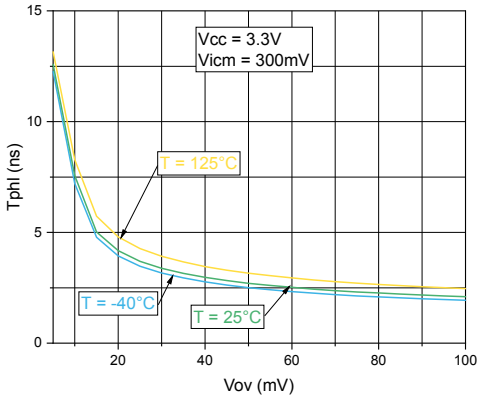


Figure 32. High-to-low propagation delay vs. overdrive at V_{CC} = 5 V, V_{ICM} = 300 mV

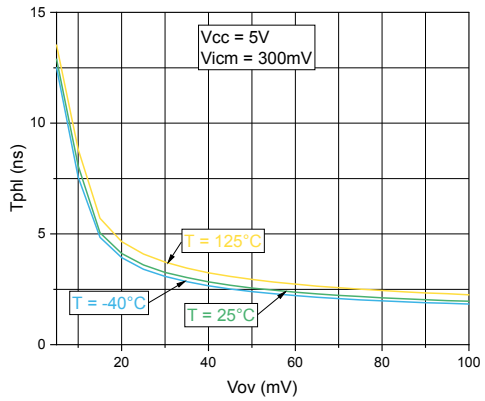


Figure 33. Low-to-high propagation delay vs. overdrive at V_{CC} = 2.5 V, V_{ICM} = 300 mV

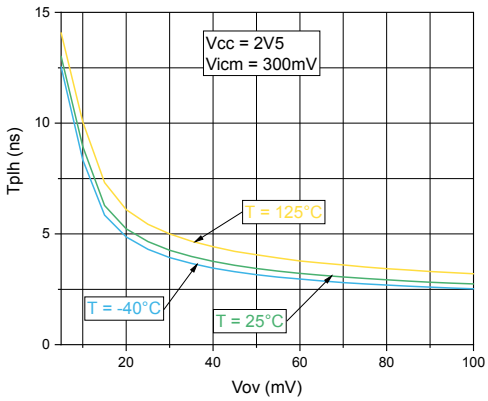


Figure 34. Low-to-high propagation delay vs. overdrive at V_{CC} = 3.3 V, V_{ICM} = 300 mV

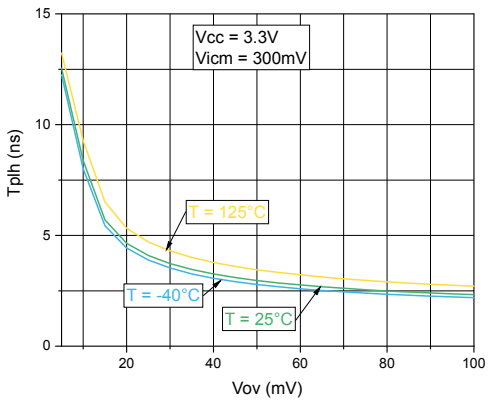


Figure 35. Low-to-high propagation delay vs. overdrive at V_{CC} = 5 V, V_{ICM} = 300 mV

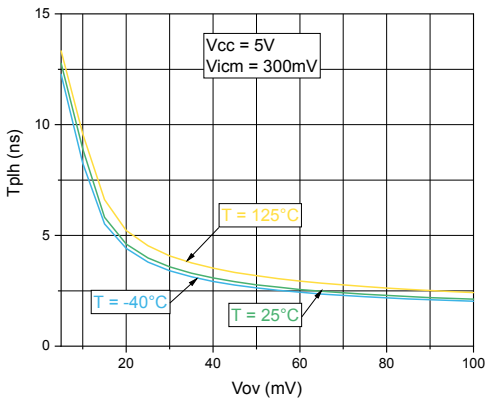


Figure 36. High-to-low propagation delay vs. input common-mode voltage at V_{CC} = 2.5 V

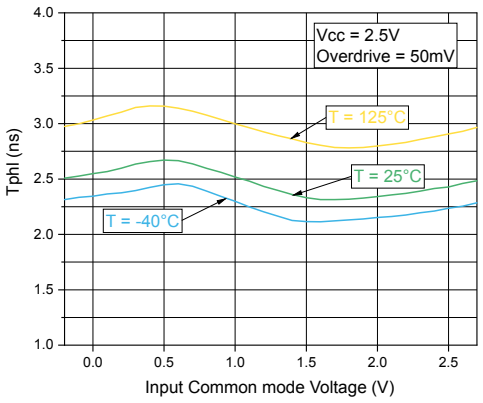


Figure 37. High-to-low propagation delay vs. input common-mode voltage at V_{CC} = 3.3 V

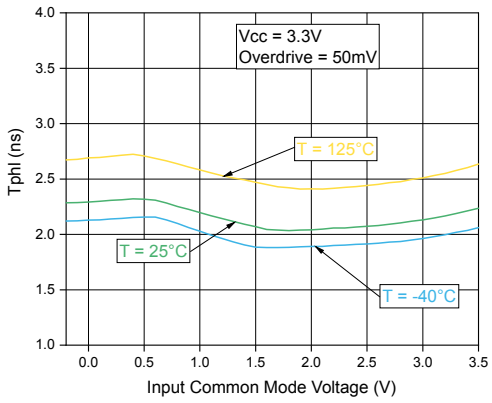


Figure 38. High-to-low propagation delay vs. input common-mode voltage at V_{CC} = 5 V

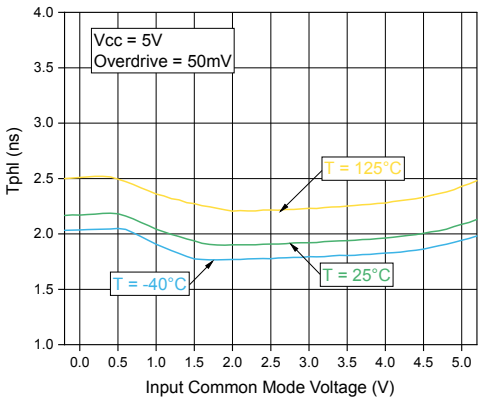


Figure 39. Low-to-high propagation delay vs. input common-mode voltage at V_{CC} = 2.5 V

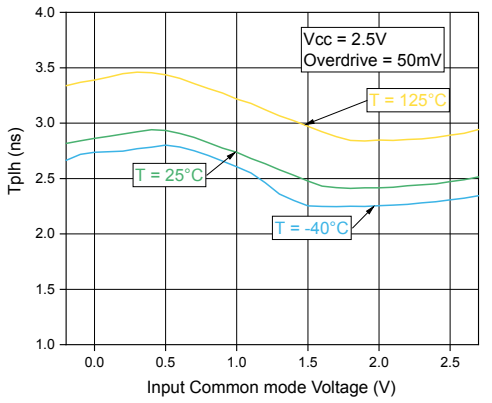


Figure 40. Low-to-high propagation delay vs. input common-mode voltage at V_{CC} = 3.3 V

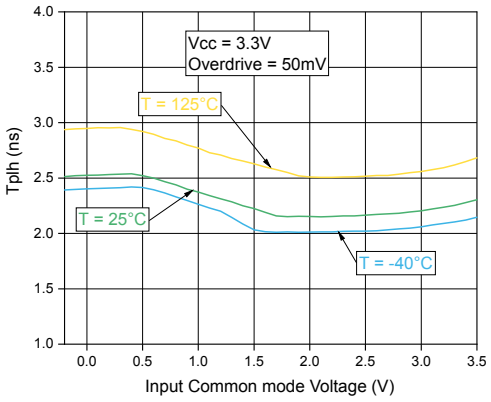


Figure 41. Low-to-high propagation delay vs. input common-mode voltage at V_{CC} = 5 V

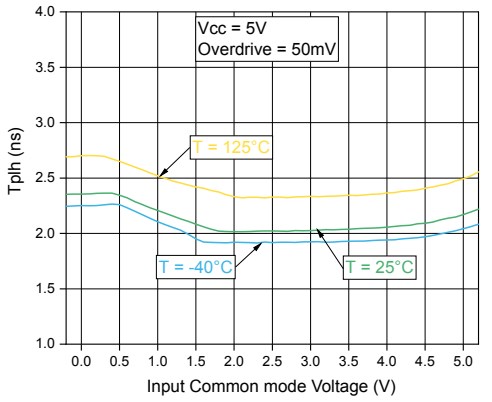


Figure 42. High-to-low propagation delay vs. temperature

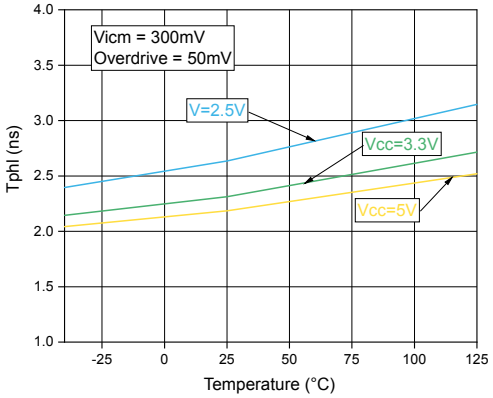


Figure 43. Low-to-high propagation delay vs. temperature

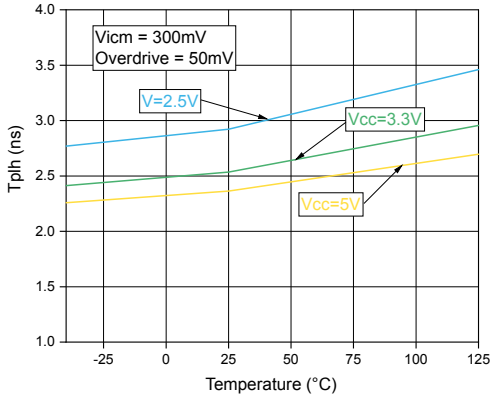


Figure 44. Hysteresis vs V_{ICM} for V_{CC} = 2.5 V

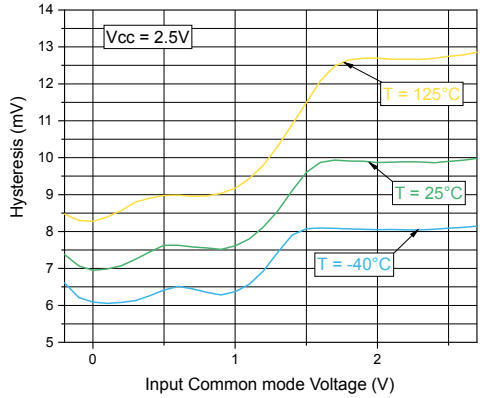


Figure 45. Hysteresis vs V_{ICM} for V_{CC} = 3.3 V

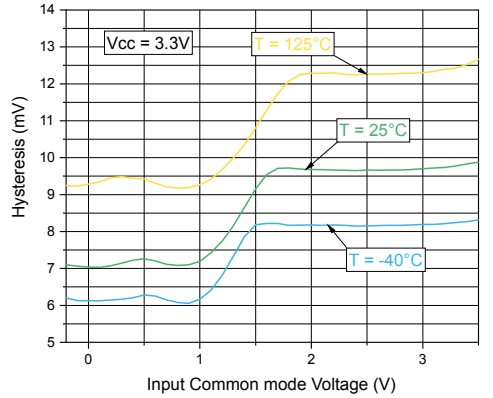


Figure 46. Hysteresis vs V_{ICM} for V_{CC} = 5 V

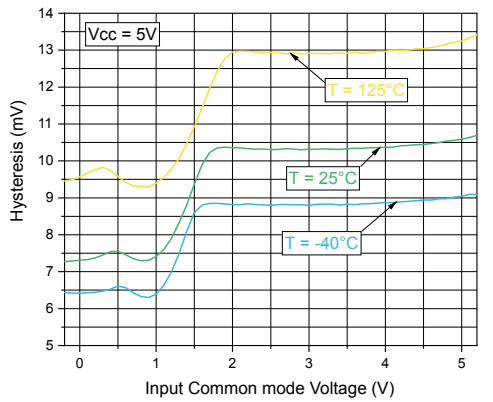


Figure 47. Hysteresis voltage vs. supply voltage

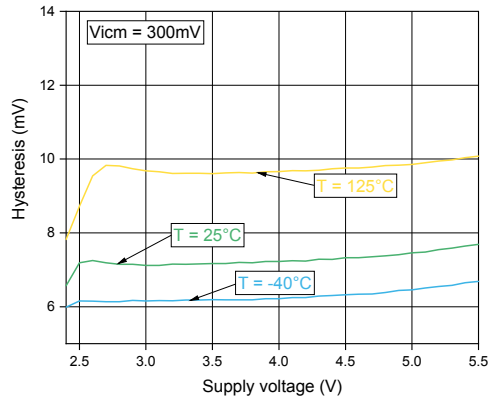
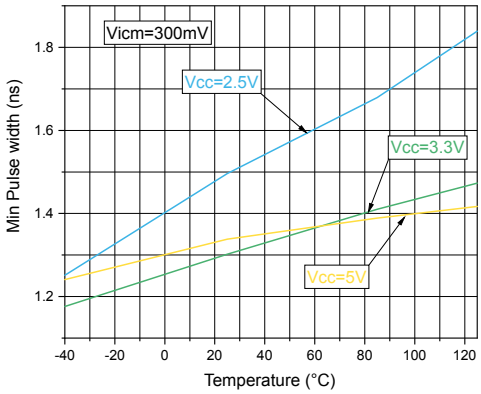


Figure 48. **Minimum pulse width vs. temperature**



5 Application information

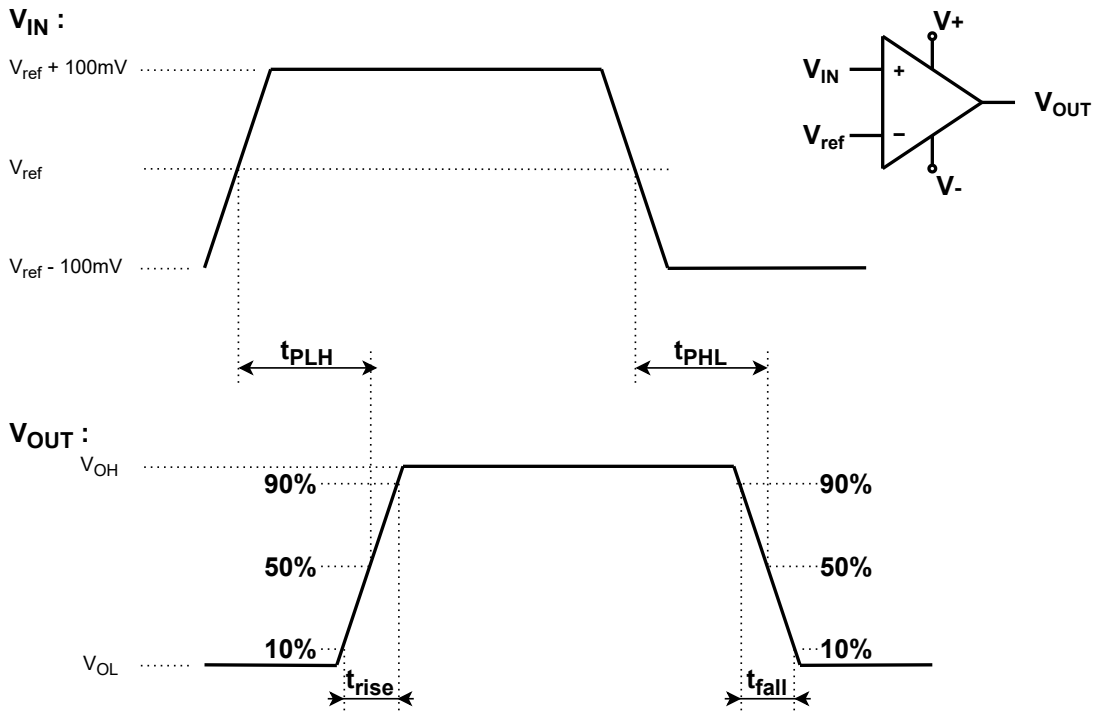
Operating voltages

The TS3002 can operate from 2.4 V to 5.5 V and parameters are fully specified at 2.5 V, 3.3 V, and 5 V. The specifications are guaranteed in the extended temperature range of -40 to +125 °C.

Propagation delay

There is a delay between when the input crosses the reference voltage and the output responds. This is called the propagation delay. Propagation delay can be different between high-to-low and low-to-high input transitions. This is shown as t_{PLH} and t_{PHL} in the figure below and is measured from the mid-point of the input to the midpoint of the output.

Figure 49. Propagation delay



PCB layout recommendations

Particular attention must be paid to the layout of the PCB tracks connected to the comparator, load, and power supply. The power and ground traces are critical as they must provide adequate energy and grounding for all circuits. The best practice is to use short and wide PCB traces to minimize voltage drops and parasitic inductance. In addition to minimizing parasitic impedance over the entire surface, a multi-via technique that connects the bottom and top layer ground planes together in many locations is often used. The copper traces that connect the output pins to the load and supply pins should be as wide as possible to minimize trace impedance.

Decoupling capacitor

The device's high-speed operation can produce rapid changes in supply current. Inductance in the supply and return paths can then cause transient voltage variations or ringing at the supply pins, potentially affecting signal integrity, timing, or stable operation. Effective local decoupling helps provide a low-impedance path for these high-frequency current transients and reduces the coupling of supply noise.

During product characterization, a parallel combination of **1 nF, 100 pF, and 10 pF** capacitors was used. For best results, place these capacitors as close as possible to the device supply pins, using short, low-inductance connections to the appropriate ground or supply return. Keep the capacitor-to-pin and capacitor-to-ground loops small. The effectiveness of the decoupling also depends on the PCB layout and the capacitors' parasitic characteristics; therefore, verify supply integrity and device performance in the final application.

6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 MiniSO8 package information

Figure 50. **MiniSO8 package outline**

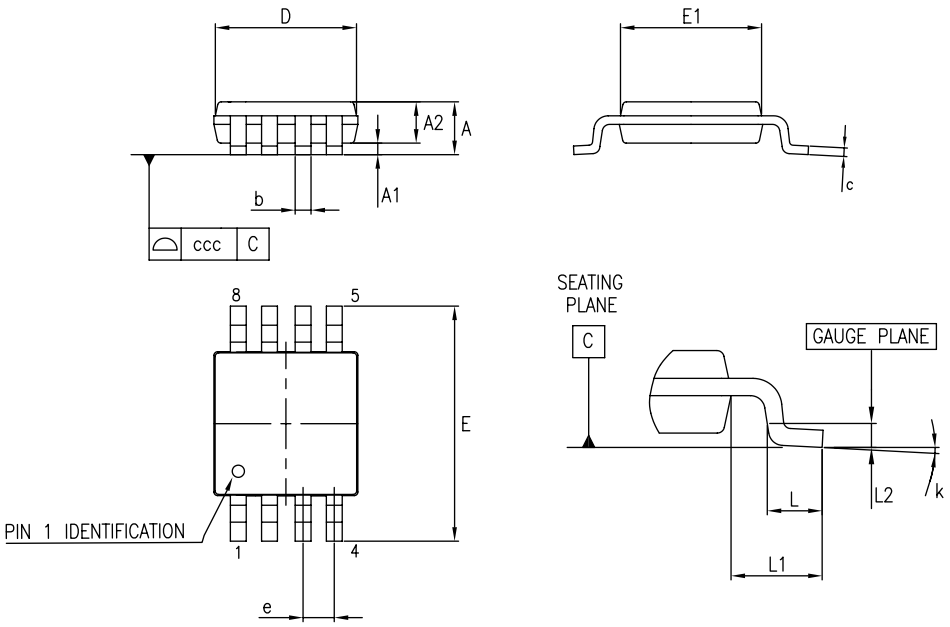


Table 7. **MiniSO8 mechanical data**

Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0		0.15	0		0.006
A2	0.75	0.85	0.95	0.03	0.033	0.037
b	0.22		0.4	0.009		0.016
c	0.08		0.23	0.003		0.009
D	2.8	3	3.2	0.11	0.118	0.126
E	4.65	4.9	5.15	0.183	0.193	0.203
E1	2.8	3	3.1	0.11	0.118	0.122
e		0.65			0.026	
L	0.4	0.6	0.8	0.016	0.024	0.031
L1		0.95			0.037	
L2		0.25			0.01	
k	0°		8°	0°		8°
ccc			0.1			0.004

6.2 DFN8 2 x 2 wettable flank package information

Figure 51. **DFN8 2 x 2 wettable flank package outline**

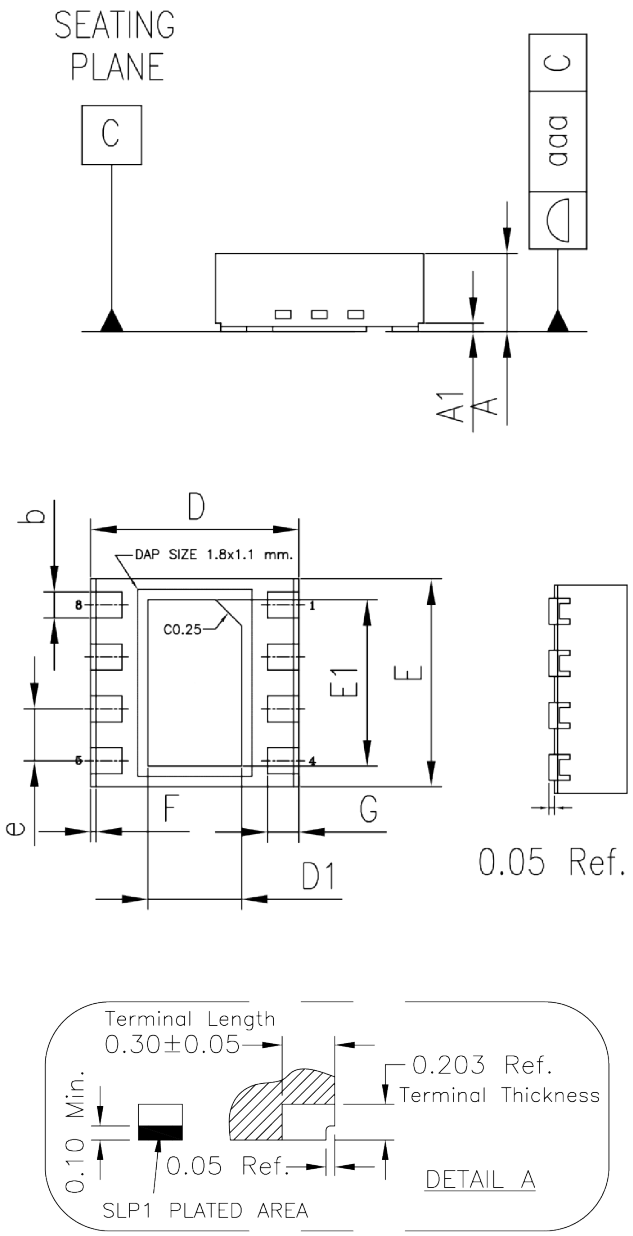
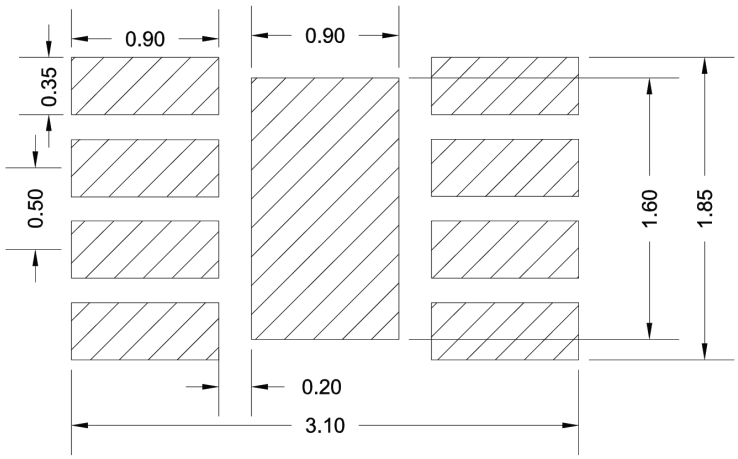


Table 8. **DFN8 2 x 2 wettable flank package mechanical data**

Ref.	Dimensions					
	Millimiters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.10			0.004		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.95	2.00	2.05	0.077	0.079	0.081
D1	0.80	0.90	1.00	0.031	0.035	0.039
E	1.95	2.00	2.05	0.077	0.079	0.081
E1	1.50	1.60	1.70	0.059	0.063	0.067
e		0.50			0.020	
F		0.05			0.002	
G	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.10			0.004	

Figure 52. **DFN8 2 x 2 wettable flank recommended footprint**



7 Ordering information

Table 9. Order code

Order code	Temp. range	Package	Packing	Marking
TS3002IST	-40 °C to 125 °C	Tape and reel	MiniSO8	K5C
TS3002IYST (1)				K5O
TS3002IQ3T			DFN8 2x2 wettable flanks	K5C
TS3002IYQ3T (1)				K5O

1. *Qualification and characterization according to AEC Q100 and Q003 or the equivalent, advanced screening according to AEC Q001 & Q002 or the equivalent. For qualification status details, check the "Maturity Status" link on the first page ("Quality & Reliability" tab on www.st.com).*

Revision history

Table 10. **Document revision history**

Date	Version	Changes
04-Nov-2026	1	Initial release.

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