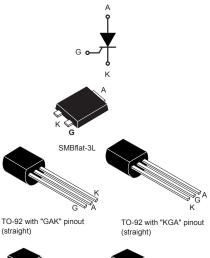
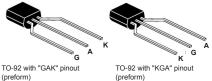


High surge voltage 1.25 A SCR for circuit breaker



TO	0-92 with "KGA" pinout	
(s	traight)	



Product status	
Custom	

Product summary			
I _{T(RMS)}	1.25 A		
V_{DRM} / V_{RRM}	800 V		
V _{DSM} / V _{RSM}	1250 V, 900 V		
I _{GT} standard	100 μΑ		
Tj	125 °C		

Features

- On-state rms current, I_{T(RMS)} 1.25 A
- Repetitive peak off-state voltage, V_{DRM/VRRM}, 800 V
- Non-repetitive direct surge peak off-state voltage, 1250 V
- Non-repetitive reverse surge peak off-state voltage, 900 V
- Triggering gate current, I_{GT (Q1)} 100 µA
- High off-state immunity: 200 V/µs
- ECOPACK2 compliant component

Applications

- GFCI (ground fault circuit interrupters)
- AFCI (arc fault circuit interrupters)
- RCD (residual current device)
- RCBO (residual current circuit breaker with overload protection)
- AFDD (arc fault detection device)

Description

Thanks to highly sensitive triggering levels, the TS110-8S series is suitable for circuit breaker applications where the available gate current is limited.

The 1250 V direct surge voltage capability of the TS110-8S enables high robustness of the whole circuit breaker. The low leakage current of the TS110-8S reduces power consumption over the entire lifetime of the circuit breaker. The high off-state immunity (200 V/µs) insures the non tripping of the breaker in case of electrical fast transient

The TS110-8S is available in through-hole TO-92 package with GAK and KGA pinout and in SMBflat-3L.



1 Characteristics

Table 1. Absolute ratings (limiting values, T_J = 25 °C unless otherwise specified)

Symbol	Parameters	Parameters					
	DMC on electe current (400 % conduction angle)	TO-92	T _L = 53 °C	4.05	_		
I _{T(RMS)}	RMS on-state current (180 ° conduction angle)	SMBflat-3L	T _{tab} = 109 °C	1.25	Α		
1	Average on state assument (400 ° conduction angle)	TO-92	T _L = 53 °C	0.0	^		
$I_{T(AV)}$	Average on-state current (180 ° conduction angle)	SMBflat-3L	T _{tab} = 109 °C	0.8	Α		
	Non repetitive ourse peak on etete ourset	t _p = 8.3 ms	T _i initial = 25 °C	21			
I _{TSM}	Non repetitive surge peak on-state current	t _p = 10 ms	- 1 _j II III (lai – 25 °C	20	Α		
TISM	1st step: one surge every 5 seconds, 25 surges	tp = 10 ms	T _{amb} = 90 °C	25 times 12 A	_ ^		
	2nd step: one surge every 5 seconds, 25 surges	τρ – 10 ms	Tamb = 90 C	25 times 16 A			
I ² t	$t_p = 10 \text{ ms}$ $t_p = 10 \text{ ms}$ $t_j = 10 \text{ ms}$			2	A ² s		
	Critical rate of rise of on-state current F = 50 Hz		T _i = 125 °C	100			
dl/dt	$I_G = 2 \times I_{GT}$, $t_r \le 100 \text{ ns}$,		A/µs			
	Non repetitive critical current rate of rise at break-ove	Non repetitive critical current rate of rise at break-over, see Figure 2, $V_D > V_{DSM}$					
$V_{ m DRM}, \ V_{ m RRM}$	Repetitive peak off-state AC voltage, R_{GK} = 220 Ω	800	V				
V_{DSM}	Non-repetitive direct surge peak off-state voltage, R_{GK} = 220 Ω	t _p = 10 ms	T _j = 25 °C	1250	V		
V _{RSM}	Non-repetitive reverse surge peak off-state voltage, R_{GK} = 220 Ω t_p = 10 ms t_p = 10 ms		T _j = 25 °C	900	V		
I _{GM}	Peak gate current $t_p = 20 \mu s$ $T_j = 125 °C$		1.2	Α			
P _{G(AV)}	Average gate power dissipation	0.2	W				
T _{stg}	Storage junction temperature range	-40 to +150	°C				
Tj	Operating junction temperature range	Operating junction temperature range -40 to +125 °C					

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Table 2. Electrical characteristics ($T_j = 25$ °C, unless otherwise specified)

Symbol		Parameters				
I _{GT} ⁽¹⁾		T _i = 25 °C	Min.	1		
'GT\''	$V_D = 12 \text{ V}, R_L = 140 \Omega$	1 - 23 0	Max.	100	μA	
V _{GT}		T _j = 125 °C	Max.	0.8	V	
	$V_D = 280 \text{ V}, R_1 = 4 \text{ k}\Omega$	T _j = -25 °C	Max.	160	μA	
I _{GT}	V _D - 200 V, K _L - 4 KΩ	T _j = -40 °C	Max.	290	μA	
V _{GD}	$V_D = V_{DRM}$, $R_L = 33 \text{ k}\Omega$, $R_{GK} = 220 \Omega$	T _j = 125 °C	Min.	0.1	V	
V _{RG}	I _{RG} = 2 mA	T _j = 25 °C	Min.	7.5	V	
I _H ⁽²⁾	I_T = 50 mA, R_{GK} = 220 Ω	T _j = 25 °C	Max.	12	mA	
Ι _L	I_G = 5 mA, R_{GK} = 220 Ω	T _j = 25 °C	Max.	12	mA	
dV/dt ⁽²⁾	$V_D = 67 \% V_{DRM}, R_{GK} = 220 \Omega$	T _j = 125 °C	Min.	200	V/µs	

^{1.} Minimum I_{GT} is guaranteed at 5 % of I_{GT} max.

Table 3. Static electrical characteristics

Symbol	Test conditions			Value	Unit
V _{TM} ⁽¹⁾	$I_{TM} = 2.5 \text{ A}, t_p = 380 \ \mu \text{s}$	Max.	1.6	V	
V _{TO} ⁽¹⁾	Threshold on-state voltage	T _j =125 °C	Max.	0.95	V
R _d	Dynamic resistance $T_j = 12$		Max.	220	mΩ
loou loou	$V_{DRM} = V_{RRM}$, $R_{GK} = 220 \Omega$	T _j =25 °C	Max.	1	μΑ
I_{DRM},I_{RRM} V_{D}	VDRM - VRRM, NGK - 220 12	T _j =125 °C	IVIAX.	100	μΑ

^{1.} For both polarities of A2 referenced to A1

Table 4. Thermal resistance

Symbol	Parameters	Max. value	Unit	
R _{th(j-l)}	Junction to lead (DC)	TO-92	65	
R _{th(j-a)}	Junction to ambient (DC)	TO-92	160	°C/W
r (tn(j-a)	sunction to ambient (DC)	SMBflat-3L	75	C/VV
R _{th(j-c)}	Junction to case ($S^{(1)} = 5 \text{ cm}^2$)	SMBflat-3L	14	

1. Copper surface under tab.

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^{2.} For both polarities of A2 referenced to A1



0.2

0.0

0.0 0.1

1.1 Characteristics (curves)

Figure 1. Maximum average power dissipation versus average on-state current

1.2 P(W)

1.0 $\alpha = 120^{\circ}$ $\alpha = 180^{\circ}$ $\alpha = DC$ 0.8 $\alpha = 30^{\circ}$ $\alpha = 60^{\circ}$ $\alpha = 90^{\circ}$ $\alpha = 90^{\circ}$

Figure 2. Average and DC on-state current versus lead temperature (TO-92) $I_{T(AV)}(A)$ TO-92 α = 30° 60° 90 ° 120° 180° DC 1.0 8.0 0.6 0.4 0.2 T_L(°C) 0.0 0 25 50 75 100 125

Figure 3. Average and DC on-state current versus case temperature (SMBflat-3L)

 $I_{T(AV)}(A)$

0.8 0.9

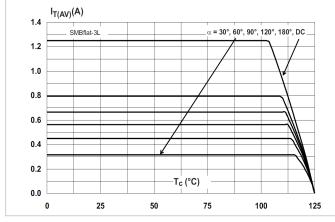


Figure 4. Average and DC on-state current versus ambient temperature

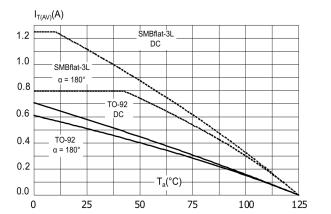


Figure 5. Relative variation of thermal impedance junction to ambient versus pulse duration

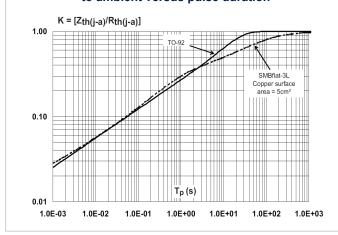
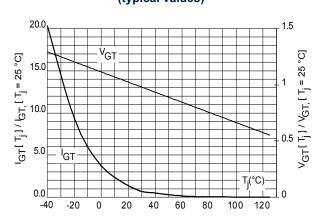


Figure 6. Relative variation of gate trigger current and trigger voltage versus junction temperature (typical values)



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Figure 7. Relative variation of latching and holding current versus junction temperature (typical values)

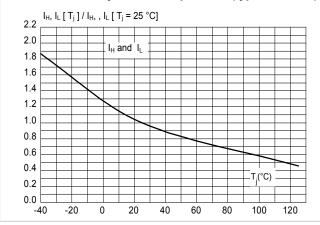


Figure 8. Relative variation of holding current versus gate-cathode resistance (typical values)

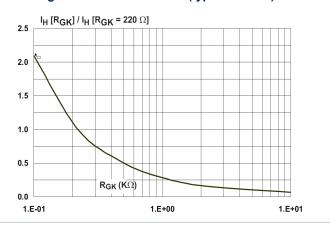


Figure 9. Relative variation of dV/dt immunity versus junction temperature (typical values)

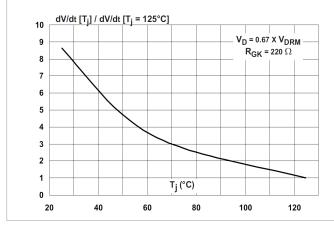


Figure 10. Relative variation of dV/dt immunity versus gate-cathode resistance (typical values)

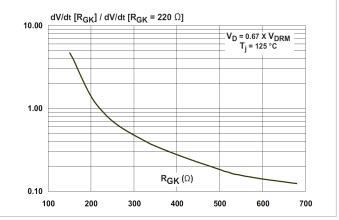


Figure 11. Relative variation of dV/dt immunity versus gate-cathode capacitor (typical values)

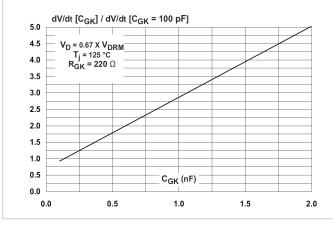
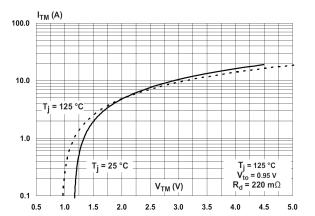
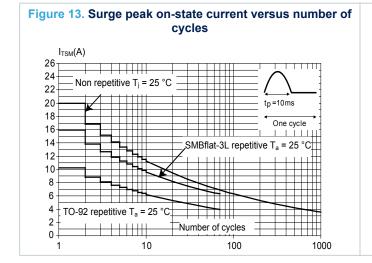


Figure 12. On-state characteristics (maximum values)



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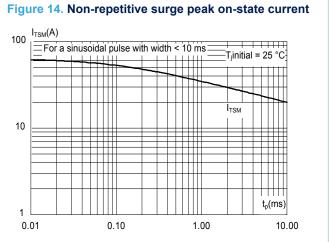
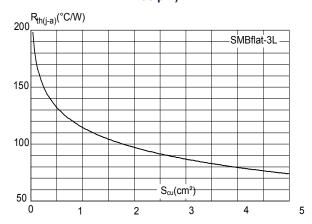


Figure 15. Thermal resistance junction to ambient versus copper surface under anode (epoxy FR4, $Cu_{th} = 35 \mu m$)



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2 AC line transient voltage ruggedness

In comparison with standard SCRs, the TS110-8S is self-protected against over-voltage. The TS110-8S switch can safely withstand AC line surge voltages by switching to the on state (for less than 10 ms on 50 Hz mains) to dissipate energy shocks through the load. The load limits the current through the TS110-8S. The self-protection against over-voltage is based on an overvoltage crowbar technology. This safety feature works even with high turn-on current ramp up.

The Figure 16 represents the TS110-8S in a test environment. It is used to stress the TS110-8S switch according to the IEC 61000-4-5 standard conditions. The TS110-8S folds back safely to the on state as shown in the Figure 17.

The TS110-8S recovers its blocking voltage capability after the surge and the next zero current crossing. Such a non repetitive test can be done at least 10 times.

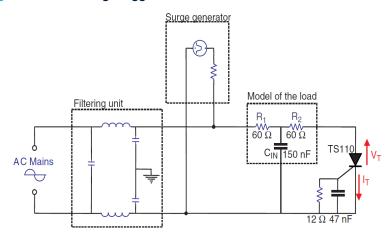
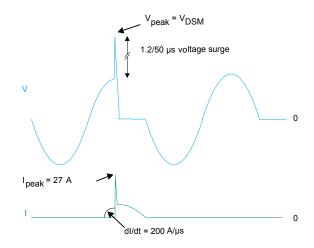


Figure 16. Overvoltage ruggedness test circuit for IEC 61000-4-5 standards

Figure 17. Typical current and voltage waveforms across the TS110-8S during IEC 61000-4-5 standard test



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3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 TO-92 package information

- Lead free plating + halogen-free molding resin
- Epoxy meets UL94, V0

Figure 18. TO-92 package outline

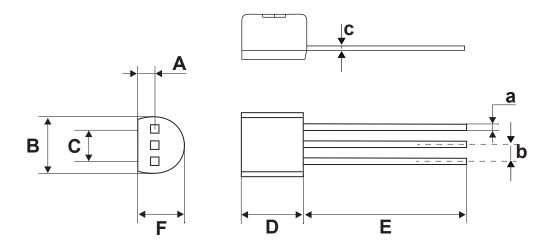


Table 5. TO-92 package mechanical data

				Dimensions		
Ref.		Millimeters			Inches ⁽¹⁾	
	Min.	Тур.	Max.	Min.	Тур.	Max.
Α		1.35			0.0531	
В			4.70			0.1850
С		2.54			0.1000	
D	4.40			0.1732		
E	12.70			0.5000		
F			3.70			0.1457
а			0.50			0.0197
b		1.27			0.0500	
С			0.48			0.0189

^{1.} Inches dimensions given for information

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3.2 TO-92 with leads preform (plastic) package information

- Lead free plating + halogen-free molding resin
- Epoxy meets UL94, V0

Figure 19. TO-92 with leads preform (plastic) package outline

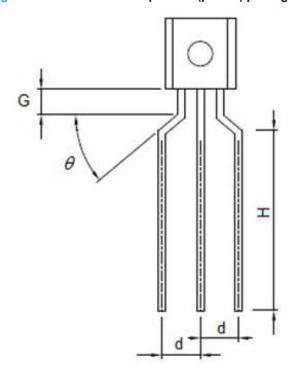


Table 6. TO-92 with leads preform (plastic) package mechanical data

Ref.		Millimeters			Inches ⁽¹⁾	
	Min.	Тур.	Max.	Min.	Тур.	Max.
G	1.30	1.70	2.00	0.051	0.067	0.079
Н	7.69		9.69	0.303		0.381
d	2.40		2.90	0.094		0.114
θ	30°	40°	50°	30°	40°	50°

1. Inches dimensions given for information

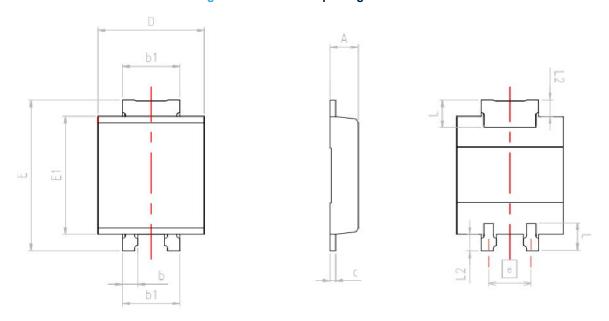
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3.3 SMBflat-3L package information

- Epoxy meets UL94, V0
- Lead-free package

Figure 20. SMBflat-3L package outline



Note: This package drawing may slightly differ from the physical package. However, all the specified dimensions in the following table are guaranteed.

Table 7. SMBflat-3L mechanical data

			Dime	nsions		
Ref.		Millimeters		Inches (dime	nsions are for re	ference only)
	Min.	Тур.	Max.	Min.	Тур.	Max.
А	0.90		1.10	0.0354		0.0433
b	0.35		0.65	0.0138		0.0256
b1	1.95		2.20	0.0768		0.0866
С	0.15		0.40	0.0059		0.0157
D	3.30		3.95	0.1299		0.1555
Е	5.10		5.60	0.2008		0.2205
E1	4.05		4.60	0.1594		0.1811
L	0.75		1.50	0.0295		0.0591
L2		0.60			0.0236	
е		1.60			0.0630	

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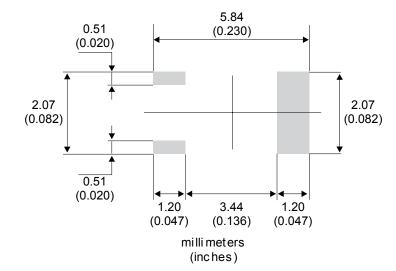


Figure 21. Footprint recommendations, dimensions in mm (inches)

Note: This drawing may not be in scale; however, all the specified dimensions are guaranteed.

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4 Ordering information

Figure 22. Ordering information scheme

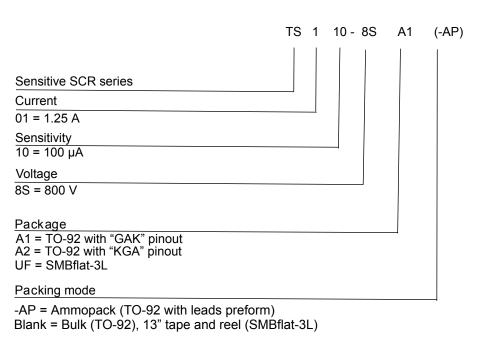


Table 8. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TS110-8SA1	TS110-8S		200 mg	2500	Bulk
TS110-8SA1-AP		TO-92		2000	Ammopack ⁽¹⁾
TS110-8SA2		10-92		2500	Bulk
TS110-8A2-AP				2000	Ammopack ⁽¹⁾
TS110-8SUF		SMBflat-3L	47 mg	5000	Tape and reel 13"

^{1.} With this packing mode the pin are preform unless in bulk mode, see TN1173 which define the TO-92 in Ammopack.

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Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Jul-2023	1	Initial release.
12-Feb-2024	2	Updated Table 2.
10-Jul-2024	3	Updated Cover image, and Table 8 for Ammopack packing. Inserted Section 3.2: TO-92 with leads preform (plastic) package information.
28-May-2025	4	Document classification changed from restricted to public.

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