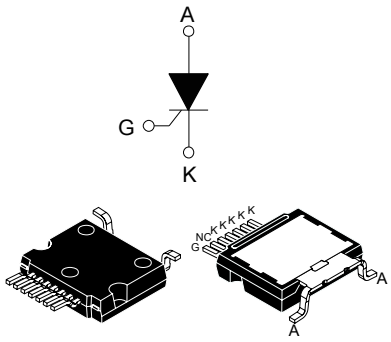
TN4050HP-12L2Y

Datasheet

40 A 1200 V automotive grade thyristor (SCR)



HU³PAK

Features

- AEC-Q101 qualified
- High junction temperature: 150 °C
- AC off state voltage: +/- 1200 V
- Nominal on-state RMS current: 40 A_{RMS}
- High EFT noise immunity: 1000 V/µs
- Max. gate triggering current: 50 mA
- ECOPACK2 compliant component

Application

- On board charger
- Capacitor discharge
- Overvoltage crowbar protection
- Power supplies
- AC switches
- Solid state relays

Product status
TN4050HP-12L2Y

Product summary	
$I_{T(RMS)}$	40 A
V_{DRM}/V_{RRM}	1200 V
V_{DSM}/V_{RSM}	1400 V
I_{GT}	50 mA
T_j	-40 to 150 °C

Description

The TN4050HP-12L2Y is an automotive grade SCR thyristor designed for applications such as automotive on board and stationary battery chargers.

This SCR Thyristor, rated for a 40 A RMS power switching, offers superior performances in peak voltage robustness up to 400 V sine wave pulse. Its key features allow the design of functions such as a 56 A RMS AC switch and a 50 A AC-DC controlled rectifier-bridge.

Available in HU3PAK package, it is ideal for compact SMD designs on surface mount boards or insulated metal substrate boards and and top-side cooling.

1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (180 ° conduction angle)		T_C = 135 °C	40	A
$I_{T(AV)}$	Average on-state current (180 ° conduction angle)			25	
I_{TSM}	Non repetitive surge peak on-state current, V_R = 0 V	t_p = 8.3 ms	T_j initial = 25 °C	440	A
		t_p = 10 ms		400	
I^2t	I^2t value for fusing	t_p = 10 ms	T_j = 25 °C	800	A^2s
dI/dt	Critical rate of rise of on-state current, I_G = 2 x I_{GT} , tr ≤ 100 ns	f = 50 Hz	T_j = 150 °C	200	A/µs
V_{DRM} / V_{RRM}	Repetitive off-state voltage		T_j = 150 °C	1200	V
V_{DSM} / V_{RSM}	Non repetitive surge peak off-state voltage	t_p = 10 ms	T_j = 25 °C	1400	V
V_{GM}	Peak forward gate voltage	t_p = 20 µs	T_j = 150 °C	10	V
I_{GM}	Peak forward gate current	t_p = 20 µs	T_j = 150 °C	8	A
V_{RGM}	Maximum peak reverse gate voltage		T_j = 25 °C	5	V
$P_{G(AV)}$	Average gate power dissipation		T_j = 150 °C	1	W
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature			-40 to +150	°C

Table 2. Electrical characteristics (T_j = 25 °C unless otherwise specified)

Symbol	Test Conditions			Value	Unit
I_{GT}	V_D = 12 V, R_L = 33 Ω		Min.	10	mA
			Max.	50	
V_{GT}			Max.	1.3	V
I_{GD}	V_D = 800 V, R_L = 3.3 Ω	T_j = 150 °C	Min.	3	mA
V_{GD}	V_D = 800 V, R_L = 3.3 Ω	T_j = 150 °C	Min.	0.2	V
I_H	I_T = 500 mA, gate open		Max.	100	mA
I_L	I_G = 1.2 x I_{GT}		Max.	125	mA
dV/dt	V_D = 800 V, gate open	T_j = 150 °C	Min.	1000	V/µs

Table 3. Timing Parameters

Symbol	Test Conditions			Value	Unit
t_{gt}	I_T = 80 A , V_D = 800 V, I_G = 100 mA, dI_G/dt = 0.2 A/µs		Typ.	1	µs
t_q	I_{TM} = 25 A, V_D = 800 V, dI_T/dt = 10 A/µs, V_R = 75 V, dV_D/dt = 20 V/µs, t_p = 100 µs	T_j = 150 °C	Typ.	150	µs

Table 4. Static Characteristics

Symbol	Test Conditions			Value	Unit
V_{TM}	I_{TM} = 80 A, t_P = 380 µs	T_j = 25 °C	Max.	1.55	V
V_{TO}	On-state threshold voltage	T_j = 150 °C	Max.	0.83	V
R_D	On-state dynamic resistance	T_j = 150 °C	Max.	10	mΩ
I_{DRM}/I_{RRM}	$V_D = V_{DRM}$, $V_R = V_{RRM}$	T_j = 25 °C	Max.	5	µA
		T_j = 125 °C		0.9	mA
		T_j = 150 °C		6	mA
I_{DSM}/I_{RSM}	$V_D = V_{DSM}$, $V_R = V_{RSM}$	T_j = 25 °C	Max.	10	µA

Table 5. Thermal parameters

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (DC)	Max.	0.4	°C/W

1.1 Characteristics (curves)

Figure 1. Maximum average power dissipation versus average on-state current

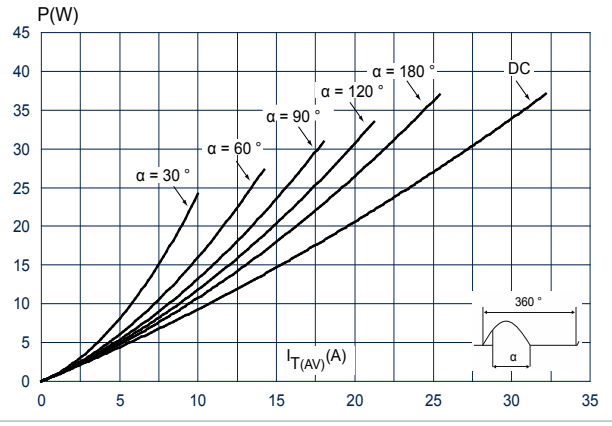


Figure 2. Average and D.C. on-state current versus case temperature

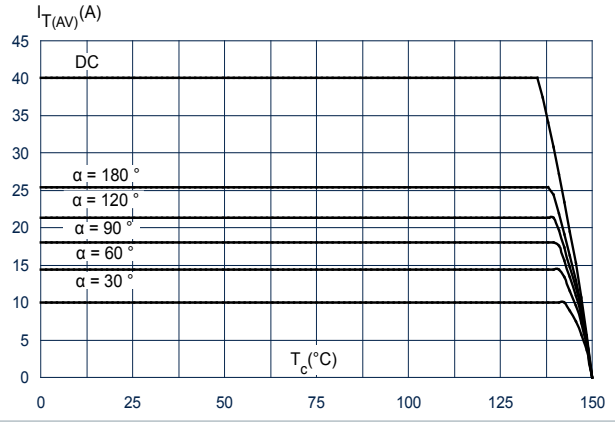


Figure 3. Average and D.C. on-state current versus ambient temperature

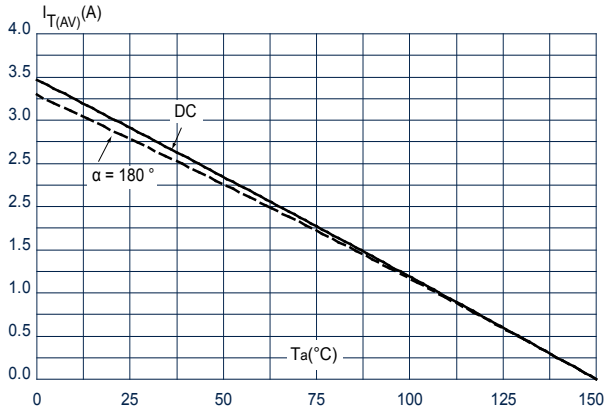


Figure 4. On-state characteristics (maximum values)

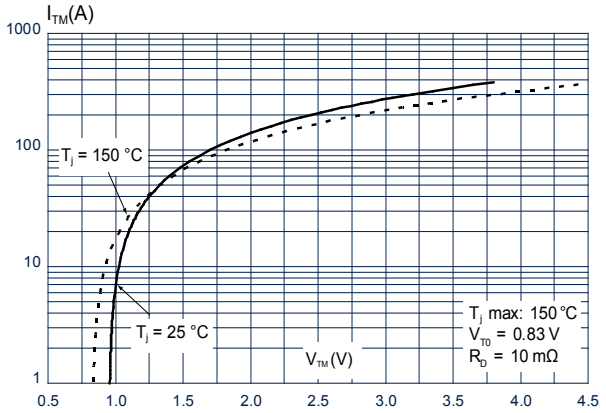


Figure 5. Surge peak on-state current versus number of cycles

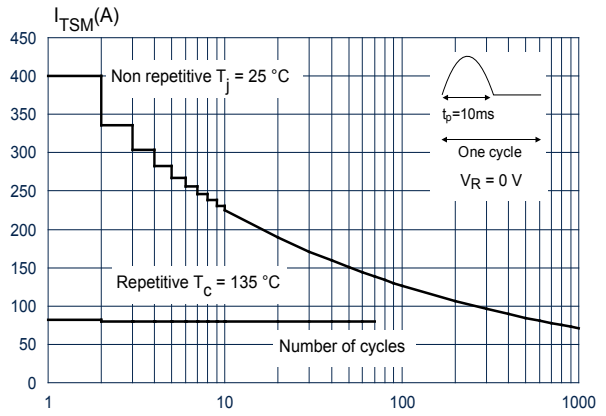


Figure 6. Non repetitive surge peak on-state current for a sinusoidal pulse with width t_p < 10 ms

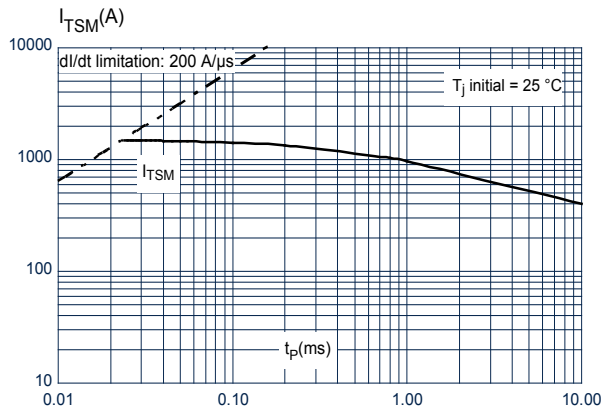


Figure 7. Relative variation of leakage current versus junction temperature for different values of blocking voltage (typical values)

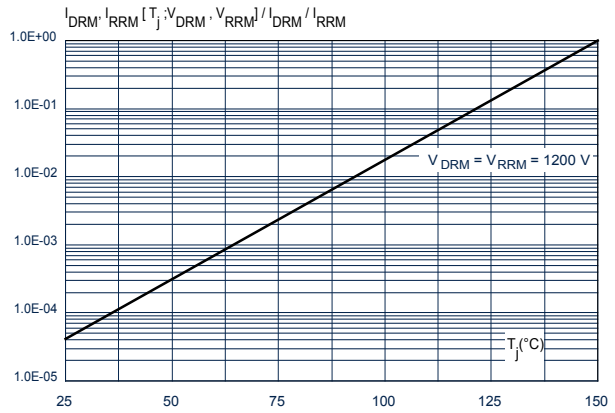


Figure 8. Relative variation of holding and latching current versus junction temperature (typical values)

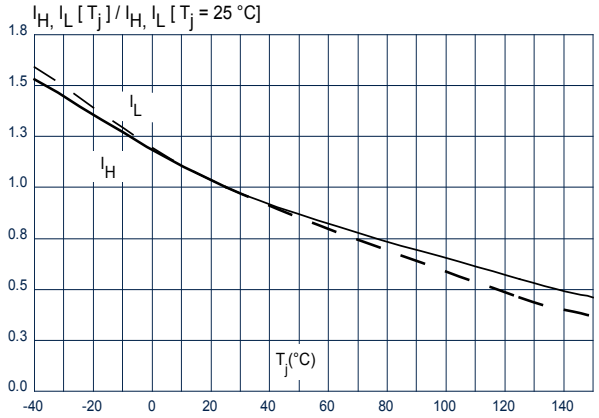


Figure 9. Relative variation of gate trigger current and gate voltage versus junction temperature (typical values)

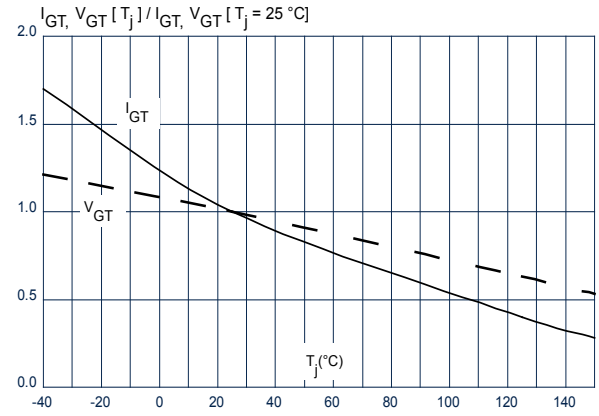


Figure 10. Relative variation of thermal impedance junction to case versus pulse duration

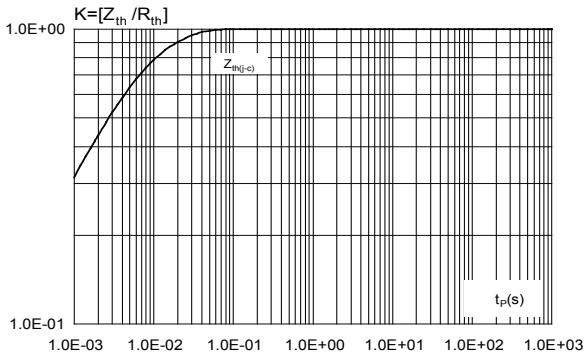
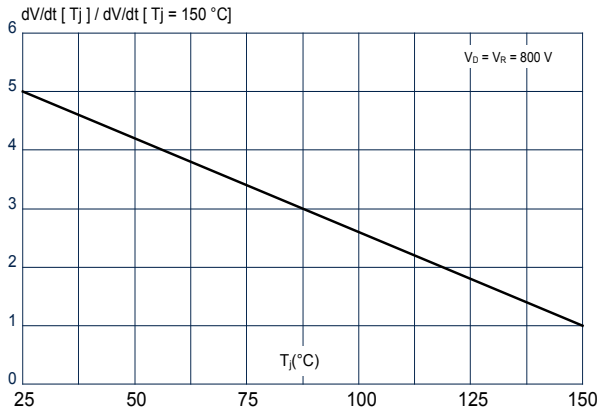


Figure 11. Relative variation of static dV/dt immunity versus junction temperature



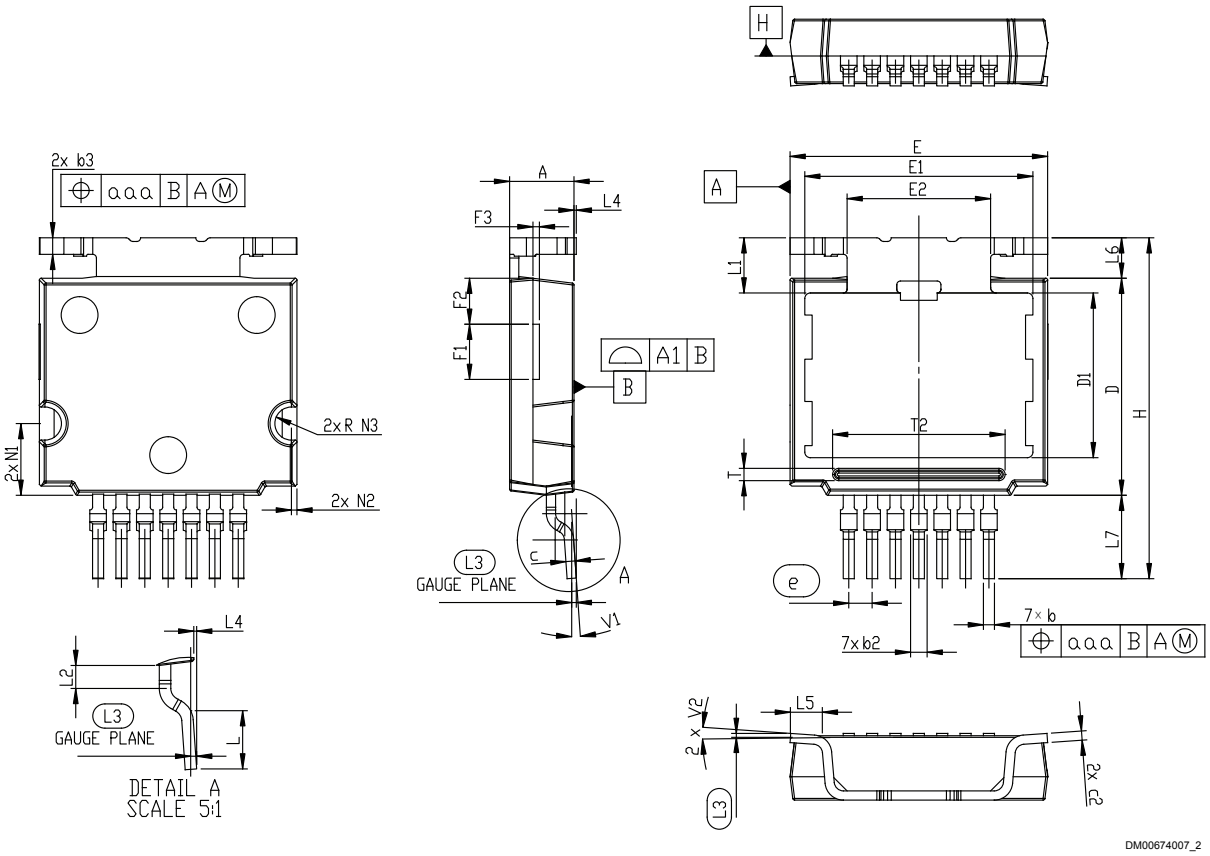
2 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 HU3PAK package information

- Epoxy meets UL94, V0

Figure 12. HU3PAK package outline



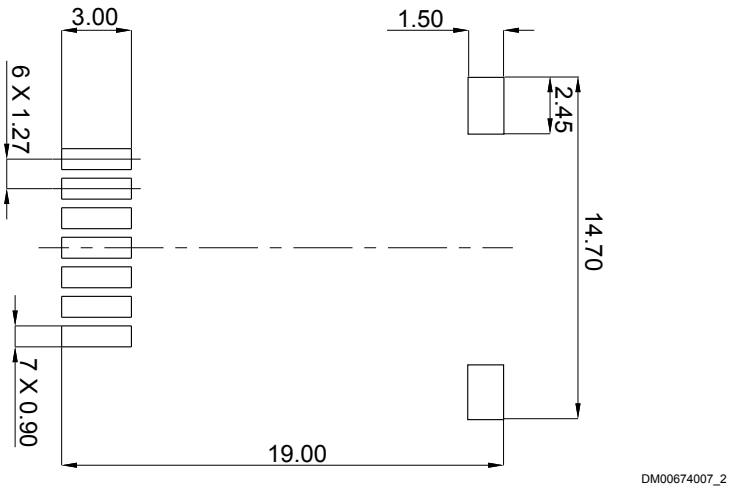
Note: This package drawing may slightly differ from the physical package. However, all the specified dimensions are guaranteed.

Table 6. HU3PAK package mechanical data

Ref.	Dimensions		
	mm		
	Min.	Typ.	Max.
A	3.40	3.50	3.60
A1		0.05	
b	0.50	0.60	0.70
b2	0.50	0.70	1.00
b3	0.80	0.90	1.00
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D	11.70	11.80	11.90
D1	8.80	8.955	9.10
E	13.90	14.00	14.10
E1	12.30	12.40	12.50
E2	7.75	7.80	7.85
e		BSC 1.27	
H	18.00	18.58	19.00
L	2.40	2.52	2.60
L1		3.05	
L2	0.90	1.00	1.10
L3		BSC 0.26	
L4	0.075	0.125	0.175
L5	1.83	1.93	2.03
L6	2.14	2.24	2.34
L7	4.44	4.54	4.64
aaa		0.10	
F1	2.90	3.00	3.10
F2	2.40	2.50	2.60
F3	0.25	0.35	0.45
N1	3.80	3.90	4.00
N2	0.25	0.30	0.45
N3	0.80	0.90	1.00
T	0.50	0.67	0.70
T2	9.18	9.38	9.43
θ1		0°	8°
θ2		0°	8°

1. Package outline exclusive of any mold flashes dimensions.
2. Package outline exclusive of burr dimensions.
3. Max resin gate protrusion: 0.25 mm.
4. The planarity of the package backside 50 micron max.
5. BSC: basic spacing between centers

Figure 13. HU3PAK recommended footprint (dimensions are in mm)



Note: For packing details you can see technical note TN1173: Packing information for IPAD, protection, rectifiers, thyristors and AC Switches.

2.2 HU^{3}PAK packing information

Figure 14. HU^{3}PAK carrier tape outline

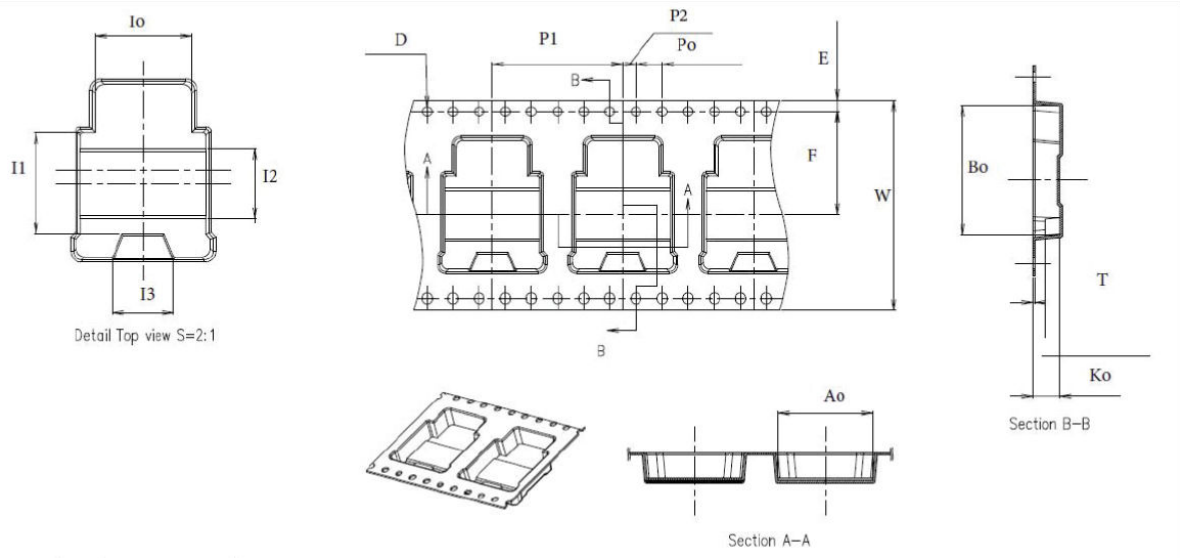


Table 7. HU^{3}PAK tape and reel mechanical data

Tape	
Dim.	mm
	Value
A0	14.40 ±0.1
B0	19.70
D	1.50 ±0.1
E	1.75 ±0.1
F	15.65 ±0.1
I0	11.00
I1	11.60 ±0.1
I2	8.0
I3	7.0
K0	4.20
P0	4.00 ±0.1
P1	20.00 ±0.1
P2	2.00 ±0.1
T	0.40 ±0.5
W	32.00 ±0.3

3 Ordering information

Figure 15. **Ordering information scheme**

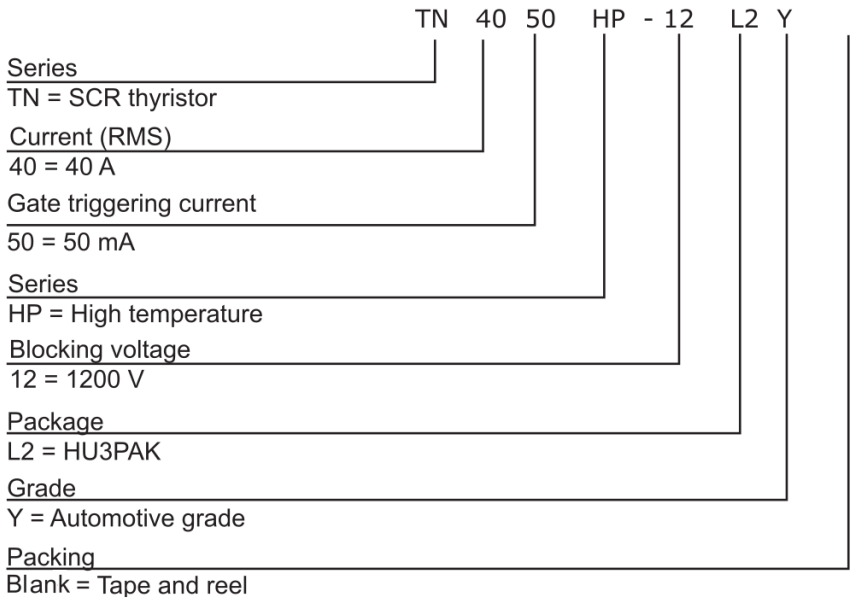


Table 8. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TN4050HP-12L2Y	TN4050HP12Y	HU^{3}PAK	2.32 g	600	Tape and reel 13"

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
08-Dec-2022	1	Initial release.
27-May-2024	2	Updated Table 5. Thermal parameters with $R_{th(j-c)}$ value.
22-Oct-2025	3	Updated Section 3: Ordering information.

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