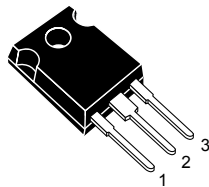
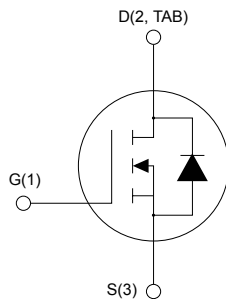


Automotive-grade N-channel 650 V, 24 mΩ typ., 69 A MDmesh M5 Power MOSFET in a TO-247 package


TO-247


AM01475v1_noZen



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW78N65M5	650 V	32 mΩ	69 A

- AEC-Q101 qualified
- Extremely low $R_{DS(on)}$
- High dv/dt capability
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested



Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Product status link

[STW78N65M5](#)

Product summary

Order code	STW78N65M5
Marking	78N65M5
Package	TO-247
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	69	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	41.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	276	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	450	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Maximum operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 69\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} \leq 520\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.28	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	50	$^{\circ}\text{C}/\text{W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	15	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	2000	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	650	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$	-	-	100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 34.5\text{ A}$	-	24	32	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	9000	-	pF
C_{oss}	Output capacitance		-	210	-	
C_{rss}	Reverse transfer capacitance		-	9	-	
$C_{o(tr)}^{(1)}$	Equivalent output capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$	-	768	-	pF
$C_{o(er)}^{(2)}$	Equivalent output capacitance energy related		-	205	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 34.5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 15. Test circuit for gate charge behavior)	-	203	-	nC
Q_{gs}	Gate-source charge		-	50	-	
Q_{gd}	Gate-drain charge		-	84	-	

1. $C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.

2. $C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 40\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	163	-	ns
$t_{r(v)}$	Voltage rise time		-	14	-	
$t_{c(off)}$	Crossing time off	(see the Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	14	-	
$t_{f(i)}$	Current fall time		-	26	-	

Table 7. Source-drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	69	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	276	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 69\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 69\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	504	-	ns
Q_{rr}	Reverse recovery charge		-	13	-	μC
I_{RRM}	Reverse recovery current		-	49	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 69\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	635	-	ns
Q_{rr}	Reverse recovery charge		-	19	-	μC
I_{RRM}	Reverse recovery current		-	59	-	A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

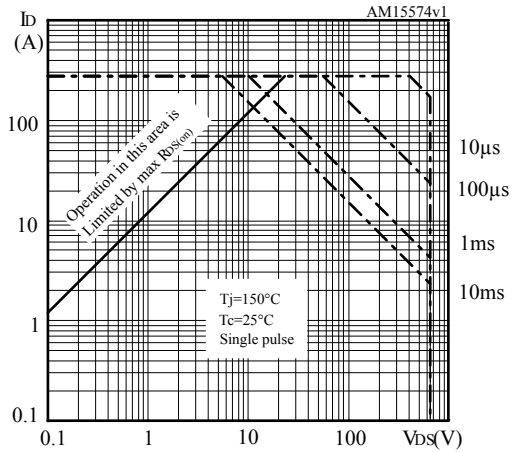
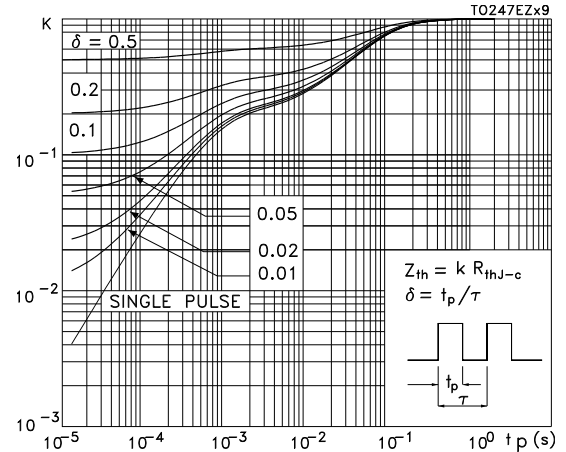
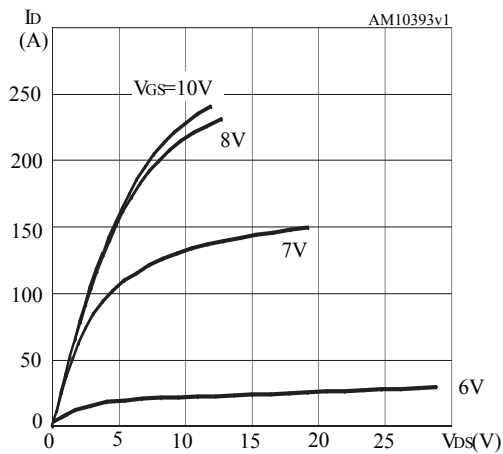
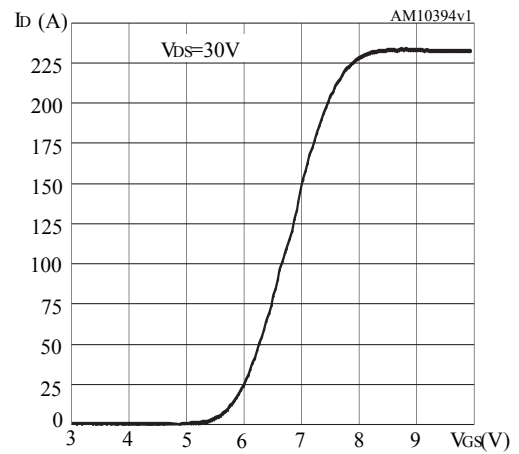
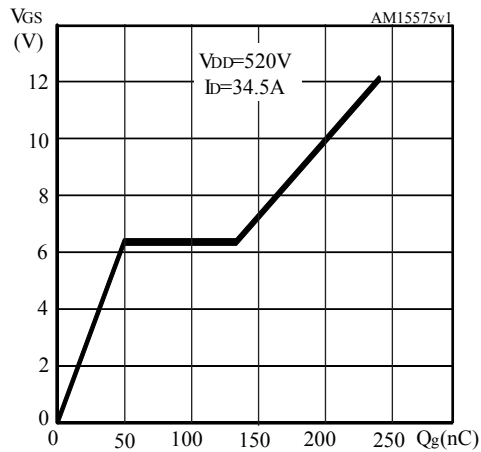
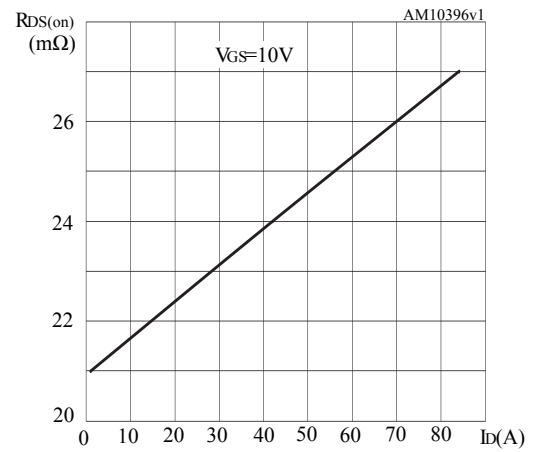
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage

Figure 6. Static drain-source on-resistance


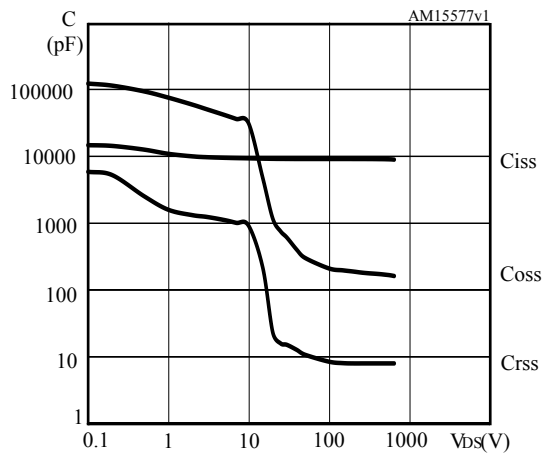
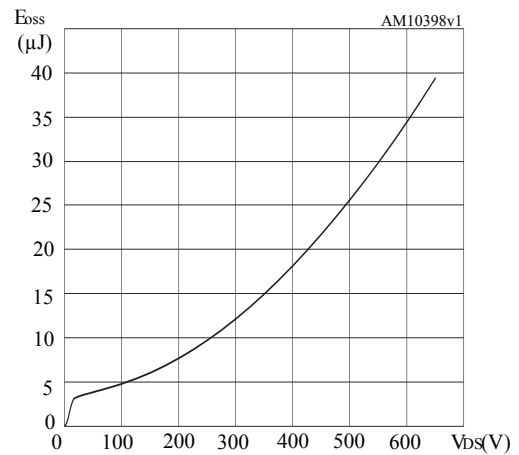
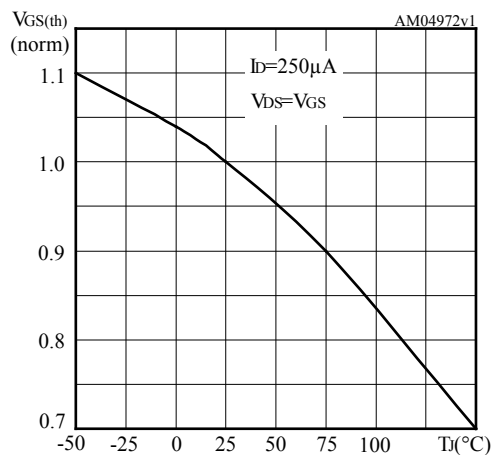
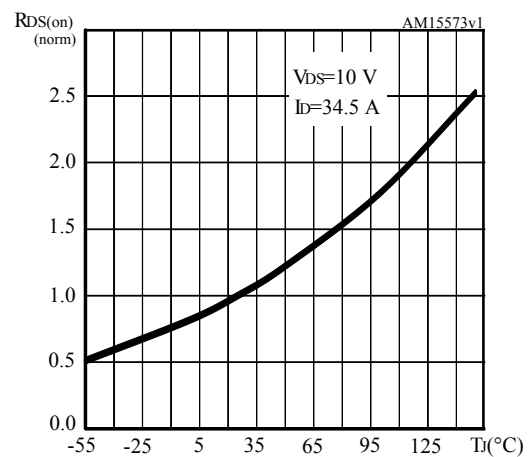
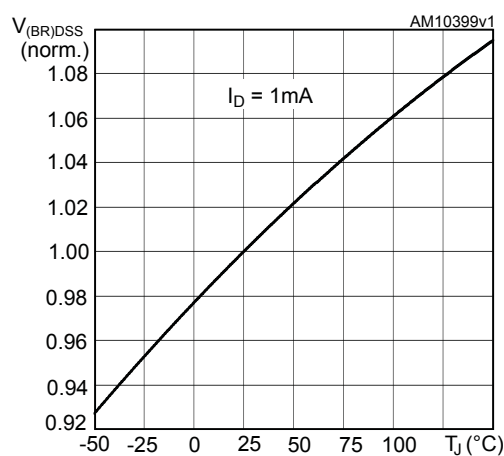
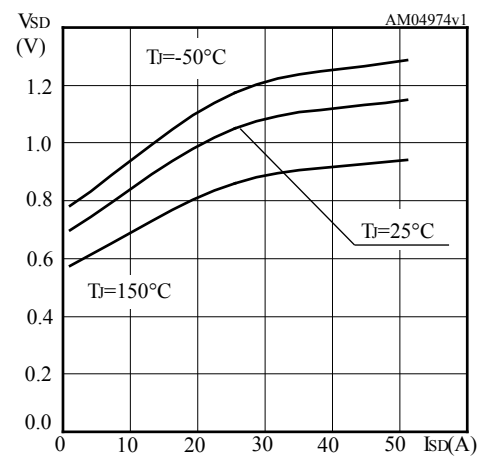
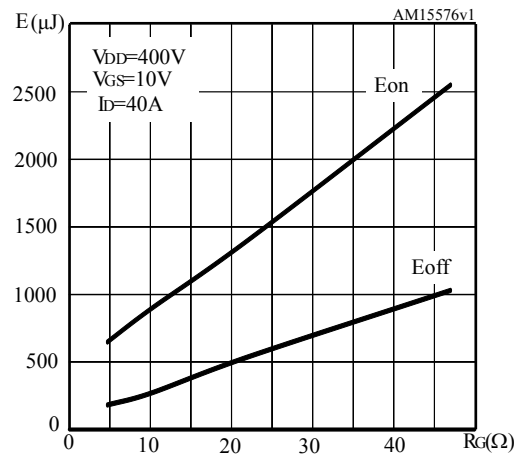
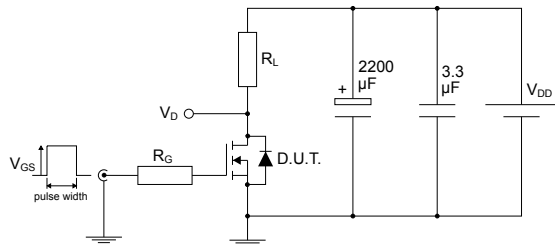
Figure 7. Capacitance variations

Figure 8. Output capacitance stored energy

Figure 9. Normalized gate threshold voltage vs temperature

Figure 10. Normalized on-resistance vs temperature

Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

Figure 12. Source-drain diode forward characteristics


Figure 13. Switching energy vs gate resistance

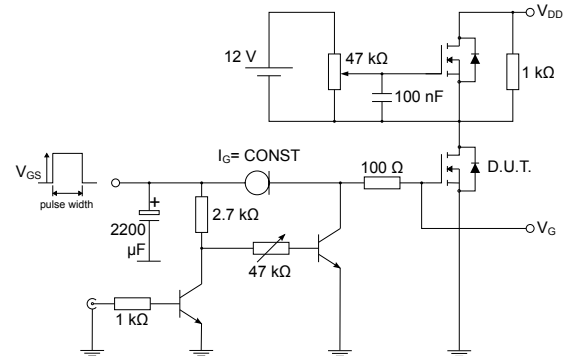


Note: E_{on} including reverse recovery of a SiC diode.

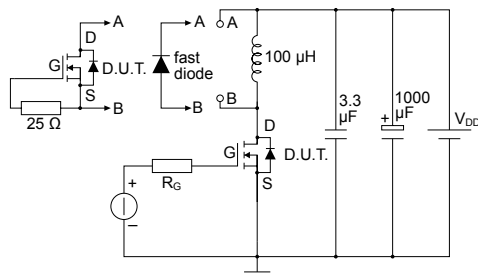
3 Test circuits

Figure 14. Test circuit for resistive load switching times


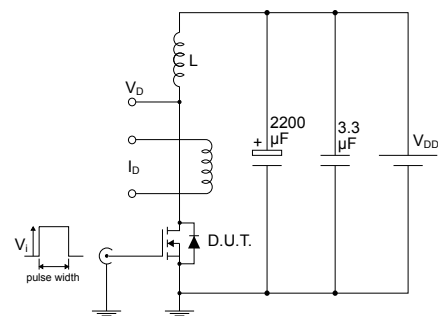
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Figure 15. Test circuit for gate charge behavior


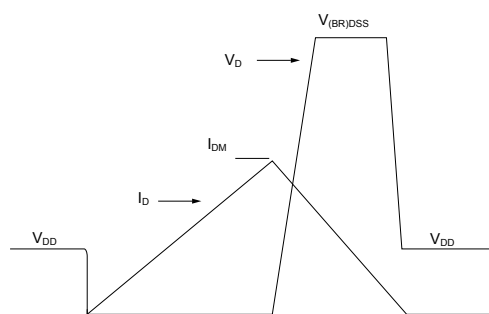
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Figure 16. Test circuit for inductive load switching and diode recovery times


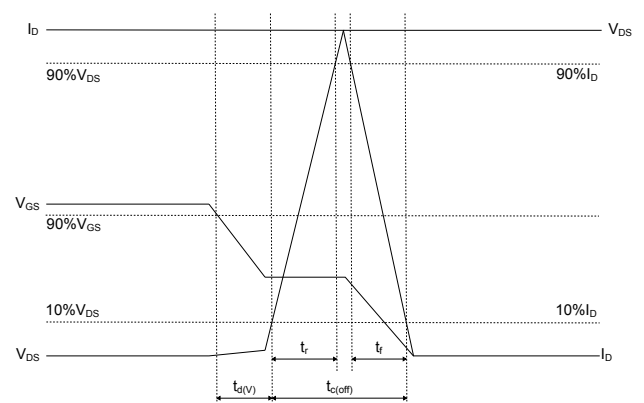
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Figure 17. Unclamped inductive load test circuit


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Figure 18. Unclamped inductive waveform


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Figure 19. Switching time waveform


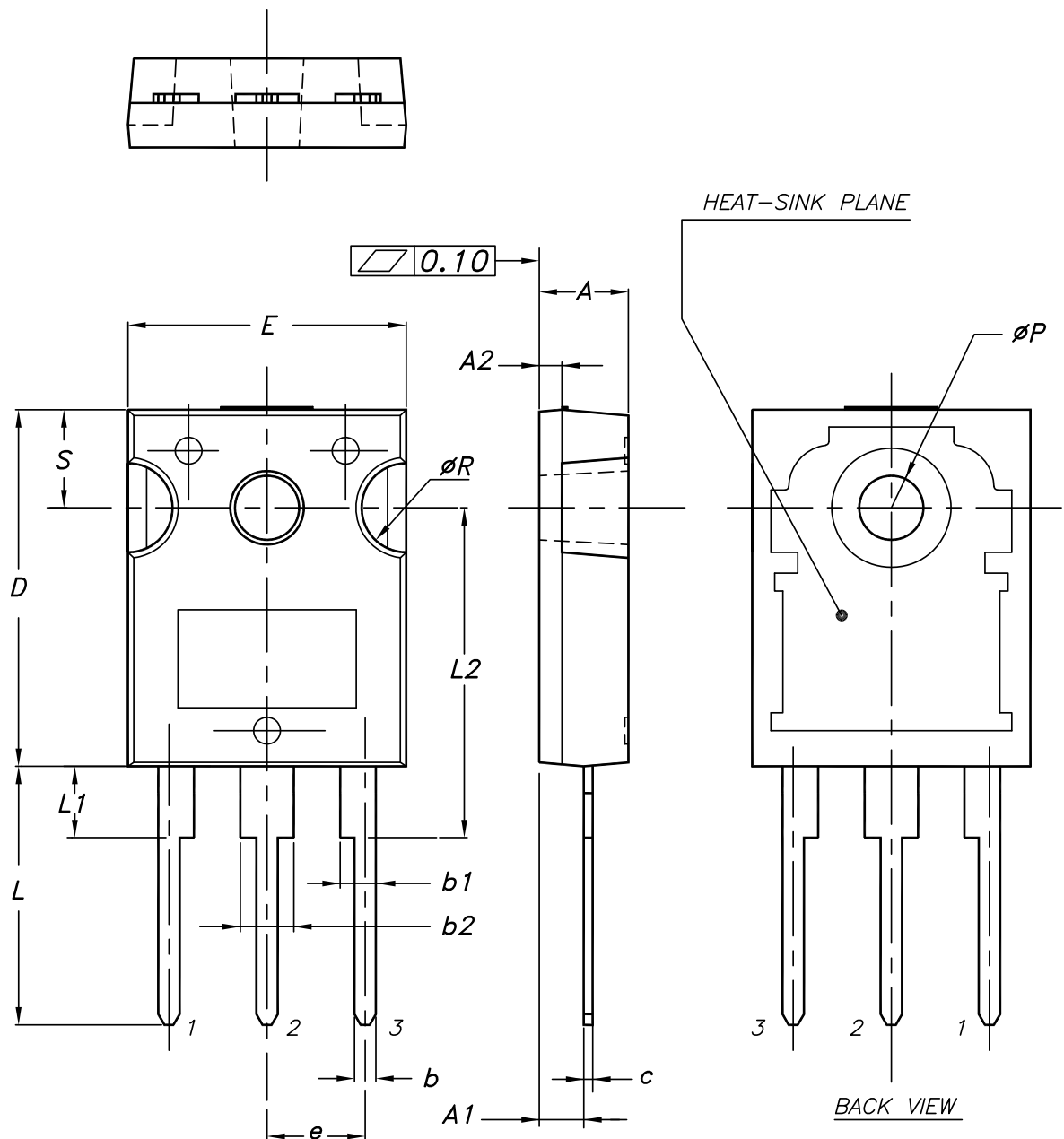
AM05540v2

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 20. TO-247 package outline



0075325_11

Table 8. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
A2		1.27	
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 9. Document revision history

Date	Revision	Changes
16-Jul-2012	1	First release.
22-Jan-2013	2	Modified: $R_{DS(on)}$ on first page, I_D , I_{DM} on <i>Table 2</i> , note 2 on <i>Table 2</i> , typical values on <i>Table 6</i> , <i>7</i> , max and typical values on <i>Table 8</i> , <i>Figure 2</i> , <i>6</i> , <i>8</i> , <i>9</i> , <i>11</i> and <i>14</i> .
07-Aug-2013	3	Minor text changes. Modified: <i>Applications</i> in first page. Added: MOSFET dv/dt ruggedness parameter in <i>Table 2</i> . Added: <i>Table 4: Avalanche characteristics</i> . Modified: <i>Figure 15</i> , <i>16</i> , <i>17</i> and <i>18</i> .
08-Aug-2013	4	Minor text changes. Modified: <i>Figure 14</i> .
26-Nov-2025	5	Updated Section 4: Package information . Minor text changes.

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