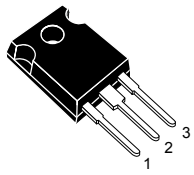
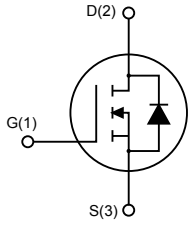
N-channel 300 V, 35 mΩ typ., 60 A STripFET™ II Power MOSFET in a TO-247 package



TO-247



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW74NF30	300 V	45 mΩ	60 A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process is specifically designed to minimize input capacitance and gate charge. It is therefore ideal as a primary switch in advanced high-efficiency isolated DC-DC converters.

STPOWER

Product status link
STW74NF30

Product summary	
Order code	STW74NF30
Marking	74NF30
Package	TO-247
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	300	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	60	A
I_D	Drain current (continuous) at T_C= 100 °C	37.8	A
I_{DM} (1)	Drain current (pulsed)	240	A
P_{TOT}	Total power dissipation at T_C = 25 °C	320	W
dv/dt (2)	Peak diode recovery voltage slope	12	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 60 A, di/dt ≤ 200 A/µs; V_{DD} ≤ 80% $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.39	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non- repetitive (pulse width limited by $T_{jmax.}$)	50	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	400	mJ

2 Electrical characteristics

(T_C= 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	300			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS} = 300 V			1	µA
		V_{GS} = 0 V, V_{DS} = 300 V, T_C = 125 °C (1)			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 30 A		35	45	mΩ

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	5930	-	pF
C_{oss}	Output capacitance		-	837	-	pF
C_{rss}	Reverse transfer capacitance		-	110	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 V to 240 V, V_{GS} = 0 V	-	462	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D=0 A	-	1.55	-	Ω
Q_g	Total gate charge	V_{DD} = 240 V, I_D = 60 A, V_{GS} = 0 to10 V (see Figure 14. Test circuit for gate charge behavior)	-	164	-	nC
Q_{gs}	Gate-source charge		-	36	-	nC
Q_{gd}	Gate-drain charge		-	69	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 150 V, I_D = 30 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	115	-	ns
t_r	Rise time		-	87	-	ns
$t_{d(off)}$	Turn-off delay time		-	141	-	ns
t_f	Fall time		-	101	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		60	A
I_{SDM} (1)	Source-drain current (pulsed)		-		240	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 60 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 60 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	252		ns
Q_{rr}	Reverse recovery charge		-	2.5		µC
I_{RRM}	Reverse recovery current		-	20		A
t_{rr}	Reverse recovery time	I_{SD} = 60 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	316		ns
Q_{rr}	Reverse recovery charge		-	3.7		µC
I_{RRM}	Reverse recovery current		-	23.2		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics curves

Figure 1. Safe operating area

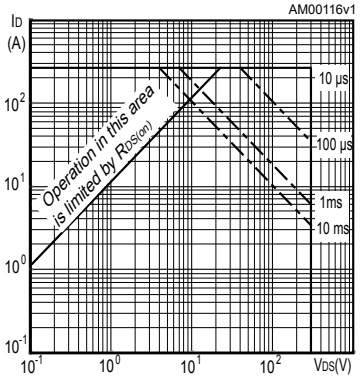


Figure 2. Thermal impedance

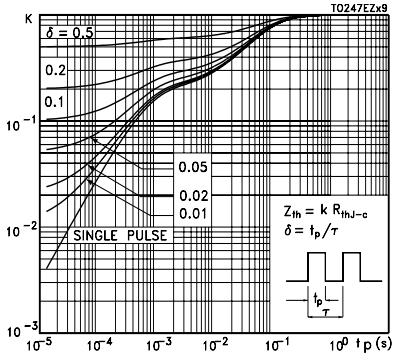


Figure 3. Output characteristics

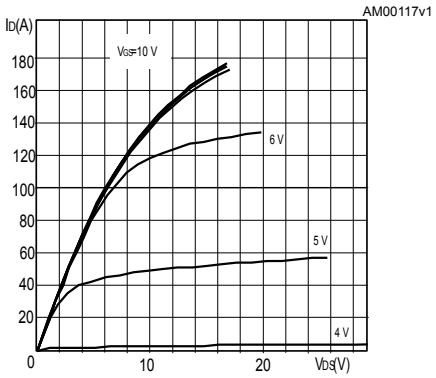


Figure 4. Transfer characteristics

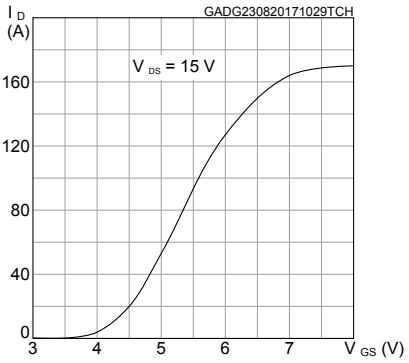


Figure 5. Gate charge vs. gate-source voltage

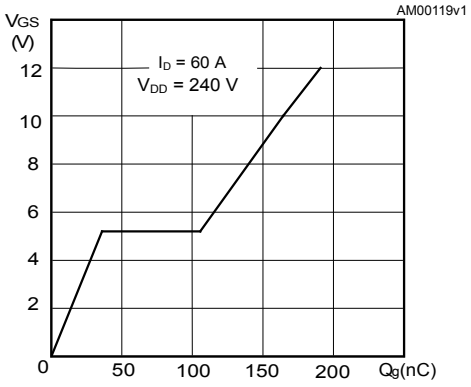


Figure 6. Static drain-source on-resistance

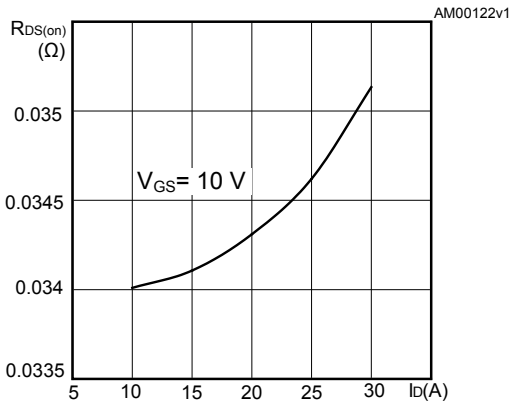


Figure 7. Capacitance variations

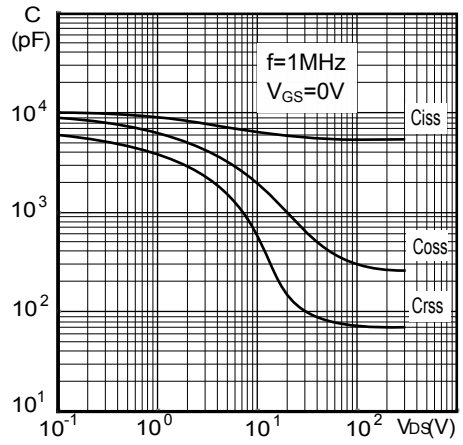


Figure 8. Normalized gate threshold voltage vs temperature

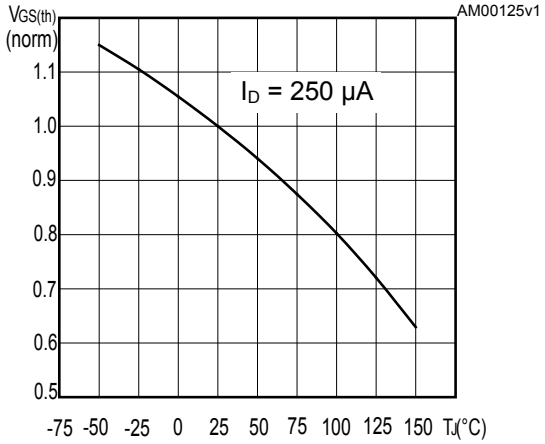


Figure 9. Normalized on-resistance vs temperature

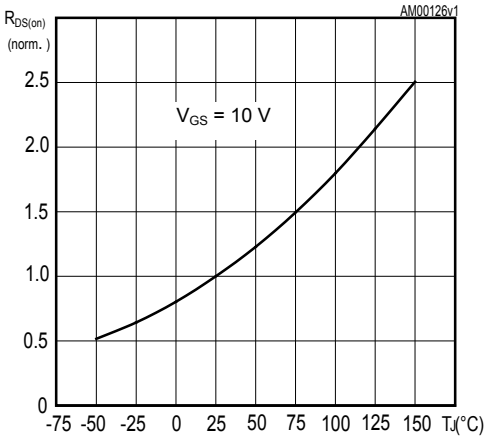


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

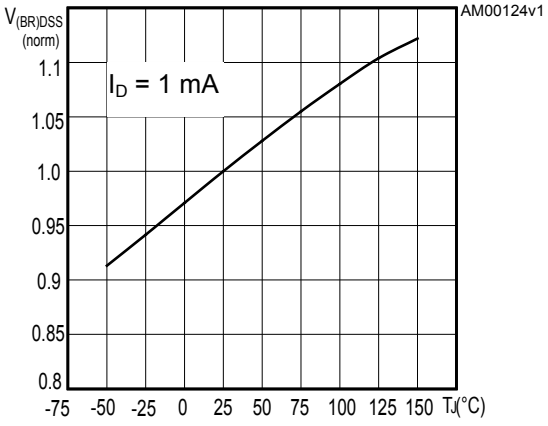


Figure 11. Maximum avalanche energy vs temperature

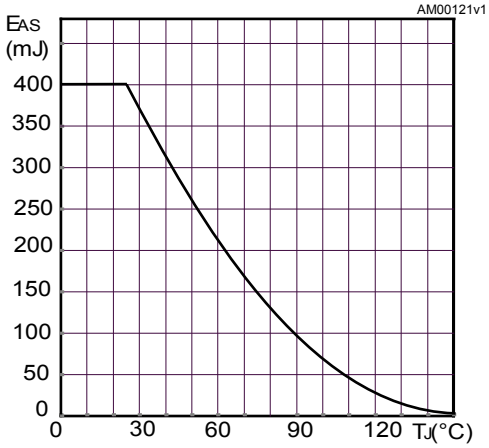
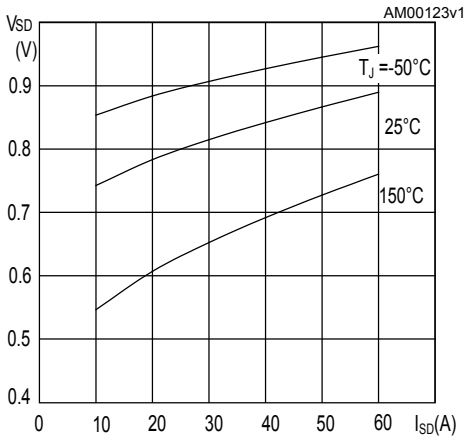


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

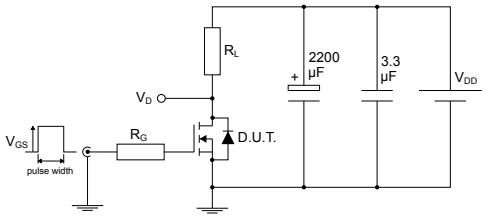


Figure 14. Test circuit for gate charge behavior

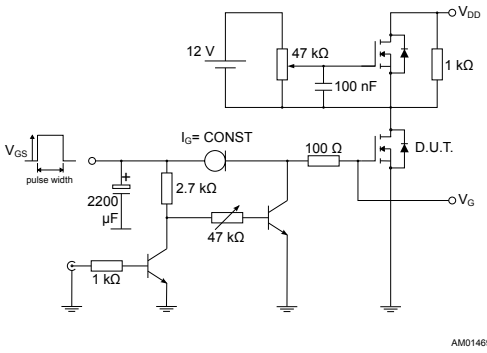


Figure 15. Test circuit for inductive load switching and diode recovery times

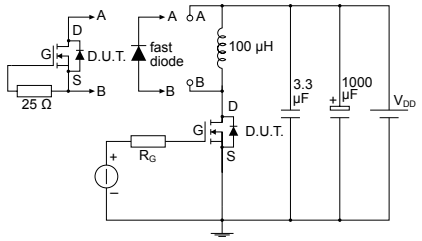


Figure 16. Unclamped inductive load test circuit

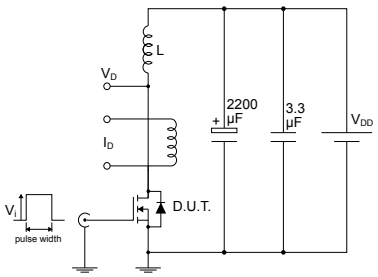


Figure 17. Unclamped inductive waveform

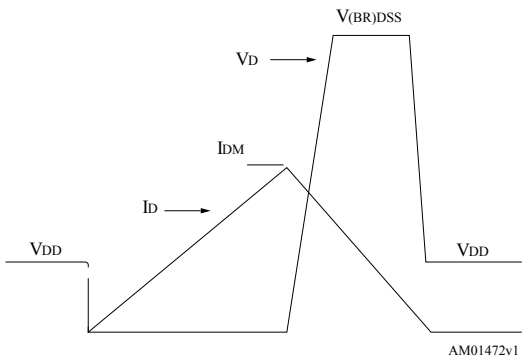
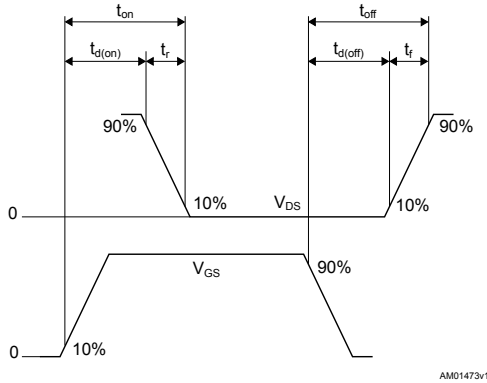


Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 19. TO-247 package outline

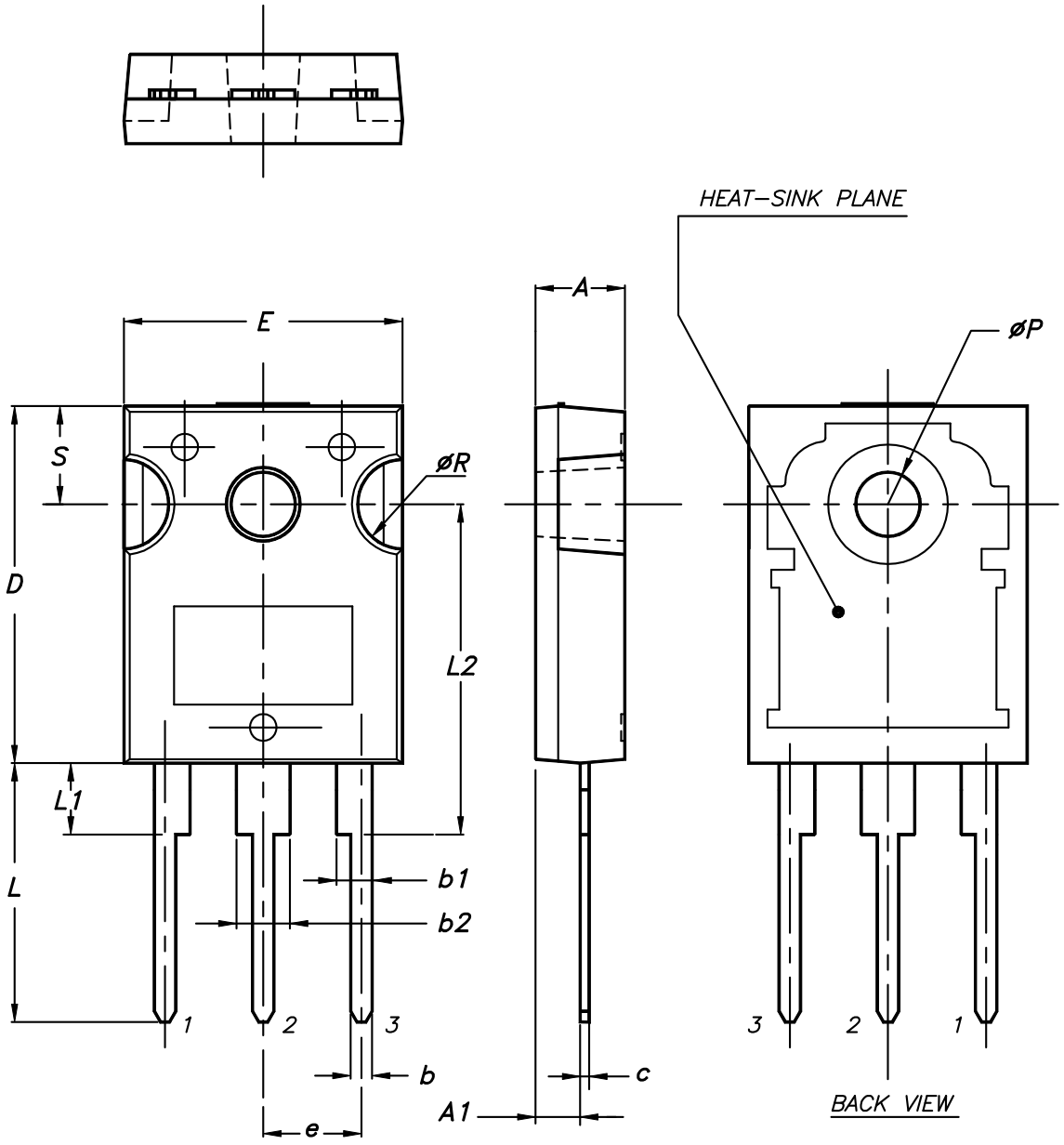


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Table 8. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
22-Oct-2018	1	First release.

Contents