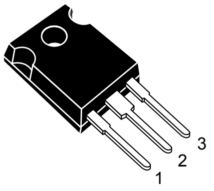
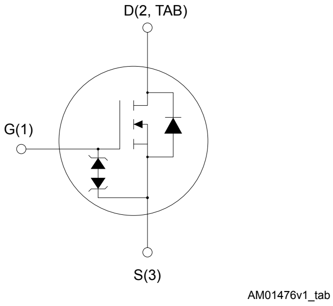
STW68N60M6

Datasheet

N-channel 600 V, 35 mΩ typ., 63 A MDmesh M6 Power MOSFET in a TO-247 package



TO-247



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW68N60M6	600 V	41 mΩ	63 A

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

Maturity status link
STW68N60M6

Device summary	
Order code	STW68N60M6
Marking	68N60M6
Package	TO-247
Packing	Tube

1 Electrical ratings

Table 1. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	63	A
	Drain current (continuous) at T_C = 100 °C	40	A
I_{DM} (1)	Drain current (pulsed)	252	A
P_{TOT}	Total power dissipation at T_C = 25 °C	390	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	100	
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *$I_{SD} \leq 63$ A, di/dt ≤ 400 A/µs, $V_{DS(peak)} < V_{(BR)DSS}$, V_{DD} = 400 V*
3. *$V_{DD} \leq 480$ V*

Table 2. **Thermal data**

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.32	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

Table 3. **Avalanche characteristics**

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	7.5	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	1100	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. **On /off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero-gate voltage drain current	V_{GS} = 0 V, V_{DS}= 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C[1]			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 31.5 A		35	41	mΩ

1. *Specified by design, not tested in production.*

Table 5. **Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	4360	-	pF
C_{oss}	Output capacitance		-	235	-	pF
C_{rss}	Reverse transfer capacitance		-	13	-	pF
$C_{oss\ eq.}$ [1]	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 480 V	-	713	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz open drain	-	1.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 63 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	106	-	nC
Q_{gs}	Gate-source charge		-	29	-	nC
Q_{gd}	Gate-drain charge		-	51	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. **Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d\ (on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 30 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	42	-	ns
t_r	Rise time		-	28	-	ns
$t_{d(off)}$	Turn-off delay time		-	130	-	ns
t_f	Fall time		-	8	-	ns

Table 7. **Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		63	A
I_{SDM} (1)	Source-drain current (pulsed)		-		252	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 63 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 63 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	308		ns
Q_{rr}	Reverse recovery charge		-	4.3		µC
I_{RRM}	Reverse recovery current		-	26		A
t_{rr}	Reverse recovery time	I_{SD} = 63 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	504		ns
Q_{rr}	Reverse recovery charge		-	10.8		µC
I_{RRM}	Reverse recovery current		-	38		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

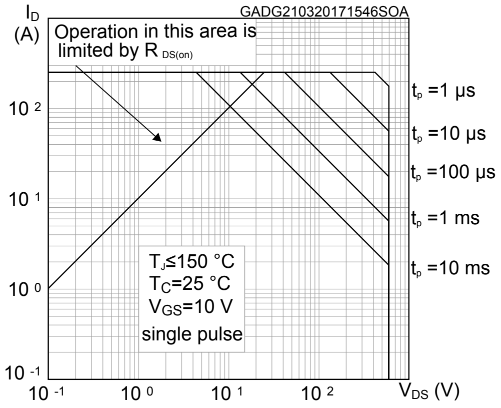


Figure 2. Thermal impedance

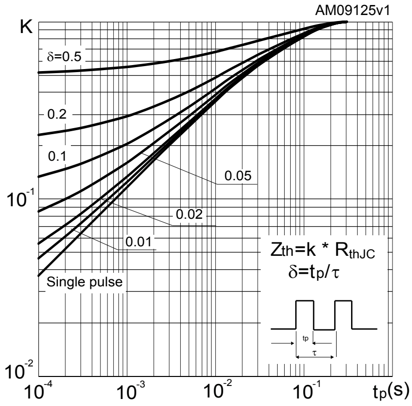


Figure 3. Output characteristics

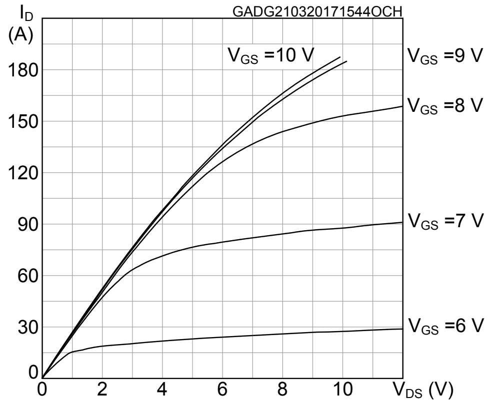


Figure 4. Transfer characteristics

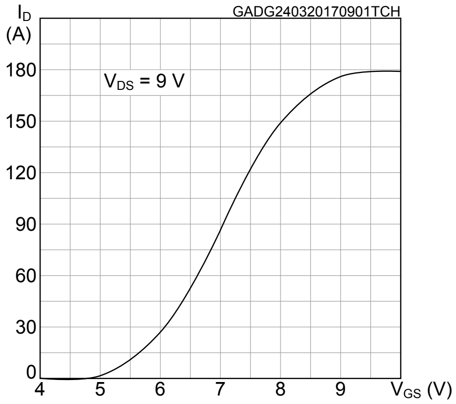


Figure 5. Gate charge vs gate-source voltage

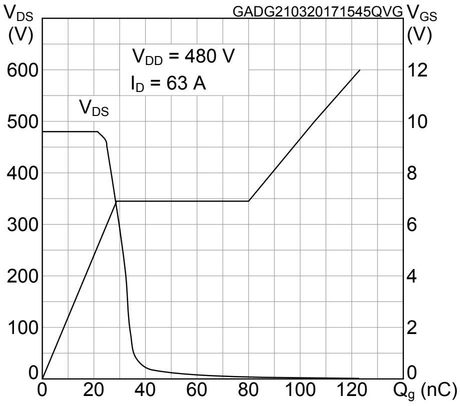


Figure 6. Static drain-source on-resistance

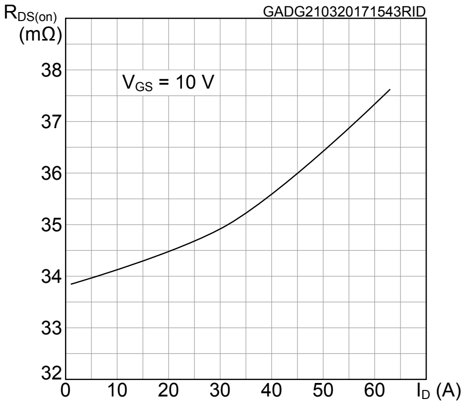


Figure 7. Capacitance variations

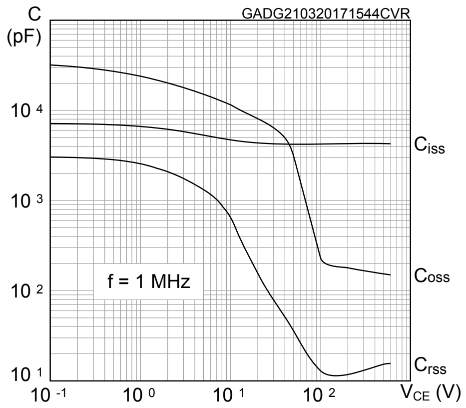


Figure 8. Normalized gate threshold vs. temperature

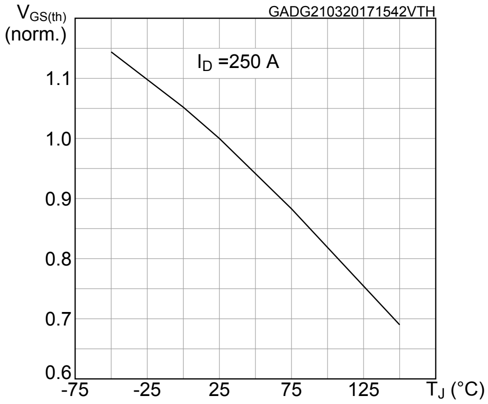


Figure 9. Normalized on-resistance vs. temperature

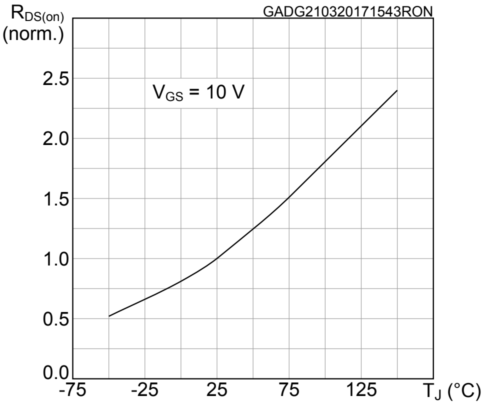


Figure 10. Normalized $V_{(BR)DSS}$ vs. temperature

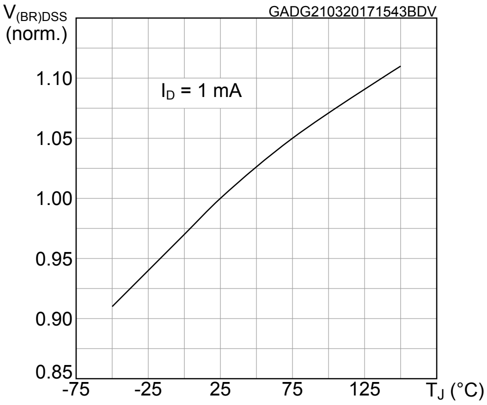


Figure 11. Output capacitance stored energy

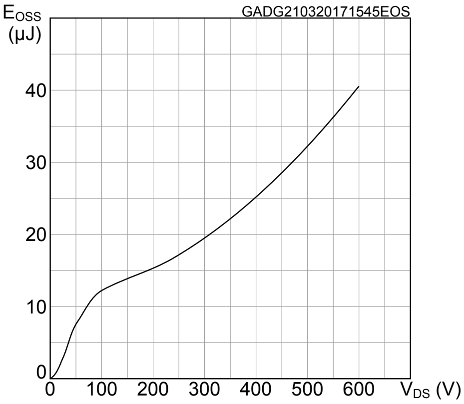
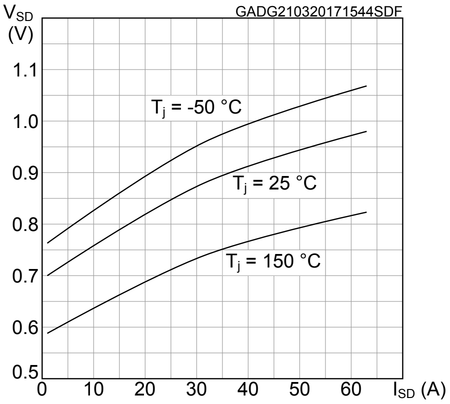


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

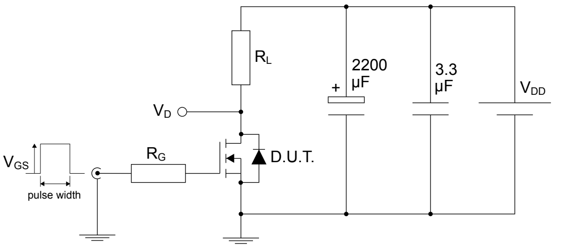


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Figure 14. Test circuit for gate charge behavior

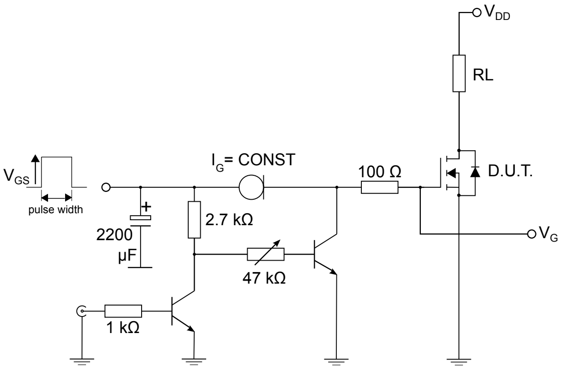

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Figure 15. Test circuit for inductive load switching and diode recovery times

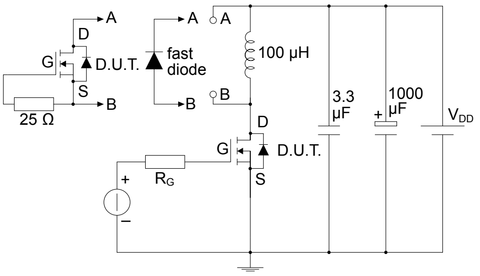

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Figure 16. Unclamped inductive load test circuit

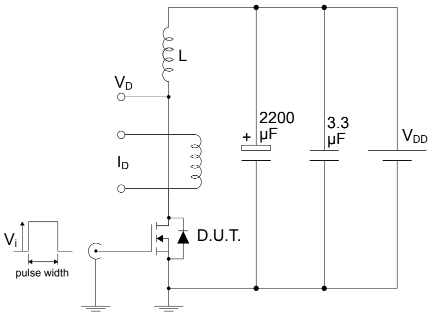

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Figure 17. Unclamped inductive waveform

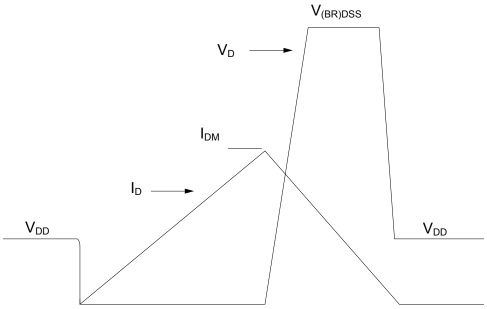

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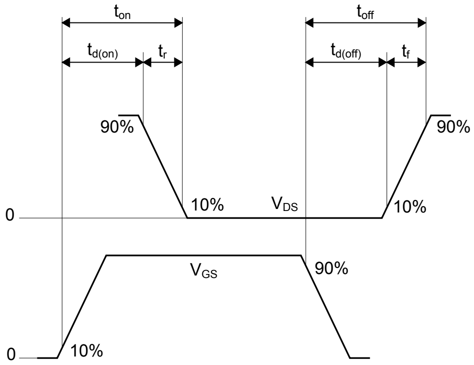
Figure 18. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 19. **TO-247 package outline**

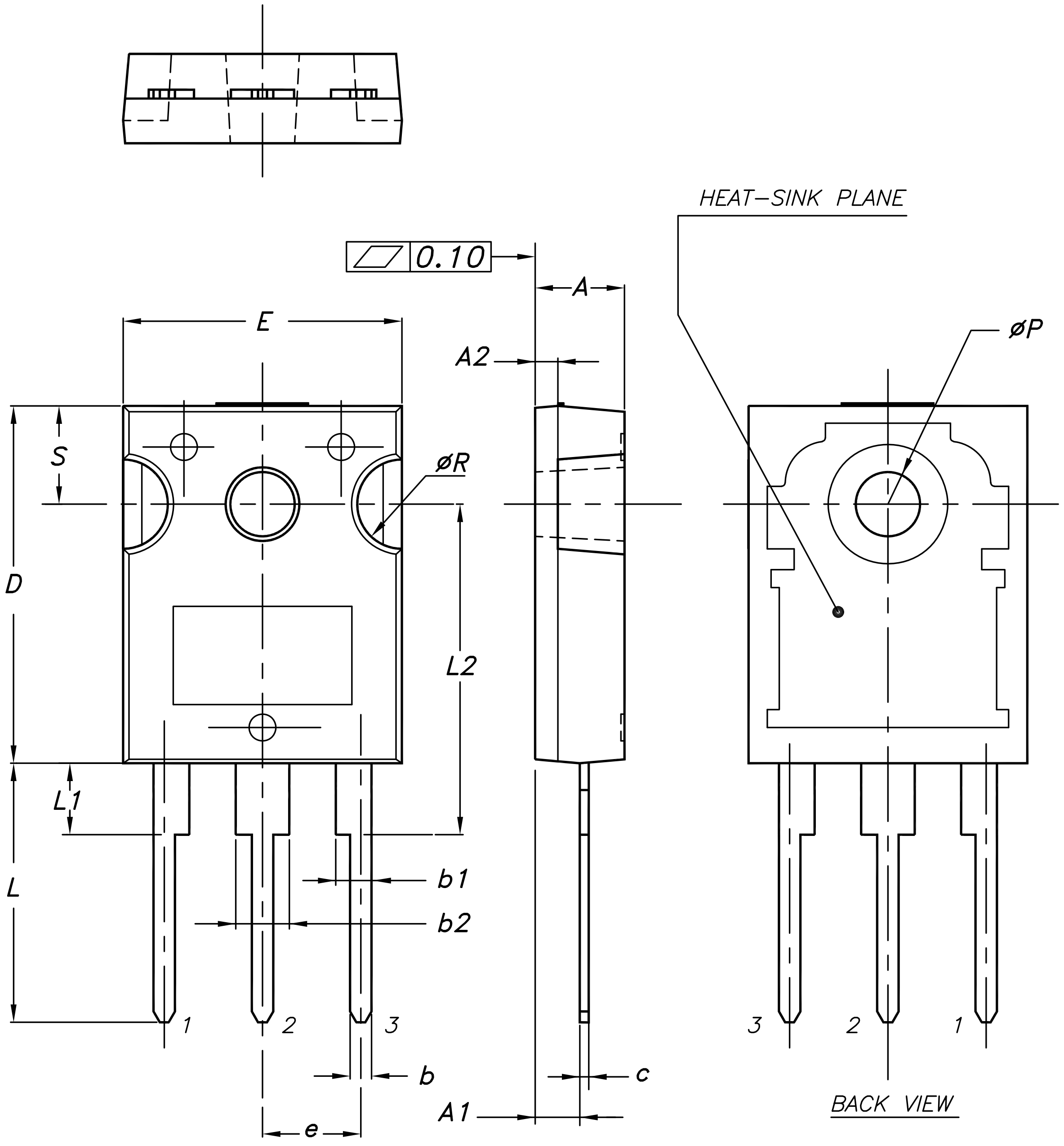

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Table 8. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
A2		1.27	
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
27-Mar-2017	1	First release.
05-Nov-2018	2	Removed maturity status indication from cover page. The document status is production data. Modified *Table 1. Absolute maximum ratings, Table 5. Dynamic* and *Table 7. Source-drain diode* Modified *Figure 1. Safe operating area, Figure 3. Output characteristics, Figure 4. Transfer characteristics, Figure 5. Gate charge vs gate-source voltage, Figure 6. Static drain-source on-resistance, Figure 7. Capacitance variations, Figure 8. Normalized gate threshold vs. temperature, Figure 9. Normalized on-resistance vs. temperature, Figure 10. Normalized V(BR)DSS vs temperature* and *Figure 12. Source-drain diode forward characteristics.* Minor text changes.
01-Dec-2025	3	Updated Section 4: Package information. Minor text changes.

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