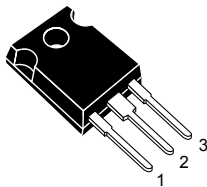
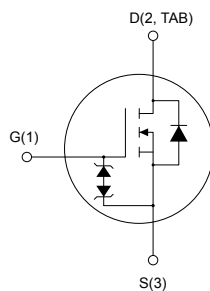


Automotive-grade N-channel 650 V, 58 mΩ typ., 48 A, MDmesh DM2 Power MOSFET in a TO-247 package



TO-247



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STW58N65DM2AG	650 V	65 mΩ	48 A	360 W

- AEC-Q101 qualified 
- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Product status link

[STW58N65DM2AG](#)

Product summary

Order code	STW58N65DM2AG
Marking	58N65DM2
Package	TO-247
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	48	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	30	
$I_{DM}^{(1)}$	Drain current (pulsed)	150	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	360	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 48\text{ A}$, $di/dt=800\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$
3. $V_{DD} \leq 520\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.35	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	50	

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (Pulse width is limited by T_J , max)	7	A
E_{AS}	Single pulse avalanche energy (Starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	1300	mJ

2 Electrical characteristics

($T_{case} = 25\text{ °C}$ unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			10	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 24\text{ A}$		58	65	m Ω

1. Specified by design, not tested in production

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	4100	-	pF
C_{oss}	Output capacitance		-	160	-	
C_{rss}	Reverse transfer capacitance		-	2.5	-	
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$	-	375	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	4.1	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 48\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	88	-	nC
Q_{gs}	Gate-source charge		-	22	-	
Q_{gd}	Gate-drain charge		-	37	-	

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D = 24\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	28	-	ns
t_r	Rise time		-	31	-	
$t_{d(off)}$	Turn-off delay time		-	157	-	
t_f	Fall time		-	7.7	-	

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		48	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		150	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 48\text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 48\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	135		ns
Q_{rr}	Reverse recovery charge		-	0.68		μC
I_{RRM}	Reverse recovery current		-	10		A
t_{rr}	Reverse recovery time	$I_{SD} = 48\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	260		ns
Q_{rr}	Reverse recovery charge		-	2.75		μC
I_{RRM}	Reverse recovery current		-	21		A

1. Pulse width is limited by safe operating area.

2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

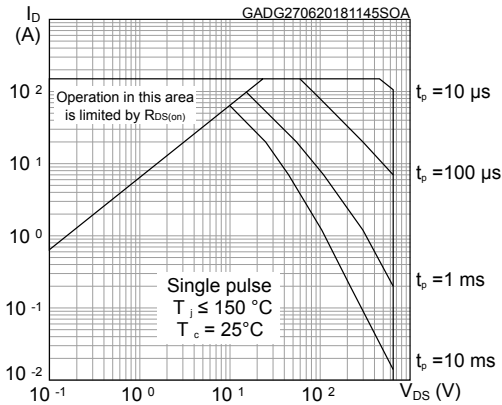
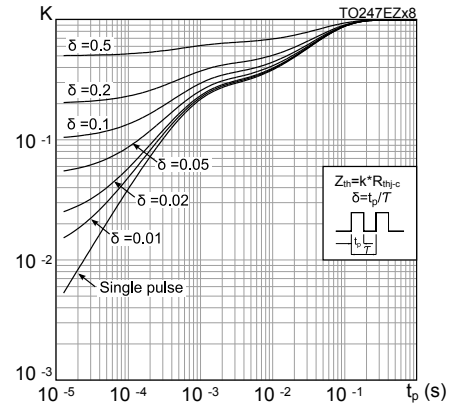
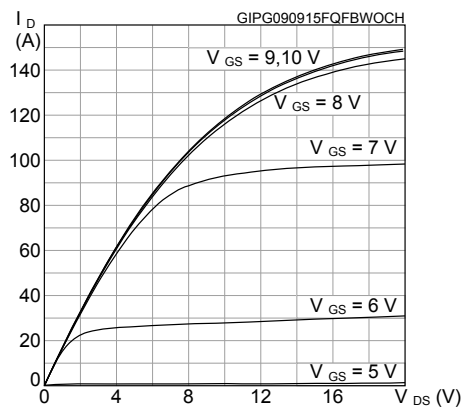
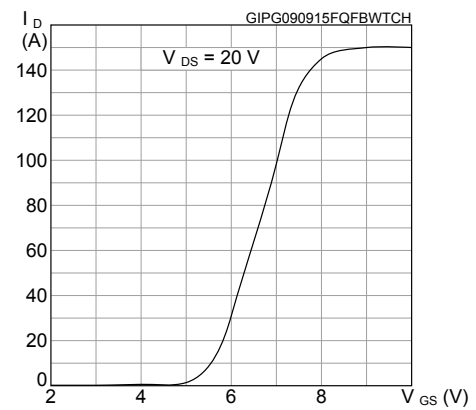
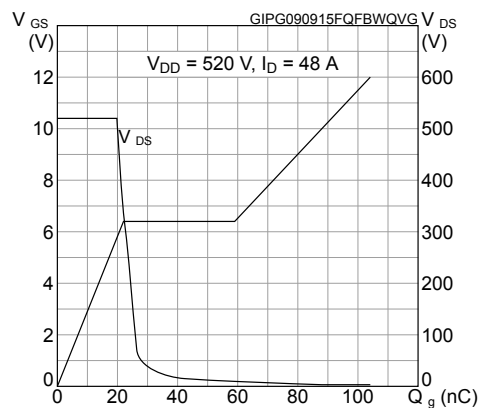
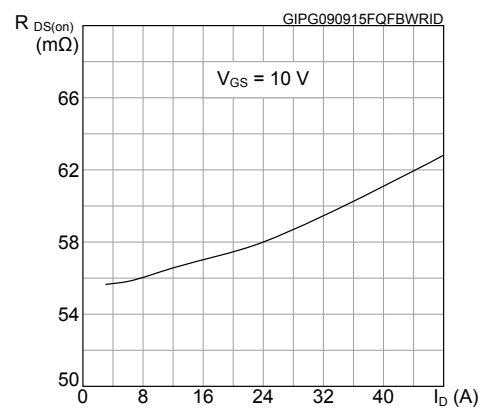
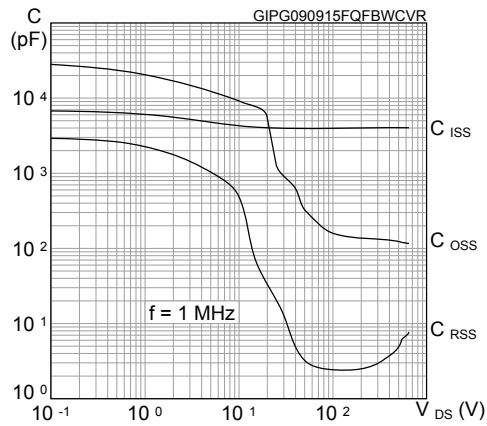
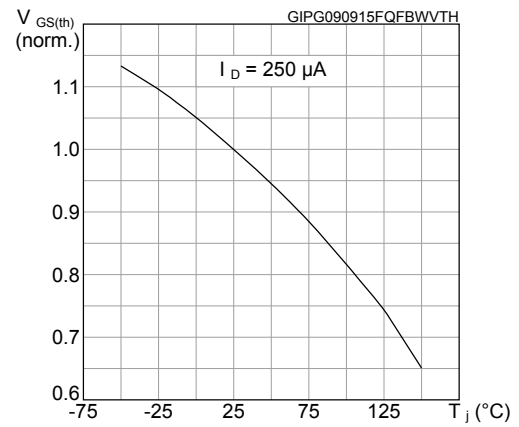
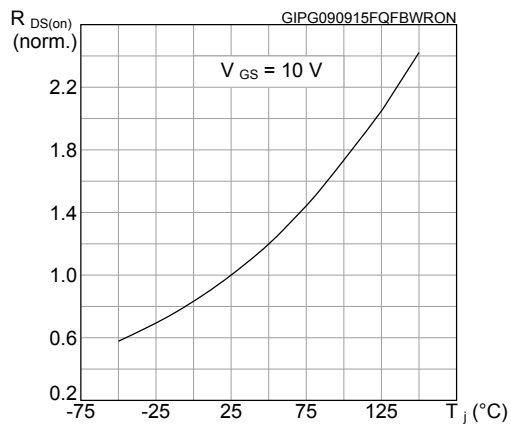
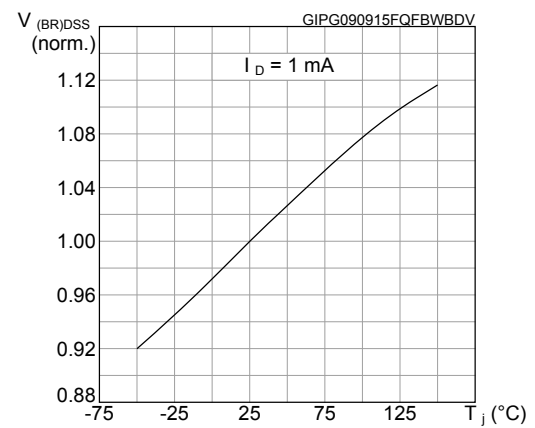
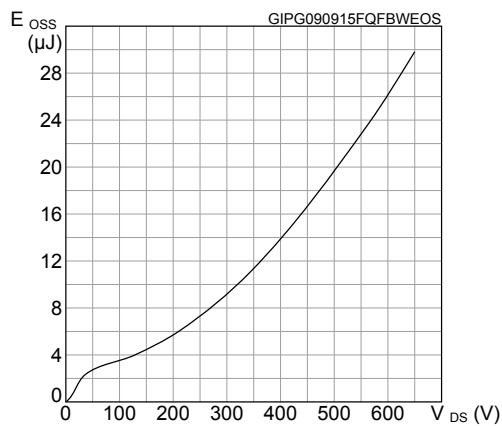
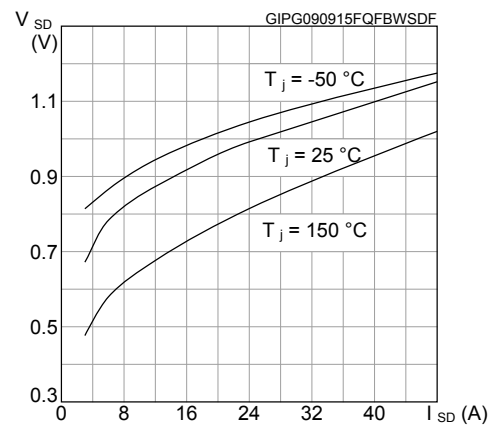
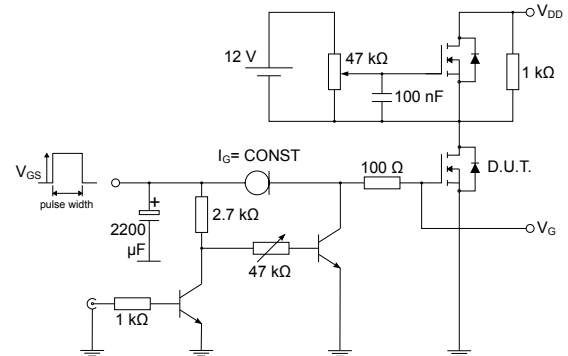
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage

Figure 6. Static drain-source on-resistance


Figure 7. Capacitance variations

Figure 8. Normalized gate threshold voltage vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Normalized V_(BR)DSS vs temperature

Figure 11. Output capacitance stored energy

Figure 12. Source-drain diode forward characteristics


3 Test circuits

Figure 13. Test circuit for resistive load switching times


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Figure 14. Test circuit for gate charge behavior


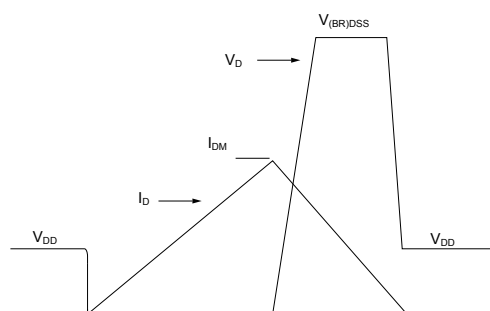
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Figure 15. Test circuit for inductive load switching and diode recovery times


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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform

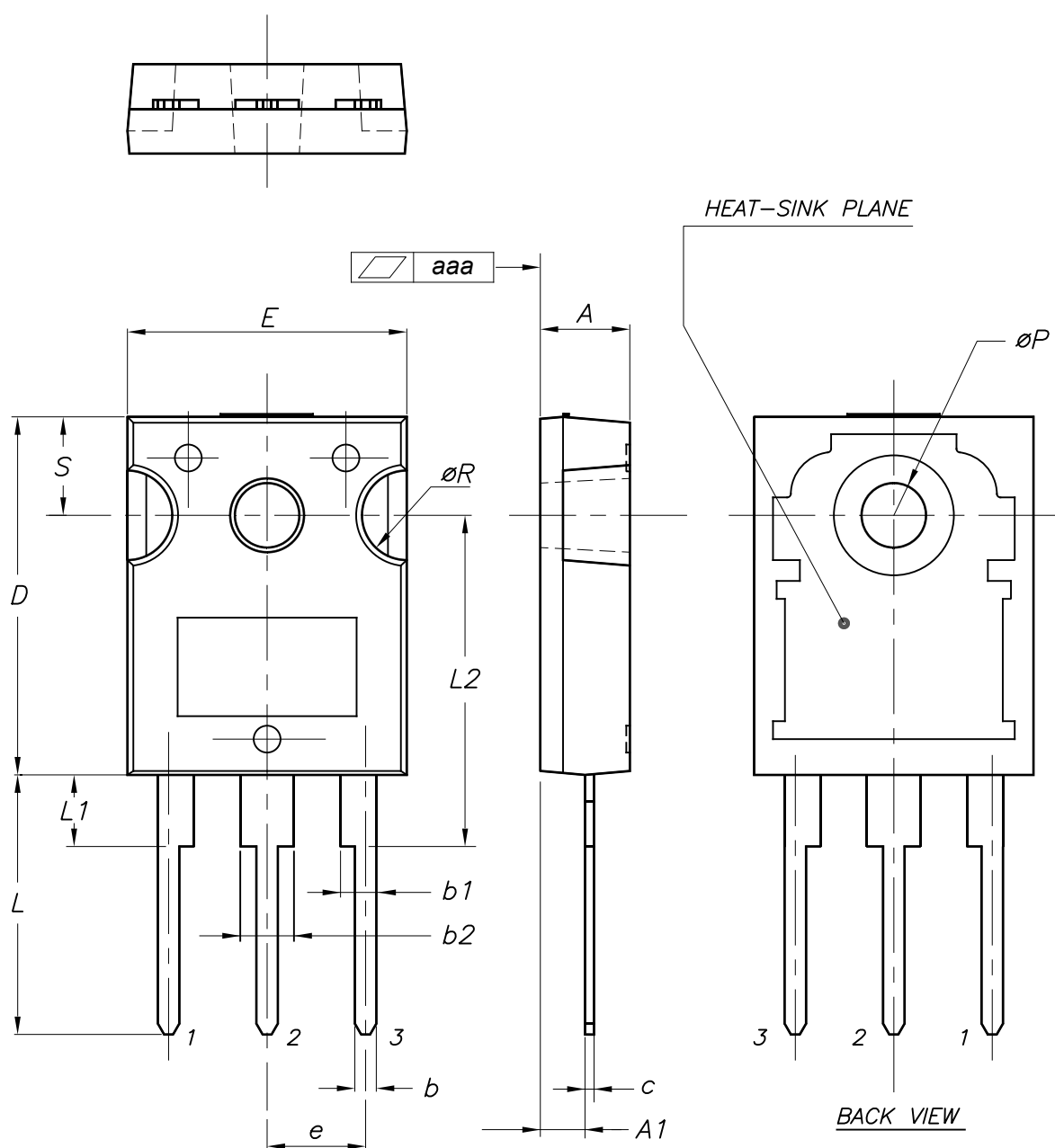

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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 19. TO-247 package outline



0075325_10

Table 8. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

Revision history

Table 9. Document revision history

Date	Version	Changes
09-Sep-2015	1	Initial release.
15-Sep-2015	2	In section <i>Electrical characteristics (curves)</i> : - updated figure <i>Safe operating area</i>
02-Jul-2018	3	Removed maturity status indication from cover page. The document status is production data. Updated <i>Table 1. Absolute maximum ratings</i> and <i>Table 7. Source-drain diode</i> . Updated <i>Figure 1. Safe operating area</i> . Minor text changes
28-Oct-2025	4	Updated Section 4: Package information . Minor text changes

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