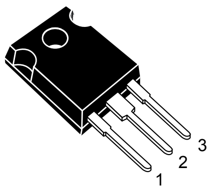
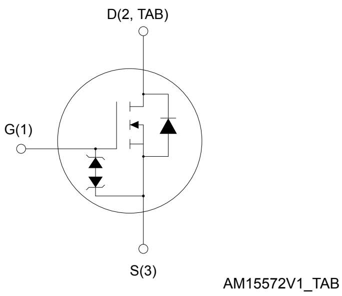
STW11NK100Z

Datasheet

N-channel 1000 V, 0.83 Ω typ., 8.3 A SuperMESH Power MOSFET in a TO-247 package



TO-247



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW11NK100Z	1000 V	1.38 Ω	8.3 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Zener-protected

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link
STW11NK100Z

Product summary	
Order code	STW11NK100Z
Marking	W11NK100Z
Package	TO-247
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1000	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	8.3	A
	Drain current (continuous) at T_C = 100 °C	5.2	
I_{DM} (1)	Drain current (pulsed)	33.2	A
P_{TOT}	Total power dissipation at T_C = 25 °C	230	W
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	6	kV
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 8.3 A, di/dt ≤ 200 A/μs, V_{DS} (peak) < $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.54	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	8.3	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	550	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	1000	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1000 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 1000 V, T_C = 125 °C[1]	-	-	50	µA
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4.15 A	-	0.83	1.38	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	3500	-	pF
C_{oss}	Output capacitance		-	270	-	pF
C_{rss}	Reverse transfer capacitance		-	60	-	pF
$C_{oss\ eq.}$[1]	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 500 V	-	170	-	pF
Q_g	Total gate charge	V_{DD} = 800 V, I_D = 8 A, V_{GS} = 0 to 10 V (see the Figure 14. Test circuit for gate charge behavior)	-	113	162[2]	nC
Q_{gs}	Gate-source charge		-	18	-	nC
Q_{gd}	Gate-drain charge		-	60	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *Specified by design, not tested in production.*

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 800 V, I_D = 8 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	27	-	ns
t_r	Rise time		-	18	-	ns
$t_{d(off)}$	Turn-off delay time		-	98	-	ns
t_f	Fall time		-	55	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	8.3	A
I_{SDM} (1)	Source-drain current (pulsed)		-	-	33.2	A
V_{SD} (2)	Forward on voltage	I_{SD} = 8.3 A, V_{GS} = 0 V	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 8.3 A, di/dt = 100 A/µs, V_{DD} = 80 V (see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	560	-	ns
Q_{rr}	Reverse recovery charge		-	4.48	-	µC
I_{RRM}	Reverse recovery current		-	16	-	A
t_{rr}	Reverse recovery time	I_{SD} = 8.3 A, di/dt = 100 A/µs, V_{DD} = 80 V, T_J = 150 °C (see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	620	-	ns
Q_{rr}	Reverse recovery charge		-	4.57	-	µC
I_{RRM}	Reverse recovery current		-	16	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

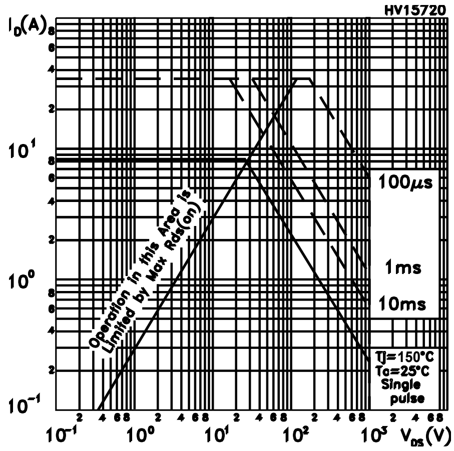


Figure 2. Normalized transient thermal impedance

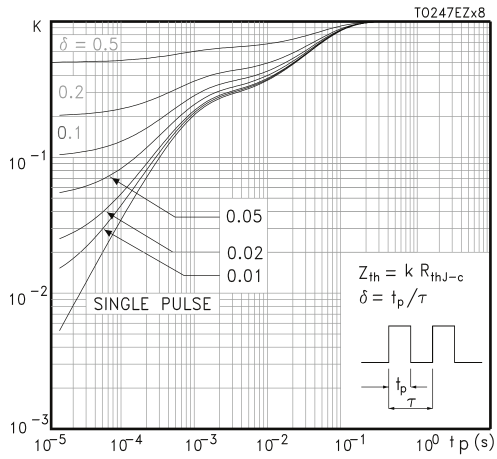


Figure 3. Typical output characteristics

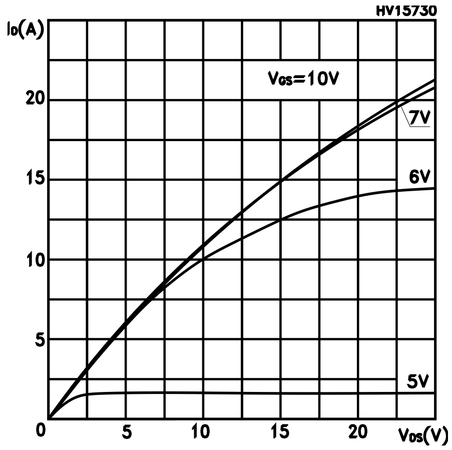


Figure 4. Typical transfer characteristics

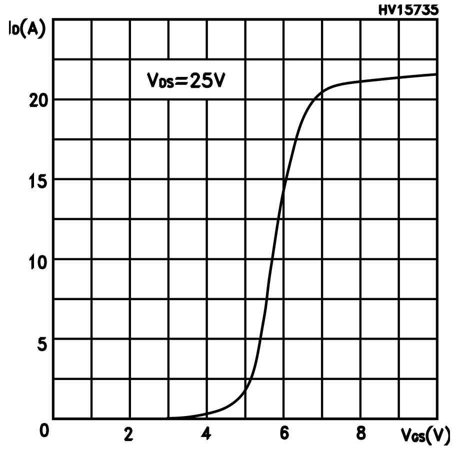


Figure 5. Gate charge vs gate-source voltage

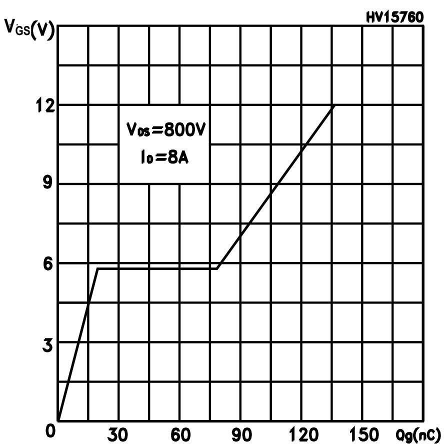


Figure 6. Typical drain-source on-resistance

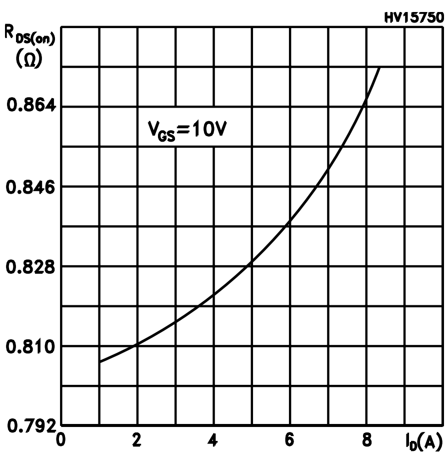


Figure 7. Capacitance variations

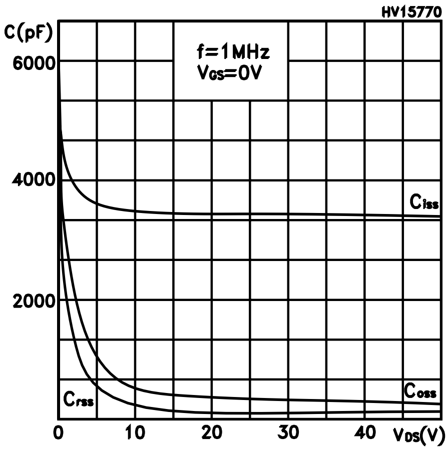


Figure 8. Normalized gate threshold vs temperature

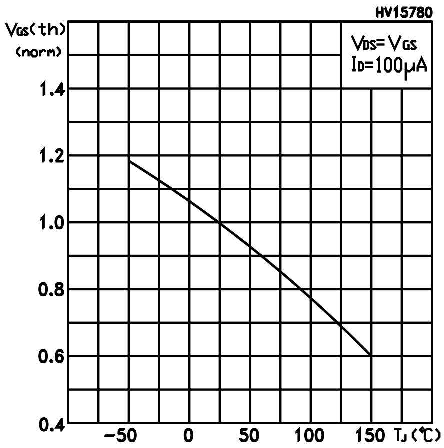


Figure 9. Normalized on-resistance vs temperature

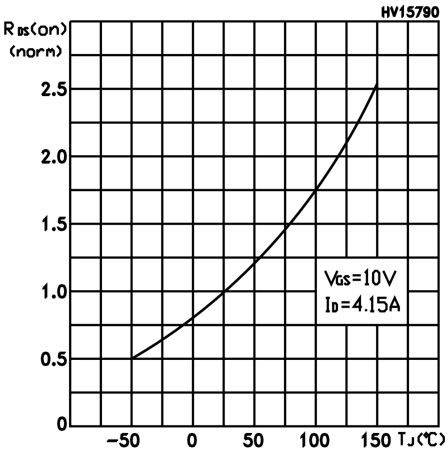


Figure 10. Normalized breakdown voltage vs temperature

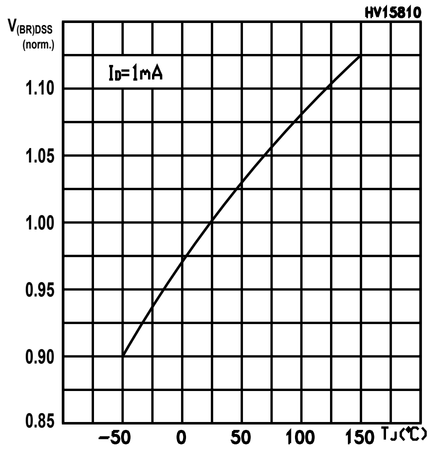


Figure 11. Maximum avalanche energy vs temperature

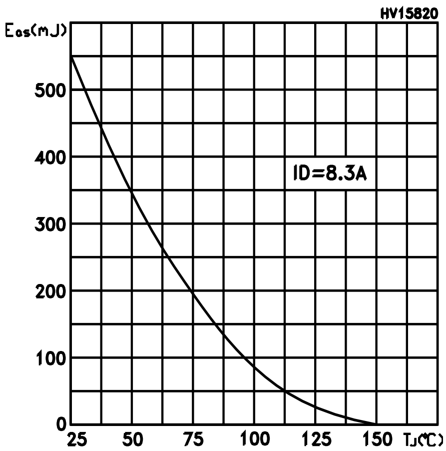
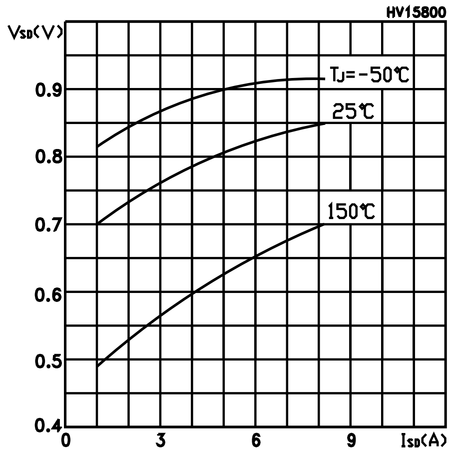


Figure 12. Typical reverse diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times

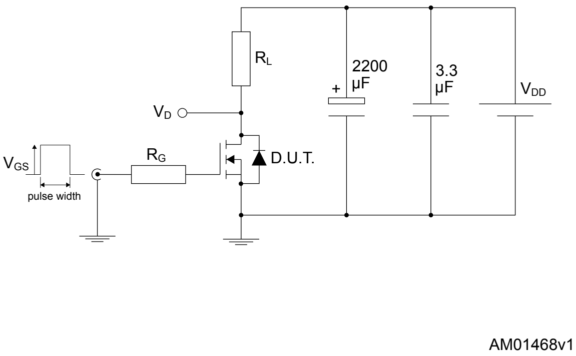


Figure 14. Test circuit for gate charge behavior

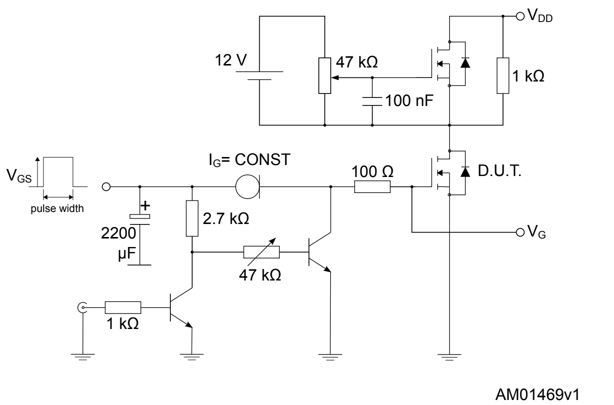


Figure 15. Test circuit for inductive load switching and diode recovery times

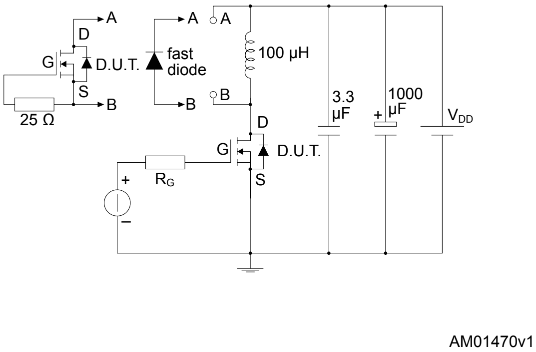


Figure 16. Unclamped inductive load test circuit

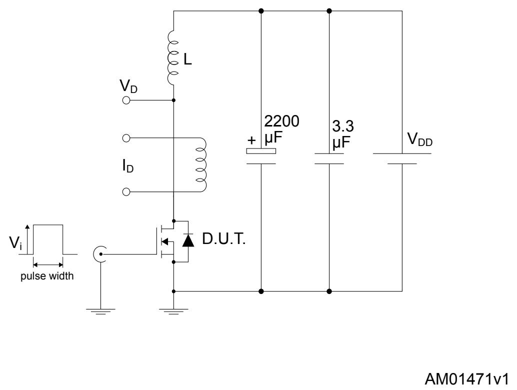


Figure 17. Unclamped inductive waveform

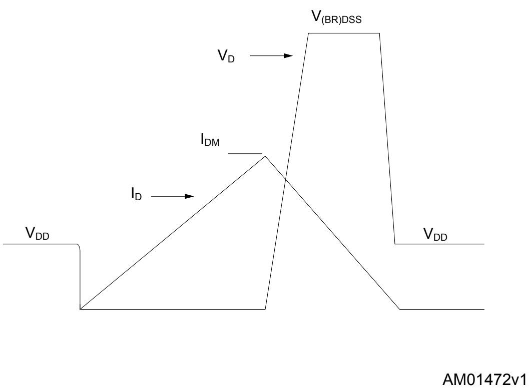
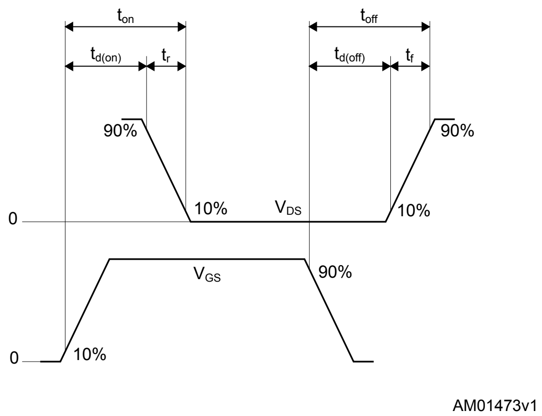


Figure 18. Switching time waveform



4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 19. TO-247 package outline

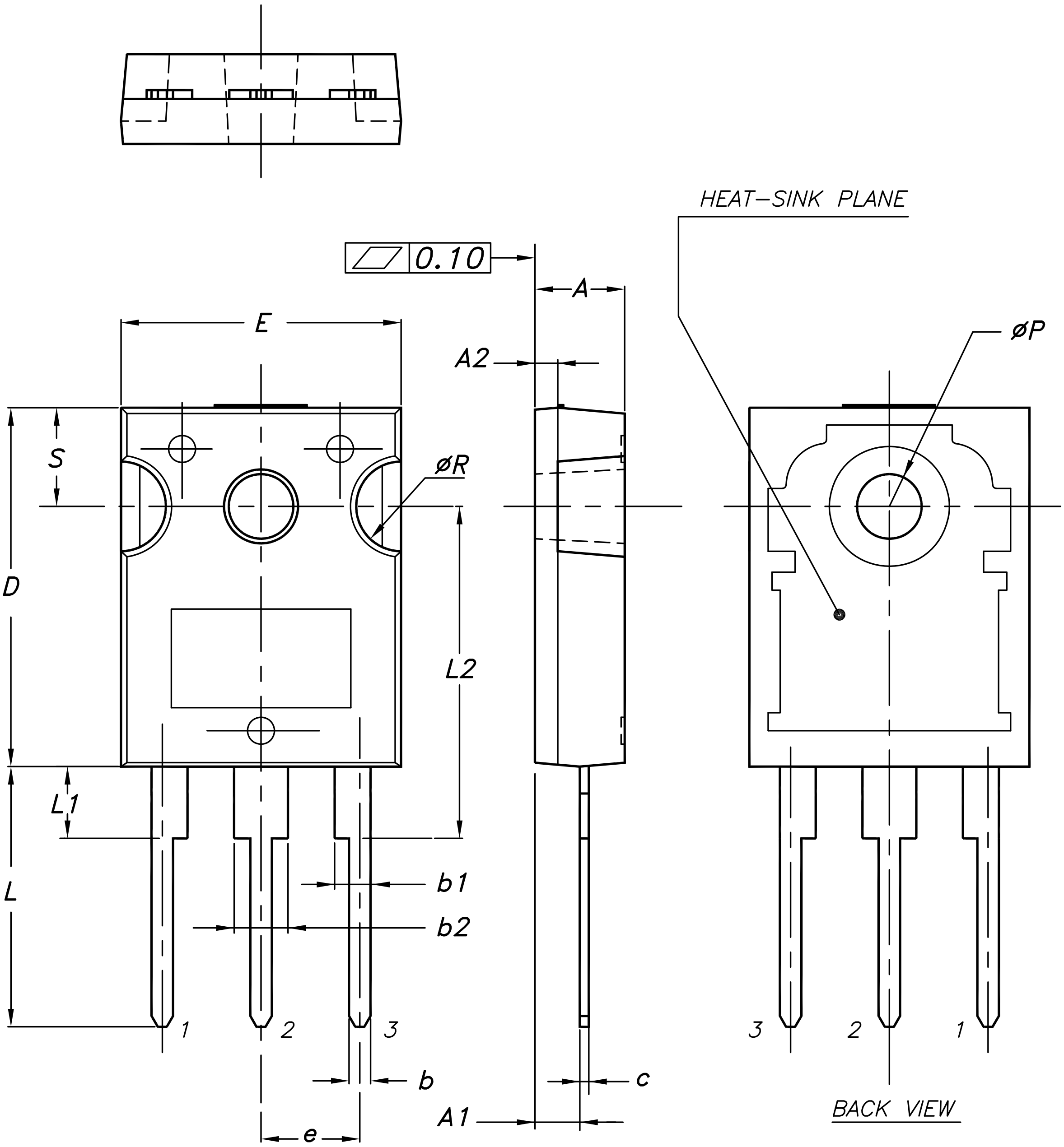


Table 8. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
A2		1.27	
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
21-Jun-2004	1	First release.
31-Jul-2006	2	New template, no content change.
19-Jan-2026	3	Updated Section 4: Package information. Minor text changes.

Contents