STUSB4531

Datasheet

Standalone SINK USB PD controller

QFN-16
3 x 3 mm²

CSP-16
2.3 x 2.3 mm²

Maturity status link
STUSB4531

Features

- Up to 5 SINK PDO profiles (fixed, variable, PPS)
- Static or dynamic PDO configuration support
- Source profile reporting
- Standalone PD stack
- Hybrid software mode
- Active V_{BUS} voltage monitoring
- Integrated system and cable discharge path
- Integrated V_{BUS} switches gate driver (PMOS)
- External Vconn support
- Short-to-V_{BUS} protections
- AMR = 28 V
- Temperature range: -40 °C up to 105 °C
- ESD = 1 kV CDM / 4 kV HBM

Certification

- USB Type-C® (rev2.4)
- USB Power delivery specifications (rev3.2)
- TID: 13956
- EU conformity: IEC 62680-1-3:2024 / IEC 62680-1-2:2024

Applications

- USB micro-B and DC barrel replacement
- VBUS powered, battery powered, and externally powered applications
- Set-top-box, camcorders, cameras, gaming, displays, and TV
- IoT, drones, printers, 3D printers
- Computer accessories and data hubs
- Accessories and battery-powered devices
- LED lighting and industrial
- Healthcare and handheld devices
- Any Type-C / PD sink device

Description

STUSB4531 addresses USB Type-C® sink devices. Based on default PDO configuration stored in an internal non-volatile memory, STUSB4531 implements proprietary algorithms to negotiate a power delivery contract with a source without any software support (autorun mode), making it the ideal device for automatic high power profile charging, especially from a dead battery power state.

STUSB4531 also implements a simple interface (hybrid mode) to support full feature applications with a light external software layer.

1 Functional description

The STUSB4531 is a USB Type-C and power delivery controller IC designed for sink applications.

The main functions of STUSB4531 are:

1. Detect the connection between two ports (attach detection)
2. Establish a valid Source-to-Sink connection
3. Determine the attached device mode: Sink or Debug Accessory Mode (oriented or not)
4. Resolve cable orientation and twist connections to establish USB data routing (mux control)
5. Negotiate a USB PD contract with a PD capable device
6. Configure the power input path accordingly
7. Monitor VBUS, manage transitions, handle protections.

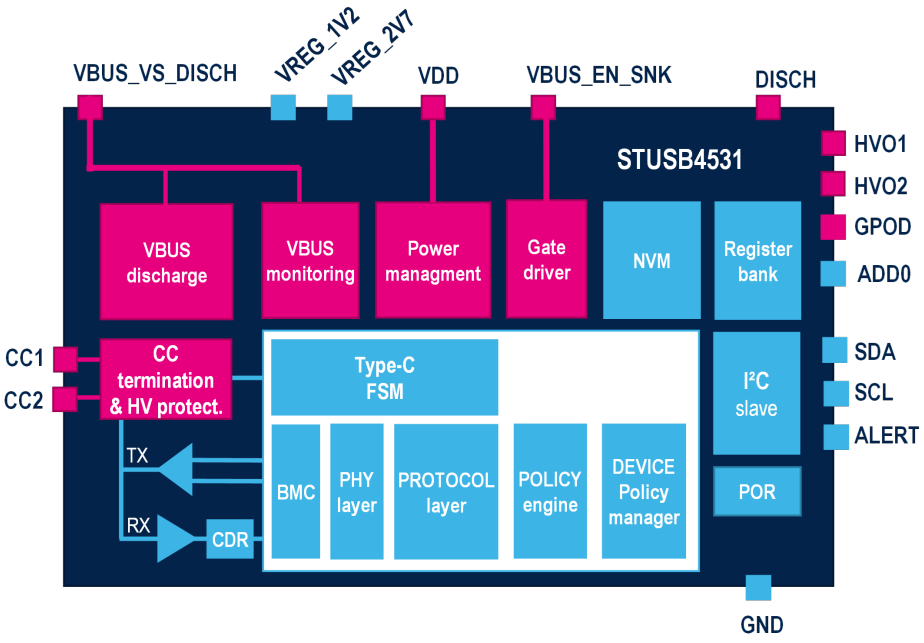
Additionally, STUSB4531 offers customizable Power Data Objects (PDO), an integrated discharge path and is natively robust to high-voltage surge, including on CC pins.

STUSB4531 addresses USB Type-C sink devices. Based on the default PDO configuration stored in an internal non-volatile memory, STUSB4531 implements proprietary algorithms to negotiate a power delivery contract with a source without any software support (Autorun mode), making it the ideal device for automatic high-power profile charging, especially from a dead battery power state. Additionally, STUSB4531 implements a simple interface to enable any kind of USB PD operation from an external MCU.

The product is available in 2 versions:

- with dead battery support to address battery/VBUS powered applications (STUSB4531QTR and STUSB4531BJR)
- without dead battery support to address externally powered applications (STUSB4531Q2TR)

Figure 1. Block diagram



2 Inputs/Outputs

2.1 Pinout

Figure 2. QFN-16 (3 x 3 mm) top view - not in scale

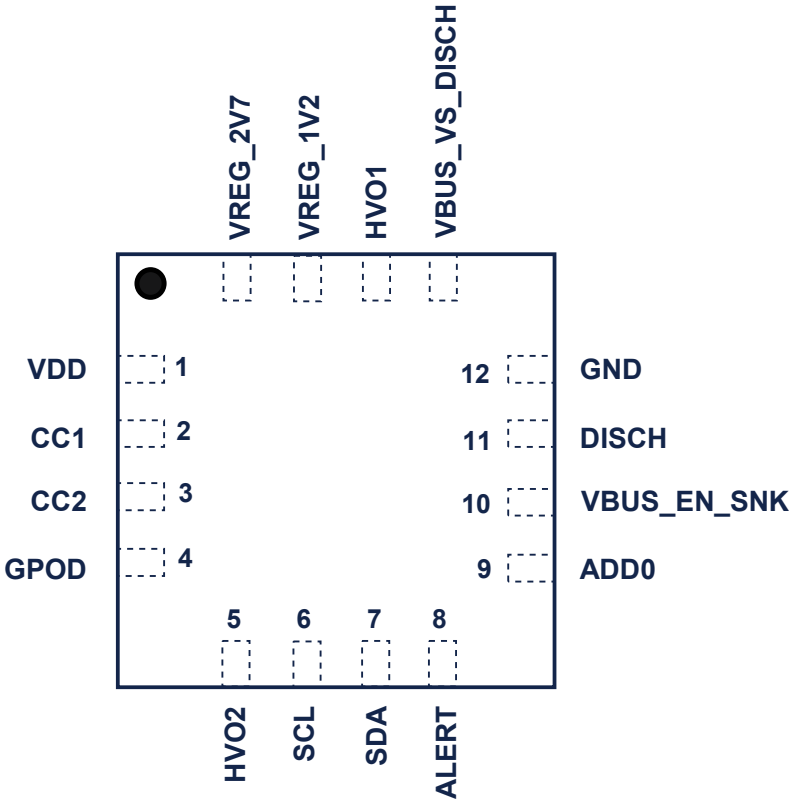
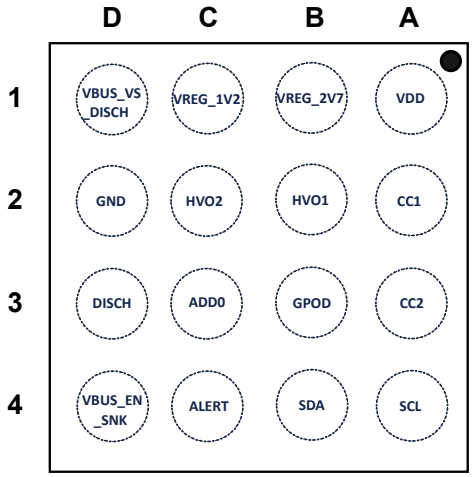


Figure 3. CSP-16 (2.3 x 2.3 mm) top view - not in scale



2.2 Pin list

Table 1. Detailed pin list (QFN and CSP)

QFN	CSP	Name	Type	Description	Typical connection
1	A1	VDD	High-voltage power	Main power supply (USB power line)	from V_{BUS}, receptacle side
2	A2	CC1	HV analog input	Type-C configuration channel 1	to Type-C receptacle A5
3	A3	CC2	HV analog input	Type-C configuration channel 2	to Type-C receptacle B5
4	B3	GPOD	HV open drain	General purpose output (open drain).	By default: POWER_OK4
5	C2	HVO2	HV open drain	High-voltage general output #2	Power contract flag, active low. By default: POWER_OK3
6	A4	SCL	Open drain	I^2C clock input	a) to I²C master – ext. pull-up b) to GND if not used
7	B4	SDA	Open drain	I^2C data input/output – active low open drain	a) to I²C master – ext. pull-up b) to GND if not used
8	C4	ALERT	Open drain	I^2C interrupt – active low open drain	a) to I²C master – ext. pull-up b) to GND if not used
9	C3	ADD0	Analog	I²C device address configuration	I²C address: 1) 0x28: Pull down to GND 2) 0x29: Pull up to VREG_2V7
10	D4	VBUS_EN_SNK	HV open drain	VBUS sink power path enable, active low	To power switch or to power system, ext. pull-up
11	D3	DISCH	HV open drain	Internal discharge path or external discharge path enable, active low	To power path (system side) or to the discharge path switch, ext. pull-up
12	D2	GND	Power	Ground	Ground
13	D1	VBUS_VS_DISCH	HV open drain	V_{BUS} voltage monitoring and discharge path	From V_{BUS}, receptacle side
14	B2	HVO1	HV open drain	High-voltage general output #1	Power contract flag, active low. By default: POWER_OK2
15	C1	VREG_1V2	Power	1.2 V internal regulator output	1 µF typ. decoupling capacitor
16	B1	VREG_2V7	Power	2.7 V internal regulator output	1 µF typ. decoupling capacitor

2.3 Pin description

2.3.1 VDD

This is the only power supply for the IC. It can be connected to VBUS from the USB Type-C receptacle, so that STUSB4531 is powered by VBUS.

2.3.2 GND

Ground.

2.3.3 CC1 / CC2

CC1 and CC2 are the configuration channel pins used for connection and attachment detection, plug orientation determination, USB power delivery communication, and system configuration management across USB Type-C cable.

Table 2. Dead battery and CC pins termination (QFN and CSP)

	Dead battery support	CC pin termination
STUSB4531BJR **STUSB4531QTR**	YES	always present (whatever VDD is powered or not)
STUSB4531Q2TR	NO	present only when VDD is powered CC1 and CC2 are HiZ when unpowered.

2.3.4 I²C interface pins

Table 3. I²C interface pin list

Name	Description
SCL	I²C clock, needs external pull-up
SDA	I²C data, needs external pull-up
ALERT	I²C interrupt, needs external pull-up

2.3.5 DISCH

This input/output pin can be used to implement a discharge path for a highly capacitive VBUS line on the power system side. When used as an input, the discharge is internal, and a serial resistor must be used to limit the discharge current through the pin. Maximum discharge current is 100 mA. The pin can also be used as an open drain output to control an external VBUS discharge path when a higher discharge current is required by the application, for instance. The pin is activated at the same time as the internal discharge path on VBUS_VS_DISCH pin. The discharge is activated automatically during cable disconnection, transition to a lower PDO voltage, hard reset, and error recovery state. The maximum discharge time is programmable by NVM (see Section 5: Startup configuration)

2.3.6 VBUS_EN_SNK

This pin handles the power path control and allows the incoming VBUS power (from the USB Type-C receptacle) to supply the application when a valid source is connected. The VBUS power path closure condition can be changed by NVM programming (see Section 3.6: VBUS power path and Section 5: Startup configuration).

2.3.7 VBUS_VS_DISCH

This input pin is used to sense VBUS presence, monitor VBUS voltage, and discharge VBUS from the USB Type-C receptacle side. A serial resistor must be used to limit the discharge current through the pin. Maximum discharge current is 50 mA. The discharge is activated automatically during cable disconnection, transition to a lower PDO voltage, hard reset, and error recovery state. The maximum discharge time is programmable by NVM (see Section 5: Startup configuration).

2.3.8 VREG_1V2

This pin is used for external decoupling of the 1.2 V internal regulator.

2.3.9 VREG_2V7

This pin is used for external decoupling of the 2.7 V internal regulator.

2.3.10 ADD0

ADD0 is latched at power-up to get the I²C ADDR0 of the device (see Section 4: I²C Interface).

2.3.11 General purpose I/O

GPOD

This pin is an active low high voltage open drain output that can be configured by NVM as per Table 4.
Depending on GPIO_CONF value, it can be used either as:
- MISMATCH : “Capability mismatch” bit (active low, set during USB PD negotiation)
- VCONN_CTRL1 : command to open or close external VCONN switch on the CC1 (active low)
- POWER_OK4 : explicit contract based on variable or PPS Sink PDO (active low)
- SW_GPOD : software driven output

HVO[2:1]

These pins are active low high voltage open drain general purpose outputs. Different configurations are proposed as stated in Table 4 to meet specific application requirements.
The configuration of the GPIO pins can be changed by NVM programming (see Table 4). Depending on the programmed configuration (GPIO_CONF), they can be used in combination with VBUS_EN_SNK pin to enable different power path scenarios.

Table 4. General purpose I/O pin configuration

NVM parameter GPIO_CONF[2:0]	Pin name	Value	Description
000b (conf 0)	GPOD = MISMATCH	Hi-Z	SOURCE capabilities offer enough power to the SINK
		0	SINK unable to fully operate at the offered capabilities
	HVO1 = VTRANS_WINDOW	Hi-Z	no ongoing power negotiation
		0	ongoing power negotiation
	HVO2 = ERROR_REC	Hi-Z	STUSB4531 is in normal operation
		0	STUSB4531 is in ErrorRecovery state
001b (conf 1)	GPOD = VCONN_CTRL1	Hi-Z	opens external CC1 VCONN switch
		0	closes external CC1 VCONN switch
	HVO1 = VTRANS_ WINDOW	Hi-Z	no ongoing power negotiation
		0	ongoing power negotiation
	HVO2 = VCONN_CTRL2	Hi-Z	opens external CC2 VCONN switch
		0	closes external CC2 VCONN switch
010b (conf 2)	GPOD = MISMATCH	Hi-Z	SOURCE capabilities offer enough power to the SINK
		0	SINK unable to fully operate at the offered capabilities
	HVO1 = POWER_OK2	Hi-Z	No PD explicit contract on fixed sink PDO2
		0	explicit contract based on fixed sink PDO2
	HVO2 = POWER_OK3	Hi-Z	No PD explicit contract on fixed sink PDO3
		0	explicit contract based on fixed sink PDO3

NVM parameter GPIO_CONF[2:0]	Pin name	Value	Description
011b (conf 3 - default)	GPOD = POWER_OK4	Hi-Z	No PD explicit contract on variable or APDO PPS PDO
		0	explicit contract based on variable or APDO PPS PDO
	HVO1 = POWER_OK2	Hi-Z	No PD explicit contract on fixed sink PDO2
		0	explicit contract based on fixed sink PDO2
	HVO2 = POWER_OK3	Hi-Z	No PD explicit contract on fixed sink PDO3
		0	explicit contract based on fixed sink PDO3
100b (conf 4)	GPOD = SW_GPOD	Hi-Z	Software controlled general purpose output (0x40 – bit 7)
		0	Software controlled general purpose output (0x40 – bit 7)
	HVO1 = POWER_OK2	Hi-Z	No PD explicit contract on fixed Sink PDO2
		0	explicit contract based on fixed Sink PDO2
	HVO2 = POWER_OK3	Hi-Z	No PD explicit contract on fixed Sink PDO3
		0	explicit contract based on fixed Sink PDO3

3 Main features description

3.1 Dead battery mode

Dead battery mode (STUSB4531QTR and STUSB4531BJR) allows battery-powered systems to charge in any battery condition. Being powered directly from the V_{BUS} receptacle pins, the IC can run independently from the application battery state of charge, even if it is fully depleted (SOC = 0%). Therefore, STUSB4531 is powered only when a source is connected and never draws current from the local battery, contributing to extended battery lifetime.

For STUSB4531QTR and STUSB4531BJR, dead battery mode is always operating. The STUSB4531 presents a pull-down termination on its CC pins and advertises itself as a sink even when the device is not supplied.

When a source system connects to a USB Type-C port with STUSB4531, it detects the pull-down termination, establishes the source-to-sink connection, and provides the VBUS. The STUSB4531 is then supplied through the VDD pin, connected to VBUS on the USB Type-C receptacle side.

The STUSB4531 can finalize the connection and enable the system power path thanks to the VBUS_EN_SNK pin, which allows the system to be powered.

By contrast, for STUSB4531Q2TR, dead battery mode is disabled, preventing correct biasing of sink termination if the IC is not already powered. This is the expected behavior for USB PD sink controllers in application that are externally powered. In this case, STUSB4531 is detected by SOURCES only when the application is powered, and not detected when the application is off.

3.2 CC pin interface

3.2.1 Functionality

The STUSB4531 controls the connection to the configuration channel (CC) pins, CC1 and CC2, through two main blocks: the CC line interface block and the CC control logic block.

The CC line interface block is used to:

- Set pull-down termination mode on the CC pins
- Monitor the CC pin voltage values related to the attachment detection thresholds
- Protect the CC pins against overvoltage

The CC control logic block is used to:

- Execute the Type-C FSM related to the sink power role with debug accessory support
- Determine the electrical state for each CC pin related to the detected thresholds
- Evaluate the conditions relative to the CC pin states and the VBUS voltage value to transition from one state to another in the Type-C FSM
- Advertise a valid source-to-sink connection
- Determine the attached device mode: source or debug accessory (oriented or not)
- Determine cable orientation to allow external routing of the USB data
- Report USB Type-C power capability on VBUS: USB default, medium, or high current mode
- Handle hardware faults

3.2.2 High-voltage protection

The STUSB4531 can be safely used in systems or connected to systems that handle high voltage on the VBUS power path. The device integrates an internal circuitry on the CC pins that tolerates high voltage and ensures protection up to 24 V in case of unexpected short-circuits with the VBUS.

3.3 Power delivery blocks

3.3.1 Physical layer (PHY)

The physical layer defines the signaling technology for USB power delivery. It is the physical link between CC pins and the protocol layer. In Tx mode, it receives packet data from the protocol layer, calculates and appends a CRC, encodes the payload (i.e. packet data and CRC), and transmits the packet (i.e. preamble, SOP*, payload, CRC and EOP) using biphase mark coding (i.e. BMC) over CC pins. In Rx mode, it recovers the clock and the data, detects the SOP*, decodes the received data including the CRC, detects the EOP, and validates the CRC.

3.3.2 Protocol layer (PRL)

The protocol layer has the responsibility to manage the messages from/to the physical layer. It automatically manages the protocol receiver timeouts, the message counter, the retry counter, and the GoodCRC messages. It communicates with the internal policy engine.

3.3.3 Policy engine (PE)

The policy engine implements the power negotiation with the connected device according to its sink role. It implements all state machines controlling the protocol layer that forms and schedules the messages. The policy engine uses the protocol layer to send/receive messages. The policy engine interprets the device policy manager's input to implement policy for port and directs the protocol layer to send appropriate messages.

3.3.4 Device policy manager (DPM)

The device policy manager deals with the power capability request and change management. It operates according to the decision algorithm described in Section 3.4: Autorun mode or according to Section 3.5: Hybrid mode.

3.4 Autorun mode

3.4.1 Overview

The STUSB4531 implements a configurable and hardcoded decision algorithm in the DPM allowing the device to negotiate autonomously a power delivery transaction with a source according to predefined power profiles called PDO (power data objects) configured in the NVM. It makes the STUSB4531 a plug-and-play, autonomous and effective solution to develop USB PD sink systems operating in standalone (ie. without external MCU support).

Additionally, STUSB4531 is also able to answer autonomously to any incoming mandatory message request using NVM default settings.

More complex power negotiation can also be managed with limited software support from the MCU. At any time, it is indeed possible to monitor, via a few I²C accesses, the status of standalone operations, the USB Type-C port, or the ongoing power negotiation. For instance, the MCU can ask STUSB4531 to collect source capabilities, overwrite default PDO settings, change negotiation algorithm parameters, or force STUSB4531 to renegotiate a power delivery contract according to new application requirements. With this limited external assistance, STUSB4531 handles incoming and outgoing messages autonomously, while still allowing dynamic application settings.

3.4.2 Power data objects (PDO) configuration

The STUSB4531 features up to 3 FIXED PDOs (1 minimum) + 1 optional VARIABLE PDO + 1 optional programmable power supply APDO or both:

- FIXED PDO can be used to support mandatory voltage nodes (9 V, 15 V, 20 V) or a custom voltage value.
- VARIABLE PDO is defined with MINIMUM and MAXIMUM voltage values (from 5 V to 20 V), and an OPERATING current (up to 5 A)
- PPS APDO is defined with MINIMUM and MAXIMUM voltage values (from 5 V to 21 V), and a MAXIMUM current (up to 5 A)

The number of fixed PDO, their value, and the selection of optional VARIABLE PDO or PPS APDO, and their respective value can be programmed in the non-volatile-memory and/or updated by software (volatile I²C registers). See Section 5: Startup configuration.

3.4.3 Power negotiation algorithm (AUTORUN)

The decision algorithm first compares the SOURCE maximum power delivery power (PDP) with the SINK PDP. The source PDP is calculated based on its highest voltage FIXED PDO profile. The result is used to set the MISMATCH bit in the RDO of the PDO requested.

Then, the algorithm compares the STUSB4531 PDOs (SNK_PDOi) with the PDO received from the source (SRC_PDOj). Table 5 summarizes the compatibility between SINK and SOURCE PDOs, depending on their type. For instance, a PPS negotiation is possible only when both SINK and SOURCE are compatible (support of PPS APDO respectively).

Table 5. SINK PDO interoperability with SOURCE PDO in autorun mode

PDO TYPES	FIXED PDO (SOURCE)	AVS APDO (SOURCE)	PPS APDO (SOURCE)	VARIABLE PDO (SOURCE)	BATTERY PDO (SOURCE)
FIXED PDO (SINK)	**yes**	**yes**	ignore	ignore	ignore
VARIABLE PDO (SINK)	**yes**	**yes**	ignore	ignore	ignore
PPS APDO (SINK)	ignore	ignore	**yes**	ignore	ignore

Note: PPS_APDO is not exposed in case of connection with a USB PD2.0 source.

Source PDOs marked as “ignore” are not considered by the STUSB4531 internal power negotiation algorithm. However, a more complex decision algorithm can still be implemented in software running on an external application MCU. This is possible by overwriting, before the end of the allocated time, the default PDO request message prepared by the STUSB4531 internal decision algorithm.

If a PPS APDO is available, the algorithm prioritizes a PPS contract (assuming SOURCE also supports PPS APDO) only if PPS_PRIORITY = 1. By default (PPS_PRIORITY = 0), the algorithm looks for an explicit contract with the highest power delivery power (PDP) based on all possible combinations of FIXED/VARIABLE PDOs comparisons. At equivalent PDP, the one with the highest voltage is selected. At identical conditions, an AVS contract is preferred to a FIXED contract.

a) Fixed PDO comparison (between SINK and SOURCE)

STUSB4531 FIXED PDO is compared by default with FIXED PDO from the SOURCE, starting from the highest voltage PDO to the lowest.

Voltage is compared first, current afterwards (ISINK = PDP/VSINK)

If VSOURCE = VSINK, the algorithm:

- stops if ISOURCE ≥ ISINK,
- stops if ISOURCE < ISINK and MISMATCH_PD is set to “Any current”,
- continues with a lower-priority PDO if ISOURCE < ISINK and MISMATCH_PD is set to “Enough current”.

 No PDO request is generated based on scanned PDO

When the algorithm stops on a given voltage node, an RDO (request data object) message is formed and sent to the source. If accepted, the source transitions to the matched PDO voltage and sends a PS_READY message to the sink, signaling the end of the power transition.

Table 6. Fixed PDO summary

V_{SOURCE}	I_{SOURCE}	MISMATCH_PD	REQUESTED CURRENT
= V_{SINK}	≥ I_{SINK}	do not care	I_{SINK}
	< I_{SINK}	= “Any current”	I_{SOURCE}
		= “Enough current”	No contract, next PDO

At the end of the comparison loop, if no match happens, the USB PD negotiation ends with an explicit USB PD contract: an RDO message is sent to the source on PDO1 with capability mismatch enabled, operating and maximum current set to source current.

b) Fixed PDO (SINK) comparison with AVS APDO (SOURCE)

STUSB4531 FIXED PDO(s) are by default compared with AVS APDO from the SOURCE, when available, and with FIXED PDO(s) from the SOURCE.

The algorithm looks for a compatible voltage, and if any, a compatible current. If both are met, a PDO request is made according to the table below. If one condition is missing, current PDOi is skipped, and the algorithm looks for a lower priority PDO.

Table 7. Fixed PDO with AVS APDO summary

RDO parameter	Condition / comment	Field value
VOLTAGE	$V\_FIX\_PDOi_{(SINK)} < 9$ V	no RDO; Skip to a lower priority SINK PDO
	$V\_FIX\_PDOi_{(SINK)} > V\_AVS\_max_{(SOURCE)}$	no RDO; Skip to a lower priority SINK PDO
	$V\_AVS\_min_{(SOURCE)} \le V\_FIX\_PDOi_{(SINK)} \le V\_AVS\_max_{(SOURCE)}$	$V_{REQ} = V\_FIX\_PDOi_{(SINK)}$
CURRENT	$I\_FIX\_PDOi_{(SINK)} \le I\_AVS_{(SOURCE)}$	$I_{OPERATING} = I\_FIX\_PDOi_{(SINK)}$ CAPA_MISMATCH = 0
	$I\_FIX\_PDOi_{(SINK)} > I\_AVS_{(SOURCE)}$ MISMATCH_PD = “Any current”	$I_{OPERATING} = I\_AVS_{(SOURCE)}$ CAPA_MISMATCH = 1
	$I\_FIX\_PDOi_{(SINK)} > I\_AVS_{(SOURCE)}$ MISMATCH_PD = “Enough current”	no RDO; Skip to a lower priority SINK PDO

c) VARIABLE_PDO (SINK) comparison with FIXED_PDO (SOURCE)

The algorithm also compares STUSB4531 VARIABLE PDO (when instantiated) with FIXED PDOi from the SOURCE, starting from the highest voltage PDO to the lowest.

The algorithm looks for a compatible voltage, and if any, a compatible current. If both are met, a PDO request is made according to the table below. If one condition is missing, the current PDO is skipped, and the algorithm looks for a lower priority PDO.

Table 8. Variable PDO with FIXED PDO summary

RDO parameter	Condition / comment	Field value
VOLTAGE	$V\_FIX\_PDOi_{(SOURCE)} > V\_VAR\_max_{(SINK)}$	no RDO; Skip to a lower priority SOURCE PDO
	$V\_FIX\_PDOi_{(SOURCE)} < V\_VAR\_min_{(SINK)}$	no RDO; Skip to a lower priority SOURCE PDO
	$V\_VAR\_min_{(SINK)} \le V\_FIX\_PDOi_{(SOURCE)} \le V\_VAR\_max_{(SINK)}$	$V_{REQ} = V\_FIX\_PDOi_{(SOURCE)}$
CURRENT	$I\_FIX\_PDOi_{(SOURCE)} \ge I\_VAR_{(SINK)}$	$I_{OPERATING} = I\_VAR_{(SINK)}$ CAPA_MISMATCH = 0
	$I\_FIX\_PDOi_{(SOURCE)} < I\_VAR_{(SINK)}$ MISMATCH_PD = “Any current”	$I_{OPERATING} = I\_FIX\_PDOi_{(SOURCE)}$ CAPA_MISMATCH = 1
	$I\_FIX\_PDOi_{(SOURCE)} < I\_VAR_{(SINK)}$ MISMATCH_PD = “Enough current”	Skip to a lower priority SOURCE PDO

d) VARIABLE_PDO (SINK) comparison with AVS_APDO (SOURCE)

VARIABLE PDO are compared by default with FIXED PDO from the SOURCE (see previous section), but also, when available, with AVS APDO from the SOURCE.

If PDP_{SOURCE} > PDP_{SINK}, the algorithm looks for a compatible voltage, and if any, a compatible current. If both are met, a PDO request is made according to the table below. If one condition is missing, the current PDO is skipped, and the algorithm looks for a lower priority PDO

Table 9. Variable PDO with AVS APDO summary

RDO parameter	Condition / comment	Field value
VOLTAGE	$V\_VAR\_max_{(SINK)}$ < 9 V	check fix SOURCE PDOs, otherwise skip to lower SINK PDO priority
	$V\_VAR\_min_{(SINK)}$ > $V\_AVS\_max_{(SOURCE)}$	Check SOURCE fixed PDO otherwise lower sink PDO priority
	$V\_VAR_{(SINK)}$ compatible with $V\_AVS_{(SOURCE)}$	V_{REQ} = Min ($V\_AVS\_max_{(SOURCE)}$; $V\_VAR\_max_{(SINK)}$)
CURRENT	$I\_VAR_{(SINK)} \leq I\_AVS_{(SOURCE)}$	$I_{OPERATING}$ = $I\_VAR_{(SINK)}$ CAPA_MISMATCH = 0
	$I\_VAR_{(SINK)}$ > $I\_AVS_{(SOURCE)}$ MISMATCH_PD = “Any current”	$I_{OPERATING}$ = $I\_AVS_{(SOURCE)}$ CAPA_MISMATCH = 1
	$I\_VAR_{(SINK)}$ > $I\_AVS_{(SOURCE)}$ MISMATCH_PD = “Enough current”	no RDO; Skip to a lower priority SINK PDO

e) PPS_APDO comparison (between SINK and SOURCE)

PPS negotiation has been introduced to enable ultra-fast battery charging based on custom algorithms. It relies on very fine grain voltage stepping (20 mV) and high current. Therefore, an advanced charging algorithm is implemented at the application processor level. STUSB4531 facilitates PPS negotiation by continuously repeating PPS requests according to standard requirements (ie, with a maximum period of 10 seconds) without any MCU specific action.

STUSB4531 PPS APDO is compared only with PPS APDO from the SOURCE. Other SOURCE PDO types are ignored.

An initial voltage is negotiated according to the PPS_VOLTAGE_SELECTION setting. If the SOURCE is compatible, a request is done automatically considering SOURCE and SINK PDPs. If no specific action is taken by the MCU, the request is repeated every 10 seconds maximum to maintain an active PPS connection (keep alive). At any time, the MCU can modify the voltage requirements up or down.

3.5 Hybrid mode

In this mode, the STUSB4531 shares policy engine (PE) and device policy manager (DPM) tasks with an external MCU. Both rely on the physical layer (PHY) and protocol layer (PRL) resources of the chip, significantly decreasing the software complexity from the user's standpoint. This mode requires average understanding of the USB PD protocol, and average software skills:

- STUSB4531 PE and DPM are used in autorun mode to handle the initial power delivery negotiation and guarantee effective system powering and boot. Extra features can then be managed by software with a stable power connection.

For every incoming message, STUSB4531 prepares an answer, and simultaneously, an interrupt is sent to the application MCU. The application software can then decide whether the default answer is appropriate or should be overridden with more relevant application information.

At the end of the allocated time, with or without MCU action, the answer (default or updated) is sent by STUSB4531 to the source, and so on, and so forth.

- Finally, any sequence can be initiated by using this mode.

With minimum software code, hybrid mode enables advanced users to implement the most advanced features defined by the standard seamlessly, without being a specialist of the protocol itself. Additionally, it saves MCU resources related to the implementation of the lower-level protocol layers, associated actions, and protections.

The detailed list of supported transmitted/received messages is available from a separate user manual. It describes the handling of control, data, extended data, and extended control messages, as well as VDM commands and reset signaling.

This mode is very effective for:

- Updating battery messages in real time
- Structured vendor define message support
- Alternate mode support
- Message support (non exhaustive list):
  - Get source capabilities
  - Get extended capabilities
  - Get manufacturer information
  - Get country codes / information
- PPS update requests
- Any request message

3.6 VBUS power path

3.6.1 VBUS assertion

The STUSB4531 controls the assertion of the VBUS power path from the USB Type-C receptacle, directly or indirectly, through the VBUS_EN_SNK pin.

To handle different application requirements, the following parameters are used to define the voltage and current condition in which the power path must be closed:

Table 10. Power path parameters

PARAMETER	FUNCTION
ABOVE_5V	Prevents VBUS switch from closing at USB Type-C attach in case 5 V is not supported by the application (MISMATCH_5V is then “don’t care”).
MISMATCH_5V	This parameter prevents the VBUS switch from closing if available current at 5 V is less than required by the application during the TypeC phase or if PDO1 is negotiated.
MISMATCH_PD	For PDO higher than PDO1, it allows to request a matching voltage profile even in case of current mismatch (if PDO is equal to PDO1, MISMATCH_5V condition applies instead of MISMATCH_PD).
PDO_0mA_MISMATCH	STUSB4531 opens the VBUS switch to limit sinking current (no load) when current offer from source is 0 mA.

The table below summarizes the operating conditions that determine the electrical value of the VBUS_EN_SNK pin, and therefore the closure of the VBUS switch (powering the system).

ABOVE_5V	MISMATCH_5V	Power path
0	0	Power path is closed at USB Type-C attach, whatever USB Type-C source current VBUS_EN_SNK = 0
	1	Power path is closed at USB Type-C attach if USB Type-C or PDO1 source current is equal or greater than PDO1 Sink current VBUS_EN_SNK = High Z if $I\_Rp_{(SOURCE)} < I\_FIX\_PDO1_{(SINK)}$ or $I\_FIX\_PDO1_{(SOURCE)} < I\_FIX\_PDO1_{(SINK)}$ VBUS_EN_SNK = 0 if I_Rp(SOURCE) ≥ $I\_FIX\_PDO1_{(SINK)}$ or $I\_FIX\_PDO1_{(SOURCE)} \geq I\_FIX\_PDO1_{(SINK)}$

ABOVE_5V	MISMATCH_5V	Power path
1	-	VBUS switch does not close with a source USB Type-C only, or for a USB PD source before an explicit contract and if PDO1 is negotiated. VBUS_EN_SNK = High Z

At the end of USB Type-C operations (Attach detection), the VBUS switch can be either closed (default) or open (application not managing 5 V or only with a minimum amount of current). See Figure 4.

USB PD negotiation between the SOURCE and STUSB4531 is then starting and may close VBUS_EN_SNK (if not closed during USB Type-C operation according to negotiation results). See Figure 5

Figure 4. USB Type-C connection flow chart

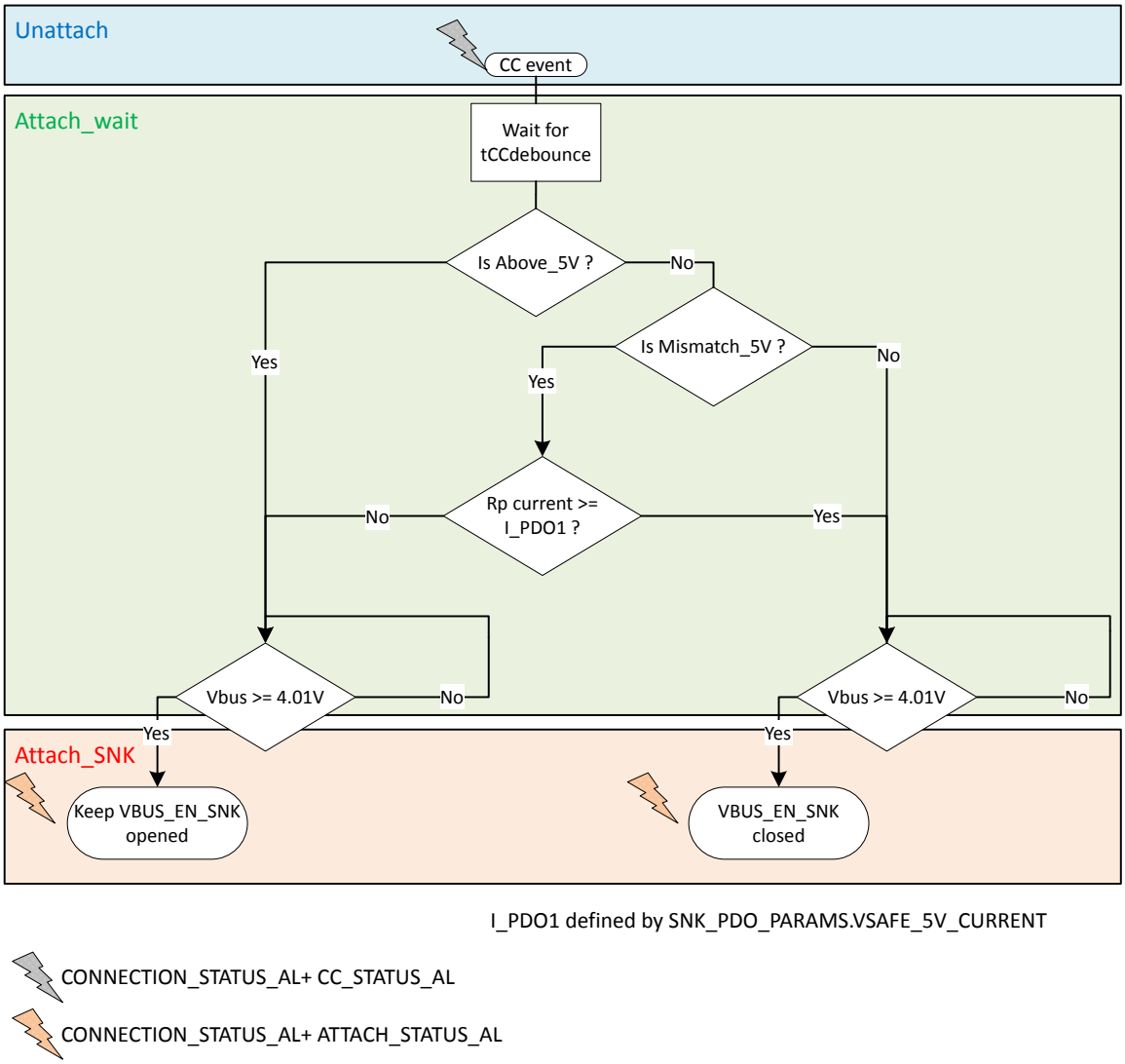
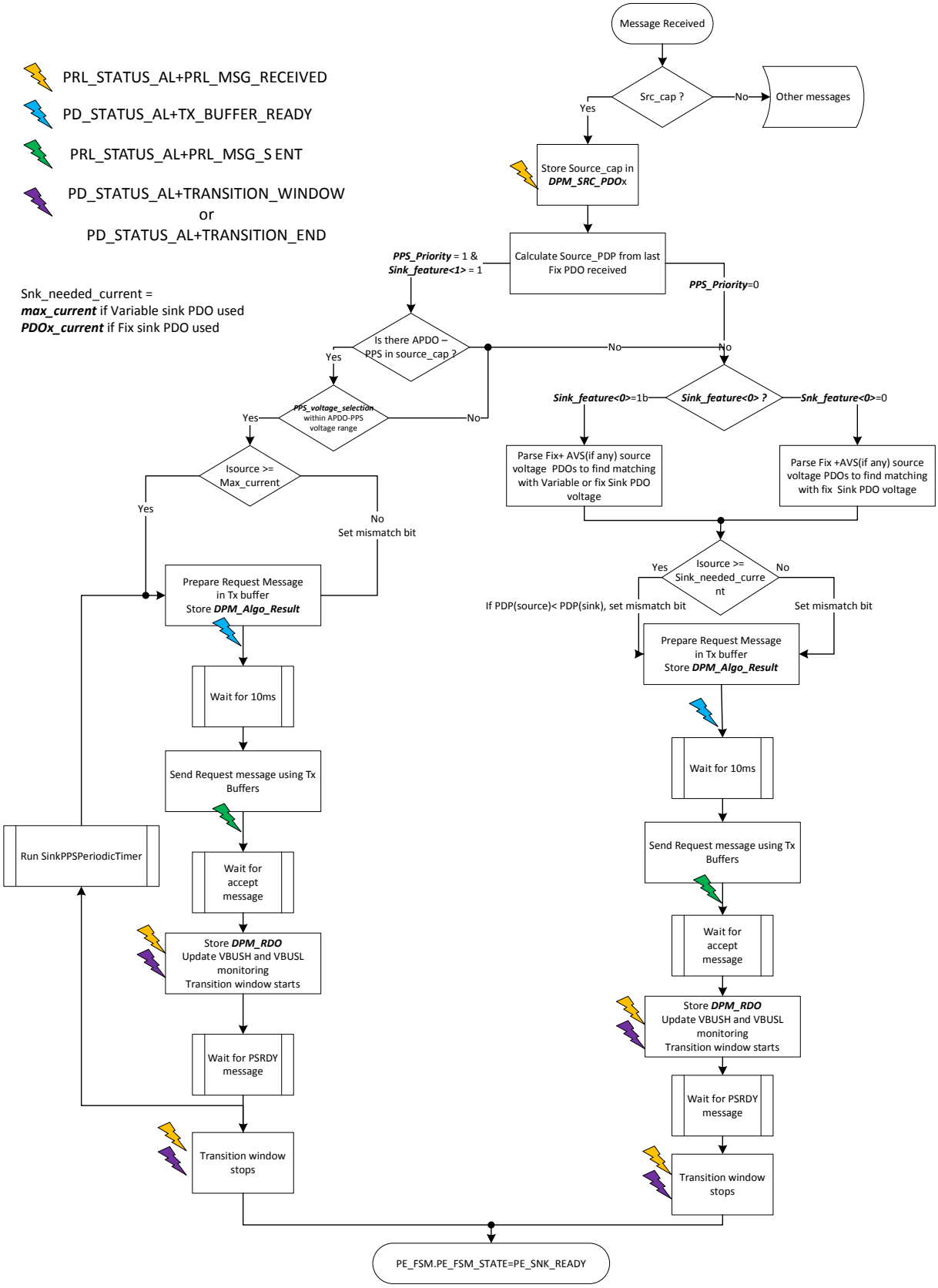


Figure 5. USB-PD power negotiation flow chart



3.6.2 VBUS monitoring

This monitoring block supervises the VBUS voltage from the VBUS_VS_DISCH input pin (the USB Type-C receptacle side). It is used to check that VBUS is within a valid voltage range to establish a valid source-to-sink connection and to safely enable the VBUS power path through the VBUS_EN_SNK pin.

It detects unexpected VBUS voltage conditions such as undervoltage or overvoltage relative to the negotiated VBUS voltage.

When such conditions occur, the STUSB4531 reacts as follows:

- At attachment, it prevents the source-to-sink connection to be established and the VBUS power path to be asserted

- After attachment, it disables the VBUS power path, protecting the application and goes into unattached state or ErrorRecovery state.

The valid VBUS voltage range is defined by a low limit VTH_LOW and a high limit V_{TH_HIGH}. Those limits depend on system operation and VBUS negotiated voltage (V_{RDO}). As per USBPD standard, source dispersion on voltage VPDO_SRC is ±5%. Additionally, specific rules apply to the disconnection thresholds (according to “USB Type-C cable and connector specification). Finally, user-defined derating factors can be adjusted to fit application specific requirements: MONITORING_SHIFT_LOW (MSL) and MONITORING_SHIFT_HIGH (MSH) (see default value in Section 5: Startup configuration).

Table 11 clarifies the low and high VBUS monitoring thresholds settings according to all these parameters.

Table 11. VBUS monitoring low and high thresholds definition

STATE	VBUS Voltage (V_{RDO})	V_{TH_LOW}	V_{TH_HIGH}
ATTACHED	= 5 V	V_{TH_LOW-5V}	min((V_{RDO} x 1.05) x MSH; 5.9 V)
ATTACHED (non PPS RDO)	> 5 V	(V_{RDO} x 0.95 – 1.25 V) x MSL	min((V_{RDO} x 1.05) x MSH; 23 V)
ATTACHED (PPS RDO)	> 5 V	(V_{RDO} x 0.95 – 0.85 V) x MSL	

Note: STUSB4531 implements active VBUS monitoring during high and low voltage transitions, according to USB PD source transition behavior (as defined by the standard).

3.6.3 VBUS discharge

The monitoring block also handles discharge connected to Type-C receptacle (VBUS_VS_DISCH pin) and on system side (DISCH pin).

The discharge paths are activated at the time that a disconnection is detected, during transition to a lower PDO voltage, when a hard reset is performed or when the device enters the error recovery state (see Section 3.7: Hardware fault management).

Although discharge times are preset by default (see Section 7.1: Electrical and timing characteristics), it can also be adjusted through NVM programming:

- At detachment, during error recovery state or hard reset, the discharge is activated for maximum DISCHARGE_TIME_TO_0V time (665 ms by default)

- During transition to a lower PDO voltage, the discharge is activated for DISCHARGE_TIME_TRANS time maximum (350 ms by default).

3.7 Hardware fault management

During system operations, the STUSB4531 handles some preidentified hardware fault conditions. When such conditions happen, the circuit goes into ErrorRecovery.

The error recovery state is equivalent to forcing a detach event. When entering this state, the device de-asserts the VBUS power path by disabling VBUS_EN_SNK, HVO1, HVO2 and GPOD, and removing the terminations from the CC pins during 275 ms (as long as $V_{VBUS\_VS\_DISCH} > V_{TH\_LOW-5V}$). Then, it transitions to the unattached state.

The STUSB4531 goes into error recovery state when at least one condition listed below is met:

- Internal overtemperature (junction temperature exceeds maximum T_J)
- Overvoltage detected on one CC pin (voltage on CC pins above V_{OVP})
- Overvoltage detected on VBUS
- After a hard reset, when power delivery communication with the source cannot be re-established despite multiple tentatives.

3.8 Thermal shutdown

STUSB4531 thermal shutdown is set to 125 °C. In case the IC internal temperature is reaching such a high level, STUSB4531 goes to Error_Recovery, and VBUS_EN_SINK is de-asserted.

To prevent such extreme conditions, a warning threshold is set to 105 °C (increasing internal temperature). If it is reached, interrupt is generated. For MCU based applications, it is recommended to take corrective action to reduce the temperature. A 15 °C hysteresis applies to resume operation (warning is released when the internal temperature decreases below 90 °C).

A new connection is not possible when the temperature is inside the warning window.

4 I²C Interface

4.1 Read and write operations

STUSB4531 implements a Fast-mode Plus I²C slave interface for high-speed Read/Write accesses (1 MHz). All data bytes are transmitted with the most significant bit first. It implements Automatic IDLE mode to save power.

The default I²C address is 0x28 or 0x29. Address selection is triggered at power-up by reading the ADD0 pin value. To guarantee proper initialization, the pin should be set as follows:

Table 12. Default I²C address

I²C address	ADD0 connection	Resistor value (R_{ADD0})
0x28	Pull-down to GND	0 to 47 kOhms
0x29	Pull-up to VREG_2V7	0 to 47 kOhms

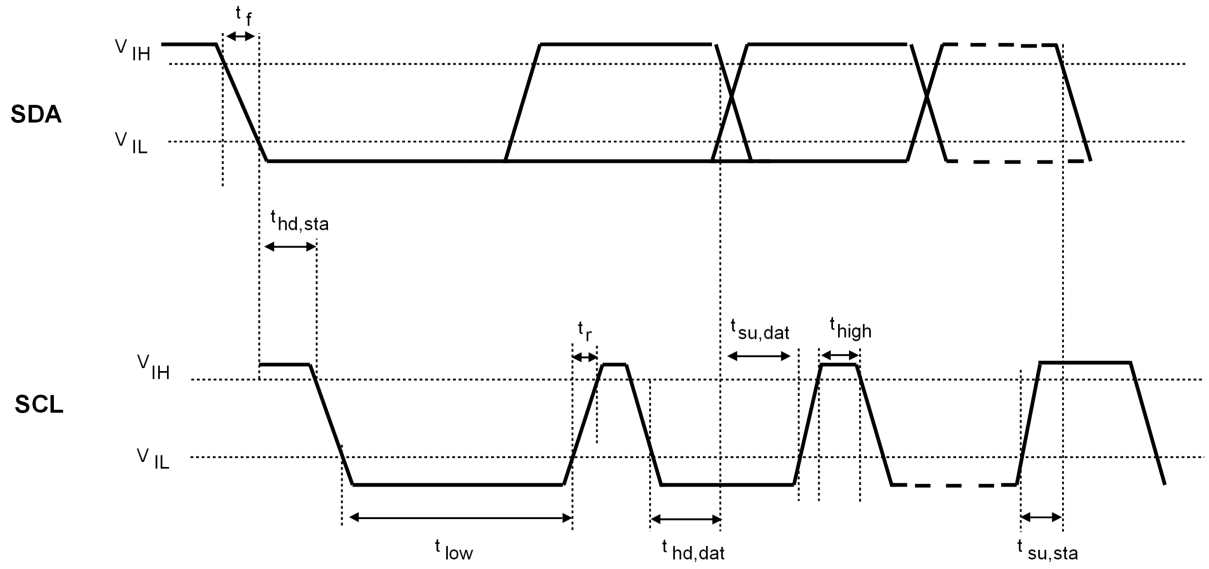
4.2 Timing specifications

Table 13. I²C timing for V_{I2C} = [1.7; 4.8 V]

		Fast mode (1)		Fast mode plus (1)		
Symbol	**Parameter**	**Min (2)**	**Max**	**Min (2)**	**Max.**	**Unit**
F_{SCL}	SCL clock frequency		400	-	1000	kHz
t_{LOW}	LOW period of the SCL clock	1.3	-	0.50	-	µs
t_{HIGH}	HIGH period of the SCL clock	0.6	-	0.26	-	
$t_{HD;STA}$	Hold time (repeated) START condition	0.6	-	0.26	-	
$t_{SU;STA}$	Setup time for repeated START condition	0.6	-	0.26	-	
$t_{SU;STO}$	Set-up time for STOP condition	0.6	-	0.26	-	
t_{BUF}	Bus free time between a STOP and START condition START condition	1.3	-	0.50	-	
$t_{HD;DAT}$	Data hold time	0	-	0	-	
$t_{SU;DAT}$	Data setup time	100	-	50	-	
$t_{VD;DAT}$	Data valid time	-	0.9	-	0.45	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	0.9	-	0.45	µs
tr	Rise time of both SDA and SCL signals	-	300	-	120	ns
tf	Fall time of both SDA and SCL signals	-	300	-	120	
Cb	Capacitive load for each bus line	-	400	-	550	pF

1. *ALL timings have been evaluated by characterization at [-40 °C; 105 °C]*
2. *MIN timings tested in production at T_{amb} = 25 °C*

Figure 6. I²C timing diagram



NB: Measurement points are done at V_{IL}=0.3*V_{I2C} and V_{IH}=0.7*V_{I2C}

5 Startup configuration

5.1 User-defined parameters

The STUSB4531 provides a set of user-defined parameters that can be customized by NVM reprogramming through a dedicated I²C sequence. This feature allows users to change the default configuration of the IC to meet specific application requirements and to address various use cases or specific implementations.

NVM reprogramming overwrites the initial factory settings, defining a new default configuration that is loaded at each power-up. This default setting is copied at each power-up from the embedded NVM into the I²C registers. Only the values copied in the I²C registers are used by the STUSB4531 during system operation. Therefore, new settings defined during NVM reprogramming are not effective until the next power-off and power-up sequence.

The list of customizable parameters is described in the tables below.

Table 14. PDO configuration

Parameter	Description	Possible values	Values description
DEVICE_PDP	Power delivery minimum power	8 bits (from 0 W to 100 W)	Contains the minimum power required by the Sink to operate at its functional modes. Expressed in steps of 0.5 Watt (LSB ignored for PDP greater than 10 W)
SINK_FEATURE	Sink PDO type selection: define the mix of PDO used	2b00: Fixed only	Only fixed PDO is used
		2b01: Fixed + VARIABLE	Fixed PDOs + 1 variable PDO
		2b10: Fixed + PPS	Fixed PDOs + 1 Programmable power supply augmented PDO (PPS APDO)
		2b11: Fixed + VARIABLE + PPS	Fixed PDOs + 1 variable PDO + 1 PPS APDO
FIXED_PDO_NUMB	Number of sink fixed PDO	2b00: 0	1 Sink fixed PDO
		2b01: 1	1 Sink fixed PDO
		2b10: 2	2 Sink fixed PDO
		2b11: 3	3 Sink fixed PDO
VSAFE_5V_CURRENT	PDO1 current (5 V)	2b00: Default	Clamped to 500 mA
		2b01: 1.5 A	Clamped to 1.5 A
		2b10: 3 A	Clamped to 3 A
		2b11: PDP/5	Clamped to 5 A
PDO2_VSEL	Fixed sink PDO2 voltage	2b00: VSEL_VAR	Custom voltage value
		2b01: 9 V	Fixed 9 V
		2b10: 15 V	Fixed 15 V
		2b11: 20 V	Fixed 20 V
FIXED_PDO2_CURRENT	Fixed sink PDO2 current clamp	1b0: clamped to 3 A	= PDP/FIXED_PDO2_VOLTAGE (3 A Max)
		1b1: clamped to 5 A	= PDP/FIXED_PDO2_VOLTAGE (5 A Max)
PDO3_VSEL	Fixed sink PDO3 voltage	2b00: VSEL_VAR	Custom value
		2b01: 9 V	Fixed 9 V
		2b10: 15 V	Fixed 15 V
		2b11: 20 V	Fixed 20 V
FIXED_PDO3_CURRENT	Fixed sink PDO3 current clamp	1b0: clamped to 3 A	= PDP/FIXED_PDO3_VOLTAGE (3 A Max)
		1b1: clamped to 5 A	= PDP/FIXED_PDO3_VOLTAGE (5 A Max)

Parameter	Description	Possible values	Values description
VSEL_VAR	Custom voltage value for PDO2_VSEL or PDO3_VSEL and PPS_VOLTAGE_SELECTION	10 bits	Custom voltage value (by steps of 50 mV)
APDO_MAX_VOLTAGE	VARIABLE and PPS maximum voltage field	8 bits	in 100 mV steps
APDO_MIN_VOLTAGE	VARIABLE and PPS Minimum voltage field	8 bits	in 100 mV steps
APDO_MAX_CURRENT	VARIABLE and PPS current field	7 bits	in 50 mA steps
SINK_MAX_PDP	Sink maximum PDP in sink capabilities extended message	2b00: DEVICE_PDP	DEVICE_PDP value
		2b01: 16 W	Expected source voltages: 5 V + 9 V
		2b10: 28 W	Expected source voltages: 5 V + 9 V + 15 V + AVS
		2b11: 46 W	Expected source voltages: 5 V + 9 V + 15 V + 20 V + AVS
SINK_OP_PDP	Sink operating PDP in sink capabilities extended message	2b00: DEVICE_PDP	DEVICE_PDP value
		2b01: 16 W	Expected source voltages: 5 V + 9 V
		2b10: 28 W	Expected source voltages: 5 V + 9 V + 15 V + AVS
		2b11: 46 W	Expected source voltages: 5 V + 9 V + 15 V + 20 V + AVS
SINK_MIN_PDP	Sink minimum PDP in sink capabilities extended message	2b00: DEVICE_PDP	DEVICE_PDP value
		2b01: 16 W	Expected source voltages: 5 V + 9 V
		2b10: 28 W	Expected source voltages: 5 V + 9 V + 15 V + AVS
		2b11: 46 W	Expected source voltages: 5 V + 9 V + 15 V + 20 V + AVS
MONITORING_SHIFT_LOW	VBUS monitoring: low-voltage threshold derating factor	2b00: 0.95	vSinkPD_Min threshold derated by -5%
		2b01: 0.90	vSinkPD_Min threshold derated by -10%
		2b10: 0.85	vSinkPD_Min threshold derated by -15%
		2b11: 1.00	vSinkPD_Min
MONITORING_SHIFT_HIGH	VBUS monitoring: high-voltage threshold derating factor	2b00: 1.10	V_{TH_HIGH} set to V_{RDO} x 1.05 x 1.10
		2b01: 1.15	V_{TH_HIGH} set to V_{RDO} x 1.05 x 1.15
		2b10: 1.20	V_{TH_HIGH} set to V_{RDO} x 1.05 x 1.20
		2b11: reserved	Do not use

Table 15. Autorun algorithm parameters and power path management

Parameter	Description	Possible values	Values description
ABOVE_5V	Controls VBUS path assertion at 5 V	1b0: no	5 V is supported by the application: At USB Type-C attach, VBUS switch closes according to MISMATCH_5V condition
		1b1: yes	5 V is not supported by the application: At USB Type-C attach, VBUS switch does not close. In USB PD mode, VBUS_EN_SNK is not closed if 5 V is requested
MISMATCH_5V	Defines current needed for closing the VBUS switch in 5 V operation (USB Type-C and PDO1), assuming ABOVE_5V = 0	1b0: Any current	At USB Type-C connection, power path is closed whatever Type-C source current
		1b1: Enough current	At USB Type-C connection, power path is closed if Type-C source current is equal or greater than PDO1 sink current. During USB PD negotiation, power path is closed on PDO1 contract if PDO1 source current is equal or greater than PDO1 sink current
MISMATCH_PD	Defines USB PD algorithm behavior when comparing source current to sink current	1b0: Enough current	SOURCE PDO is skipped if proposed current is lower than SINK requirements
		1b1: Any current	SOURCE PDO is selected whatever current capability
PDO_0mA_MISMATCH	Defines USB PD algorithm behavior when 0 mA PDO negotiated with SOURCE	1b0: System operated	No load condition is managed by the system
		1b1: Default	STUSB4531 manages no load condition (Suspend_Mode) by opening VBUS power path
OPERATING_CURRENT_SEL	In case a PDO is selected, defines operating current field from RDO	1b0: SINK	Operating current = calculated through the algorithm Maximum current = Operating current
		1b1: SOURCE	Operating current = SOURCE current Maximum current = SOURCE current
PPS_PRIORITY	Defines the order in which the sink PDOs must be compared with the source PDOs	1b0: High priority to fixed/ variable	Priority to FIXED/ VARIABLE PDO, then to PPS APDO
		1b1: High priority to PPS	Priority to PPS APDO, then to FIXED/ VARIABLE PDO.
PPS_VOLTAGE_SELECTION	PPS voltage value used by the algorithm	2b00: Min	APDO_MIN_VOLTAGE is used
		2b01: Mid	Mean of APDO_MIN_VOLTAGE and APDO_MAX_VOLTAGE
		2b10: Max	APDO_MAX_VOLTAGE is used
		2b11: VSEL_VAR	VSEL_VAR is used

Table 16. **Application specific parameters**

Parameter	Description	Possible values	Values description
BATTERY_PRESENT	Application implements a battery	1b0: No	No battery in application
		1b1: yes	Battery in application
BATTERY_SWAP	Indicates if battery can be removed or not	1b0: No	Fixed battery
		1b1: Yes	Swappable battery
HIGHER_CAPABILITY	PDO1 higher capability bit	1b0: No	Sink is fully functional at vSafe5V.
		1b1: Yes	In the case the Sink needs more than vSafe5V (e.g., 15 V) to provide full functionality, then the higher capability bit shall be set.
UNCONS_POWER	Unconstrainted power	1b0: No	No external power supply or power supply is not always able to sustain system functionality
		1b1: Yes	An external power supply is available and is sufficient to adequately power the system while charging external devices
USB_COMM_CAPABLE	USB2.0 or 3.x data capable	1b0: No	Application does not support USB data communication
		1b1: Yes	Application implements USB data controller
DRD_CAPABLE	Dual role data support	1b0: No	Single role only (UFP - Peripheral)
		1b1: Yes	Dual role data capable (UFP and DFP - Peripheral and host)
DR_SWAP_2_UFP	Data role swap to UFP support	1b0: Disabled	Data role swap to UFP is rejected
		1b1: Enabled	Data role swap to UFP can be accepted
DR_SWAP_2_DFP	Data role swap to DFP support	1b0: Disabled	Data role swap to DFP is rejected
		1b1: Enabled	Data role swap to DFP can be accepted
VDM_SUPPORT	Indicated if vendor defined message is supported by the application	1b0: No	Incoming VDM message requests are discarded
		1b1: yes	Incoming VDM message requests are supported
VBUS_CTRL_LOW_MASK	V_{TH_LOW} threshold bypass	1b0: No	V_{TH_LOW} info is not masked to VBUS switch control
		1b1: Yes	V_{TH_LOW} info is masked to VBUS switch control
VCONN_EN	V_{CONN} supply ENABLE	1b0: Disabled	V_{CONN} is disabled
		1b1: Enabled	V_{CONN} is supplied (see Table 4: GPIO – conf 1)
VCONN_SWAPP_2_ON	Support of VCONN SWAP to ON	1b0: Disabled	VCONN_SWAPP_2_ON is rejected
		1b1: Enabled	VCONN_SWAPP_2_ON can be accepted
VCONN_SWAPP_2_OFF	Support of VCONN SWAP to OFF	1b0: Disabled	VCONN_SWAPP_2_OFF is rejected
		1b1: Enabled	VCONN_SWAPP_2_OFF can be accepted
GPIO_CONF	GPIO pin selection	3b000: Conf 0	Recommended for current transition management
		3b001: Conf 1	Recommended for external VCONN support
		3b010: Conf 2	Recommended for POWER_OK support
		3b011: Conf 3	Recommended for extended POWER_OK support
		3b100: Conf 4	Recommended for software controlled GPIO

Parameter	Description	Possible values	Values description
DISCHARGE_TIME_TO_0V	Maximum VBUS discharge time to 0 V	5b10010: 665 ms (default)	Discharge time (max.): (DISCHARGE_TIME_TO_0V + 1) x 35 ms
DISCHARGE_TIME_TRANS	Maximum VBUS discharge time to lower voltage	3b111: 350 ms (default)	Discharge time (max.): (DISCHARGE_TIME_TRANS + 3) x 35 ms

5.2 Factory settings

Table 17. **Power profiles**

Parameter	Description
DEVICE_PDP	30 W
SINK_FEATURE	Fixed PDO + VARIABLE PDO
SNK_PDO_NUMB	3
VSAFE_5V_CURRENT	3 A
FIXED_PDO2_VOLTAGE	9 V
FIXED_PDO2_CURRENT	Clamped to 3 A
FIXED_PDO3_VOLTAGE	15 V
FIXED_PDO3_CURRENT	Clamped to 5 A
VSEL_VAR	12 V
APDO_MIN_VOLTAGE	9 V
APDO_MAX_VOLTAGE	20 V
APDO_MAX_CURRENT	1.5 A
SINK_MAX_PDP	Device PDP
SINK_OP_PDP	Device PDP
SINK_MIN_PDP	Device PDP
MONITORING_SHIFT_LOW	-5%
MONITORING_SHIFT_HIGH	+10%

Summary

- PDO1 - FIXED 5 V; 3 A
- PDO2 - FIXED 9 V; 3 A
- PDO3 - FIXED 15 V; 2 A
- PDO4 - VARIABLE [9 V - 20 V; 1.5 A]

Table 18. **Autorun algorithm**

Parameter	Description
ABOVE_5V	no
MISMATCH_5V	any current
MISMATCH_PD	Enough current
PDO_0mA_mismatch	Default
OPERATING_CURRENT_SEL	SINK
PPS_PRIORITY	Priority to PPS APDO (if used) then to FIXED/VARIABLE PDO
PPS_VOLTAGE_SELECTION	Maximum AVS/PPS operating voltage

Table 19. **Application specific**

Parameter	Description
BATTERY_PRESENT	No battery
BATTERY_SWAP	NO
HIGHER_CAPABILITY	NO
UNCONS_POWER	NO – (STUSB4531QTR / STUSB4531BJR) YES – (STUSB4531Q2TR)
USB_COMM_CAPABLE	NO
DRD_CAPABLE	NO
DR_SWAP_2_UFP	Disabled
DR_SWAP_2_DFP	Disabled
VDM_SUPPORT	NO
VBUS_CTRL_LOW_MASK	unmasked
VCONN_EN	Disabled
VCONN_SWAPP_2_ON	Disabled
VCONN_SWAPP_2_OFF	Disabled
GPIO_CONF	Conf 3 (POWER_OK2, POWER_OK3, POWER_OK4)
DISCHARGE_TIME_TO_0V	665 ms
DISCHARGE_TIME_TRANS	350 ms

Table 20. **Interrupts masks (ALERT pin)**

Parameter	Field	Initial value	Description
STATUS_MASK	**CONNECTION_STATUS_AL_MASK**	1b1	CONNECTION_STATUS alert is masked
	NVM_DOWNLOADED_AL	1b1	NVM_DOWNLOADED alert is masked
	CC_STATUS_AL_MASK	1b1	CC_STATUS alert is masked
	ATTACH_STATUS_AL_MASK	1b1	ATTACH_STATUS alert is masked
	PD_STATUS_AL_MASK	1b1	PD_STATUS alert is masked
	PRL_STATUS_AL_MASK	1b1	PRL_STATUS alert is masked
	MONITORING_STATUS	1b1	MONITORING_STATUS alert is masked
STATUS_EVENT_MASK	**TX_BUFFER_READY_MASK**	1b1	TX_BUFFER_READY event is masked
	AMS_STOPPED_MASK	1b1	AMS_STOPPED event is masked
	TRANSITION_END_MASK	1b1	TRANSITION_END event is masked
	TRANSITION_WINDOW_MASK	1b1	TRANSITION_WINDOW event is masked

Table 21. **Product identification**

Parameter	Description	Possible values	Factory settings
VID	Vendor ID (16 bits)	VID_7_0	0x83
		VID_15_8	0x04
PID	Product ID (16 bits)	PID_7_0	0x31
		PID_15_8	0x45
XID	provided by the USB-IF to the vendor who in turns assigns it to a product. If the vendor does not have an XID, then it shall return zero in this field	XID_7_0	0x00
		XID_15_8	0x00
		XID_23_16	0x00
		XID_31_24	0x00
HW_VERSION	Hardware version (8 bits)	HW_VERSION_7_0	0x10
PD_REVISION	Power delivery revision (8 bits)	PD_REV_MAJ_7_0	0x32
PD_VERSION	Power delivery version (8 bits)	PD_VER_MAJ 7_0	0x11

6 Applications

The sections below are not part of ST product specification. It is intended to give a generic application overview to be used by the customer as a starting point for further implementation and customization. ST does not warrant compliance with customer specification. Full system implementation and validation are under customer responsibility.

6.1 General information

6.1.1 Power supplies

STUSB4531 is powered by VDD pin, connected to VBUS (from USB Type-C connector and before the switch). It addresses the following classes of applications:

- Use case 1: VBUS powered applications (no battery or external supply)
- Use case 2: Battery-powered applications (removable)
- Use case 3: Fixed battery applications (non-removable)

Use case 4: no dead battery support

Table 22. Recommended application specific parameters settings

USE CASE	BATTERY_PRESENT	BATTERY_SWAP	UNCONS_POWER
#1: VBUS powered	NO	NO	NO
#2: Battery powered (removable)	YES	YES	NO
#3: fixed battery	YES	NO	NO
#4: externally powered	NO	NO	YES

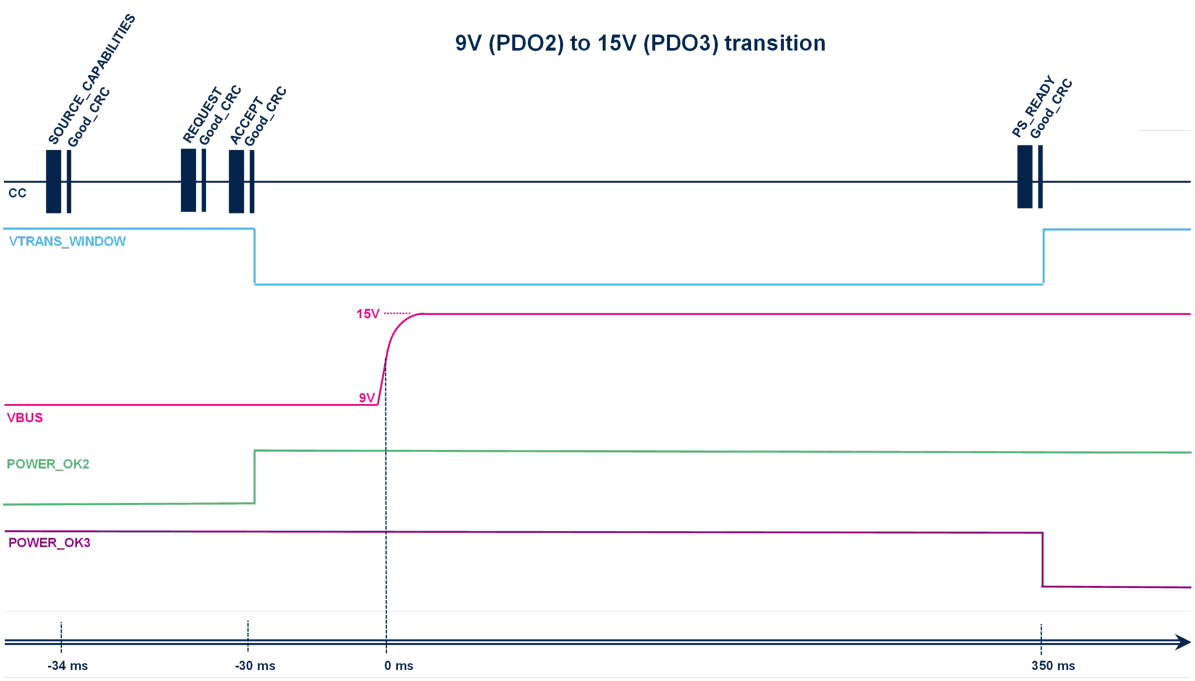
Note:
- *use cases #1, #2, #3 are supported by STUSB4531QTR / STUSB4531BJR*
- *use case #4 is supported by STUSB4531Q2TR (no dead battery)*

6.1.2 Powering a system under high charging profile

According to the USB PD standard, any USB sink application is expected to limit sink current to 500 mA max during power transition. **VTRANS_WINDOW** signal can be used by the system to limit current consumption on VBUS during voltage transition (**VTRANS_WINDOW** asserted).

See Figure 7 timing diagram for a typical 9 V to 15 V voltage transition (from sink PDO2 to sink PDO3).

Figure 7. **Voltage transition timing diagram**



6.1.3 Connection to MCU or application processor

The STUSB4531 can run as a standalone USB PD sink controller: in this case, IC behavior is fully defined through custom parameters stored in Non-Volatile-Memory. Connection to an MCU or an application processor is optional.

When the application hosts a microcontroller or an application processor, the I²C interface can be used to provide additional flexibility and/or additional functionality during system operations. For instance, it may be used to:

1. Define the port configuration during system boot (in case NVM parameters are not customized during manufacturing),
2. Provide real-time diagnostic of the Type-C connection,
3. Dynamically update the power configuration based on contextual application requirements, source profile information, or fine-grain charging optimization,
4. Overwrite the STUSB4531 default answer to specific messaging sequences,
5. Support, by software, specific messaging sequences, which cannot be fully supported in autorun mode (such as alternate mode transitions or vendor define messaging),
6. Etc…

At power-up, access to I²C registers is limited during t_{LOAD}, which corresponds to the time required to initialize the I²C registers with the default values from the embedded NVM. At the end of t_{LOAD}, an interrupt is generated **(NVM_DOWNLOADED_AL)**.

Figure 8. **I²C registers initialization sequence**

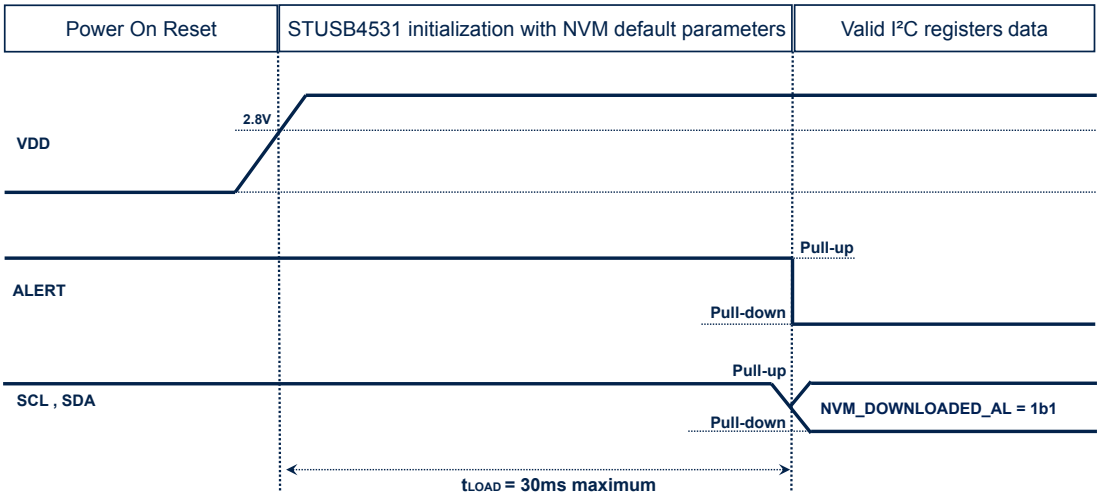


Figure 9. **Minimum implementation (autorun mode)**

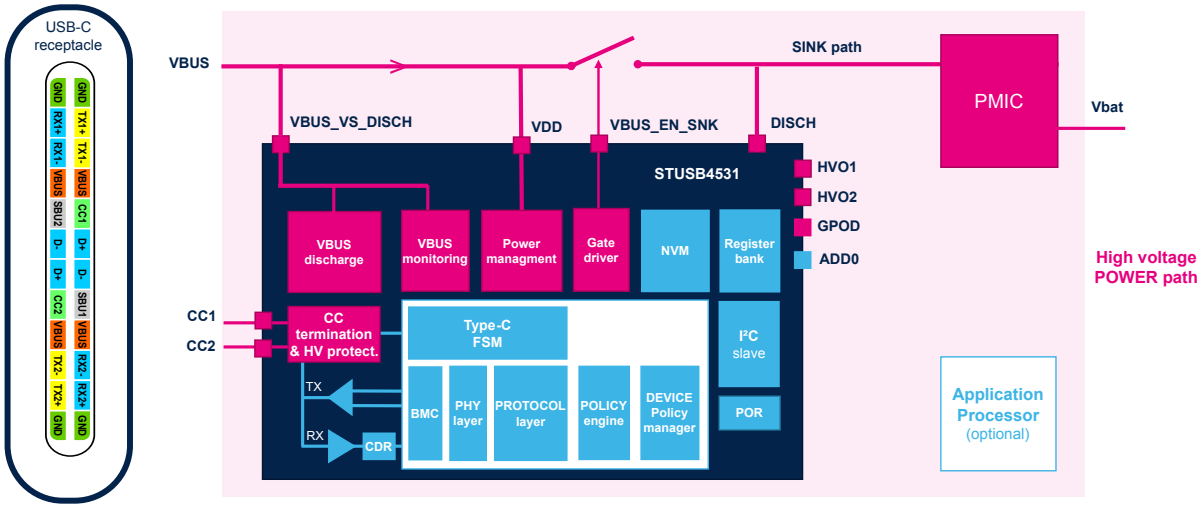


Figure 10. **Typical application (hybrid mode)**

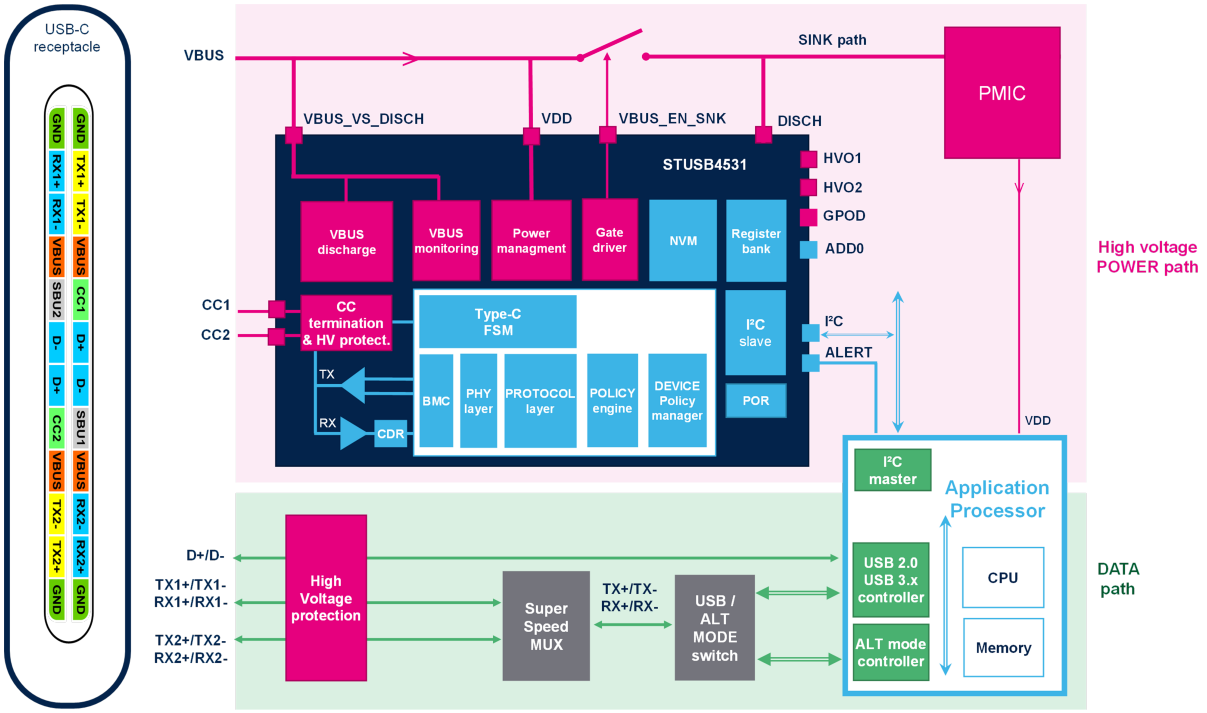
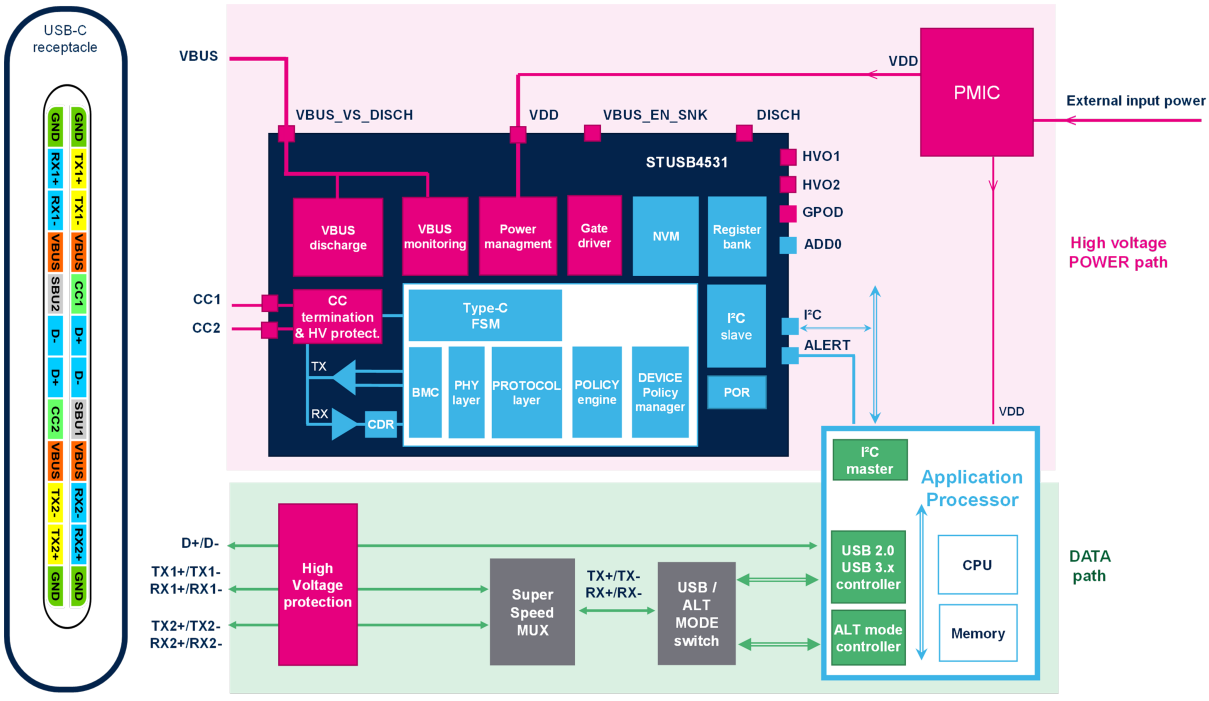


Figure 11. **Externally powered application (no dead battery support)**



7 Electrical characteristics

Table 23. Absolute maximum rating

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.3 to 28	V
V_{CC1}, V_{CC2}	High voltage on CC pins	-0.3 to 24	V
V_{DISCH} $V_{VBUS\_EN\_SNK}$ $V_{VBUS\_VS\_DISCH}$ $V_{HVO[2.1]}$ V_{GPOD}	High voltage pins	-0.3 to 28	V
V_{SCL}, V_{SDA} V_{ALERT}	I²C interface pins	-0.3 to 4.8	V
V_{ADD0}	I²C interface address setting	-0.3 to 4.8	V
T_{STG}	Storage temperature	-55 to 150	°C
T_J	Maximum junction temperature	145	°C
ESD	HBM	4	kV
	CDM	1	

Note:
- *All voltages are referenced to GND.*
- *Stresses above the absolute maximum ratings listed in Table 23 may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.*

Table 24. Operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	3.3 to 23	V
V_{CC1}, V_{CC2}	CC pins (1)	0 to 5.5	V
V_{DISCH} $V_{VBUS\_EN\_SNK}$ $V_{VBUS\_VS\_DISCH}$ $V_{HVO[2.1]}$ V_{GPOD}	High voltage pins	0 to 23	V
V_{SCL}, V_{SDA} V_{ALERT}	I²C interface pins (V_{I2C})	1.7 to 4.8	V
V_{ADD0}	I²C interface address setting	0 to VREG_2V7	V
T_A	Operating ambient temperature	-40 to 105	°C
T_J	Operating junction temperature	-40 to 125	°C

1. *Transient voltage on CC1 and CC2 pins are allowed to go down to -0.3 during BMC communication from connected devices.*

7.1 Electrical and timing characteristics

Table 25. Electrical and timing characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD						
V_{VDD_UVLO}	V_{DD} UVLO threshold	Rising			2.80	V
		Falling	2.65			
		Hysteresis		0.15		
$I_{VDD\_UNATTACH}$	Standby current consumption	UNATTACHED (Device standby) V_{DD}= 5 V, VBUS = 0 V, T_A = +25 °C		45	55	µA
$I_{VDD\_ATTACHED}$	Operating current consumption	ATTACHED.SINK (PD explicit) V_{DD} = 5 V, V_{BUS}= 5 V, T_A = + 25 °C V_{DD} = 5 V, V_{BUS} = 20 V, T_A = + 25 °C		495 550	550 620	µA
Internal LDO (VREG_1V2 and VREG_2V7)						
C_{VREG_1V2}	1.2 V LDO decoupling capacitor		-30%	1	+30%	µF
C_{VREG_2V7}	2.7 V LDO decoupling capacitor		-30%	1	+30%	µF
CC1 and CC2						
R_d	CC pull-down	After internal NVM is loaded	-10%	5.1	+10%	kΩ
R_{INCC}	input impedance	Terminations off	200			kΩ
$C_{receiver}$	CC receiver sensitivity	external capacitor on CC line	200		600	pF
$V_{THOVP-CC}$	Overvoltage protection threshold		5.8		6.2	V
VBUS_VS_DISCH						
$I_{DISVBUS}$	VBUS discharge current	Through external resistor connected to VBUS_VS_DISCH pin			50	mA
$Z_{VBUS\_VS\_DISCH}$	Input impedance	Discharge = disabled		1.8		MΩ
V_{TH_LOW-5V}	VBUS disconnection threshold for VBUS = 5 V			2.9	3.1	V
V_{TH_LOW-PD}	VBUS disconnection threshold for VBUS > 5 V			V_{TH_LOW}	+2%	V
$V_{TH\_HIGH-5V}$	VBUS monitoring High-voltage threshold	Valid at 5 V	-2%	V_{TH_HIGH}	+2%	V
$V_{TH\_HIGH-PD}$	VBUS monitoring High-voltage threshold	Valid if VBUS > 5 V	-2%	V_{TH_HIGH}	+2%	V
DISCH						
I_{DISSYS}	Power system discharge current	Through external resistor connected to DISCH pin			100	mA
I²C interface + interrupt (ADD0, SCL, SDA, ALERT)						
V_{I2C}	I²C bus voltage		1.7		4.8	V
R_{ADD0}	Pull-down resistor to GND Pull-up resistor to VREG_2V7	I²C address = 0x28 I²C address = 0x29	47			kΩ
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.35	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage	Ioh = 3 mA			0.40	V
HV open drain outputs (GPOD, HVO[2:1])						
V_{OL}	Low-level output voltage	Ioh = 3 mA			0.40	V
I_{IL}	Leakage current				1	µA
I_{OD}	Maximum current				150	mA
VBUS_EN_SNK						
V_{OL}	Low-level output voltage	Ioh = 3 mA			0.40	V
I_{IL} (1)	Leakage current				1	µA
I_{OD} (1)	Maximum current				150	mA
t_{OVP_VBUS}	VBUS over voltage protection response time	VBUS = 5 V (crossing $V_{TH\_HIGH-5V}$)		2.5		µs
		VBUS > 5 V (crossing $V_{TH\_HIGH-PD}$)		6		
Thermal shutdown						
$TH_{SHUTDOWN}$ (1)	Junction temperature shutdown threshold	rising	125			°C
TH_{WARN} (1)	Junction temperature warning threshold	rising	105			°C
TH_{HYST} (1)	Hysteresis			15		°C
Non-volatile memory (NVM)						
t_{LOAD}	I²C register loading time (from NVM)	At power-up (V_{DD} > V_{VDD_UVLO})			30	ms
T_{RET}	Retention time	T_A = 25 °C T_A = 105 °C	25 10			years
Cycling	Write cycles endurance	T_A = 105 °C			1000	cycles

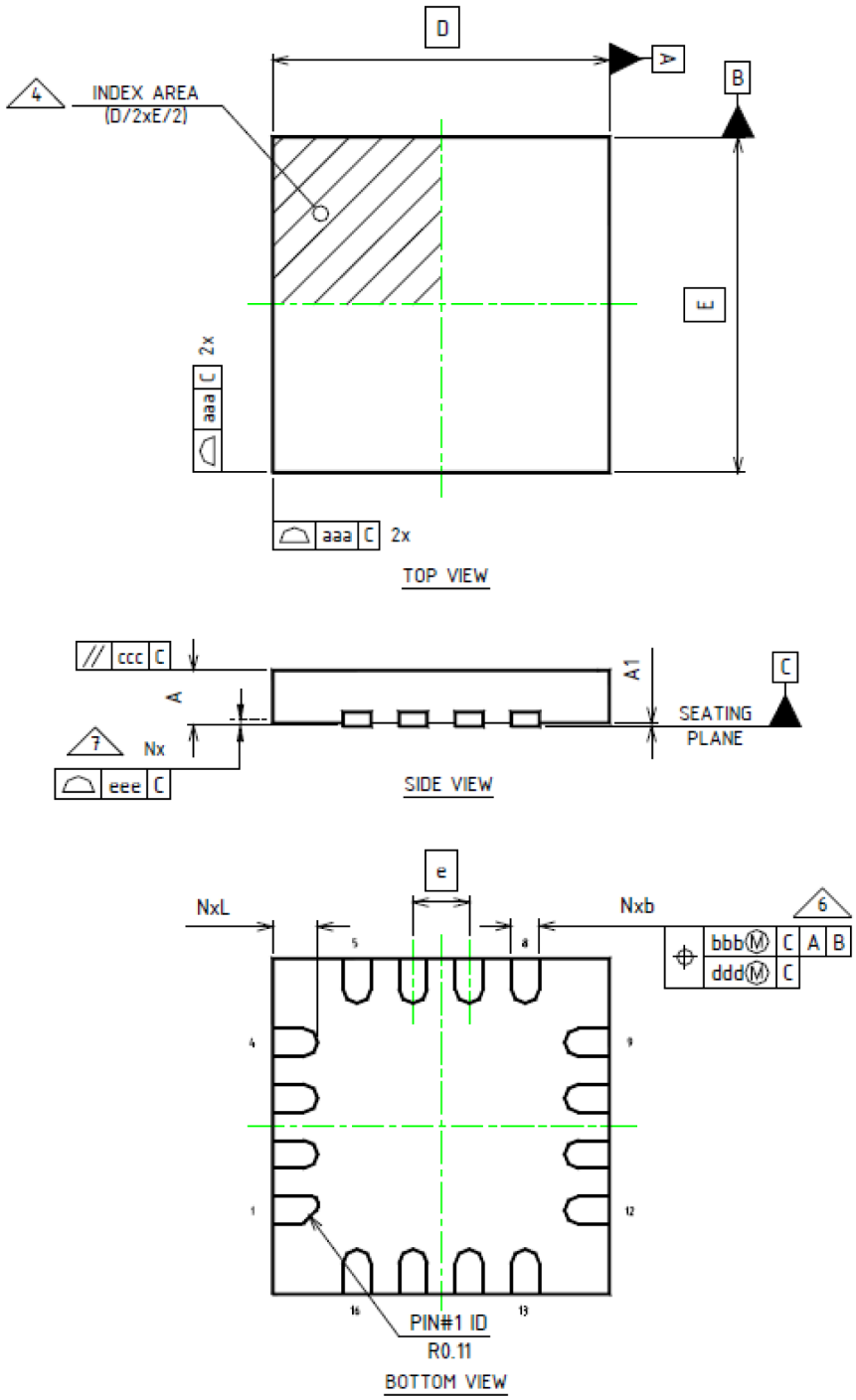
1. *Guaranteed by design/characterization, not tested in production.*

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

8.1 QFN-16 (3x3 mm), pitch 0.50 package information

Figure 12. **QFN-16 (3x3 mm) package outline**



Note:
- *Nxb means N pads with b width*
- *NxL means N pads with L length*

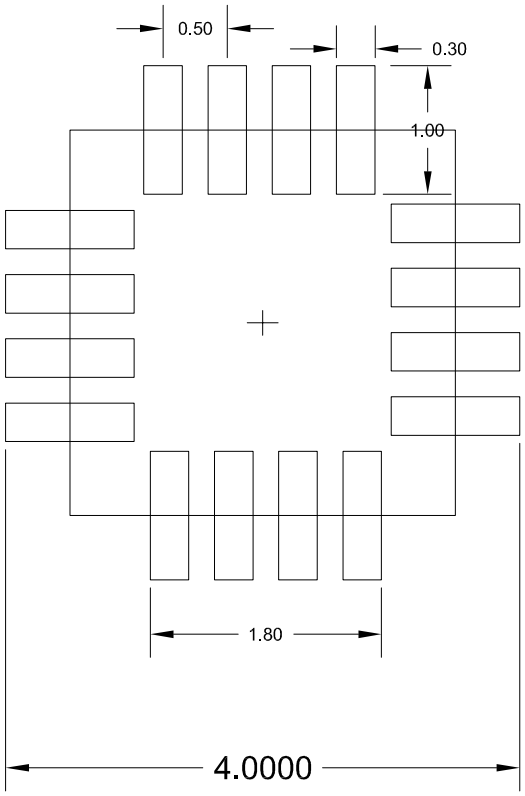
Table 26. **QFN-16 (3x3 mm) mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A	0.5		0.65
A1	0		0.05
b	0.18	0.25	0.30
D		3.00 bsc	
E		3.00 bsc	
e		0.50	
L	0.40	0.50	0.60
aaa			0.15
bbb			0.10
ccc			0.10
ddd			0.05
eee			0.08
n		16	
nD		4	
nE		4	

Note:

1. *N is the total number of terminals*
2. *nD and nE refer to the number of terminals on D and E side respectively*
3. *Dimensions b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured on that radius area*

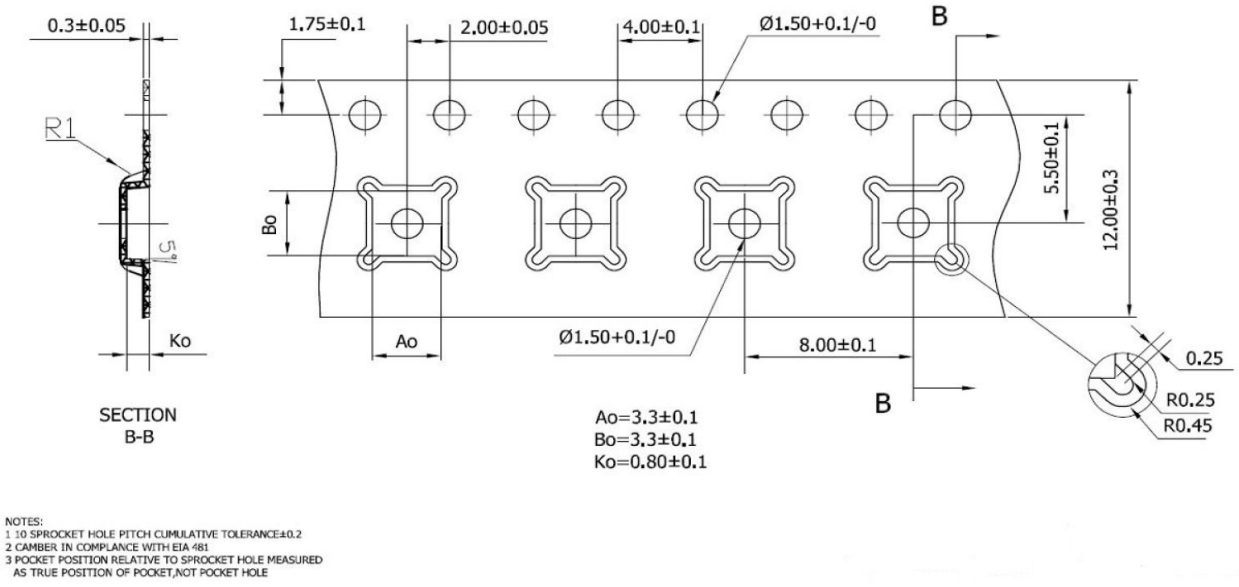
Figure 13. **QFN-16 (3x3 mm) recommended footprint**



8.2 QFN-16 (3x3 mm) packing information

According to “EIA 481-A” and “IEC 286-3” standard.

Figure 14. Drawing carrier tape for QFN 3x3 mm



NOTES:
1 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE±0.2
2 CAMBER IN COMPLIANCE WITH EIA 481
3 POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET,NOT POCKET HOLE

8.3 CSP-16 (2.3x2.3 mm²) - pitch 0.40 package information

Figure 15. **CSP-16 (2.3x2.3 mm²) package outline**

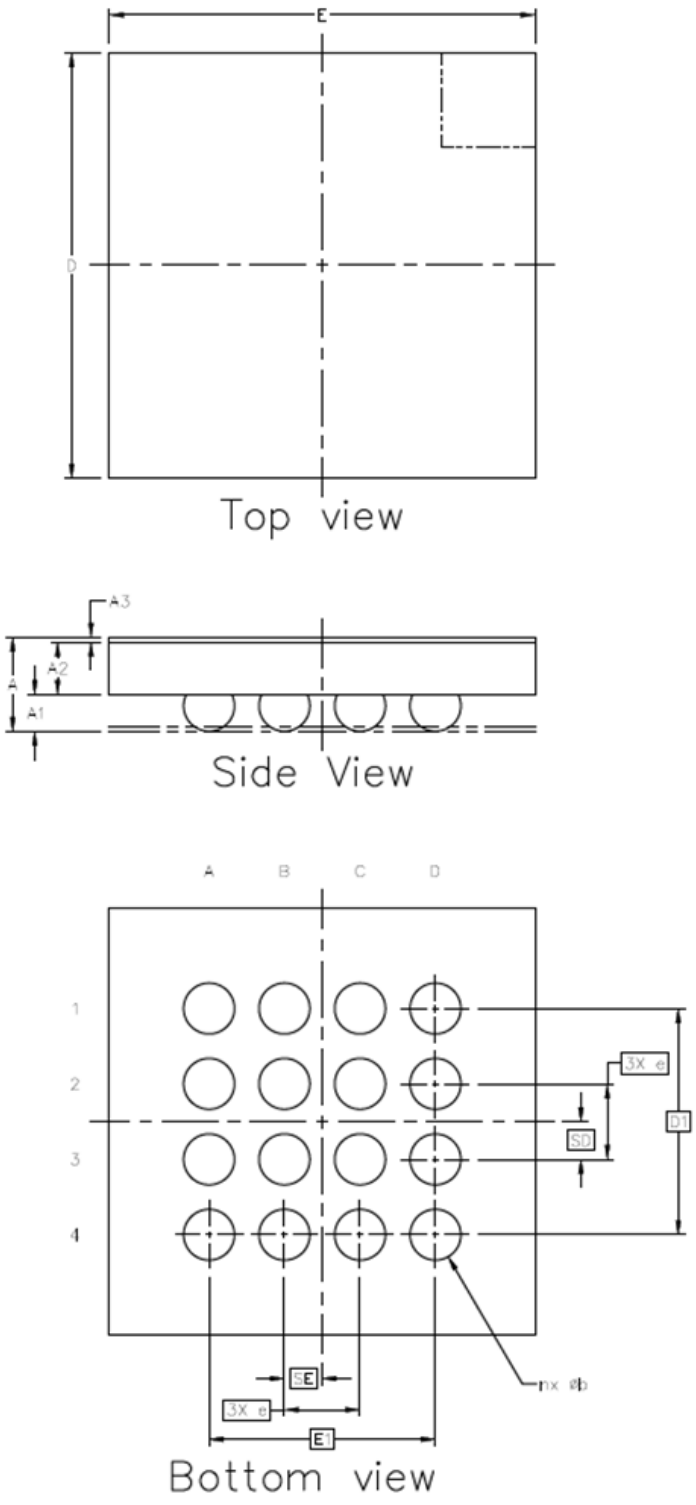
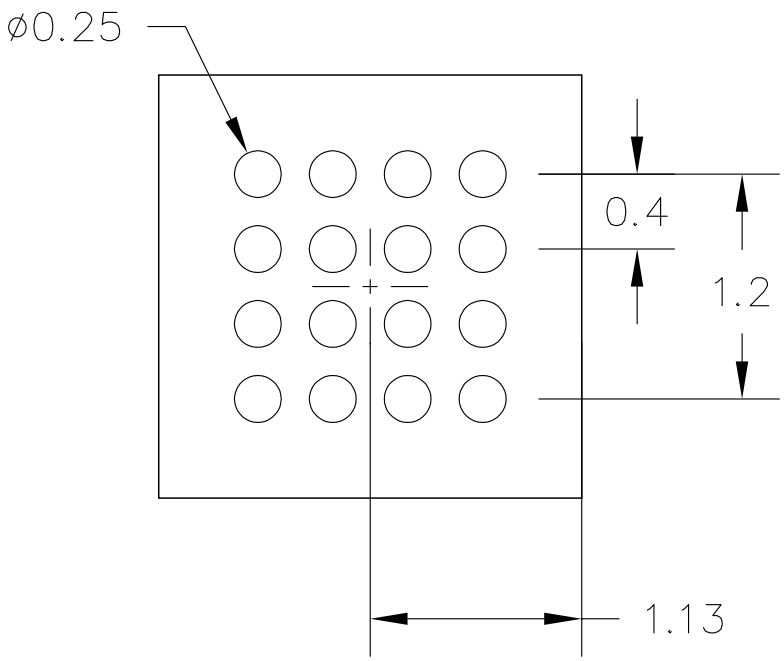


Table 27. **CSP-16 (2.3x2.3 mm²) package mechanical data**

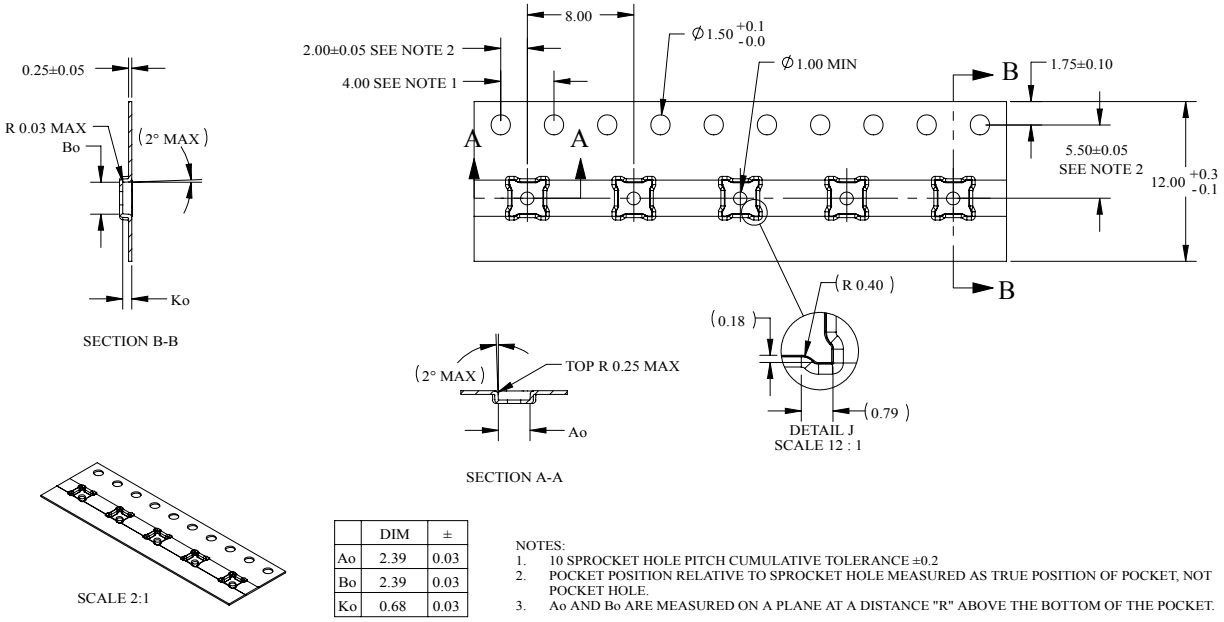
Symbol	mm		
	Min.	Typ.	Max.
A	0.456	0.50	0.544
A1	0.179		0.211
A2	0.255	0.28	0.305
A3	0.022	0.025	0.028
E		2.2575	
D		2.2575	
SE		0.2 BSC	
SD		0.2 BSC	
E1		1.2 BSC	
D1		1.2 BSC	
e		0.4 BSC	
b	0.24		0.3
n		16	

Figure 16. **CSP-16 (2.3x2.3 mm²) recommended footprint**



8.4 CSP-16 (2.3 x 2.3) packing information

Figure 17. **Carrier tape for CSP-16 (2.3 x 2.3 mm²) package outline**



	DIM	±
Ao	2.39	0.03
Bo	2.39	0.03
Ko	0.68	0.03

NOTES:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3. Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

8.5 Thermal information

Table 28. **Thermal information**

Symbol	Parameter	Value	Unit
QFN-16 3x3			
$R_{\theta JA}$	Junction to ambient thermal resistance	78	°C/W
$R_{\theta JC}$	Junction to case thermal resistance	30	
CSP-16 2.3x2.3			
$R_{\theta JA}$	Junction to ambient thermal resistance	50	°C/W
$R_{\theta JC}$	Junction to case thermal resistance	25	

9 Ordering Information

Table 29. **Order codes**

CP	Description	Package	Marking
STUSB4531BJR	Standalone USB PD SINK controller (with dead battery support)	CSP-16 (2.3 x 2.3 mm)	4531
STUSB4531QTR		QFN-16 (3x3 mm)	4531
STUSB4531Q2TR	Standalone USB PD SINK controller (externally powered application)	QFN-16 (3x3 mm)	5531

Revision history

Table 30. **Document revision history**

Date	Revision	Changes
08-Oct-2025	1	Initial release.

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