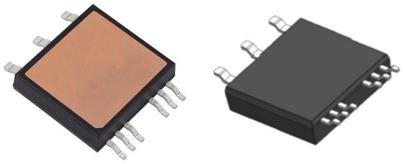
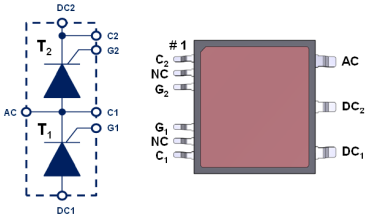
STTN6050H-12M1Y

Datasheet

60 A 1200 V thyristor controlled bridge leg in ACEPACK SMIT module



ACEPACK SMIT



ACEPACK SMIT
top view

Prerelease product(s)

Product status
STTN6050H-12M1Y

Product summary	
$I_{T(RMS)}$	60 A
$I_{OUT(AV)}$	75 A
$I_{IN\_AC(RMS)}$	85 A
V_{DRM}/V_{RRM}	1200 V
V_{DSM}/V_{RSM}	1400 V
I_{GT}	50 mA
T_j	-40 to +150 °C

Features

- AEC-Q101 qualified
- 1200 V symmetrical blocking voltage
- High junction temperature: 150 °C
- High noise immunity, static dV/dt: 1000 V/µs
- Embed two TN6050HP-12 dies in series
- Module qualified according to AQG324 recommendation
- SMD with isolated top cooled tab
- 4000 V insulated tab-to-lead package
  - UL recognized, File E81734
- Terminal pins opposite to cooling side
  - Fully automatic PCB mounting to heat sink
- Large creepage distance to meet IEC 60664-1
  - 250 V_{AC}, material group 2, pollution degree 3
  - 600 V_{AC}, material group 2, pollution degree 2
- ECOPACK2 compliant component

Applications

- Single and tri-phase controlled rectifier bridge
- AC phasing half bridge of a totem pole PFC
- On-board and stationary chargers
- AC / DC converter for motor drive, UPS and SMPS
- Output full wave DC current up to 75 A_{AV}
- AC Input converter current up to 85 A_{RMS}
- Solid-state relay in heating control, by pass switch and motor starter

Description

The STTN6050H-12M1Y achieves a 1200 V 60 A full controlled SCR bridge leg in ACEPACK SMIT module, and it can control an AC current up to 85 A_{RMS} when connected to an AC line network. Thus, it allows to design a single or three-phase AC / DC rectifier bridge, a phase recombination branch of a totem pole PFC up to 75 $A_{(AV)}$ output current, the AC phasing arm of a line inverter or even an back-to-back SCR based AC switch for a heating controller or the by pass relay of an UPS.

With its top cooling pad opposite to the printed circuit board this device allows the PCB-module-heat sink stack to be automatically assembled. This provides a low profile and compact converter in the field of on-board charger, charging station, motor drive, UPS and AC / DC power supplies.

Based on the ST high temperature automotive ASD technology, it offers higher specified noise immunity of 1000 V/µs at the 150 °C junction temperature T_j, and an over-voltage robustness V_{DSM} up to 1400 V.

1 Characteristics

Table 1. Absolute maximum ratings (limiting values, per single SCR)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current, sine half wave		T_C = 106 °C	60	A
$I_{T(AV)}$	Average on-state current, sine half wave			38	A
I_{TSM}	Non repetitive surge peak on-state current, V_R = 0 V, I_G = 100 mA	t_p = 8.3 ms	T_j initial = 25 °C	660	A
		t_p = 10 ms		600	
I^2t	I^2t value for fusing	t_p = 10 ms	T_j = 25 °C	1800	A^2s
dI/dt	Critical rate of rise of on-state SCR current I_G = 2 x I_{GT} , tr ≤ 100 ns	f = 50 and 60 Hz	T_j = 150 °C	200	A/µs
V_{DRM} / V_{RRM}	Repetitive off-state voltage		T_j = -40 °C to 150 °C	1200	V
V_{DSM} / V_{RSM}	Non repetitive surge peak off-state voltage	t_p = 10 ms	T_j = 25 °C	1400	V
V_{GM}	Peak forward SCR gate voltage	t_p = 20 µs	T_j = 150 °C	10	V
I_{GM}	Peak forward SCR gate current	t_p = 20 µs	T_j = 150 °C	8	A
I_{GCM}	Peak cathode drive current, C1 and C2 pins	t_p = 20 µs	T_j = 150 °C	8	A
V_{RGM}	Peak SCR gate voltage		T_j = 25 °C	5	V
$P_{G(AV)}$	Average SCR gate power dissipation		T_j = 150 °C	1	W
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature range			-40 to +150	°C
V_{INS}	RMS tab-to-pin lead insulation voltage, 1 minute			4	kV

Table 2. SCR electrical characteristics, per single SCR

Symbol	Test Conditions			Value	Unit
SCR triggering characteristics					
I_{GT}	V_D = 12 V, R_L = 33 Ω	T_j = 25 °C	Min.	10	mA
			Max.	50	
V_{GT}	V_D = 12 V, R_L = 33 Ω	T_j = 25 °C	Max.	1.3	V
V_{GD}	V_D = 2/3 V_{DRM}, R_L = 3.3 kΩ	T_j = 150 °C	Min.	0.2	V
I_H	I_T = 500 mA, gate open	T_j = 25 °C	Max.	100	mA
I_L	I_G = 1.2 x I_{GT}	T_j = 25 °C	Max.	125	mA
SCR dynamic characteristics					
t_{GT}	I_T = 60 A , V_D = 800 V, I_G = 100 mA, dI_G/dt = 0.2 A/µs	T_j = 25 °C	Typ.	1	µs
t_Q	I_T = 38 A, V_D = 800 V, dI_T/dt = 10 A/µs, V_R = 75 V, dV_D/dt = 20 V/µs, t_p = 100 µs	T_j = 150 °C	Typ.	150	µs
dV/dt	V_D = 800 V, gate open	T_j = 150 °C	Min.	1000	V/µs
SCR static characteristics					
V_{TM}	I_{TM} = 60 A, t_P = 380 µs	T_j = 25 °C	Max.	1.3	V
		T_j = 150 °C	Max.	1.3	V
V_{TOT}	SCR on-state threshold voltage	T_j = 150 °C	Max.	0.8	V
R_{DT}	SCR on-state dynamic resistance	T_j = 150 °C	Max.	7.35	mΩ
I_{DRM}/I_{RRM}	V_D = V_{DRM}, V_R = V_{RRM}	T_j = 25 °C	Max.	5	µA
		T_j = 150 °C	Max.	7.5	mA
I_{DSM}/I_{RSM}	V_D = V_{DSM}, V_R = V_{RSM}	T_j = 25 °C	Max.	10	µA
SCR losses evaluation					
P_{LT}	V_{TOT} x $I_{T(AV)}$ + R_{DT} x $I_{T(RMS)}^2$				W

Table 3. Thermal characteristics

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (DC), per SCR(1)	Max.	0.75	°C/W

1. *The case temperature is measured right underneath the device die on cooling pad*

1.1 Characteristics (curves)

Figure 1. SCR on-state characteristics (maximum value), T_j = 25 °C and 150 °C

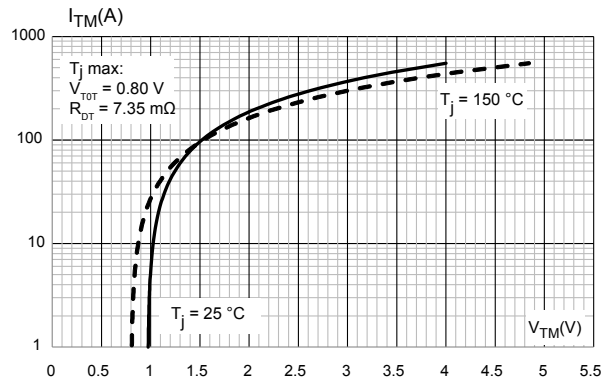


Figure 2. SCR maximum average power dissipation versus average half-wave on-state current, a = 30° to 180°

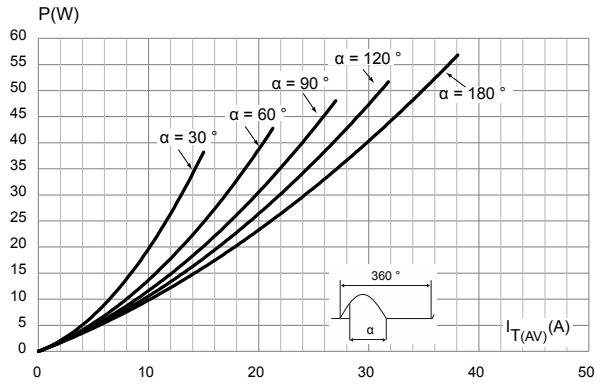


Figure 3. SCR average on-state current versus case temperature

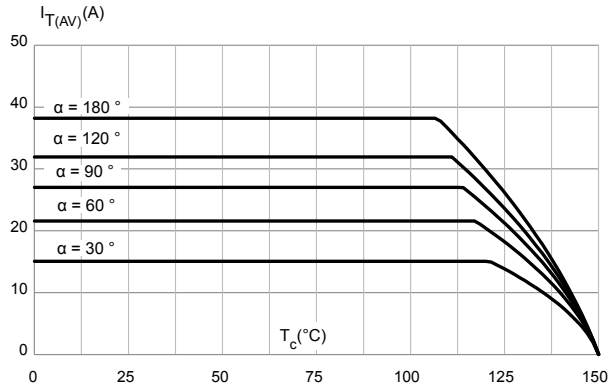


Figure 4. SCR relative variation of thermal impedance junction to case and junction to ambient versus pulse duration, 1 ms to 1 s

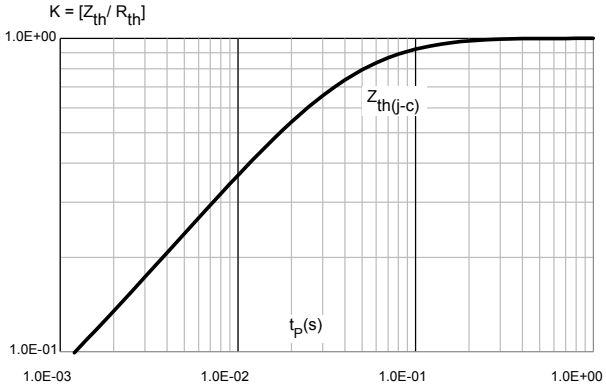


Figure 5. SCR relative variation of gate trigger voltage and current versus junction temperature (typical values)

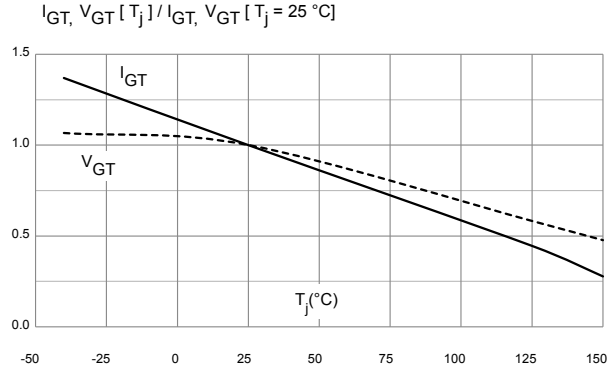


Figure 6. SCR relative variation of holding current and latching current versus junction temperature (typical values)

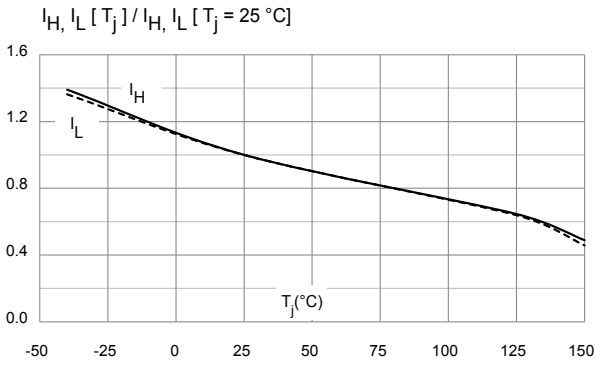


Figure 7. SCR non repetitive surge peak on-state current for a sinusoidal pulse (t_p < 10 ms), V_R = 0 V

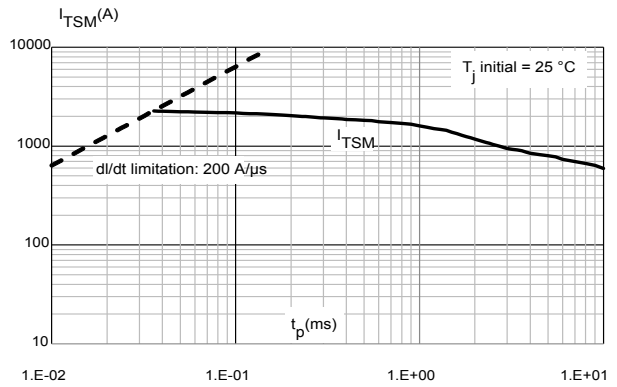


Figure 8. SCR surge peak forward current versus number of half cycles, V_R = 0 V

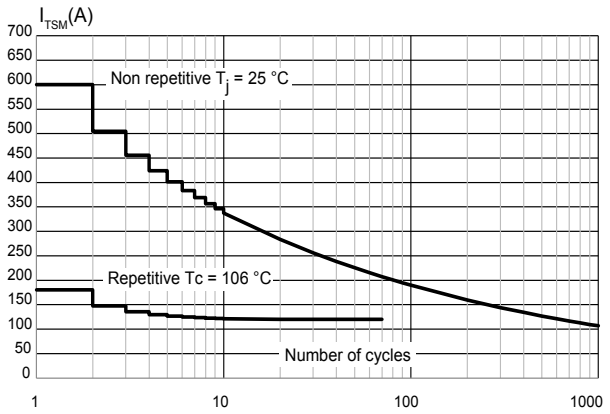


Figure 9. SCR relative variation of the static dV/dt immunity versus junction temperature (typical values

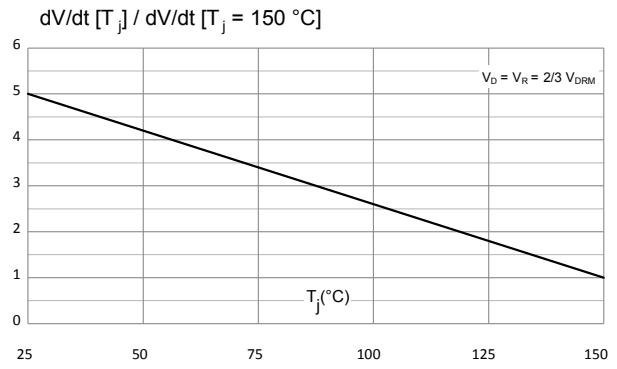


Figure 10. SCR junction capacitance versus reverse voltage applied, gate open (typical values)

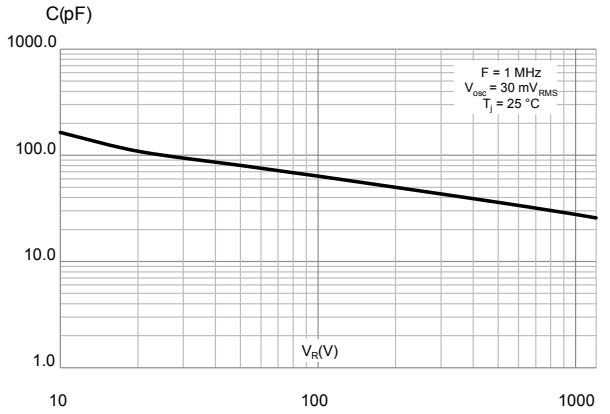
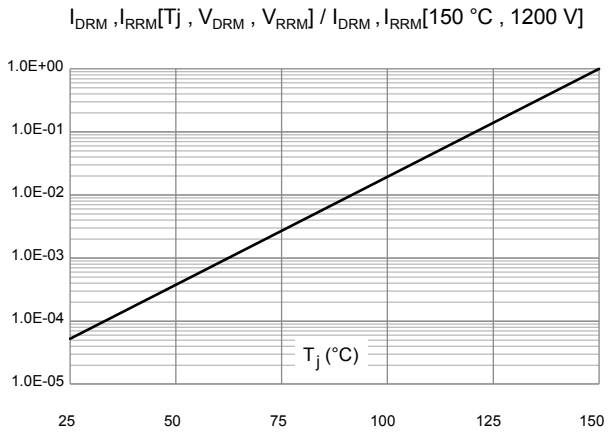


Figure 11. SCR relative variation of leakage current versus junction temperature for max blocking voltage (typical values)



2 Application

2.1 Solid state Inrush current limitation (ICL) using STTN6050H-12M1Y

SCRs can be used in single and three phase applications as AC line polarity switches with an active current limitation at power up or line recovery.

For more information, refer to the application note:

- AN4606: Inrush-current limiter circuits (ICL) with Triacs and thyristors (SCR) and controlled bridge design tips.

Solid-state topologies with SCR allow the applications to easily comply to the following standard:

1. IEC61000-3-3 (voltage fluctuations and flicker in public low-voltage supply systems, for equipment with rated current ≤ 16 A). the high current powered from the grid may lead to voltage fluctuations and drops due to the line impedance. Those mains voltage disturbances have an impact on any other equipment connected to the same circuit and cause undesired brightness variation of lamps or displays (commonly called flickering phenomenon).
2. IEC61000-4-11 (voltage dips, short interruptions, and voltage variations immunity tests) As any appliance connected to the mains can be subject to line voltage dips or interruptions, a high input current may occur when the line voltage suddenly comes back to its nominal value. This high current may damage the front-end circuit components and can trigger an AC fuse for example.

2.1.1 Single- phase applications

Figure 12 and Figure 13 define an active inrush current limiter in single-phase application with SCRs respectively in full wave SCRs bridge and in PFC totem pole bridgeless topology.

Figure 12. Single-phase full wave SCRs bridge rectifier

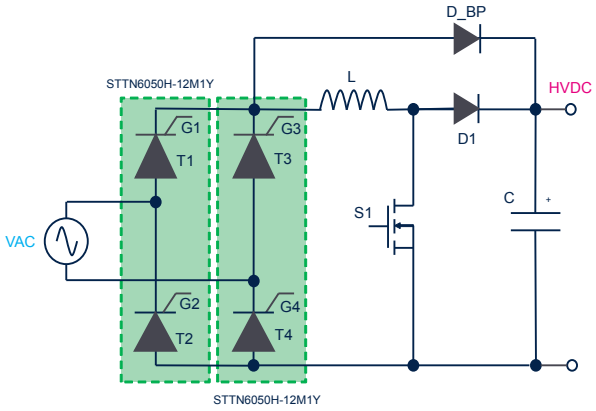
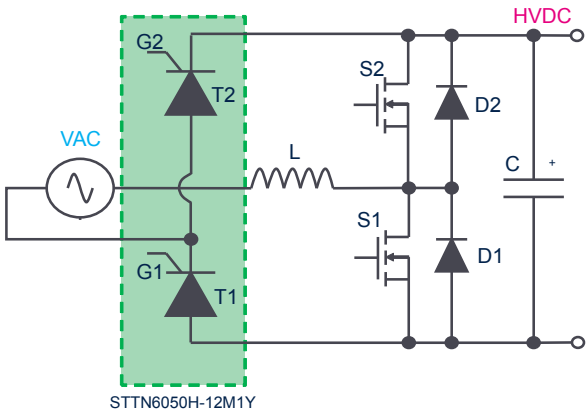
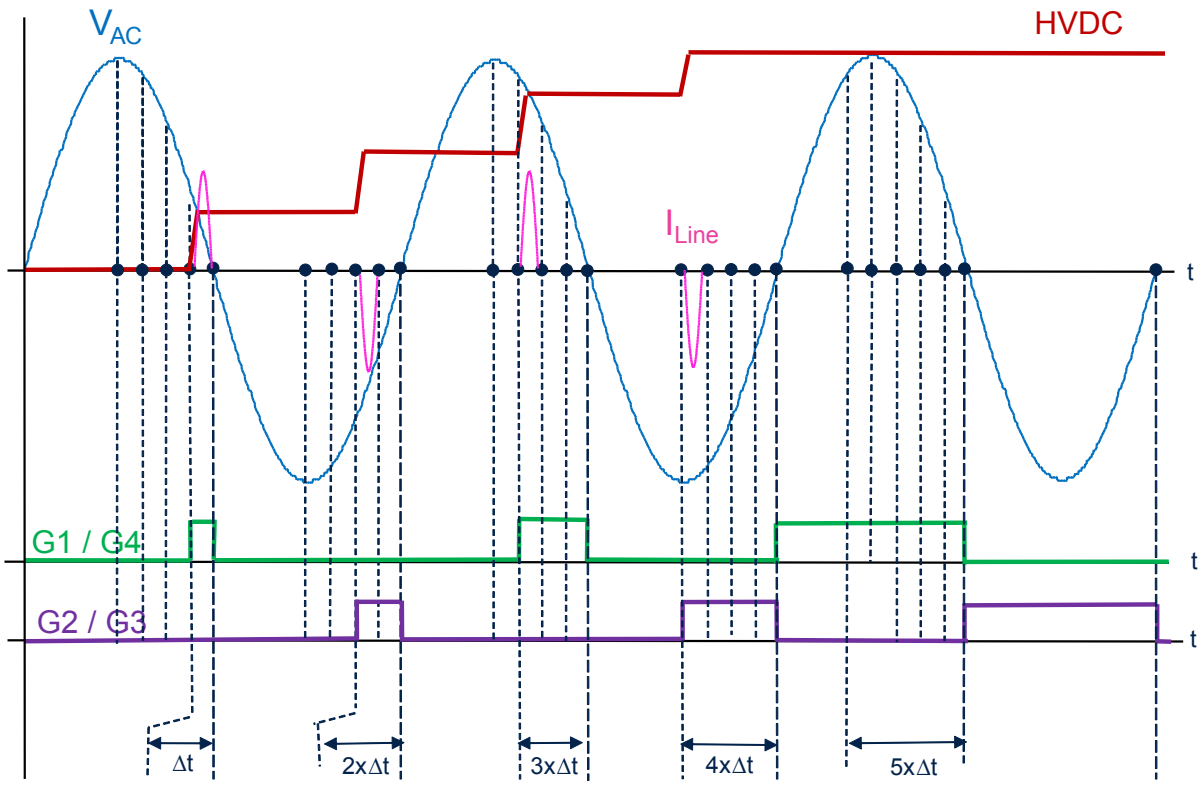


Figure 13. Single-phase PFC Totem Pole bridgeless



SCRs are controlled in phase angle to smoothly increase the PFC output capacitor voltage up to peak AC line voltage. The pre-charging peak current value is controlled by a microcontroller which smartly synchronize the SCRs gate driving signal angle step (referred as Δt in the Figure 14 here below). Limiting resistor like a negative temperature coefficient resistor (NTC) is no more needed.

Figure 14. **Inrush current controlled by SCRs principle**



2.1.2 Three-phase applications

Figure 15 and Figure 16 define an example of active inrush current limiter in three-phase application with SCR respectively in three-phase SCRs bridge rectifier and in three-phase VIENNA with 6 totem-pole SCRs topology.

Figure 15. **Three-phase SCRs bridge rectifier**

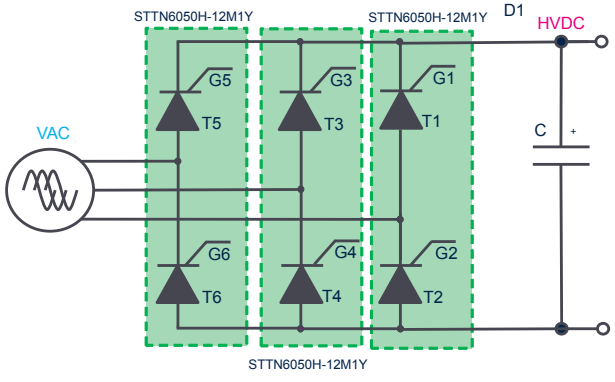
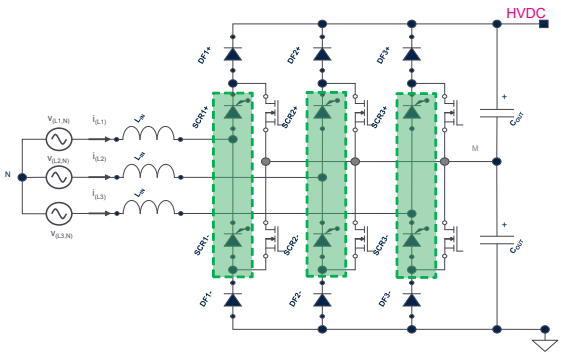


Figure 16. **Three-phase VIENNA with 6 Totem-Pole SCR**



2.2 Solid state relay (SSR) using STTN6050H-12M1Y

Solid-state relays (SSR) can perform same tasks as electromechanical relay. SSR provides a high reliability, a long service life, an electromagnetic interference reduction, a fast response. Moreover, the SSR has no moving parts to wear out or arcing contacts to deteriorate that are cause of failure about the electromechanical relay.

As defined by the Figure 17 , when a control current is applied to the input of the opto-TRIAC, the SCRs are turned on. When the control current is removed from the input of the opto-TRIAC, SCRs are turned off when the load current falls to the zero. Note the SSR can be used as contactor for 2-phase motor (see Figure 18) or as bypass relay (see Figure 19).

Figure 17. SSR as AC load control

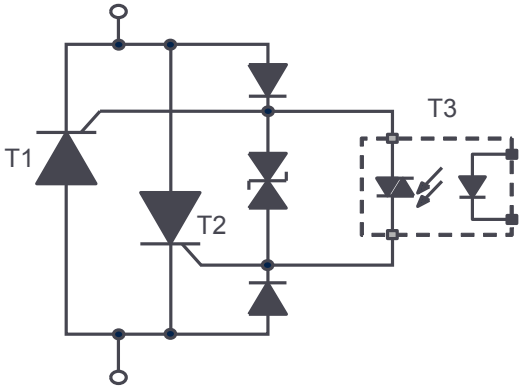


Figure 18. SSR as contactor

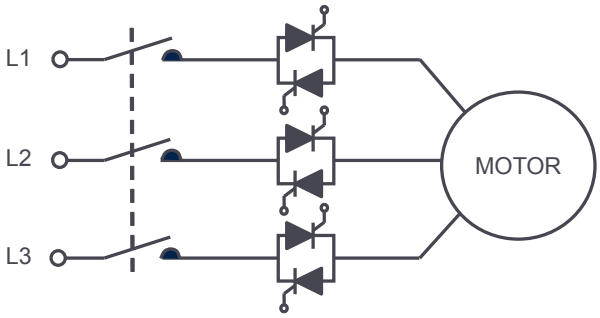
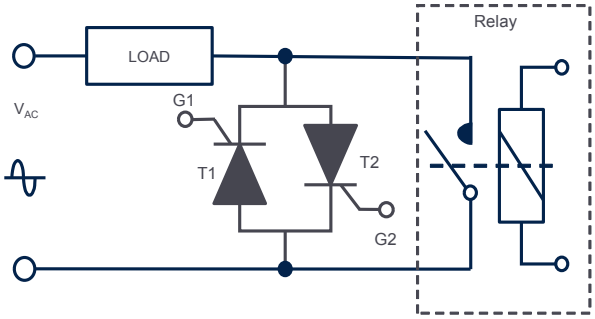


Figure 19. SSR as relay bypass



2.3 Dissipated power and junction temperature calculation at steady state

2.3.1 Dissipated power definition

Dissipated power of the SCR is defined by the following equation with V_{TOT} the SCR on-state threshold voltage, R_{DT} the SCR on-state dynamic resistance, $I_{T(AV)}$ the SCR average current and $I_{T(RMS)}$ the SCR RMS current:

$$P_d = V_{TOT} \times I_{T(AV)} + R_{DT} \times I^2_{T(RMS)} \quad (1)$$

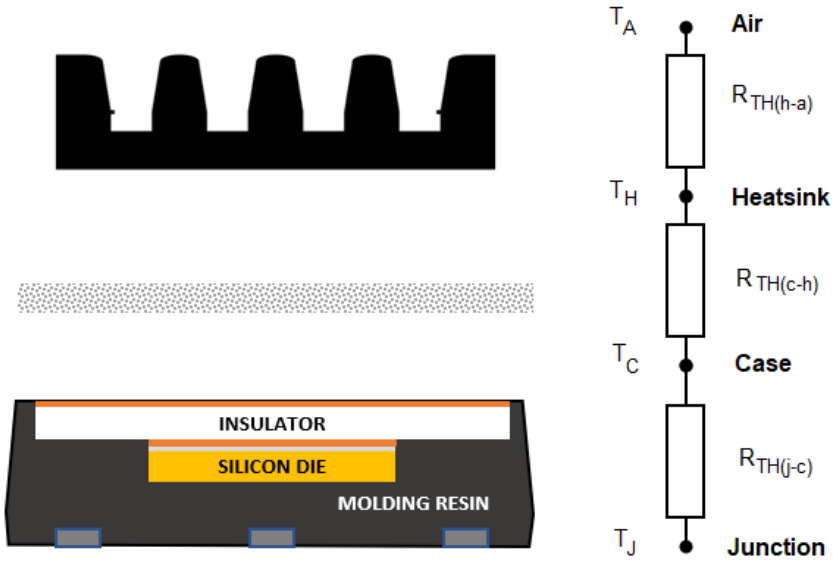
Table 4 gives the average and RMS current of SCR according to the topology defined in the previous section by considering the RMS current of the AC line $I_{L(RMS)}$ is a sinus waveform.

Table 4. $I_{T(AV)}$ and $I_{T(RMS)}$ definition

Topology	Current definition	
Single-phase full wave SCRs bridge rectifier	$I_{T(AV)}$	$I_{T(AV)} = \frac{\sqrt{2}}{\pi} \times I_{L(RMS)}$
Single-phase PFC Totem Pole bridgeless		
SSR	$I_{T(RMS)}$	$I_{T(RMS)} = \frac{I_{L(RMS)}}{\sqrt{2}}$
Three-phase VIENNA with 6 Totem-Pole SCRs		

2.3.2 Junction temperature definition

Figure 20. Die assembly representation



When Tc value is known, silicon junction temperature can be calculated as follows:

$$T_j = T_C + P_D \times R_{TH(j-c)}$$

Otherwise, starting from ambient temperature measurement, junction temperature can be calculated as follows:

$$T_j = T_A + P_D \times R_{TH(j-a)}$$

Note: $R_{th(j-c)}$ value is given in the datasheet above.

with:

$$R_{TH(j-a)} = R_{TH(j-c)} + R_{TH(c-h)} + R_{TH(h-a)}$$

and where $R_{TH(c-h)}$ is the thermal interface resistance (grease or foil) and $R_{TH(h-a)}$ is the heatsink thermal resistance.

For more information about the thermal management and power dissipation calculation, refer to the application note:

- AN533: SCRs, TRIACs, and AC switches, thermal management precautions for handling and mounting

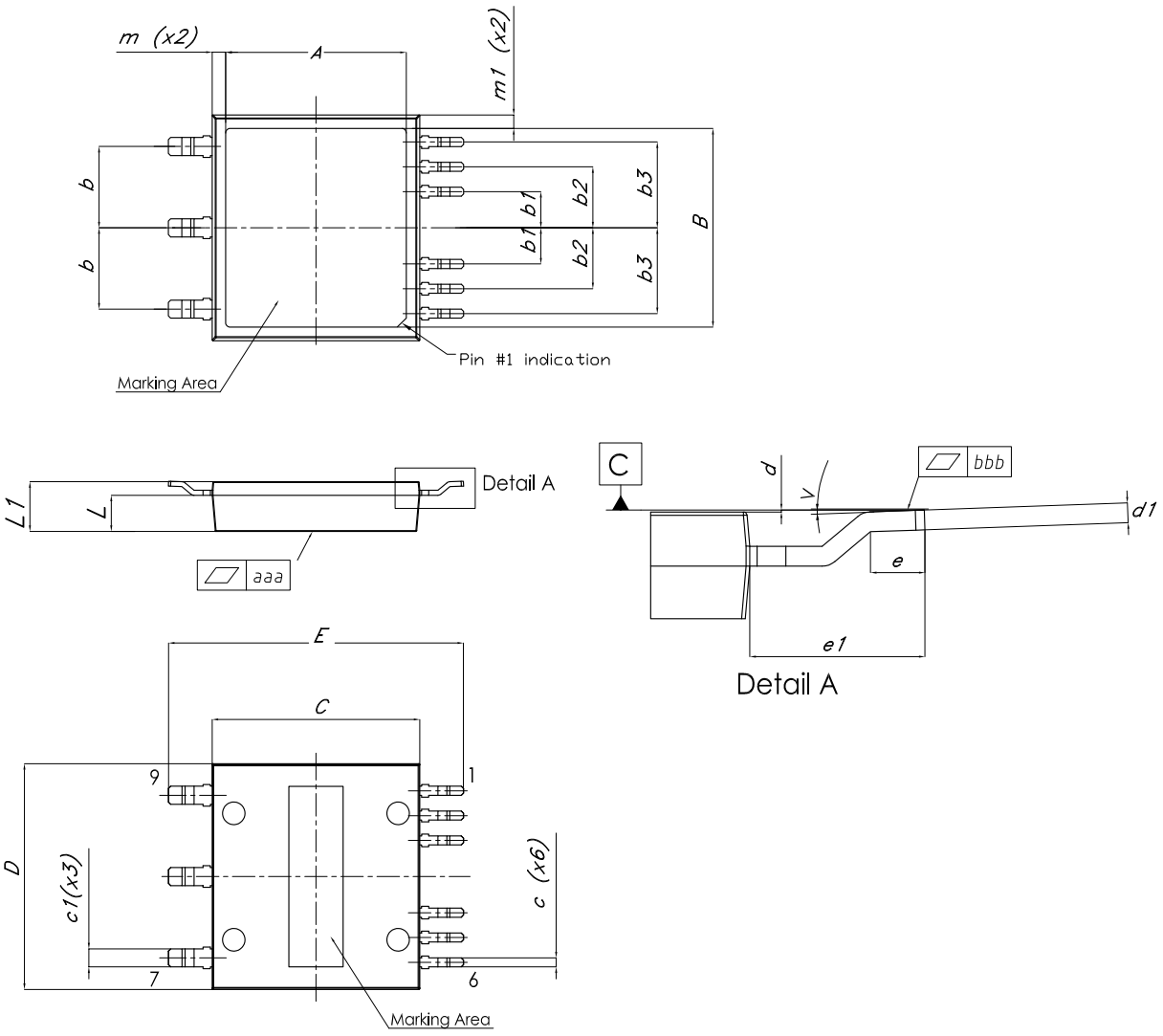
3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 ACEPACK SMIT package information

- Lead-free package leads finishing
- Halogen-free molding compound resin meets UL94 standard level V0

Figure 21. ACEPACK SMIT package outline

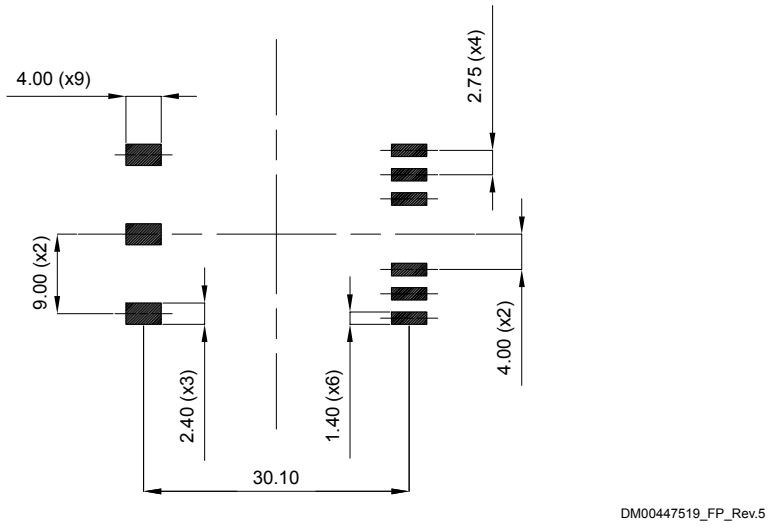


DM00447519_Rev.6

Table 5. ACEPACK SMIT package mechanical data

Dim.	mm			Inches (for reference only)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	19.50	20.00	20.50	0.7677	0.7874	0.8071
B	21.50	22.00	22.50	0.8465	0.8661	0.8858
C	22.80	23.00	23.20	0.8976	0.9055	0.9134
D	24.80	25.00	25.20	0.9764	0.9843	0.9921
E	32.20	32.70	33.20	1.2677	1.2874	1.3071
b		9.00			0.3543	
b1		4.00			0.1575	
b2		6.75			0.2657	
b3		9.50			0.3740	
c	0.95	1.00	1.10	0.0374	0.0394	0.0433
c1	1.95	2.00	2.10	0.0768	0.0787	0.0827
d	0.00		0.15	0.0000	0.0000	0.0059
d1	0.45	0.55	0.65	0.0177	0.0217	0.0256
e	1.30	1.50	1.70	0.0512	0.0591	0.0669
e1	4.65	4.85	5.05	0.1831	0.1909	0.1988
L	3.95	4.00	4.05	0.1555	0.1575	0.1594
L1	5.40	5.50	5.60	0.2126	0.2165	0.2205
m	1.30	1.50	1.80	0.0512	0.0591	0.0709
m1	1.30	1.50	1.80	0.0512	0.0591	0.0709
V	0°	2°	4°	0°	2°	4°
aaa	0.01		0.05		0.0004	0.0020
bbb	0.00		0.10		0.0000	0.0039

Figure 22. ACEPACK SMIT recommended footprint (dimensions are in mm)



Note: Recommended pressing force on package to the heatsink: 50 N as described in application note AN5384.

3.2 ACEPACK SMIT package insulation information

Figure 23. **ACEPACK SMIT package insulation information**

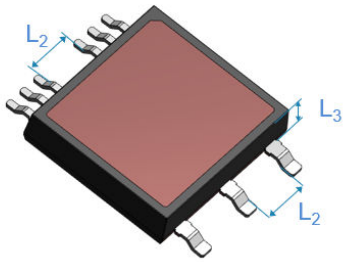


Table 6. **ACEPACK SMIT package insulation characteristics**

Symbol	Parameter			Value	Unit
L2	Pin-to-pin creepage distance	Terminal to terminal: 3 to 4, 7 to 8, 8 to 9	Min.	6.6	mm
L3	Pin-to-backside creepage distance		Min.	4	mm
I_{INS}	RMS tab-to-pin lead insulation current	Duration = 1 s., V_{INS} = 4.8 kV	Max.	1	mA

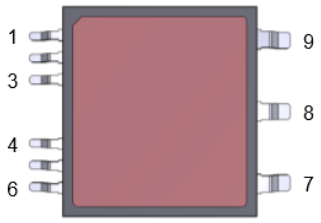
Note: Recommended pressing force on package to the heatsink: 50 N as described in application note AN5384.

3.3 ACEPACK SMIT terminal description

Table 7. ACEPACK SMIT STTN6050H-12M1Y module pinout description

Pin #	Name	Description
1	C2	T2 cathode drive
2	NC	Not connected
3	G2	T2 gate
4	G1	T1 gate
5	NC	Not connected
6	C1	T1 cathode drive
7	DC1	DC output 1
8	DC2	DC output 2
9	AC	AC line

Figure 24. ACEPACK SMIT STTD6050H-12M2Y module pinout



TOP VIEW
Pin 1 at cut pad top edge

3.4 ACEPACK SMIT packing information

Figure 25. **ACEPACK SMIT carrier tape outline, bottom view**

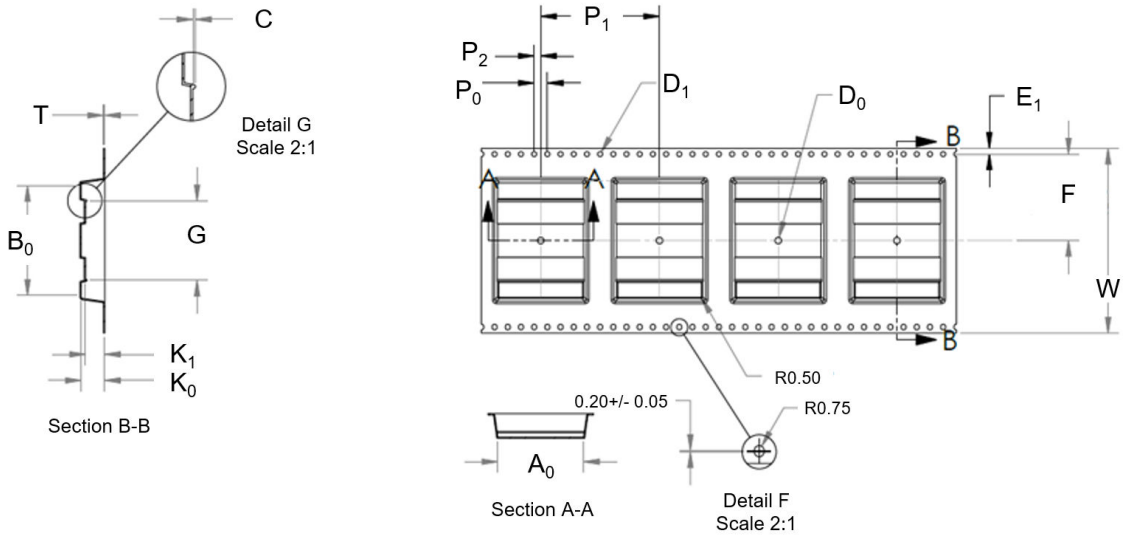


Table 8. **ACEPACK SMIT carrier tape dimensions**

Carrier tape typical dimension (mm)														
A_0	B_0	C	D_0	D_1	E_1	F	G	K_0	K_1	P_0	P_1	P_2	T	W
26.00	33.30	0.40	2.00	1.50	1.75	26.20	24.10	7.10	5.80	4.00	36.00	2.00	0.35	56.00

Figure 26. **ACEPACK SMIT reel outline**

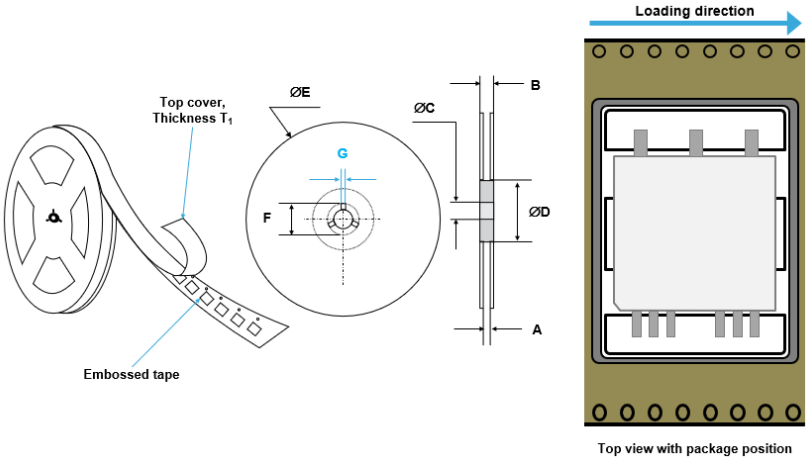


Table 9. **ACEPACK SMIT reel dimensions**

Base qty.	Reel dimension (mm)							
	A	B (max.)	C	D (min.)	E (max.)	F (min.)	G	T_1 (max.)
200	16.4 ±0.3	22.4	13.2 ±0.2	20.2 ±0.25	330	20.2	2.0 ±0.5	0.1

4 Ordering information

Figure 27. **Ordering information scheme**

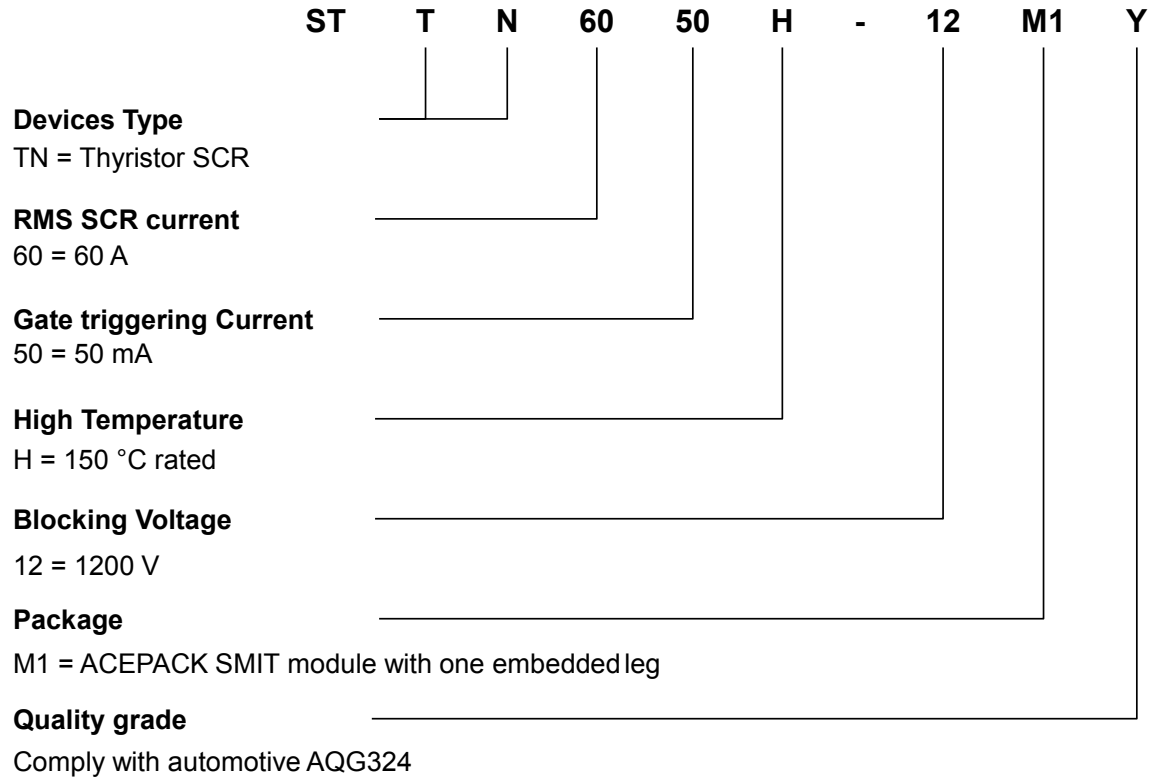


Table 10. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
STTN6050H-12M1Y	STTN6050H12M1Y	ACEPACK SMIT	8.1 g	200	Tape and reel

Revision history

Table 11. **Document revision history**

Date	Revision	Changes
15-Jun-2021	1	Initial release.
15-Feb-2023	2	Updated product summary table on cover page.