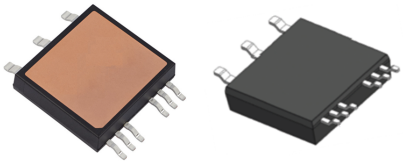
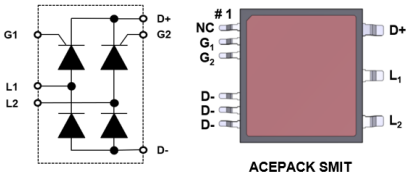
STTD6050H-12M2Y

Datasheet

60 A 1200 V half-controlled bridge rectifier in ACEPACK SMIT module



ACEPACK SMIT



ACEPACK SMIT
top view

STPOWER

Product status
Internal

Product summary	
$I_{T(RMS)}$,$I_{F(RMS)}$	60 A
$I_{OUT(AV)}$	75 A
V_{DRM}/V_{RRM}	1200 V
V_{DSM}/V_{RSM}	1400 V
I_{GT}	50 mA
T_j max.	150 °C

Features

- AEC-Q101 qualified
- 1200 V symmetrical blocking voltage
- High junction temperature: 150 °C
- High noise immunity, static dV/dt: 1000 V/µs
- Embed two TN6050HP-12 and two STBR6012 dies
- Module qualified according to AQG324 recommendation
- SMD with isolated top cooled tab
- Terminal pins opposite to cooling side
  - Fully automatic PCB mounting to heat sink
- Moisture Sensitivity Level : Level 3
  - IPC/JEDEC J-STD-033
- 4000 V insulated tab-to-lead package
  - UL recognized, File E81734
- Large creepage distance to meet IEC 60664-1
  - 250 V_{AC}, material group 2, pollution degree 3
  - 600 V_{AC}, material group 2, pollution degree 2
- Smaller footprint than four TO-247
- ECOPACK2 compliant component

Applications

- Single-phase controlled bridge rectifier
- On-board and stationary chargers
- AC DC converter for motor drive, UPS and SMPS
- AC input converter current up to 85 A_{RMS}
- Output full wave DC current up to 75 A_{AV}

Description

The STTD6050H-12M2Y is a top cooled surface mount module that integrates a single-phase half-controlled bridge rectifier. It is rated at 1200 V and delivers an output full wave DC current up to 75 A_{AV}. Each single embedded device has a rated current of 60 A_{RMS} and a symmetric blocking voltage of 1200 V.

With its top cooling pad opposite to the printed circuit board this device allows the PCB-module-heat sink stack to be automatically assembled.

This provides a low profile and compact converter in the field of on-board charger, charging station, motor drive, UPS and AC-DC power supplies.

Based on the ST high temperature automotive planar technology, it offers higher specified noise immunity of 1000 V/µs up to the 150 °C junction temperature T_j, and an over-voltage robustness V_{DSM} up to 1400 V.

1 Characteristics

Table 1. Diode and SCR absolute maximum ratings (limiting values)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$, $I_{F(RMS)}$	RMS on-state current, sine half wave		T_{C_SCR} = 106 °C	60	A
$I_{T(AV)}$, $I_{F(AV)}$	Average on-state current, sine half wave		T_{C_DIODE} = 110 °C	38	A
$I_{OUT(AV)}$	Average output current, sine full wave		$T_{C(AV)}$ = 106 °C	75	A
I_{TSM}, I_{FSM}	Non repetitive surge peak on-state current, V_R = 0 V, I_G = 100 mA	t_p = 8.3 ms	T_j initial = 25 °C	525	A
		t_p = 10 ms		500	
I^2t	I^2t value for fusing	t_p = 10 ms	T_j = 25 °C	1250	A^2s
dI/dt	Critical rate of rise of on-state SCR current I_G = 2 x I_{GT} , tr ≤ 100 ns	f = 100 Hz	T_j = 150 °C	200	A/µs
V_{DRM} / V_{RRM}	Repetitive off-state voltage(1)		T_j = -40 °C to 150 °C	1200	V
V_{DSM} / V_{RSM}	Non repetitive surge peak off-state voltage(1)	t_p = 10 ms	T_j = 25 °C	1400	V
V_{GM}	Peak forward SCR gate voltage	t_p = 20 µs	T_j = 150 °C	10	V
I_{GM}	Peak forward SCR gate current	t_p = 20 µs	T_j = 150 °C	8	A
V_{RGM}	Peak SCR gate voltage		T_j = 25 °C	5	V
$P_{G(AV)}$	Average SCR gate power dissipation		T_j = 150 °C	1	W
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature range			-40 to +150	°C
V_{INS}	RMS tab-to-leads insulation voltage, 1 minute, f = 50 - 60 Hz			4	kV

1. *V_{DRM} and V_{DSM} apply to SCR only.*

Table 2. SCR electrical characteristics, per single SCR

Symbol	Test Conditions(1)			Value	Unit
SCR triggering characteristics					
I_{GT}	V_D = 12 V, R_L = 33 Ω	T_j = 25 °C	Min.	10	mA
			Max.	50	
V_{GT}	V_D = 12 V, R_L = 33 Ω	T_j = 25 °C	Max.	1.3	V
V_{GD}	V_D = 2/3 V_{DRM}, R_L = 3.3 kΩ	T_j = 150 °C	Min.	0.2	V
I_H	I_T = 500 mA, gate open	T_j = 25 °C	Max.	100	mA
I_L	I_G = 1.2 x I_{GT}	T_j = 25 °C	Max.	125	mA
SCR dynamic characteristics					
t_{GT}	I_T = 60 A , V_D = 800 V, I_G = 100 mA, dI_G/dt = 0.2 A/µs	T_j = 25 °C	Typ.	1	µs
t_Q	I_T = 38 A, V_D = 800 V, dI_T/dt = 10 A/µs, V_R = 75 V, dV_D/dt = 20 V/µs, t_p = 100 µs	T_j = 150 °C	Typ.	150	µs
dV/dt	V_D = 800 V, gate open	T_j = 150 °C	Min.	1000	V/µs

Symbol	Test Conditions[1]			Value	Unit
SCR static characteristics					
V_{TM}	I_{TM} = 60 A, t_P = 380 µs	T_j = 25 °C	Max.	1.3	V
		T_j = 150 °C	Max.	1.3	V
V_{TOT}	SCR on-state threshold voltage	T_j = 150 °C	Max.	0.8	V
R_{DT}	SCR on-state dynamic resistance	T_j = 150 °C	Max.	7.45	mΩ
I_{DRMT}/I_{RRMT}	$V_D = V_{DRM}$, $V_R = V_{RRM}$	T_j = 25 °C	Max.	5	µA
		T_j = 150 °C	Max.	7.5	mA
I_{DSMT}/I_{RSMT}	$V_D = V_{DSM}$, $V_R = V_{RSM}$	T_j = 25 °C	Max.	10	µA
SCR losses evaluation					
P_{LT}	$V_{TOT} \times I_{T(AV)} + R_{DT} \times I_{T(RMS)}^2$				W

1. *Refer to application note AN4608 for parameter definition*

Table 3. Diode Electrical Characteristics, per single diode

Symbol	Test Conditions			Value	Unit
Diode static characteristics					
V_F	I_F = 60 A, t_P = 380 µs, duty cycle δ < 2%	T_j = 25 °C	Max.	1.3	V
		T_j = 150 °C	Max.	1.2	V
V_{TOD}	On-state rectifier threshold	T_j = 150 °C	Max.	0.96	V
R_{DD}	On-state rectifier dynamic resistance	T_j = 150 °C	Max.	4	mΩ
I_{RRMD}	$V_R = V_{RRM}$, t_p = 5 ms, duty cycle δ < 2%	T_j = 25 °C	Max.	5	µA
		T_j = 150 °C	Max.	250	
I_{RSMD}	$V_R = V_{RSM}$	T_j = 25 °C	Max.	25	µA
Diode losses evaluation					
P_{LD}	$V_{TOD} \times I_{T(AV)} + R_{DD} \times I_{T(RMS)}^2$				W

Table 4. Thermal characteristics

Symbol	Parameter		Value	Unit
$R_{th(j\text{-}c)\,T}$	Junction to case (DC), per SCR[1]	Max.	0.75	°C/W
$R_{th(j\text{-}c)\,D}$	Junction to case (DC), per diode [1]	Max.	0.75	°C/W

1. *The case temperature is measured right underneath the device die on cooling pad*

For more information, please refer to the following application note related to the thermal management:

- AN5384: ACEPACK SMIT module package guidelines for mounting and thermal management

1.1 Characteristics (curves)

Figure 1. Diode forward on-state characteristics (maximum value), T_j = 25 °C and 150 °C

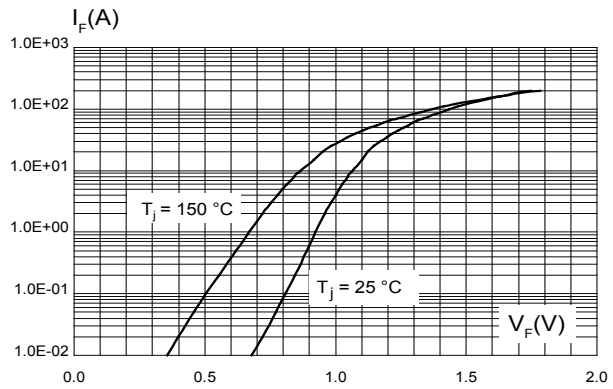


Figure 2. SCR on-state characteristics (maximum values), T_j = 25 °C and 150 °C

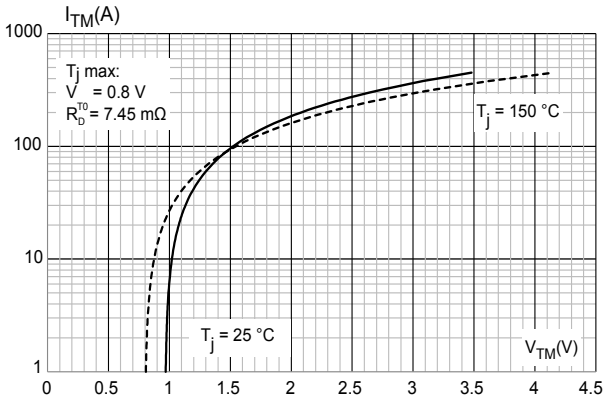


Figure 3. Diode maximum average power dissipation versus average half-wave on-state current, a = 30 ° to 180 °

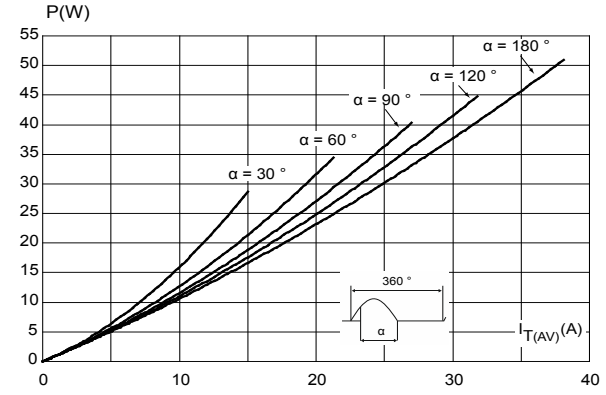


Figure 4. SCR maximum average power dissipation versus average half-wave on-state current, a = 30 ° to 180 °

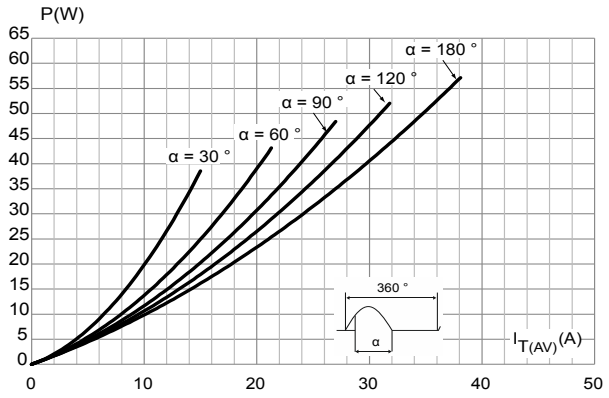


Figure 5. Diode average on-state current versus case temperature

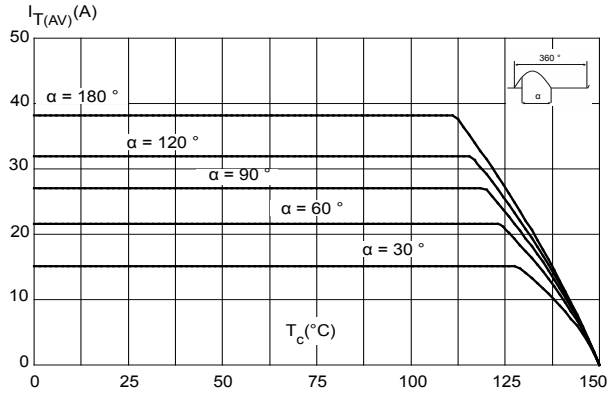


Figure 6. SCR average on-state current versus case temperature

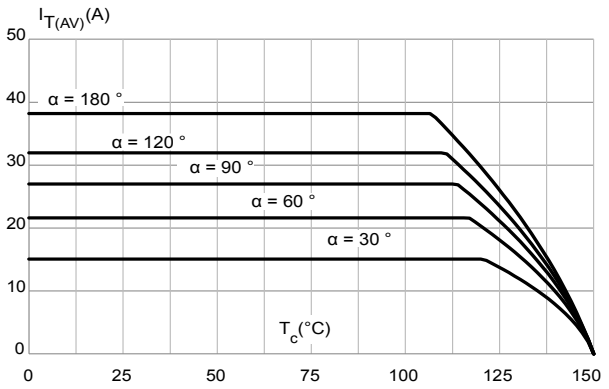


Figure 7. Diode relative variation of thermal impedance junction to case versus pulse duration, 1 ms to 1 s

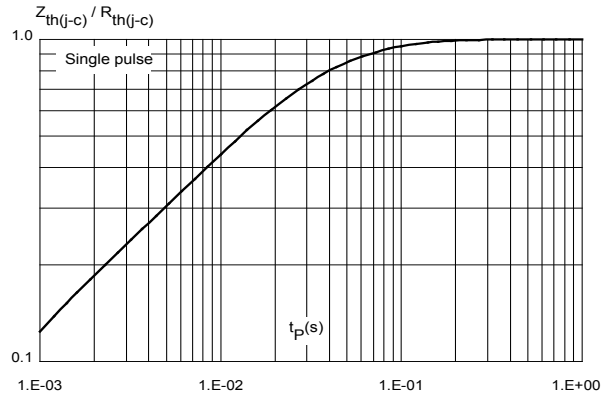


Figure 8. SCR relative variation of thermal impedance junction to case versus pulse duration, 1 ms to 1 s

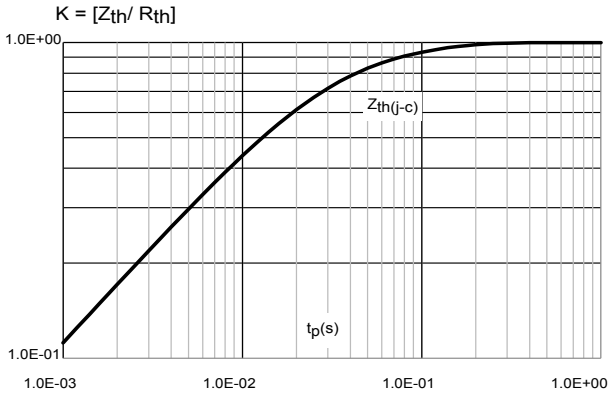


Figure 9. SCR relative variation of gate trigger current and gate trigger voltage versus junction temperature (typical values)

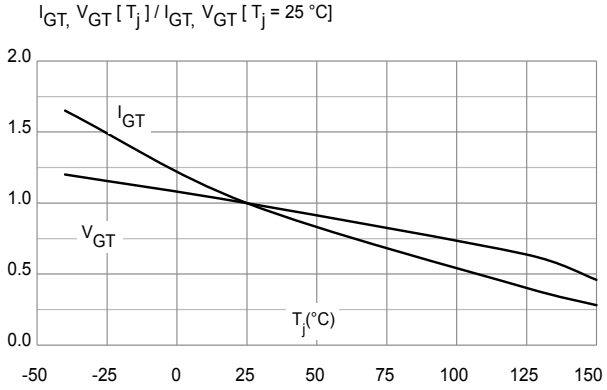


Figure 10. SCR relative variation of holding and latching current versus junction temperature (typical values)

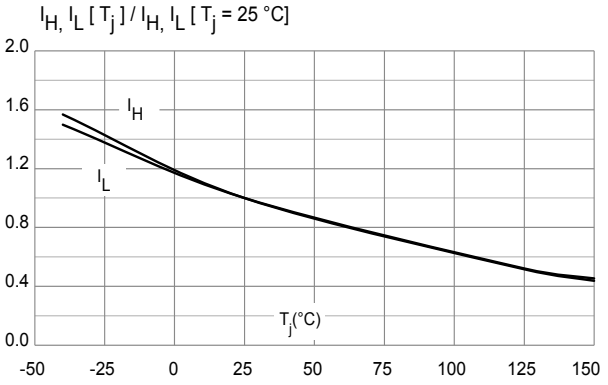


Figure 11. Diode non repetitive surge peak on-state current for a sinusoidal pulse (t_p < 10 ms) , V_r = 0 V

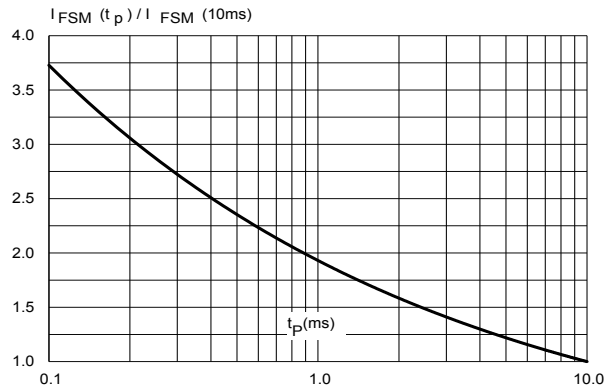


Figure 12. SCR non repetitive surge peak on-state current for a sinusoidal pulse (t_p < 10 ms) , V_r = 0 V

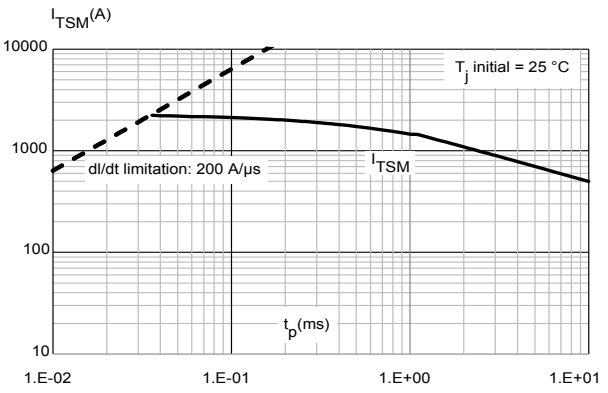


Figure 13. SCR and diode surge peak forward current versus number of half cycles, V_r = 0 V and T_j initial = 25 °C

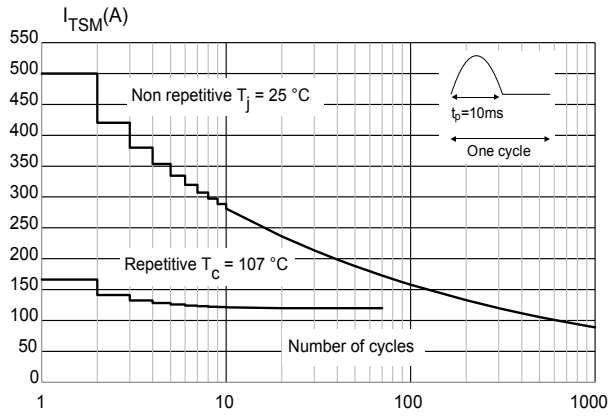


Figure 14. SCR and Diode junction capacitance versus reverse voltage applied, gate open, in discrete package (typical values)

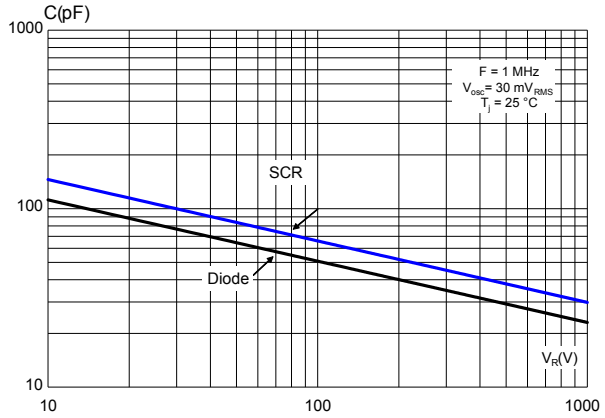
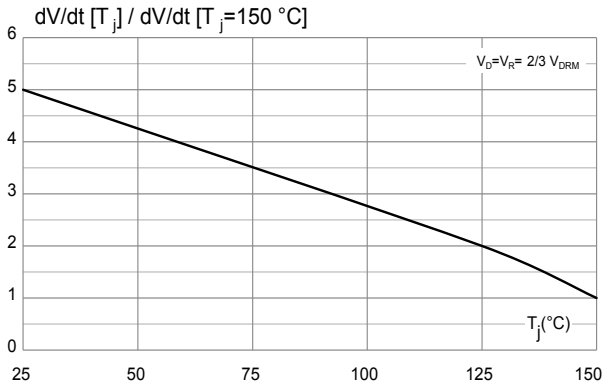


Figure 15. SCR relative variation of the static dV/dt immunity versus junction temperature (typical values)



2 Application

2.1 Solid state Inrush current limitation topologies using STTD6050H-12M2Y

As illustrated here below, bypass and mixed bridge rectifiers are two topologies dedicated to the AC line voltage rectification which include the solid-state inrush current limitation feature.

Figure 16. Bypass function ensured by SCR

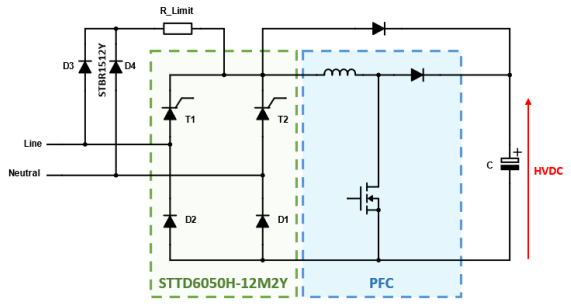
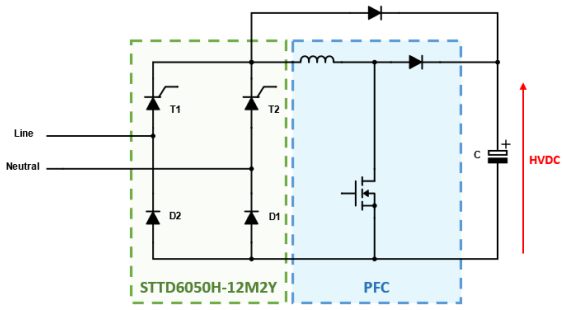


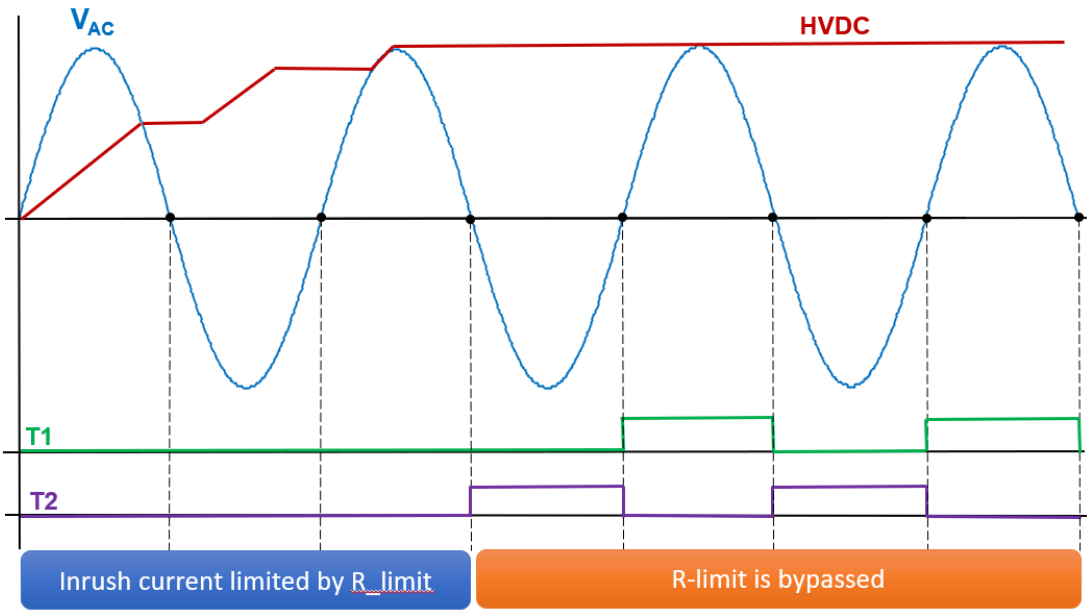
Figure 17. Soft start / mixed control bridge rectifier



In the bypass topology, at system start-up both T1 and T2 SCRs are OFF. The output bulk capacitor is then charged through the D3, D4, D2, D1 diodes and the current is limited by the R_limit resistor placed in the current path.

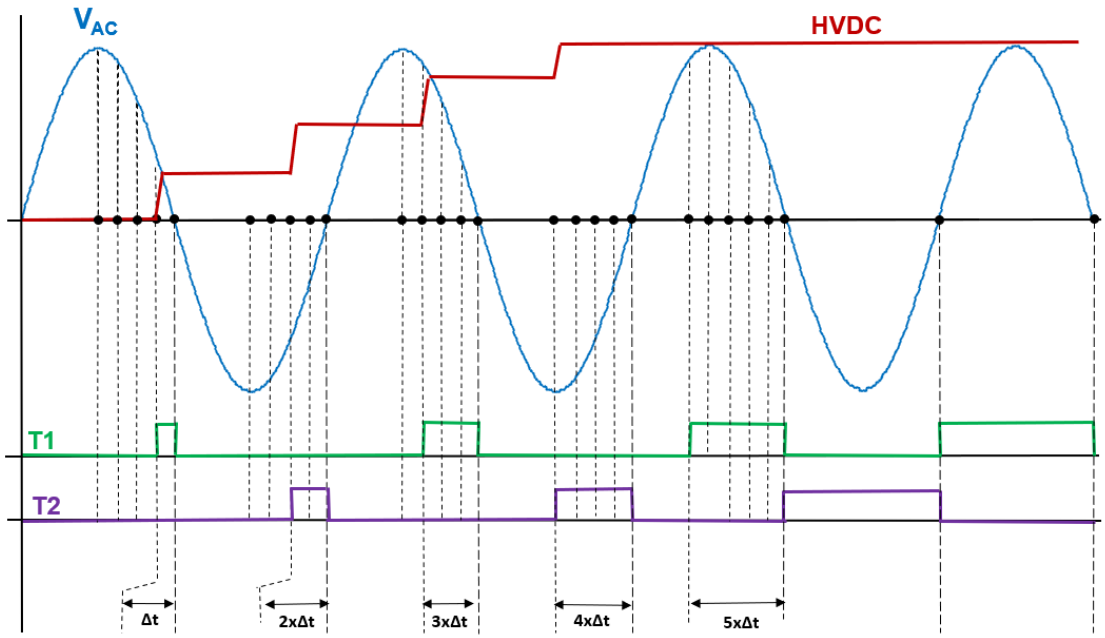
At steady state, R_limit power losses are cut by switching ON alternatively the T1 and T2 SCRs according to line polarity which are then bypassing R_limit.

Figure 18. Bypass topology waveform working principle



In the mixed bridge topology, SCRs are controlled in phase angle to smoothly increase the PFC output capacitor voltage up to peak AC line voltage. The pre-charging peak current value is controlled by a microcontroller which smartly synchronizes the SCRs gate driving signal angle step (referred as Δt in the figure here below). Limiting resistor is no more needed.

Figure 19. Mixed bridge phase angle principle



For more information, refer to the application note:

- AN4606: Inrush-current limiter circuits (ICL) with Triacs and Thyristors (SCR) and controlled bridge design tips.

Those two robust solid-state topologies allow the applications to easily comply to the following standards:

1. IEC61000-3-3 (voltage fluctuations and flicker in public low-voltage supply systems, for equipment with rated current ≤ 16 A). the high current powered from the grid may lead to voltage fluctuations and drops due to the line impedance. Those mains voltage disturbances have an impact on any other equipment connected to the same circuit and cause undesired brightness variation of lamps or displays (commonly called flickering phenomenon).
2. IEC61000-4-11 (voltage dips, short interruptions, and voltage variations immunity tests) As any appliance connected to the mains can be subject to line voltage dips or interruptions, a high input current may occur when the line voltage suddenly comes back to its nominal value. This high current may damage the front-end circuit components and can trigger an AC fuse for example.

2.2 Dissipated power and junction temperature calculation at steady state

In below example, STTD6050H-12M2Y is placed upstream from PFC stage. I_T and I_F define respectively SCR and diode current value. Therefore, the current taken from the line and flowing through the mixed bridge is a sinus waveform.

Figure 20. Soft start / mixed control bridge rectifier

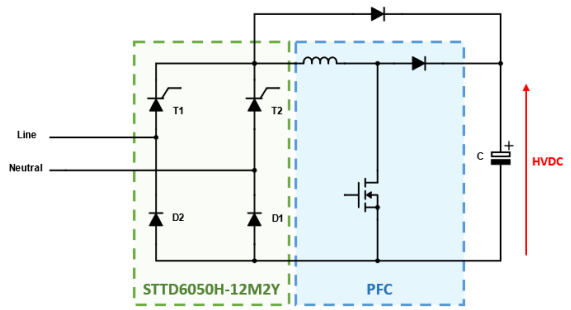
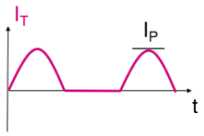


Figure 21. SCR / diode current waveform (sinusoidal half wave)



$$I_{T(AV)} = \frac{1}{T}\int_0^T i(t)dt \Rightarrow \boldsymbol{I_{T(AV)} = I_{F(AV)} = \frac{I_P}{\pi}}$$

$$I^2_{T(RMS)} = \frac{1}{T}\int_0^T i^2(t)dt \Rightarrow \boldsymbol{I^2_{T(RMS)} = I^2_{F(RMS)} = \frac{I_P{}^2}{4}}$$

2.2.1 Dissipated power into SCRs and diodes

Dissipated power into SCRs and diodes is defined by the following equation:

$$\boldsymbol{P_d = V_{T0X} \times I_{T(AV)} + R_{DX} \times I^2_{T(RMS)}} \quad (1)$$

Note: V_{T0X} and R_{DX} are given in Eq. (1) and Eq. (4) where X = T for the SCR and F for the diode.

$$I_{T(AV)} = \frac{I_P}{\pi}\,; Ip = I_{Line(RMS)} \times \sqrt{2} = > I_{T(AV)} = \frac{\sqrt{2}}{\pi} \times I_{L(RMS)} \quad (2)$$

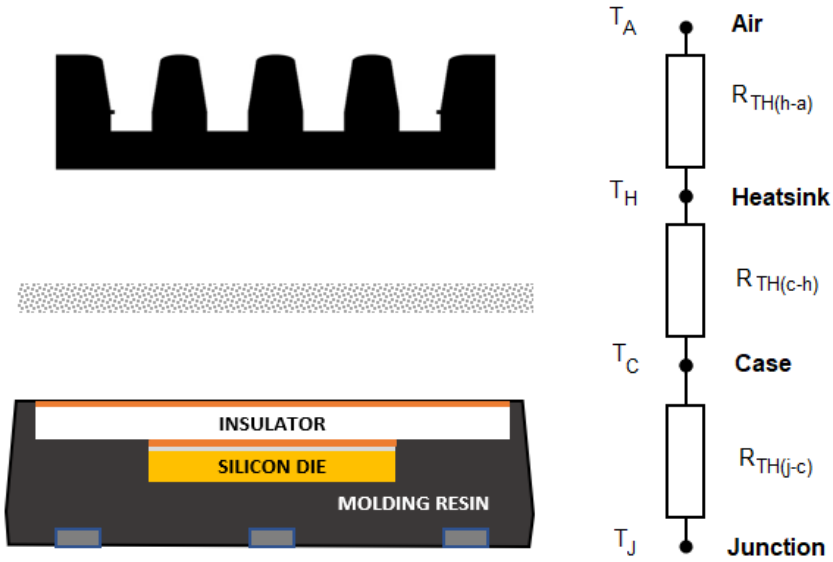
$$I^2_{T(RMS)} = \frac{I_P{}^2}{4} = \frac{I^2_{L(RMS)}}{2} \quad (3)$$

Using equations (1), (2) and (3), dissipated power can directly be calculated from AC line RMS current value $I_{L(RMS)}$ for a single SCR or diode in the mixed bridge:

$$\boldsymbol{P_d = \frac{V_{T0X} \cdot \sqrt{2}}{\pi} \times I_{L(RMS)} + \frac{R_{DX}}{2} \times I^2_{L(RMS)}} \quad (4)$$

2.2.2 Junction temperature calculation

Figure 22. **Die assembly representation**



When Tc value is known, silicon junction temperature can be calculated as follows:

$$T_j = T_C + P_D \times R_{TH(j-c)}$$

Otherwise, starting from ambient temperature measurement, junction temperature can be calculated as follows:

$$T_j = T_A + P_D \times R_{TH(j-a)}$$

Note: $R_{th(j-c)}$ and $R_{th(j-a)}$ values are given in the datasheet.

with:

$$R_{TH(j-a)} = R_{TH(j-c)} + R_{TH(c-h)} + R_{TH(h-a)}$$

and where $R_{TH(c-h)}$ is the thermal interface resistance (grease or foil) and $R_{TH(h-a)}$ is the heatsink thermal resistance.

For more information about the thermal management and power dissipation calculation, refer to the application note:

- AN533: SCRs, TRIACs, and AC switches, thermal management precautions for handling and mounting
- AN604 : Calculation of conduction losses in a power rectifier
- AN4021 : Calculation of reverse losses in a power diode

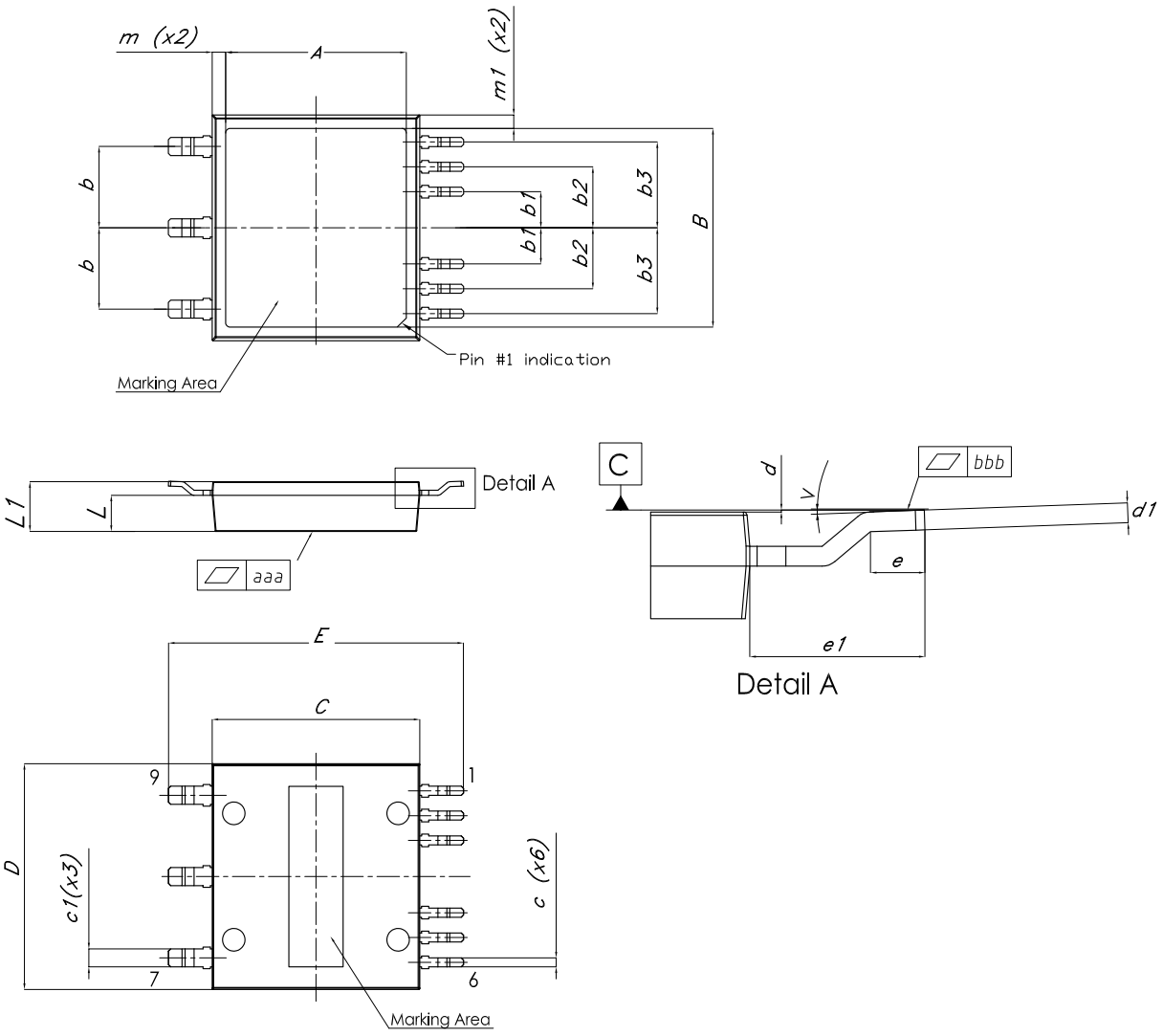
3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 ACEPACK SMIT package information

- Lead-free package leads finishing
- Halogen-free molding compound resin meets UL94 standard level V0

Figure 23. ACEPACK SMIT package outline

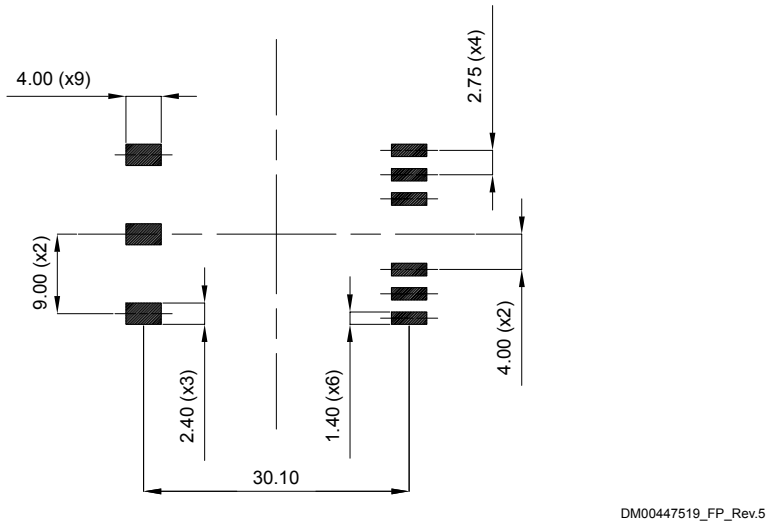


DM00447519_Rev.5

Table 5. ACEPACK SMIT package mechanical data

Dim.	mm			Inches (for reference only)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	19.50	20.00	20.50	0.7677	0.7874	0.8071
B	21.50	22.00	22.50	0.8465	0.8661	0.8858
C	22.80	23.00	23.20	0.8976	0.9055	0.9134
D	24.80	25.00	25.20	0.9764	0.9843	0.9921
E	32.20	32.70	33.20	1.2677	1.2874	1.3071
b		9.00			0.3543	
b1		4.00			0.1575	
b2		6.75			0.2657	
b3		9.50			0.3740	
c	0.95	1.00	1.10	0.0374	0.0394	0.0433
c1	1.95	2.00	2.10	0.0768	0.0787	0.0827
d	0.00		0.15	0.0000	0.0000	0.0059
d1	0.45	0.55	0.65	0.0177	0.0217	0.0256
e	1.30	1.50	1.70	0.0512	0.0591	0.0669
e1	4.65	4.85	5.05	0.1831	0.1909	0.1988
L	3.95	4.00	4.05	0.1555	0.1575	0.1594
L1	5.40	5.50	5.60	0.2126	0.2165	0.2205
m	1.30	1.50	1.80	0.0512	0.0591	0.0709
m1	1.30	1.50	1.80	0.0512	0.0591	0.0709
V	0°	2°	4°	0°	2°	4°
aaa	0.01		0.05		0.0004	0.0020
bbb	0.00		0.10		0.0000	0.0039

Figure 24. ACEPACK SMIT recommended footprint (dimensions are in mm)



Note: Recommended pressing force on package to the heatsink: 50 N as described in application note AN5384.

3.2 ACEPACK SMIT package insulation information

Figure 25. **ACEPACK SMIT package insulation information**

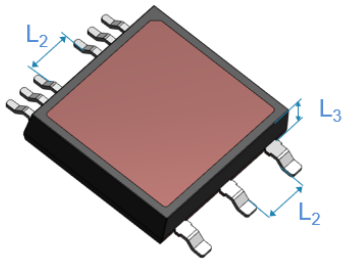


Table 6. **ACEPACK SMIT package insulation characteristics**

Symbol	Parameter			Value	Unit
L2	Pin-to-pin creepage distance	Terminal to terminal: 3 to 4, 7 to 8, 8 to 9	Min.	6.6	mm
L3	Pin-to-backside creepage distance		Min.	4	mm
I_{INS}	RMS tab-to-pin lead insulation current	Duration = 1 s., V_{INS} = 4.8 kV	Max.	1	mA

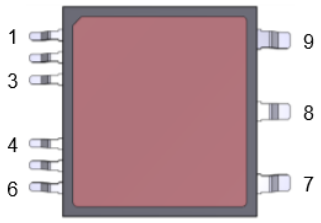
Note: Recommended pressing force on package to the heatsink: 50 N as described in application note AN5384.

3.3 ACEPACK SMIT terminal description

Table 7. **ACEPACK SMIT STTD6050H-12M2Y module pinout description**

Pin #	Name	Description
1	NC	Not connected
2	G1	Gate SCR1
3	G2	Gate SCR2
4	D-	Output minus
5	D-	Output minus
6	D-	Output minus
7	L2	AC line 2
8	L1	AC line 1
9	D+	Output plus

Figure 26. **ACEPACK SMIT STTD6050H-12M2Y module pinout**



TOP VIEW
Pin 1 at cut pad top edge

3.4 ACEPACK SMIT packing information

Figure 27. **ACEPACK SMIT carrier tape outline, bottom view**

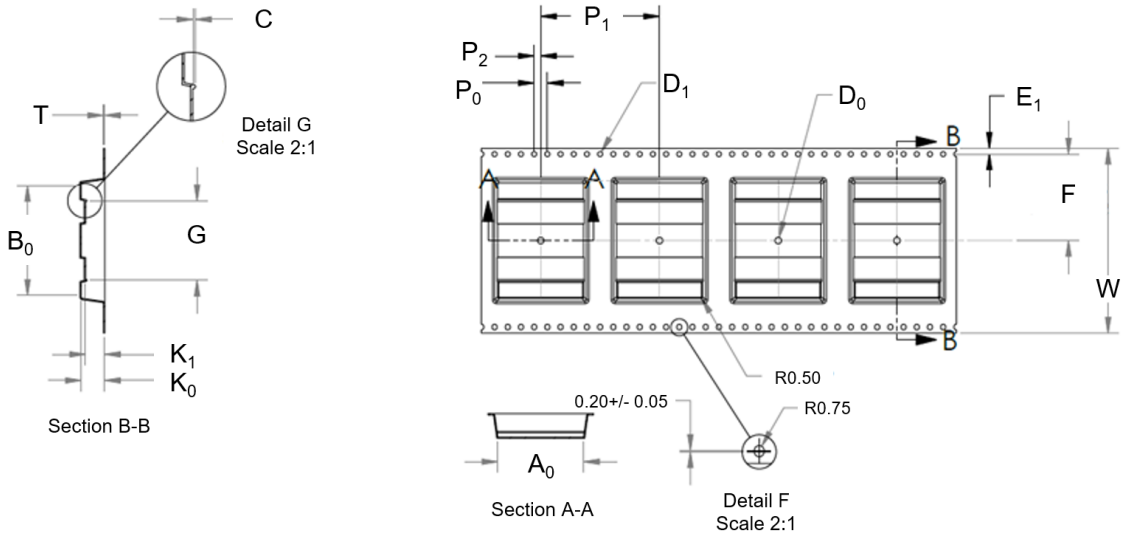


Table 8. **ACEPACK SMIT carrier tape dimensions**

Carrier tape typical dimension (mm)														
A_0	B_0	C	D_0	D_1	E_1	F	G	K_0	K_1	P_0	P_1	P_2	T	W
26.00	33.30	0.40	2.00	1.50	1.75	26.20	24.10	7.10	5.80	4.00	36.00	2.00	0.35	56.00

Figure 28. **ACEPACK SMIT reel outline**

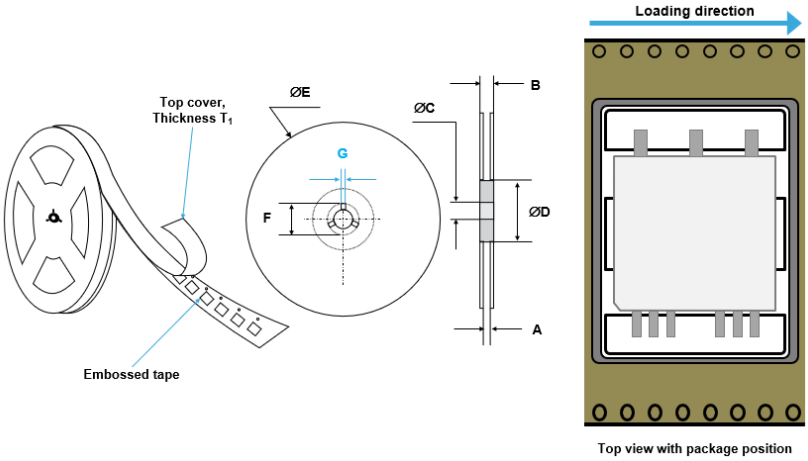


Table 9. **ACEPACK SMIT reel dimensions**

Base qty.	Reel dimension (mm)							
	A	B (max.)	C	D (min.)	E (max.)	F (min.)	G	T_1 (max.)
200	16.4 ±0.3	22.4	13.2 ±0.2	20.2 ±0.25	330	20.2	2.0 ±0.5	0.1

4 Ordering information

Figure 29. **Ordering information scheme**

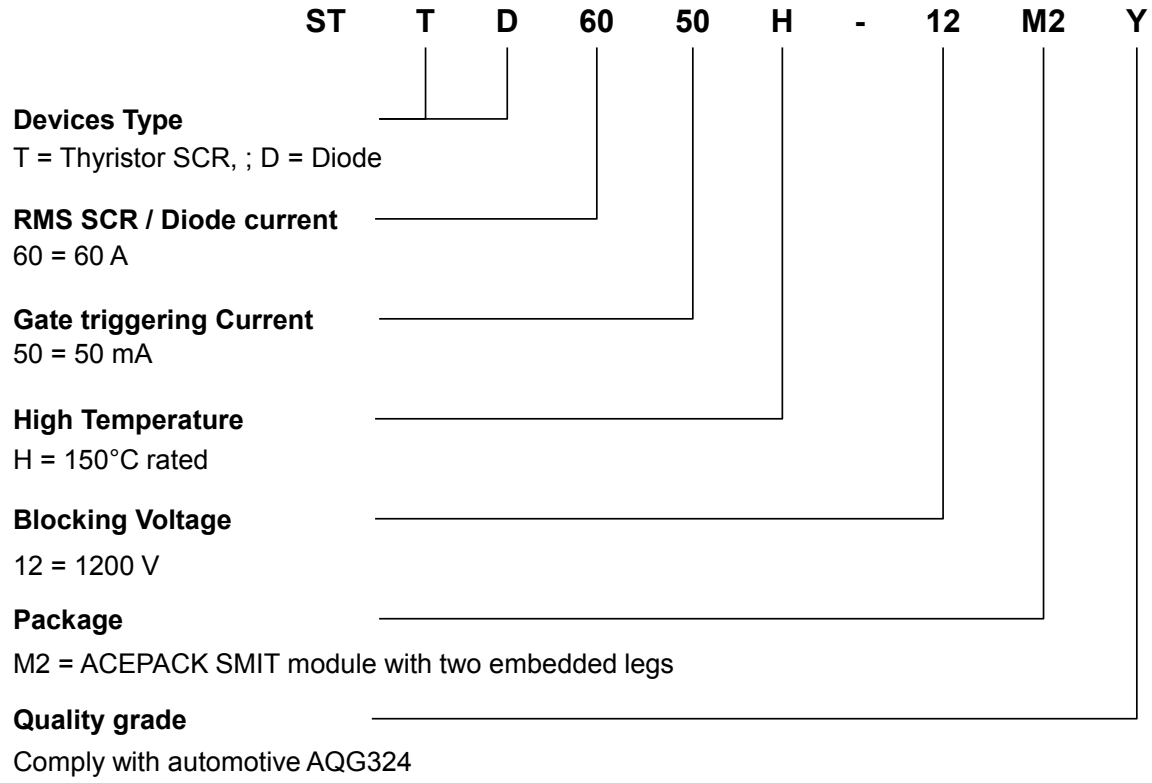


Table 10. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
STTD6050H-12M2Y	STTD6050H12M2Y	ACEPACK SMIT	8.1 g	200	Tape and reel

Revision history

Table 11. **Document revision history**

Date	Version	Changes
14-Apr-2021	1	Initial release.
22-Apr-2021	2	Confidentiality level changed from ST Resctricted to public.