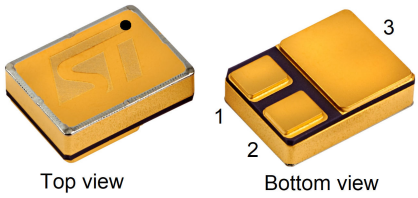
STPS60A150CHR

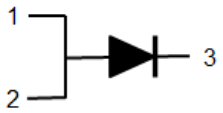
Datasheet

Rad-Hard 2 x 30 A - 150 V Schottky rectifier in SMD.5 package



Top view Bottom view

SMD.5



Terminals 1 and 2: Anode
Terminals 3: cathode

Product status link
STPS60A150CHR

Product summary	
$I_{F(AV)}$	2 x 30 A
V_{RRM}	150 V
T_j(max)	175 °C
$V_{F(max)}$ at 2 x 30 A / 125 °C	0.83 V

Features

- Forward current: 2 x 30 A
- Repetitive peak reverse voltage: 150 V
- Low forward voltage drop
- dV/dt up to 10 kV/µs
- Monolithic dual die - common cathode
- Hermetic package
- TID and SEE characterized
- Package mass: 1 g
- ESCC qualified : 5106/023

Description

The STPS60A150CHR is package and screened to comply with the ESCC5000 specification for aerospace products. It is a dual monolithic Schottky rectifier assembled in an SMD.5 hermetic package and characterized in total dose at high dose rate and in single event effect to be used in aerospace applications. It is ESCC qualified.

The complete ESCC specification for this device is available from the European Space Agency web site. ST guarantees full compliance of qualified parts with the ESCC detailed specification.

1 Characteristics

1.1 Absolute maximum ratings

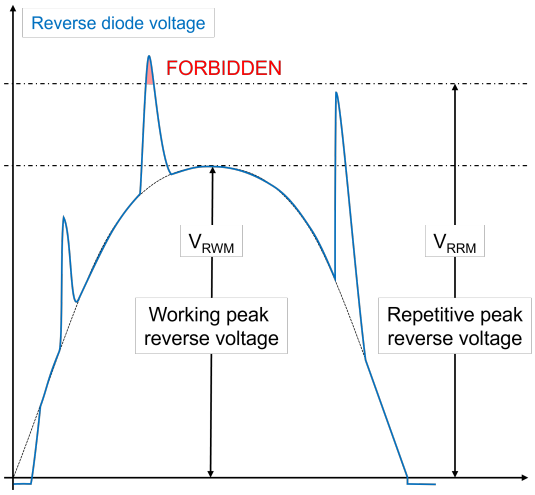
The absolute maximum ratings are limiting values at 25°C, per diode unless otherwise notified. Values provided in Table 1 shall not be exceeded at any time during use or storage

Table 1. Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{RRM}(1)	Repetitive peak reverse voltage		150	V
V_{RWM}(1)	Peak working reverse voltage		150	V
I_O(2)	Average output rectified current	Per diode	30	A
		Per package	60	A
I_{FSM}	Non repetitive surge forward current	t_p = 10 ms sinusoidal, T_J = 25 °C	190	A
dV/dt(3)	Reverse voltage maximum rise rate (4)		10	kV/µs
T_{op}	Operating temperature range (case temperature)		-65 to +175	°C
T_j(5)	Maximum operating junction temperature		+175	°C
T_{stg}	Storage temperature range		-65 to +175	°C
T_{sol}(6)	Maximum soldering temperature(4)		+245	°C
ESD	Electro static discharge	Air discharge, HBM model, class 3	8	kV

1. *See Figure 1.*
2. *Per diode: for T_{case} > +74 °C, derate linearly to 0 A at +175 °C. Per device: for case > +44 °C, derate linearly to 0 A at +175 °C.*
3. *Evaluated by characterization. Tested in production at 25 °C on 5 parts per wafer lot.*
4. *V_{RRM} from stationary no-conduction state to V_{RRM} < V_{RRM} max*
5. *$(dP_{tot}/dT_j) < (1/R_{th(j-a)})$ condition to avoid thermal runaway for a diode on its own heatsink.*
6. *Duration 5 seconds maximum with at least 3 minutes between consecutive temperature peaks.*

Figure 1. V_{RRM} and V_{WRM} definition with their waveform



1.2 Thermal parameters

Table 2. Thermal parameters

Symbol	Parameter		Typ. value	Max. value	Unit
$R_{th(j-c)}$	Thermal resistance, junction to case[1]	Per diode	-	3.4	°C/W
		Per package	-	2.2	

1. *When only 1 diode is used, the dissipation is made from a part of the die, hence to a higher thermal resistance.*

1.3 Electrical characteristics

Limiting value per diodes, unless otherwise specified.

Table 3. Static electrical characteristics

Symbol	Parameter	MIL-STD-750 test method	Test conditions		Min.	Typ.	Max.	Unit
I_R (1)	Reverse leakage current	4016	DC method, V_R = 150 V	T_j = 25 °C	-		14	µA
				T_j = 125 °C	-	2.0	8	mA
V_{F1} (2)(3)	Forward voltage drop	4011	I_F = 5 A	T_j = -55 °C	-	0.77	0.84	V
				T_j = 25 °C	-	0.70	0.78	
				T_j = 125 °C	-	0.56	0.62	
			I_F = 10 A	T_j = -55 °C	-	0.92	1.03	
				T_j = 25 °C	-	0.77	0.85	
				T_j = 125 °C	-	0.62	0.69	
			I_F = 20 A	T_j = -55 °C	-	1.27	1.435	
				T_j = 25 °C	-	0.85	0.93	
				T_j = 125 °C	-	0.70	0.78	
			I_F = 30 A	T_j = -55 °C	-	1.65	1.87	
				T_j = 25 °C	-	0.90	0.99	
				T_j = 125 °C	-	0.76	0.83	
C (3)	Junction capacitance	4001	V_R = 10 V, F = 1 MHz	T_j = 25 °C	-	237	310	pF

1. *100% tested at 25 °C. Compliance with the 125 °C specification is supported by simulation, characterization and, as per STMicroelectronics wafer lot acceptance procedure, by sampling on 5 parts per wafer lot, with an acceptance criteria of 0. In case of fail, a 100% test is performed.*
2. *Pulse width 680 µs, duty cycle ≤ 2%*
3. *Compliance with the specification is supported by simulation, characterization and, as per STMicroelectronics wafer lot acceptance procedure, by sampling on 5 parts per wafer lot, with an acceptance criteria of 0. In case of fail, a 100% test is performed.*

1.4 Characteristics (curves)

Figure 2. Average forward current versus case temperature (DC, per diode)

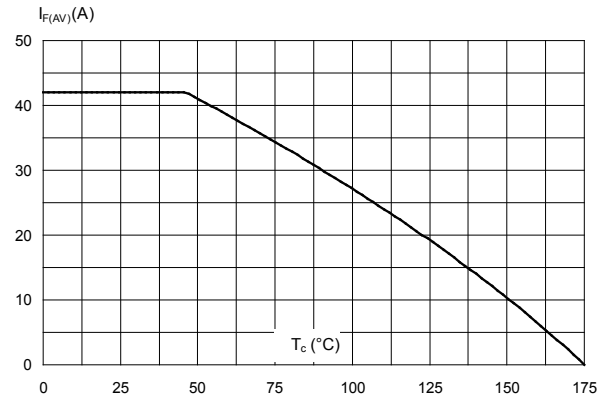


Figure 3. Forward voltage drop versus forward current (typical values, per diode)

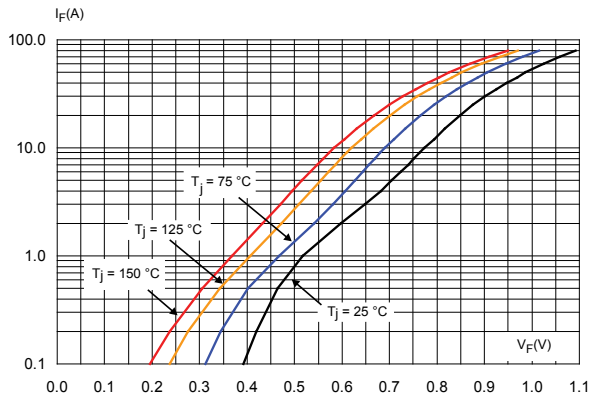


Figure 4. Reverse leakage current versus reverse voltage (typical values, per diode)

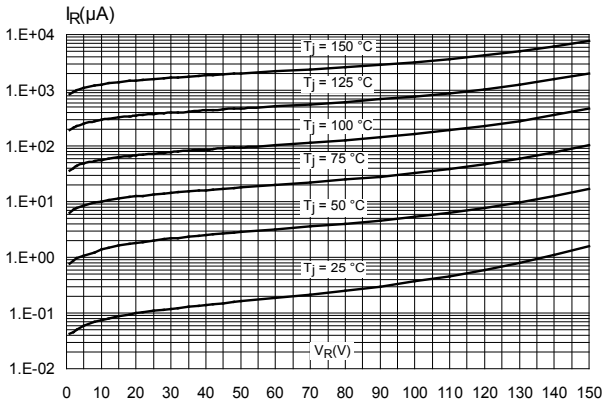


Figure 5. Relative variation of $Z_{th(j-c)}$ versus pulse duration

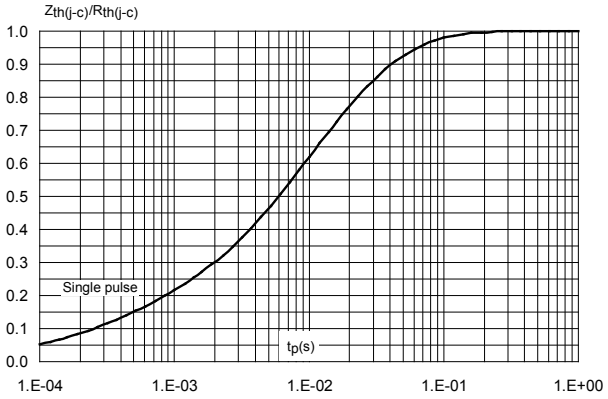
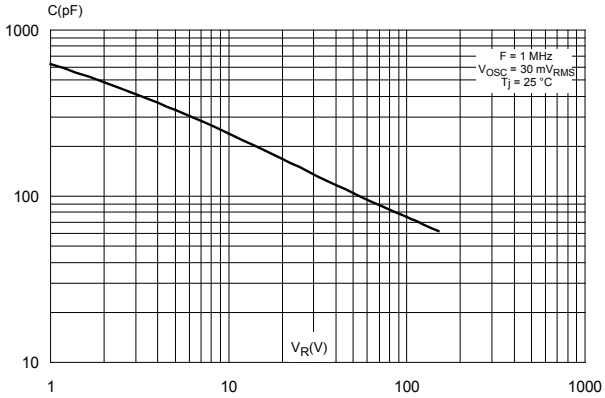


Figure 6. Junction capacitance versus reverse voltage (typical values, per diode)



2 Radiation

The technology of the STMicroelectronics Rad-Hard rectifier's diodes is intrinsically highly resistant to radiative environments.

The product radiation hardness assurance is supported by a total ionisation dose (TID) test at high dose rate and a single effect event (SEE) characterization.

2.1 Total dose radiation (TID) testing

The part has been characterized in total ionizing dose at high dose rate on 12 parts packaged in SMD.5, 4 parts unbiased, 4 parts reverse biased and 4 parts forward biased. All parts were from the same wafer lot.

The irradiation has been done according to the ESCC 22900 specification, standard window.

Both pre-irradiation and post-irradiation performances have been tested using the same circuitry and test conditions for a direct comparison can be done (T_{amb} = 22 ±3 °C unless otherwise specified).

The following parameters were measured :

- Before irradiation
- After irradiation at final dose 3 Mrad (Si)
- After 168 hrs at room temperature
- after 168 hrs at 100 °C anneal

Based on this characterization, the device is deemed able to sustain 3 Mrad(Si) while maintaining all its parameters within its specifications.

2.2 Single event effect

The Single Event Effect (SEE) relevant to power rectifiers are characterized, i.e. the Single Event Burnout (SEB).

The tests are performed as per ESCC 25100, each one on 3 pieces from 1 wafer at room temperature.

The accept/reject criteria are :

- SEB (Destructive mode):
  The diode is reverse biased during irradiation. The test is stopped as soon as a SEB occurs or when the reverse leakage current is above the specification or when the overall fluency on the component reaches 1E7 cm².
- Post irradiation stress test (PIST):
  After the irradiation, a stress is applied to the diode in order to reveal any latent damage on the irradiated devices.
  The reverse voltage value is increased from 0 V to 100% of $V_R$max. and then decreased from 100% of the $V_R$max. to 0 V. At each step, the reverse leakage current value is measured.

Table 4. Radiation hardness assurance summary

Type	Conditions	Result
Total ionisation dose	High dose rate 4 reverse biased + 4 forward biased + 4 unbiased	Immune up to 3 Mrad(Si)
Single effect burnout	LET : 62.5 MeV.cm²/mg: $V_r \leq 100\%\ V_{Rmax}$	No burnout
PIST	LET : 62.5 MeV.cm²/mg: • $V_r \leq 85\%\ V_{Rmax}$ • $V_r \leq 55\%\ V_{Rmax}$ LET : 32.4 MeV.cm²/mg: $V_r \leq 100\%\ V_{Rmax}$	Part functional(1) Part fully compliant to specification Part fully compliant to specification

1. *I_r gets above its max specification during the test without recovery.*

3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 SMD.5 package information

The top metallic lid is not connected to any part of the die nor any terminal of the package.

Figure 7. Surface mount SMD.5 package outline (3-terminal)

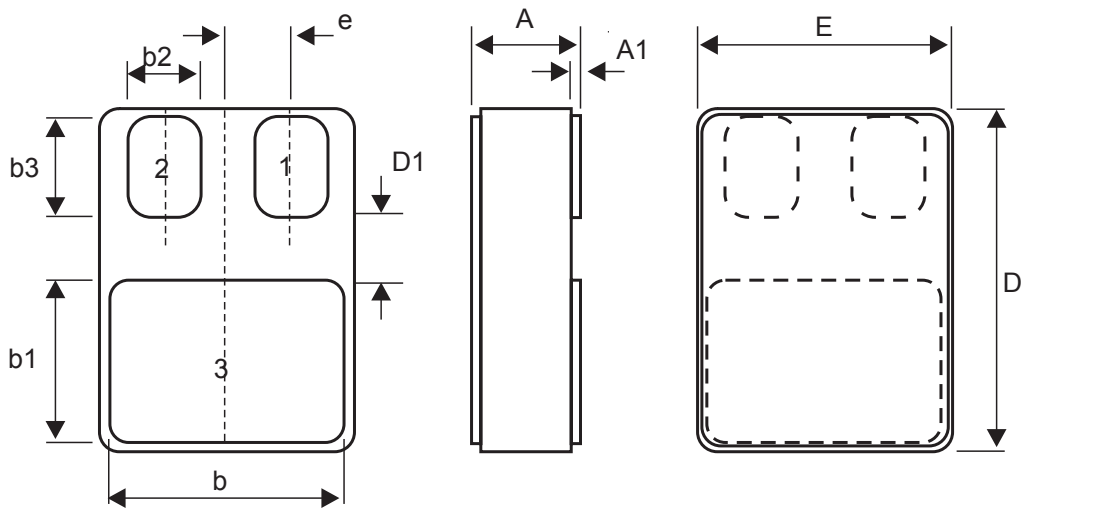


Table 5. SMD.5 package mechanical data

Symbols	Dimensions (mm)			Dimensions (inches)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.84		3.30	0.112		0.130
A1	0.25	0.38	0.51	0.010	0.015	0.020
b	7.13	7.26	7.39	0.281	0.286	0.291
b1	5.58	5.72	5.84	0.220	0.225	0.230
b2[1]	2.28	2.41	2.54	0.090	0.095	0.100
b3	2.92	3.05	3.18	0.115	0.120	0.125
D	10.03	10.16	10.28	0.395	0.400	0.405
D1	0.76			0.030		
E	7.39	7.52	7.64	0.291	0.296	0.301
e		1.91 BSC			0.075	

1. 2 locations

4 Ordering information

Table 6. Ordering information

Order code	ESCC detail specification	Quality level	Package	Lead finishing	Marking	Mass	Base qty	Packing
STPS60A150CS1	-	Design model	SMD.5	Gold	STPS60A150CS1	1 g	20	Strip pack
STPS60A150CSG	5106/023/02	Flight model			510602302			
STPS60A150CST	5106/023/06	Flight Model		Hot solder dip	510602306			

Note: Contact ST sales office for information about the specific conditions for products in die form.

5 Other information

5.1 Traceability information

Figure 8. **Product marking outline, flight model top view**

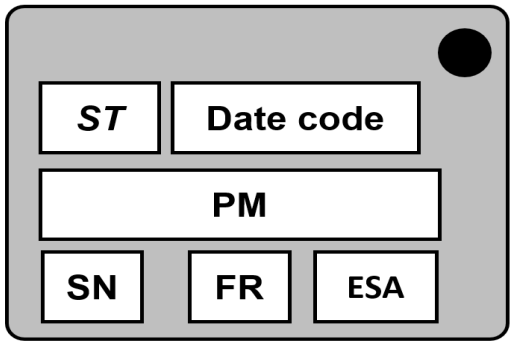


Figure 9. **Product marking outline, engineering model top view**

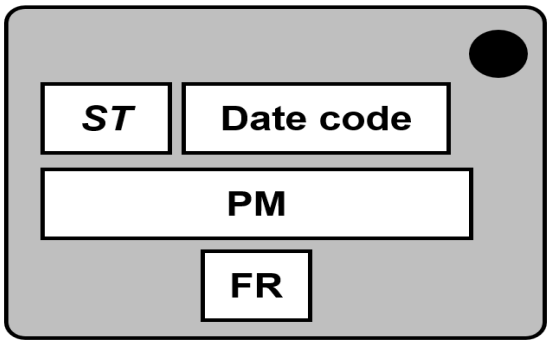


Table 7. **Product marking description**

Field	Model	Description
ST	Engineering and flight	Standard ST logo
PM	Engineering	Product part number
	Flight	ESCC part number
Date code	Engineering	3yywwN(1)
	Flight	yywwN(2)
SN	Flight	Serialization number
ESA	Flight	ESA logo
FR	Engineering and flight	Country of origin

1. *yy= year ; ww = week ; N = alfa-numeric digit for lot of week; 3 = EM type*
2. *yy= year ; ww = week ; N = alfa-numeric digit for lot of week*

Note: Black dot marks terminal 1 position underneath.

5.2 Packing information

Figure 10. **Strip pack view, label side**

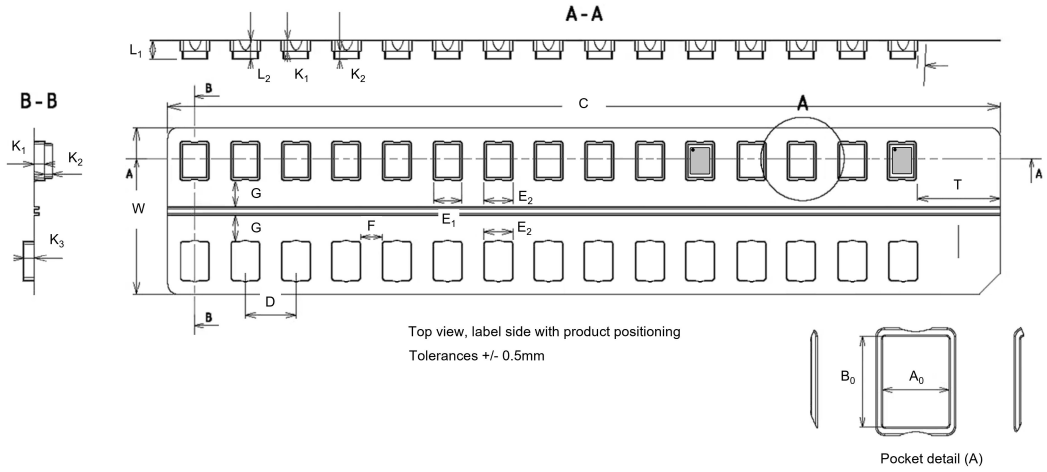


Table 8. **Strip pack dimension data**

Strip pack typical dimension (mm)														
A0	B0	C	D	E1	E2	F	G	K1	K2	K3	L1	L2	T	W
7.80	10.40	400.00	18.20	9.50	10.00	8.10	12.00	5.00	3.30	5.00	8.60	8.30	39.20	70.00

5.3 Documentation

In the Table 9 is a summary of the documentation provided with each type of products. Further quality information on engineering model product is also available in the technical note TN1181.

Table 9. **Documentation provided for each type of product**

Quality level	Documentation
Engineering model	Certificate of conformance including : • Customer name • Customer purchase order number • ST sales order number and item • ST commercial product code • Quantity delivered • Date code • Reference data sheet • Reference to TN1181 on engineering models • ST Rennes assembly lot ID number
Flight model	Certificate of conformance including : • Customer name • Customer purchase order number • ST sales order number and item • ST commercial product code • Quantity delivered • Date code • Serial numbers • Wafer diffusion plant location and wafer size • Wafer diffusion lot ID number and wafer ID number • Reference of the applicable ESCC qualification maintenance lot • Reference to the ESCC detail specification • ST Rennes assembly lot ID number

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
06-Dec-2018	1	First issue.
18-Sep-2019	2	Added Section 1.4 .Updated Section 1.3 Electrical characteristics and Table 7.
24-Sep-2019	3	Updated Table 1, Figure 4 and Figure 5.
24-Sep-2020	4	Updated title description and *Table 1*.
03-Nov-2020	5	Updated *Features*, *Table 1* and *Table 4*.
26-Jan-2022	6	Updated *Features* and *Table 1*. Added Figure 1.
25-Nov-2025	7	Updated Section Features, and Table 6.

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