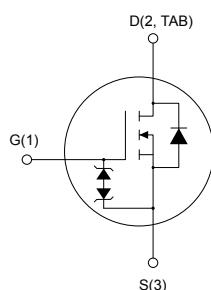
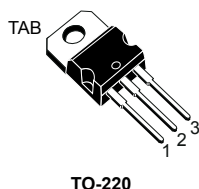


## N-channel 800 V, 3.5 $\Omega$ typ., 2 A MDmesh K5 Power MOSFET in a TO-220 package



### Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|------------|----------|-------------------|-------|
| STP2N80K5  | 800 V    | 4.5 $\Omega$      | 2 A   |

- Industry's lowest  $R_{DS(on)}$  x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



#### Product status link

[STP2N80K5](#)

#### Product summary

|            |           |
|------------|-----------|
| Order code | STP2N80K5 |
| Marking    | 2N80K5    |
| Package    | TO-220    |
| Packing    | Tube      |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value      | Unit               |
|----------------|-------------------------------------------------------------------|------------|--------------------|
| $V_{GS}$       | Gate-source voltage                                               | $\pm 30$   | V                  |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 2          | A                  |
|                | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 1.3        |                    |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 8          | A                  |
| $P_{TOT}$      | Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$     | 45         | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 4.5        | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                         | 50         | V/ns               |
| $T_{stg}$      | Storage temperature range                                         | -55 to 150 | $^{\circ}\text{C}$ |
| $T_J$          | Operating junction temperature range                              |            | $^{\circ}\text{C}$ |

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 2\text{ A}$ ,  $di/dt = 100\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ .
3.  $V_{DS} \leq 640\text{ V}$ .

**Table 2. Thermal data**

| Symbol     | Parameter                               | Value | Unit                        |
|------------|-----------------------------------------|-------|-----------------------------|
| $R_{thJC}$ | Thermal resistance, junction-to-case    | 2.78  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thJA}$ | Thermal resistance, junction-to-ambient | 62.5  | $^{\circ}\text{C}/\text{W}$ |

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                              | Value | Unit |
|----------|------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)                                    | 0.5   | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 60.5  | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

**Table 4. On/off-state**

| Symbol        | Parameter                         | Test conditions                                                                             | Min. | Typ. | Max.     | Unit          |
|---------------|-----------------------------------|---------------------------------------------------------------------------------------------|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                 | 800  |      |          | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$                                             |      |      | 1        | $\mu\text{A}$ |
|               |                                   | $V_{DS} = 800\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$ |      |      | 50       |               |
| $I_{GSS}$     | Gate body leakage current         | $V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$                                          |      |      | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$                                          | 3    | 4    | 5        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 1\text{ A}$                                                 |      | 3.5  | 4.5      | $\Omega$      |

1. Specified by design, not tested in production.

**Table 5. Dynamic**

| Symbol            | Parameter                             | Test conditions                                                                                                                             | Min. | Typ. | Max. | Unit     |
|-------------------|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$         | Input capacitance                     | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                                        | -    | 105  | -    | pF       |
| $C_{oss}$         | Output capacitance                    |                                                                                                                                             | -    | 8    | -    | pF       |
| $C_{rss}$         | Reverse transfer capacitance          |                                                                                                                                             | -    | 0.5  | -    | pF       |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance time related   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }640\text{ V}$                                                                                 | -    | 16   | -    | pF       |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance energy related |                                                                                                                                             | -    | 7    | -    | pF       |
| $R_g$             | Intrinsic gate resistance             | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                     | -    | 18   | -    | $\Omega$ |
| $Q_g$             | Total gate charge                     | $V_{DD} = 640\text{ V}$ , $I_D = 2\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 15. Test circuit for gate charge behavior) | -    | 5    | -    | nC       |
| $Q_{gs}$          | Gate-source charge                    |                                                                                                                                             | -    | 1    | -    | nC       |
| $Q_{gd}$          | Gate-drain charge                     |                                                                                                                                             | -    | 3.7  | -    | nC       |

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

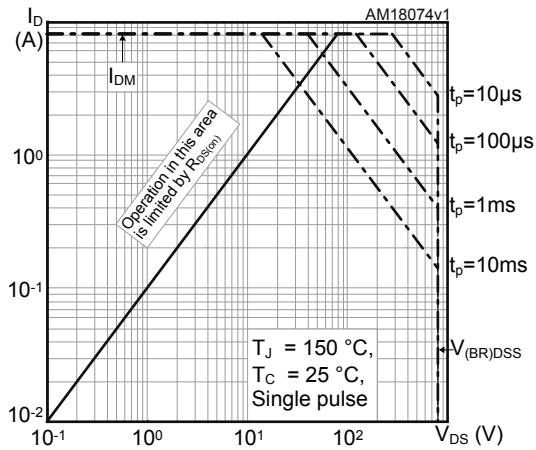
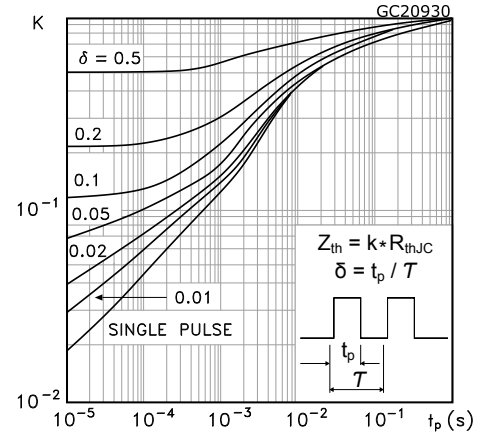
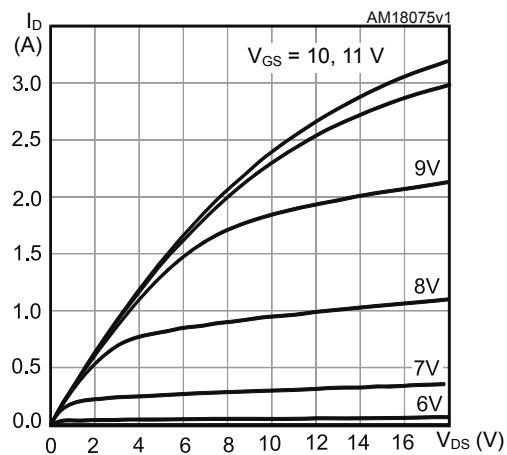
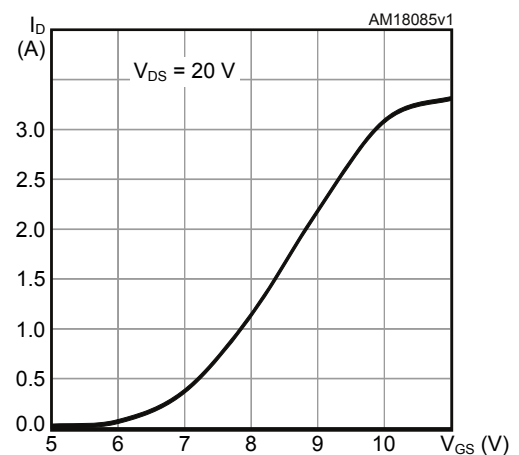
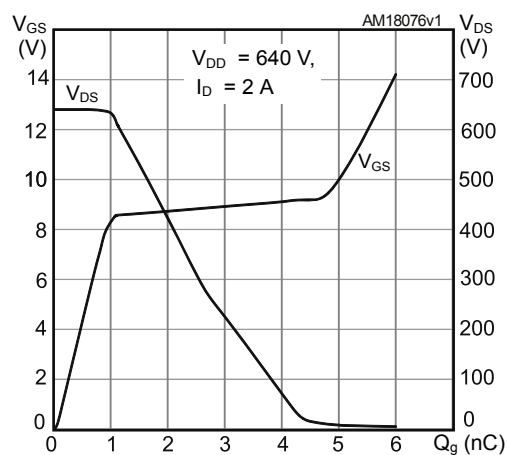
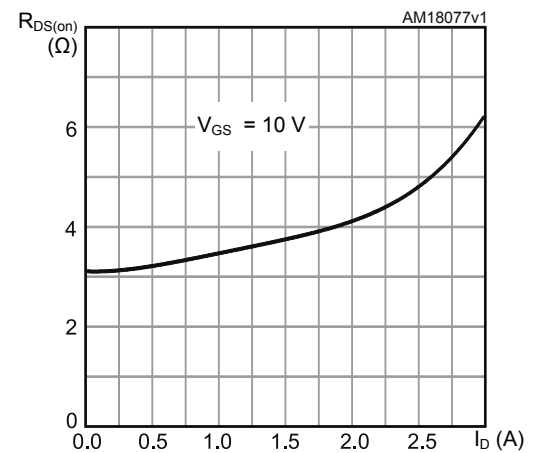
| Symbol       | Parameter           | Test conditions                                                                                         | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 400\text{ V}$ , $I_D = 1\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$    | -    | 8    | -    | ns   |
| $t_r$        | Rise time           |                                                                                                         | -    | 12   | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform) | -    | 19   | -    | ns   |
| $t_f$        | Fall time           |                                                                                                         | -    | 32   | -    | ns   |

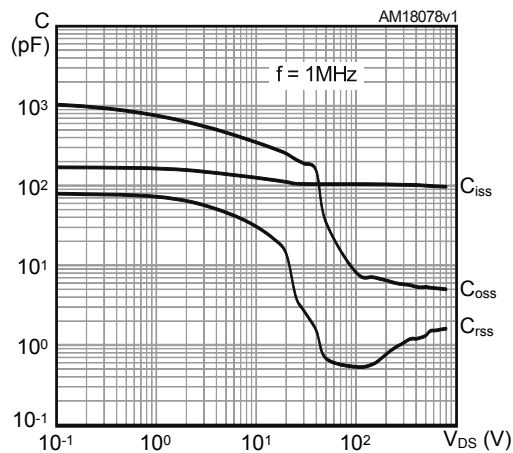
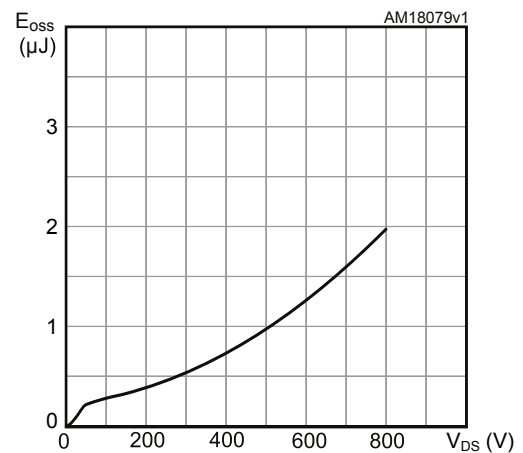
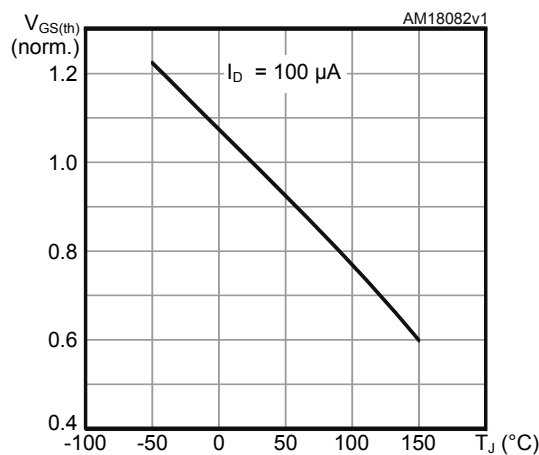
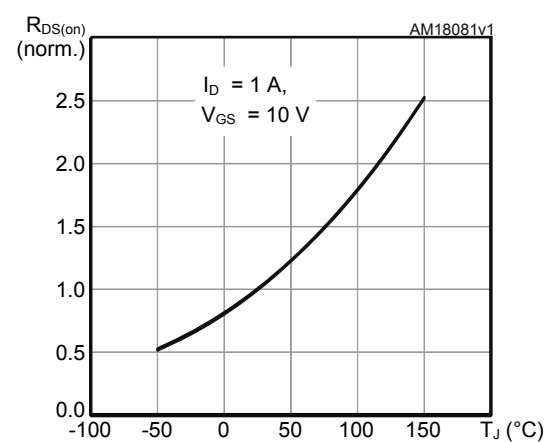
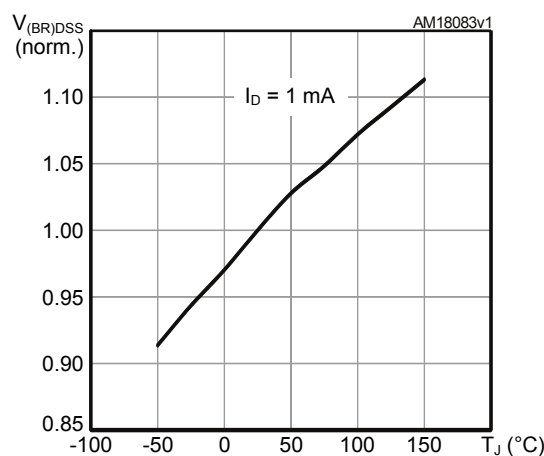
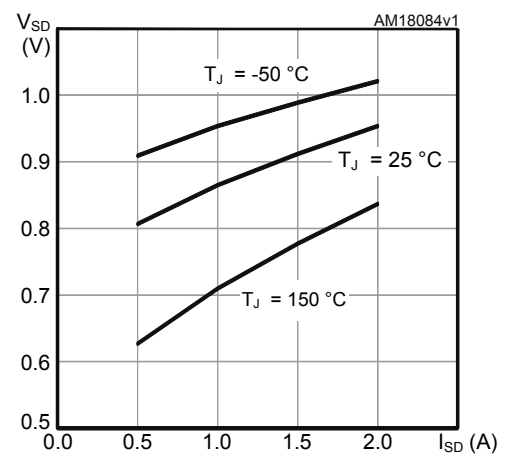
**Table 7. Source-drain diode**

| Symbol          | Parameter                     | Test conditions                                                                                                                                                                                                   | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                                                                                                   | -    |      | 2    | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                                                                                                   | -    |      | 8    | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 2\text{ A}$ , $V_{GS} = 0\text{ V}$                                                                                                                                                                     | -    |      | 1.5  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$<br>(see Figure 16. Test circuit for inductive load switching and diode recovery times)                                     | -    | 255  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                   | -    | 1    |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                   | -    | 8    |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 2\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$<br>(see Figure 16. Test circuit for inductive load switching and diode recovery times) | -    | 285  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                                                                                                   | -    | 1.45 |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                                                                                                   | -    | 7.5  |      | A             |

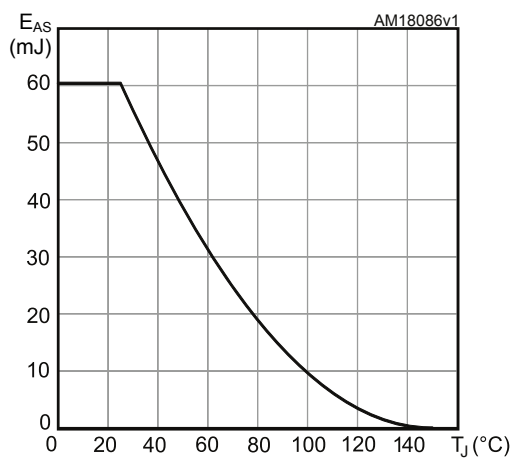
1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

**Figure 2. Thermal impedance**

**Figure 3. Output characteristics**

**Figure 4. Transfer characteristics**

**Figure 5. Gate charge vs gate-source voltage**

**Figure 6. Static drain-source on-resistance**


**Figure 7. Capacitance variations**

**Figure 8. Output capacitance stored energy**

**Figure 9. Normalized gate threshold voltage vs temperature**

**Figure 10. Normalized on-resistance vs temperature**

**Figure 11. Normalized V\_(BR)DSS vs temperature**

**Figure 12. Source-drain diode forward characteristics**


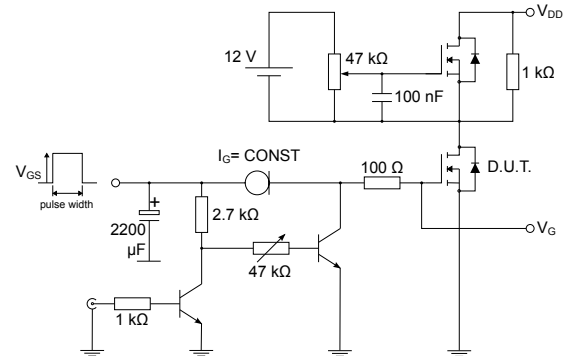
**Figure 13. Maximum avalanche energy vs starting  $T_J$**



### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


AM01468v1

**Figure 15. Test circuit for gate charge behavior**


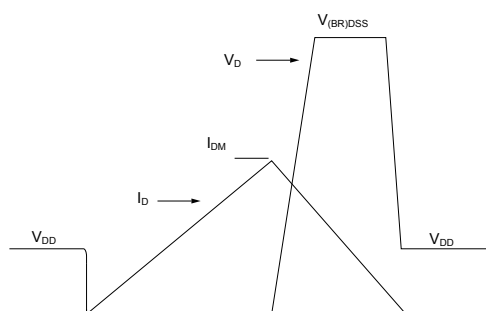
AM01469v1

**Figure 16. Test circuit for inductive load switching and diode recovery times**

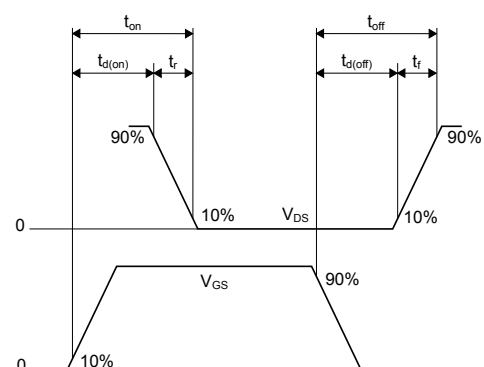

AM01470v1

**Figure 17. Unclamped inductive load test circuit**


AM01471v1

**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


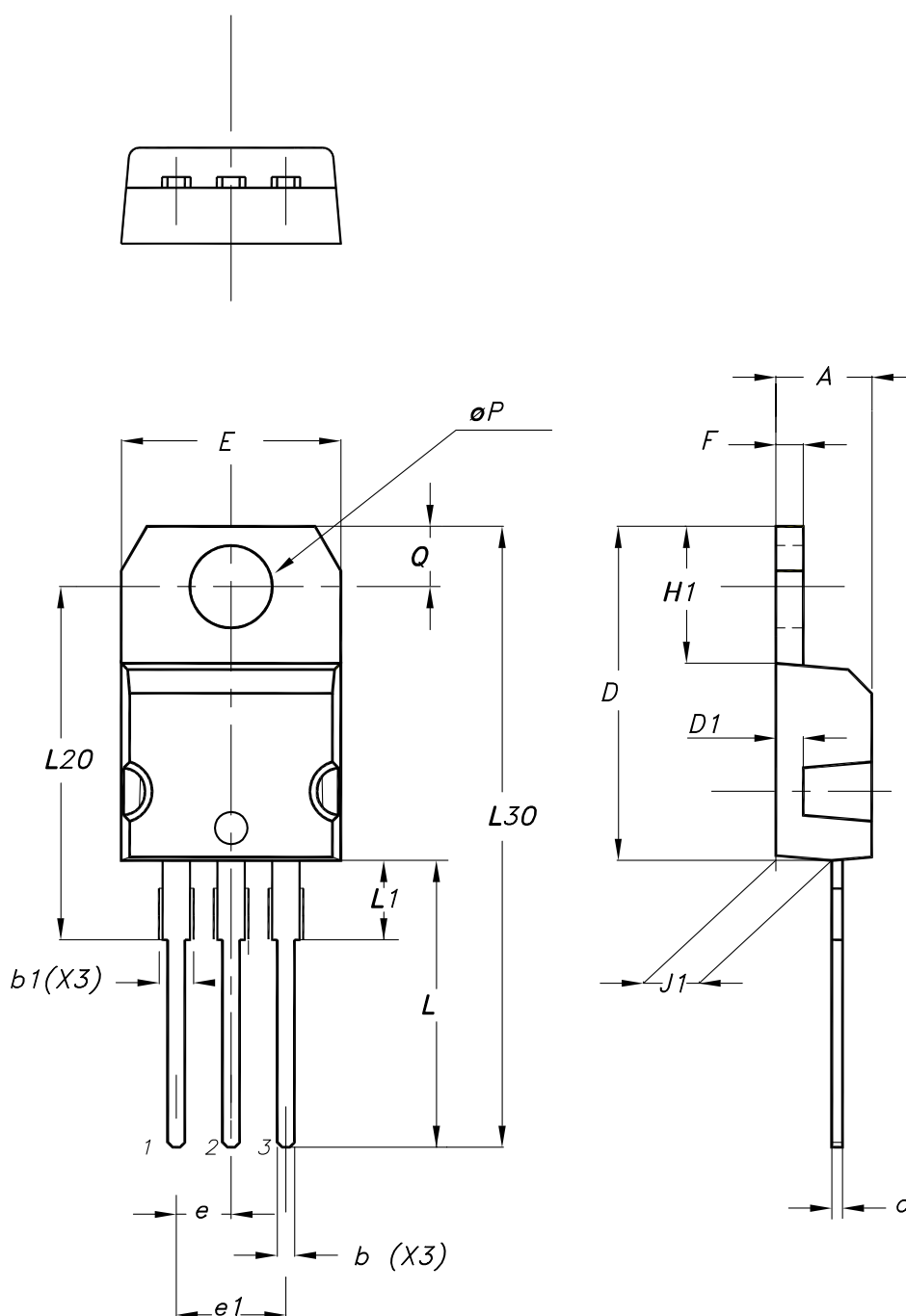
AM01473v1

## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220 type A package information

Figure 20. TO-220 type A package outline



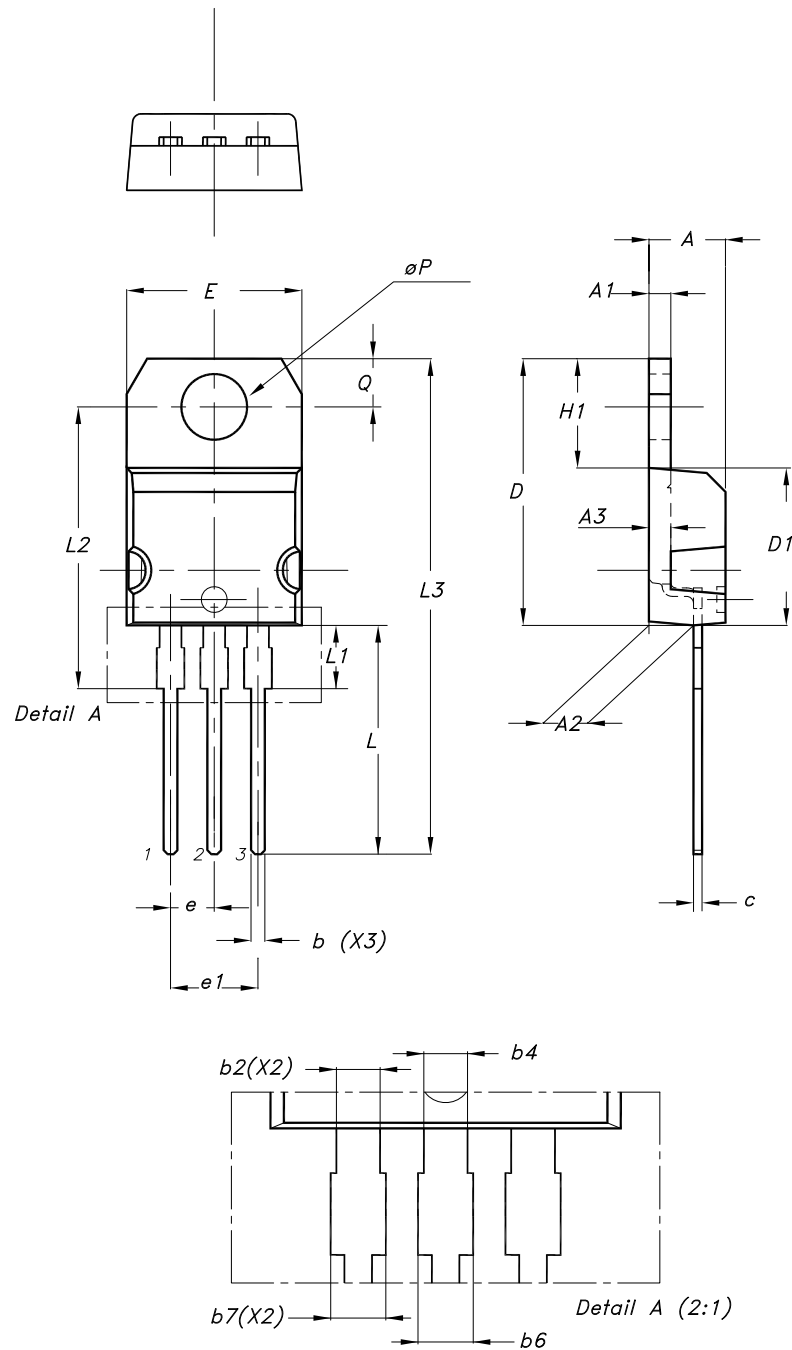
0015988\_typeA\_Rev\_23

**Table 8. TO-220 type A package mechanical data**

| Dim.          | mm    |       |       |
|---------------|-------|-------|-------|
|               | Min.  | Typ.  | Max.  |
| A             | 4.40  |       | 4.60  |
| b             | 0.61  |       | 0.88  |
| b1            | 1.14  |       | 1.55  |
| c             | 0.48  |       | 0.70  |
| D             | 15.25 |       | 15.75 |
| D1            |       | 1.27  |       |
| E             | 10.00 |       | 10.40 |
| e             | 2.40  |       | 2.70  |
| e1            | 4.95  |       | 5.15  |
| F             | 1.23  |       | 1.32  |
| H1            | 6.20  |       | 6.60  |
| J1            | 2.40  |       | 2.72  |
| L             | 13.00 |       | 14.00 |
| L1            | 3.50  |       | 3.93  |
| L20           |       | 16.40 |       |
| L30           |       | 28.90 |       |
| øP            | 3.75  |       | 3.85  |
| Q             | 2.65  |       | 2.95  |
| Slug flatness |       | 0.03  | 0.10  |

## 4.2 TO-220 type H package information

**Figure 21.** TO-220 type H package outline



0015988\_H\_23

**Table 9. TO-220 type H package mechanical data**

| Dim.          | mm    |       |       |
|---------------|-------|-------|-------|
|               | Min.  | Typ.  | Max.  |
| A             | 4.40  | 4.45  | 4.50  |
| A1            | 1.22  |       | 1.32  |
| A2            | 2.49  | 2.59  | 2.69  |
| A3            | 1.17  | 1.27  | 1.37  |
| b             | 0.78  |       | 0.87  |
| b2            | 1.25  |       | 1.34  |
| b4            | 1.20  |       | 1.29  |
| b6            |       |       | 1.50  |
| b7            |       |       | 1.45  |
| c             | 0.49  |       | 0.56  |
| D             | 15.40 | 15.50 | 15.60 |
| D1            | 9.05  | 9.15  | 9.25  |
| E             | 10.08 | 10.18 | 10.28 |
| e             | 2.44  | 2.54  | 2.64  |
| e1            | 4.98  | 5.08  | 5.18  |
| H1            | 6.25  | 6.35  | 6.45  |
| L             | 13.20 | 13.40 | 13.60 |
| L1            | 3.50  | 3.70  | 3.90  |
| L2            | 16.30 | 16.40 | 16.50 |
| L3            | 28.70 | 28.90 | 29.10 |
| ØP            | 3.75  | 3.80  | 3.85  |
| Q             | 2.70  | 2.80  | 2.90  |
| Slug flatness |       | 0.03  | 0.10  |

## Revision history

**Table 10. Document revision history**

| Date        | Revision | Changes                                                                         |
|-------------|----------|---------------------------------------------------------------------------------|
| 07-Dec-2023 | 1        | First release. The part number STP2N80K5 was previously inserted in the DS9820. |

---

## Contents

|          |                                           |           |
|----------|-------------------------------------------|-----------|
| <b>1</b> | <b>Electrical ratings .....</b>           | <b>2</b>  |
| <b>2</b> | <b>Electrical characteristics.....</b>    | <b>3</b>  |
| 2.1      | Electrical characteristics (curves) ..... | 5         |
| <b>3</b> | <b>Test circuits .....</b>                | <b>8</b>  |
| <b>4</b> | <b>Package information.....</b>           | <b>9</b>  |
| 4.1      | TO-220 type A package information .....   | 9         |
| 4.2      | TO-220 type H package information .....   | 11        |
|          | <b>Revision history .....</b>             | <b>13</b> |

**IMPORTANT NOTICE – READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved