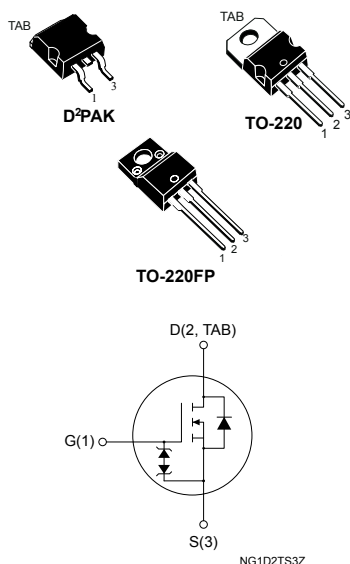




N-channel 400 V, 0.47 Ω typ., 9 A SuperMESH Power MOSFETs
in a D²PAK, TO-220 and TO-220FP packages



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB11NK40ZT4	400 V	0.55 Ω	9 A
STP11NK40Z			
STP11NK40ZFP			

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.



Product status links

[STB11NK40ZT4](#)

[STP11NK40Z](#)

[STP11NK40ZFP](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK, TO-220	TO-220FP	
V _{DS}	Drain-source voltage	400		V
V _{GS}	Gate-source voltage	±30		V
I _D	Drain current (continuous) at T _C = 25 °C	9	9 ⁽¹⁾	A
	Drain current (continuous) at T _C = 100 °C	5.67	5.67 ⁽¹⁾	
I _{DM} ⁽²⁾	Drain current (pulsed)	36	36 ⁽¹⁾	A
P _{TOT}	Total dissipation at T _C = 25 °C	110	30	W
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	3.5		kV
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)		2.5	kV
T _J	Operating junction temperature range	-55 to 150		°C
T _{stg}	Storage temperature range			

1. Limited by maximum junction temperature.

2. Pulse width limited by safe operating area.

3. I_{SD} ≤ 9 A, di/dt ≤ 200 A/μs, V_{DD} = 320 V.

Table 2. Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	TO-220	TO-220FP	
R _{thJC}	Thermal resistance, junction-to-case	1.14		4.17	°C/W
R _{thJA}	Thermal resistance, junction-to-ambient	50 ⁽¹⁾	62.5		°C/W

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _J max.)	9	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	190	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	400			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			50	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 4.5\text{ A}$		0.47	0.55	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	930	-	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Reverse transfer capacitance		-	30	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }320\text{ V}$, $V_{GS} = 0\text{ V}$	-	78	-	pF
Q_g	Total gate charge	$V_{DD} = 320\text{ V}$, $I_D = 9\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 16. Test circuit for gate charge behavior)	-	32	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	18.5	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 200\text{ V}$, $I_D = 4.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	20	-	ns
t_r	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	40	-	ns
t_f	Fall time		-	18	-	ns
$t_{r(voff)}$	Off-voltage rise time	$V_{DD} = 320\text{ V}$, $I_D = 9\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	15	-	ns
t_f	Fall time		-	17	-	ns
t_c	Cross-over time		-	30	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 9\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 9\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 45\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	225		ns
Q_{rr}	Reverse recovery charge		-	1.6		μC
I_{RRM}	Reverse recovery current		-	14		A

1. Pulse width is limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

Figure 1. Safe operating area for TO-220, D²PAK

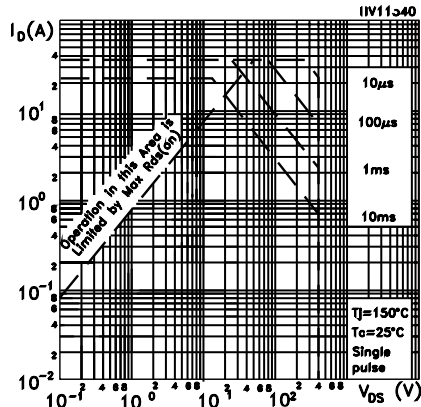


Figure 2. Thermal impedance for TO-220, D²PAK

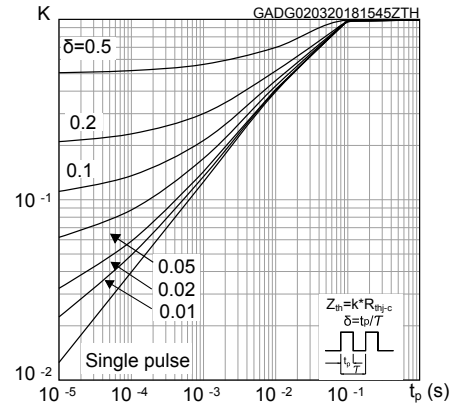


Figure 3. Safe operating area for TO-220FP

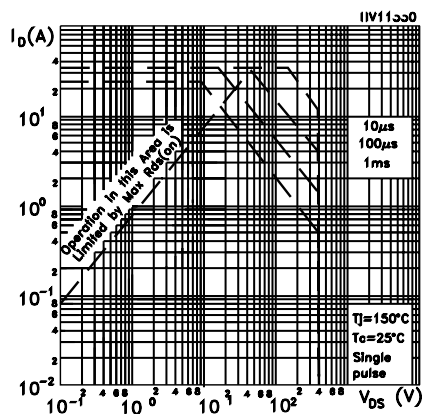


Figure 4. Thermal impedance for TO-220FP

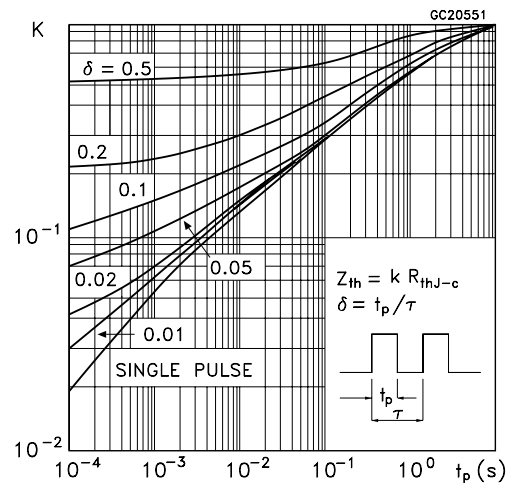


Figure 5. Typical output characteristics

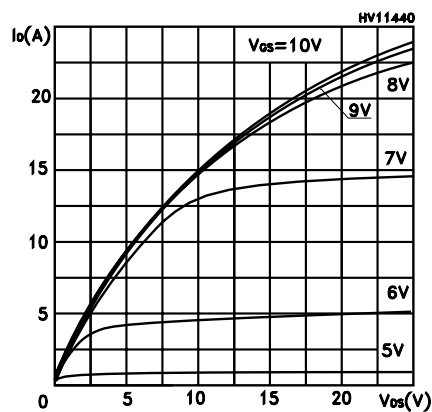


Figure 6. Typical transfer characteristics

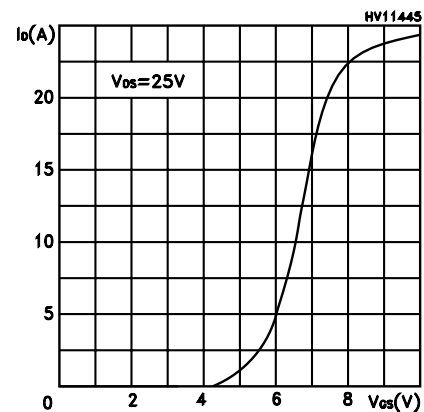


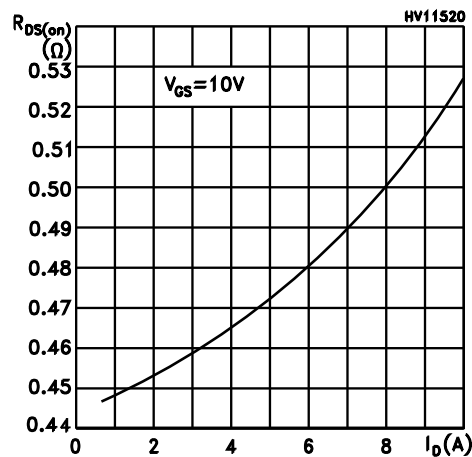
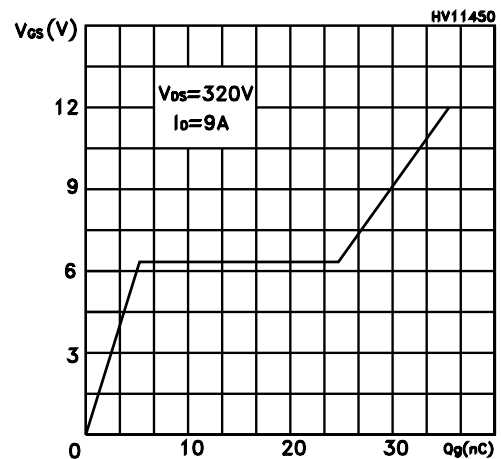
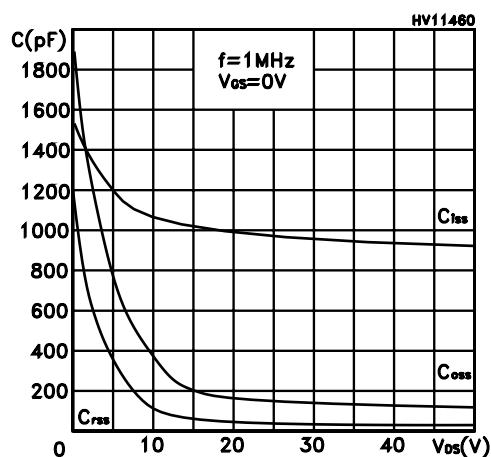
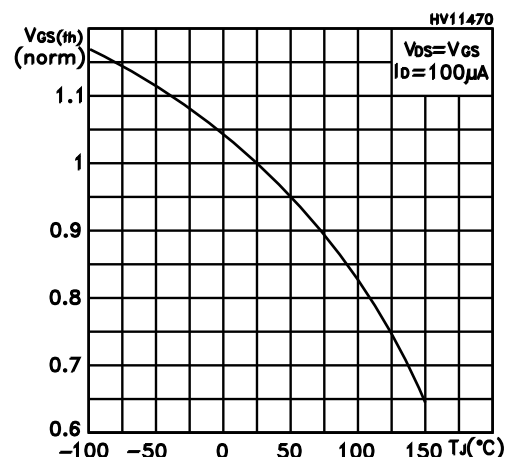
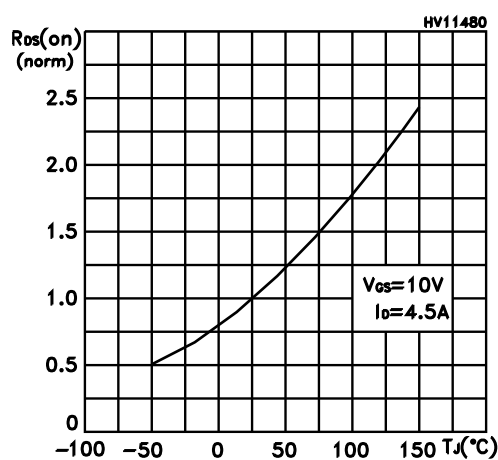
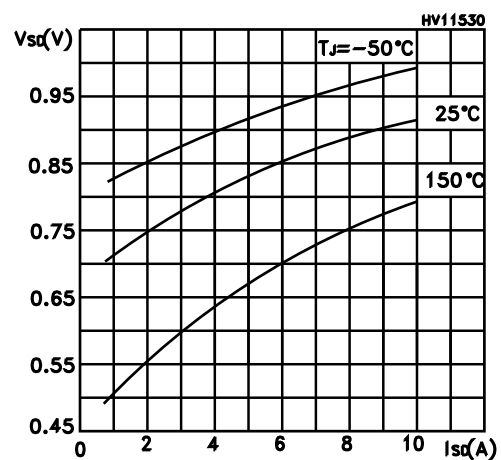
Figure 7. Typical static drain-source on-resistance

Figure 8. Typical gate charge characteristics

Figure 9. Typical capacitance variations

Figure 10. Normalized gate threshold vs temperature

Figure 11. Normalized on-resistance vs temperature

Figure 12. Typical reverse diode forward characteristics


Figure 13. Normalized breakdown voltage vs temperature

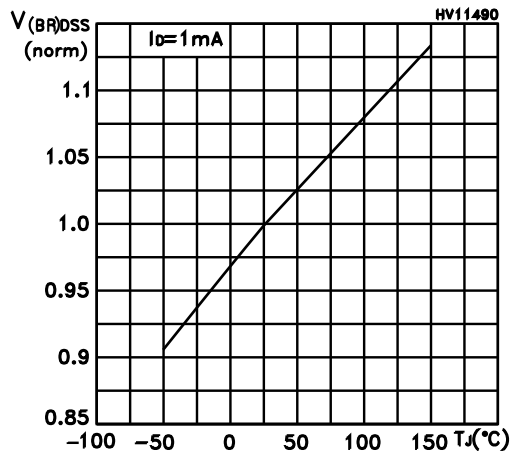
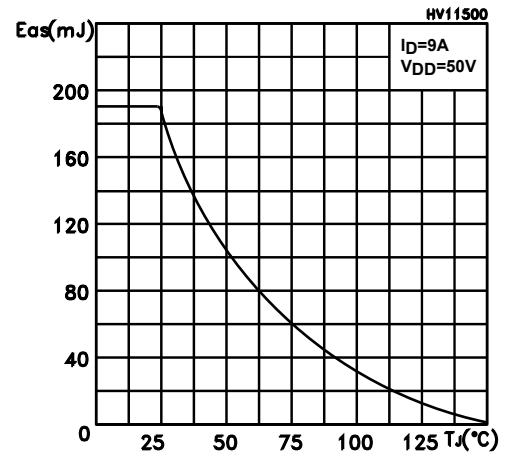


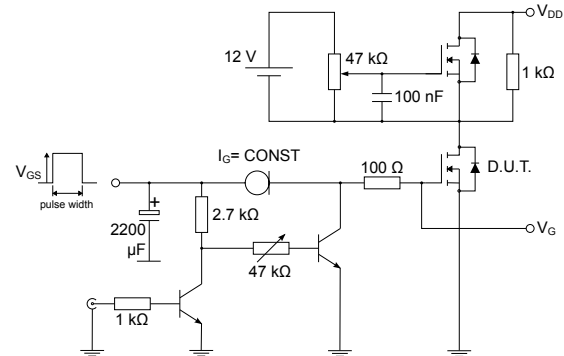
Figure 14. Maximum avalanche energy vs temperature



3 Test circuits

Figure 15. Test circuit for resistive load switching times


AM01468v1

Figure 16. Test circuit for gate charge behavior


AM01469v1

Figure 17. Test circuit for inductive load switching and diode recovery times

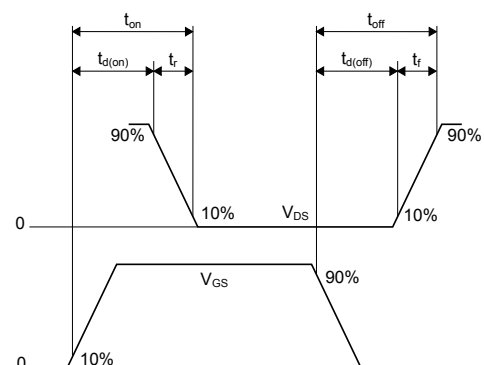

AM01470v1

Figure 18. Unclamped inductive load test circuit


AM01471v1

Figure 19. Unclamped inductive waveform


AM01472v1

Figure 20. Switching time waveform


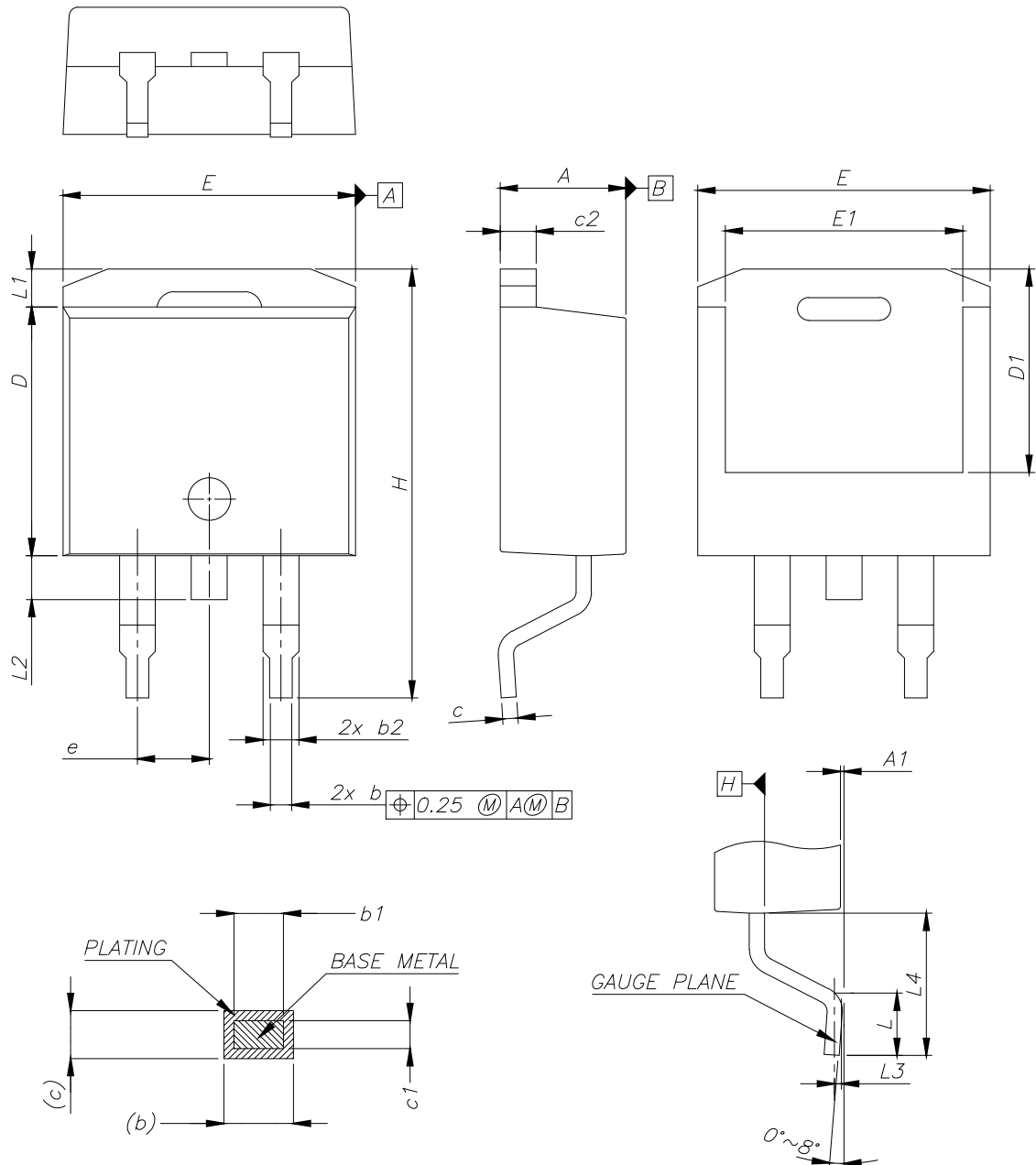
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type B package information

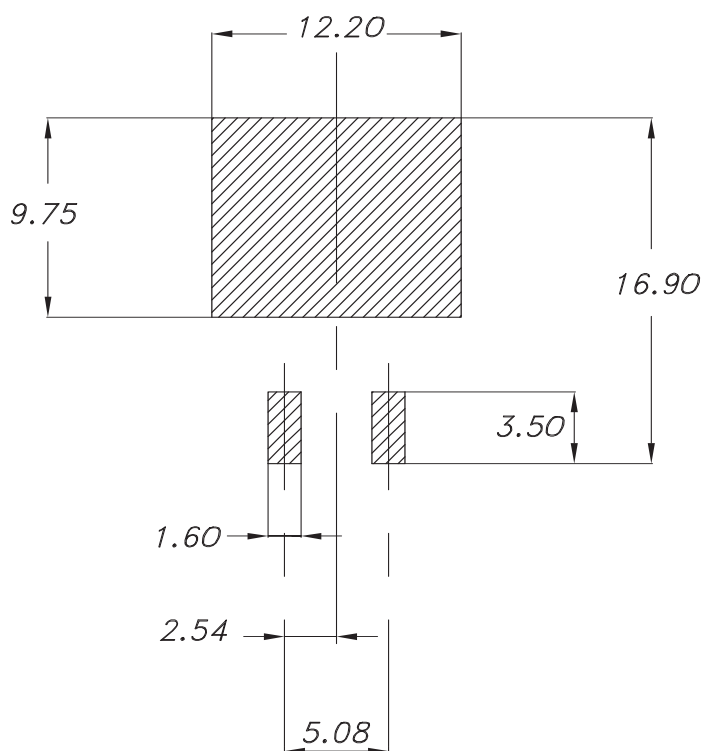
Figure 21. D²PAK (TO-263) type B package outline



0079457_27_B

Table 8. D²PAK (TO-263) type B mechanical data

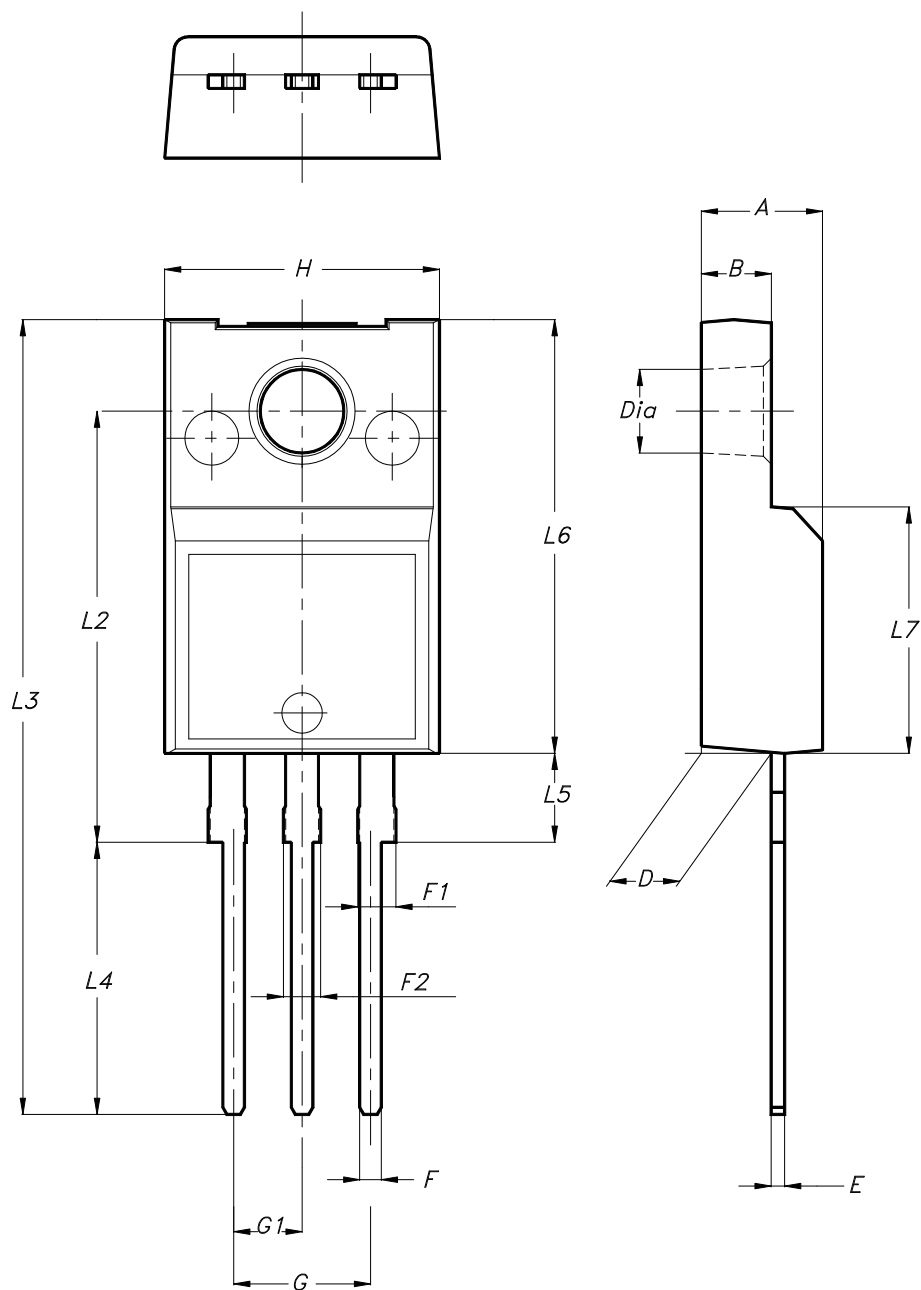
Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0.00		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 22. D²PAK (TO-263) recommended footprint (dimensions are in mm)


0079457_Rev27_footprint

4.2 TO-220FP type B package information

Figure 23. TO-220FP type B package outline



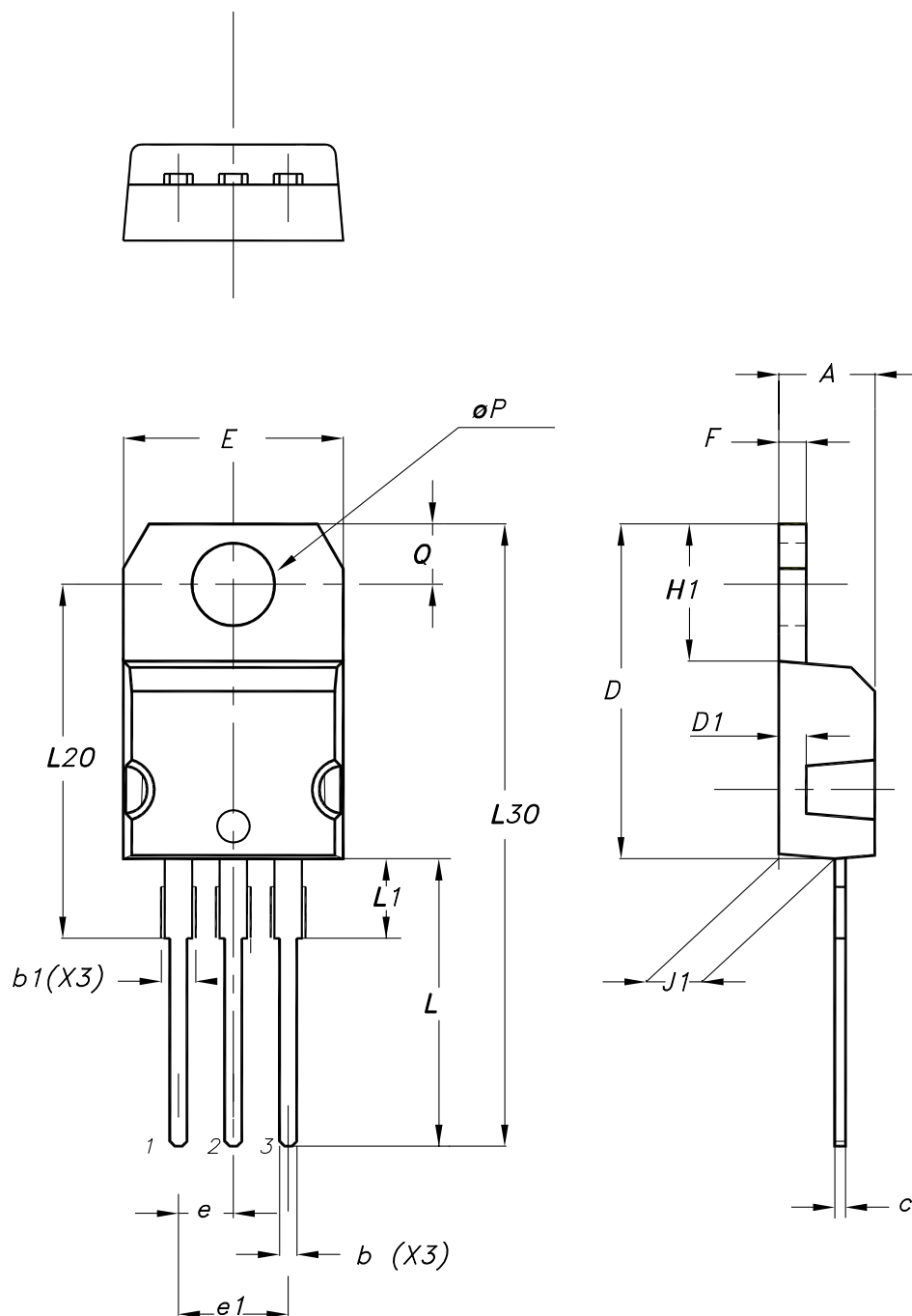
7012510_B_rev.14

Table 9. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.3 TO-220 type A package information

Figure 24. TO-220 type A package outline



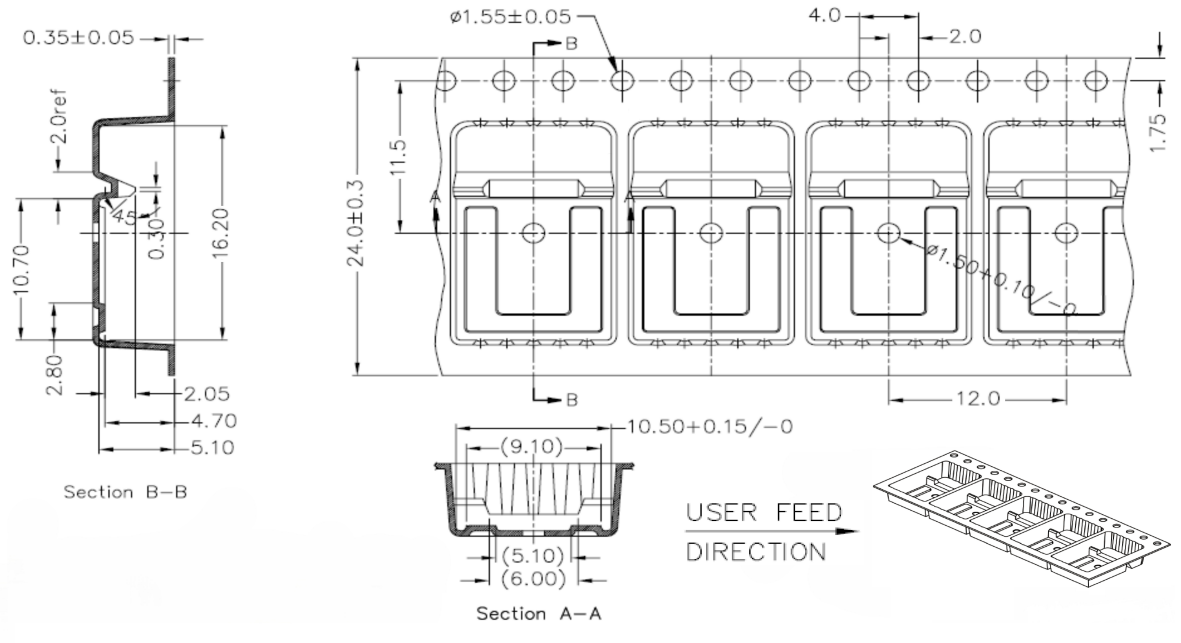
0015988_typeA_Rev_24

Table 10. TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.4 D²PAK packing information

Figure 25. D²PAK tape drawing (dimensions are in mm)



DM01095771_2



5 Ordering information

Table 11. Order codes

Order codes	Marking	Package	Packing
STB11NK40ZT4	B11NK40Z	D ² PAK	TO-220FP
STP11NK40Z	P11NK40Z	TO-220	Tube
STP11NK40ZFP	P11NK40ZFP	TO-220FP	

Revision history

Table 12. Document revision history

Date	Version	Changes
23-Aug-2005	2	Preliminary version
28-Oct-2005	3	Complete version
26-Jul-2006	4	New template, no content change
22-Nov-2006	5	Corrected unit on <i>Table 5.: On/off states</i>
18-Jan-2007	6	Typo mistakes on page 1
20-Apr-2009	7	Updated mechanical data
02-Oct-2018	8	Updated <i>Section 4 Package information</i> . Minor text changes.
16-Jul-2025	9	Updated Section 4: Package information .



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