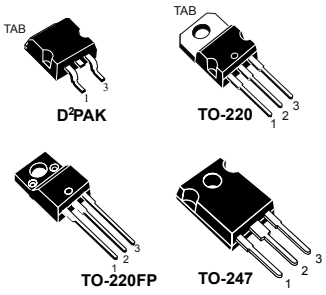
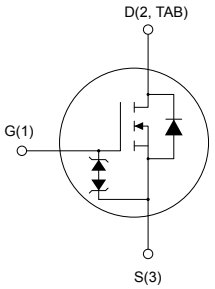
STB10NK60ZT4, STP10NK60Z
STP10NK60ZFP, STW10NK60Z

Datasheet

N-channel 600 V, 0.68 Ω typ., 10 A SuperMESH Power MOSFETs in D²PAK, TO-220, TO-220FP and TO-247 packages





AM01476v1_tab

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB10NK60ZT4	600 V	0.75 Ω	10 A
STP10NK60Z			
STP10NK60ZFP			
STW10NK60Z			

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status links
STB10NK60ZT4
STP10NK60Z
STP10NK60ZFP
STW10NK60Z

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		D^2PAK TO-220	TO-220FP	TO-247	
V_{DS}	Drain-source voltage	600			V
V_{GS}	Gate-source voltage	±30			V
I_D	Drain current (continuous) at T_C = 25 °C	10	10(1)	10	A
	Drain current (continuous) at T_C = 100 °C	5.7	5.7(1)	5.7	
I_{DM}(2)	Drain current (pulsed)	36	36(1)	36	A
P_{TOT}	Total power dissipation at T_C = 25 °C	115	35	156	W
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	4			kV
dv/dt(3)	Peak diode recovery voltage slope	4.5			V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	-	2.5	-	kV
T_{stg}	Storage temperature range	-55 to 150			°C
T_J	Operating junction temperature range				

1. *Limited by maximum junction temperature.*
2. *Pulse width is limited by safe operating area.*
3. *I_{SD} ≤ 10 A, di/dt ≤ 200 A/µs, V_{DD} = 480 V.*

Table 2. Thermal data

Symbol	Parameter	Value				Unit
		D^2PAK	TO-220	TO-220FP	TO-247	
R_{thJC}	Thermal resistance, junction-to-case	1.09		3.6	0.8	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	35(1)	62.5		50	°C/W

1. *When mounted on a standard 1 inch^2 area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.)	10	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	300	mJ
E_{AR}	Repetitive avalanche energy (pulse width limited by T_J max.)	3.5	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0 V	600	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)	-	-	50	
I_{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.00	3.75	4.50	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4.5 A	-	0.68	0.75	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}(1)	Forward transconductance	V_{DS} = 25 V, I_D = 4.5 A	-	7.8	-	S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	1370	-	pF
C_{oss}	Output capacitance		-	156	-	pF
C_{rss}	Reverse transfer capacitance		-	37	-	pF
$C_{oss\ eq.}$(2)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 480 V	-	93	-	pF
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 8 A, V_{GS} = 0 to 10 V (see the Figure 18. Test circuit for gate charge behavior)	-	48	70(3)	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain charge		-	25	-	nC

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*
2. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
3. *Specified by design, not tested in production.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 17. Test circuit for resistive load switching times and Figure 22. Switching time waveform)	-	20	-	ns
t_r	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
t_f	Fall time		-	30	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	10	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	36	A
V_{SD}(2)	Forward on voltage	I_{SD} = 10 A, V_{GS} = 0 V	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs,	-	570	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 40 V, T_J = 150 °C	-	4.3	-	µC
I_{RRM}	Reverse recovery current	(see the Figure 19. Test circuit for inductive load switching and diode recovery times)	-	15	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for D²PAK and TO-220

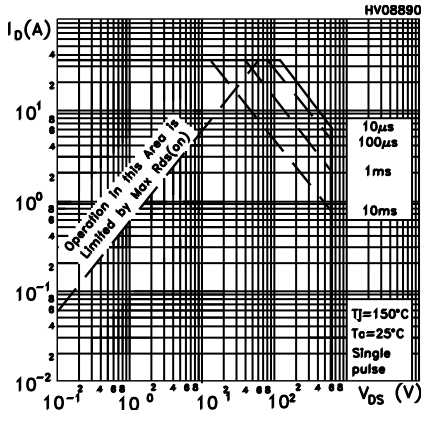


Figure 2. Normalized transient thermal impedance for D²PAK and TO-220

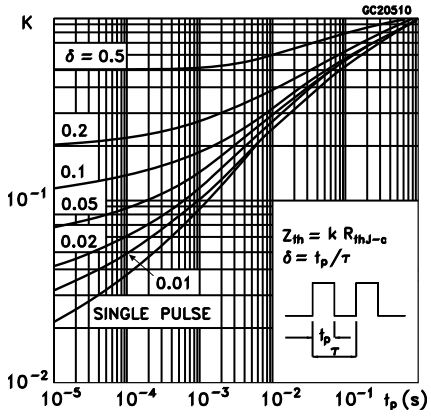


Figure 3. Safe operating area for TO-220FP

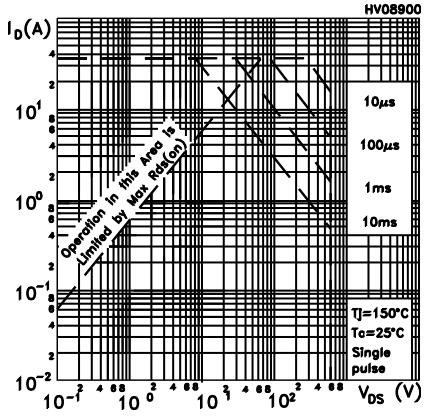


Figure 4. Normalized transient thermal impedance for TO-220FP

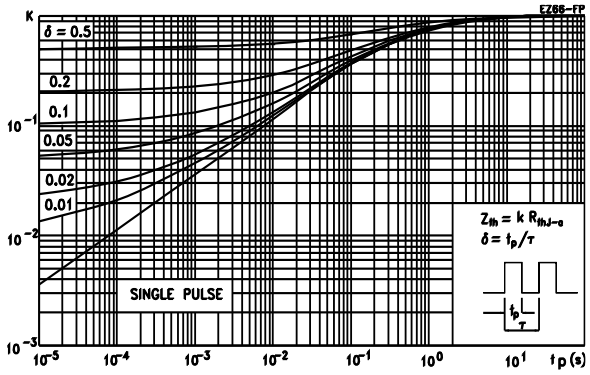


Figure 5. Safe operating area for TO-247

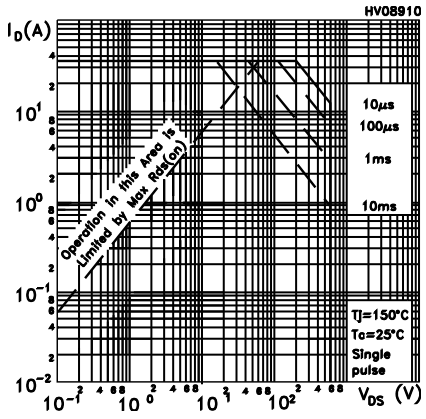


Figure 6. Normalized transient thermal impedance for TO-247

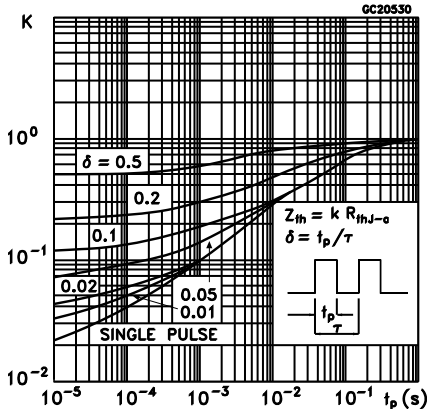


Figure 7. Typical output characteristics

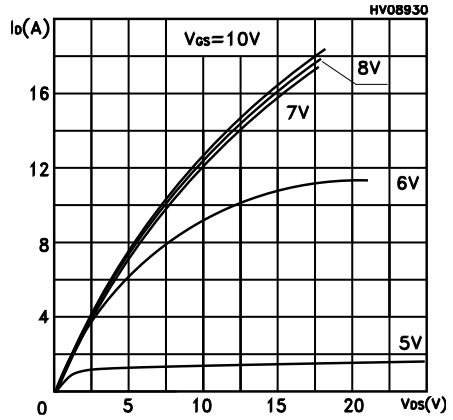


Figure 8. Typical transconductance characteristics

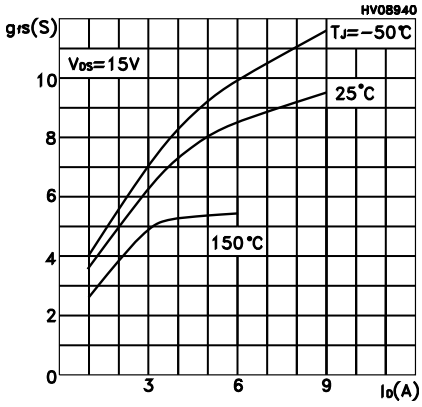


Figure 9. Typical drain-source on-resistance

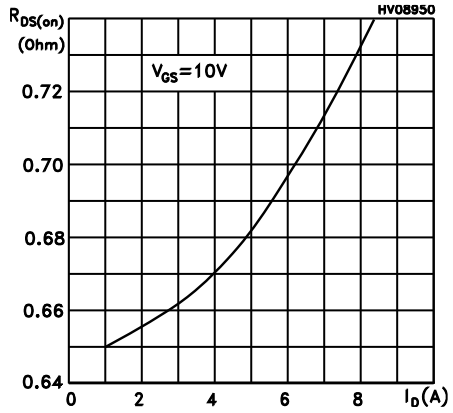


Figure 10. Typical gate charge characteristics

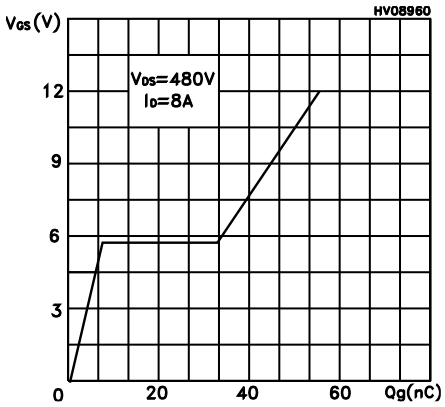


Figure 11. Typical capacitance characteristics

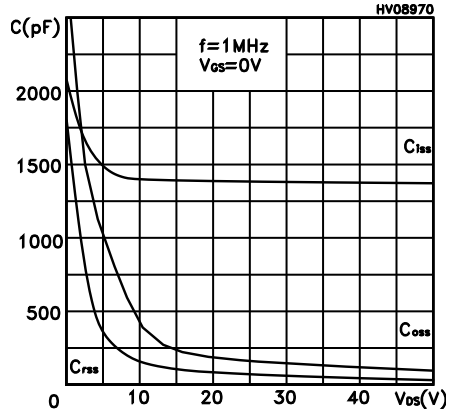


Figure 12. Normalized gate threshold vs temperature

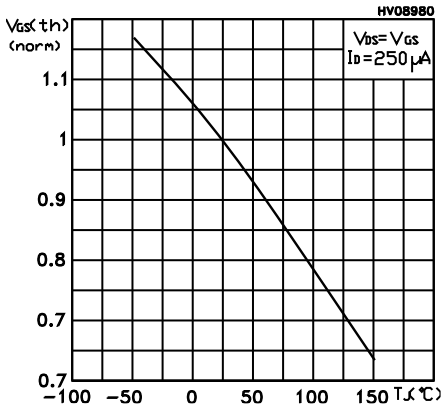


Figure 13. Normalized on-resistance vs temperature

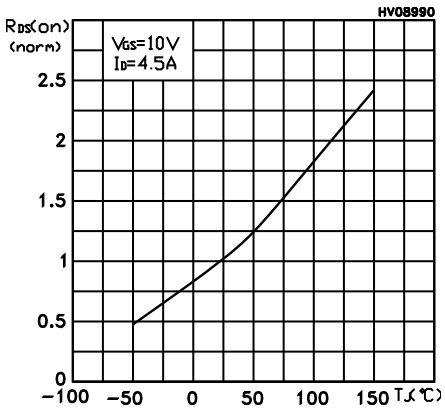


Figure 14. Typical reverse diode forward characteristics

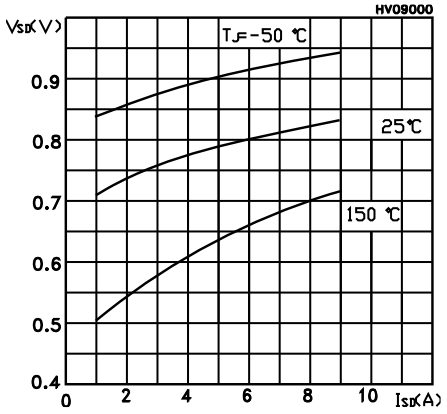


Figure 15. Maximum avalanche energy vs temperature

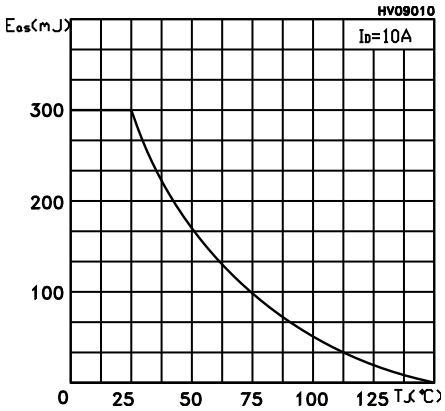
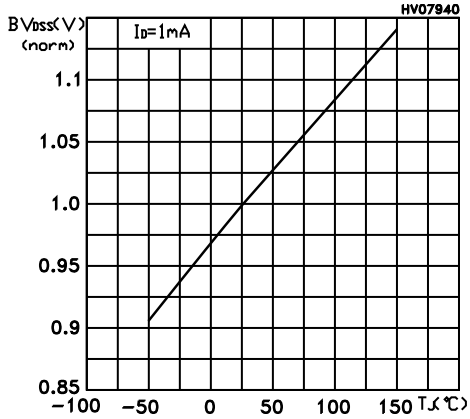


Figure 16. Normalized breakdown voltage vs temperature



3 Test circuits

Figure 17. Test circuit for resistive load switching times

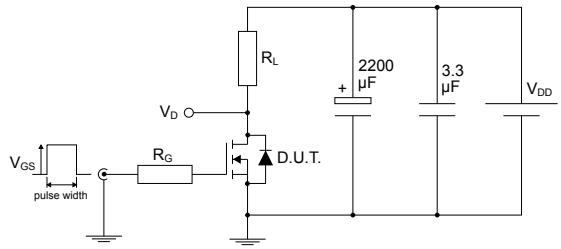


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Figure 18. Test circuit for gate charge behavior

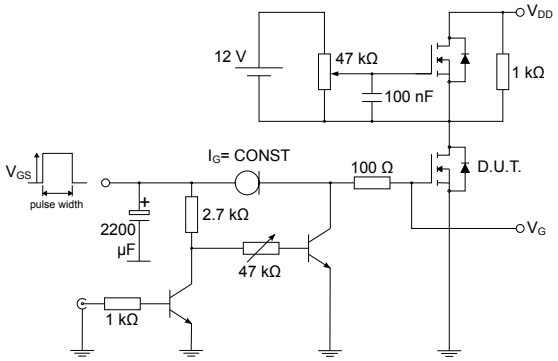

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Figure 19. Test circuit for inductive load switching and diode recovery times

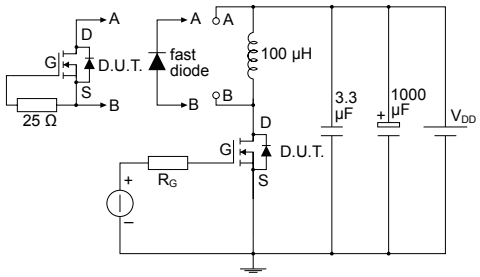

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Figure 20. Unclamped inductive load test circuit

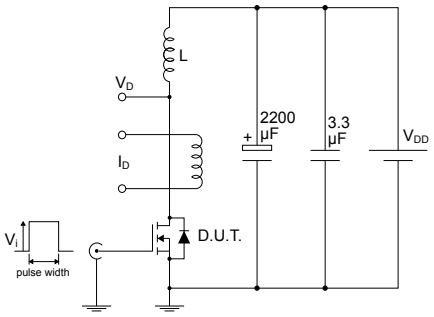

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Figure 21. Unclamped inductive waveform

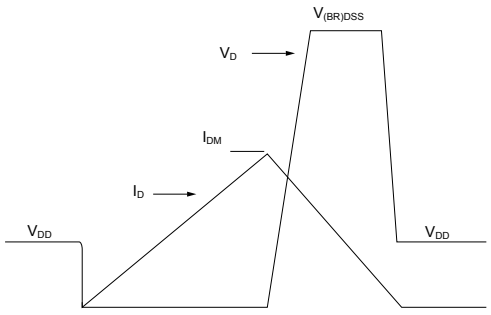

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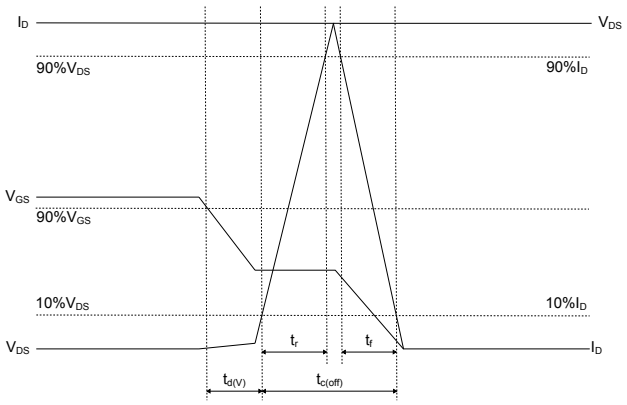
Figure 22. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 23. **D²PAK (TO-263) type A package outline**

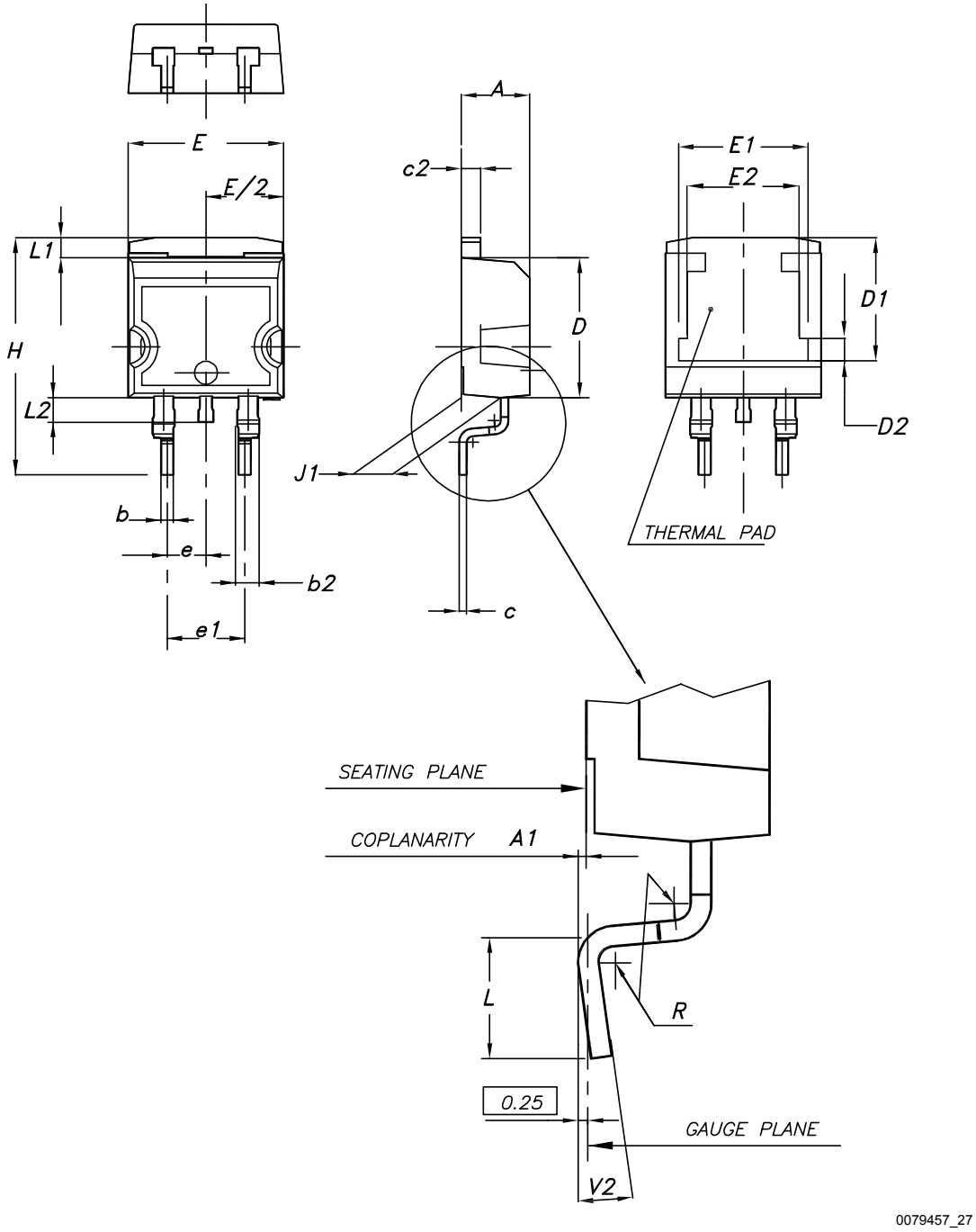

Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

4.2 D²PAK (TO-263) type B package information

Figure 24. **D²PAK (TO-263) type B package outline**

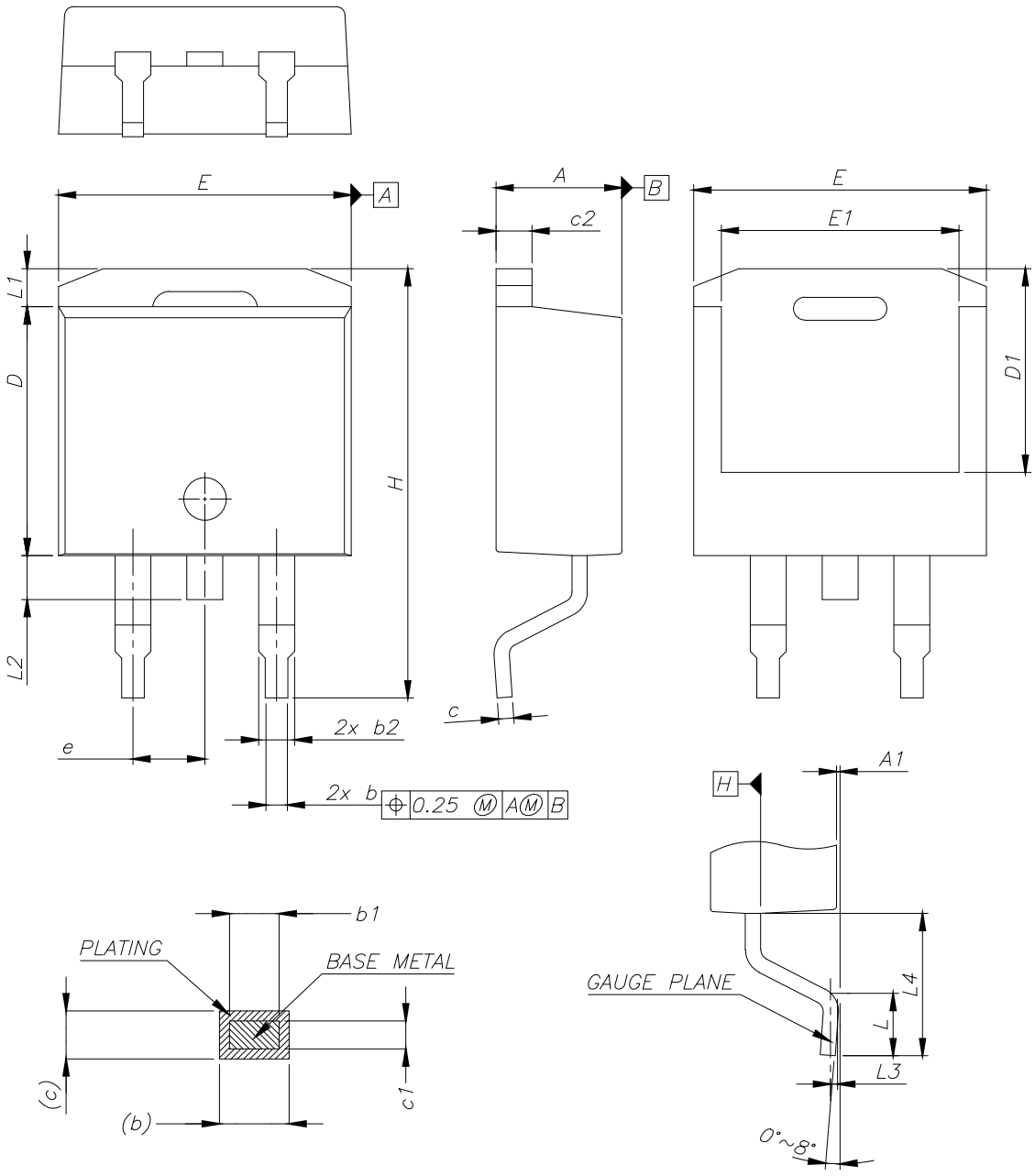

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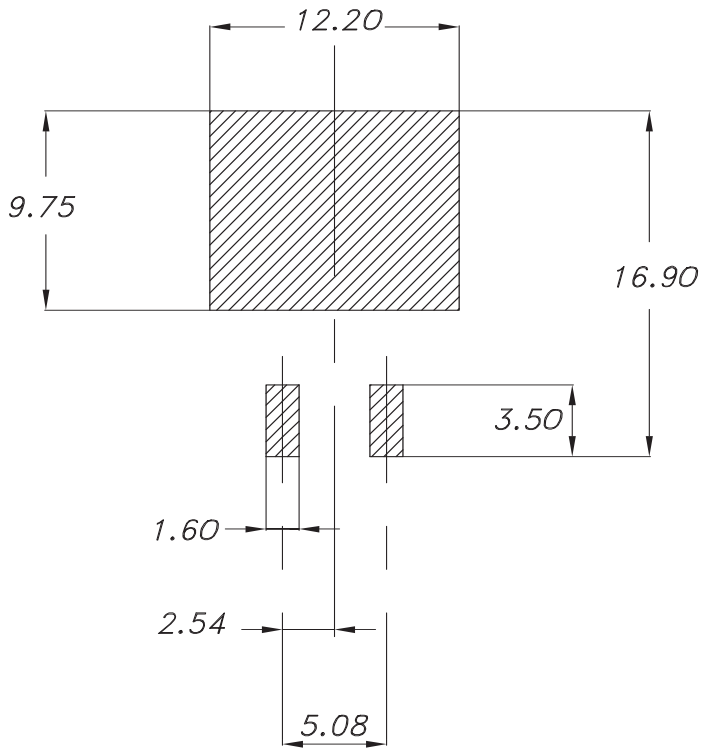
Table 9. **D²PAK (TO-263) type B mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0.00		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 25. **D²PAK (TO-263) recommended footprint (dimensions are in mm)**



4.3 TO-220 type A package information

Figure 26. **TO-220 type A package outline**

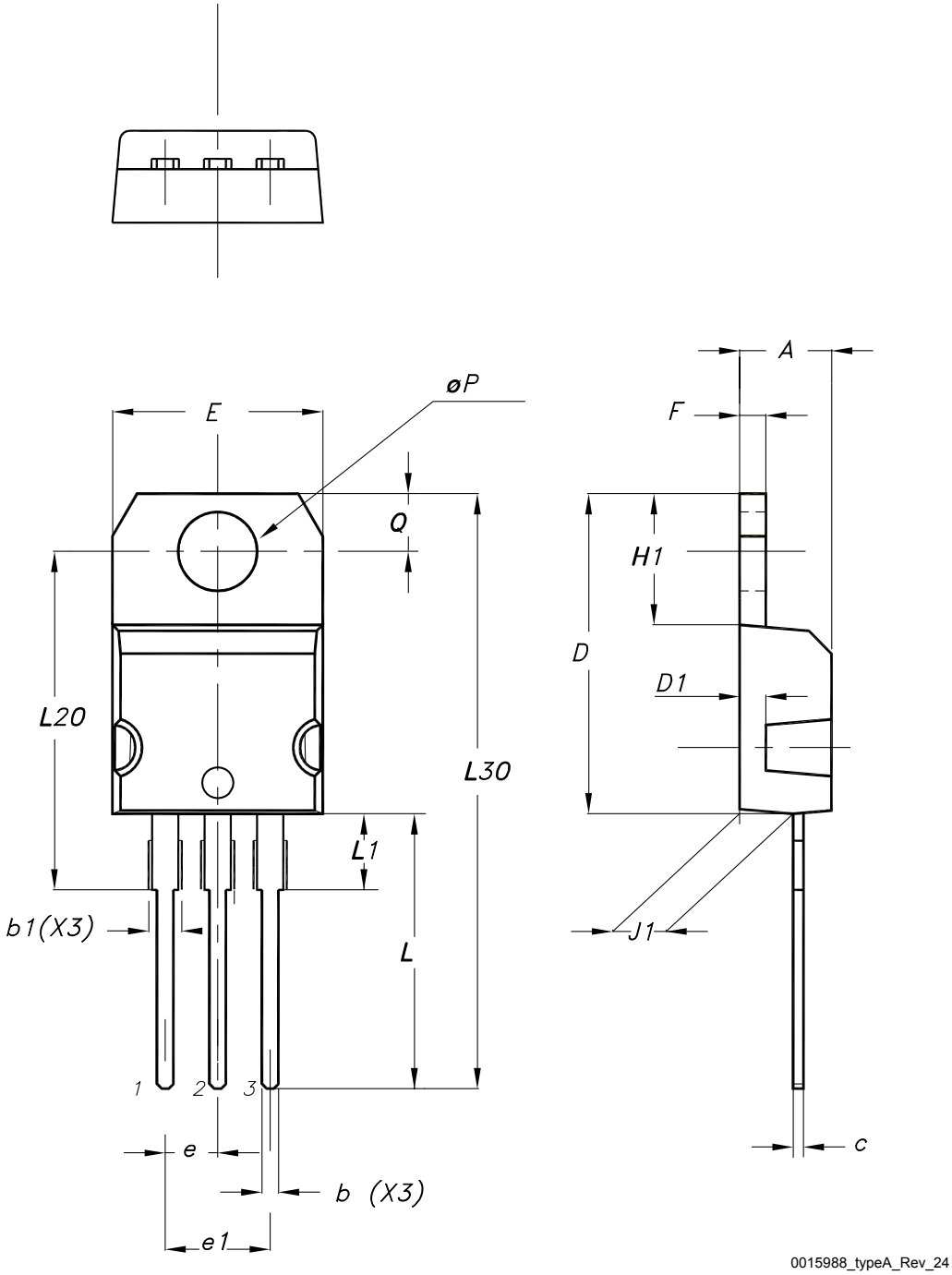


Table 10. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.4 TO-220FP type B package information

Figure 27. **TO-220FP type B package outline**

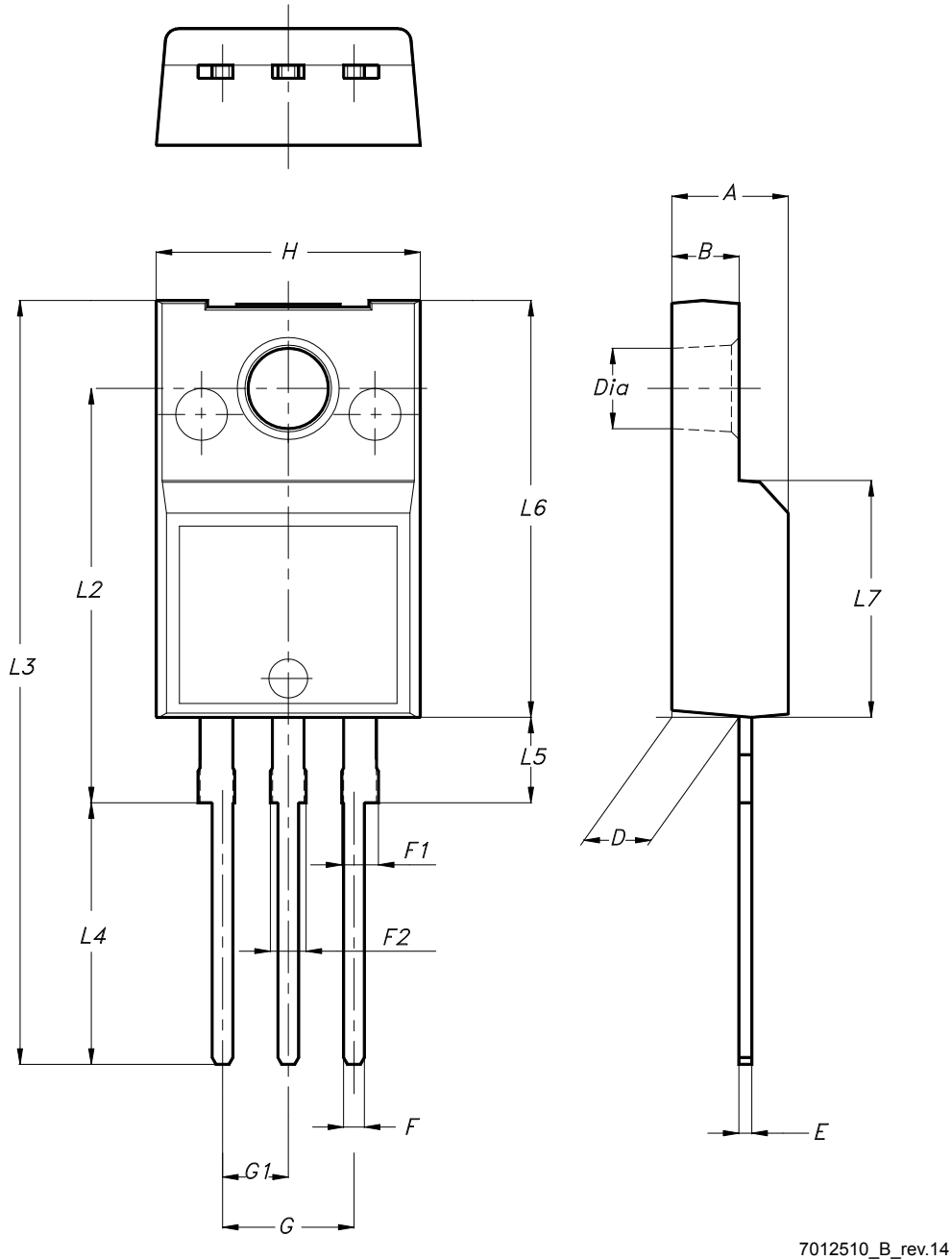


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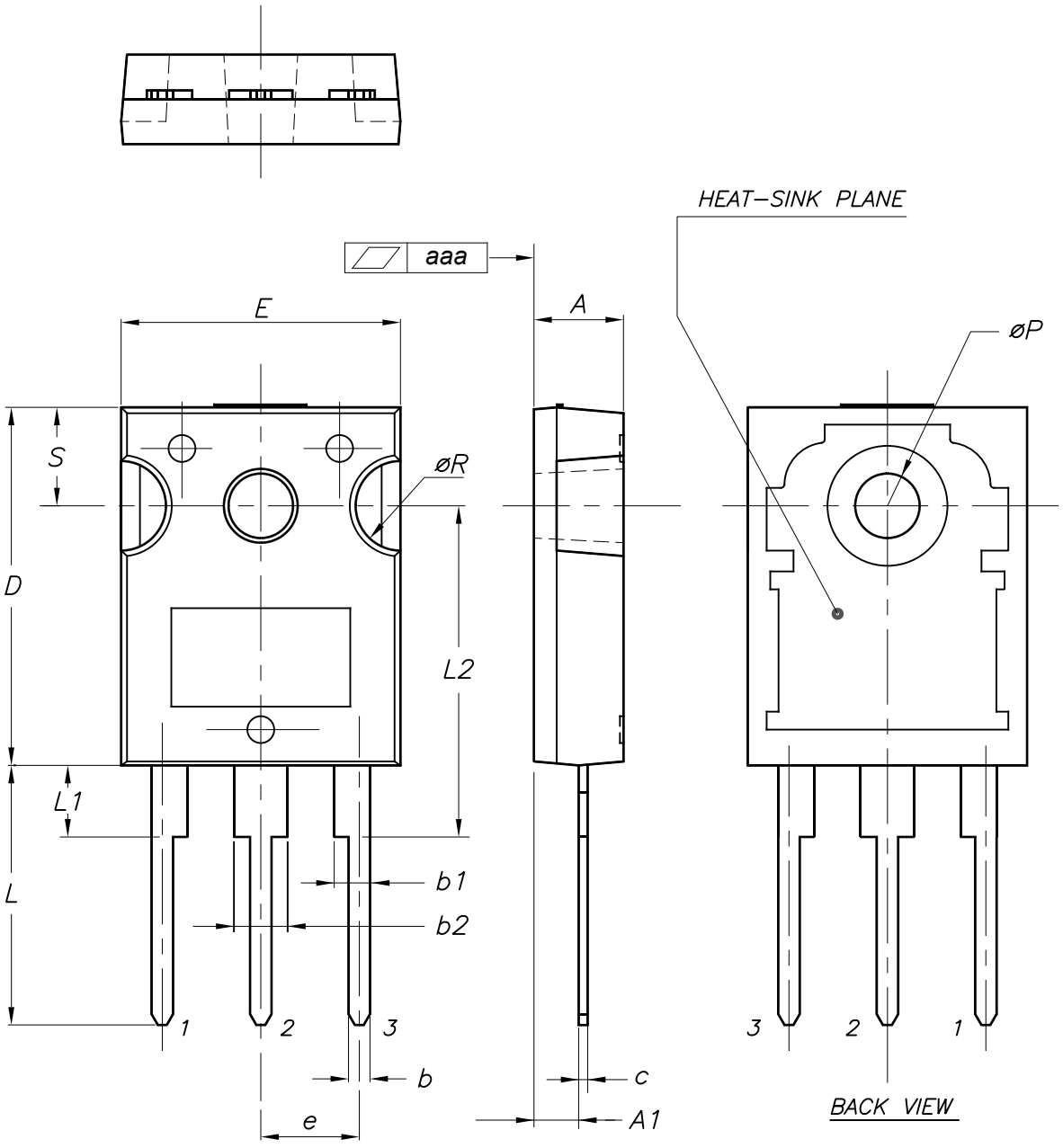
Table 11. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.5 TO-247 package information

Figure 28. **TO-247 package outline**



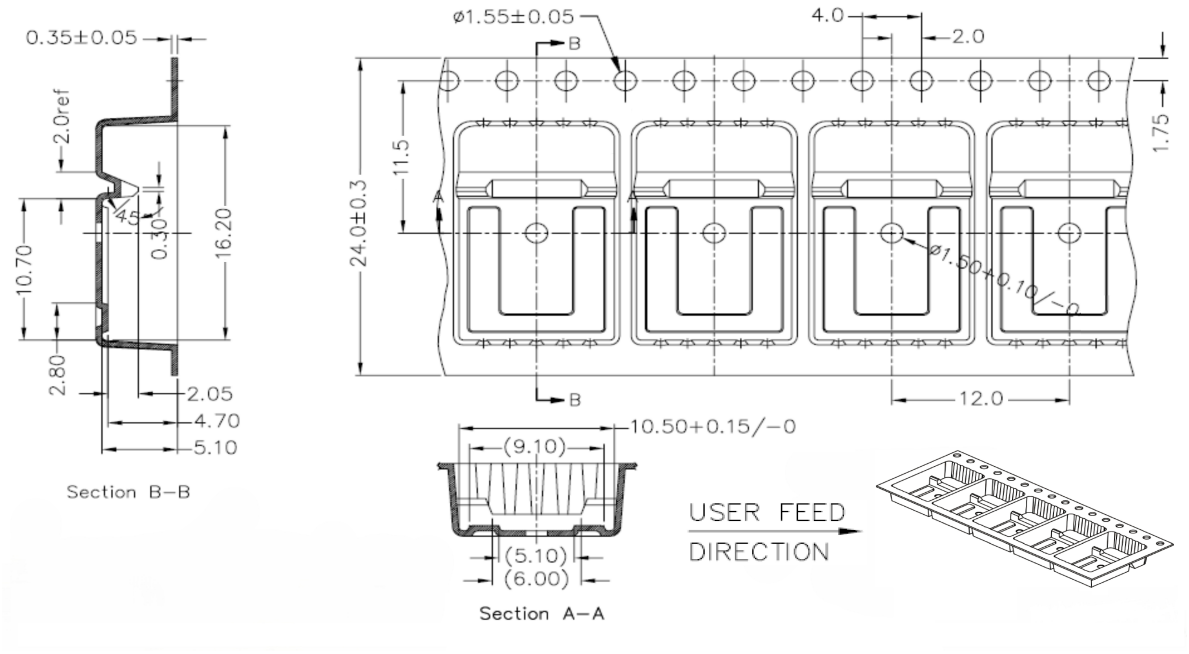
0075325_10

Table 12. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

4.6 D²PAK packing information

Figure 29. **D²PAK tape drawing (dimensions are in mm)**



DM01095771_2

5 Ordering information

Table 13. **Order codes**

Order codes	Marking	Package	Packing
STB10NK60ZT4	B10NK60Z	D²PAK	Tape and reel
STP10NK60Z	P10NK60Z	TO-220	Tube
STP10NK60ZFP	P10NK60ZFP	TO-220FP	
STW10NK60Z	W10NK60Z	TO-247	

Revision history

Table 14. **Document revision history**

Date	Revision	Changes
29-Sep-2005	6	Inserted ecopack indication.
29-Oct-2005	7	New value inserted in *Table 6*.
11-Apr-2006	8	New template.
19-Sep-2006	9	Unit changed in *Table 5*.
17-Nov-2008	10	Updated *Section 4: Package mechanical data*.
15-Nov-2012	11	Updated *Table 2: Absolute maximum ratings*, *Table 3: Thermal data*, *Table 5: On /off states* and *Table 9: Gate-source Zener diode*. Updated *Section 4: Package mechanical data* and *Section 5: Packaging mechanical data*. Minor text changes.
14-Jul-2025	12	Removed order code STB10NK60Z-1. Updated Section 4: Package information.

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