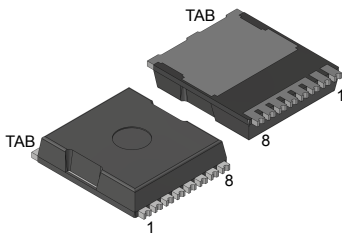
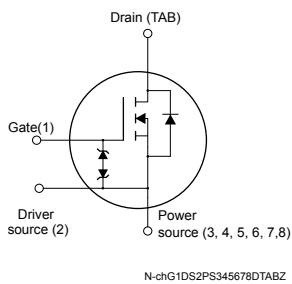


N-channel 600 V, 45 mΩ typ., 57 A MDmesh M6 Power MOSFET in a TO-LL package


TO-LL

Product status link
[STO67N60M6](#)
Product summary

Order code	STO67N60M6
Marking	67N60M6
Package	TO-LL
Packing	Tape and reel

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STO67N60M6	600 V	54 mΩ	57 A

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected
- Excellent switching performance thanks to the extra driving source pin

Applications

- Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	57	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	36	
$I_{DM}^{(2)}$	Drain current (pulsed)	227	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	357	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	100	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Referred to TO-247 long leads.
2. Pulse width is limited by safe operating area.
3. $I_{SD} \leq 57\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS} (\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$
4. $V_{DD} \leq 480\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.35	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient ⁽¹⁾	43	$^\circ\text{C}/\text{W}$
	Thermal resistance, junction-to-ambient ⁽²⁾	22	

1. When mounted on 1 inch² FR-4 pcb, standard footprint 2 Oz copper board.
2. When mounted on 40x40mm FR-4 pcb, 6 cm² 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	760	mJ

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On /off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.25	4.00	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 28.5\text{ A}$		45	54	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$	-	3035	-	pF
C_{oss}	Output capacitance		-	110	-	pF
$C_{oss\ eq.}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }400\text{ V}$	-	750	-	pF
R_g	Intrinsic gate resistance	$f = 250\text{ kHz}$, open drain	-	3.6	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 57\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	75.1	-	nC
Q_{gs}	Gate-source charge		-	20.3	-	nC
Q_{gd}	Gate-drain charge		-	34.6	-	nC

1. $C_{oss\ eq.}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 28.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	22	-	ns
t_r	Rise time		-	9.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	82.1	-	ns
t_f	Fall time		-	10.2	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		57	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		227	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 57\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 57\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	340		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	5.6		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	29.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 57\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$,	-	510		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	12		μC
I_{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	39.5		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

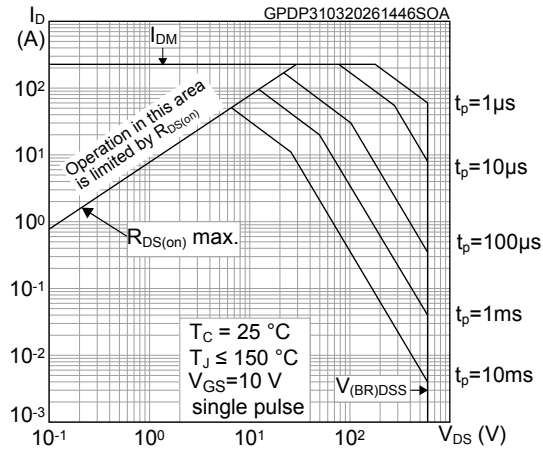


Figure 2. Maximum transient thermal impedance

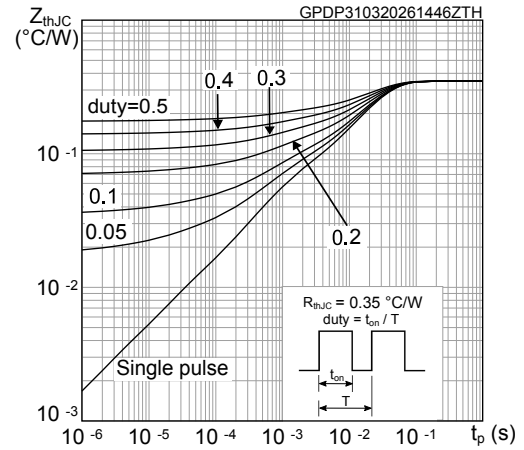


Figure 3. Typical output characteristics

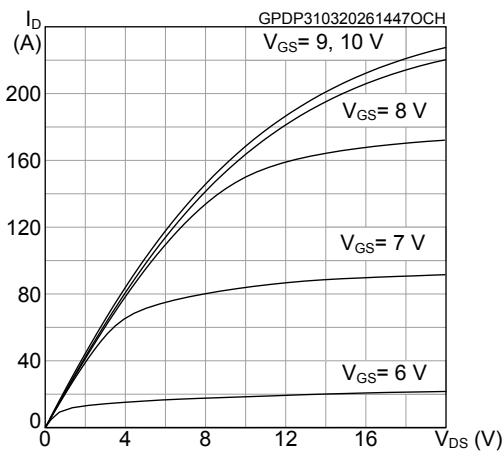


Figure 4. Typical transfer characteristics

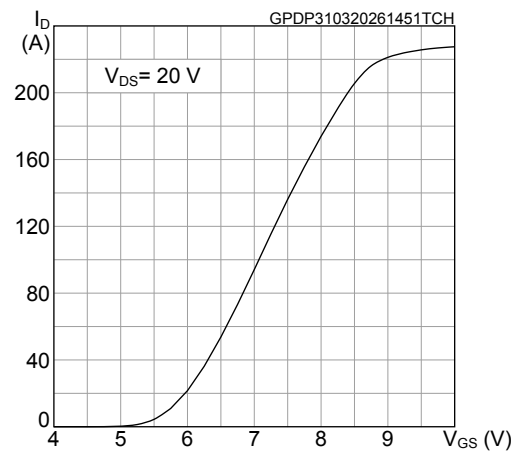


Figure 5. Typical gate charge characteristics

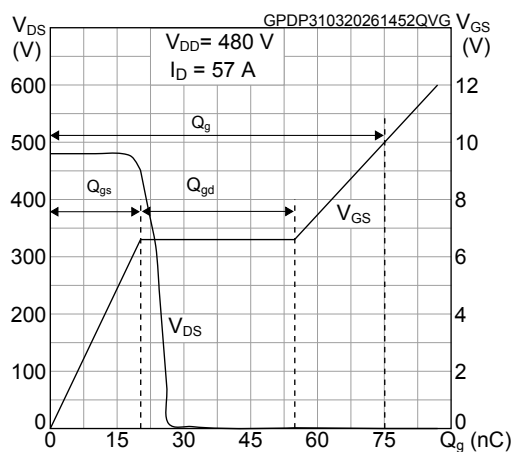


Figure 6. Typical capacitance characteristics

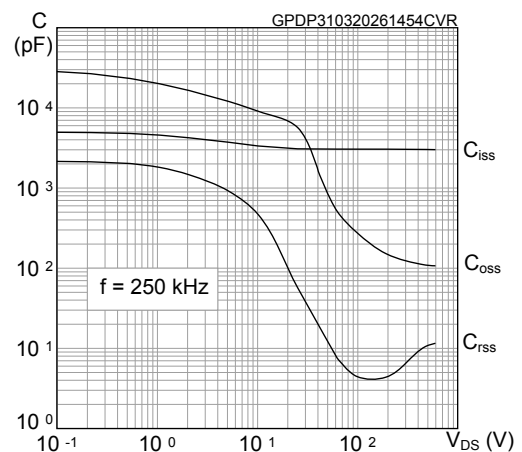


Figure 7. Typical drain-source on-resistance

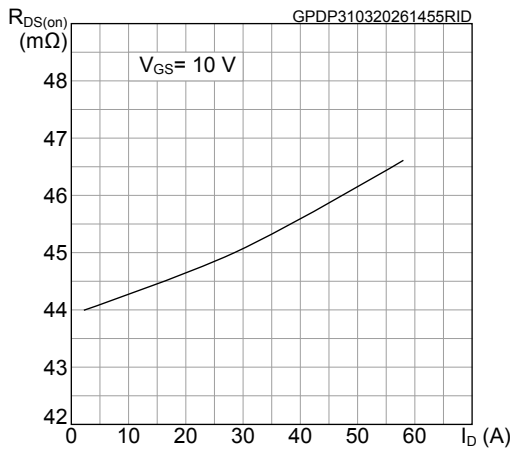


Figure 8. Normalized on-resistance vs temperature

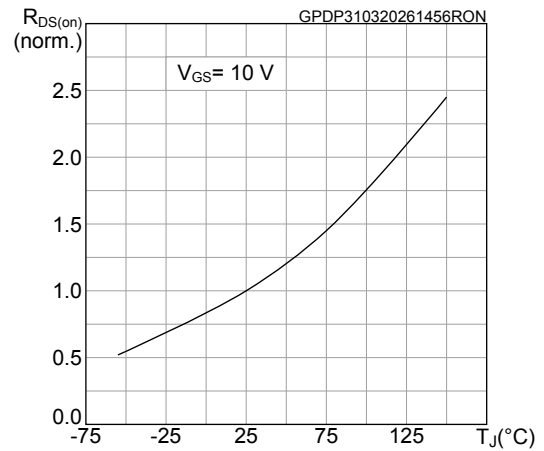


Figure 9. Normalized gate threshold vs temperature

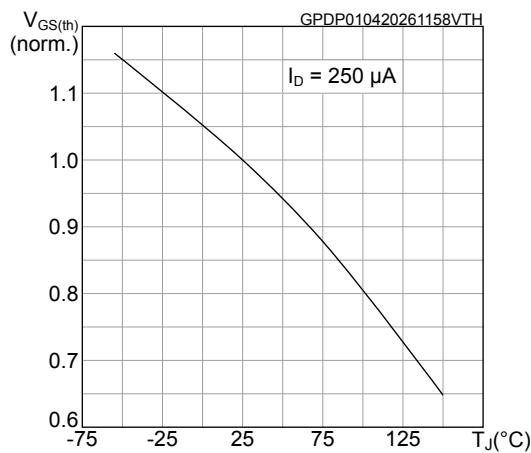


Figure 10. Normalized breakdown voltage vs temperature

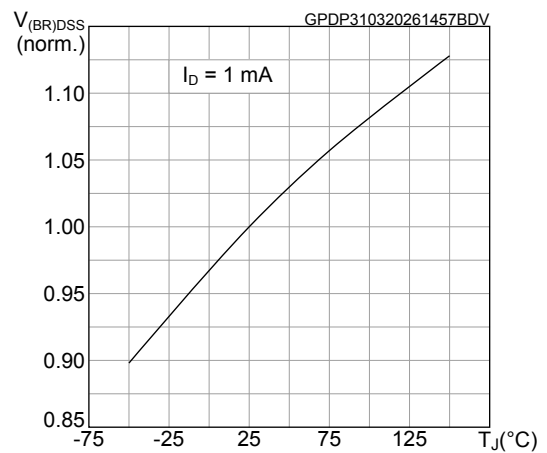


Figure 11. Typical reverse diode forward characteristics

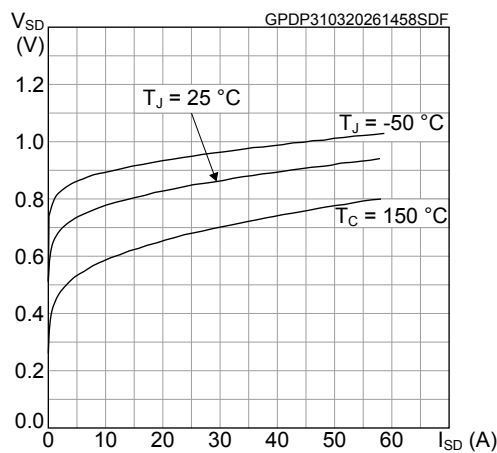
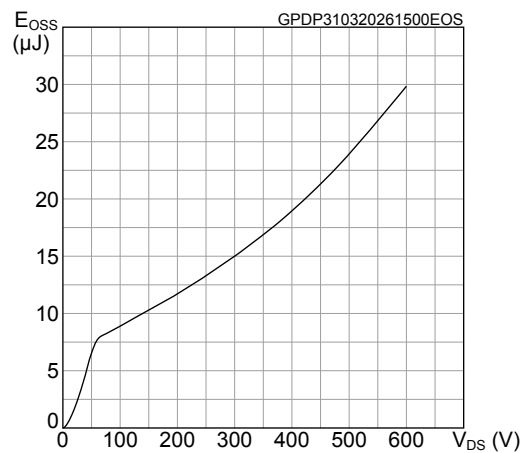
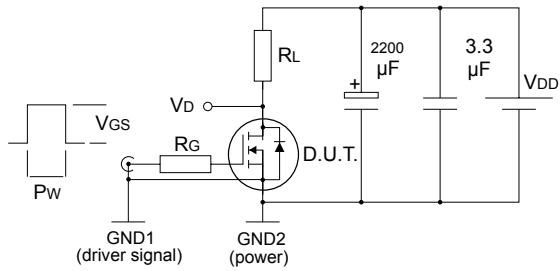


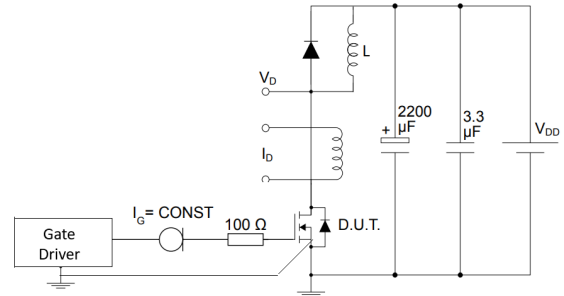
Figure 12. Typical output capacitance stored energy



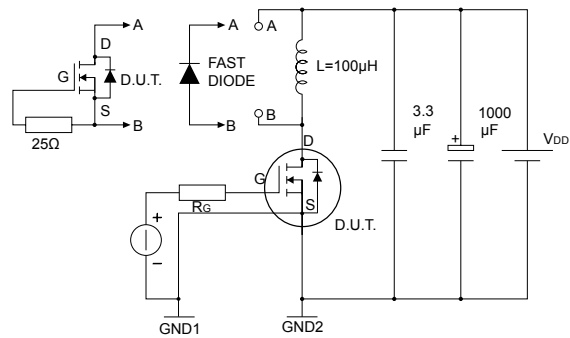
3 Test circuits

Figure 13. Test circuit for resistive load switching times


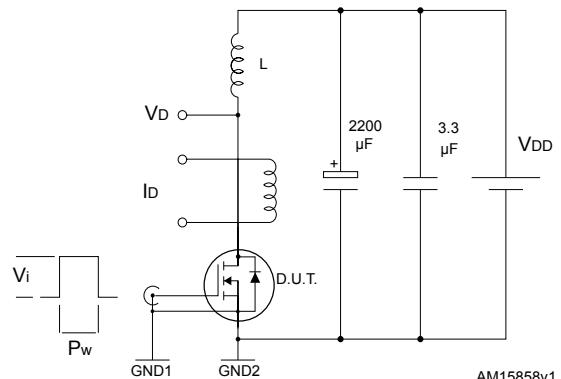
AM15855v1

Figure 14. Test circuit for gate charge behavior


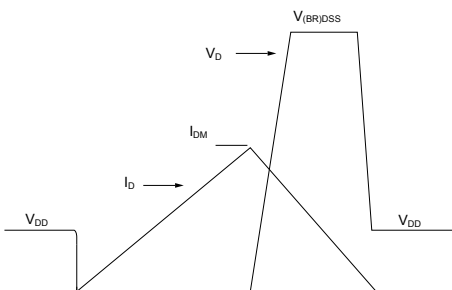
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Figure 15. Test circuit for inductive load switching and diode recovery times


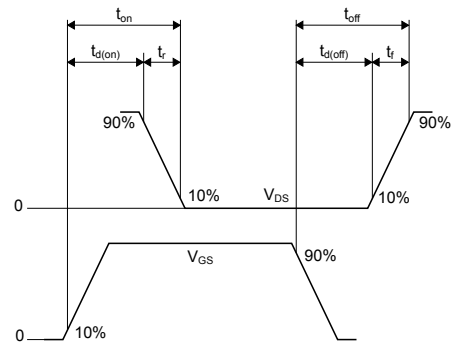
AM15857v1

Figure 16. Unclamped inductive load test circuit


AM15858v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform


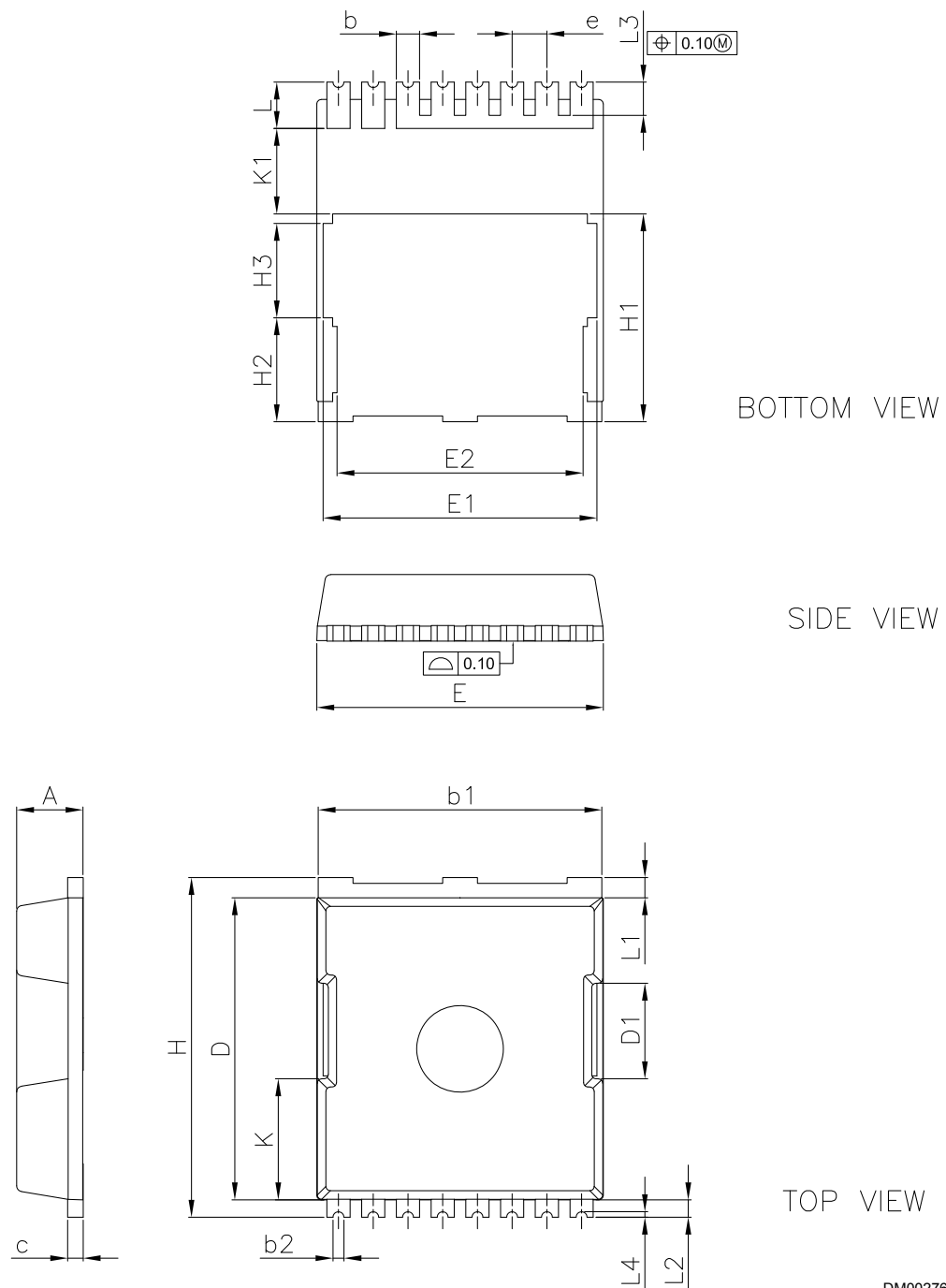
AM01473v1

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL package information

Figure 19. TO-LL package outline

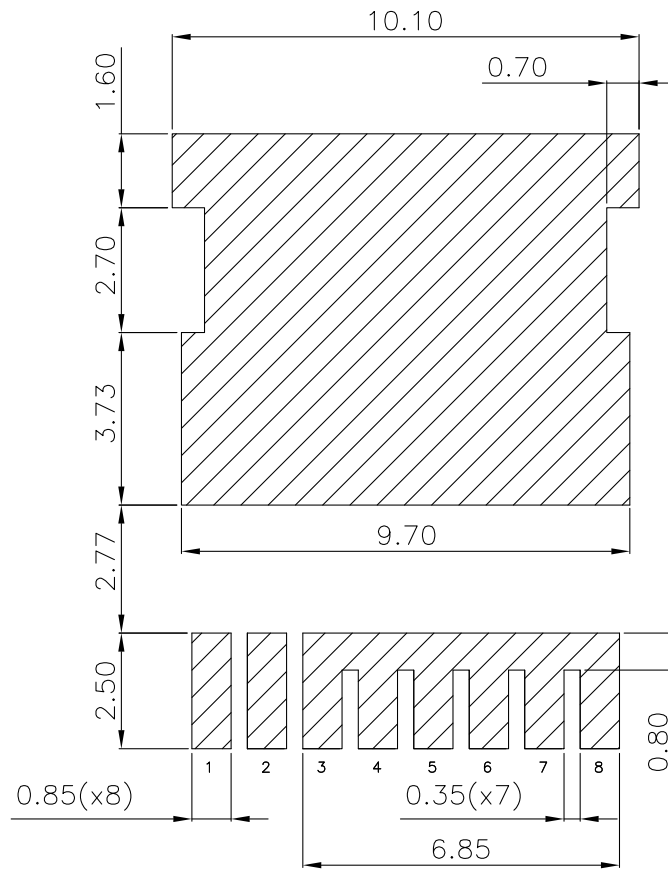


DM00276569_Rev_10

Table 8. TO-LL package mechanical data

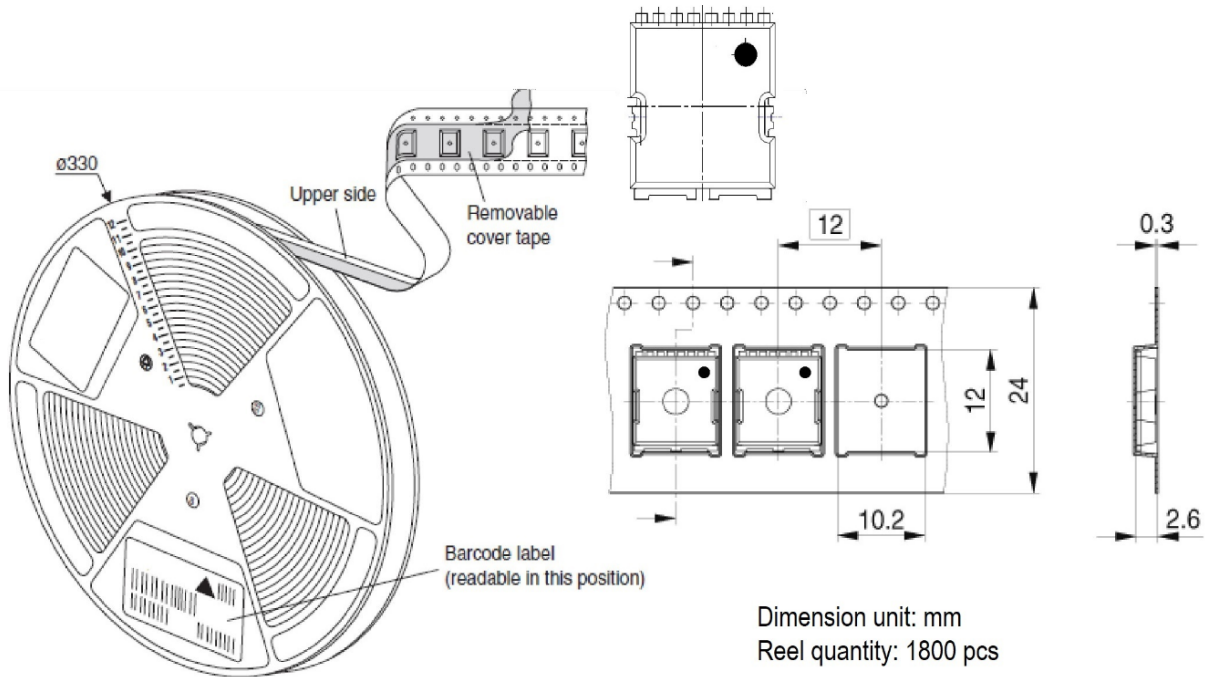
Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
b	0.60	0.80	0.90
b1	9.70	9.80	9.90
b2	0.20		0.50
c	0.40	0.50	0.60
D	10.28	10.43	10.58
D1	3.15	3.30	3.45
E	9.70	9.90	10.10
E1	9.31	9.46	9.61
E2	8.35	8.50	8.65
e	1.10	1.20	1.30
H	11.48	11.73	11.88
H1	7.00	7.15	7.30
H2	3.34	3.59	3.84
H3	3.11	3.26	3.41
K	4.03	4.18	4.33
K1	2.85	2.95	3.05
L	1.45	1.60	1.75
L1	0.55	0.70	0.85
L2	0.45	0.60	0.75
L3	1.00	1.15	1.30
L4	0.05		0.40

Figure 20. TO-LL recommended footprint (dimensions are in mm)



DM00276569_10_FP

Figure 23. TO-LL orientation in tape pocket



Revision history

Table 9. Document revision history

Date	Version	Changes
18-Dec-2019	1	First release.
29-Apr-2021	2	Updated title and <i>Device summary</i> in cover page. Updated <i>Section 4 Package information</i> . Minor text changes.
09-Apr-2026	3	Updated TO-LL package drawing on cover page. Updated <i>Section 1: Electrical ratings</i> , <i>Section 2: Electrical characteristics</i> , <i>Section 2.1: Electrical characteristics (curves)</i> and <i>Section 3: Test circuits</i> . Updated <i>Section 4: Package information</i> .
27-Apr-2026	4	Updated <i>Table 3. Avalanche characteristics</i> . Updated <i>Table 5. Dynamic</i> .

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