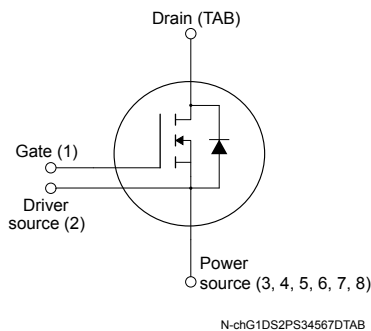
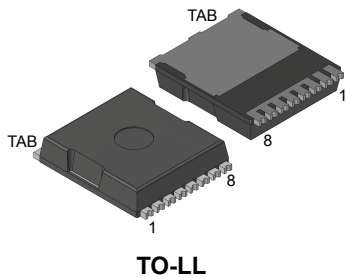


N-channel 650 V, 24.7 mΩ typ., 72 A MDmesh M9 Power MOSFET in a TO-LL package



Product status link

[STO65N033M9](#)

Product summary

Order code	STO65N033M9
Marking	65N033M9
Package	TO-LL
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STO65N033M9	650 V	33 mΩ	72 A

- Easy to drive
- Excellent switching performance thanks to the extra driving source pin
- Higher dv/dt capability
- Higher V_{DSS} rating
- Very low FOM (R_{DS(on)} · Q_g)
- 100% avalanche tested

Applications

- Boost PFC converters
- LLC converters
- Switching applications

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh M9 technology, suitable for medium/high voltage MOSFETs featuring very low R_{DS(on)} per area. The silicon based M9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The resulting product has one of the lower on-resistance and reduced gate charge values, among all silicon based fast switching super-junction Power MOSFETs, making it particularly suitable for applications that require superior power density and outstanding efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 30	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	72	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	45	
$I_{DM}^{(2)}$	Drain current (pulsed)	273	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	357	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	50	V/ns
$di/dt^{(3)}$	Peak diode recovery current slope	400	A/ μ s
$dv/dt^{(4)}$	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range		$^\circ\text{C}$

1. Referred to TO-247 long leads package.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 36\text{ A}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
4. $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.35	$^\circ\text{C/W}$
R_{thJA}	Thermal resistance, junction-to-ambient ⁽¹⁾	43	$^\circ\text{C/W}$
	Thermal resistance, junction-to-ambient ⁽²⁾	22	

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.
2. When mounted on 40x40 mm area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	8	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	932	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$	-	-	200	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.2	3.7	4.2	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 36\text{ A}$	-	24.7	33	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$, $V_{GS} = 0\text{ V}$	-	6400	-	pF
C_{oss}	Output capacitance		-	110	-	pF
$C_{oss\text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	1307	-	pF
R_g	Intrinsic gate resistance	$f = 250\text{ kHz}$, open drain	-	5.9	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 36\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 14. Test circuit for gate charge behavior)	-	123	-	nC
Q_{gs}	Gate-source charge		-	35	-	nC
Q_{gd}	Gate-drain charge		-	43	-	nC

1. $C_{oss\text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 36\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	48.7	-	ns
t_r	Rise time		-	16.6	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	162.7	-	ns
t_f	Fall time		-	4.3	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-	-	72	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-	-	273	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 72\text{ A}$	-	-	1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 72\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 150\text{ V}$	-	292	-	ns
Q_{rr}	Reverse recovery charge		-	4.3	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	26.6	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 72\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 150\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	450	-	ns
Q_{rr}	Reverse recovery charge		-	10.2	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	41.4	-	A

1. Referred to TO-247 long leads package.
2. Pulse width is limited by safe operating area.
3. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

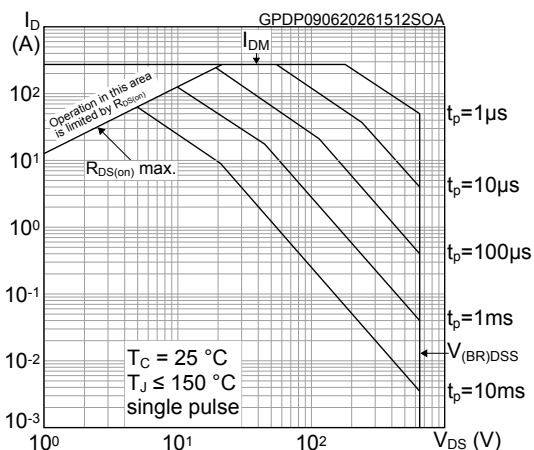
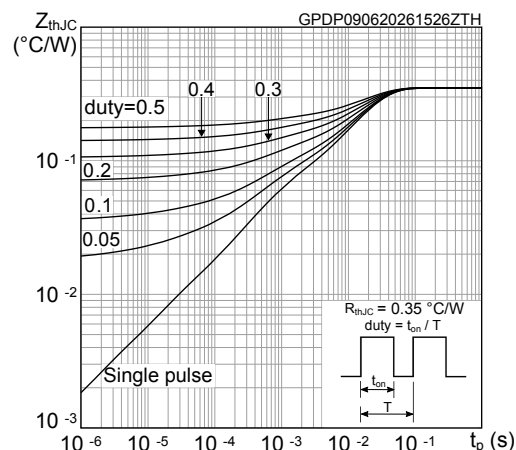
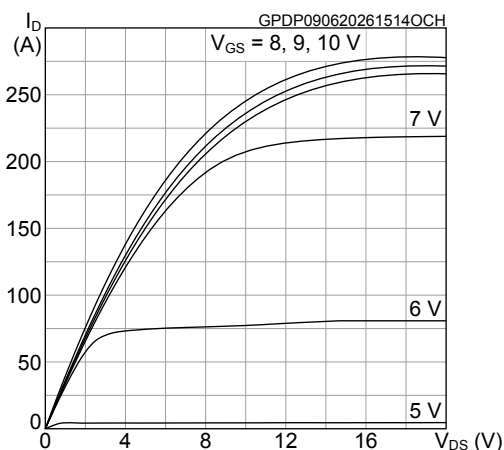
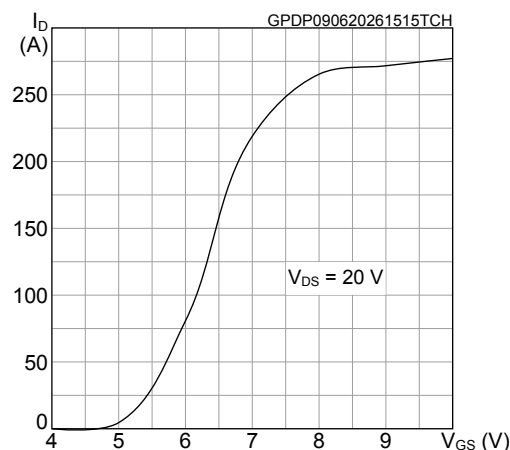
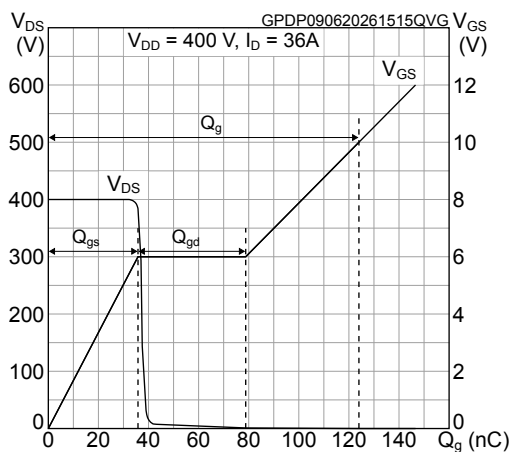
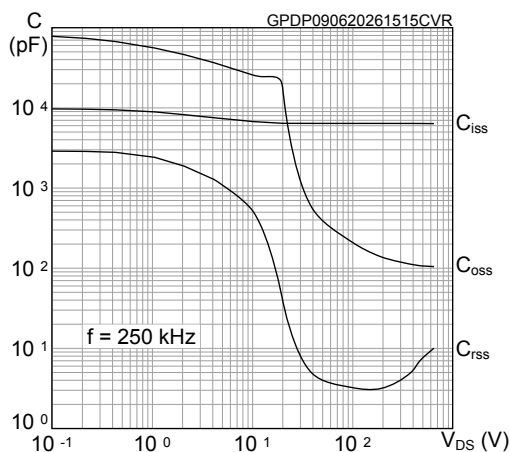
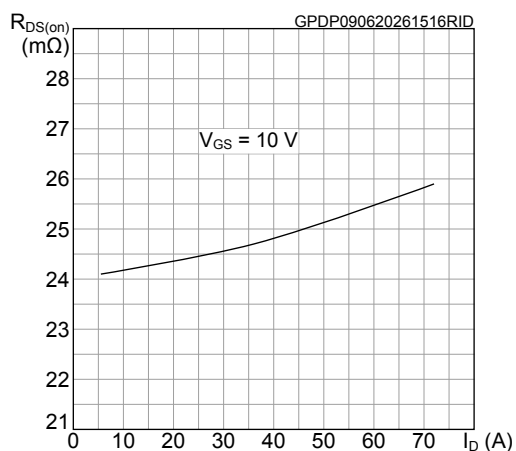
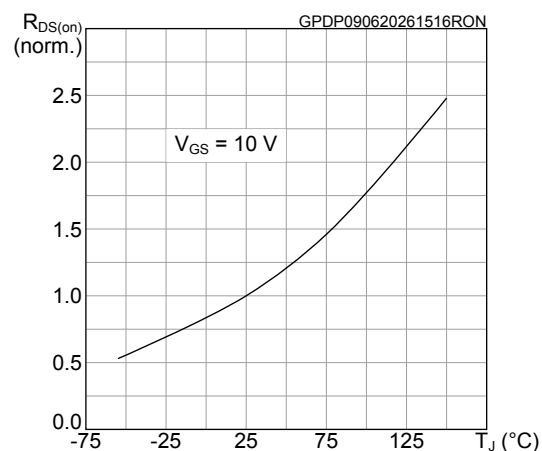
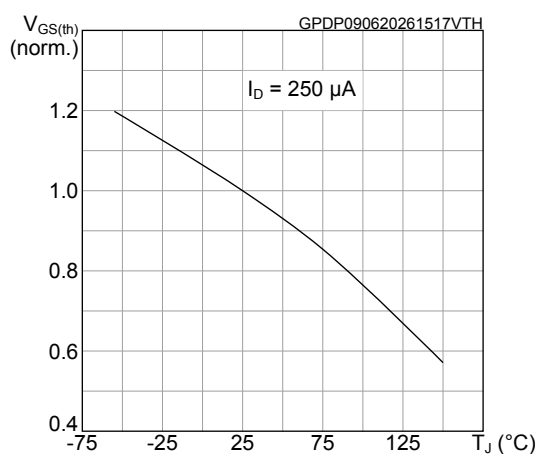
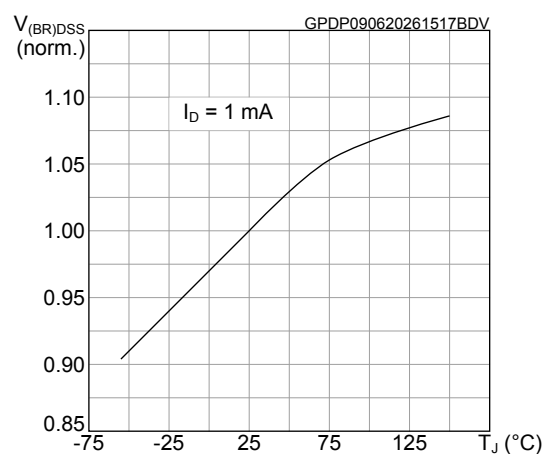
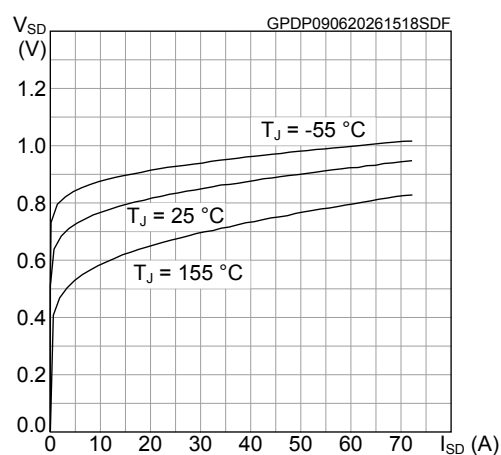
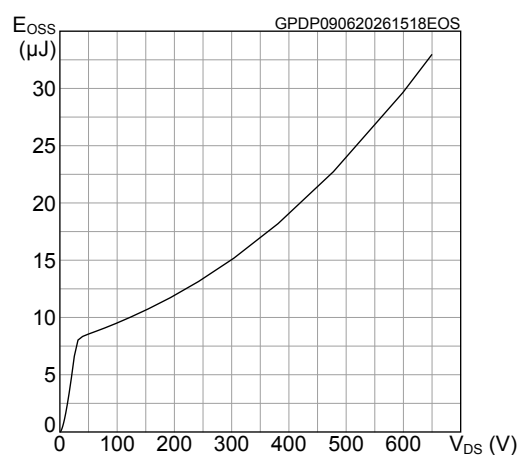
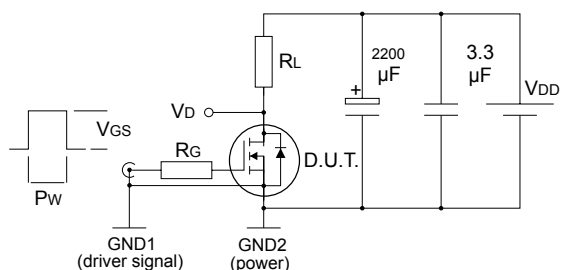
Figure 1. Safe operating area

Figure 2. Maximum transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical capacitance characteristics


Figure 7. Typical drain-source on-resistance

Figure 8. Normalized on-resistance vs temperature

Figure 9. Normalized gate threshold vs temperature

Figure 10. Normalized breakdown voltage vs temperature

Figure 11. Typical reverse diode forward characteristics

Figure 12. Typical output capacitance stored energy


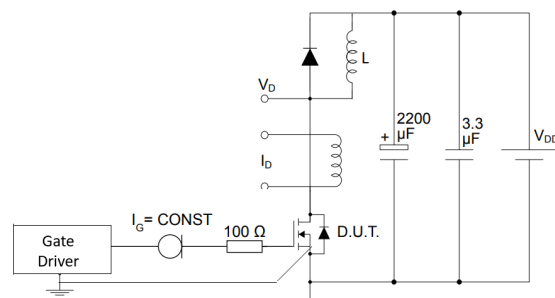
3 Test circuits

Figure 13. Test circuit for resistive load switching times



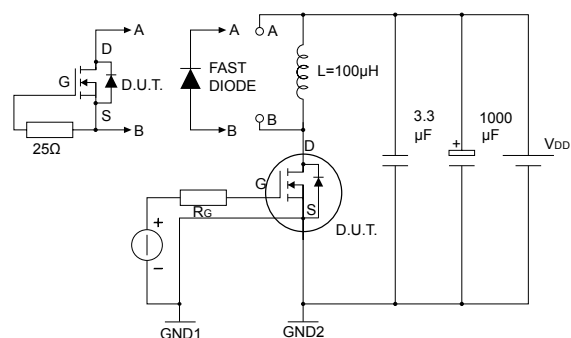
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Figure 14. Test circuit for gate charge behavior



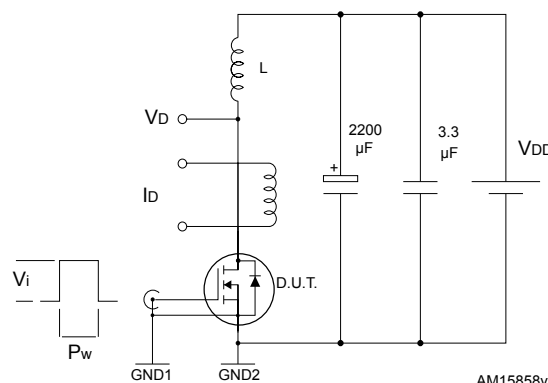
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Figure 15. Test circuit for inductive load switching and diode recovery times



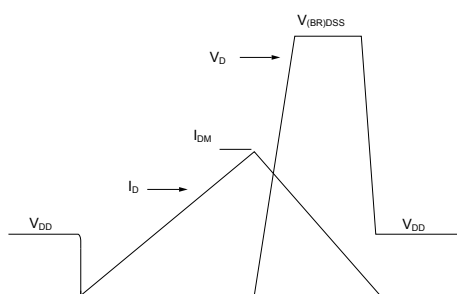
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Figure 16. Unclamped inductive load test circuit



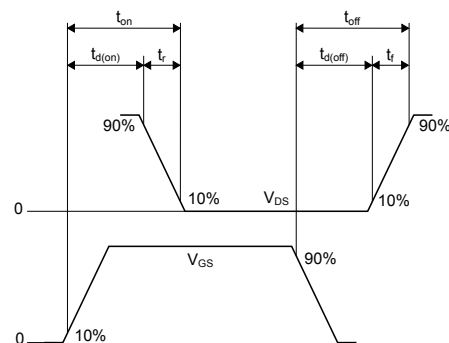
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Figure 17. Unclamped inductive waveform



AM01472v1

Figure 18. Switching time waveform



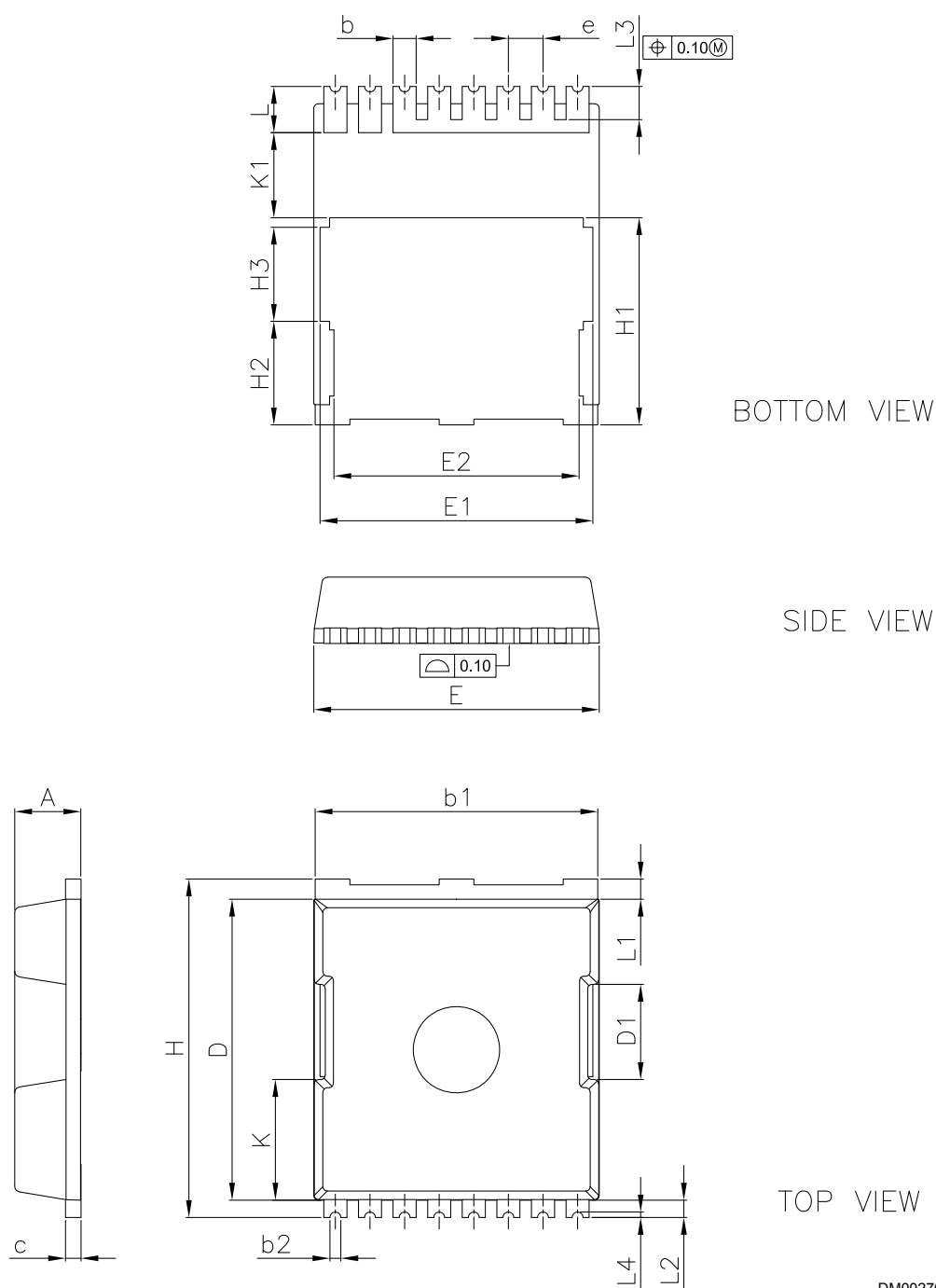
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL package information

Figure 19. TO-LL package outline

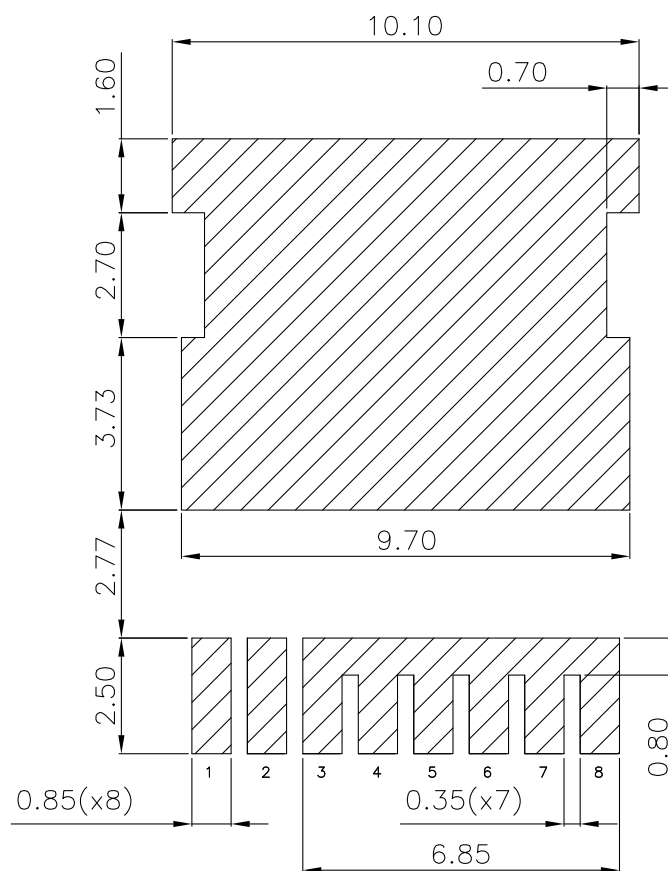


DM00276569_Rev_10

Table 8. TO-LL package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
b	0.60	0.80	0.90
b1	9.70	9.80	9.90
b2	0.20		0.50
c	0.40	0.50	0.60
D	10.28	10.43	10.58
D1	3.15	3.30	3.45
E	9.70	9.90	10.10
E1	9.31	9.46	9.61
E2	8.35	8.50	8.65
e	1.10	1.20	1.30
H	11.48	11.73	11.88
H1	7.00	7.15	7.30
H2	3.34	3.59	3.84
H3	3.11	3.26	3.41
K	4.03	4.18	4.33
K1	2.85	2.95	3.05
L	1.45	1.60	1.75
L1	0.55	0.70	0.85
L2	0.45	0.60	0.75
L3	1.00	1.15	1.30
L4	0.05		0.40

Figure 20. TO-LL recommended footprint (dimensions are in mm)



DM00276569_10_FP

4.2 TO-LL packing information

Figure 21. Carrier tape outline and dimensions

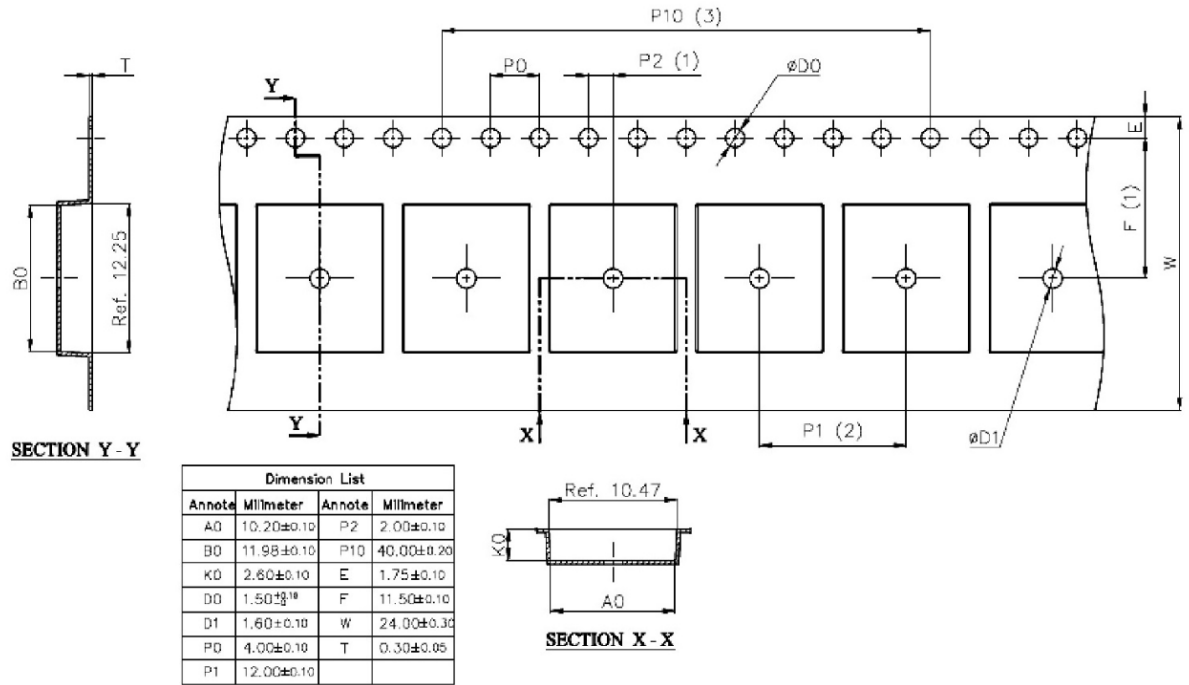


Figure 22. Reel outline and dimensions

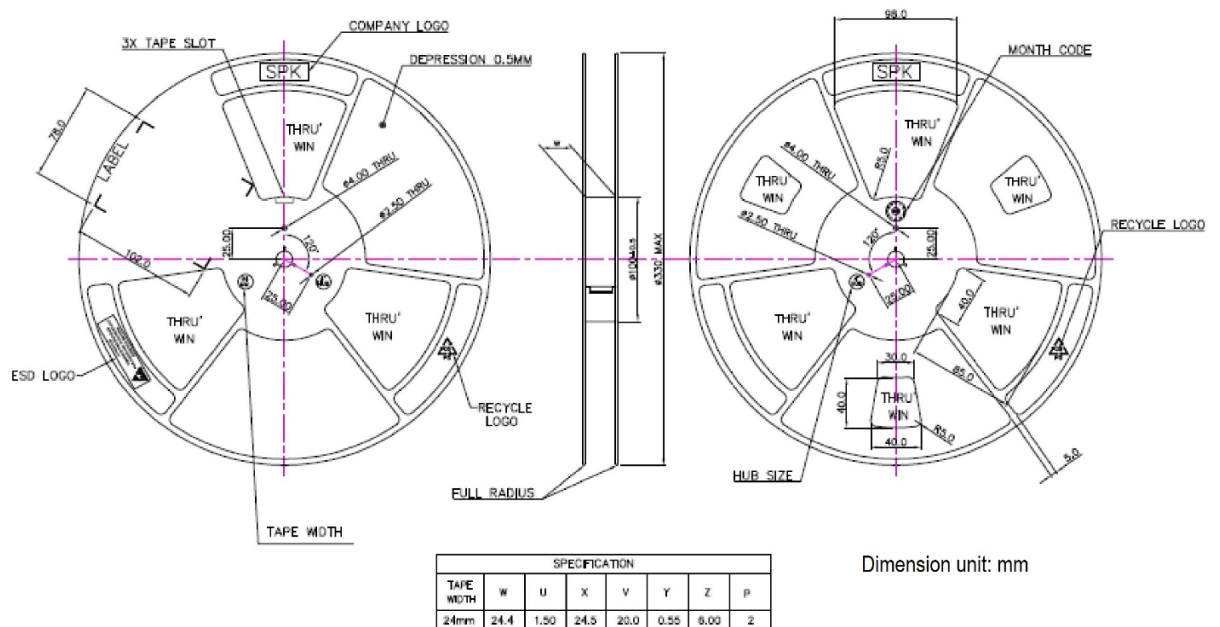
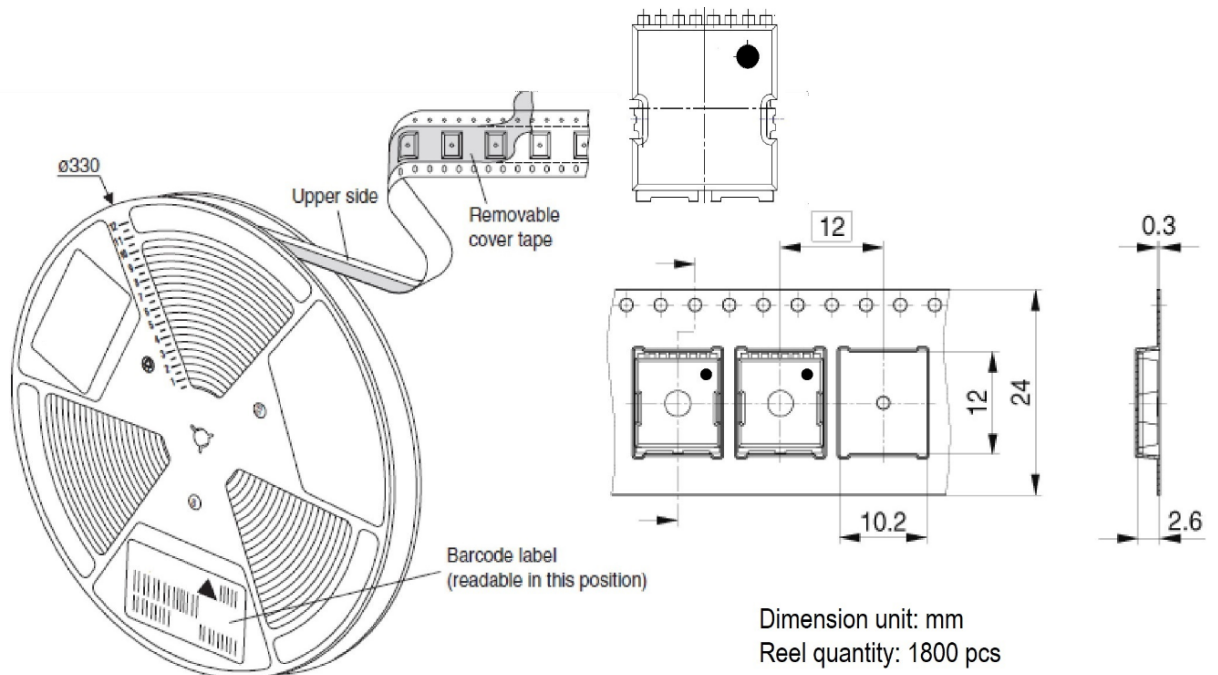


Figure 23. TO-LL orientation in tape pocket



Revision history

Table 9. Document revision history

Date	Revision	Changes
10-Jun-2026	1	First release.

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1	Electrical ratings	2
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