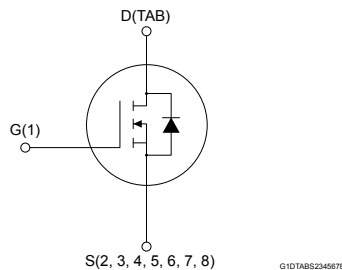
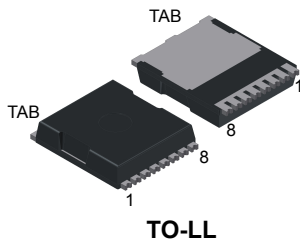


N-channel 100 V, 1.6 mΩ max., 366 A STripFET F8 Power MOSFET in a TO-LL package



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STO350N10F8	100 V	1.6 mΩ	366 A

- MSL1 grade
- 175 °C maximum operating junction temperature
- 100% avalanche tested
- Low gate charge Q_g

Applications

- Industrial tools, motor drives and equipment
- Industrial motor control
- Power supplies and converters

Description

The **STO350N10F8** is a 100 V N-channel enhancement mode Power MOSFET designed in STripFET F8 technology featuring an enhanced trench gate structure. It ensures a state-of-the-art of figure of merit for very low on-state resistance while reducing internal capacitances and gate charge for faster and more efficient switching.



Product status link

[STO350N10F8](#)

Product summary

Order code	STO350N10F8
Marking	350N10F8
Package	TO-LL
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings (at $T_C = 25\text{ °C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}^{(2)}$	366	A
	Drain current (continuous) at $T_C = 100\text{ °C}^{(2)}$	259	
	Drain current (continuous) at $T_C = 25\text{ °C}^{(3)}$	300	
$I_{DM}^{(1)(2)(4)}$	Drain current (pulsed), $t_P = 10\text{ }\mu\text{s}$	1466	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	450	W
I_{AS}	Single pulse avalanche current (pulse width limited by maximum junction temperature)	90	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = 90\text{ A}$, $R_G = 25\text{ }\Omega$)	810	mJ
T_J	Operating junction temperature range	-55 to 175	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		$^{\circ}\text{C}$

1. Specified by design, not tested in production.
2. This is the theoretical current value only related to the silicon.
3. This current value is limited by package.
4. Pulse width is limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient (on 2s2p FR-4 board vertical in still area)	12	$^{\circ}\text{C/W}$
$R_{thJC}^{(2)}$	Thermal resistance, junction-to-case	0.33	$^{\circ}\text{C/W}$

1. Measured on 4 layer PCB according to Jedec 51.2 in natural convection (still air).
2. Measured according to Jedec 51.14.

2 Electrical characteristics

$T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	100	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}^{(1)}$	-	-	100	
I_{GSS}	Gate-body leakage current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$	-	-	100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 90\text{ A}$	-	1.1	1.6	m Ω
R_G	Gate resistance		-	0.7	-	Ω

1. Specified by design and evaluated by characterization, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}^{(1)}$	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	13790	-	pF
$C_{oss}^{(1)}$	Output capacitance		-	2800	-	pF
$C_{rss}^{(1)}$	Reverse transfer capacitance		-	80	-	pF
$Q_g^{(1)}$	Total gate charge	$V_{DD} = 50\text{ V}$, $I_D = 90\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$	-	222	-	nC
$Q_{gs}^{(1)}$	Gate-source charge		-	66	-	nC
$Q_{gd}^{(1)}$	Gate-drain charge		-	57	-	nC
$Q_{g(sync)}^{(1)}$	Total gate charge, sync. MOSFET	$V_{DS} = 0.1\text{ V}$, $V_{GS} = 0\text{ to }10\text{ V}$	-	181	-	nC
$Q_{oss}^{(1)}$	Output charge	$V_{DD} = 50\text{ V}$, $V_{GS} = 0\text{ V}$	-	251	-	nC

1. Specified by design and evaluated by characterization, not tested in production.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}^{(1)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$, $I_D = 90\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	50	-	ns
$t_r^{(1)}$	Rise time		-	30	-	ns
$t_{d(off)}^{(1)}$	Turn-off delay time		-	121	-	ns
$t_f^{(1)}$	Fall time		-	42	-	ns

1. Specified by design and evaluated by characterization, not tested in production.

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)(2)}$	Forward on current (continuous)	$T_C = 25\text{ }^{\circ}\text{C}$	-	-	300	A
V_{SD}	Forward on voltage	$I_{SD} = 90\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.2	V
$t_{rr}^{(1)}$	Reverse recovery time	$I_D = 90\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 80\text{ V}$	-	88	-	ns
$Q_{rr}^{(1)}$	Reverse recovery charge		-	218	-	nC
$I_{RRM}^{(1)}$	Reverse recovery current		-	5	-	A

1. Specified by design and evaluated by characterization, not tested in production.
2. This is the theoretical current value only related to the silicon.

2.1 Electrical characteristics (curves)

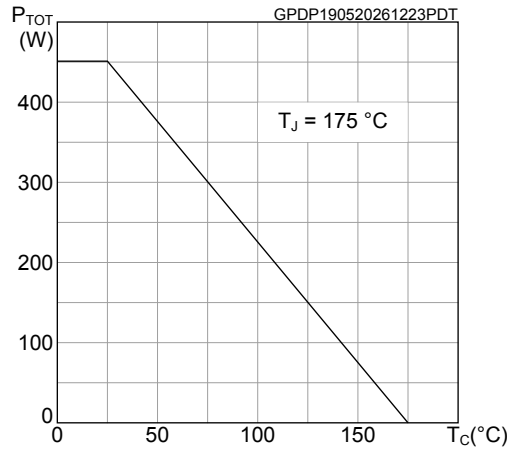
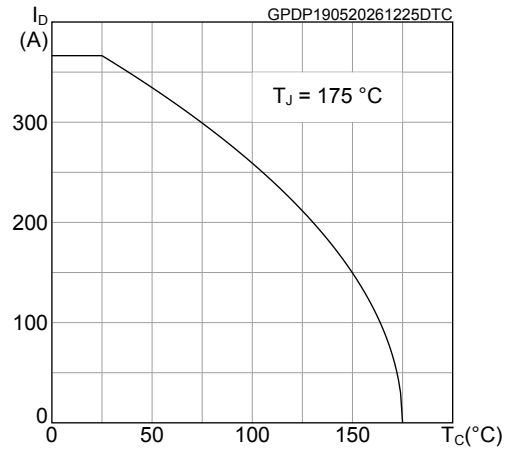
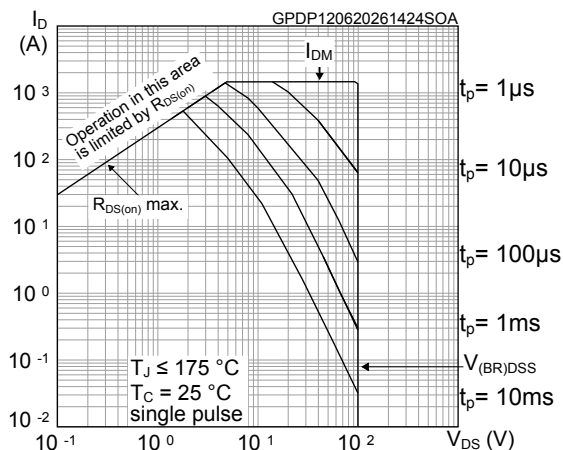
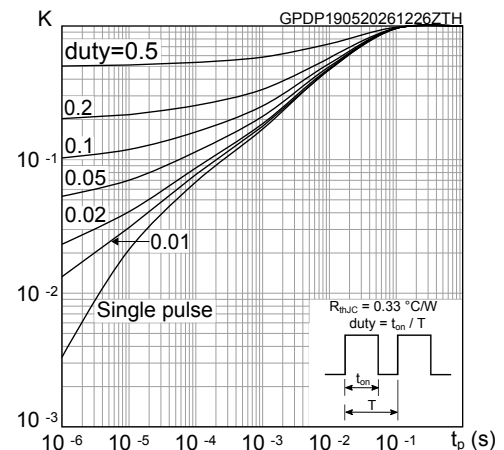
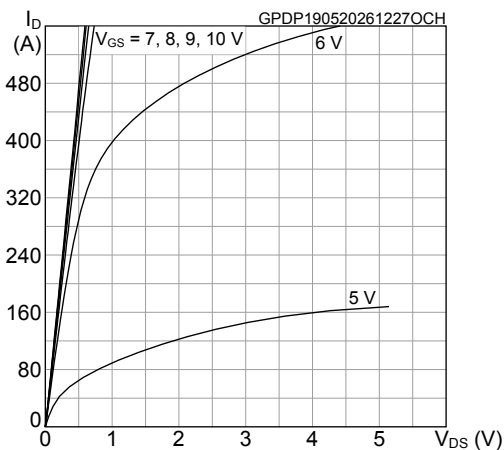
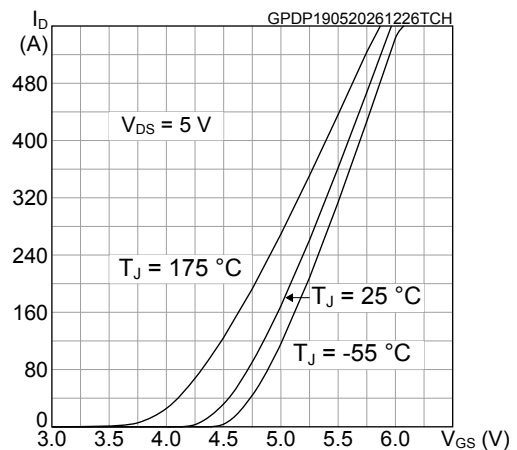
Figure 1. Total power dissipation

Figure 2. Drain current vs case temperature

Figure 3. Safe operating area

Figure 4. Normalized transient thermal impedance

Figure 5. Typical output characteristics

Figure 6. Typical transfer characteristics


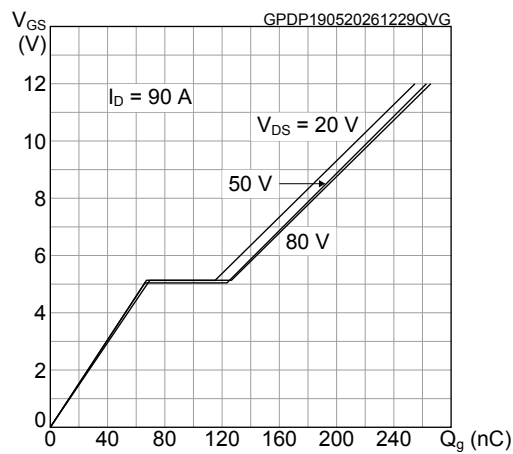
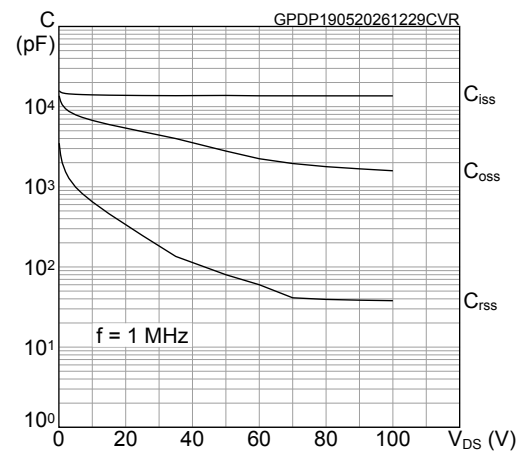
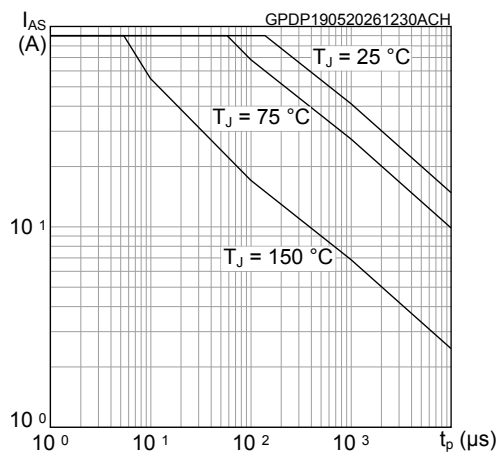
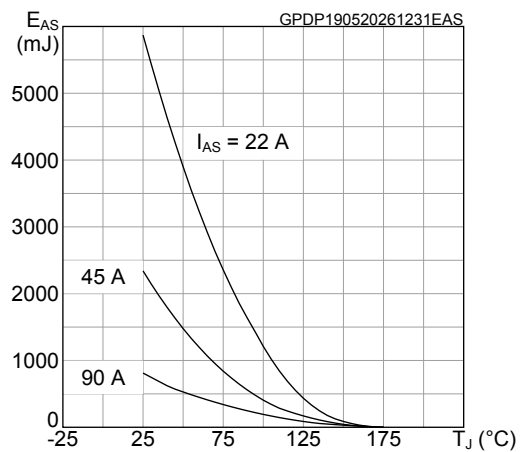
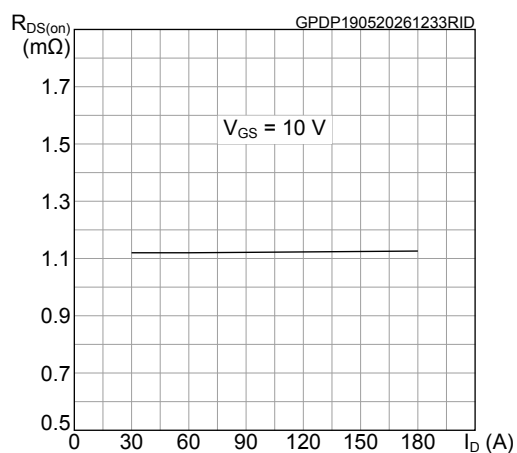
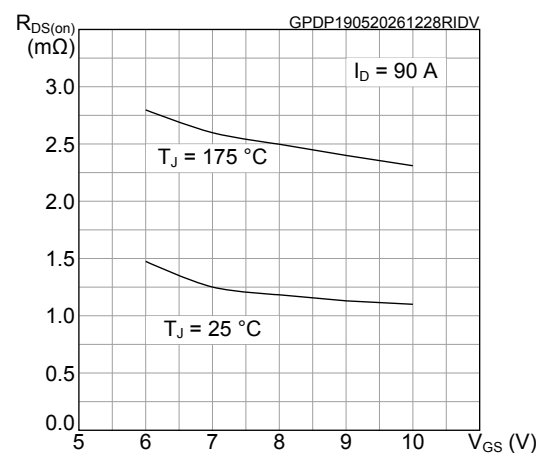
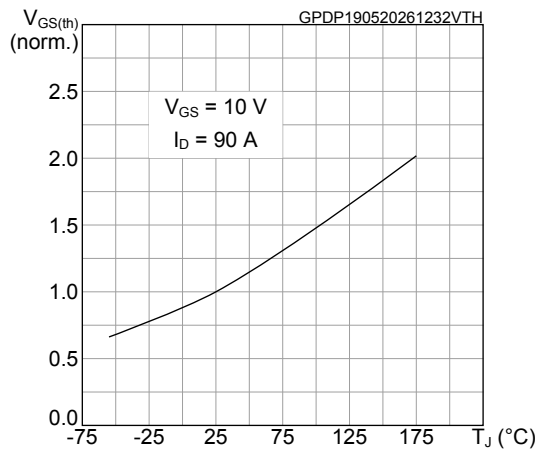
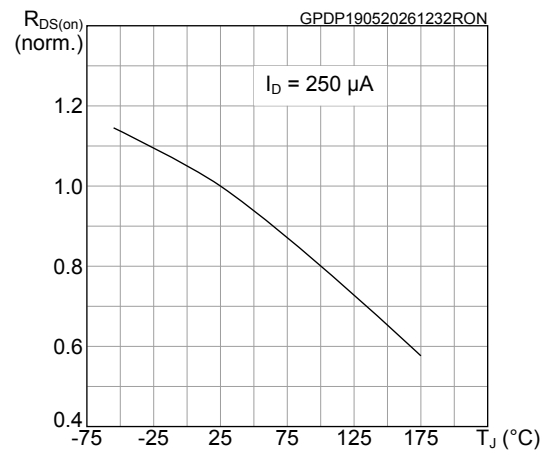
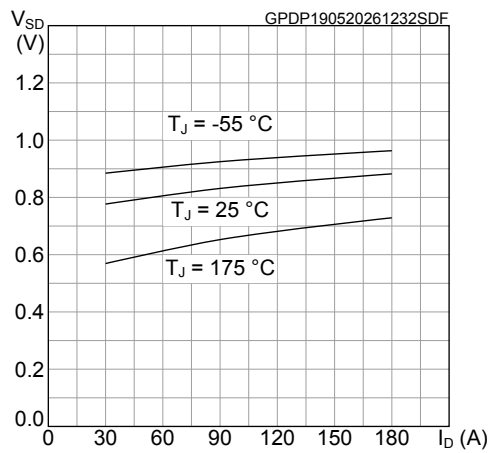
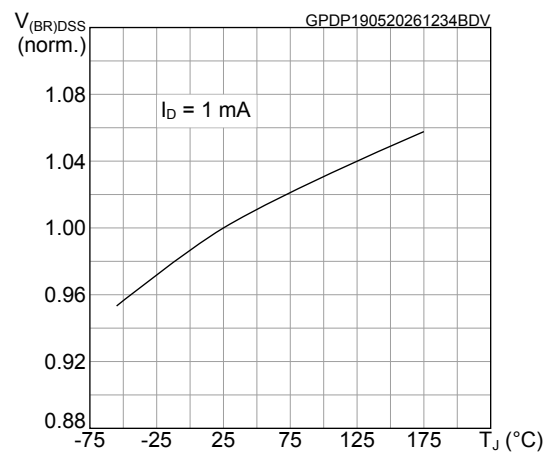
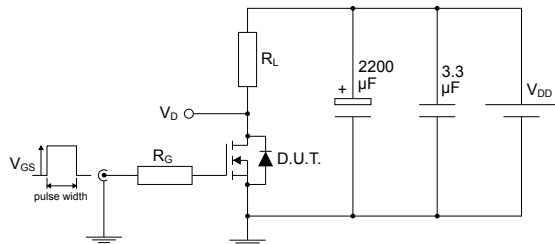
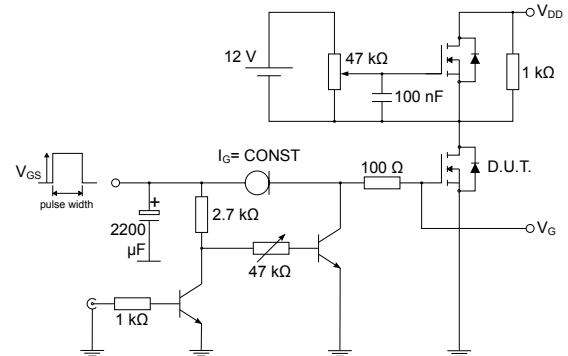
Figure 7. Typical gate charge characteristics

Figure 8. Typical capacitance characteristics

Figure 9. Avalanche characteristics

Figure 10. Avalanche energy

Figure 11. Typical drain-source on-resistance

Figure 12. Typical on-resistance vs gate-source voltage


Figure 13. Normalized on-resistance vs temperature

Figure 14. Normalized gate threshold voltage vs temperature

Figure 15. Typical reverse diode forward characteristics

Figure 16. Normalized $V_{(BR)DSS}$ vs temperature


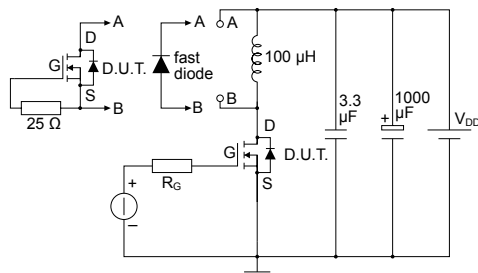
3 Test circuits

Figure 17. Test circuit for resistive load switching times


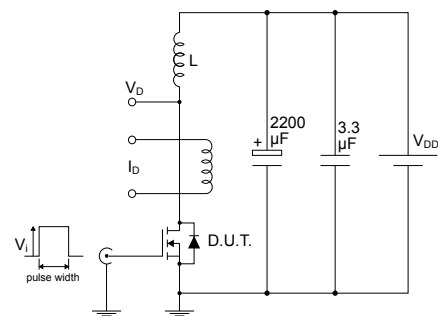
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Figure 18. Test circuit for gate charge behavior


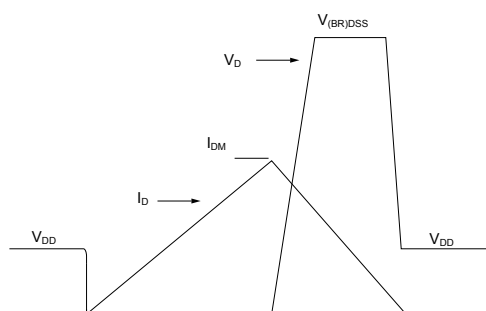
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Figure 19. Test circuit for inductive load switching and diode recovery times


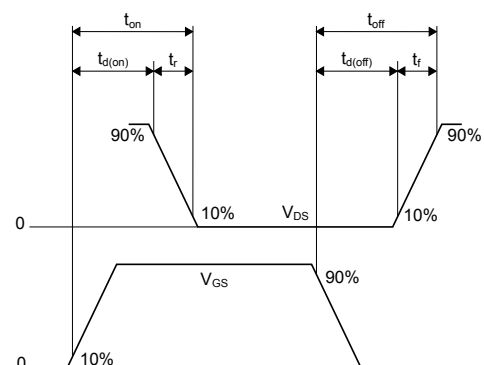
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Figure 20. Unclamped inductive load test circuit


AM01471v1

Figure 21. Unclamped inductive waveform


AM01472v1

Figure 22. Switching time waveform


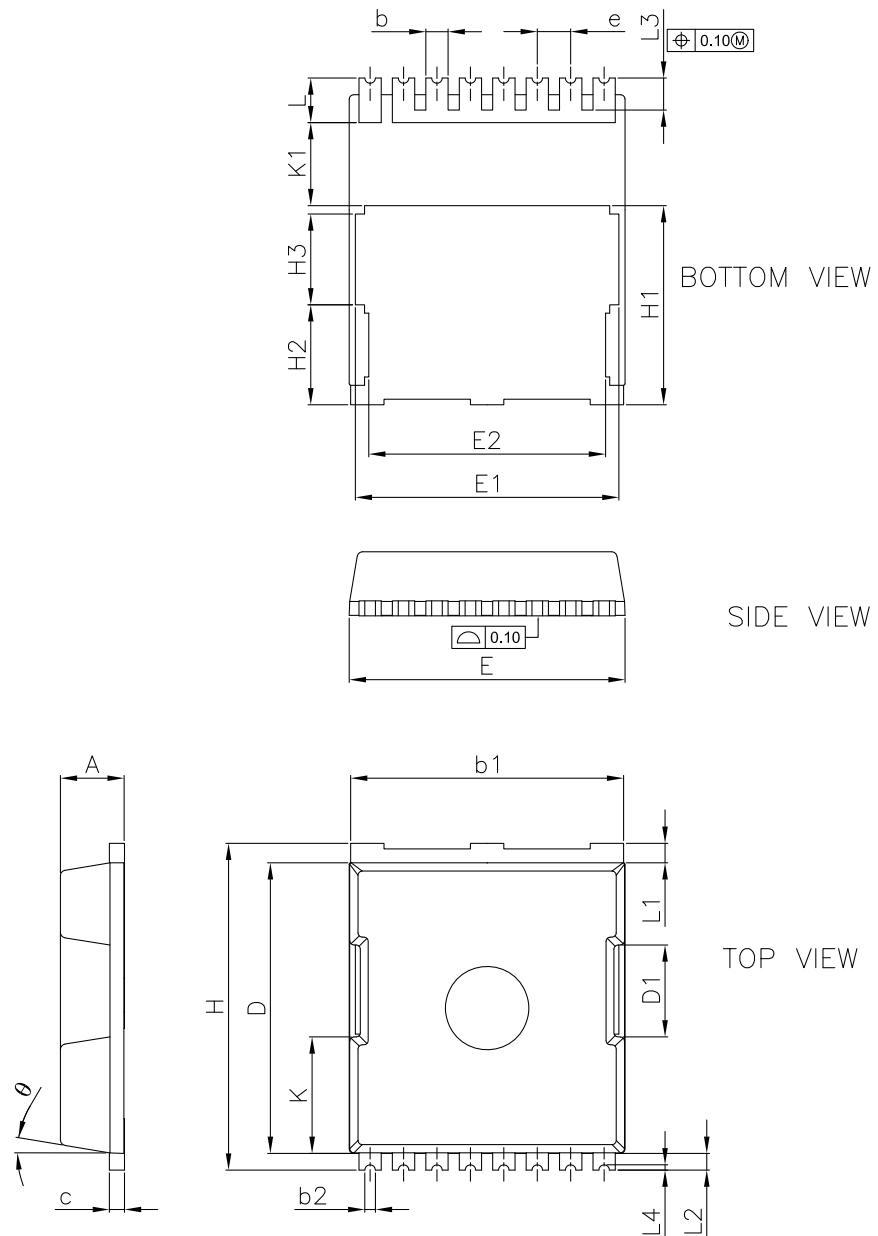
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-LL package information

Figure 23. TO-LL package outline

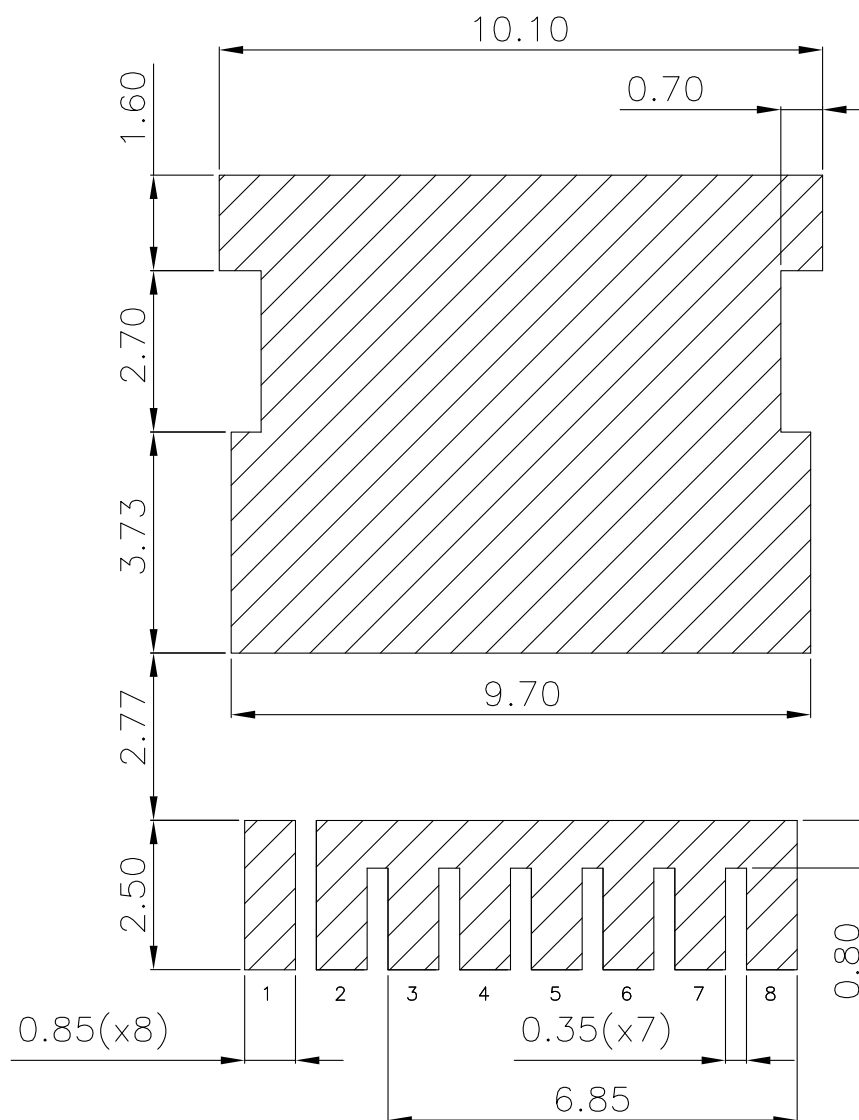


DM00276569_10

Table 7. TO-LL package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.40
b	0.60	0.80	0.90
b1	9.70	9.80	9.90
b2	0.20		0.50
c	0.40	0.50	0.60
D	10.28	10.43	10.58
D1	3.15	3.30	3.45
E	9.70	9.90	10.10
E1	9.31	9.46	9.61
E2	8.35	8.50	8.65
e	1.10	1.20	1.30
H	11.48	11.73	11.88
H1	7.00	7.15	7.30
H2	3.34	3.59	3.84
H3	3.11	3.26	3.41
K	4.03	4.18	4.33
K1	2.85	2.95	3.05
L	1.45	1.60	1.75
L1	0.55	0.70	0.85
L2	0.45	0.60	0.75
L3	1.00	1.15	1.30
L4	0.05		0.40

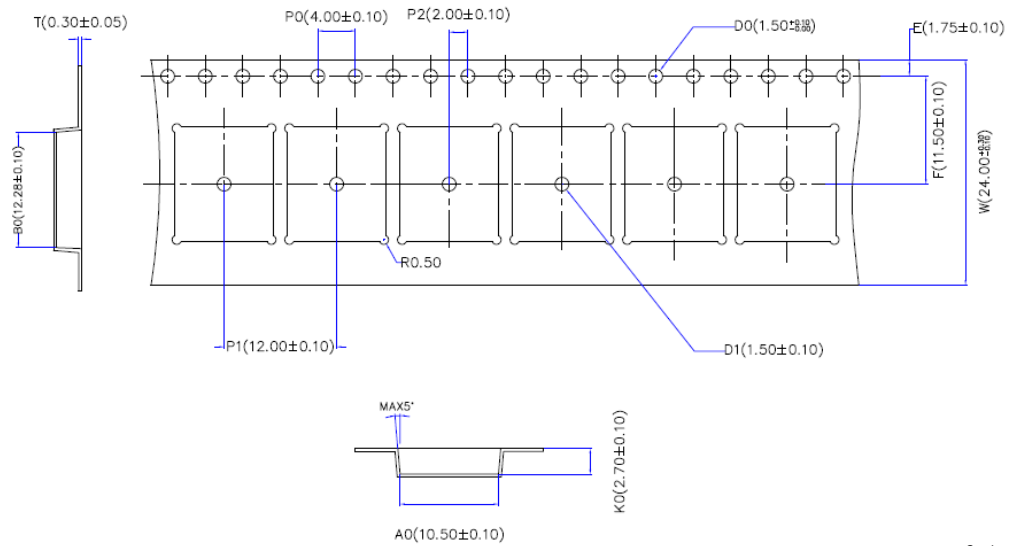
Figure 24. TO-LL recommended footprint (dimensions are in mm)



DM00276569_10_FP

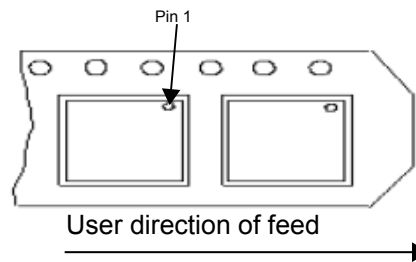
4.2 TO-LL packing information

Figure 25. Carrier tape outline and dimensions



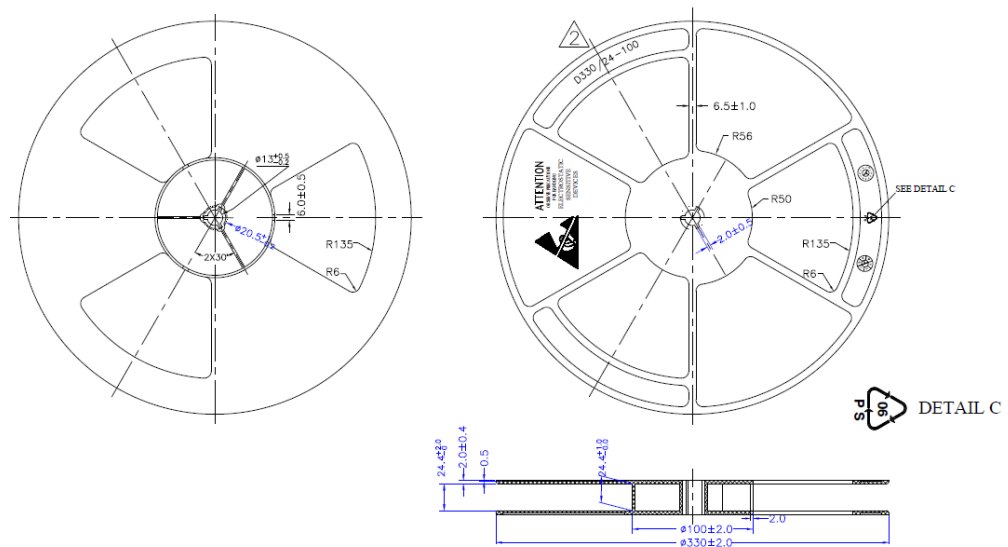
Carrier_DM00282027_5

Figure 26. TO-LL orientation in carrier tape



orientation_carrier_tape_0031932_65

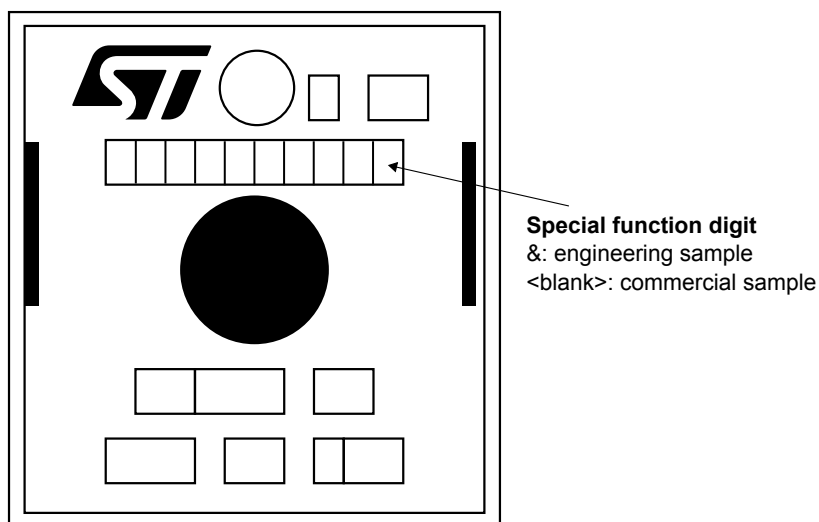
Figure 27. Reel outline and dimensions



Reel_DM00282027_5

4.3 TO-LL marking information

Figure 28. TO-LL marking information



Note: *Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.*

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

Revision history

Table 8. Document revision history

Date	Version	Changes
21-Jul-2025	1	First release.
21-May-2026	2	Updated <i>Section 1: Electrical ratings</i> , <i>Section 2: Electrical characteristics</i> and <i>Section 2.1: Electrical characteristics (curves)</i> .
15-Jun-2026	3	Updated <i>Figure 3. Safe operating area</i> .

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