STM32WBA2xxx

Multiprotocol wireless 32-bit MCU Arm® Cortex®-M33 with TrustZone®, FPU, Bluetooth® LE, and IEEE802.15.4 radio solution

Datasheet - production data

Features

Includes ST state-of-the-art patented technology

Ultra-low-power radio

- 2.4 GHz radio
- RF transceiver supporting Bluetooth® LE, IEEE 802.15.4-2015 PHY and MAC, supporting Matter and Zigbee®
- RX sensitivity: -96 dBm (Bluetooth® LE at 1 Mbps), -100 dBm (IEEE 802.15.4 at 250 kbps)
- Programmable output power, up to +10 dBm with 1 dB steps
- Support for external PA
- Packet traffic arbitration
- Integrated balun to reduce BOM
- Suitable for systems requiring compliance with radio frequency regulations ETSI EN 300 328, EN 300 440, FCC CFR47 Part 15, and ARIB STD-T66

Bluetooth® LE

- LE 2M
- LE coded
- Direction finding
- LE power control
- Isochronous channels
- Extended advertising
- Periodic advertising
- LE secure connections
- LE audio
- Mesh networking
- Qualified against Bluetooth® Core 6.0

UFQFPN32 (5 x 5 mm)
UFQFPN48 (7 x 7 mm)

Thin WLCSP37
(2.61 x 2.41 mm)

Ultra-low-power with FlexPowerControl

- 1.71 to 3.6 V power supply
- -40 to 85/105 °C ambiant temperature range
- Autonomous peripherals with DMA, functional down to Stop 1 mode
- 110 nA Standby mode (7 wake-up pins)
- 490 nA Standby mode with 64-Kbyte SRAM
- 980 nA Standby mode with 64-Kbyte SRAM, 2.4 GHz radio, RTC
- 4.81 µA Stop 1 mode with 64-Kbyte SRAM, 2.4 GHz radio, RTC
- 21 µA/MHz Run mode
- Radio: Rx 3.58 mA/ Tx at 0 dBm 4.65 mA

Core

- Arm® 32-bit Cortex®-M33 CPU with TrustZone®, MPU, DSP, and FPU running at up to 64 MHz

ART Accelerator

- 4-Kbyte instruction cache allowing 0-wait-state execution from flash memory (frequency up to 64 MHz, 96 DMIPS)

Benchmarks

- 264 CoreMark® (4.12 CoreMark/MHz)

Memories

- 512-Kbyte flash memory with ECC and 10 kcycles

- 96-Kbyte SRAM, including 32 Kbytes with parity check
- 512-byte (32 rows) OTP
- One Quad-SPI memory interface

Power management

- Embedded regulator LDO and SMPS step-down converter, supporting switch on-the-fly and voltage scaling

Clock management

- 32 MHz crystal oscillator
- 32 kHz crystal oscillator (LSE)
- Internal low-power 32 kHz (±5%) RC
- Internal 16 MHz factory-trimmed RC (±1%)
- PLL for system clock, audio, USB, and ADC

General-purpose input/output

- Up to 27 I/Os (most of them 5 V-tolerant) with interrupt capability

Analog peripherals (independent supply)

- 12-bit ADC 2.5 Msps, up to 16-bit with hardware oversampling

Communication peripherals

- One USB full-speed selectable host or device controller
- One SAI (serial audio interface)
- One USART (ISO 7816, IrDA, modem)
- One LPUART (ISO 7816, modem)
- One SPI
- Two I2Cs Fm+ (1 Mbit/s), SMBus/PMBus®

System peripherals

- Two 16-bit timers
- One 32-bit timer
- Two low-power 16-bit timers (available in Stop mode)
- Two SysTick timers
- RTC with hardware calendar and calibration
- One watchdog
- 8-channel DMA controller, functional in Stop mode

Security and cryptography

Arm® TrustZone® and securable I/Os, memories, and peripherals

- Flexible life cycle scheme with readout protection (RDP) and password protected debug
- Root of trust thanks to unique boot entry and secure hide protection area (HDP)
- Secure boot and secure firmware update
- AES accelerator
- Public key accelerator, ECC and RSA, SCA resistant
- HASH hardware accelerator
- True random number generator, NIST SP800-90B compliant
- 96-bit unique ID
- Antitamper protections

Development support

- Serial wire debug (SWD), JTAG
- Embedded trace (ETM)

All packages are ECOPACK2 compliant.

Table 1. Device summary

Reference	Part numbers
STM32WBA23xx	STM32WBA23KE, STM32WBA23CE
STM32WBA25xx	STM32WBA25HE, STM32WBA25CE

Contents

List of tables

List of figures

1 Introduction

This document provides the ordering information and mechanical device characteristics the STM32WBA2xxx microcontrollers, based on the Arm®(a) Cortex®-M33 core. It must be read in conjunction with the reference manual (RM0521), available from the STMicroelectronics website *www.st.com*.

Throughout the whole document TBD indicates a value to be defined.

For information on the Arm® Cortex®(b)-M33 core, refer to the Cortex®-M33 Technical Reference Manual, available on the www.arm.com website.

For information on 802.15.4, refer to the IEEE website (www.ieee.org).

For information on Bluetooth® LE, refer to www.bluetooth.com.

a. Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries or affiliates) in the US and/or elsewhere.

b. The Arm word and logo are trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. All rights reserved.

2 Description

The STM32WBA2xxx multiprotocol wireless and ultra-low-power devices embed a powerful and ultra-low-power 2.4 GHz RADIO compliant with the Bluetooth® LE specifications and with IEEE 802.15.4-2015. They contain a high-performance Arm® Cortex®-M33 32-bit RISC core. They operate at a frequency of up to 64 MHz.

The devices integrate a 2.4 GHz RADIO supporting Bluetooth® LE, Thread®, and Zigbee®. It provides support for an array of up to eight antennas and an external power amplifier. The PTA (packet traffic arbitration) interface is supported.

The Cortex®-M33 core features a single-precision floating-point unit (FPU), supporting all the Arm single-precision data-processing instructions and all the data types. This core also implements a full set of DSP (digital signal processing) instructions and a memory protection unit (MPU) that enhances the application security.

The devices embed high-speed memories (512 Kbytes of flash memory and 96 Kbytes of SRAM), one Quad-SPI memory interface, and a range of enhanced I/Os and peripherals connected to AHB and APB buses on the 32-bit multi-AHB bus matrix.

The devices offer a security foundation compliant with the TBSA (trusted-based security architecture) requirements from Arm. It embeds the necessary security features to implement a secure boot, secure data storage, and secure firmware update. A flexible life cycle is managed through multi-level readout protection and debug unlock with password.

Firmware hardware isolation is supported using securable peripherals, memories and I/Os, and privilege configuration of peripherals and memories.

The devices feature several protection mechanisms for embedded flash memory and SRAM: readout protection, write protection, secure, and hide protection areas.

The devices embed several peripherals reinforcing security: a fast AES coprocessor, a PKA (public key accelerator) with DPA resistance, a HASH hardware accelerator, and a true random number generator.

The devices offer active tamper detection and protection against transient perturbation attacks with several internal monitoring mechanisms generating secret data erasure in the case of an attack.

The devices offer one 12-bit ADC (2.5 Msps), a low-power RTC, one 32-bit and two 16-bit general-purpose timers, and two 16-bit low-power timers. They also feature standard and advanced communication interfaces, namely two I2Cs, one SPI, one SAI, one USART and one low-power UART, and one full-speed Host- and Device-capable USB.
The feature set is product-dependent.

The devices operate in the -40 to 85 °C and -40 to 105 °C temperature ranges from a 1.71 to 3.6 V power supply.

The design of low-power applications is enabled by a comprehensive set of power-saving modes.

Many peripherals (including radio, communication, analog, and timer peripherals) can be functional and autonomous in Stop mode with direct memory access thanks to BAM (background autonomous mode) support.

Some independent power supplies are supported, like an analog independent supply input for ADC, a 3.3 V dedicated supply input for USB, and radio-dedicated supply inputs for the 2.4 GHz RADIO.

The devices offer three packages, up to 48 pins, with or without SMPS.

Table 2. STM32WBA2xxx device features and peripheral counts

Peripherals		STM32WBA23KE	STM32WBA25HE	STM32WBA23CE	STM32WBA25CE
TrustZone®		Yes			
Flash memory density (Kbytes)		512			
SRAM density	SRAM1 (Kbytes)	64			
	SRAM2 (Kbytes)	32			
Quad-SPI		No	Quad	No	Quad
Bluetooth® LE	2 Mbps	Yes			
	Other data rates	Yes			
IEEE 802.15.4		Yes			
SMPS		No	Yes		
PTA		Yes			
External PA support		Yes			
Bluetooth® LE AoA, AoD support		Yes			
Backup registers		32 × 32-bit			
Timers	General purpose 32-bit	1			
	General purpose 16-bit	2			
	Low-power 16-bit	2			
	SysTick	2			
Communication interfaces	SPI	1			
	I2C	2			
	USART	1			
	LPUART	1			
	SAI	Yes			
	USB	No	Yes	No	Yes
RTC		Yes			

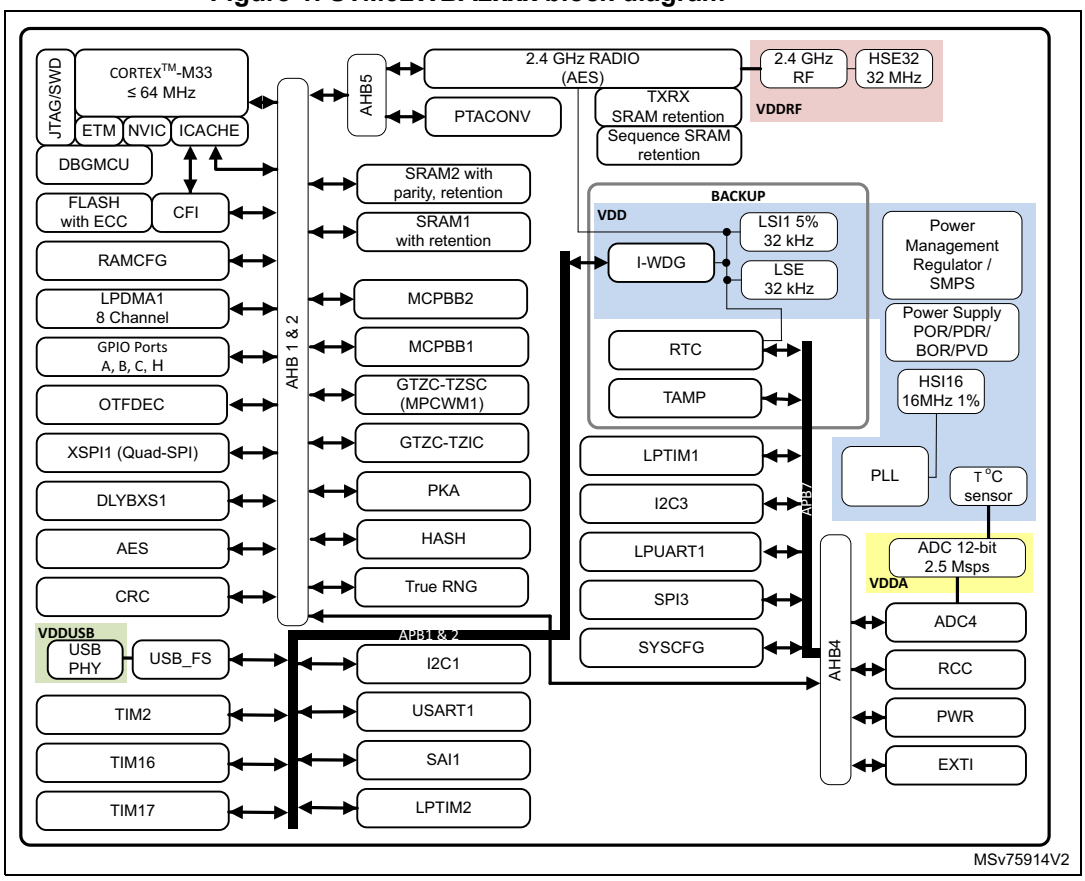
Table 2. STM32WBA2xxx device features and peripheral counts (continued)

Peripherals	STM32WBA23KE	STM32WBA25HE	STM32WBA23CE	STM32WBA25CE
Tamper pins (active tampers)(1)	3 (2)	2 (1)	4 (3)	
Wake-up pins	8	4	11	10
GPIOs	20	15	27	26
12-bit ADC	1 (7 ch)	1 (3 ch)	1 (7 ch)	1 (6 ch)
True random number generator	Yes			
AES	Yes			
Public key accelerator (PKA)	Yes			
HASH	Yes			
Maximum CPU frequency	64 MHz			
Operating temperature	-40 to 85 °C			
	-40 to 105 °C			
Operating voltage	1.71 to 3.6 V			
Package	UFQFPN32	Thin WLCSP37	UFQFPN48	

1. Active tampers in output sharing mode (one output shared by all inputs).

Figure 1 shows the general block diagram of the devices (some blocks may be unavailable on some versions).

Figure 1. STM32WBA2xxx block diagram



3 Functional overview

3.1 Arm® Cortex®-M33 core with TrustZone®, MPU, DSP, and FPU

The Cortex®-M33 core with TrustZone®, MPU, DSP, and FPU is a highly energy-efficient processor designed for microcontrollers and deeply embedded applications, especially those requiring efficient security.

The Cortex®-M33 processor delivers a high computational performance with low-power consumption and an advanced response to interrupts. It features:

- Arm® TrustZone® technology, using the Armv8-M main extension supporting secure and nonsecure states
- MPUs (memory protection units), supporting up to 16 regions for secure and nonsecure applications
- Configurable SAU (secure attribute unit) supporting up to eight memory regions as secure or nonsecure
- Floating-point arithmetic functionality, with support for single-precision arithmetic

The processor supports a set of DSP instructions for efficient signal processing and complex algorithm execution.

The Cortex®-M33 processor supports the following bus interfaces:

- System AHB (S-AHB) bus, used for instruction fetching and data access to the memory-mapped SRAM, peripheral, and Vendor_SYS regions of the Armv8-M memory map.
- Code AHB (C-AHB) bus, used for instruction fetching and data access to the code region of the Armv8-M memory map.

3.2 ART accelerator (ICACHE)

The instruction cache (ICACHE) is introduced on the C-AHB code bus of the Cortex®-M33 processor to improve performance when fetching an instruction (or data) from internal memories.

ICACHE offers the following features:

- Multi-bus interface:
  - Slave port receiving the memory requests from the Cortex®-M33 C-AHB code execution port
  - Master1 port performing refill requests to internal flash and RAM memories.
  - Master2 port performing refill requests to external XSPI memories.
  - Second slave port dedicated to ICACHE register access
- Close to 0 wait-states instructions/data access performance:
  - 0 wait-state on cache hit
  - Hit-under-miss capability, making it possible to serve new processor requests while a line refill (due to a previous cache miss) is still ongoing
  - Critical-word-first refill policy, minimizing processor stalls on cache miss
  - Hit ratio improved by two-way set-associative architecture and pLRU-t replacement policy (pseudo-least-recently-used, based on binary tree), algorithm with best complexity/performance balance
  - Dual master ports to decouple internal memory and external memory traffic, on fast and slow buses, respectively; also minimizing impact on interrupt latency
  - Optimal cache line refill thanks to AHB burst transactions (of the cache line size)
  - Performance monitoring by means of a hit counter and a miss counter
- Extension of the cacheable region beyond the code memory space, by means of address-remapping logic, enabling the definition of four cacheable regions
- Power consumption reduced intrinsically (more access to cache memory than bigger main memories); further improved by configuring ICACHE as direct-mapped (rather than the default two-way set-associative mode)
- TrustZone® security support
- Maintenance operation for software management of cache coherency
- Error management: detection of unexpected cacheable write access, with optional interrupt raising

3.3 Memory protection unit

The MPU is used to manage the CPU access requests to the memory and to prevent one task from accidentally corrupting the memory or the resources used by other active tasks. This memory area is organized into up to 16 protected areas. The MPU regions and registers are banked across secure and nonsecure states.

The MPU is especially helpful for applications where some critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by a real-time operating system (RTOS). If a program accesses a memory location prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Multi-AHB bus matrix

A 32-bit multi-AHB bus matrix interconnects all masters (CPU, LPDMA1) and slave peripherals (flash memory, SRAMs, AHB, and APB). It also ensures seamless and efficient operation even when several peripherals work simultaneously.

3.5 Embedded flash memory

The devices feature 512 Kbytes of embedded flash memory, available to store programs and data. This memory supports 10 000 cycles.

A 64-bit instruction prefetch is implemented and can optionally be enabled.

The flash memory contains 128 pages of 4 Kbytes and embeds a 512-byte one time programmable (OTP) region for user data.

The configuration of flexible protections is possible thanks to the option bytes:

- Readout protection (RDP), used to protect the entire memory, has four levels of protection available (see *Table 3* and *Table 4*):
  - Level 0: no readout protection
  - Level 0.5: available only when TrustZone® is enabled

    All read/write operations (if no write protection is set) from/to the nonsecure flash memory are possible. Debug access to the secure area is prohibited but remains possible to the nonsecure area.
  - Level 1: memory readout protection

    The flash memory cannot be read from or written to if either the debug features are connected or the boot in SRAM or bootloader are selected. If TrustZone® is enabled, the nonsecure debug is possible and the boot in SRAM is not possible. Regressions from Level 1 to lower levels can be protected by password authentication.
  - Level 2: chip readout protection

    The debug features, the boot in RAM and the bootloader selection are disabled. A secure secret key can be configured in the secure options to allow the regression capability from Level 2 to Level 1. By default (key not configured), this Level 2 selection is irreversible and JTAG/SWD interfaces are disabled. If the secret key was previously configured in lower RDP levels, the device enables the RDP regression from Level 2 to Level 1 after password authentication through the JTAG/SWD interface.
- Write protection (WRP) to protect areas against erasing and programming. Two areas can be selected with a 4-Kbyte granularity.

Table 3. Access status versus protection level and execution modes when TZEN = 0

Area	RDP level	User execution (boot from flash memory)			Debug/boot from RAM/ bootloader(1)		
		Read	Write	Erase	Read	Write	Erase
Flash main memory	1	Yes	Yes	Yes	No	No	No(4)
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory (2)	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A
Option bytes(3)	1	Yes	Yes(4)	N/A	Yes	Yes(4)	N/A
	2	Yes	No	N/A	N/A	N/A	N/A
OTP	1	Yes	Yes(5)	N/A	Yes	Yes(5)	N/A
	2	Yes	Yes(5)	N/A	N/A	N/A	N/A
Backup registers	1	Yes	Yes	N/A	No	No	N/A(6)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	1	Yes	Yes	N/A	No	No	N/A(7)
	2	Yes	Yes	N/A	N/A	N/A	N/A
OTFDEC regions (Quad-SPI)	1	Yes	Yes	Yes	No(8)	Yes	Yes
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. When the protection level 2 is active, the debug port, the boot from RAM, and the boot from system memory are disabled.
2. The system memory is only read-accessible, whatever the protection level (0, 1 or 2) and execution mode.
3. Option bytes are accessible only through the flash memory interface registers and OPSTRT bit.
4. The flash main memory is erased when the RDP option byte changes from level 1 to level 0.
5. OTP can be written only once.
6. The backup registers are erased when RDP changes from level 1 to level 0.
7. All SRAMs are erased when RDP changes from level 1 to level 0.
8. The OTFDEC keys are erased when the RDP option byte changes from level 1 to level 0.

Table 4. Access status versus protection level and execution modes when TZEN = 1

Area	RDP level	User execution (boot from flash memory)			Debug/bootloader(1)		
		Read	Write	Erase	Read	Write	Erase
Flash main memory	0.5	Yes	Yes	Yes	Yes(2)	Yes(2)	Yes(2)
	1	Yes	Yes	Yes	No	No	No(5)
	2	Yes	Yes	Yes	N/A	N/A	N/A
System memory (3)	0.5	Yes	No	No	Yes	No	No
	1	Yes	No	No	Yes	No	No
	2	Yes	No	No	N/A	N/A	N/A

Table 4. Access status versus protection level and execution modes when TZEN = 1 (continued)

Area	RDP level	User execution (boot from flash memory)			Debug/bootloader(1)		
		Read	Write	Erase	Read	Write	Erase
Option bytes(4)	0.5	Yes	Yes(5)	N/A	Yes	Yes (5)	N/A
	1	Yes	Yes(5)	N/A	Yes	Yes(5)	N/A
	2	Yes	No	N/A	N/A	N/A	N/A
OTP	0.5	Yes	Yes(6)	N/A	Yes	Yes(6)	N/A
	1	Yes	Yes(6)	N/A	Yes	Yes(6)	N/A
	2	Yes	Yes(6)	N/A	N/A	N/A	N/A
Backup registers	0.5	Yes	Yes	N/A	Yes(2)	Yes(2)	N/A(7)
	1	Yes	Yes	N/A	No	No	N/A(7)
	2	Yes	Yes	N/A	N/A	N/A	N/A
SRAM2	0.5	Yes	Yes	N/A	Yes(2)	Yes(2)	N/A(8)
	1	Yes	Yes	N/A	No	No	N/A(8)
	2	Yes	Yes	N/A	N/A	N/A	N/A
OTFDEC regions (Quad-SPI)	0.5	Yes	Yes	Yes	No(9)	Yes	Yes
	1	Yes	Yes	Yes	No(9)	Yes	Yes
	2	Yes	Yes	Yes	N/A	N/A	N/A

1. When the protection level 2 is active, the debug port and the bootloader mode are disabled.
2. Depends on TrustZone security access rights.
3. The system memory is only read-accessible, whatever the protection level (0, 1 or 2) and execution mode.
4. Option bytes are only accessible through the flash registers interface and OPSTRT bit.
5. The flash main memory is erased when the RDP option byte regresses from level 1 to level 0.
6. OTP can be written only once.
7. The backup registers are erased when RDP changes from level 1 to level 0.5 or level 0.
8. All SRAMs are erased when RDP changes from level 1 to level 0.5 or level 0.
9. The OTFDEC keys are erased when the RDP option byte changes from level 1 to level 0.

The whole nonvolatile memory embeds the error correction code (ECC) feature, supporting:

- Single-error detection and correction
- Double-error detection
- ECC fail address report

3.5.1 Flash memory protections when TrustZone® is activated

When the TrustZone® security is enabled through the option bytes, the entire flash memory is secure after reset and the following protections are available:

- Nonvolatile watermark-based secure flash memory area

  The secure area can be accessed only in Secure mode. One area can be selected with a page granularity.
- Secure hide protection area (HDP)

  It is part of the flash memory secure area and can be protected to deny access to this area by any data read, write, and instruction fetch. For example, a software code in the secure flash memory hide protection area can be executed only once and deny any further access to this area until the next system reset. One area can be selected at the beginning of the secure area.
  The hide protection area can be extended (HDP extension).
- Volatile block-based secure flash memory area

  Each page can be programmed on the fly as secure or nonsecure.

3.5.2 FLASH privilege protection

Each flash memory page can be programmed on the fly as privileged or unprivileged.

3.6 Embedded SRAMs

SRAM1 and SRAM2 are the main SRAMs embedded in the STM32WBA2xxx devices, each with specific features. These memories can be used for peripherals background autonomous mode (BAM).

These SRAMs can be powered down in Stop mode to reduce consumption:

- SRAM1: one 64-Kbyte block, which can be retained in Standby mode
- SRAM2: one 24-Kbyte block and one 8-Kbyte block, both with parity, can be retained in Standby mode.

3.6.1 SRAMs TrustZone® security

When TrustZone® security is enabled, SRAMs are secure after reset. SRAM1 and SRAM2 can be programmed as secure or nonsecure by blocks, using the MPCBB (block-based memory protection controller).

The granularity of SRAM secure block based is a page of 512 bytes.

3.6.2 SRAMs privilege protection

The SRAM1 and SRAM2 can be programmed as privileged or nonprivileged by blocks, using the MPCBB. The granularity of SRAM block-based privilege is a page of 512 bytes.

3.7 Boot modes

At startup, a BOOT0 pin, as well as nBOOT0 and NSBOOTADDx[24:0] (x = 0, 1), and SECBOOTADD0[24:0] option bytes are used to select the boot memory address. This includes:

- Boot from any address in the user flash memory
- Boot from the system memory bootloader
- Boot from any address in the embedded SRAM
- Boot from RSS (root security services)

The BOOT0 value comes from the PH3-BOOT0 pin or from an option bit, depending on the value of a user option bit to free the GPIO pad if needed.

The bootloader is located in the system memory, programmed by ST during production. It is used to program the flash memory by using USART, I^2C, SPI, or USB in device mode through the DFU (device firmware upgrade).

The bootloader is available on all devices. Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606), available on *www.st.com*, for more details.

The RSS is embedded in the flash memory area named secure information block, programmed during ST production.

The RSS is available on all devices, after enabling the TrustZone through the TZEN option bit.

Refer to *Table 5* and *Table 6*, respectively, for boot modes with TrustZone® disabled and enabled.

Table 5. Boot modes when TrustZone® is disabled (TZEN = 0)

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot address option-bytes selection	Boot area	ST programmed default value
-	0	1	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash memory: 0x0800 000
-	1	1	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF8 5000
1	-	0	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash memory: 0x0800 0000
0	-	0	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF8 5000

When TrustZone® is enabled by setting the TZEN option bit, the boot space must be in the secure area. The SECBOOTADD0[24:0] option bytes are used to select the boot secure memory address.

A unique boot entry option can be selected by setting the BOOT_LOCK option bit, allowing to boot always at the address selected by the SECBOOTADD0[24:0] option bytes. All other boot options are ignored.

Table 6. Boot modes when TrustZone® is enabled (TZEN = 1)

BOOT_LOCK	nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	RSS command	Boot address option bytes selection	Boot area	ST programmed default value
0	-	0	1	0	SECBOOT-ADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000
	-	1	1	0	N/A	RSS	RSS: 0x0FF8 0000
	1	-	0	0	SECBOOT-ADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000
	0	-	0	0	N/A	RSS	RSS: 0x0FF8 0000
	-	-	-	≠0	N/A	RSS	RSS: 0x0FF8 0000
1	-	-	-	-	SECBOOT-ADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000

The boot address option bytes allow any boot memory address to be programmed. However, the allowed address space depends on the flash memory RDP level.

If the programmed boot memory address is out of the allowed memory mapped area when the RDP level is 0.5 or higher, the default boot address is forced either in secure or nonsecure flash memory, depending on the TrustZone® security option, as detailed in *Table 7*.

Table 7. Boot space versus RDP protection

RDP	TZEN = 1	TZEN = 0
0	Any boot address	Any boot address
0.5	Boot address only in RSS or secure flash memory: 0x0C00 0000 - 0x0C07 FFFF. Otherwise, forced boot address is 0x0FF8 0000	N/A
1		Any boot address
2		Boot address only in flash memory: 0x0800 0000 - 0x0807 FFFF. Otherwise, forced boot address is: 0x0800 0000

3.8 Global TrustZone® controller (GTZC)

GTZC is used to configure TrustZone® and privileged attributes within the full system.

The GTZC includes different subblocks:

- **TZSC**: TrustZone® security controller

  This subblock defines the secure/privilege state of slave/master peripherals. It also controls the nonsecure area size for the watermark memory peripheral control (MPCWM). The TZSC block informs some peripherals (such as RCC or GPIO) about the secure status of each securable peripheral.
- **TZIC**: TrustZone® illegal access controller

  This subblock gathers all security illegal access events in the system and generates a secure interrupt towards NVIC.
- **MPCBB**: block-based memory protection controller

  This subblock controls the secure states of all memory blocks (512-byte pages) of the associated SRAM. This peripheral configures the internal RAM in a TrustZone® system product having segmented SRAM with programmable-security and privileged attributes.

The GTZC main features are:

- Independent 32-bit AHB interfaces for TZSC, TZIC, and MPCBBs
- Secure and nonsecure access supported for privileged/unprivileged part of TZSC
- Set of registers to define product security settings:
  - Secure/privilege access mode for securable peripherals
  - Secure/privilege access mode for securable memories
  - Illegal access interrupt notification

3.9 TrustZone® security architecture

The security architecture is based on Arm® TrustZone® with the Armv8-M main extension.

The TZEN option bit in the FLASH_OPTR register activates the TrustZone® security.

When TrustZone® is enabled, the security attribution unit (SAU) and implementation defined attribution unit (IDAU) define the access permissions based on the secure and nonsecure state.

- SAU: up to eight SAU configurable regions are available for security attribution.
- IDAU: provides a first memory partition as nonsecure or nonsecure callable attributes. It is then combined with the results from the SAU security attribution and the higher security state is selected.

Based on the IDAU security attribution, the flash memory, system SRAM, and peripheral memory space are aliased twice for secure and nonsecure states.

Table 8 shows an example of typical SAU regions configuration based on IDAU regions.

Table 8. Example of memory map security attribution versus SAU configuration regions

Region description	Address range	IDAU security attribution	SAU security attribution typical configuration	Final security attribution
Reserved	0x0000 0000 0x07FF FFFF	Nonsecure	Secure or nonsecure or nonsecure callable	
Code flash memory and SRAM	0x0800 0000 0x0BFF FFFF	Nonsecure		
	0x0C00 0000 0x0FFF FFFF	Nonsecure callable	Secure or nonsecure callable	
Reserved	0x1000 0000 0x17FF FFFF	Nonsecure	Nonsecure	
	0x1800 0000 0x1FFF FFFF			
SRAM	0x2000 0000 0x2FFF FFFF	Nonsecure		
	0x3000_0000 0x3FFF FFFF	Nonsecure callable	Secure or nonsecure callable	
Peripherals	0x4000 0000 0x4FFF FFFF	Nonsecure		
	0x5000 0000 0x5FFF FFFF	Nonsecure callable	Secure or nonsecure callable	
External memories	0x6000 0000 0xDFFF FFFF	Nonsecure	Secure or nonsecure or nonsecure callable	

3.9.1 TrustZone® peripheral classification

When the TrustZone® security is active, a peripheral can be either the securable or TrustZone®-aware type as follows:

- Securable: peripheral protected by an AHB/APB firewall gate controlled from TZSC to define security properties.
- TrustZone®-aware: peripheral connected directly to the AHB or APB bus and implementing specific TrustZone® behavior, such as a subset of registers being secure.

3.9.2 Default TrustZone® security state

The default system security state is detailed below:

- CPU: Cortex®-M33 is in secure state after reset. The boot address must be in the secure area.
- Memory map: SAU is fully secure after reset. Consequently, the entire memory map is fully secure. Up to eight SAU configurable regions are available for security attribution.
- Flash memory:
  - The flash memory security area is defined by watermark user options.
  - The flash memory block based area is nonsecure after reset.

- SRAMs: All are secure after reset, MPCBB is secure.
- Peripherals
  - Securable peripherals are nonsecure after reset.
  - TrustZone®-aware peripherals are nonsecure after reset.
- All GPIOs are secure after reset.
- External memories:
  - Quad-SPI banks are secure after reset. MPCWM (memory protection watermark based controller) is secure.
- Interrupts (NVIC): all interrupts are secure after reset. NVIC is banked for secure and nonsecure state.
- TZIC: all illegal access interrupts are disabled after reset.

3.10 2.4 GHz RADIO

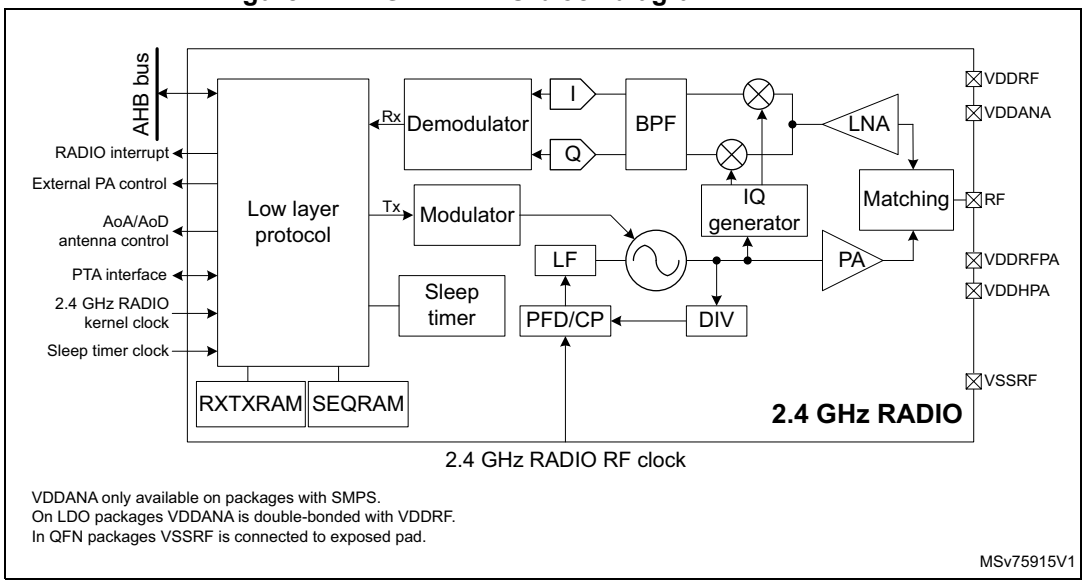
The 2.4 GHz RADIO is ultra-low-power, operating in the 2.4 GHz ISM band. It provides Bluetooth® LE 1 Mbps coded, 1 Mbps and 2 Mbps non-coded GFSK, and IEEE802.15.4 chip rate 2 Mchip/s, spreading mode DSSS, data rate 125 kbps and 250 kbps, and O-QPSK-C modulation. It is compliant with the Bluetooth 6.0, Zigbee®, and Thread® specifications and radio regulations including ETSI EN 300 328, EN 300 440, EN 301 489-17, ARIB STD-T66, FCC CFR47 part 15 section 15.205, 15.209, 15.247 and 15.249, IC RSS-139, and RSS-210.

The 2.4 GHz RADIO supports the following features:

- Radio protocol:
  - Bluetooth® LE
  - IEEE802.15.4
- Bluetooth® LE:
  - Data rate 1 Mbps, 2 Mbps, 500 kbps, and 125 kbps
  - Device privacy and network privacy mode
  - Anonymous device address
  - Advertising extension PDUs
  - Advertising channel index
  - Periodic advertising synchronous transfer
  - High-duty cycle, nonconnectable advertising
  - Angle-of-arrival (AoA)/angle-of-departure (AoD)
  - Audio connected isochronous streams
  - Audio broadcast isochronous streams
  - Candidated for Bluetooth® Core 6.0 qualification.

- IEE802.15.4 features:
  - Beacon management
  - 16-bit short and 64-bit IEEE addressing mode
  - PAN formation along with association and disassociation
  - Full handshake protocol for transfer reliability, frame validation, and acknowledgment frame delivery
  - IEEE802.15.4 2020 MAC for non-beaconed PANs
- Matter coprocessor operation
- Thread®
- Zigbee®
- External PA support
- Packet traffic arbitration

Figure 2. 2.4 GHz RADIO block diagram



VDDANA only available on packages with SMPS.
On LDO packages VDDANA is double-bonded with VDDRF.
In QFN packages VSSRF is connected to exposed pad.

MSv75915V1

3.11 PTA interface

The PTA interface enables packet traffic arbitration with other connectivity devices, such as WiFi.

PTA main features:

- Based on IEEE802.15.4 standard
- Supports both grant and deny signaling
- Supports from 1- to 4-wire protocols
- Programmable transmit receive PTA_STATUS polarity
- Programmable priority polarity
- Programmable grant polarity
- Programmable active polarity
- Programmable PTA_ACTIVE timing
- Programmable PTA_STATUS time multiplexed priority timing.
- Programmable transmit packet abort

3.12 Power supply management

The power controller (PWR) main features are:

- Power supplies and supply domains
  - Core domain (V_{CORE})
  - V_{DD} and backup domain
  - Analog domain (V_{DDA})
  - SMPS power stage (V_{DDSMPS}, available only on SMPS packages)
  - V_{DDUSB} for USB transceiver
  - V_{DDRF} for 2.4 GHz RADIO
- System supply voltage regulation
  - SMPS step-down converter
  - Voltage regulator (LDO)
- Power supply supervision
  - BOR monitor
  - PVD monitor
- Power management
  - Operating modes
  - Voltage scaling control
  - Low-power modes
- TrustZone® security and privilege protection

3.12.1 Power supply schemes

The devices require a 1.71 to 3.6 V V_{DD} operating voltage supply. Several independent supplies can be provided for specific peripherals:

- V_{DD} = 1.71 to 3.6 V (functionality guaranteed down to V_{BORx} minimum value)

  V_{DD} is the external power supply for the I/Os, the internal regulator, the system analog such as reset, power management, and internal clocks and the backup domain. It is provided externally through the VDD pins. VDDRF must be connected to the same supply used for VDD.
- V_{DDUSB} = 3.0 to 3.6 V

  V_{DDUSB} is the external independent power supply for the USB transceiver. The V_{DDUSB} voltage level is independent from the V_{DD} voltage and must be connected to the VDD (preferably) or VSS pin when this peripheral is not used.
- V_{DDA} = 1.62 to 3.6 V

  V_{DDA} is the external analog power supply for ADC. The V_{DDA} voltage level is independent from the V_{DD} voltage and must be connected to the VDD (preferably) or VSS pin when this peripheral is not used.
- V_{DDSMPS} = 1.71 to 3.6 V

  V_{DDSMPS} is the external power supply for the SMPS step down converter. It is provided externally through the VDDSMPS supply pin and must be connected to the same supply as V_{DD}.
- V_{LXSMPS} is the switched SMPS step-down converter output.

Note: The SMPS power supply pins are available only on packages with the SMPS step-down converter option.

- V_{DDRF} = 1.71 to 3.6 V

  V_{DDRF} is the external power supply for the 2.4 GHz RADIO; it must be connected to the same supply used for VDD.
- V_{DDANA} = 0 to 3.6 V (needs to be ≥ 1.2 V for 2.4 GHz RADIO operation)

  V_{DDANA} is an external power supply for the 2.4 GHz RADIO; it can be connected to V_{DD11}.
- V_{DDRFPA} = 0 to 3.6 V (must be ≥ 1.2 V for 2.4 GHz RADIO operation)

  V_{DDRFPA} is an external power supply for the 2.4 GHz RADIO and power amplifier regulator, it can be connected to V_{DD11}. The maximum reachable transmit output power is determined by the V_{DDRFPA} supply level.

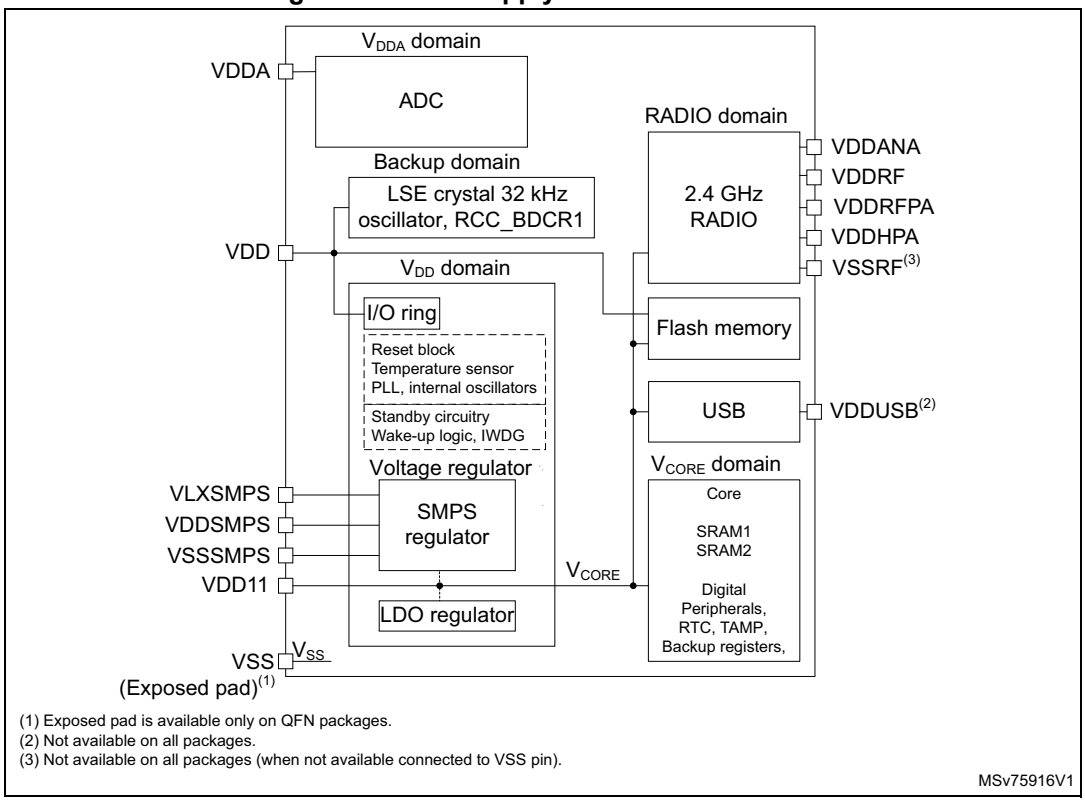
The devices embed two regulators: one LDO and one SMPS in parallel to provide the V_{CORE} supply for digital peripherals, SRAM1, SRAM2, 2.4 GHz RADIO, and embedded flash memory. The LDO generates this voltage on VCAP pin connected to an external capacitor of 4.7 µF (typical). The SMPS generates this voltage on VDD11 pin, with a total external capacitor of 4.7 µF (typical). The SMPS requires an external coil of 2.2 µH (typical).

Both regulators can provide two different voltages (voltage scaling) and can operate in Stop modes.

On-the-fly switching from SMPS to LDO and from LDO to SMPS is possible.

The VDDHPA pin is provided to connect to an external capacitor (typical value 470 nF).

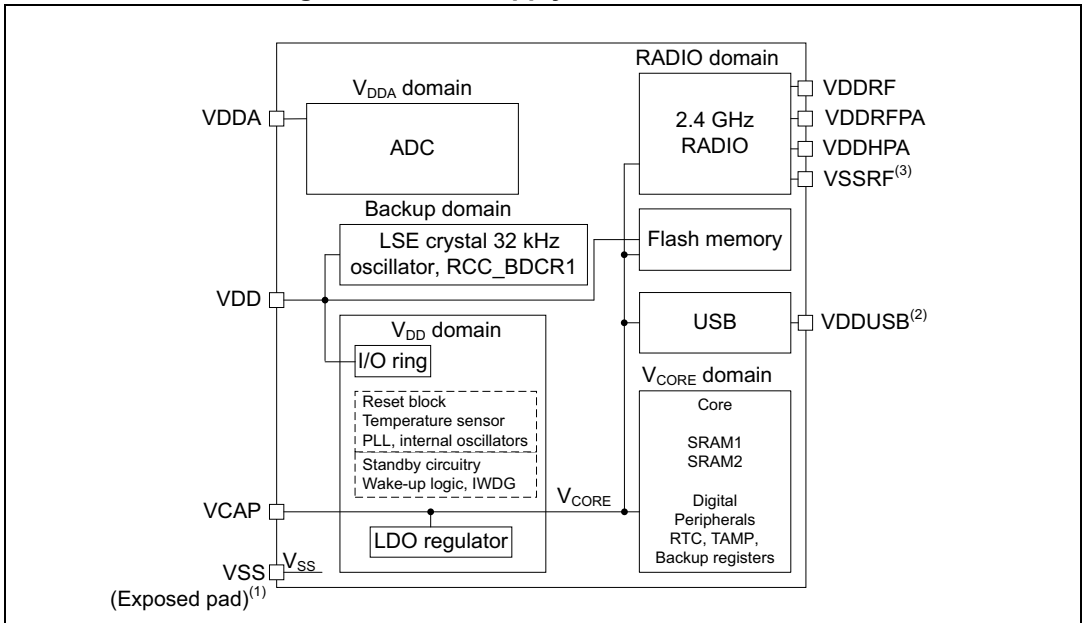
Figure 3. Power supply overview with SMPS



(1) Exposed pad is available only on QFN packages.
(2) Not available on all packages.
(3) Not available on all packages (when not available connected to VSS pin).

MSv75916V1

Figure 4. Power supply overview with LDO



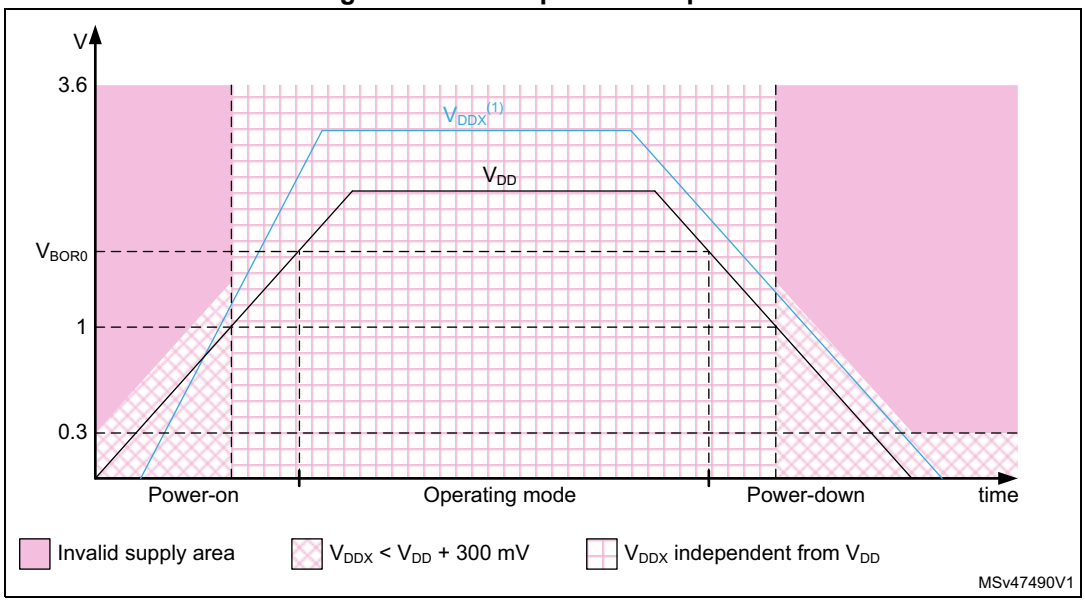
(1) Exposed pad is available only on QFN packages.
(2) Not available on all packages.
(3) Not available on all packages (when not available connected to VSS pin).

MSv75917V1

During power-up and power-down phases, respect the following requirements:

- When V_{DD} is below 1 V, other power supplies (namely V_{DDA}, V_{DDUSB}) must remain below V_{DD} + 300 mV.
- When V_{DD} is equal to or above 1 V, other power supplies are independent.
- During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

Figure 5. Power-up /down sequence



1. V_{DDX} refers to power supply V_{DDA} and V_{DDUSB}.

3.12.2 Power supply supervisor

The devices have an integrated ultra-low-power BOR (brownout reset) active in all modes. The BOR ensures proper operation after power-on and during power-down. The devices remain in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71 V at power-on, and other higher thresholds can be selected through option bytes.The devices feature an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold.

An interrupt can be generated when V_{DD} drops below and/or rises above the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

The devices support dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the main regulator that supplies the logic (V_{CORE}) can be adjusted according to the system's maximum operating frequency.

The main regulator operates in the following ranges:

- Range 1 (V_{CORE} = 1.2 V) with CPU and peripherals running at up to 64 MHz
- Range 1.5 (V_{CORE} = 1.1 V) with CPU and peripherals running at up to 64 MHz
- Range 2 (V_{CORE} = 0.9 V) with CPU and peripherals running at up to 16 MHz

Low-power modes

The devices support different low-power modes to achieve the best compromise between low-power consumption, startup time, available peripherals, and available wake-up sources.

Table 9 on the following pages shows an overview of the different operating modes.

Table 9. Operating modes overview

Mode	Regulator[1]	CPU	Flash memory	SRAM	Clocks	DMA and peripherals[2]	Wake-up source
Run	Range 1	Yes	ON[3]	ON	Any	All	N/A
	Range 1.5						
	Range 2					All except 2.4 GHz RADIO	
Sleep	Range 1	No	ON	ON[4]	Any	All	Any interrupt or event
	Range 1.5						
	Range 2					All except 2.4 GHz RADIO	
Stop 0	Range 1 and Range 1.5	No	OFF	ON[5]	LSE LSI [6]	BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4[7] (temperature sensor), USART1[8], LPUART1, SPI3[9], I2Cx (x = 1, 3)[10], LPTIMx (x = 1, 2)[11], USB (suspend) GPIO, LPDMA1[12], 2.4 GHz RADIO All other peripherals are frozen.	Reset pin, all I/Os, BOR, PVD, RTC, TAMP, IWDG, WKUP, SLEEP_TIMER, ADC4 (temperature sensor), USART1, LPUART1, SPI3, I2Cx (x = 1, 3), LPTIMx (x = 1, 2), USB LPDMA1, 2.4 GHz RADIO
	Range 2					All from Stop 0 Range 1 except 2.4 GHz RADIO	
Stop 1[13]	LPR	No	OFF	ON[5]	LSE LSI	BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4 (temperature sensor), USART1, LPUART1, SPI3, I2Cx (x = 1, 3), LPTIMx (x = 1, 2), GPIO All other peripherals are frozen.	Reset pin, all I/Os, BOR, PVD, RTC, TAMP, IWDG, WKUP, SLEEP_TIMER, ADC4 (temperature sensor), USART1, LPUART1, SPI3, I2Cx (x = 1, 3), LPTIMx (x = 1, 2)

Table 9. Operating modes overview (continued)

Mode	Regulator[1]	CPU	Flash memory	SRAM	Clocks	DMA and peripherals[2]	Wake-up source
Stop 2[13]	LPR	No	OFF	ON[5]	LSE LSI	BOR, PVD, RTC, TAMP, IWDG, SLEEP_TIMER, ADC4 and temperature sensor), LPUART1, SPI3, I2C3, LPTIM1, GPIO All other peripherals powered down.	Reset pin, all I/Os, BOR, PVD, RTC, TAMP, IWDG, WKUP, SLEEP_TIMER, ADC4 and temperature sensor, LPUART1, SPI3, I2C3, LPTIM1
Stop 3	LPR	No	OFF	ON[5]	LSE LSI	BOR, PVD, GPIO IWDG Other Stop 2 peripherals are frozen. All other peripherals powered down.	WKUP IWDG
Standby retention	LPR	Powered off	OFF	ON[5]	LSE LSI	BOR, RTC, TAMP, IWDG, SLEEP_TIMER All other peripherals are powered off. I/O configuration can be retained, floating, pull-up or pull-down.	Reset pin, BOR, RTC, TAMP, IWDG, WKUP, SLEEP_TIMER
Standby	OFF			OFF		BOR, IWDG All other peripherals are powered off. I/O configuration can be retained, floating, pull-up or pull-down.	Reset pin, BOR, IWDG, WKUPR

1. LPR means that the main regulator is OFF and the low-power regulator is ON.
2. All peripherals can be active or clock gated to save power consumption.
3. The flash memory can be put in power-down and its clock can be gated off when executing from SRAM.
4. The SRAM1 and SRAM2 clocks can be gated on or off independently.
5. The SRAM can be individually powered off to save power consumption.
6. HSI16 can be temporary enabled upon peripheral request, for autonomous functions with DMA or wake-up from Stop event detections.
7. The ADC conversion is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on conversion events.

8. U(S)ART and LPUART transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
9. SPI transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
10. I2C transmission and reception is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on transfer events.
11. LPTIM is functional and autonomous with DMA in Stop 0 mode, and can generate a wake-up interrupt on all events.
12. LPDMA is functional and autonomous in Stop 0 mode, and can generate a wake-up interrupt on events.
13. Active peripherals ADC, U(S)ART, LPUART, SPI, I2C and LPTIM, can generate bus clock request and/or a wake-up interrupt on event.

By default, the microcontroller is in Run mode after a system or power-on reset. It is up to the user to select one of the low-power modes described below:

- **Sleep**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt or event occurs.

- **Stop 0 and Stop 1**

  Stop modes achieves the lowest power consumption while retaining the content of registers. The SRAM content can be selected to be retained or not. All clocks (except some autonomous peripherals bus and kernel clocks) in the core domain are stopped. The PLL1 and HSE32 crystal oscillator are disabled. The HSI16 RC oscillator is disabled when not activated as the autonomous peripheral bus or kernel clock. The LSE or LSI can also still run.

  Some peripherals are autonomous and can operate in Stop modes by requesting their kernel clock and in Stop 0 mode also when requesting their bus clock when needed. When a peripheral request its (APB or AHB) bus clock, that is, in order to transfer data with LPDMA1, the device transitions from Stop 1 to Stop 0 mode. Refer to *Background autonomous mode (BAM)* for more details.

  The I2C, USART, LPUART, SPI, LPTIM, ADC, RTC, TAMP, and IWDG can remain active in Stop modes when the kernel clock is LSE, LSI, or HSI16. The 2.4 GHz RADIO can remain active in Stop 0 mode on its kernel clock HSE32. In Stop 0 mode the autonomous peripheral bus clock can remain active using HSI16.

  The brownout reset (BOR) always remains active and the PVD can be kept active in Stop modes. In Stop 1 mode the BOR0 can be configured in ultra-low-power mode to further reduce power consumption.

  In Stop 0 mode, the regulator remains in main regulator mode, allowing a very fast wakeup time but with much higher consumption than Stop 1.

  The system clock when exiting from Stop mode is HSI16 at 16 MHz.

- **Stop 2**

  Stop 2 mode achieves lower power consumption while retaining some peripherals and the system configuration registers content. The SRAM content can be selected to be retained or not. All clocks (except some autonomous peripherals kernel clocks) in the core domain are stopped. The PLL and HSE32 crystal oscillator are disabled. The HSI16 RC oscillator is disabled when not activated as the autonomous peripheral kernel clock. The LSE or LSI can still run.

  Some peripherals are autonomous and can operate in Stop 2 mode by requesting their kernel clock when needed.

  The I2C3, LPUART1, SPI3, LPTIM1, RTC, TAMP, IWDG can remain active in Stop 2 mode when the kernel clock is LSE, LSI, or HSI16.

  The brownout reset (BOR) always remains active and the PVD can be kept active in Stop 2 mode. The BOR0 can be configured in ultra-low-power mode to further reduce power consumption.

  The system clock when exiting from Stop mode is HSI16 at 16 MHz.

- **Stop 3**

  Stop 3 mode achieves the lowest power consumption while retaining some peripherals and the system configuration registers content. The SRAM content can be selected to be retained or not. All clocks in the core domain are stopped. The PLL, HSI16, and HSE32 crystal oscillator are disabled. The LSE or LSI can still run.

  The IWDG can remain active in Stop 3 mode.

The brownout reset (BOR) always remains active and the PVD can be kept active in Stop 3 mode. The BOR0 can be configured in ultra-low-power mode to further reduce power consumption.

The system clock when exiting from Stop mode is HSI16 at 16 MHz.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal regulator is switched off so the core domain is powered off. The PLL1, HSI16 RC, and HSE32 crystal oscillators are also switched off. The LSE or LSI can still run.

  The IWDG can remain active in Standby mode.

  The BOR always remains active in Standby mode. The BOR can be configured in ultra-low-power mode to further reduce power consumption during standby mode. The state of each I/O during Standby mode can be selected by software: I/O with internal pull-up, internal pull-down or floating.

  When entering Standby mode, register contents are lost except for registers in the backup domain VDD and Standby circuitry.

  The device exits Standby mode in the event of an NRST pin external reset, an IWDG early interrupt or reset, or a WKUP pin event (configurable rising or falling edge), and from Standby retention mode when an RTC event occurs (alarm, periodic wakeup, timestamp), a TAMP tamper detection, or a 2.4 GHz RADIO sleep timer event. The tamper detection can be raised either due to external pins or due to an internal failure detection.

  The system clock after wakeup is HSI16 at 16 MHz.

  Standby retention mode

  Optionally SRAMs can be retained in Standby mode, supplied by the regulator.

  Optionally the RTC and TAMPER can remain active when the kernel clock is LSE or LSI, supplied by the regulator.

  Optionally, the 2.4 GHz RADIO sleep timer, RXTXRAM and sequence SRAM can be retained in Standby mode, supplied by the regulator.

Background autonomous mode (BAM)

The devices support BAM (background autonomous mode), that allows peripherals to be functional and autonomous in Stop mode (Stop 0 and Stop 1 modes), without any software running.

In Stop 0 mode, the autonomous peripherals are the following: ADC4, LPTIMx (x = 1, 2), U(S)ART1, LPUART1, SPI3, I2Cx (x = 1, 3), 2.4 GHz RADIO, and LPDMA1. In this mode, the LPDMA1 can be used to transfer data or control peripherals and access SRAM1 and SRAM2. The ADC4 can also be used to measure temperature. The 2.4 GHz RADIO is autonomous only in Stop 0 range 1.

In Stop 1 mode, the autonomous peripherals are the following: ADC4, LPTIMx (x = 1, 2), U(S)ART1, LPUART1, SPI3, I2Cx (x = 1, 3). These peripherals can request a transition to Stop 0 mode allowing then data transfers with LPDMA1.

Those peripherals support the features detailed below:

- Functionality in Stop mode thanks to its own independent clock (named kernel clock) request capability: the peripheral kernel clock is automatically switched on when

requested by a peripheral, and automatically switched off when no peripheral requests it.

- DMA transfers supported in Stop 0 mode thanks to the system clock request capability: the system clock (HSI16) is automatically switched on when requested by a peripheral, and automatically switched off when no peripheral requests it. When the system clock is requested by an autonomous peripheral, Stop 0 mode is automatically entered and the system clock is woken up and distributed to all peripherals enabled in the RCC. This allows the DMA to access the enabled SRAM, and any enabled peripheral register (for instance, GPIO registers). When no peripheral requests its bus clock Stop 1 mode is automatically re-entered when Stop 1 mode is selected as the low-power mode.
- Automatic start of the peripheral thanks to hardware synchronous or asynchronous triggers (such as I/Os edge detection and low-power timer event).
- Wake-up from Stop mode with peripheral interrupt.

The LPDMA is fully functional and the linked-list is updated in Stop 0 mode, allowing the different DMA transfers to be linked without any CPU wake-up. This can be used to chain different peripheral transfers, or to write in peripheral registers to change their configuration while remaining in Stop 0 mode.

The DMA transfers from memory to memory can be started by hardware synchronous or asynchronous triggers, and the DMA transfers between peripherals and memories can also be gated by those triggers.

Below are listed some use-cases that can be done while remaining in Stop mode:

- A/D conversion triggered by a low-power timer (or any other trigger)
  - Wake-up from Stop mode on analog watchdog if the A/D conversion result is outside of the programmed thresholds
  - Wake-up from Stop mode on DMA buffer event
- I^2C slave reception or transmission, SPI reception, USART/LPUART reception
  - Wake-up at the end of peripheral transfer or on DMA buffer event
- I^2C master transfer, SPI transmission, USART/LPUART transmission, triggered by a low-power timer (or any other trigger):
  - Example: sensor periodic read
  - Wake-up at the end of peripheral transfer or on DMA buffer event
- Bridges between peripherals
  - Example: ADC converted data transferred by communication peripherals
- Data transfer from/to GPIO to/from SRAM for:
  - Controlling external components
  - Implementing data transmission and reception protocols

Table 10. Functionalities depending on the working mode[1]

Peripheral	Run/ Sleep		Stop 0			Stop 1		Stop 2		Stop 3		Standby retention		Standby	
	Range 1 or 1.5	Range 2	Range 1 or 1.5	Range 2	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability
CPU	A		R		-	R	-	R	-	R	-	-	-	-	-
ICACHE	A		R		-	R	-	R	-	R	-	-	-	-	-
Flash memory	O[2]		R		-	R	-	R	-	R	-	R	-	R	-
SRAM1	A		O		-	O	-	O	-	O	-	O	-	-	-
SRAM2	A		O		Y	O	-	O	-	O	-	O	-	-	-
RAMCFG	O		O		Y	R	-	R	-	R	-	-	-	-	-
SYSCFG	O		O		-	R	-	R	-	R	-	-	-	-	-
XSPI1	O		R		-	R	-	-	-	-	-	-	-	-	-
DLYBXS1	O		R		-	R	-	-	-	-	-	-	-	-	-
OTFDEC1	O		R		-	R	-	-	-	-	-	-	-	-	-
Backup registers	A		R		-	R	-	R	-	R	-	R	-	-	-
2.4 GHz RADIO	O	R	O	R	Y	R	-	-	-	-	-	-	-	-	-
2.4 GHz RADIO SRAM	O	R	O	R	-	R	-	R	-	R	-	O	-	-	-
2.4 GHz RADIO Sleep timer	O	O	O	O	Y	O	Y	O	Y	R	-	O	Y	-	-
BOR	A		A		Y	A	Y	A	Y	A	Y	A	Y	A	Y
PVD	O		O		Y	O	Y	O	Y	O	Y	-	-	-	-
HSI16 clock	O		O[3]		-	O[3]	-	O[3]	-	-	-	-	-	-	-
HSE32 clock	O		O[4]	-	-	-	-	-	-	-	-	-	-	-	-
LSI clock	O		O		-	O	-	O	-	O	-	O	-	O	-
LSE clock	O		O		-	O	-	O	-	O	-	O	-	O	-
CSSHSE clock security	O		O	-	Y	-	-	-	-	-	-	-	-	-	-
CSSLSE clock security	O		O		Y	O	Y	O	Y	R	-	O	Y	-	-
RTC	O		O		Y	O	Y	O	Y	R	-	O	Y	-	-
TAMP	O		O		Y	O	Y	O	Y	R	-	O	Y	-	-
GPIO	O		R[5]		Y[6]	R[5]	Y[6]	R[5][7]	Y[6]	R[5][7]	Y[6]	R[8]	Y[9]	R[8]	Y[9]
IWDG	O		O		Y	O	Y	O	Y	O	Y	O	Y	O	Y
LPDMA1	O		O		Y	R	-	-	-	-	-	-	-	-	-
USART1	O		O		Y	O	Y	-	-	-	-	-	-	-	-

Table 10. Functionalities depending on the working mode(1) (continued)

Peripheral	Run/ Sleep		Stop 0			Stop 1		Stop 2		Stop 3		Standby retention		Standby	
	Range 1 or 1.5	Range 2	Range 1 or 1.5	Range 2	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability
LPUART1	O		O		Y	O	Y	O	Y	R	-	-	-	-	-
I2C1	O		O		Y	O	Y	-	-	-	-	-	-	-	-
I2C3	O		O		Y	O	Y	O	Y	R	-	-	-	-	-
SPI3	O		O		Y	O	Y	O	Y	R	-	-	-	-	-
USB	O	R	O	R	Y	R	-	-	-	-	-	-	-	-	-
ADC4	O		O		Y	O	Y	-	-	-	-	-	-	-	-
Temperature sensor	O		O(10)		Y(10)	O(10)	Y(10)	-	-	-	-	-	-	-	-
LPTIM1	O		O		Y	O	Y	O	Y	R	-	-	-	-	-
LPTIM2	O		O		Y	O	Y	-	-	-	-	-	-	-	-
PTACONV(12)	O		R		-	R	-	-(7)	-	-(7)	-	-	-	-	-
TIMx (x = 2, 16, 17)	O		R		-	R	-	-	-	-	-	-	-	-	-
SAI1	O		R		-	R	-	-	-	-	-	-	-	-	-
RNG	O		R		-	R	-	-	-	-	-	-	-	-	-
AES	O		R		-	R	-	-	-	-	-	-	-	-	-
HASH	O		R		-	R	-	-	-	-	-	-	-	-	-
PKA	O		R		-	R	-	-	-	-	-	-	-	-	-
CRC	O		R		-	R	-	-	-	-	-	-	-	-	-
GTZC1_TZSC-(MPCWM1)	O		R		-	R	-	R	-	R	-	-	-	-	-
GTZC1_TZIC	O		R		-	R	-	R	-	R	-	-	-	-	-
GTZC1_MPCBB1	O		R		-	R	-	R	-	R	-	-	-	-	-
GTZC1_MPCBB2	O		R		-	R	-	R	-	R	-	-	-	-	-
SysTick timer	O		R		-	R	-	-	-	-	-	-	-	-	-
Debug	O		O(11)		-	O(11)	-	O(11)	-	O(11)	-	O(12)	-	O(12)	-

1. A = Active, Y = yes. O = optional (can be enabled/disabled by software).R = Retained, - = not available. Gray cells highlight the wakeup capability in each mode.
2. The Flash memory can be configured in power-down mode.
3. Some peripherals with autonomous mode and wakeup from Stop capability can request HSI16 to be enabled. In this case, the oscillator is woken up by the peripheral, and is automatically put off when no peripheral needs it.
4. For the autonomous 2.4 GHz RADIO the HSE32 can be kept running.
5. GPIO pins from peripherals supporting autonomous mode are still operational.

6. Only GPIOs with enabled wakeup functionality in the EXTI or WKUP are able to wakeup the system.
7. GPIO level retention from PTA interface in Stop 2 and Stop 3 mode can be enabled.
8. GPIO level retention in Standby modes can be enabled.
9. Only GPIOs with WKUP functionality are able to wakeup the system.
10. Functional through ADC4 in autonomous mode.
11. DBGMCU remains accessible trough AP0.
12. DBGMCU remains accessible through AP0 when CDBGPWRUPREQ is set.

3.12.3 Reset mode

To improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O Schmitt trigger is disabled). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.12.4 PWR TrustZone security

When TrustZone security is activated by the TZEN option bit, the PWR is switched in TrustZone security mode.

The PWR TrustZone® security secures the following configuration:

- Low-power mode
- WKUP (wake-up) pins
- Voltage detection
- Backup domain control

Some of the PWR configuration bits security is defined by the security of other peripherals:

- The VOS (voltage scaling) configuration is secure when the system clock selection is secure in RCC.
- The I/O Standby mode retention configuration is secure when the corresponding GPIO is secure.

3.13 Reset and clock controller (RCC)

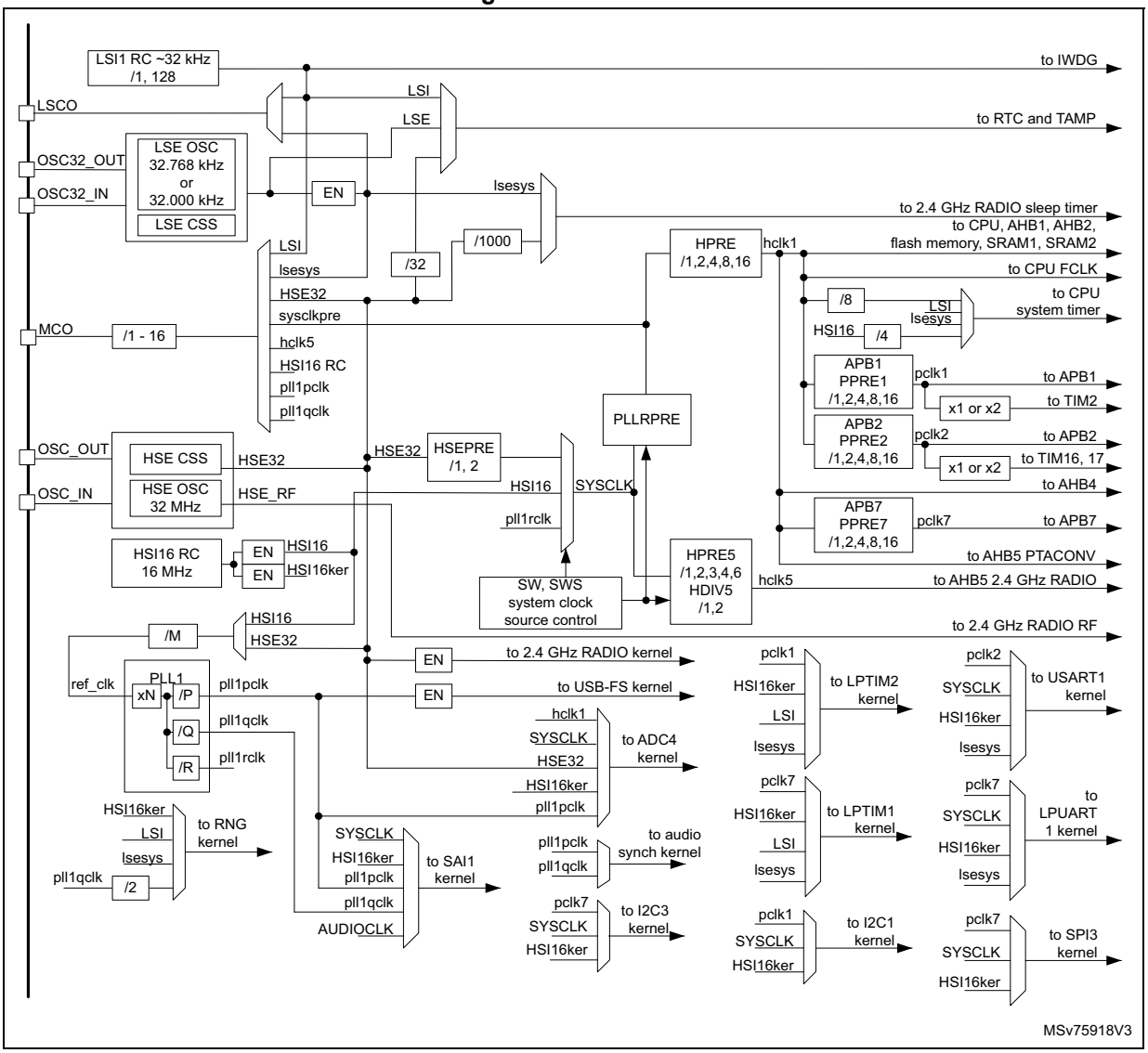
The RCC (reset and clock controller) manages the device and peripheral reset and distributes the clocks coming from the different oscillators to the core and to the peripherals. It also manages the clock gating for low-power modes and ensures clock robustness. It features:

- Device reset source monitoring.
- Individual peripheral reset control.
- Clock prescaler: to get the best trade-off between speed and current consumption, the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler.
- Clock selection system: clock sources can be changed safely on the fly in Run mode through a configuration register.
- Clock management: to reduce the power consumption, the clock controller can stop the clock to the core, individual peripherals, or memory.
- System clock source: different clock sources can be used to drive the system clock (SYSCLK):

  - HSE32 (32 MHz high-speed external crystal oscillator), trimmable by software. The HSE32 can also be used with an external clock.
  - HSI16 (16 MHz high-speed internal RC oscillator), trimmable by software.
  - System PLL that can be fed by HSE32 or HSI16 with a maximum output frequency at 64 MHz.
- Auxiliary clock source: two ultra-low-power clock sources that can be used to drive, for instance the real-time clock:
  - LSE (32.000 kHz or 32.768 kHz low-speed external crystal oscillator), supporting programmable drive capability modes. The LSE can also be configured in bypass mode for an external clock.
  - LSI (32 kHz low-speed internal RC oscillators), also used to drive the independent watchdog. The LSI1 clock absolute accuracy is ±5%, it can be divided by 128 to output a 250 Hz as the source clock.
- Peripheral clock sources: several peripherals have their own independent kernel clock whatever the system clock. The PLL has three independent outputs allowing the highest flexibility and can generate clocks for the ADC, SAI and audio, USB, and the RNG.
- Startup clock: after reset, the microcontroller restarts by default with the HSI16. The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- Clock security systems (CSS): these features can be enabled by software.
  - If an HSE32 clock failure occurs, the system clock automatically switches to HSI16 and a software interrupt is generated if enabled.
  - LSE failure can also be detected and generates an interrupt, in which case the clock switches to LSI.
- Clock-out capability:
  - MCO (microcontroller clock output): outputs one of the internal clocks for external use by the application (only available in Run, Sleep and Stop mode).
  - LSCO (low-speed clock output): outputs LSI or LSE in all operating modes.

Several prescalers allow AHB and APB frequency configuration. The maximum frequency of the AHB and the APB clock domains is 64 MHz, except for the AHB5 2.4 GHz RADIO domain, which is limited to 32 MHz.

Figure 6. Clock tree



3.13.1 RCC TrustZone® security

When the TrustZone® security is activated by the TZEN option bit, the RCC is switched in TrustZone security mode.

The RCC TrustZone® security secures some RCC system configuration and peripheral configurations from being read or modified by nonsecure access operations: when a peripheral is secure, the related peripheral clock, reset, clock source selection, and clock enable during low-power modes control bits are secure.

A peripheral is in secure state:

- For securable peripherals, when the corresponding SEC security bit is set in the TZSC (TrustZone® security controller).
- For TrustZone®-aware peripherals, when a security feature of the peripheral is enabled through dedicated peripheral bits.

3.14 General-purpose input/output (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down), or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/Os alternate function configuration can be locked, if needed, following a specific sequence in order to avoid spurious writing to the I/Os registers.

The GPIO allows dynamic I/O control in Stop 0 mode thanks to LPDMA1. All I/Os can be configured and controlled as input or output (open-drain or push-pull depending on GPIO configuration).

When enabled in the PWR, latest I/Os output level can be retained by pulling the I/Os high or low before entering Standby mode. I/O levels are retained after exit from Standby mode, until they are reconfigured by software.

3.14.1 GPIO TrustZone® security

Each I/O pin of a GPIO port can be individually configured as secure. When the selected I/O pin is configured as secure, its corresponding configuration bits for alternate function, mode selection, I/O data are secure against nonsecure access. The associated registers bit access is restricted to secure software only. After reset, all GPIO ports are secure.

3.15 System configuration controller (SYSCFG)

The main tasks of the SYSCFG (system configuration controller) are the following:

- Managing latency
- Managing robustness features
- Configuring FPU interrupts
- Enabling/disabling the I^2C fast-mode plus high-drive mode of some I/Os and booster for I/Os analog switches
- Managing the I/O compensation
- Providing memory erase status
- Communication channel with the RSS

3.15.1 SYSCFG TrustZone® security

When TrustZone® security is activated by the TZEN option bit, the SYSCFG is switched to TrustZone® security mode.

The SYSCFG TrustZone® security secures the following configuration:

- FPU interrupt configuration
- Robustness features
- I/O compensation and memory erase status

Some of the SYSCFG configuration bits security is defined by the security of other peripherals:

- The FMP high-drive mode of some I/Os configuration is secure when the corresponding GPIO is secure.
- The booster for I/Os analog switches configuration is secure when the ADC4 is secure.

3.16 Peripheral interconnect matrix

Several peripherals have direct connections that allow autonomous communication between them and thus save CPU resources (thus power supply consumption). In addition, these hardware connections allow fast and predictable latency.

Depending on the peripherals, these interconnections can operate in Run, Sleep, and Stop modes.

3.17 Low-power direct memory access controller (LPDMA)

The low-power direct memory access (LPDMA) controller is a bus master and system peripheral.

The LPDMA is used to perform programmable data transfers between memory-mapped peripherals and/or memories via linked-lists, upon the control of an off-loaded CPU.

The main LPDMA features are:

- Single bidirectional AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Run, Sleep, and Stop 0 modes
- Transfers arbitration based on a four-grade programmed priority at a channel level:
  - One high-priority traffic class, for time-sensitive channels (queue 3)
  - Three low-priority traffic classes, with a weighted round-robin allocation for non time-sensitive channels (queues 0, 1, 2)
- Per-channel event generation, on any of the following events: transfer complete or half transfer complete or data transfer error or user setting error, and/or update linked-list item error or completed suspension and trigger overrun
- Per-channel interrupt generation, with separately programmed interrupt enable per event
- Eight concurrent LPDMA channels:
  - Intra-channel DMA transfers chaining via programmable linked-list into memory, supporting two execution modes: run-to-completion and link step mode
  - Intra-channel and inter-channel DMA transfers chaining via programmable DMA input triggers connection to DMA task completion events
- Per linked-list item within a channel:
  - Separately programmed source and destination transfers

  - Programmable data handling between source and destination: byte-based padding or truncation, sign extension and left/right realignment
  - Programmable number of data bytes to be transferred from the source, defining the block level
  - Linear source and destination addressing: either fixed or contiguously incremented addressing, programmed at a block level, between successive single transfers
  - Programmable LPDMA request and trigger selection
  - Programmable LPDMA half-transfer and transfer complete events generation
  - Pointer to the next linked-list item and its data structure in memory, with automatic update of the LPDMA linked-list control registers
- Debug:
  - Channel suspend and resume support
  - Channel status reporting and event flags
- TrustZone® support:
  - Support for secure and nonsecure LPDMA transfers, independently at a first-channel level, and independently at a source/destination and link sublevels
  - Secure and nonsecure interrupt reporting, resulting from any of the respectively secure and nonsecure channels
  - TrustZone®-aware AHB slave port, protecting any LPDMA secure resource (register, register field) from a nonsecure access
- Privileged/unprivileged support:
  - Support for privileged and unprivileged DMA transfers, independently at a channel level
  - Privileged-aware AHB slave port

Table 11. LPDMA1 channels implementation and usage

Channel x	Hardware parameters		Features
	dma_fifo_ size[x]	dma_ addressing[x]	
x = 0 to 7	0	0	Channel x is implemented with: – No FIFO. Only a single source transfer cell is internally registered. – Fixed/contiguously incremented addressing

Table 12. LPDMA1 autonomous mode and wake-up in low-power modes

Feature	Low-power modes
Autonomous mode and wake-up	Sleep and Stop 0 modes (wake-up also from Stop 1 mode)

3.18 Interrupts and events

3.18.1 Nested vectored interrupt controller (NVIC)

The devices embed a NVIC (nested vectored interrupt controller) that can manage 16 priority levels and handle up to 68 maskable interrupt vectors, plus the 16 interrupt vectors of the Cortex®-M33 processor.

The NVIC benefits are the following:

- Closely coupled NVIC giving low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead
- TrustZone® support: NVIC registers banked across secure and nonsecure states

The NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

3.18.2 Extended interrupt/event controller (EXTI)

The EXTI (extended interrupts and event controller) manages the individual CPU and system wake-up through configurable event inputs. It provides wake-up requests to the power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input.

The EXTI wake-up requests allow the system to be woken up from Stop modes.

The interrupt request and event request generation can also be used in Run and Sleep modes. The EXTI also includes the peripheral interconnect EXTI multiplexer I/O port selection.

The EXTI main features are the following:

- All event inputs are allowed to wake up the system
- Configurable events (signals from I/Os or peripherals able to generate a pulse)
  - Selectable active trigger edge
  - Interrupt pending status register bit independent for the rising and falling edge
  - Individual interrupt and event generation mask, used for conditioning the CPU wake-up, interrupt and event generation
  - Software trigger possibility
- TrustZone® secure events
  - The access to control and configure bits of secure input events can be made secure
- EXTI I/O port selection for peripheral interconnect use.

3.19 Cyclic redundancy check calculation unit (CRC)

The CRC is used to get a CRC code using a configurable generator with polynomial value and size.

Among other applications, the CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means to verify the flash memory integrity.

The CRC calculation unit helps to compute a signature of the software during runtime, that can be ulteriorly compared with a reference signature generated at link-time and that can be stored at a given memory location.

3.20 Quad-SPI interface (XSPI)

The devices embed one XSPI (Quad-SPI). The XSPI supports most external serial memories such as serial PSRAMs, and serial NAND and serial NOR flash memories, with the following functional modes:

- Indirect mode: all operations are performed using the XSPI registers to preset commands, addresses, data, and transfer parameters.
- Memory-mapped mode: the external memory is memory-mapped and is seen by the system as if it were an internal memory supporting read operations.

The XSPI supports the following protocols with associated frame formats:

- The standard frame format with the command, address, alternate byte, dummy cycles, and data phase

The XSPI offers the following features:

- Functional modes: indirect and memory-mapped
- Read support in memory-mapped mode
- Support for single, dual, and quad communication
- SDR (single-data rate) and DTR (double-transfer rate) support
- Data strobe support
- Fully programmable opcode
- Fully programmable frame format
- Integrated FIFO for reception and transmission
- 8-, 16-, and 32-bit data access allowed
- DMA channel for indirect-mode operations
- Interrupt generation on FIFO threshold, timeout, operation complete, and access error

3.20.1 XSPI TrustZone® security

When the TrustZone® security is enabled, the entire XSPI bank is secure after reset.

Up to two nonsecure areas can be configured through the TZSC MPCWM1 controller with a granularity of 128 Kbytes.

The XSPI registers can be configured as secure through the TZSC controller.

3.21 Delay block (DLYB)

The delay block (DLYB) is used to generate an output clock that is dephased from the input clock. The phase of the output clock must be programmed by the user application. The output clock is then used to clock the data received by another peripheral, such as the Quad-SPI interface. The delay is voltage- and temperature-dependent, that may require the application to reconfigure and recenter the output clock phase with the received data.

The delay block main features are:

- Input clock frequency ranging from 25 to maximum interface frequency
- Up to 12 oversampling phases

3.22 Analog-to-digital converter (ADC4)

The devices embed one successive-approximation analog-to-digital converter.

Table 13. ADC features

ADC modes/features(1)	ADC4
Resolution	12 bits
Maximum sampling speed for 12-bit resolution	2.5 Msps
Hardware offset calibration	X
Hardware linearity calibration	-
Single-ended inputs	X
Differential inputs	-
Injected channel conversion	-
Oversampling	Up to x256
Data register	16 bits
DMA support	X
Autonomous mode	X
Offset compensation	-
Gain compensation	-
Number of analog watchdogs	3
Wake-up from Stop mode	X

1. X = supported.

3.22.1 Analog-to-digital converter (ADC4)

The 12-bit ADC4 is a successive-approximation analog-to-digital converter. It has up to 19 multiplexed channels allowing it to measure signals from up to 7 external and 3 internal sources (the other channels are reserved). ADC conversion of the various channels can be performed in single, continuous, scan, or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.

An efficient low-power mode is implemented to allow very low consumption at low frequency. The ADC4 is autonomous in low-power modes down to Stop modes.

A built-in hardware oversampler allows analog performances to be improved while off-loading the related computational burden from the CPU.

The ADC4 main features are:

- High performance
  - 12-, 10-, 8-, or 6-bit configurable resolution
  - ADC conversion time: 0.4 µs for 12-bit resolution (2.5 MHz), faster conversion times obtained by lowering resolution
  - Self-calibration
  - Programmable sampling time
  - Data alignment with built-in data coherency
  - DMA support
- Low power consumption
  - PCLK frequency reduced for low-power operation while still keeping optimum ADC performance
  - Wait mode: ADC overrun prevented in applications with low frequency PCLK
  - Auto-off mode: ADC automatically powered off except during the active conversion phase, dramatically reducing the ADC power consumption
  - Autonomous mode: in low-power modes down to Stop 1 mode, the ADC4 is automatically switched on when a trigger occurs to start conversion, and it is automatically switched off after conversion. Data are transfered to SRAM with DMA.
  - ADC4 interrupts wake up the device from Stop 0 and Stop 1 modes.
- Analog input channels
  - Up to 7 external analog inputs
  - One channel for the internal temperature sensor (V_{SENSE})
  - One channel for the internal reference voltage (V_{REFINT})
  - One channel for the internal digital core voltage (V_{CORE})
- Start-of-conversion can be initiated:
  - By software
  - By hardware triggers with configurable polarity (timer events or GPIO input events)
- Conversion modes
  - Conversion of a single channel or scan of a sequence of channels
  - Selected inputs converted once per trigger in single mode
  - Selected inputs converted continuously in continuous mode
  - Discontinuous mode
- Interrupt generation at the end of sampling, end of conversion, end of sequence conversion, and in case of analog watchdog or overrun events, with wake-up from Stop capability
- Three analog watchdogs

- ADC supply requirements: 1.62 to 3.6 V
- ADC input range: $V_{SSA} < V_{IN} < V_{DDA}$

Note: The ADC4 analog block clock frequency after the ADC4 prescaler must be between 140 kHz and 55 MHz.

Note: V_{SSA} is connected to package pin VSS.

3.22.2 Temperature sensor (V_{SENSE})

The temperature sensor generates a voltage V_{SENSE} that varies linearly with temperature. The temperature sensor is internally connected to ADC4 input channel that is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it must be calibrated to obtain a good accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by STMicroelectronics in the system memory area, accessible in read-only mode.

Table 14. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	Temperature sensor ADC4 12-bit raw data acquired at (30 ± 5) °C, V_{DDA} = 3.0 V (± 10 mV)	0x0BF9 0710 - 0x0BF9 0711
TS_CAL2	Temperature sensor ADC4 12-bit raw data acquired at (130 ± 5) °C, V_{DDA} = 3.0 V (± 10 mV)	0x0BF9 0742 - 0x0BF9 0743

3.23 True random number generator (RNG)

The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a non-deterministic random bit generator (NDRBG).

The true random generator:

- Delivers 32-bit true random numbers, produced by an analog entropy source conditioned by a NIST SP800-90B approved conditioning stage
- Can be used as an entropy source to construct a non-deterministic random bit generator (NDRBG)
- Produces four 32-bit random samples every 412 AHB clock cycles if $f_{AHB} < 77$ MHz (256 RNG clock cycles otherwise)
- Embeds startup and NIST SP800-90B approved continuous health tests (repetition count and adaptive proportion tests), associated with specific error management

- Can be disabled to reduce power consumption, or enabled with an automatic low-power mode (default configuration)
- Has an AHB slave peripheral, accessible through 32-bit word single access only (otherwise an AHB bus error is generated, and the write access operations are ignored)

3.24 Encryption standard hardware accelerator (AES)

The devices embed one fast AES accelerators.

The AES can be used to both encrypt and decrypt data using the AES algorithm. It is a fully compliant implementation of the advanced encryption standard (AES) as defined by the Federal Information Processing Standards Publication (FIPS PUB 197, Nov 2001).

Multiple chaining modes are supported for key sizes of 128 or 256 bits. ECB, CBC, CTR, CCM, GCM, and GMAC chaining is supported by AES.

AES support DMA single transfers for incoming and outgoing data (two DMA channels required).

The AES supports the selection of all of the following key sources:

- 256-bit software key, written by the application in the key registers (write only)

Note: 128-bit key size can also be selected.

The AES peripherals support:

- Compliant implementation of standard NIST *Special Publication 197*, *Advanced Encryption Standard (AES)*, and *Special Publication 800-38A, Recommendation for Block Cipher Modes of Operation*
- 128-bit data block processing
- Support for 128- and 256-bit cipher key length
- Encryption and decryption with multiple chaining modes:
  - Electronic codebook (ECB) mode
  - Cipher block chaining (CBC) mode
  - Counter (CTR) mode
  - Galois counter mode (GCM)
  - Galois message authentication code (GMAC) mode
  - Counter with CBC-MAC (CCM) mode
- 51 or 75 clock cycle latency in ECB encryption mode for AES processing one 128-bit block of data with, respectively, 128- or 256-bit key
- Integrated round key scheduler to compute the last round key for AES ECB/CBC decryption
- 256-bit register for storing the cryptographic key (eight 32-bit registers), with key atomicity enforcement
- 128-bit registers for storing initialization vectors (four 32-bit registers)
- One 32-bit input buffer and one 32-bit output buffer
- Automatic data flow control with support of single-transfer direct memory access (DMA) using two channels (one for incoming data, one for processed data)
- Data swapping logic to support 1-, 8-, 16-, or 32-bit data

- Possibility for software to suspend a message if the AES needs to process another message with a higher priority (suspend/resume operation)

Table 15. AES features

AES modes/features(1)	AES
ECB, CBC chaining	X
CTR, CCM, GCM chaining	X
AES 128-bit ECB encryption in cycles	51
Side-channel attacks resistance	-

1. X = supported.

3.25 HASH hardware accelerator (HASH)

The HASH is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA2-224, and SHA-256) and the keyed-hash message authentication code (HMAC) algorithm. HMAC is suitable for applications requiring message authentication.

The HASH computes federal information processing standards (FIPS) approved digests of length of 160, 224, 256 bits, for messages of up to (2^{64} – 1) bits.

The HASH main features are:

- Suitable for data authentication applications, compliant with:
  - Federal Information Processing Standards Publication FIPS PUB 180-4, *Secure Hash Standard* (SHA-1 and SHA-2 family)
  - Federal Information Processing Standards Publication FIPS PUB 186-4, *Digital* Signature Standard (DSS)
  - Internet Engineering Task Force (IETF) Request For Comments RFC 2104, *HMAC: Keyed-Hashing for Message Authentication* and Federal Information Processing Standards Publication FIPS PUB 198-1, *The Keyed-Hash Message* Authentication Code (HMAC)
- Fast computation of SHA-1, SHA2-224, and SHA-256
  - 82 (respectively 66) clock cycles for processing one 512-bit block of data using SHA-1 (respectively SHA-256) algorithm
- Corresponding 32-bit words of the digest from consecutive message blocks are added to each other to form the digest of the whole message
  - Automatic 32-bit words swapping to comply with the internal little-endian representation of the input bit string
  - Word swapping supported: bits, bytes, half-words, and 32-bit words
- Automatic padding to complete the input bit string to fit digest minimum block size of 512 bits (16 × 32 bits)
- Single 32-bit input register associated to an internal input FIFO of sixteen 32-bit words, corresponding to one block size
- AHB slave peripheral, accessible through 32-bit word accesses only (else an AHB error is generated)
- 8 × 32-bit words (H0 to H7) for output message digest

- Automatic data flow control with support of direct memory access (DMA) using one channel. Single or fixed burst of four supported.
- Interruptible message digest computation, on a per-32-bit word basis
  - Re-loadable digest registers
  - Hashing computation suspend/resume mechanism, including using DMA

3.26 On-the-fly decryption engine (OTFDEC)

The OTFDEC allows the decryption of the on-the-fly AHB traffic based on the read request address information, for example, execute-in-place of a code stored encrypted. Four independent and nonoverlapping encrypted regions can be defined in OTFDEC.

OTFDEC uses AES-128 in counter mode to achieve the lowest possible latency. Consequently, each time the content of one encrypted region is changed, the entire region must be re-encrypted with a different cryptographic context (key or initialization vector). This constraint makes OTFDEC suitable for decrypting read-only data or code, stored in an external NOR flash memory.

Note: When OTFDEC is used with XSPI, it is mandatory to access the flash memory using the memory-mapped mode of the flash memory controller.

When security is enabled in the product, OTFDEC can be programmed only by a secure host.

The OTFDEC main features are the following:

- On-the-fly 128-bit decryption during XSPI memory-mapped read operations (single or multiple)
  - Use of AES in counter (CTR) mode, with two 128-bit key stream buffers
  - Support for any read size
  - Physical address of the reads is used for the encryption/decryption
- Up to 4 independent encrypted regions
  - Granularity of the region definition: 4096 bytes
  - Region configuration write locking mechanism
  - Each region has its own 128-bit key, two-byte firmware version, and eight bytes of application-defined nonce. At least one of those must be changed each time an encryption is performed by the application.
- Encryption keys confidentiality and integrity protection
  - Write-only registers, with software locking mechanism
  - Availability of 8-bit CRC as public key information
- Support for the XSPI prefetching mechanism
- Possibility to select an enhanced encryption mode to add a proprietary layer of protection on top of the AES stream cipher (execute only)
- AMBA® AHB slave peripheral, accessible through 32-bit word single access only (otherwise an AHB bus error is generated, and write access operations are ignored)
- Secure-only programming if TrustZone® security is enabled
- Encryption mode

3.27 Public key accelerator (PKA)

The PKA is intended for the computation of cryptographic public key primitives, specifically those related to RSA, DU (Diffie-Hellmann), or (ECC) elliptic curve cryptography over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

All needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

The PKA main features are:

- Acceleration of RSA, DH and ECC over GF(p) operations, based on the Montgomery method for fast modular multiplications. More specifically:
  - RSA modular exponentiation, RSA CRT (Chinese remainder theorem) exponentiation
  - ECC scalar multiplication, point on curve check, complete addition, double base ladder, projective to affine
  - ECDSA signature generation and verification
- Capability to handle operands up to 4160 bits for RSA/DH and 640 bits for ECC
- Arithmetic and modular operations such as addition, subtraction, multiplication, modular reduction, modular inversion, comparison, and Montgomery multiplication
- Built-in Montgomery domain inward and outward transformations
- Protection against DPA (differential power analysis) and related side-channel attacks

3.28 Timers and watchdog

The devices include three general-purpose timers, two low-power timers, one watchdog timer, and two SysTick timers.

Table 16 compares the features of the advanced control, general-purpose, and basic timers.

Table 16. Timers comparison

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
General-purpose	TIM2	32 bits	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM16, TIM17	16 bits	Up			1	1

3.28.1 General-purpose timers (TIM2, TIM16, TIM17)

There are up to four synchronizable general-purpose timers embedded in the device (see *Table 16* for differences). Each general-purpose timer can be used to generate PWM outputs, or act as a simple time base.

- TIM2
  - This is a full-featured general-purpose timer with a 32-bit auto-reload up/downcounter, with 16-bit prescaler.
  - This timer features four independent channels for input capture/output compare, PWM, or one-pulse mode output. It can work with the other general-purpose timers via the *Timer Link* feature for synchronization or event chaining.
  - The counter can be frozen in Debug mode.
  - It has independent DMA request generation and support quadrature encoders.
- TIM16 and 17
  - They are general-purpose timers with mid-range features.
  - They have 16-bit auto-reload upcounters and 16-bit prescalers. and have one channel and one complementary channel.
  - All channels can be used for input capture/output compare, PWM or one-pulse mode output.
  - The timers can work together via the *Timer Link* feature for synchronization or event chaining. The timers have independent DMA request generation.
  - The counters can be frozen in Debug mode.
  - All have independent DMA request generation.

3.28.2 Low-power timers (LPTIM1, LPTIM2)

The devices embed two low-power timers. These timers have an independent clock and are running in Stop mode if they are clocked by HSI16, LSE, LSI, or an external clock. They are able to wake up the system from Stop mode.

LPTIM1 and LPTIM2 are active in Stop modes.

The low-power timer supports the following features:

- 16-bit upcounter with 16-bit autoreload register
- 3-bit prescaler with the following possible dividing factors: 1, 2, 4, 8, 16, 32, 64, and 128
- Selectable clock
  - Internal clock sources: LSE, LSI, HSI16 or APB clock
  - External clock source over LPTIM input (working with no LP oscillator running, used by *Pulse Counter* application)
- 16-bit ARR autoreload register
- 16-bit capture/compare register
- Continuous/one-shot mode
- Selectable software/hardware input trigger
- Programmable digital glitch filter
- Configurable output: pulse, PWM
- Configurable I/O polarity

- Encoder mode
- Repetition counter
- Up to two independent channels for:
  - Input capture
  - PWM generation (edge-aligned mode)
  - One-pulse mode output
- Interrupt generation on ten events
- DMA request generation on the following events:
  - Update event
  - Input capture

3.28.3 Infrared interface (IRTIM)

An infrared interface (IRTIM) for remote control is available on the device. It can be used with an infrared LED to perform remote control functions. It uses internal connections with TIM16 and TIM17.

3.28.4 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and a 10-bit prescaler. It is clocked from the independent LSI and, as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware- or software-enabled through the option bytes. The counter can be frozen in low-power and Debug modes.

3.28.5 SysTick timer

The Cortex®-M33 with TrustZone® embeds two SysTick timers.

When TrustZone® is activated, two SysTick timer are available:

- SysTick, secure instance
- SysTick, nonsecure instance

When TrustZone® is disabled, only one SysTick timer is available.

This timer (secure or nonsecure) is dedicated to real-time operating systems, but can also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.29 Real-time clock (RTC)

The real-time clock (RTC) is an independent BCD timer/counter. The RTC provides a time-of-day clock/calendar with programmable alarm interrupts.

Down to Standby retention, the RTC never stops, regardless of the device status (even under reset).

The RTC supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, and year, in binary-coded decimal (BCD) format
- Binary mode with 32-bit free-running counter
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a reference clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature that can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event
- 17-bit auto-reload wake-up timer (WUT) for periodic events with programmable resolution and period
- TrustZone® support:
  - RTC fully securable
  - Alarm A, alarm B, wake-up timer, and timestamp individual secure or nonsecure configuration
  - Alarm A, alarm B, wake-up timer, and timestamp individual privileged protection

The RTC is supplied from the V_{DD} supply.

The RTC clock sources can be one of the following:

- LSE, used as 32.768 kHz external crystal oscillator
- LSE, with external resonator or oscillator
- LSI, internal low-power RC oscillator (with a typical frequency of 32 kHz)
- HSE32, high-speed external clock divided by a prescaler in the RCC.

The RTC is functional in all low-power modes (except Standby) when it is clocked by the LSE or LSI.

All RTC events (alarm, wake-up timer, timestamp) can generate an interrupt and wake up the device from the low-power modes (except Standby).

3.30 Tamper and backup registers (TAMP)

The anti-tamper detection circuit is used to protect sensitive data from external attacks. 32 32-bit backup registers are retained down to Standby retention mode. The backup registers, as well as other secrets in the device, are protected by this anti-tamper detection circuit with four tamper pins and nine internal tampers. The external tamper pins can be configured for level detection with or without filtering, or active tamper that increases the security level by auto checking that the tamper pins are not externally opened or shorted.

Main TAMP features:

- A tamper detection can erase the backup registers, SRAM2, ICACHE, and cryptographic peripherals.
- 32 32-bit backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the Backup domain that remains powered-on down to Standby retention mode.
- Up to 4 tamper pins for external tamper detection events:
  - Active tamper mode: continuous comparison between tamper output and input to protect from physical open-short attacks
  - Flexible active tamper I/O management: from two (each input associated to its own exclusive output) to three meshes (single output shared for up to three tamper inputs)
  - Passive tampers: ultra-low-power edge or level detection with internal pull-up hardware management
  - Configurable digital filter
- Nine internal tamper events to protect against transient or environmental perturbation attacks:
  - LSE monitoring
  - RTC calendar overflow
  - JTAG/SWD access if RDP different from 0
  - Monotonic counter overflow
  - Cryptographic peripherals fault (RNG, AES, PKA)
  - Independent watchdog reset when tamper flag is already set
  - Three ADC4 watchdogs
- Each tamper can be configured in two modes:
  - Hardware mode: immediate erase of secrets on tamper detection, including backup registers erase
  - Software mode: erase of secrets following a tamper detection launched by software
- Any tamper detection can generate an RTC time stamp event.
- TrustZone® support:
  - Tamper secure or nonsecure configuration.
  - Backup registers configuration in three configurable-size areas:
    - a read/write secure area
    - a write secure/read nonsecure area
    - a read/write nonsecure area
- Tamper configuration and backup registers privilege protection
- Monotonic counter

3.31 Inter-integrated circuit interface (I2C)

The device embeds two I2Cs, refer to *Table 17* for the features implementation.

The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration, and timing.

The I2C peripheral supports:

- I²C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multi-master capability
  - Standard mode (Sm), with a bit rate up to 100 Kbit/s
  - Fast mode (Fm), with a bit rate up to 400 Kbit/s
  - Fast mode Plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 3.0 compatibility:
  - Hardware packet error checking (PEC) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming
- Autonomous functionality in Stop modes with wake-up from Stop capability
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

Table 17. I2C implementation

I2C features(1)	I2C1	I2C3
Standard-mode (up to 100 Kbit/s)	X	X
Fast-mode (up to 400 Kbit/s)	X	X
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X	X
Programmable analog and digital noise filters	X	X
SMBus/PMBus hardware support	X	X
Independent clock	X	X
Autonomous in Stop 0 and Stop 1 modes with wake-up capability	X	X
Wake-up capability from Stop 2 mode	-	X

1. X: supported

3.32 Universal synchronous/asynchronous receiver transmitter (USART/UART) and low-power universal asynchronous receiver transmitter (LPUART)

The devices have two embedded universal synchronous receiver transmitters (USART) and one low-power universal asynchronous receiver transmitter (LPUART1).

Table 18. U(S)ART and LPUART features

USART modes/features[1]	USART1	LPUART1
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (master/slave)	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual-clock domain and wake-up from Stop modes	X	X
Receiver timeout interrupt	X	-
Modbus communication	X	-
Auto-baud rate detection	X	-
Driver enable	X	X
USART data length	7, 8, and 9 bits	
Tx/Rx FIFO	X	X
Tx/Rx FIFO size	8 bytes	
Autonomous mode in Stop 0 and Stop 1 mode	X	X
Wake-up capability from Stop 2 mode	-	X

1. X = supported.

3.32.1 USART/UART

The U(S)ART offers a flexible means to perform full-duplex data exchanges with external equipments requiring an industry-standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The U(S)ART supports both synchronous one-way and half-duplex single-wire communications, as well as LIN (local interconnection network), Smartcard protocol, IrDA (infrared data association) SIR ENDEC specifications, and modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications up to 20 Mbaud/s are possible by using the direct memory access (DMA) for multibuffer configuration.

The main U(S)ART features are:

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Two internal FIFOs for transmitting and receiving data
  Each FIFO can be enabled/disabled by software and come with a status flag.

- A common programmable transmit and receive baud rate
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Automatic baud rate detection
- Programmable data word length (7, 8, or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Synchronous master/slave mode and clock output/input for synchronous communications
- SPI slave transmission underrun error flag
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Communication control/error detection flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Interrupt sources with flags
- Multiprocessor communications: wake-up from mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from stop capability
- LIN master synchronous break send capability and LIN slave break detection capability
  - 13-bit break generation and 10/11-bit break detection when USART is hardware configured for LIN
- IrDA SIR encoder decoder supporting 3/16-bit duration for Normal mode
- Smartcard mode
  - Supports the T = 0 and T = 1 asynchronous protocols for smartcards as defined in the ISO/IEC 7816-3 standard
  - 0.5 and 1.5 stop bits for Smartcard operation
- Support for Modbus communication
  - Timeout feature
  - CR/LF character recognition

3.32.2 LPUART

The LPUART supports bidirectional asynchronous serial communication with minimum power consumption. It also supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame

while having an extremely low energy consumption. Higher-speed clock can be used to reach higher baudrates.

The LPUART interface can be served by the DMA controller.

The LPUART main features are:

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 baud/s to 9600 baud/s using a 32.768 kHz clock source
- Higher baud rates can be achieved by using a higher frequency clock source
- Two internal FIFOs to transmit and receive data
  Each FIFO can be enabled/disabled by software and come with status flags for FIFOs states.
- Dual-clock domain with dedicated kernel clock for peripherals independent from PCLK
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire half-duplex communications
- Continuous communications using DMA
- Received/transmitted bytes are buffered in reserved SRAM using centralized DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Swappable Tx/Rx pin configuration
- Hardware flow control for modem and RS-485 transceiver
- Transfer detection flags:
  - Receive buffer full
  - Transmit buffer empty
  - Busy and end of transmission flags
- Parity control:
  - Transmits parity bit
  - Checks parity of received data byte
- Four error detection flags:
  - Overrun error
  - Noise detection
  - Frame error
  - Parity error
- Interrupt sources with flags
- Multiprocessor communications: wake-up from mute mode by idle line detection or address mark detection
- Autonomous functionality in Stop mode with wake-up from Stop capability

3.33 Serial peripheral interface (SPI)

The devices embed one serial peripheral interface (SPI) that can be used to communicate with external devices while using the specific synchronous protocol. The SPI protocol supports half-duplex, full-duplex, and simplex synchronous serial communication with external devices.

The interface can be configured as master or slave and can operate in multi-slave or multi-master configurations. The device configured as master provides communication clock (SCK) to the slave device. The slave select (SS) and ready (RDY) signals can be applied optionally to set up communication with concrete slave devices and to assure it handles the data flow properly. The Motorola data format is used by default, but several other specific modes are supported as well.

The main SPI features are:

- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfers on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- 4- to 32-bit data size selection or fixed at 8- and 16-bit only
- Multimaster or multislave mode capability
- Dual-clock domain, separated clock for the peripheral kernel that can be independent of PCLK
- Baud rate prescaler up to kernel frequency/2 or bypass from RCC in master mode
- Protection of configuration and setting
- Hardware or software management of SS for both master and slave
- Adjustable minimum delays between data and between SS and data flow
- Configurable SS signal polarity and timing, MISO and MOSI swap capability
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Programmable number of data within a transaction to control SS and CRC
- Dedicated transmission and reception flags with interrupt capability
- SPI Motorola and TI formats support
- Hardware CRC feature can secure communication at the end of transaction by:
  - Adding CRC value in Tx mode
  - Automatic CRC error checking for Rx mode
- Error detection with interrupt capability in case of data overrun, CRC error, data underrun at slave, mode fault at master
- Two 8 x 8-bit embedded Rx and TxFIFOs with DMA capability
- Programmable number of data in transaction
- Configurable FIFO thresholds (data packing)
- Configurable behavior at slave underrun condition (support of cascaded circular buffers)
- Autonomous functionality in Stop modes (handling of the transaction flow and required clock distribution) with wake-up from stop capability
- Optional status pin RDY signaling the slave device is ready to handle the data flow.

Table 19. SPI features

SPI feature[1]	SPI3 (limited feature set instance)
Data size	8- and 16-bit
CRC computation	CRC polynomial length, configurable from 9- to 17-bit
Size of FIFOs	8 x 8-bit
Number of transfered data	Up to 1024, no data counter
Autonomous in Stop 0 and Stop 1 modes with wake-up capability	X
Wake-up capability from Stop 2 mode	-

1. X: supported

3.34 Serial audio interfaces (SAI)

The devices embed one SAI, refer to *Table 20* for its features. The SAI bus interface handles communications between the microcontroller and the serial audio protocol.

Depending upon the device, the SAI peripheral can support:

- Two independent audio sub-blocks that can be transmitters or receivers with their respective FIFOs
- 8-word integrated FIFOs for each audio subblock
- Synchronous or asynchronous mode between the audio subblocks
- Master or slave configuration independent for both audio subblocks
- Clock generator for each audio block to target independent audio frequency sampling when both audio sub-blocks are configured in master mode
- Data size configurable: 8-, 10-, 16-, 20-, 24-, and 32-bit
- Peripheral with large configurability and flexibility allowing to target as example the following audio protocol: I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97, and SPDIF out
- Up to 16 slots available with configurable size and with the possibility to select which ones are active in the audio frame
- Number of bits by frame may be configurable
- Frame synchronization active level configurable (offset, bit length, level)
- First active bit position in the slot is configurable
- LSB first or MSB first for data transfer
- Mute mode
- Stereo/mono audio frame capability
- Communication clock strobing edge configurable (SCK)

- Error flags with associated interrupts if enabled respectively
  - Overrun and underrun detection
  - Anticipated frame synchronization signal detection in slave mode
  - Late frame synchronization signal detection in slave mode
  - Codec not ready for the AC’97 mode in reception
- Interruption sources when enabled:
  - Errors
  - FIFO requests
- DMA interface with two dedicated channels to handle access to the dedicated integrated FIFO of each SAI audio subblock

Table 20. SAI implementation(1)

Features	SAI1	
	block A	block B
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC’97 X	X	X
Mute mode	X	X
Stereo/mono audio frame capability	X	X
16 slots	X	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, and 32-bit	X	X
FIFO size	X (8 words)	X (8 words)
SPDIF	X	X
PDM	X	-
FS	X	-
SCK	X	-
SD	X	X
MCLK	X	-

1. X: supported.

3.35 USB full speed (USB)

Main USB features

- USB specification version 2.0 full-speed compliant
- Host and device functions
- 2048 bytes of dedicated SRAM data buffer memory
- Configurable number of endpoints from 1 to 8
- Cyclic redundancy check (CRC) generation/checking, non-return-to-zero inverted (NRZI) encoding/decoding, and bit-stuffing
- Isochronous transfers support
- Double-buffered bulk/isochronous endpoint support
- USB suspend/resume operations
- Frame-locked clock pulse generation
- USB 2.0 Link power management support in device mode
- Battery charging specification revision 1.2 support in device mode

3.36 Development support

3.36.1 Serial-wire/JTAG debug port (SWJ-DP)

The Arm SWJ-DP interface is embedded and is a combined JTAG and serial-wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using two pins only instead of five required by the JTAG (JTAG pins can be re-used as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.36.2 Embedded Trace Macrocell

Arm Embedded Trace Macrocell (ETM) provides greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the devices through a small number of ETM pins to an external hardware trace port analyzer (TPA) device.

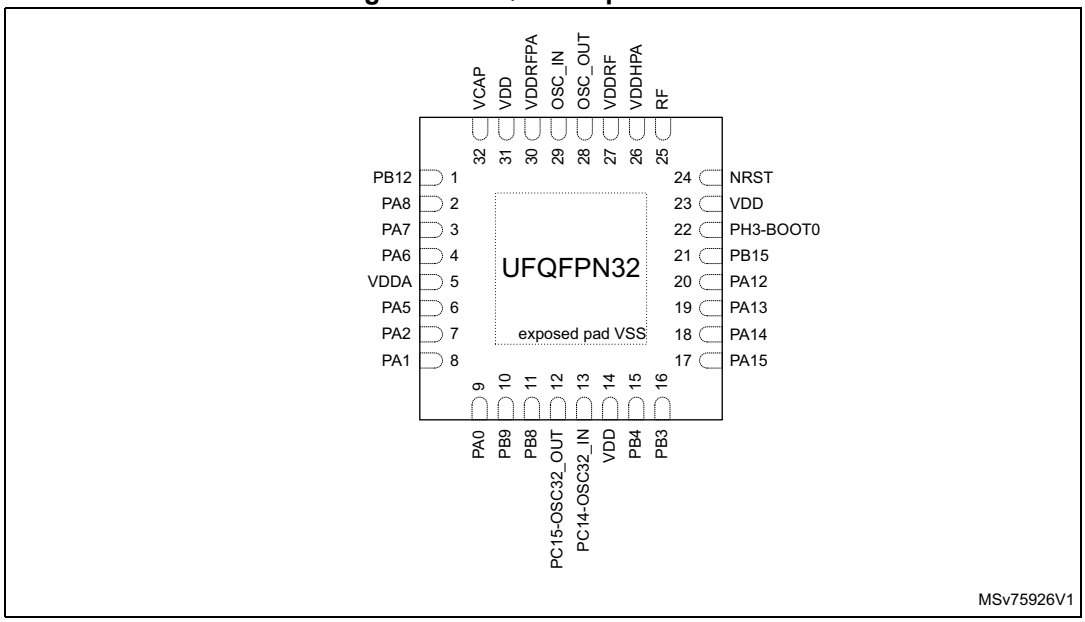
Real-time instruction and data flow activity is recorded and then formatted for display on the host computer running the debugger software. TPA hardware is commercially available from common development tool vendors.

ETM operates with third party debugger software tools.

4 Pinout, pin description, and alternate functions

4.1 Pinout/ballout schematics

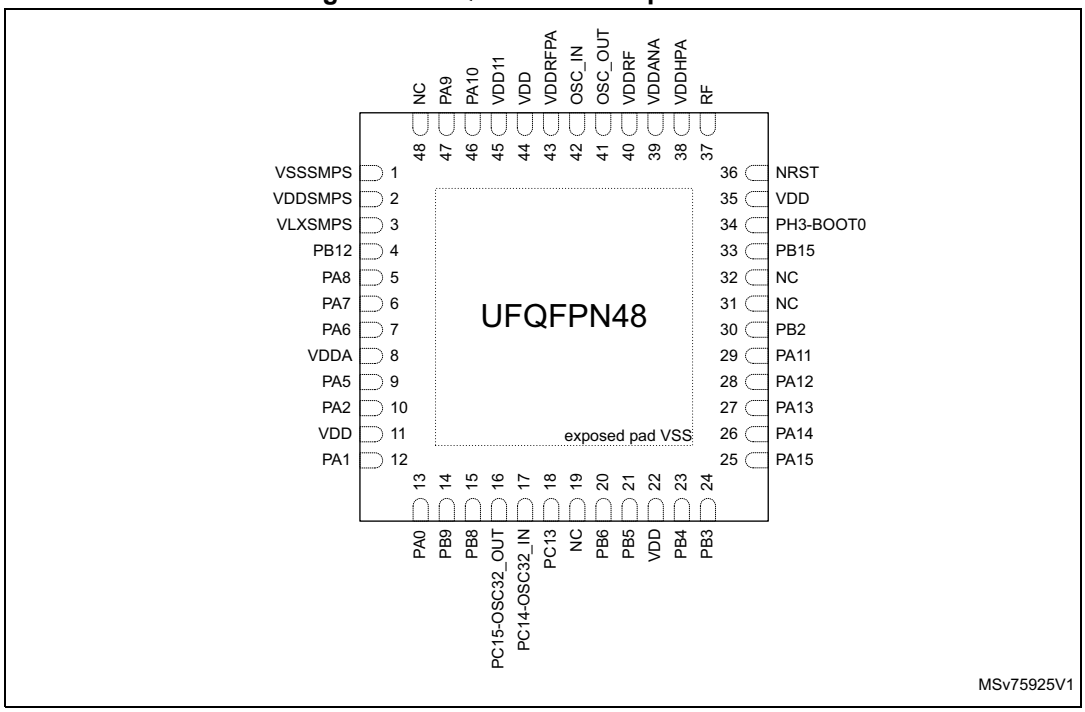
Figure 7. UFQFPN32 pinout(1) (2)



1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

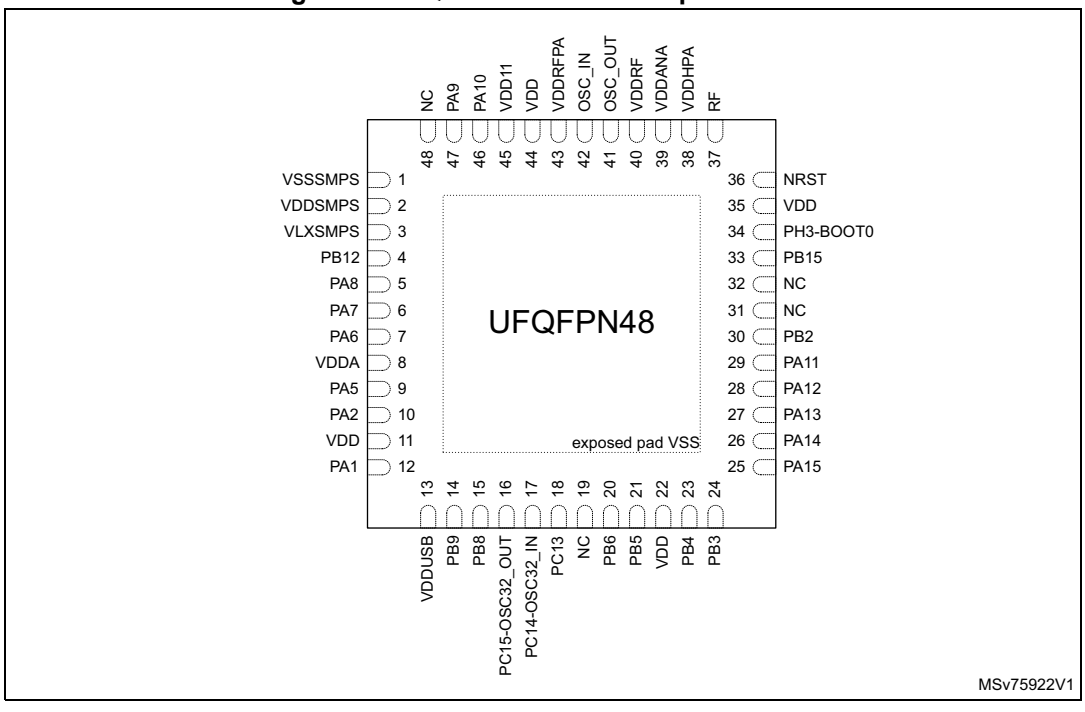
1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.
1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Figure 8. UFQFPN48 SMPS pinout(1) (2)



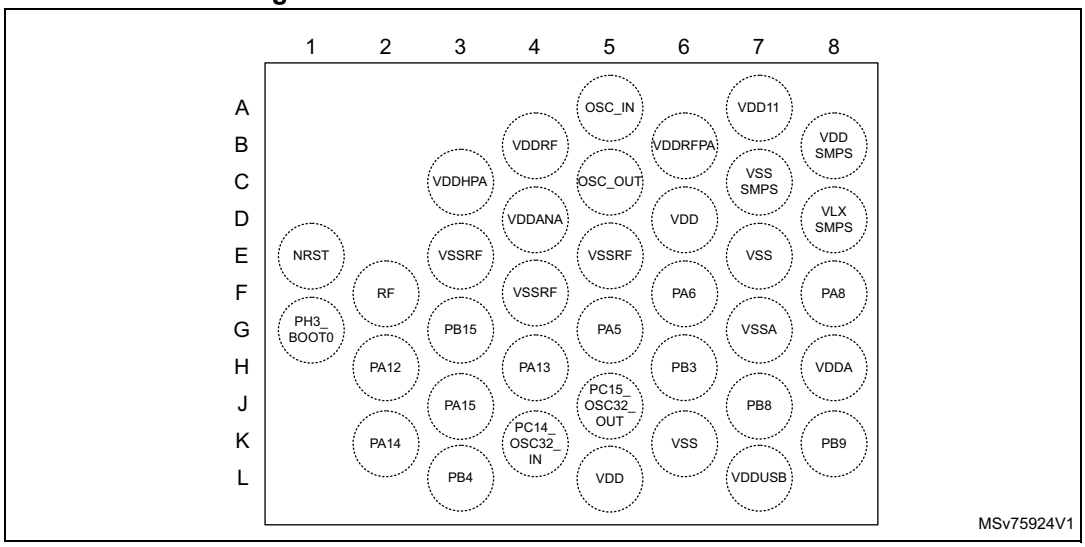
1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Figure 9. UFQFPN48 SMPS USB pinout(1) (2)



1. The above figure shows the package top view.
2. The exposed pad must be connected to ground plane.

Figure 10. Thin WLCSP37 SMPS USB ballout(1)



1. The above figure shows the package top view.

4.2 Pin description

Table 21. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V-tolerant I/O
		TT	3.6 V-tolerant I/O
		RF	RF I/O
		RST	Bidirectional reset pin with weak pull-up resistor
		Option for TT or FT I/Os(1)	
		_f	I/O, Fm+ capable
		_a	I/O, with analog switch function supplied by V_{DDA}
		_u	I/O, with USB switch function supplied by V_{DDUSB}
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. The related I/O structures in *Table 22* are a concatenation of various options. Examples: FT_a, FT_fa, FT_f.

Table 22. STM32WBA2xxx pin/ball definitions

Pin number				Name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	Thin WLCSP37 SMPS USB	UFQFPN48 SMPS	UFQFPN48 SMPS USB						
-	C7	1	1	VSSSMPS	S	-	-	-	-
-	B8	2	2	VDDSMPS	S	-	-	-	-
-	D8	3	3	VLXSMPS	S	-	-	-	-
1	-	4	4	PB12	I/O	FT	-	TIM2_CH1, TIM2_ETR, USART1_TX, SAI1_SD_A, EVENTOUT	-
2	F8	5	5	PA8	I/O	FT_fa	-	MCO, TIM2_CH2, LPTIM1_CH2, SAI1_D1, I2C3_SDA, SPI3_SCK, SPI3_RDY, USART1_RX, USB_SOF, SAI1_FS_A, EVENTOUT	ADC4_IN1
3	-	6	6	PA7	I/O	FT_fa	-	TIM2_CH3, I2C3_SDA, SPI3_MISO, USART1_CTS, USART1_RX, SAI1_SCK_A, EVENTOUT	ADC4_IN2, WKUP8, TAMP_IN1/TAMP_OUT2
4	F6	7	7	PA6	I/O	FT_fa	-	CSTOP, TIM2_CH4, SAI1_CK2, I2C3_SCL, SPI3_MOSI, SPI3_RDY, USART1_RTS_DE, USART1_TX, SAI1_SD_A, SAI1_MCLK_A, EVENTOUT	ADC4_IN3, WKUP7
-	G7	-	-	VSSA	S	-	-	-	-
5	H8	8	8	VDDA	S	-	-	-	-

Table 22. STM32WBA2xxx pin/ball definitions (continued)

Pin number				Name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	Thin WLCSP37 SMPS USB	UFQFPN48 SMPS	UFQFPN48 SMPS USB						
6	G5	9	9	PA5	I/O	FT_a	-	CSLEEP, TIM2_CH1, TIM2_ETR, SAI1_D2, SPI3_NSS, USART1_CK, USART1_TX, SAI1_SCK_A, AUDIOCLK, LPTIM2_ETR, EVENTOUT	ADC4_IN4, WKUP6
7	-	10	10	PA2	I/O	FT_a	-	SAI1_D1, USART1_RTS_DE, LPUART1_TX, XSPI1_DQS, XSPI1_NCS, LPTIM2_CH1, TIM16_CH1, EVENTOUT	ADC4_IN7, WKUP4, LSCO
-	D6	11	11	VDD	S	-	-	-	-
8	-	12	12	PA1	I/O	FT_a	-	SAI1_CK1, USART1_CK, LPUART1_RX, LPTIM2_CH2, TIM17_CH1, EVENTOUT	ADC4_IN8, WKUP3
9	-	13	-	PA0	I/O	FT_a	-	LPTIM1_IN1, SPI3_SCK, LPUART1_CTS, EVENTOUT	ADC4_IN9, WKUP1
-	L7	-	13	VDDUSB	S	-	-	-	-
10	K8	14	14	PB9	I/O	FT_u	-	RTC_REFIN, SPI3_MISO, LPUART1_RTS_DE, XSPI1_IO3, LPTIM2_IN1, TIM16_CH1, EVENTOUT	USB_DM, WKUP8
11	J7	15	15	PB8	I/O	FT_u	-	LPTIM1_ETR, SPI3_MOSI, LPUART1_CTS, XSPI1_IO2, TIM16_CH1N, EVENTOUT	USB_DP

Table 22. STM32WBA2xxx pin/ball definitions (continued)

Pin number				Name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	Thin WLCSP37 SMPS USB	UFQFPN48 SMPS	UFQFPN48 SMPS USB						
12	J5	16	16	PC15-OSC32_OUT	I/O	FT	-	EVENTOUT	OSC32_OUT
13	K4	17	17	PC14-OSC32_IN	I/O	FT	-	EVENTOUT	OSC32_IN
-	-	18	18	PC13	I/O	FT	-	EVENTOUT	WKUP2, RTC_TS/RTC_OUT1, TAMP_IN4/TAMP_OUT3
-	-	19	19	NC	-	-	-	-	-
-	-	20	20	PB6	I/O	FT	-	TIM2_CH1, TIM2_ETR, TRACECLK, XSPI1_IO3, EVENTOUT	WKUP3
-	-	21	21	PB5	I/O	FT	-	SAI1_D2, TRACED3, LPUART1_TX, XSPI1_IO2, EVENTOUT	-
-	K6	-	-	VSS	S	-	-	-	-
14	L5	22	22	VDD	S	-	-	-	-
15	L3	23	23	PB4	I/O	FT	(1)	NJTRST, LPTIM2_IN2, SPI3_MISO, TRACED2, USART1_CTS, SAI1_CK1, XSPI1_IO1, TIM17_CH1, PTA_ACTIVE, PTA_PRIORITY, EVENTOUT	-

Table 22. STM32WBA2xxx pin/ball definitions (continued)

Pin number				Name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	Thin WLCSP37 SMPS USB	UFQFPN48 SMPS	UFQFPN48 SMPS USB						
16	H6	24	24	PB3	I/O	FT_f	(1)	JTDO/TRACESWO, LPTIM1_IN2, I2C1_SDA, TRACED1, XSPI1_IO0, TIM17_CH1N, PTA_ACTIVE, EVENTOUT	-
17	J3	25	25	PA15	I/O	FT_f	(1)	JTDI, LPTIM1_CH2, I2C1_SCL,TRACED0, XSPI1_CLK, TIM17_BKIN, PTA_STATUS, EVENTOUT	-
18	K2	26	26	PA14	I/O	FT	(1)	JTCK/SWCLK, PTA_STATUS, EVENTOUT	TAMP_IN3/TAMP_OUT4
19	H4	27	27	PA13	I/O	FT	(1)	JTMS/SWDIO, IR_OUT, USB_NOE, PTA_PROIORITY, EVENTOUT	-
20	H2	28	28	PA12	I/O	FT	-	LPTIM1_CH1, USART1_RX, SAI1_SD_B, XSPI1_NCS, RF_ANTSW0, PTA_STATUS, PTA_ACTIVE, EVENTOUT	WKUP6
-	-	29	29	PA11	I/O	FT_f	-	I2C1_SDA, I2C3_SDA, LPTIM2_CH1, RF_ANTSW1, PTA_ACTIVE, EVENTOUT	-
-	-	30	30	PB2	I/O	FT_f	-	I2C1_SCL, I2C3_SCL, USART1_TX, XSPI1_NCS, RF_ANTSW2, EVENTOUT	WKUP1, RTC_OUT2
-	-	31	31	NC	-	-	-	-	-

Table 22. STM32WBA2xxx pin/ball definitions (continued)

Pin number				Name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	Thin WLCSP37 SMPS USB	UFQFPN48 SMPS	UFQFPN48 SMPS USB						
-	-	32	32	NC	-	-	-	-	-
21	G3	33	33	PB15	I/O	TT	-	I2C1_SMBA, I2C3_SMBA, LPUART1_CTS, LPUART1_RX, TIM16_BKIN, PTA_GRANT, RF_EXTPABYP1, EVENTOUT	-
22	G1	34	34	PH3-BOOT0	I/O	TT	-	LPUART1_RTS, LPUART1_TX, RF_EXTPABYP2, PTA_GRANT, EVENTOUT	TAMP_IN2/TAMP_OUT1
23	-	35	35	VDD	S	-	-	-	-
24	E1	36	36	NRST	I/O	RST	-	-	-
-	E3	-	-	VSSRF	S	-	-	-	-
25	F2	37	37	RF	I/O	RF	-	-	-
-	F4	-	-	VSSRF	S	-	-	-	-
26	C3	38	38	VDDHPA	S	-	-	-	-
-	E5	-	-	VSSRF	S	-	-	-	-
-	D4	39	39	VDDANA	S	-	-	-	-
27	B4	40	40	VDDRF	S	-	-	-	-
28	C5	41	41	OSC_OUT	O	RF	-	-	-
29	A5	42	42	OSC_IN	I	RF	-	-	-
30	B6	43	43	VDDRFPA	S	-	-	-	-

Table 22. STM32WBA2xxx pin/ball definitions (continued)

Pin number				Name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UFQFPN32	Thin WLCSP37 SMPS USB	UFQFPN48 SMPS	UFQFPN48 SMPS USB						
31	-	44	44	VDD	S	-	-	-	-
-	E7	-	-	VSS	S	-	-	-	-
32	-	-	-	VCAP	S	-	-	-	-
-	A7	45	45	VDD11	S	-	-	-	-
-	-	46	46	PA10	I/O	FT	-	SAI1_D1, SPI3_MISO, LPUART1_RX, LPUART1_RTS, EVENTOUT	-
-	-	47	47	PA9	I/O	FT	-	SAI1_CK1, SPI3_MOSI, USART1_RX, LPUART1_RTS_DE, EVENTOUT	-
-	-	48	48	NC	-	-	-	-	-
33	-	49	49	VSS (exposed pad)	S	-	-	-	-

1. After reset, this pin is configured as JTAG/SWD alternate function, with internal pull-up on PA15, PA13, PB4 pins and internal pull-down on PA14 pin.

4.3 Alternate functions

Table 23. Alternate function AF0 to AF7(1)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		LPTIM1/SYS_AF	TIM2	LPTIM1/2TIM2	SAI1/USB	I2C1/3/SPI3	SPI3	I2C3/SPI3/ SYS_AF	USART1
A	PA0	LPTIM1_IN1	-	-	-	-	-	SPI3_SCK	-
	PA1	-	-	-	SAI1_CK1	-	-	-	USART1_CK
	PA2	-	-	-	SAI1_D1	-	-	-	USART1_RTS_DE
	PA5	CSLEEP	TIM2_CH1	TIM2_ETR	SAI1_D2	-	-	SPI3_NSS	USART1_CK
	PA6	CSTOP	TIM2_CH4	-	SAI1_CK2	I2C3_SCL	SPI3_MOSI	SPI3_RDY	USART1_RTS_DE
	PA7	-	TIM2_CH3	-	-	I2C3_SDA	SPI3_MISO		USART1_CTS
	PA8	MCO	TIM2_CH2	LPTIM1_CH2	SAI1_D1	I2C3_SDA	SPI3_SCK	SPI3_RDY	USART1_RX
	PA9	-	-	-	SAI1_CK1	SPI3_MOSI	-	-	USART1_RX
	PA10	-	-	-	SAI1_D1	-	SPI3_MISO	-	-
	PA11	-	-	-	-	I2C1_SDA	-	I2C3_SDA	-
	PA12	-	-	LPTIM1_CH1	-	-	-	-	USART1_RX
	PA13	JTMS/SWDIO	IR_OUT	-	USB_NOE	-	-	-	-
	PA14	JTCK/SWCLK	-	-	-	-	-	-	-
	PA15	JTDI	-	LPTIM1_CH2	-	I2C1_SCL	-	TRACED0	-

Table 23. Alternate function AF0 to AF7[1] (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		LPTIM1/SYS_AF	TIM2	LPTIM1/2TIM2	SAI1/USB	I2C1/3/SPI3	SPI3	I2C3/SPI3/ SYS_AF	USART1
B	PB2	-	-	-	-	I2C1_SCL	-	I2C3_SCL	USART1_TX
	PB3	JTDO/ TRACESWO	-	LPTIM1_IN2	-	I2C1_SDA	-	TRACED1	-
	PB4	NJTRST	-	LPTIM2_IN2	-	SPI3_MISO	-	TRACED2	USART1_CTS
	PB5	-	-	-	SAI1_D2	-	-	TRACED3	-
	PB6	-	TIM2_CH1	TIM2_ETR	-	-	-	TRACECLK	-
	PB8	LPTIM1_ETR	-	-	-	-	-	SPI3_MOSI	-
	PB9	RTC_REFIN	-	-	-	-	-	SPI3_MISO	-
	PB12	-	TIM2_CH1	TIM2_ETR	-	-	-	-	USART1_TX
	PB15	-	-	-	-	I2C1_SMBA	-	I2C3_SMBA	-
C	PC13	-	-	-	-	-	-	-	-
	PC14	-	-	-	-	-	-	-	-
	PC15	-	-	-	-	-	-	-	-
H	PH3	-	-	-	-	-	-	-	-

1. For AF8 to AF15 refer to *Table 24*.

Table 24. Alternate function AF8 to AF15(1)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/PTA/SAI1	LPUART1	PTA/USART1/ USB/XSPI1	RF/SAI1/XSPI1	PTA	LPTIM2/ SAI1/XSPI1	LPTIM2/ TIM16/17/XSPI1	EVENTOUT
A	PA0	LPUART1_CTS	-	-	-	-	-	-	EVENTOUT
	PA1	LPUART1_RX	-	-	-	-	LPTIM2_CH2	TIM17_CH1	EVENTOUT
	PA2	LPUART1_TX	-	XSPI1_DQS	XSPI1_NCS	-	LPTIM2_CH1	TIM16_CH1	EVENTOUT
	PA5	-	-	USART1_TX	SAI1_SCK_A	-	AUDIOCLK	LPTIM2_ETR	EVENTOUT
	PA6	-	-	USART1_TX	SAI1_SD_A	-	SAI1_MCLK_A	-	EVENTOUT
	PA7	-	-	USART1_RX	-	-	SAI1_SCK_A	-	EVENTOUT
	PA8	-	-	USB_SOF	-	-	SAI1_FS_A	-	EVENTOUT
	PA9	LPUART1_RTS_DE	-	-	-	-	-	-	EVENTOUT
	PA10	LPUART1_RX	LPUART1_RTS	-	-	-	-	-	EVENTOUT
	PA11	-	-	PTA_ACTIVE	RF_ANTSW1	-	-	LPTIM2_CH1	EVENTOUT
	PA12	PTA_ACTIVE	-	PTA_STATUS	RF_ANTSW0	-	SAI1_SD_B	XSPI1_NCS	EVENTOUT
	PA13	-	-	PTA_PRIORITY	-	-	-	-	EVENTOUT
	PA14	-	-	PTA_STATUS	-	-	-	-	EVENTOUT
	PA15	-	-	PTA_STATUS	-	-	XSPI1_CLK	TIM17_BKIN	EVENTOUT
B	PB2	-	-	XSPI1_NCS	RF_ANTSW2	-	-	-	EVENTOUT
	PB3	-	-	PTA_ACTIVE	-	-	XSPI1_IO0	TIM17_CH1N	EVENTOUT
	PB4	SAI1_CK1	-	PTA_PRIORITY	XSPI1_IO1	PTA_ACTIVE	-	TIM17_CH1	EVENTOUT
	PB5	LPUART1_TX	-	XSPI1_IO2	-	-	-	-	EVENTOUT
	PB6	-	-	XSPI1_IO3	-	-	-	-	EVENTOUT
	PB8	LPUART1_CTS	-	-	XSPI1_IO2	-	-	TIM16_CH1N	EVENTOUT
	PB9	LPUART1_RTS_DE	-	-	XSPI1_IO3	-	LPTIM2_IN1	TIM16_CH1	EVENTOUT
	PB12	-	-	-	-	-	SAI1_SD_A	-	EVENTOUT
	PB15	LPUART1_CTS	LPUART1_RX	PTA_GRANT	RF_EXTPABYP1	-	-	TIM16_BKIN	EVENTOUT

Table 24. Alternate function AF8 to AF15[1] (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1/PTA/SAI1	LPUART1	PTA/USART1/ USB/XSPI1	RF/SAI1/XSPI1	PTA	LPTIM2/ SAI1/XSPI1	LPTIM2/ TIM16/17/XSPI1	EVENTOUT
C	PC13	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	EVENTOUT
H	PH3	LPUART1_RTS_DE	LPUART1_TX	PTA_GRANT	RF_EXTPABYP2	-	-	-	EVENTOUT

1. For AF0 to AF7 refer to *Table 23*.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

5.1 Device marking

Refer to "*Reference device marking schematics for STM32 microcontrollers and microprocessors*" (TN1433), available on *www.st.com*, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E", or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

5.2 UFQFPN32 package information (A0B8)

This UFQFPN is a 32-pin, 5 x 5 mm, 0.5 mm pitch ultrathin fine pitch quad flat package.

Note: Figure 11 and Figure 12 are not to scale.
Refer to the notes section for the list of notes on Figure 11, Table 25, and Table 26.

Figure 11. UFQFPN32 - Outline

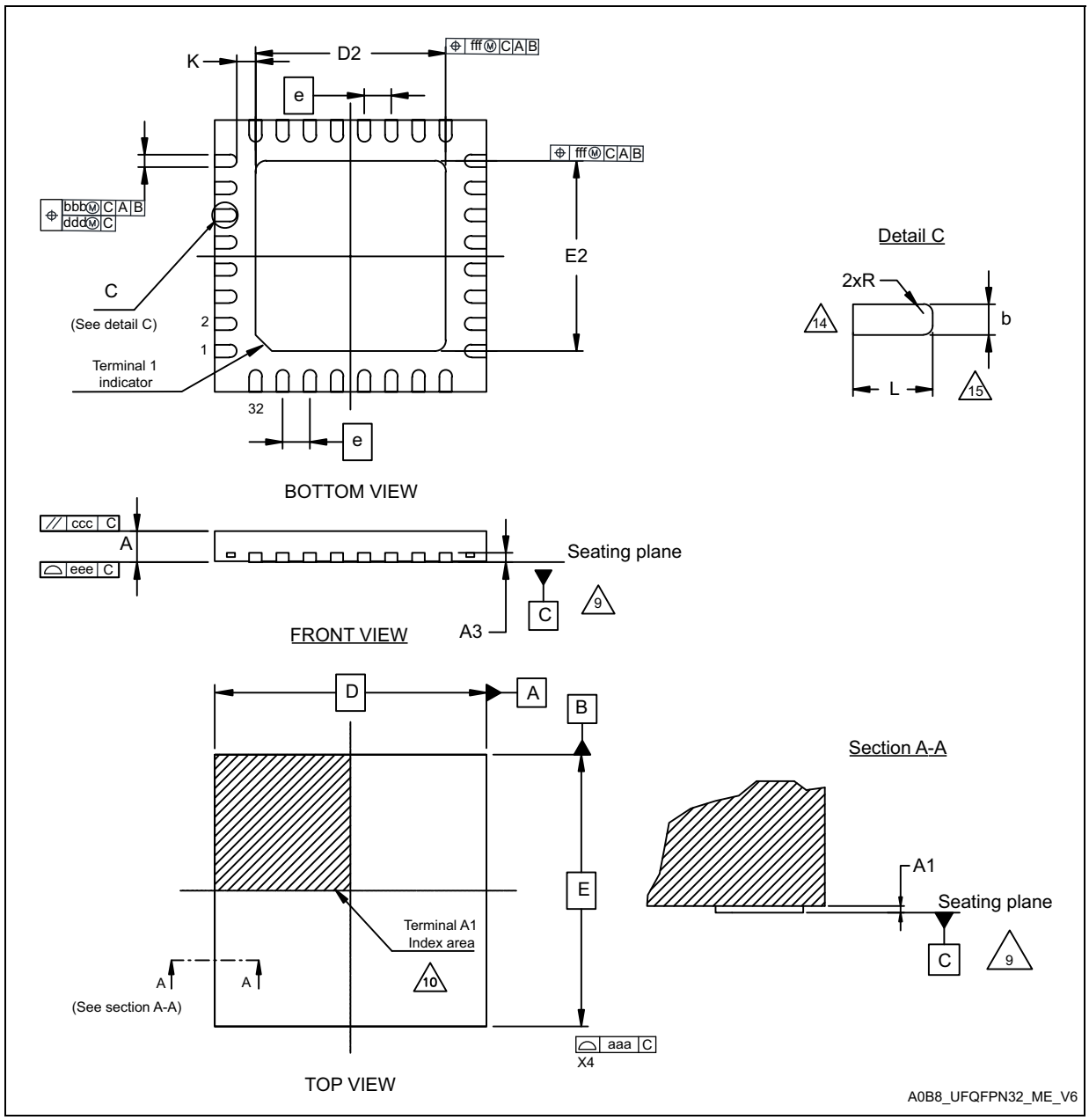


Table 25. UFQFPN32 - Mechanical data

Symbol	Millimeters			Inches[8]		
	Min	Typ	Max	Min	Typ	Max
A[2][3]	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1[4]	0.00	-	0.05	0.000	-	0.0020
b[6][15]	0.18	0.25	0.30	0.0071	0.0098	0.0118
D[7]	5.00 BSC			0.1969 BSC		
D2	3.40	3.50	3.60	0.1339	0.1378	0.1417
E[7]	5.00 BSC			0.1969 BSC		
E2	3.40	3.50	3.60	0.1339	0.1378	0.1417
e	0.50 BSC			0.0197 BSC		
N[12]	32					
L[15]	0.30	-	0.50	0.0118	-	0.0197
R	0.09	-	-	0.0035	-	-

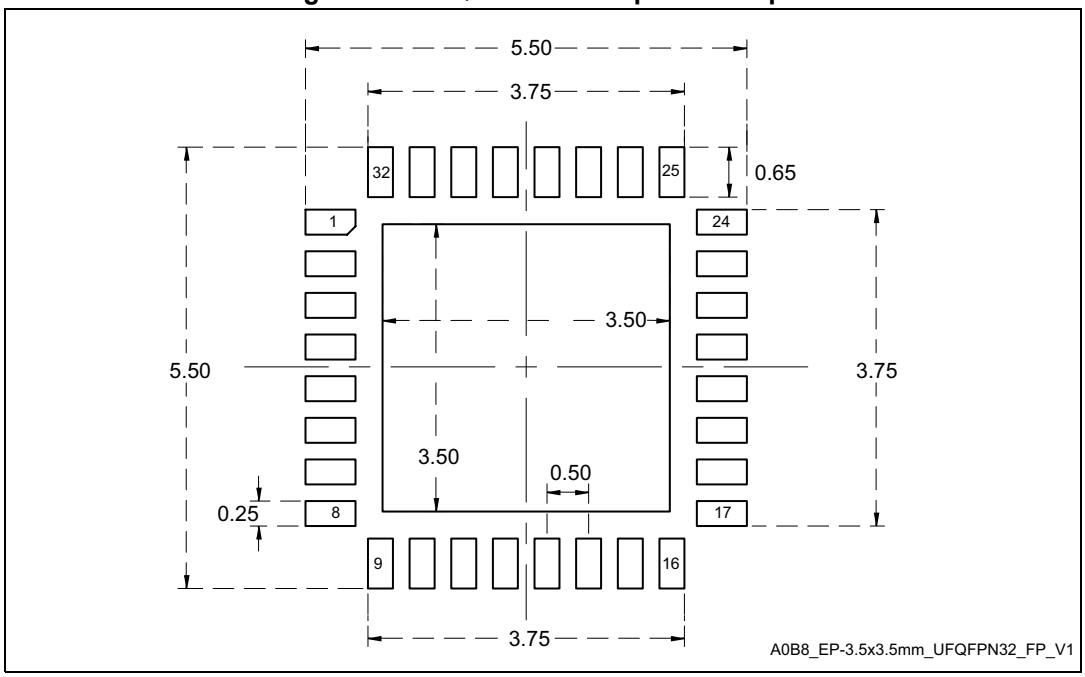
Table 26. Tolerance of form and position

Symbol	Millimeters	Inches[8]
aaa	0.15	0.0059
bbb	0.10	0.0039
ccc	0.10	0.0039
ddd	0.05	0.0020
eee	0.08	0.0315
fff	0.10	0.0039

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2018 except for European.
2. UFQFPN stands for ultra-thin fine pitch quad flat package no lead: A ≤ 0.60 mm / Fine pitch e ≤ 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is the vertical distance from the bottom surface of the plastic body to the nearest metallized package feature.
5. A3 is the distance from the seating plane to the upper surface of the terminals.
6. Dimension b applies to metallized terminal. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measured in that radius area.
7. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance.
8. Values in inches are converted from millimeters and rounded to four decimal digits.
9. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
10. Terminal A1 identifier and terminal numbering convention must conform to JEP95 SPP-002. Terminal A1 identifier must be located within the zone indicated on the outline drawing. Topside terminal A1 indicator may be a molded, or metallized feature. Optional indicator on bottom surface may be a molded, marked, or metallized feature.
11. ddd coplanarity zone applies to the exposed pad as well as the terminals.
12. N represents the total number of terminals.
13. K gives the minimum separation between any two terminals or the terminals and the edges of the exposed metal heat feature.
14. The inner edge of corner terminals may be chamfered or rounded to achieve minimum gap k. This feature should not affect the terminal width b, which is measured L/2 from the edge of the package body.
15. Dimension b and L are measured at the terminal planting surface.

Figure 12. UFQFPN32 - Footprint example

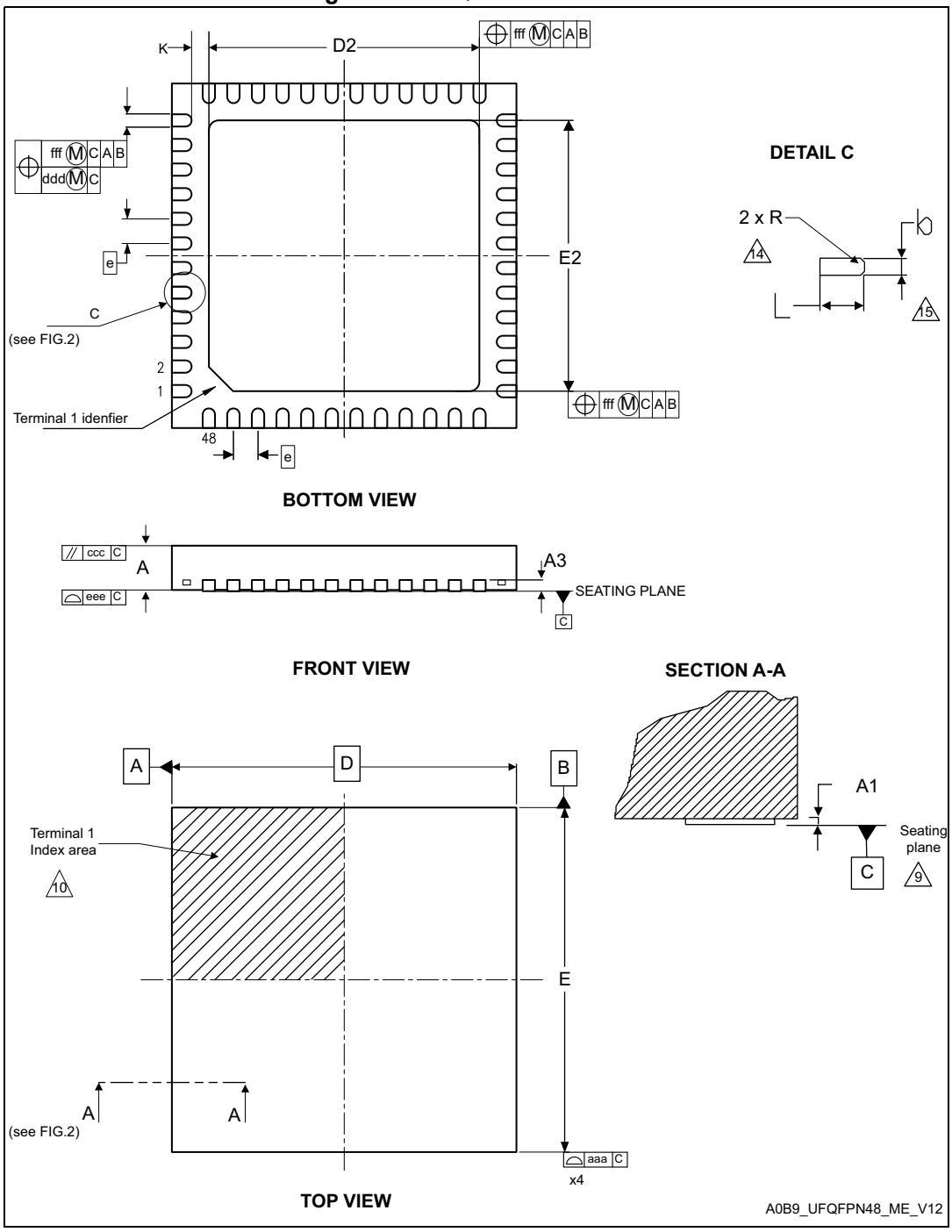


Note: Dimensions are expressed in millimeters.

5.3 UFQFPN48 package information (A0B9)

This UFQFPN is a 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package.

Figure 13. UFQFPN48 – Outline



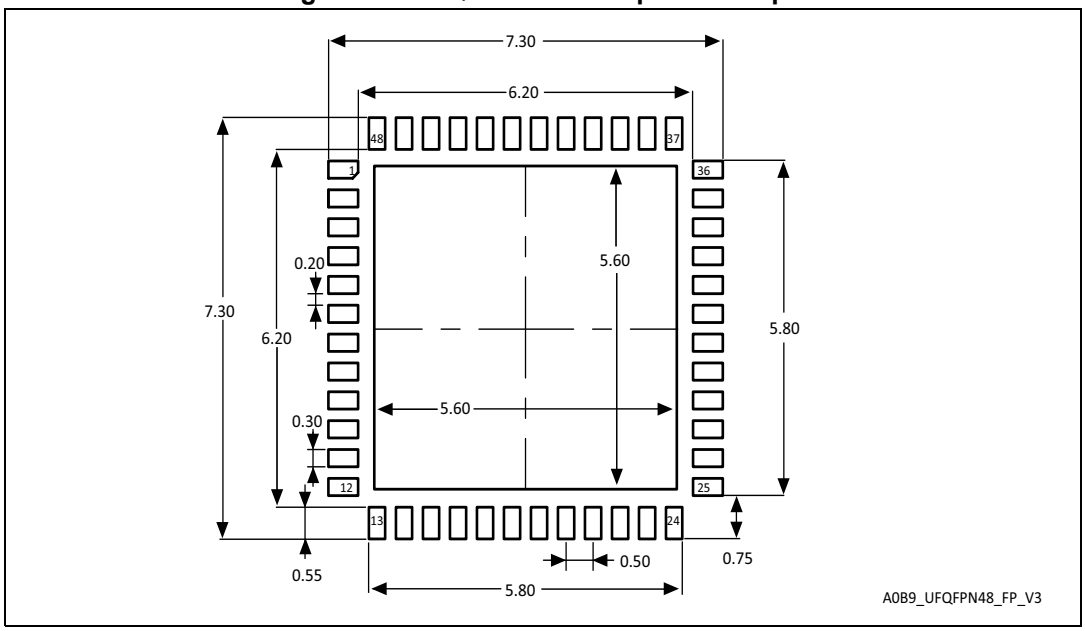
1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN48 package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 27. UFQFPN48 – Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.50	0.55	0.60	0.0197	0.0217	0.0236
A1	0.00	-	0.05	0.0000	-	0.0020
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D[2]	7.00 BSC			0.2756 BSC		
D2[3]	5.50	5.60	5.70	0.2165	0.2205	0.2244
E[2]	7.00 BSC			0.2756 BSC		
E2[3]	5.50	5.60	5.70	0.2165	0.2205	0.2244
e	0.50 BSC			0.0197 BSC		
N	48					
L	0.30	-	0.50	0.0118	-	0.0197
R	0.10	-	-	0.0039	-	-
aaa	0.15			0.0059		
bbb	0.10			0.0039		
ccc	0.10			0.0039		
ddd	0.05			0.0020		
eee	0.08			0.0031		
fff	0.10			0.0039		

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimensions D and E do not include mold protrusion, not exceed 0.15 mm.
3. Dimensions D2 and E2 are not in accordance with JEDEC.

Figure 14. UFQFPN48 – Footprint example

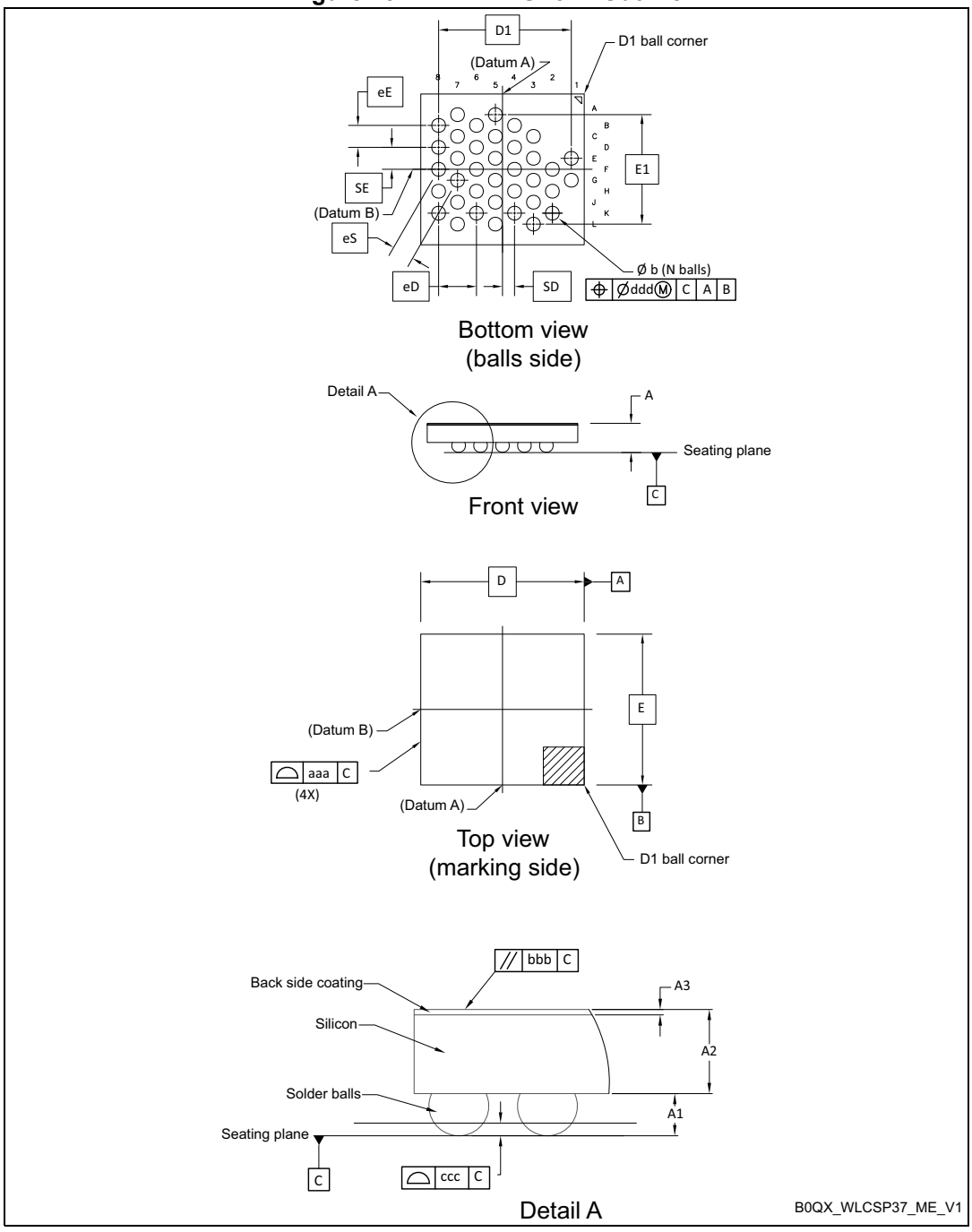


1. Dimensions are expressed in millimeters.

5.4 Thin WLCSP37 package information (B0QX)

This WLCSP is a 37-ball, 2.61 x 2.41 mm, 0.35 mm pitch, thin wafer level chip scale package.

Figure 15. Thin WLCSP37 - Outline



1. The drawing is not to scale.

Table 28. Thin WLCSP37 - Mechanical data

Symbol	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	0.50	-	-	0.0197
A1[3]	0.12	-	-	0.0047	-	-
A2	-	0.30	-	-	0.0118	-
A3	-	0.025	-	-	0.0010	-
b[4]	0.20	0.23	0.25	0.0079	0.0091	0.0098
D[5]	2.61 BSC			0.1028 BSC		
D1[5]	2.12 BSC			0.0835 BSC		
E[5]	2.41 BSC			0.0949 BSC		
E1[5]	1.75 BSC			0.0689 BSC		
eD[5][6]	0.61 BSC			0.0240 BSC		
eE[5][6]	0.35 BSC			0.0138 BSC		
eS[5][6]	0.35 BSC			0.0138 BSC		
SD[5][7]	0.19 BSC			0.0075 BSC		
SE[5][7]	0.35 BSC			0.0138 BSC		
N[8]	37					
aaa[9]	0.02			0.0008		
bbb[9]	0.06			0.0024		
ccc[9]	0.03			0.0012		
ddd[9]	0.015			0.0006		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. The profile height A is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
3. A1 is defined as the distance from the seating plane to the lowest point on the package body.
4. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to datum C.
5. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance.
6. e represents the solder balls grid pitch(es).
7. Basic dimensions SD and SE are defining the ball matrix position with respect to datums A and B.
8. N represents the total number of balls.
9. Tolerance of form and position drawing.

5.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the specified values.

T_J max (in Celsius degrees), can be calculated using the equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max)
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watt (this is the maximum chip internal power)

$P_{I/O}$ max represents the maximum power dissipation on output pins:

- $P_{I/O}$ max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DD} - V_{OH}) \times I_{OH})$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 29. Package thermal characteristics

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient**	UFQFPN32 - 5 mm x 5 mm	41.0	°C / W
		UFQFPN48 - 7 mm x 7 mm	30.5	
		Thin WLCSP37 - 2.61 mm x 2.41 mm	82.2	
Θ_{JB}	**Thermal resistance junction-board**	UFQFPN32 - 5 mm x 5 mm	22.9	
		UFQFPN48 - 7 mm x 7 mm	14.8	
		Thin WLCSP37 - 2.61 mm x 2.41 mm	52.1	
Θ_{JC}	**Thermal resistance junction-case**	UFQFPN32 - 5 mm x 5 mm	18.6	
		UFQFPN48 - 7 mm x 7 mm	11.4	
		Thin WLCSP37 - 2.61 mm x 2.41 mm	5.0	

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_A max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C and supply voltage V_{DD} = V_{DDA} = V_{DDRF} = 3 V. They are only given as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error lower than or equal to the value indicated (mean ± 2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines, and are not tested.

6.1.4 Loading capacitor

Unless otherwise specified, the loading conditions used for pin parameter measurement are shown in *Figure 16*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 17*.

Figure 16. Pin loading conditions

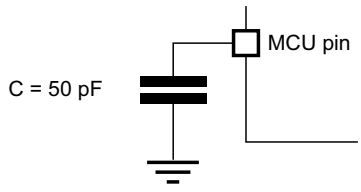
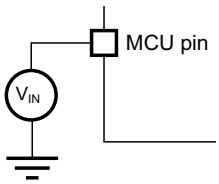


Figure 17. Pin input voltage



6.1.6 Power supply scheme

Figure 18. Power supply scheme with LDO

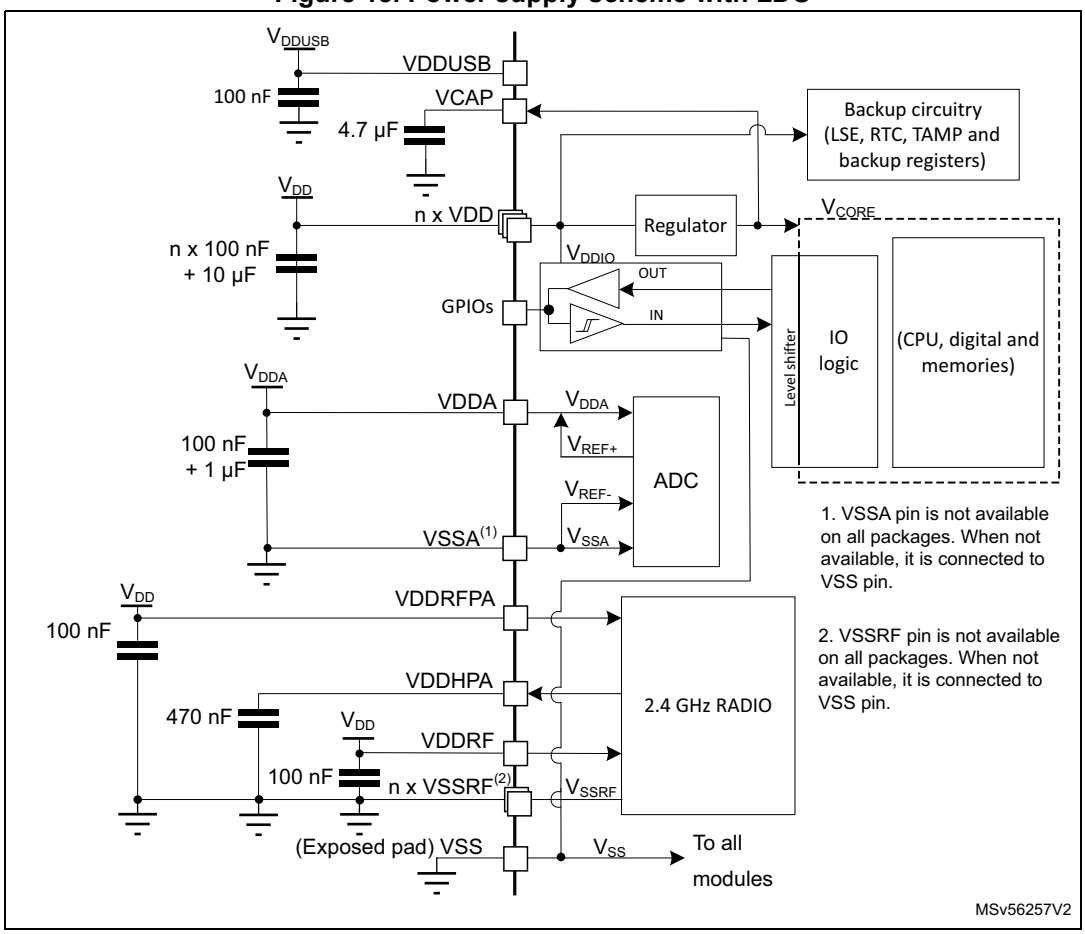


Figure 19. Power supply scheme with SMPS

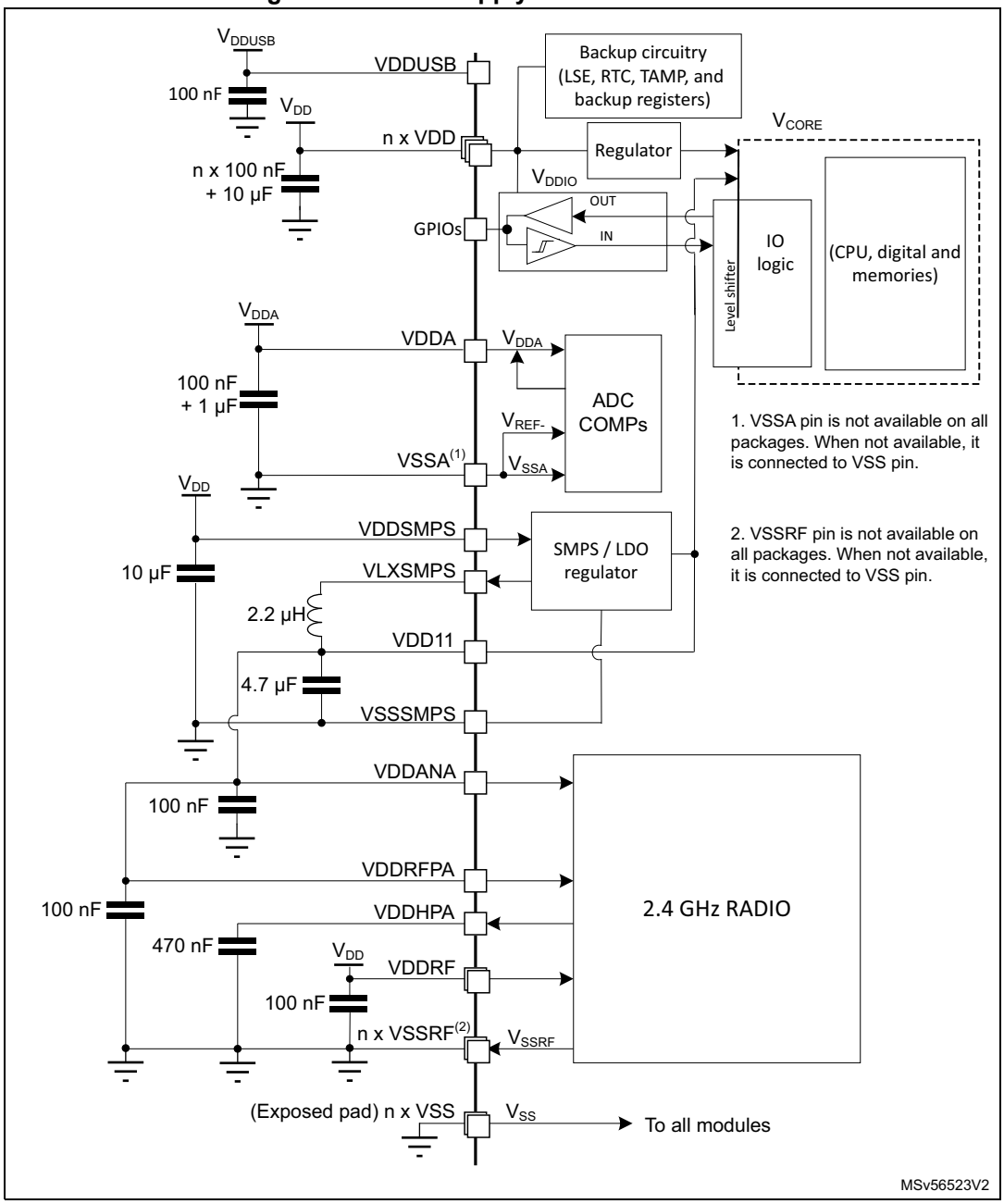
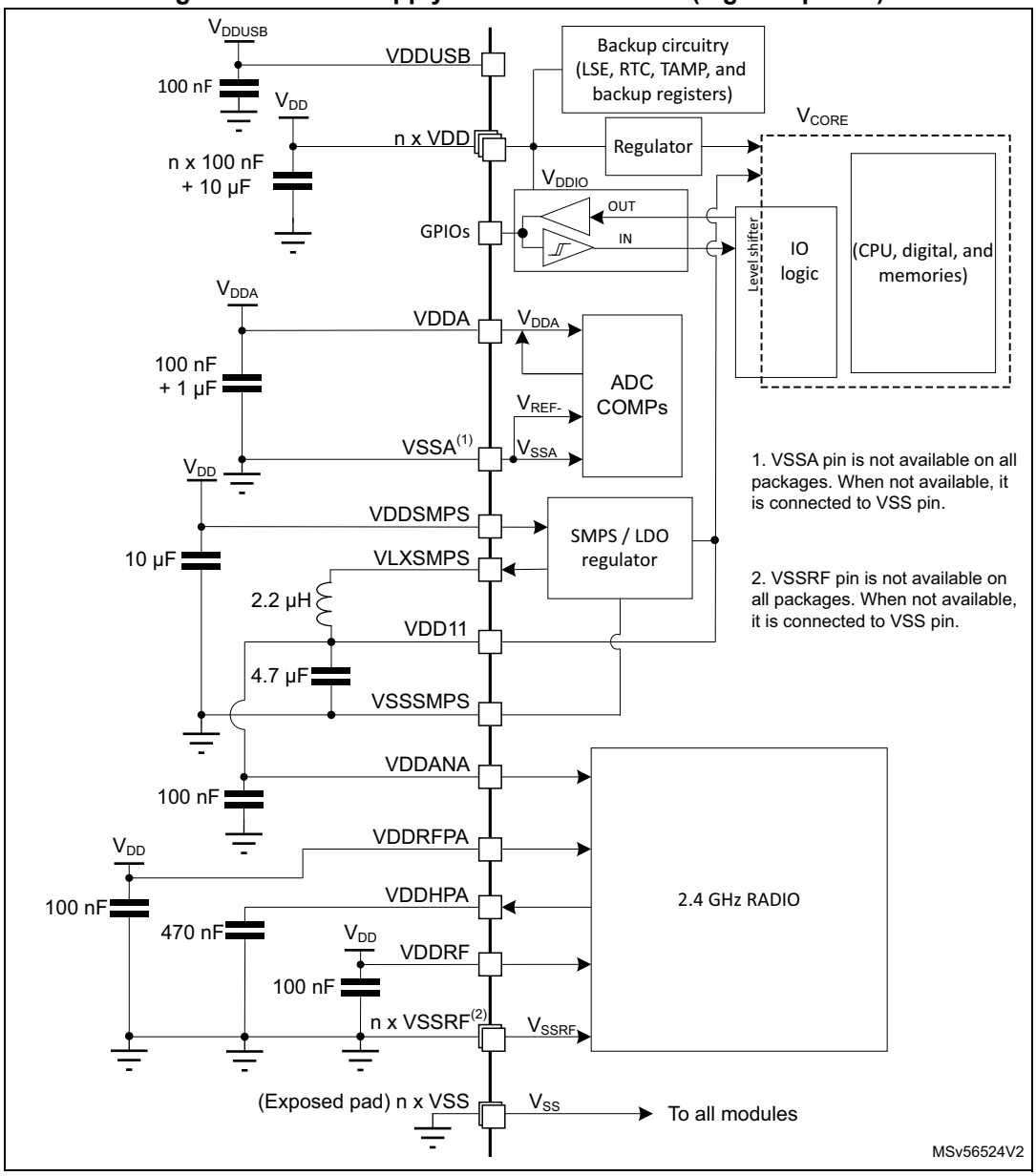


Figure 20. Power supply scheme with SMPS (high RF power)



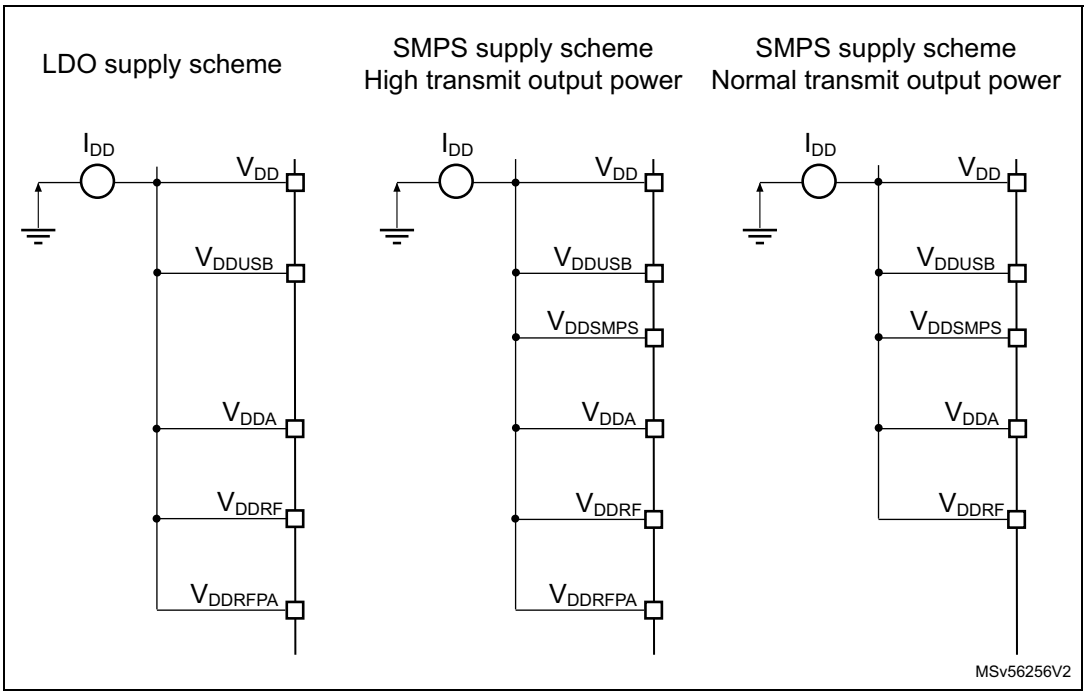
Caution: Each power supply pair (V_{DD} / V_{SS}, V_{DDA} / V_{SS}, V_{DDRFPA} / V_{SS}, V_{DDRF} / V_{SS}) must be decoupled with filtering ceramic capacitors as shown. These capacitors must be placed as close as possible to (or below) the appropriate pins to ensure correct device functionality.

Caution: V_{DD} and V_{DDRF} must be connected to the same supply.

6.1.7 Current consumption measurement

The I_{DD} parameters in the tables in the next sections represent the total MCU consumption, including the current supplying V_{DD}, V_{DDUSB}, V_{DDA}, V_{DDRF}, V_{DDRFPA}, and V_{DDSMPS} (if the device embeds the SMPS), or the total 2.4 GHz RADIO current supplying V_{DDRF} and V_{DDRFPA}.

Figure 21. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 30*, *Table 31*, and *Table 32* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 30. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DDX} - V_{SS}	External main supply voltage (including V_{DDUSB}, V_{DDA}, V_{DDRF}, V_{DDRFPA}, V_{DDANA}, V_{DDSMPS})	-0.3	4.0	V
V_{IN}(2)	Input voltage on FT_ (any option) pins	V_{SS} - 0.3	min (min (V_{DD}, V_{DDUSB}, V_{DDA}) + 4.0, 6.0)(3)(4)	
	Input voltage on any other pin		4.0	

Table 30. Voltage characteristics(1) (continued)

Symbol	Ratings	Min	Max	Unit
$\lvert\Delta V_{DDx}\rvert$	Variations between different VDDX power pins of the same domain	-	50.0	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50.0	

1. All main power (VDD, VDDUSB, VDDA, VDDRF, VDDRFPA, VDDANA, VDDSMPS) and ground (VSS, VSSA, VSSRF, VSSSMPS) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 31* for the maximum allowed injected current values.
3. To sustain a voltage higher than 4 V, the internal pull-up/pull-down resistors must be disabled.
4. This formula applies only to power supplies related to the I/O structure described by the pin definition table.

Table 31. Current characteristics

Symbol	Ratings	Max	Unit
$\sum IV_{DD}$	Total current into sum of all V_{DD} power lines (source)(1)	200	mA
$\sum IV_{SS}$	Total current out of sum of all V_{SS} ground lines (sink)(1)	200	
$IV_{DD(PIN)}$	Maximum current into each VDD power pin (source)(1)	100	
$IV_{SS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	100	
I_{IO}	Output current sunk by any I/O and control pin	20	
$\sum I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	120	
	Total output current sourced by sum of all I/Os and control pins(2)	120	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xxx, TT_xx, RST pins	-5/+0	
$\sum\lvert I_{INJ(PIN)}\rvert$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. All main power (VDD, VDDUSB, VDDA, VDDRF, VDDRFPA, VDDANA, VDDSMPS) and ground (VSS, VSSA, VSSRF, VSSSMPS) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. Positive injection (when $V_{IN} > V_{DD}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 30* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum\lvert I_{INJ(PIN)}\rvert$ is the absolute sum of the negative injected currents (instantaneous values).

Table 32. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_{JMAX}	Maximum junction temperature	140	

6.3 Operating conditions

6.3.1 Summary of main performance

Table 33. Main performance at V_{DD} = 3.3 V

Parameter			Test conditions	Typ	Unit
I_{DD}	Core current consumption		Standby (32 Kbytes RAM retention)	0.40	µA
			Stop 1	4.57	
			Stop 2	N/A	
			Stop 3	N/A	
			Sleep (V_{DD} = 3.0 V, 16 MHz)	0.21	mA
			Run (64 MHz)	2.0	
			Radio BLE Rx 1 Mbps(1)	3.58	
			Radio BLE Tx 0 dBm output power(1)	4.65	
I_{DD}	Peripheral current consumption	BLE	Advertising using Standby mode(2) (Tx = 0 dBm; 31 bytes, period 1.28 s, 3 channels)	7.6	µA
			Advertising using Standby mode(2) (Tx = 0 dBm, 6 bytes; period 10.24 s, 3 channels)	2.04	

1. Power consumption including RF subsystem and digital processing.
2. Power consumption integrated over 100 s, including Cortex-M33, 2.4 GHz RADIO subsystem and digital processing.

6.3.2 General operating conditions

Table 34. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	-	1.71(1)	-	3.6	V
V_{DDUSB}	USB supply voltage	USB used	3.0	-	3.6	V
		USB not used	0	-		
V_{DDSMPS}	Supply voltage for internal SMPS step-down converter	-	V_{DD}			V
V_{DDA}	Analog supply voltage	ADC used	1.62	-	3.6	V
V_{DDRF}	RF operating voltage	-	1.71	-	3.6	V
V_{DDRFPA}	RF power amplifier operating voltage	V_{DDRFPA} supply must be equal or lower than V_{DDRF}.	1.15	-	3.6	V

Table 34. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDANA}	RF analog supply	V_{DDANA} supply must be equal or lower than V_{DDRF}.	1.15	-	3.6	V
V_{IN}	I/O input voltage	All I/Os FT_ (any option) pins	-0.3	-	min (min (V_{DD}, V_{DDA}) + 3.6, 5.5)(2)(3)	
		TT I/O pins			V_{DD} + 0.3	
V_{CORE}	Internal regulator ON	Range 1	1.15	1.21	1.27	
		Range 1.5	1.05	1.1	1.16	
		Range 2	0.81	0.9	0.99	
f_{HCLK}	Internal AHB1, AHB2, and AHB4 clock frequency	Range 1	-	-	64	MHz
		Range 1.5	-	-	64	
		Range 2	-	-	16	
f_{PCLK}	Internal APB1, APB2, and APB7 clock frequency	Range 1	-	-	64	
		Range 1.5	-	-	64	
		Range 2	-	-	16	
f_{HCLK5}	Internal AHB5 clock frequency	Range 1	-	-	32	
		Range 1.5	-	-	32	
		Range 2	-	-	12	
Δf_{HCLK1}	Internal AHB1, AHB2 and AHB4 clock incremental frequency step(4)	-	-	-	64	MHz
P_D	Power dissipation at T_A = 85 °C (suffix 6 version) or T_A = 105 °C (suffix 7 version)	See *Section 5.5* for appropriate thermal resistance and package. Power dissipation is calculated according to ambient temperature (T_A), maximum junction temperature (T_J), and selected thermal resistance.				mW
T_A	Ambient temperature	Suffix 6 version	–40	-	85	°C
		Suffix 7 version			105	
T_J	Junction temperature range	Suffix 6 version	–40	-	105	°C
		Suffix 7 version(5)			125	

1. When RESET is released functionality is guaranteed down to V_{BORx} min.
2. Applies only on the power supplies related to the I/O structure described by the pin definition table. The maximum I/O input voltage is the smallest value between min (V_{DD}, V_{DDA}, V_{DDUSB}) +3.6 V and 5.5 V.
3. For operation with voltages higher than min (V_{DD}, V_{DDA}, V_{DDUSB}) +3.6 V the internal pull-up and pull-down resistors must be disabled.
4. Without system clock frequency step limiting.
5. Junction temperature above 105 °C must be limited to 30% of 10 years life time.

6.3.3 RF characteristics

Table 35. RF Bluetooth® LE transmitter characteristics(1)

Symbol	Parameter		Test conditions	Standard	Min	Typ	Max	Unit
P_{txmax}	Maximum output power		V_{DDRFPA} ≥ 2.50 V	-	-	9.5	-	dBm
			V_{DDRFPA} ≥ 1.71 V	-	-	7.5	-	
P_{txmin}	Minimum output power		-	-	-	-20	-	
ΔP_{tx}	Output power step		-	-	0.5	1	2	dB
$P_{freqband}$	Output power ± variation over the frequency band		P_{txmax} max setting	-	-	0.4	-	
P_{temp}	Output power ± variation over the temperature		P_{txmax} max setting -40 °C ≤ T_J ≤ +105 °C	-	-	2.9	-	
$P_{2ndHARM}$	Second harmonic		P_{txmax} max setting	-	-	-69.5	-	dBm
$P_{3rdHARM}$	Third harmonic		P_{txmax} max setting	-	-	-70.5	-	
$OBSE_{1Mbps}$	Out of band spurious emission 1 Mbps	< 1 GHz	P_{txmax} max setting	(2)	-	-51	-	
		≥ 1 GHz	P_{txmax} max setting		-	-43	-	
$OBSE_{2Mbps}$	Out of band spurious emission 2 Mbps	< 1 GHz	P_{txmax} max setting	(2)	-	-54	-	
		≥ 1 GHz	P_{txmax} max setting		-	-45	-	

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.
2. Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

Table 36. Generic RF receiver characteristics(1)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
$Rssi_{max}$	RSSI maximum value	-	-	-	-32	-	dBm
$Rssi_{min}$	RSSI minimum value	-	-	-	-75	-	
$Rssi_{accu}$	RSSI accuracy	-	-	-	±6	-	dB

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 37. RF Bluetooth® LE characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
F_{op}	Frequency channel operating band	-	2402	-	2480	MHz
ΔF	Delta frequency	-	-	250	-	kHz
Rgfsk	On air data rate	-	0.125	-	2	Mbps
PLLres	RF channel spacing	-	-	2	-	MHz

Table 38. RF transmitter Bluetooth® LE characteristics(1)

Symbol	Parameter		Test conditions	Standard	Min	Typ	Max	Unit
$BW6dB_{1Mbps}$	6 dB signal bandwidth		P_{txmax} max setting	-	-	665	-	kHz
$BW6dB_{2Mbps}$	6 dB signal bandwidth		P_{txmax} max setting	-	-	1142	-	
$IBSE_{1Mbps}$	In band spurious emission	2 MHz	-	-20	-	-41	-20	dBm
		≥ 3 MHz	-	-30	-	-47.5	-30	
$IBSE_{2Mbps}$	In band spurious emission	4 MHz	-	-20	-	-42.5	-20	dBm
		5 MHz	-	-20	-	-44	-20	
		≥ 6 MHz	-	-30		-45	-30	
f_d	Frequency drift		-	±50	-50	-	+50	kHz
dr_{max}	Maximum drift rate	Uncoded	-	±20	-20	-	+20	kHz/ 50 µs
		Coded	-	±19.2	-19.2	-	+19.2	
fo	Frequency offset		-	±150	-150	-	+150	kHz
$\Delta f1_{1Mbps}$	Frequency deviation average 1 Mbps		-	225 - 275	225	-	275	
$\Delta f1_{2Mbps}$	Frequency deviation average 2 Mbps		-	450 - 550	450	-	550	
$\Delta f1_{CodedS8}$	Frequency deviation average Coded S = 8		-	225 - 275	225	-	275	
$\Delta f2_{1Mbps}$	Frequency deviation 99.9% 1 Mbps		-	185	185	-	-	
$\Delta f2_{2Mbps}$	Frequency deviation 99.9% 2 Mbps		-	370	370	-	-	

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 39. RF receiver Bluetooth® LE characteristics (1)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
P_{rxmax}	Maximum input signal	PER ≤ 30.8%	-10	-	6	-	dBm
$P_{sens2Mbps}$(2)	Sensitivity 2 Mbps	SMPS bypass(3)	-70	-	-93	-	
		SMPS on(3)	-	-	-	-	
$P_{sens1Mbps}$(2)	Sensitivity 1 Mbps	SMPS bypass(3)	-70	-	-96	-	
		SMPS on(3)	-	-	-	-	
$P_{sens500kbps}$(2)	Sensitivity 500 kbps	SMPS bypass(3)	-75	-	-99	-	
		SMPS on(3)	-	-	-	-	
$P_{sens125kbps}$(2)	Sensitivity 125 kbps	SMPS bypass(3)	-82	-	-102	-	
		SMPS on(3)	-	-	-	-	
$P_{IMD1Mbps}$	Intermodulation 1 Mbps	|f2 - f1| = 3 MHz	-50	-50	-37	-	
		|f2 - f1| = 4 MHz	-	-50	-27	-	
		|f2 - f1| = 5 MHz	-	-50	-28	-	
$P_{OBB1Mbps}$	Out of band blocking (for desired signal at -67 dBm and 1 Mbps)	30 to 2000 MHz	-30	-30	-10	-	
		2000 to 2399 MHz	-35	-35	-22	-	
		2484 to 2999 MHz	-35	-35	-18	-	
		3 to 12.75 GHz	-30	-30	-10	-	
$P_{IMD2Mbps}$	Intermodulation 2 Mbps	|f2 - f1| = 3 MHz	-50	-50	-37	-	
		|f2 - f1| = 4 MHz	-	-50	-30	-	
		|f2 - f1| = 5 MHz	-	-50	-30	-	
$P_{OBB2Mbps}$	Out of band blocking (for desired signal at -67 dBm and 2 Mbps)	30 to 2000 MHz	-30	-30	-10	-	
		2000 to 2399 MHz	-35	-35	-33	-	
		2484 to 2999 MHz	-35	-35	-19	-	
		3 to 12.75 GHz	-30	-30	-10	-	

Table 39. RF receiver Bluetooth® LE characteristics (1) (continued)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
$C/Ico_{125kbps}$	Co-channel rejection 125 kbps	-	12	-	3	-	dB
$C/I_{125kbps}$	Adjacent channel interference 125 kbps	Adj = ±1 MHz	6	-	-2	6	
		Adj = 2 MHz	-26	-	-38	-26	
		Adj-Image = -2 MHz	-18	-	-27	-18	
		Adj ≥ 3 MHz	-36	-	-43	-36	
		Adj = -3 MHz	-24	-	-28	-24	
		Adj ≤ -4 MHz	-36	-	-43	-36	
$C/Ico_{250kbps}$	Co-channel rejection 250 kbps	-	17	-	5	17	
$C/I_{500kbps}$	Adjacent channel interference 500 kbps	Adj = ±1 MHz	11	-	-2	11	
		Adj = 2 MHz	-21	-	-34	-21	
		Adj-Image = -2 MHz	-13	-	-26	-13	
		Adj ≥ 3 MHz	-31	-	-39	-31	
		Adj = -3 MHz	-19	-	-27	-19	
		Adj ≤ -4 MHz	-31	-	-37	-31	
C/Ico_{1Mbps}	Co-channel rejection 1 Mbps	-	21	-	8	21	
C/I_{1Mbps}	Adjacent channel interference 1 Mbps	Adj = ±1 MHz	15	-	0	15	
		Adj = 2 MHz	-17	-	-38	-17	
		Adj-Image = -2 MHz	-9	-	-23	-9	
		Adj ≥ 3 MHz	-27	-	-36	-27	
		Adj = -3 MHz	-15	-	-27	-15	
		Adj ≤ -4 MHz	-27	-	-38	-27	
C/Ico_{2Mbps}	Co-channel rejection 2 Mbps	-	21	-	8	21	
C/I_{2Mbps}	Adjacent channel interference 2 Mbps	Adj = ±2 MHz	15	-	0	15	
		Adj = 4 MHz	-17	-	-35	-17	
		Adj-Image = -4 MHz	-9	-	-23	-9	
		Adj = ≥ 6 MHz	-27	-	-33	-27	
		Adj = -6 MHz	-15	-	-26	-15	
		Adj = ≤ -8 MHz	-27	-	-34	-27	

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.
2. With ideal transmitter.
3. The payload length used in all receiver tests is 37 bytes which means that the limit for each parameter is reached for a BER of 0.1% (PER of 30.8%), as defined in the Bluetooth® LE core specification.

Table 40. RF Bluetooth® LE power consumption for V_{DD} = 3.3 V(1)(2)

Symbol	Parameter	Typ	Unit
I_{tx}	Tx 0 dBm output power consumption (LDO)	10.46	mA
	Tx 0 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD)	5.19	
	Tx 0 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD11)	4.65	
	Tx +10 dBm output power consumption (LDO)	20.98	
	Tx +10 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD)	19.41	
I_{rx}	Rx consumption 1 Mbps (LDO)	7.53	
	Rx consumption 1 Mbps (SMPS ON, VDDRFPA connected to VDD)	4.65	
	Rx consumption 1 Mbps (SMPS ON, VDDRFPA connected to VDD11)	3.58	
	Rx consumption 2 Mbps (LDO)	8.34	
	Rx consumption 2 Mbps (SMPS ON, VDDRFPA connected to VDD)	4.98	
	Rx consumption 2 Mbps (SMPS ON, VDDRFPA connected to VDD11)	3.98	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Power consumption including 2.4 GHz RADIO subsystem and digital processing, voltage scaling range 1.5.

6.3.4 RF IEEE802.15.4 characteristics

Table 41. RF IEEE802.15.4 characteristics(1)

Symbol	Parameter	Conditions	Standard	Min	Typ	Max	Unit
F_{op}	Frequency channel operating band	-	-	2405	-	2480	MHz
ΔF	Delta frequency	-	-	-	5	-	
Roqpsk	On air data rate	-	-		250	-	kbps
PLLres	RF channel spacing	-	-	-	5	-	MHz

1. Guaranteed by characterization results, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 42. RF transmitter IEEE802.15.4 characteristics(1)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
P_{txmax}	Maximum output power	V_{DDRFPA} ≥ 2.50 V	-	-	9.5	-	dBm
		V_{DDRFPA} ≥ 1.71 V	-	-	7.5	-	
P_{txmin}	Minimum output power	-	-	-	-20	-	
ΔP_{tx}	Output power step	-	-	0.5	1	2	dB
$P_{freqband}$	Output power ± variation over the frequency band	P_{txmax} max setting	-	-	0.4	-	
P_{temp}	Output power ± variation over the temperature	P_{txmax} max setting -40 °C ≤ T_J ≤ +130 °C	-	-	2.9	-	

Table 42. RF transmitter IEEE802.15.4 characteristics(1) (continued)

Symbol	Parameter	Test conditions	Standard	Min	Typ	Max	Unit
$P_{2ndHARM}$	Second harmonic	P_{txmax} max setting	-	-	-69.5	-	dBm
$P_{3rdHARM}$	Third harmonic	P_{txmax} max setting	-	-	-70.5	-	

1. Evaluated by characterization, not tested in production, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 43. RF receiver IEEE802.15.4 characteristics(1)

Symbol	Parameter	Conditions	Standard	Min	Typ	Max	Unit
P_{rxmax}	Maximum input signal	PER ≤ 1%	-20	-	-20	-	dBm
$P_{sens250kbps}$	Sensitivity 250 kbps (LDO)	PER ≤ 1%	-85	-	-100	-	
	Sensitivity 250 kbps (SMPS ON)		-85	-	-100	-	
C/I_{adj}	Adjacent channel rejection	-	0	-	10	-	dB
C/I_{alt}	Alternate channel rejection	-	30	-	30	-	

1. Guaranteed by characterization results, unless otherwise specified. Measured in conducted mode, based on reference design (see AN5165), using output power specific external RF filter and impedance matching networks to interface with a 50 Ω antenna.

Table 44. RF IEEE802.15.4 power consumption for V_{DD} = 3.3 V(1)(2)

Symbol	Parameter	Typ	Unit
I_{tx}	Tx 0 dBm output power consumption (LDO)	13.6	mA
	Tx 0 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD)	6.8	
	Tx 0 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD11)	6.3	
	Tx +10 dBm output power consumption (LDO)	24.5	
	Tx +10 dBm output power consumption (SMPS ON, VDDRFPA connected to VDD)	21.8	
I_{rx}	Rx consumption (LDO)	10.7	
	Rx consumption (SMPS ON, VDDRFPA connected to VDD)	6.1	
	Rx consumption (SMPS ON, VDDRFPA connected to VDD11)	5.2	

1. Guaranteed by characterization results, unless otherwise specified.
2. Power consumption including 2.4 GHz RADIO subsystem and digital processing, voltage scaling range 1.

6.3.5 Operating conditions at power-up/power-down

The parameters in *Table 45* are evaluated by characterization under ambient temperature and supply voltage conditions summarized in *Table 34*.

Table 45. Operating conditions at power-up/power-down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate	ULPMEN = 0	20	∞	
		Standby mode with ULPMEN = 1	250	∞	ms/V

1. Evaluated by characterization, not tested in production, unless otherwise specified.

6.3.6 Embedded reset and power control block characteristics

The parameters in *Table 46* are derived under ambient temperature and supply voltage conditions summarized in *Table 34*.

Table 46. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset temporization after V_{BOR0} threshold detection	V_{DD} rising	-	-	900	µs
V_{BOR0}(2)	Brown-out reset threshold 0	V_{DD} rising	1.60	1.66	1.71	V
		V_{DD} falling	1.58	1.64	1.69	
V_{BOR1}(2)	Brown-out reset threshold 1	V_{DD} rising	1.98	2.08	2.17	
		V_{DD} falling	1.90	2.00	2.10	
V_{BOR2}(2)	Brown-out reset threshold 2	V_{DD} rising	2.18	2.29	2.39	
		V_{DD} falling	2.08	2.18	2.25	
V_{BOR3}(2)	Brown-out reset threshold 3	V_{DD} rising	2.48	2.59	2.70	
		V_{DD} falling	2.39	2.50	2.61	
V_{BOR4}(2)	Brown-out reset threshold 4	V_{DD} rising	2.76	2.88	3.00	
		V_{DD} falling	2.67	2.79	2.90	

Table 46. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}(2)	Programmable voltage detector threshold 0	V_{DD} rising	2.03	2.13	2.23	V
		V_{DD} falling	1.93	2.03	2.12	
V_{PVD1}(2)	PVD threshold 1	V_{DD} rising	2.18	2.29	2.39	
		V_{DD} falling	2.08	2.18	2.28	
V_{PVD2}(2)	PVD threshold 2	V_{DD} rising	2.33	2.44	2.55	
		V_{DD} falling	2.23	2.34	2.44	
V_{PVD3}(2)	PVD threshold 3	V_{DD} rising	2.47	2.59	2.70	
		V_{DD} falling	2.39	2.50	2.61	
V_{PVD4}(2)	PVD threshold 4	V_{DD} rising	2.60	2.72	2.83	
		V_{DD} falling	2.50	2.62	2.73	
V_{PVD5}(2)	PVD threshold 5	V_{DD} rising	2.76	2.88	3.00	
		V_{DD} falling	2.66	2.78	2.90	
V_{PVD6}(2)	PVD threshold 6	V_{DD} rising	2.83	2.96	3.08	
		V_{DD} falling	2.76	2.88	3.00	
V_{hyst_BOR0}(2)	BOR0 hysteresis voltage	-	-	20	-	mV
$V_{hyst\_BOR\_PVD}$(2)	BOR1, 2, 3, 4 and PVD hysteresis voltage	-	-	80	-	
$t_{sampling\_BOR0}$(2)	BOR0 ultra-low-power sampling monitoring period	ULPMEN = 1	-	12	30	ms
$I_{DD\_BOR\_PVD}$(1)	BOR1, 2, 3, 4 and PVD consumption from V_{DD}, and additional BOR0 consumption for ULPMEN = 0 vs. ULPMEN = 1 (3)	-	-	1.7	2.5	µA

1. Specified by design, not tested in production.
2. Evaluated by characterization, not tested in production.
3. BOR0 is enabled in all modes, its consumption is therefore included in the supply current characteristics tables.

6.3.7 Embedded voltage reference

The parameters in *Table 47* are derived under ambient temperature and supply voltage conditions summarized in *Table 34*.

Table 47. Embedded internal voltage reference

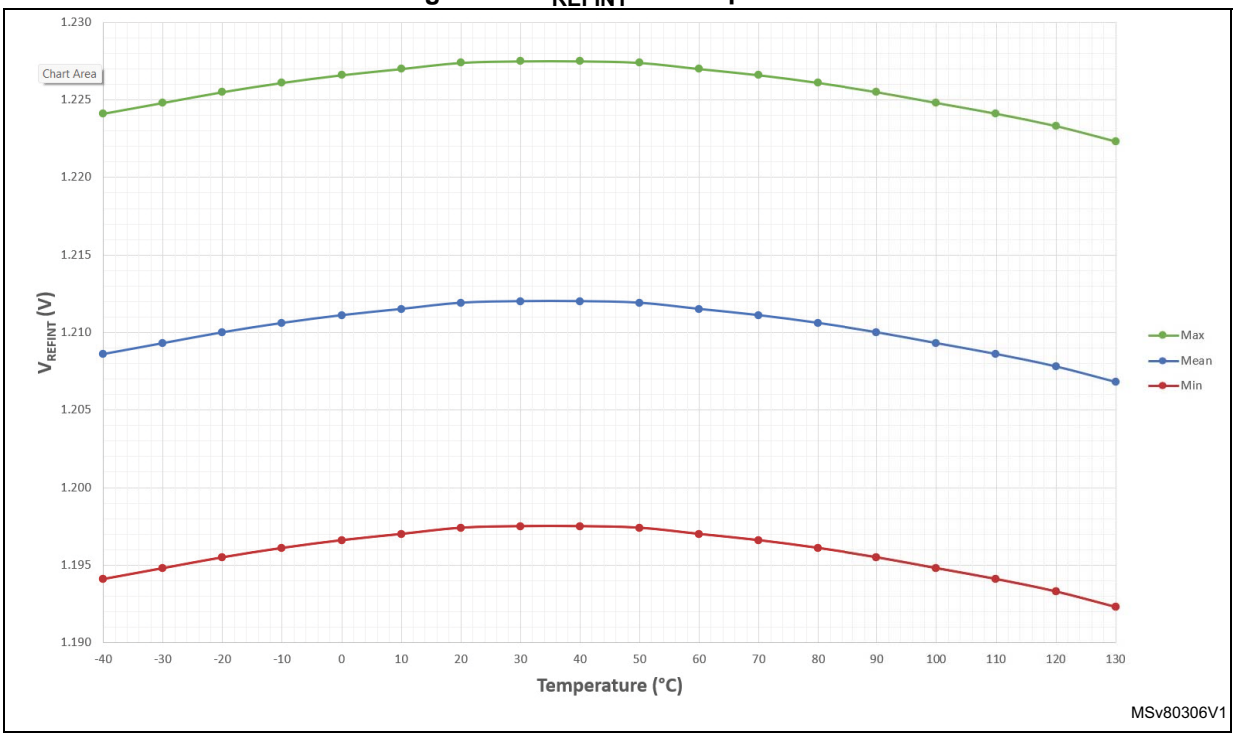
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}(1)	Internal reference voltage	Range 1	1.175	1.209	1.243	V
		Range 1.5	1.175	1.209	1.243	V
		Range 2 and low-power modes	1.170	1.206	1.248	V
$t_{S\_vrefint}$(2)(3)	ADC sampling time when reading the internal reference voltage	-	11.25	-	-	µs

Table 47. Embedded internal voltage reference (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{start\_vrefint}$(2)	Start time of reference voltage buffer when ADC is enabled	-	-	4	6	µs
$I_{DD(VREFINTBUF)}$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	1.5	2.1	µA
ΔV_{REFINT}(4)	Internal reference voltage spread over the temperature range	V_{DD} = 3 V –40 °C ≤ T_J ≤ +130 °C	-	6	19	mV
T_{Coeff}(4)	Temperature coefficient	V_{DD} = 3 V –40 °C ≤ T_J ≤ +130 °C	-	84	155	ppm/°C
A_{Coeff}(2)	Long term stability	1000 hours, T = 25 °C	-	400	-	ppm
$V_{DDCoeff1}$(4)	Voltage coefficient	3.0 V ≤ V_{DD} ≤ 3.6 V –40 °C ≤ T_J ≤ +130 °C	-	600	2300	ppm/V
$V_{DDCoeff2}$(4)	Voltage coefficient	1.8 V ≤ V_{DD} ≤ 3.6 V –40 °C ≤ T_J ≤ +130 °C	-	270	1350	ppm/V

1. VREFINT does not consider package and soldering effects.
2. Specified by design, not tested in production.
3. The shortest sampling time for the application can be determined by multiple iterations.
4. Evaluated by characterization, not tested in production

Figure 22. V_{REFINT} vs. temperature



6.3.8 Supply current characteristics

The current consumption is measured as described in *Section 6.1.7*. It depends upon several parameters, such as operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequency, I/O pin switching rate, program location in memory, and executed binary code.

Typical and maximum current consumption

The MCU is put under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled, except when otherwise mentioned
- The flash memory and SRAM access time is adjusted with the minimum wait states number, depending upon the f_{HCLK} frequency (refer to tables in the reference manual).
- When the peripherals are enabled $f_{PCLKx} = f_{HCLK1}$
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Voltage range 1 and range 1.5 for 16 MHz < f_{HCLK1} ≤ 64 MHz and 12 MHz < f_{HCLK5} ≤ 32 MHz
  - Voltage range 2 for f_{HCLK1} ≤ 16 MHz and f_{HCLK5} ≤ 12 MHz

The parameters given in *Table 48* and *Table 49* are evaluated by characterization under ambient temperature and supply voltage conditions summarized in *Table 34*.

Table 48. Current consumption in Run modes on LDO, code with data processing running from flash memory, Cache ON (1-way), prefetch OFF, V_{DD} = 3.3 V(1)(2)(3)

Symbol	Parameter	Conditions			Typ			Unit
		-	Voltage scaling	f_{HCLK1}	25 °C	55 °C	85 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK1} = f_{HSI16}$ = 16 MHz	Range 2	16 Mhz	0.83	0.86	0.94	mA
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz	Range 1.5	32 Mhz	2.00	2.07	2.21	
		f_{HCLK1} = HSE32 + PLL > 32 MHz		64 Mhz	3.74	3.82	3.98	
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz	Range 1	32 Mhz	2.16	2.24	2.41	
		f_{HCLK1} = HSE32 + PLL > 32 MHz		64 MHz	4.07	4.16	4.34	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Reduced code used for characterization.
3. All peripherals disabled, SRAM1 and SRAM2 enabled.

Table 49. Current consumption in Run modes on SMPS, code with data processing running from flash memory, Cache ON (1-way), prefetch OFF, V_{DD} = 3.3 V(1)(2)(3)

Symbol	Parameter	Conditions			Typ			Unit
		-	Voltage scaling	f_{HCLK1}	25 °C	55 °C	85 °C	
$I_{DD(Run)}$	Supply current in Run mode	$f_{HCLK1} = f_{HSI16}$ = 16 MHz	Range 2	16 MHz	0.41	0.42	0.44	mA
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz	Range 1.5	32 MHz	1.13	1.16	1.24	
		f_{HCLK1} = HSE32 + PLL > 32 MHz		64 MHz	2.00	2.02	2.09	
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz	Range 1	32 MHz	1.28	1.30	1.39	
		f_{HCLK1} = HSE32 + PLL > 32 MHz		64 MHz	2.29	2.30	2.38	

1. Guaranteed by characterization results, unless otherwise specified.
2. Reduced code used for characterization results
3. All peripherals disabled, SRAM1 and SRAM2 enabled.

Table 50. Current consumption in Run mode on LDO, with different codes running from flash memory, Cache ON (2-way), Prefetch OFF(1)

Symbol	Parameter	Conditions			Typ			Unit	Typ			Unit
					25 °C				25 °C			
		-	Voltage scaling	Code	1.8 V	3.0 V	3.3 V		1.8 V	3.0 V	3.3 V	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, SRAM1 and SRAM2 enabled	Range 2, $f_{HCLK1} = f_{HSI16}$ = 16 MHz	Reduced code	0.87	0.87	0.87	mA	54.10	54.09	54.14	µA/MHz
				Coremark®	0.85	0.85	0.85		53.07	53.07	53.11	
				SecureMark	0.91	0.91	0.91		57.10	57.11	57.16	
				Fibonacci	0.77	0.77	0.77		48.03	48.04	48.07	
				While(1)	0.65	0.65	0.65		40.70	40.73	40.75	
			Range 1.5, $f_{HCLK1} = f_{HSI16}$ = 16 MHz	Reduced code	1.10	1.10	1.10		68.93	68.83	68.78	
				Coremark®	1.07	1.07	1.08		67.04	67.09	67.19	
				SecureMark	1.20	1.20	1.20		74.81	74.78	75.08	
				Fibonacci	0.99	0.99	0.99		61.59	61.64	61.69	
				While(1)	0.88	0.89	0.89		55.27	55.33	55.39	

Table 50. Current consumption in Run mode on LDO, with different codes running from flash memory, Cache ON (2-way), Prefetch OFF(1) (continued)

Symbol	Parameter	Conditions			Typ			Unit	Typ			Unit
					25 °C				25 °C			
		-	Voltage scaling	Code	1.8 V	3.0 V	3.3 V		1.8 V	3.0 V	3.3 V	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, SRAM1 and SRAM2 enables	Range 1.5, f_{HCLK1} = HSE32 + PLL at 64 MHz	Reduced code	3.76	3.78	3.79	mA	58.73	59.09	59.21	µA/MHz
				Coremark®	3.65	3.67	3.68		56.96	57.33	57.44	
				SecureMark	4.05	4.07	4.08		63.24	63.64	63.79	
				Fibonacci	3.35	3.38	3.38		52.37	52.76	52.87	
				While(1)	2.92	2.95	2.95		45.65	46.04	46.15	
			Range 1, $f_{HCLK1} = f_{HSE32}$ = 32 MHz	Reduced code	2.08	2.11	2.12		65.07	66.09	66.32	
				Coremark®	2.03	2.06	2.07		63.34	64.36	64.59	
				SecureMark	2.30	2.33	2.34		71.73	72.74	72.98	
				Fibonacci	1.85	1.88	1.88		57.66	58.69	58.90	
				While(1)	1.62	1.65	1.66		50.51	51.56	51.78	
			Range 1, f_{HCLK1} = HSE32 + PLL at 64 MHz	Reduced code	4.09	4.12	4.12		63.84	64.32	64.44	
				Coremark®	3.97	4.00	4.01		62.07	62.55	62.67	
				SecureMark	4.40	4.43	4.44		68.71	69.29	69.42	
				Fibonacci	3.58	3.61	3.61		55.86	56.35	56.47	
				While(1)	3.15	3.19	3.19		49.28	49.78	49.90	

1. Guaranteed by characterization results, unless otherwise specified.

Table 51. Current consumption in Run mode on SMPS, with different codes running from flash memory, Cache ON (2-way), Prefetch OFF(1)

Symbol	Parameter	Conditions			Typ			Unit	Typ			Unit
					25 °C				25 °C			
		-	Voltage scaling	Code	1.8 V	3.0 V	3.3 V		1.8 V	3.0 V	3.3 V	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, SRAM1 and SRAM2 enabled	Range 2, $f_{HCLK1} = f_{HSI16}$ = 16 MHz	Reduced code	0.58	0.43	0.41	mA	36.54	27.17	25.89	µA/MHz
				Coremark®	0.57	0.43	0.41		35.91	26.78	25.52	
				SecureMark	0.62	0.46	0.43		38.45	28.45	27.09	
				Fibonacci	0.52	0.40	0.38		32.77	24.77	23.68	
				While(1)	0.45	0.35	0.34		28.27	21.92	21.05	
			Range 1.5, $f_{HCLK1} = f_{HSI16}$ = 16 MHz	Reduced code	0.87	0.66	0.63		54.55	40.97	39.31	
				Coremark®	0.85	0.64	0.62		53.23	40.13	38.55	
				SecureMark	0.94	0.70	0.67		58.98	44.00	41.89	
				Fibonacci	0.79	0.60	0.58		49.37	37.67	36.28	
				While(1)	0.71	0.55	0.54		44.55	34.60	33.46	

Table 51. Current consumption in Run mode on SMPS, with different codes running from flash memory, Cache ON (2-way), Prefetch OFF(1) (continued)

Symbol	Parameter	Conditions			Typ			Unit	Typ			Unit
					25 °C				25 °C			
		-	Voltage scaling	Code	1.8 V	3.0 V	3.3 V		1.8 V	3.0 V	3.3 V	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, SRAM1 and SRAM2 enables	Range 1.5, f_{HCLK1} = HSE32 + PLL at 64 MHz	Reduced code	2.99	2.12	2.00	mA	46.79	33.15	31.27	µA/MHz
				Coremark®	2.91	2.06	1.95		45.40	32.25	30.44	
				SecureMark	3.23	2.28	2.15		50.41	35.61	33.55	
				Fibonacci	2.67	1.92	1.81		41.79	29.94	28.28	
				While(1)	2.34	1.69	1.60		36.50	26.48	25.07	
			Range 1, $f_{HCLK1} = f_{HSE32}$ = 32 MHz	Reduced code	1.72	1.22	1.16		53.69	38.25	36.20	
				Coremark®	1.67	1.20	1.13		52.29	37.37	35.38	
				SecureMark	1.89	1.34	1.26		59.21	41.82	39.50	
				Fibonacci	1.52	1.10	1.04		47.65	34.39	32.63	
				While(1)	1.34	0.98	0.93		41.74	30.62	28.92	
			Range 1, f_{HCLK1} = HSE32 + PLL at 64 MHz	Reduced code	3.38	2.34	2.19		52.84	36.51	34.25	
				Coremark®	3.29	2.28	2.14		51.41	35.59	33.41	
				SecureMark	3.65	2.51	2.35		56.96	39.16	36.74	
				Fibonacci	2.97	2.07	1.95		46.34	32.34	30.44	
				While(1)	2.62	1.85	1.74		40.90	28.87	27.24	

1. Guaranteed by characterization results, unless otherwise specified.

Table 52. Current consumption in Sleep modes, flash memory in power-down(1)(2)

Symbol	Parameter	Conditions				Typ			Unit
		-	-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	
$I_{DD(Sleep)}$	Supply current in Sleep mode	$f_{HCLK1} = f_{HSI16}$ = 16 MHz	LDO	Range 2	16 MHz	0.31	0.34	0.40	mA
		$f_{HCLK1} = f_{HSI16}$ = 16 MHz		Range 1.5	16 MHz	0.44	0.48	0.58	
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz			32 MHz	0.64	0.69	0.80	
		f_{HCLK1} = HSE32 + PLL > 32 MHz			64 MHz	1.22	1.27	1.39	
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz		Range 1	32 MHz	0.70	0.76	0.92	
		f_{HCLK1} = HSE32 + PLL > 32 MHz			64 MHz	1.31	1.38	1.54	
		$f_{HCLK1} = f_{HSI16}$ = 16 MHz	SMPS	Range 2	16 MHz	0.21	0.22	0.24	
		$f_{HCLK1} = f_{HSI16}$ = 16 MHz		Range 1.5	16 MHz	0.34	0.36	0.42	
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz			32 MHz	0.45	0.47	0.53	
		f_{HCLK1} = HSE32 + PLL > 32 MHz			64 MHz	0.82	0.84	0.90	
		$f_{HCLK1} = f_{HSE32}$ = 32 MHz		Range 1	32 MHz	0.47	0.51	0.60	
		f_{HCLK1} = HSE32 + PLL > 32 MHz			64 MHz	0.86	0.90	1.00	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. All peripherals disabled.

Table 53. Flash memory static power consumption(1)

Symbol	Parameter	Conditions	Typ			Unit
			25 °C	55 °C	85 °C	
I_{DD} (Flash)	Static consumption in normal mode	PD = 1 versus PD = 0	17.98	18.93	21.28	µA
I_{DD} (Flash_LPM)	Additional static consumption in normal versus low-power mode	LPM = 1 versus LPM = 0	11.42	11.90	19.12	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 54. Current consumption in Stop 0 mode(1)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	
$I_{DD(Stop\ 0)}$	Supply current in Stop 0 mode, no retention	LDO	Range 2	1.8 V	42.06	59.16	108.61	µA
				2.4 V	42.45	59.45	108.94	
				3.0 V	42.87	59.84	109.08	
				3.3 V	43.23	59.96	109.11	
				3.6 V	43.89	60.10	108.43	
	Supply current in Stop 0 mode, all retention (SRAM1 64K + SRAM2 32K + PKA RAM+ USB RAM)			1.8 V	43.15	61.50	115.19	
				2.4 V	43.56	61.80	115.52	
				3.0 V	43.96	62.14	115.63	
				3.3 V	44.32	62.22	115.40	
				3.6 V	44.92	62.34	114.67	
	Supply current in Stop 0 mode, SRAM1 64K retained			1.8 V	42.72	60.57	112.89	
				2.4 V	43.13	60.95	113.13	
				3.0 V	43.58	61.33	113.24	
				3.3 V	43.91	61.44	113.01	
				3.6 V	44.55	61.47	112.37	
	Supply current in Stop 0 mode, SRAM2 32K retained			1.8 V	42.43	59.93	110.94	
				2.4 V	42.81	60.27	111.19	
				3.0 V	43.20	60.67	111.43	
				3.3 V	43.58	60.79	111.31	
				3.6 V	44.20	60.92	110.71	

Table 54. Current consumption in Stop 0 mode(1) (continued)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	
$I_{DD(Stop\ 0)}$	Supply current in Stop 0 mode, no retention	SMPS	Range 2	1.8 V	10.81	20.31	50.01	µA
				2.4 V	9.62	17.02	40.37	
				3.0 V	9.09	15.37	34.79	
				3.3 V	9.08	14.87	32.95	
				3.6 V	9.28	14.66	31.59	
	Supply current in Stop 0 mode, all retention (SRAM1 64K + SRAM2 32K + PKA RAM+ USB RAM)			1.8 V	11.48	21.71	54.03	
				2.4 V	10.18	18.15	43.50	
				3.0 V	9.54	16.26	37.35	
				3.3 V	9.46	15.73	35.27	
				3.6 V	9.63	15.45	33.80	
	Supply current in Stop 0 mode, SRAM1 64K retained			1.8 V	11.23	21.25	52.50	
				2.4 V	9.99	17.79	42.46	
				3.0 V	9.41	15.94	36.36	
				3.3 V	9.32	15.41	34.34	
				3.6 V	9.49	15.13	32.90	
	Supply current in Stop 0 mode, SRAM2 32K retained			1.8 V	11.06	20.78	51.30	
				2.4 V	9.78	17.45	41.39	
				3.0 V	9.25	15.69	35.63	
				3.3 V	9.20	15.16	33.78	
				3.6 V	9.42	14.93	32.33	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 55. Current consumption in Stop 1 mode, ULPMEN = 1(1)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	
$I_{DD(Stop\ 1)}$	Supply current in Stop 1 mode, no retention	LDO	Range 2	1.8 V	11.33	25.80	72.28	µA
				2.4 V	11.41	25.80	72.16	
				3.0 V	11.46	25.74	72.08	
				3.3 V	11.57	25.77	71.73	
				3.6 V	11.84	25.87	71.36	
	Supply current in Stop 1 mode, all retention (SRAM1 64K + SRAM2 32K + PKA RAM+ USB RAM)			1.8 V	12.46	28.15	78.77	
				2.4 V	12.53	28.16	78.62	
				3.0 V	12.61	28.13	78.65	
				3.3 V	12.75	28.15	78.20	
				3.6 V	12.96	28.26	77.68	
	Supply current in Stop 1 mode, SRAM1 64K retained			1.8 V	12.04	27.31	76.15	
				2.4 V	12.09	27.29	76.29	
				3.0 V	12.16	27.24	76.20	
				3.3 V	12.28	27.28	75.80	
				3.6 V	12.53	27.39	75.38	
	Supply current in Stop 1 mode, SRAM2 32K retained			1.8 V	11.67	26.66	74.66	
				2.4 V	11.73	26.68	74.59	
				3.0 V	11.83	26.67	74.52	
				3.3 V	11.94	26.60	74.32	
				3.6 V	12.18	26.79	73.97	
$I_{DD(Stop\ 1)}$	Supply current in Stop 1 mode, no retention	SMPS	Range 2	1.8 V	7.15	16.06	44.44	µA
				2.4 V	5.66	12.57	34.68	
				3.0 V	4.80	10.52	29.02	
				3.3 V	4.57	9.84	27.11	
				3.6 V	4.52	9.56	25.67	
	Supply current in Stop 1 mode, all retention (SRAM1 64K + SRAM2 32K + PKA RAM+ USB RAM)			1.8 V	7.82	17.46	48.42	
				2.4 V	6.24	13.67	37.78	
				3.0 V	5.24	11.46	31.55	
				3.3 V	4.99	10.70	29.35	
				3.6 V	4.91	10.30	27.79	
	Supply current in Stop 1 mode, SRAM1 64K retained			1.8 V	7.57	16.93	46.81	
				2.4 V	6.03	13.21	36.59	
				3.0 V	5.08	11.08	30.58	

Table 55. Current consumption in Stop 1 mode, ULPMEN = 1(1) (continued)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	V_{DD}	25 °C	55 °C	85 °C	
$I_{DD(Stop\ 1)}$	Supply current in Stop 1 mode, SRAM1 64K retained	SMPS	Range 2	3.3 V	4.81	10.37	28.46	µA
				3.6 V	4.76	10.03	26.95	
	Supply current in Stop 1 mode, SRAM2 retained			1.8 V	7.40	16.52	45.76	
				2.4 V	5.87	12.94	35.74	
				3.0 V	4.95	10.79	29.87	
				3.3 V	4.69	10.13	27.83	
				3.6 V	4.66	9.77	36.41	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 56. Current consumption in Stop 2 mode, ULPMEN = 1(1)

Symbol	Parameter	Conditions		Typ			Unit
		-	V_{DD}	25 °C	55 °C	85 °C	
$I_{DD(Stop\ 2)}$	Supply current in Stop 2 mode, no retention	LDO	1.8 V	N/A	N/A	N/A	µA
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	
	Supply current in Stop 2 mode, all retention (SRAM1 64K + SRAM2 32K)		1.8 V	N/A	N/A	N/A	
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	
	Supply current in Stop 2 mode, SRAM2 retained		1.8 V	N/A	N/A	N/A	
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	
$I_{DD(Stop\ 2)}$	Supply current in Stop 2 mode, no retention	SMPS	1.8 V	N/A	N/A	N/A	
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	
	Supply current in Stop 2 mode, all retention (SRAM1 64K + SRAM2 32K)		1.8 V	N/A	N/A	N/A	
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	
	Supply current in Stop 2 mode, SRAM2 retained		1.8 V	N/A	N/A	N/A	
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 57. Current consumption in Stop 3 mode, ULPMEN = 1(1)

Symbol	Parameter	Conditions		Typ			Unit
		-	V_{DD}	25 °C	55 °C	85 °C	
$I_{DD(Stop\ 3)}$	Supply current in Stop 3 mode, no retention	LDO	1.8 V	N/A	N/A	N/A	µA
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	
	Supply current in Stop 3 mode, all retention (SRAM1 64K + SRAM2 32K)		1.8 V	N/A	N/A	N/A	
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	
	Supply current in Stop 3 mode, SRAM2 retained		1.8 V	N/A	N/A	N/A	
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	
$I_{DD(Stop\ 3)}$	Supply current in Stop 3 mode, no retention	SMPS	1.8 V	N/A	N/A	N/A	
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	
	Supply current in Stop 3 mode, all retention (SRAM1 64K + SRAM2 32K)		1.8 V	N/A	N/A	N/A	
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	
	Supply current in Stop 3 mode, SRAM2 retained		1.8 V	N/A	N/A	N/A	
			2.4 V	N/A	N/A	N/A	
			3.0 V	N/A	N/A	N/A	
			3.3 V	N/A	N/A	N/A	
			3.6 V	N/A	N/A	N/A	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 58. Current consumption in Standby retention mode, ULPMEN = 1

Symbol	Parameter	Conditions			Typ			Unit
		-	-	VDD	25 °C	55 °C	85 °C	
IDD(Standby with retention)	SRAM1 64 KB + SRAM2 32 K + 2.4 GHz Radio + RTC	RTCRSB = 1, RADIORSB = 1	LDO	1.8 V	2.22	4.94	13.22	µA
				2.4 V	2.18	4.96	13.26	
				3.0 V	2.24	5.08	13.48	
				3.3 V	2.37	5.20	13.74	
				3.6 V	2.68	5.51	14.07	
	SRAM1 64K + 2.4 GHz Radio + RTC			1.8 V	1.85	4.07	11.06	
				2.4 V	1.78	4.12	11.07	
				3.0 V	1.87	4.27	11.31	
				3.3 V	1.98	4.39	11.61	
				3.6 V	2.29	4.78	12.14	
	SRAM1 64K + RTC	RTCRSB = 1, RADIORSB = 0		1.8 V	1.69	3.81	10.34	
				2.4 V	1.66	3.85	10.41	
				3.0 V	1.75	3.95	10.63	
				3.3 V	1.85	4.12	10.91	
				3.6 V	2.11	4.50	11.41	
	SRAM2 32K + RTC			1.8 V	0.68	2.24	7.60	
				2.4 V	0.74	2.23	7.69	
				3.0 V	0.76	2.35	8.00	
				3.3 V	0.88	2.52	8.35	
				3.6 V	1.15	2.89	8.89	
	SRAM1 64K	RTCRSB = 0, RADIORSB = 0		1.8 V	0.98	3.00	10.38	
				2.4 V	1.02	3.00	10.45	
				3.0 V	1.04	3.10	10.77	
				3.3 V	1.13	3.25	11.07	
				3.6 V	1.42	3.63	11.60	
	SRAM2 8K			1.8 V	0.53	1.73	5.98	
				2.4 V	0.55	1.72	6.10	
				3.0 V	0.60	1.91	6.39	
				3.3 V	0.72	2.03	6.68	
				3.6 V	0.94	2.43	7.33	
	SRAM1 64 KB + SRAM2 32 K + 2.4 GHz Radio + RTC	RTCRSB = 1, RADIORSB = 1	SMPS	1.8 V	1.49	3.31	8.75	
				2.4 V	1.24	2.70	7.15	

Table 58. Current consumption in Standby retention mode, ULPMEN = 1 (continued)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	VDD	25 °C	55 °C	85 °C	
IDD(Standby with retention)	SRAM1 64 KB + SRAM2 32 K + 2.4 GHz Radio + RTC	RTCRSB = 1, RADIORSB = 1	SMPS	3.0 V	1.12	2.38	6.40	µA
				3.3 V	1.13	2.41	6.33	
				3.6 V	1.31	2.64	6.51	
	SRAM1 64K + 2.4 GHz Radio + RTC			1.8 V	1.26	2.85	7.36	
				2.4 V	1.03	2.26	6.11	
				3.0 V	0.98	2.02	5.50	
				3.3 V	0.98	2.12	5.52	
				3.6 V	1.17	2.33	5.77	
	SRAM1 64K + RTC	RTCRSB = 1, RADIORSB = 0		1.8 V	1.14	2.62	6.91	
				2.4 V	0.92	2.14	5.75	
				3.0 V	0.89	1.90	5.22	
				3.3 V	0.92	2.01	5.26	
				3.6 V	1.12	2.23	5.55	
	SRAM2 32K + RTC			1.8 V	0.45	1.28	4.36	
				2.4 V	0.40	1.09	3.76	
				3.0 V	0.40	1.08	3.62	
				3.3 V	0.46	1.17	3.82	
				3.6 V	0.69	1.47	4.24	
	SRAM1 64K	RTCRSB = 0, RADIORSB = 0		1.8 V	0.57	1.66	5.73	
				2.4 V	0.51	1.39	4.80	
				3.0 V	0.49	1.31	4.48	
				3.3 V	0.55	1.39	4.60	
				3.6 V	1.14	1.67	4.95	
	SRAM2 8K			1.8 V	0.34	1.05	3.55	
				2.4 V	0.32	0.92	3.14	
				3.0 V	0.33	0.92	3.15	
				3.3 V	0.43	1.02	3.37	
				3.6 V	0.63	1.36	3.81	
IDD(Standby with RTC)	Supply current in Standby mode, SRAM2 32K, RTC enabled, RTCRSB = 1	Clocked by LSE crystal 32.768 kHz in medium low-drive	ULPMEN = 1	1.8 V	1.47	3.22	8.82	
				2.4 V	1.65	3.25	9.03	
				3.0 V	1.66	3.48	9.29	
				3.3 V	1.86	3.76	9.71	
				3.6 V	2.16	4.19	10.53	

Table 58. Current consumption in Standby retention mode, ULPMEN = 1 (continued)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	VDD	25 °C	55 °C	85 °C	
IDD(Standby with RTC)	Supply current in Standby mode, SRAM2 32K, RTC enabled, RTCRSB = 1	Clocked by LSE crystal 32.768 kHz in medium low-drive	ULPMEN = 0	1.8 V	2.53	4.33	9.91	µA
				2.4 V	3.07	4.63	10.29	
				3.0 V	3.35	5.12	10.84	
				3.3 V	3.66	5.55	11.38	
				3.6 V	4.16	6.19	12.30	
		Clocked by LSI1	ULPMEN = 1	1.8 V	1.28	3.01	8.57	
				2.4 V	1.43	3.05	8.74	
				3.0 V	1.45	3.25	9.00	
				3.3 V	1.65	3.53	9.37	
				3.6 V	1.95	3.96	10.24	
			ULPMEN = 0	1.8 V	2.35	4.02	9.56	
				2.4 V	2.81	4.43	10.03	
				3.0 V	3.14	4.89	10.54	
				3.3 V	3.50	5.37	11.06	
				3.6 V	3.97	5.95	12.05	
		Clocked by LSI1 / 128	ULPMEN = 1	1.8 V	1.16	2.83	8.26	
				2.4 V	1.26	2.87	8.32	
				3.0 V	1.26	2.97	8.55	
				3.3 V	1.42	3.21	8.95	
				3.6 V	1.66	3.67	9.76	
			ULPMEN = 0	1.8 V	2.23	3.90	9.29	
				2.4 V	2.64	4.25	9.61	
				3.0 V	2.95	4.65	10.10	
				3.3 V	3.22	5.05	10.63	
				3.6 V	3.66	5.65	11.60	
		Clocked by LSE bypass 32.768 kHz	ULPMEN = 1	1.8 V	N/A	N/A	N/A	
				2.4 V	N/A	N/A	N/A	
				3.0 V	N/A	N/A	N/A	
				3.3 V	N/A	N/A	N/A	
				3.6 V	N/A	N/A	N/A	
			ULPMEN = 0	1.8 V	N/A	N/A	N/A	
				2.4 V	N/A	N/A	N/A	
				3.0 V	N/A	N/A	N/A	

Table 58. Current consumption in Standby retention mode, ULPMEN = 1 (continued)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	VDD	25 °C	55 °C	85 °C	
IDD(Standby with RTC)	Supply current in Standby mode, SRAM2 32K, RTC enabled, RTCRSB = 1	Clocked by LSE bypass 32.768 kHz	ULPMEN = 0	3.3 V	N/A	N/A	N/A	µA
				3.6 V	N/A	N/A	N/A	
	Supply current in Standby mode, SRAM2 8K, RTC enabled, RTCRSB = 1	Clocked by LSE crystal 32.768 kHz in medium low-drive	ULPMEN = 1	1.8 V	1.22	2.67	7.39	
				2.4 V	1.37	2.73	7.57	
				3.0 V	1.45	2.97	7.86	
				3.3 V	1.60	3.18	8.31	
				3.6 V	1.90	3.67	9.11	
			ULPMEN = 0	1.8 V	2.29	3.78	8.48	
				2.4 V	2.79	4.11	8.84	
				3.0 V	3.14	4.61	9.41	
				3.3 V	3.40	4.97	9.98	
				3.6 V	3.90	5.66	10.88	
		Clocked by LSI1	ULPMEN = 1	1.8 V	1.03	2.46	7.14	
				2.4 V	1.15	2.53	7.28	
				3.0 V	1.24	2.74	7.57	
				3.3 V	1.40	2.95	7.97	
				3.6 V	1.69	3.44	8.82	
			ULPMEN = 0	1.8 V	2.10	3.47	8.13	
				2.4 V	2.53	3.91	8.57	
				3.0 V	2.94	4.38	9.11	
				3.3 V	3.24	4.79	9.66	
				3.6 V	3.71	5.43	10.63	
		Clocked by LSI1 / 128	ULPMEN = 1	1.8 V	0.92	2.28	6.83	
				2.4 V	0.98	2.35	6.86	
				3.0 V	1.06	2.45	7.12	
				3.3 V	1.16	2.63	7.55	
				3.6 V	1.39	3.15	8.34	
			ULPMEN = 0	1.8 V	1.98	3.35	7.85	
				2.4 V	2.36	3.73	8.16	
				3.0 V	2.75	4.14	8.67	
				3.3 V	2.96	4.47	9.23	
				3.6 V	3.40	5.12	10.18	

Table 58. Current consumption in Standby retention mode, ULPMEN = 1 (continued)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	VDD	25 °C	55 °C	85 °C	
IDD(Standby with RTC)	Supply current in Standby mode, SRAM2 8K, RTC enabled, RTCRSB = 1	Clocked by LSE bypass 32.768 kHz	ULPMEN = 1	1.8 V	N/A	N/A	N/A	µA
				2.4 V	N/A	N/A	N/A	
				3.0 V	N/A	N/A	N/A	
				3.3 V	N/A	N/A	N/A	
				3.6 V	N/A	N/A	N/A	
			ULPMEN = 0	1.8 V	N/A	N/A	N/A	
				2.4 V	N/A	N/A	N/A	
				3.0 V	N/A	N/A	N/A	
				3.3 V	N/A	N/A	N/A	
				3.6 V	N/A	N/A	N/A	
	Supply current in Standby mode, RTC enabled, RTCRSB = 1	Clocked by LSE crystal 32.768 kHz in medium low-drive	ULPMEN = 1	1.8 V	1.22	2.67	7.32	
				2.4 V	1.31	2.71	7.51	
				3.0 V	1.41	2.96	7.85	
				3.3 V	1.60	3.16	8.30	
				3.6 V	1.90	3.63	9.05	
			ULPMEN = 0	1.8 V	2.28	3.78	8.42	
				2.4 V	2.73	4.09	8.78	
				3.0 V	3.10	4.60	9.41	
				3.3 V	3.40	4.95	9.97	
				3.6 V	3.90	5.62	10.82	
		Clocked by LSI1	ULPMEN = 1	1.8 V	1.03	2.45	7.07	
				2.4 V	1.10	2.52	7.22	
				3.0 V	1.20	2.72	7.57	
				3.3 V	1.40	2.92	7.96	
				3.6 V	1.69	3.39	8.76	
			ULPMEN = 0	1.8 V	2.10	3.47	8.07	
				2.4 V	2.48	3.90	8.51	
				3.0 V	2.89	4.37	9.11	
				3.3 V	3.24	4.77	9.66	
				3.6 V	3.71	5.39	10.56	
		Clocked by LSI1 / 128	ULPMEN = 1	1.8 V	0.91	2.28	6.76	
				2.4 V	0.93	2.34	6.80	
				3.0 V	1.01	2.44	7.11	

Table 58. Current consumption in Standby retention mode, ULPMEN = 1 (continued)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	VDD	25 °C	55 °C	85 °C	
IDD(Standby with RTC)	Supply current in Standby mode, RTC enabled, RTCRSB = 1	Clocked by LSI1 / 128	ULPMEN = 1	3.3 V	1.16	2.60	7.54	µA
				3.6 V	1.39	3.10	8.28	
			ULPMEN = 0	1.8 V	1.98	3.35	7.79	
				2.4 V	2.30	3.72	8.10	
				3.0 V	2.70	4.13	8.67	
				3.3 V	2.96	4.44	9.22	
				3.6 V	3.39	5.08	10.12	
		Clocked by LSE bypass 32.768 kHz	ULPMEN = 1	1.8 V	N/A	N/A	N/A	
				2.4 V	N/A	N/A	N/A	
				3.0 V	N/A	N/A	N/A	
				3.3 V	N/A	N/A	N/A	
				3.6 V	N/A	N/A	N/A	
			ULPMEN = 0	1.8 V	N/A	N/A	N/A	
				2.4 V	N/A	N/A	N/A	
				3.0 V	N/A	N/A	N/A	
				3.3 V	N/A	N/A	N/A	
				3.6 V	N/A	N/A	N/A	
IDD(Standby with IWDG+RTC)	Supply current in Standby mode, IWDG enabled, RTC enabled, RTCRSB = 1	Clocked by LSI1	ULPMEN = 1	1.8 V	1.05	2.46	7.04	
				2.4 V	1.13	2.55	7.20	
				3.0 V	1.24	2.71	7.55	
				3.3 V	1.39	2.92	8.01	
				3.6 V	1.74	3.44	8.73	
			ULPMEN = 0	1.8 V	2.12	3.50	8.07	
				2.4 V	2.51	3.88	8.49	
				3.0 V	2.93	4.40	9.16	
				3.3 V	3.28	4.76	9.68	
				3.6 V	3.75	5.38	10.55	

Table 59. Current consumption in Standby mode(1)

Symbol	Parameter	Conditions			Typ			Unit
		-	-	VDD	25 °C	55 °C	85 °C	
I_{DD} (Standby)	Supply current in Standby mode, all peripherals disabled	Clocks off	ULPMEN = 1	1.8 V	0.11	0.29	1.15	µA
				2.4 V	0.13	0.31	1.27	
				3.0 V	0.13	0.42	1.60	
				3.3 V	0.25	0.58	2.01	
				3.6 V	0.46	1.00	2.73	
			ULPMEN = 0	1.8 V	1.18	1.36	2.18	
				2.4 V	1.51	1.69	2.56	
				3.0 V	1.82	2.11	3.15	
				3.3 V	2.05	2.42	3.68	
				3.6 V	2.47	2.97	4.57	
I_{DD} (Standby with IWDG)	IDWG enabled, RTCRSB = 0	Clocked by LSI1	ULPMEN = 1	1.8 V	1.02	2.43	6.87	
				2.4 V	1.07	2.44	7.00	
				3.0 V	1.17	2.62	7.32	
				3.3 V	1.38	2.83	7.70	
				3.6 V	1.69	3.35	8.51	
			ULPMEN = 0	1.8 V	2.09	3.50	7.89	
				2.4 V	2.45	3.82	8.29	
				3.0 V	2.86	4.30	8.87	
				3.3 V	3.19	4.66	9.38	
				3.6 V	3.69	5.33	10.36	
		Clocked by LSI1 / 128	ULPMEN = 1	1.8 V	0.95	2.28	6.77	
				2.4 V	0.97	2.33	6.83	
				3.0 V	0.97	2.44	7.12	
				3.3 V	1.12	2.61	7.50	
				3.6 V	1.40	3.11	8.28	µA
			ULPMEN = 0	1.8 V	2.02	3.35	7.79	
				2.4 V	2.35	3.72	8.13	
				3.0 V	2.66	4.12	8.68	
				3.3 V	2.92	4.44	9.18	
				3.6 V	3.40	5.08	10.12	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up or pull-down generate current consumption when the pin is externally held to the opposite level. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Section 6.3.17*.

For the output pins, any internal or external pull-up or pull-down and external load must also be considered to estimate the current consumption.

An additional current consumption is due to I/Os configured as inputs when an intermediate voltage level is applied externally. This is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is the case of ADC input pins, which must be configured as analog inputs.

Caution: Any floating input pin can settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must be configured in analog mode, or forced internally to a definite digital value. This can be done by using pull-up/down resistors, or by configuring the pins in output mode.

I/O dynamic current consumption

The I/Os used in application increase the consumption measured previously (see *Table 60*). When an I/O pin switches, it uses the current from the I/O supply voltage to supply the pin circuitry, and to charge/discharge the capacitive load (internal and external) connected to it:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where:

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DD} is the I/O supply voltage
- f_{SW} is the I/O switching frequency
- C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$
  - C_{INT} is the I/O pin capacitance
  - C_{EXT} is any connected external device pin capacitance
  - C_S is the PCB board capacitance

The pin is configured in push-pull output mode, and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The power consumption of the digital part of the peripherals is given in *Table 60*, while that of the analog part (when applicable) is indicated in the related sections.

The MCU is put under the following conditions:

- All I/O pins are in analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- The ambient operating temperature and supply voltage conditions summarized in *Table 34*

Table 60. Peripheral typical dynamic current consumption(1)

Bus	Peripheral	Range 1 LDO	Range 1.5 LDO	Range 2 LDO	Range 1 SMPS	Range 1.5 SMPS	Range 2 SMPS	Unit
AHB1	AHB1 bus	-	-	-	-	-	-	µA/MHz
	SRAM1	0.32	0.29	0.22	0.16	0.14	0.09	
	CRC	0.29	0.26	0.20	0.14	0.12	0.08	
	RAMCFG	0.22	0.20	0.16	0.11	0.10	0.06	
	LPDMA	1.56	1.42	1.11	0.82	0.69	0.42	
	ICACHE	0.36	0.41	0.41	0.41	0.39	0.38	
	FLASH interface	1.32	1.19	0.93	0.69	0.58	0.36	
	GTZC1	0.44	0.40	0.31	0.23	0.19	0.11	
AHB2	AHB2 bus(2)	-	-	-	-	-	-	µA/MHz
	SRAM2	0.68	0.61	0.24	0.35	0.29	0.09	
	PKA	4.77	4.27	3.20	2.28	1.88	1.05	
	RNG	1.36	1.22	0.95	0.71	0.59	0.37	
	HASH	1.27	1.15	0.89	0.67	0.55	0.35	
	AES	1.57	1.41	1.09	0.81	0.68	0.43	
	GPIOA	0.03	0.03	0.03	0.02	0.01	0.02	
	GPIOB	0.03	0.02	0.03	0.01	0.01	0.01	
	GPIOC	0.03	0.02	0.02	0.02	0.01	0.02	
	GPIOH	0.03	0.03	0.01	0.02	0.01	0.02	
AHB4	AHB4 bus	-	-	-	-	-	-	µA/MHz
	ADC4 kernel clock domain	1.31	1.20	0.92	0.69	0.57	0.37	
	ADC4 bus clock domain	2.24	2.04	1.57	1.16	0.98	0.62	
	PWR	0.07	0.06	0.05	0.03	0.02	0.02	
AHB5	AHB5 bus and peripherals(3)	0.04	0.02	0.03	0.01	0.02	0.01	µA/MHz
APB1	AHB to APB1(4)	-	-	-	-	-	-	µA/MHz
	TIM2	2.78	2.54	1.96	1.45	1.22	0.77	
	I2C1 kernel clock domain	1.54	1.39	1.08	0.80	0.68	0.42	
	I2C1 bus clock domain	2.21	2.01	1.55	1.15	0.97	0.61	
	LPTIM2 kernel clock domain	2.81	2.67	1.98	1.46	1.23	0.77	
	LPTIM2 bus clock domain	3.73	3.33	2.48	1.71	1.41	0.75	

Table 60. Peripheral typical dynamic current consumption(1) (continued)

Bus	Peripheral	Range 1 LDO	Range 1.5 LDO	Range 2 LDO	Range 1 SMPS	Range 1.5 SMPS	Range 2 SMPS	Unit
APB2	AHB to APB2(4)	-	-	-	-	-	-	µA/MHz
	USB	2.71	2.48	1.93	1.45	1.23	0.77	
	TIM17	1.60	1.52	1.29	1.08	0.93	0.74	
	TIM16	1.58	1.51	1.30	1.06	0.93	0.73	
	USART1 kernel clock domain	2.81	2.56	1.99	1.47	1.23	0.77	
	USART1 bus clock domain	2.72	2.54	2.06	1.65	1.42	1.02	
	SAI1 kernel clock domain	0.68	0.63	0.49	0.36	0.25	0.19	
APB2	SAI1 bus clock domain	1.25	1.21	1.05	0.89	0.78	0.63	µA/MHz
APB7	AHB to APB7(4)	-	-	-	-	-	-	
	SYSCFG	0.29	0.26	0.21	0.15	0.13	0.07	
	SPI3 kernel clock domain	0.72	0.66	0.51	0.39	0.32	0.20	
	SPI3 bus clock domain	2.50	2.27	1.76	1.30	1.10	0.39	
	LPUART1 kernel clock domain	2.21	2.03	1.58	1.16	0.98	0.61	
	LPUART1 bus clock domain	3.59	3.09	2.40	1.76	1.49	0.93	
	I2C3 kernel clock domain	1.67	1.52	1.18	0.88	0.73	0.46	
	I2C3 bus clock domain	2.40	2.19	1.70	1.25	1.06	0.66	
	LPTIM1 kernel clock domain	2.92	2.56	2.07	1.52	1.28	0.81	
	LPTIM1 bus clock domain	4.05	3.53	2.72	2.01	1.69	1.07	
	RTC/TAMP	1.45	1.33	1.00	0.76	0.64	0.41	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. The AHB bus is automatically active when at least one peripheral is ON on the AHB or associated APB.
3. RADIO inactive.
4. The AHB to APB bridge is automatically active when at least one peripheral is ON on the APB.

6.3.9 Wake-up time from low-power modes and voltage scaling transition times

The times given in *Table 61* are the latency between the event and the execution of the first user instruction (FSTEN = 1 in PWR_CR3 if not mentioned differently).

The device goes in Low-power mode after the WFE (Wait For Event) instruction.

Table 61. Low-power mode wake-up timings - LDO(1)

Symbol	Parameter	Conditions	Typ	Unit
$t_{WU(Sleep)}$	Wake-up time from Sleep to Run mode	SLEEP_PD = 0	14	CPU clock cycle
$t_{WU(Stop\ 0)}$	Wake-up time from Stop 0 to Run mode in flash memory, SRAMs retained	FLASHFWU = 0	8.99	µs
	Wake-up time from Stop 0 to Run mode in SRAM2		9.18	
$t_{WU(Stop\ 1)}$	Wake-up time from Stop 1 to Run mode in flash memory, SRAMs retained		18.25	
	Wake-up time from Stop 1 to Run mode in SRAM2		17.48	
$t_{WU(Stop\ 2)}$	Wake-up time from Stop 2 to Run mode in flash memory, SRAMs retained	-	28.05	
	Wake-up time from Stop 2 to Run mode in SRAM2		28.22	
$t_{WU(Stop\ 3)}$	Wake-up time from Stop 3 to Run mode in flash memory, SRAMs retained		36.37	
	Wake-up time from Stop 3 to Run mode in SRAM2		36.56	
$t_{WU(Standby\ with\ retention)}$	Wake-up time from Standby retention to Run mode in flash memory		71.10	
	Wake-up time from Standby to Run mode in SRAM2		71.12	
$t_{WU(Standby)}$	Wake-up time from Standby to Run mode in flash memory	FSTEN = 1	97	
		FSTEN = 0	262	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 62. Low-power mode wake-up timings - SMPS(1)

Symbol	Parameter	Conditions	Typ	Unit
$t_{WU(Sleep)}$	Wake-up time from Sleep to Run mode	SLEEP_PD = 0	14	CPU clock cycle
$t_{WU(Stop\ 0)}$	Wake-up time from Stop 0 to Run mode in flash memory, SRAMs retained	FLASHFWU = 0	8.99	µs
	Wake-up time from Stop 0 to Run mode in SRAM2		9.18	
$t_{WU(Stop\ 1)}$	Wake-up time from Stop 1 to Run mode in flash memory, SRAMs retained		14.82	
	Wake-up time from Stop 1 to Run mode in SRAM2		14.52	

Table 62. Low-power mode wake-up timings - SMPS(1) (continued)

Symbol	Parameter	Conditions	Typ	Unit
$t_{WU(Stop\ 2)}$	Wake-up time from Stop 2 to Run mode in flash memory, SRAMs retained	-	25.04	µs
	Wake-up time from Stop 2 to Run mode in SRAM2		25.24	
$t_{WU(Stop\ 3)}$	Wake-up time from Stop 3 to Run mode in flash memory, SRAMs retained		31.77	
	Wake-up time from Stop 2 to Run mode in SRAM2		32.56	
$t_{WU(Standby\ with\ retention)}$	Wake-up time from Standby retention to Run mode in flash memory		68.40	
	Wake-up time from Standby to Run mode in SRAM2		68.39	
$t_{WU(Standby)}$	Wake-up time from Standby to Run mode in flash memory	FSTEN = 1	97	
		FSTEN = 0	262	

1. Guaranteed by characterization results, unless otherwise specified.

Table 63. Regulator modes transition times(1)

Symbol	Parameter	Conditions	Typ	Unit
t_{LDO}	SMPS to LDO transition time	Range 2	19.82	µs
		Range 1.5	18.98	
		Range 1	19.15	
t_{SMPS}	LDO to SMPS transition time	Range 2	19.18	
		Range 1.5	21.87	
		Range 1	21.59	
t_{VOST}(2)	Range 2 to range 1	LDO	2.48	
		SMPS	2.79	
	Range 1 to range 2(3)	LDO	2.22	
		SMPS	2.01	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Time for ACTVOSRDY in PWR_SVMSR to indicate selected new VOS range.
3. VOSRDY remains at 1 on a transition from range 1 to range 2.

Table 64. Wake-up time using USART/LPUART(1)

Symbol	Parameter	Typ	Max	Unit
,$t_{WUUSART}$ $t_{WULPUART}$	Wake-up time needed to calculate the maximum USART/LPUART baudrate needed to wake up from Stop mode when USART/LPUART kernel clock source is HSI16	-	$t_{su(HSI16)}$ max	µs

1. Specified by design, not tested in production.

6.3.10 External clock source characteristics

High-speed external clock

The high-speed external (HSE32) clock can be supplied with a 32 MHz crystal or a clock source.

The devices include internal programmable capacitances that can be used to trim the crystal frequency, to compensate the PCB parasitic one.

Table 65. HSE32 crystal requirements(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	Oscillator frequency(2)	-	-	32	-	MHz
f_{TOL}	Frequency tolerance(3) includes initial accuracy, stability over temperature, aging, and frequency pulling due to incorrect load capacitance	Bluetooth® LE	-50	-	50	ppm
		IEEE802.15.4	-40	-	40	
C_L	Load capacitance	-	8	-	18	pF
C_O	Shunt capacitance	-	-	-	4	
ESR	Equivalent series resistance	-	60	-	150	Ω
C_{bank}	Capacitor bank range	-	6.6	-	23.6	pF
$C_{bank\text{-}step}$	Capacitor bank step size	-	215	270	325	fF
t_{STAB}	Oscillator stabilization time	-	-	100	160	µs
$I_{DDRF(HSE32)}$	Current consumption	-	-	205	-	µA

1. Specified by design, not tested in production.
2. 32 MHz XTAL is specified for two specific references: NX2016SA and NX1612SA.
3. After capacitor bank trimming.

Table 66. HSE32 clock source requirements(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE32}	External clock source frequency(2)	-	-	32	-	MHz
f_{TOL}	Frequency tolerance includes initial accuracy, stability over temperature, and aging	Bluetooth® LE	-50	-	50	ppm
		IEEE802.15.4	-40	-	40	
V_{HSE32}	Clock input voltage limits	Input level	0	-	0.9	V
		Amplitude(3)	200	-	900	mV_{PP}
$DuCy_{HSE32}$	Duty cycle	-	45	-	55	%
$\varphi_{n(HSE32)}$	Phase noise for 32 MHz	Offset = 10 kHz	-	-	-127	dBc/Hz
		Offset = 100 kHz	-	-	-135	
		Offset = 1 MHz	-	-	-138	

1. Specified by design, not tested in production.
2. $f_{HSE} = 1/t_{HSE}$.

3. AC coupling is supported (470 pF to 100 nF capacitor).

Note: For information about oscillator trimming, refer to AN5042 "Precise HSE frequency and startup time tuning for STM32 wireless MCUs", available on www.st.com.

Low-speed external clock

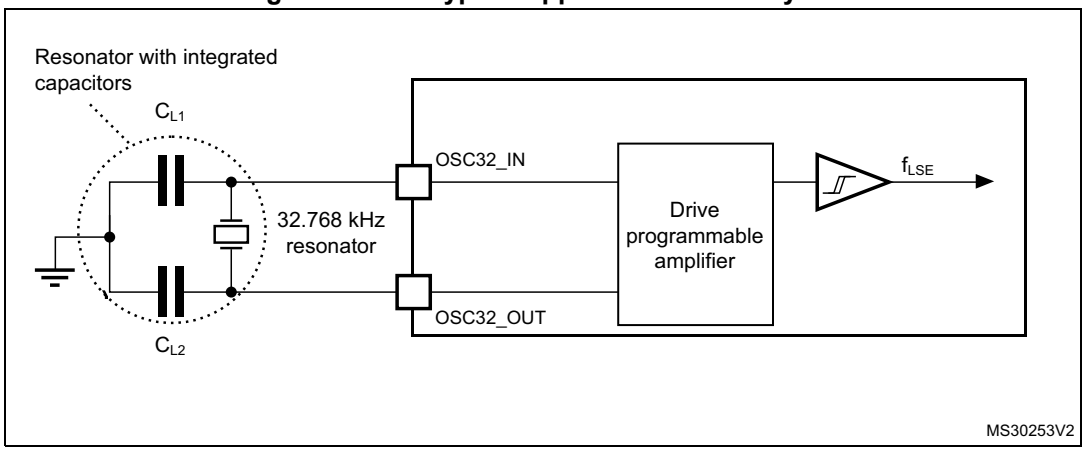
The low-speed external (LSE) clock can be supplied with a crystal or a clock source. The information provided in this section is based on design simulation results, obtained with the typical external components specified in *Table 67*. In the application, the crystal and the load capacitors must be placed as close as possible to the oscillator pins, to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 67. LSE oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Oscillator frequency(2)	-	-	32.000 or 32.768	-	kHz
f_{TOL}	Frequency tolerance includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance	Bluetooth® LE	-500	-	500	ppm
		Thread CSL	-255	-	255	
$I_{DD(LSE)}$	LSE current consumption	LSEDRV = medium-low drive capability	-	450	-	nA
		LSEDRV = medium-high drive capability	-	590	-	
		LSEDRV = high drive capability	-	700	-	
$Gm_{critmax}$	Maximum critical crystal Gm	LSEDRV = medium-low drive capability	-	-	0.75	µA/V
		LSEDRV = medium-high drive capability	-	-	1.70	
		LSEDRV = high drive capability	-	-	2.70	
C_{S_PARA}	Internal stray parasitic capacitance(3)	-	-	3	-	pF
$t_{SU(LSE)}$	Startup time(4)	V_{DD} is stabilized	-	2	-	s

1. Specified by design, not tested in production.
2. For information on selecting the crystal, refer to AN2867 '*Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs*".
3. CS_PARA is the equivalent capacitance seen by the crystal due to OSC32_IN and OSC32_OUT internal parasitic capacitances.
4. Time measured from when the LSE is enabled by software, until a stable LSE oscillation is reached. This value is measured for a standard crystal, and can vary significantly with the crystal used.

Figure 23. LSE typical application with a crystal



Note: No external resistors are required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

In bypass mode the LSE oscillator is switched off, and the input pin OSC32_IN is a standard GPIO.

Table 68. LSE external clock bypass mode characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	External clock source frequency(2)	-	32.000	32.768	-	kHz
f_{TOL}	Frequency tolerance includes initial accuracy and stability over temperature	Bluetooth® LE	-500	-	500	ppm
		Thread CSL	-225	-	225	
V_{IL}	OSC32_IN input low level voltage	-	-	-	0.3 x V_{DD}	V
V_{IH}	OSC32_IN input high level voltage	-	0.7 x V_{DD}	-	-	V
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN input high or low time for square signal	-	10	-	-	µs

1. Specified by design, not tested in production.
2. $f_{LSE} = 1/t_{LSE}$.

6.3.11 Internal clock source characteristics

The parameters given in the following tables are derived under ambient operating temperature and supply voltage conditions summarized in *Table 34*.

High-speed internal (HSI16) RC oscillator

Table 69. HSI16 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI16}	Frequency after factory calibration	V_{DD} = 3.0 V, T_J = 30 °C calibrated during production	15.92	16	16.08	MHz
		1.71 V ≤ V_{DD} ≤ 3.6 V, T_J = -10 to 100 °C(1)	15.84	16	16.16	
		1.71 V ≤ V_{DD} ≤ 3.6 V, T_J = -40 to 130 °C (1)	15.65	16	16.35	
TRIM(2)	User trimming step	-	18	29	40	kHz
$DuCy_{HSI16}$(2)	Duty cycle	-	45	-	55	%
$t_{su(HSI16)}$(2)	Startup time	-	-	2.5	3.6	µs
$t_{stab(HSI16)}$(2)	Stabilization time	-	-	4	6	
$I_{DD(HSI16)}$(2)	Power consumption	-	-	150	210	µA

1. Evaluated by characterization, not tested in production, unless otherwise specified. It does not take into account package and soldering effects.
2. Specified by design, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 70. LSI1 oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI1}	Frequency	V_{DD} = 3.0 V, T_J = 30 °C, LSIPREDIV = 1	0.245	0.25	0.255	kHz
		V_{DD} = 3.0 V, T_J = 30 °C, LSIPREDIV = 0	31.4	32.0	32.6	
		1.71 V ≤ V_{DD} ≤ 3.6 V, T_J = -40 to 85 °C, LSIPREDIV = 0 (1)	30.4	32.0	33.6	
$DuCy_{LSI1}$	Duty cycle	LSIPREDIV = 1	-	50	-	%
$t_{SU(LSI1)}$(2)	Startup time	-	-	230	260	µs
$t_{STAB(LSI1)}$(2)	Stabilization time	5% of final frequency	-	230	260	
$I_{DD(LSI1)}$(2)	Power consumption	LSIPREDIV = 0	-	140	255	nA
		LSIPREDIV = 1	-	130	240	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Specified by design, not tested in production.

6.3.12 PLL characteristics

The parameters given in *Table 71* are derived from tests performed at ambient temperature and under the supply voltage conditions summarized in *Table 34*.

Table 71. PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}(1)	PLL input clock	-	4	-	16	MHz
$DuCy_{PLL\_IN}$(1)	PLL input clock duty cycle	-	10	-	90	%
f_{PLL_OUT}(1)	PLL output clock P, Q, and R	-	1	-	64	MHz
$DuCy_{PLL\_OUT}$(1)	PLL output clock duty cycle	Division 1	40	-	60	%
f_{VCO_OUT}(1)	PLL VCO output	-	128	-	544	MHz
t_{LOCK}(2)	PLL lock time(3)	Integer mode	-	25	54	µs
		Fractional mode	-	40	65	
Jitter(1)	RMS cycle-to-cycle jitter	Integer mode, VCO = 544 MHz	-	±20	-	ps
		Fractional mode, VCO = 544 MHz	-	±70	-	
	RMS period jitter	Integer mode, VCO = 544 MHz	-	±35	-	
		Fractional mode, VCO = 544 MHz	-	±45	-	
	Long-term jitter(4) f_{PLL_IN} = 8 MHz	Integer mode, VCO = 544 MHz	-	±160	-	
		Fractional mode, VCO = 544 MHz	-	±170	-	
$I_{DD(PLL)}$(1)	PLL power consumption on V_{DD} with LDO	VCO freq = 100 MHz	-	370	-	µA
		VCO freq = 200 MHz	-	460	-	
		VCO freq = 336 MHz	-	710	-	
		VCO freq = 544 MHz	-	1100	-	
	PLL power consumption on V_{DD} with SMPS.	VCO freq = 100 MHz, 1 clock output	-	260	-	µA
		VCO freq = 100 MHz, 3 clock outputs	-	270	-	
		VCO freq = 200 MHz, 1 clock output	-	320	-	
		VCO freq = 336 MHz, 1 clock output	-	470	-	
		VCO freq = 544 MHz, 1 clock output	-	730	-	

1. Specified by design, not tested in production.
2. Evaluated by characterization, not tested in production, unless otherwise specified.
3. Lock time is the duration until PLL1RDY flag (2% of final frequency).
4. Measured on 5000 cycles.

6.3.13 Flash memory characteristics

Table 72. Flash memory characteristics

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog}(2)	64-bit programming time	Normal mode	73.1	81.2	µs
		Burst mode	41.6	46.1	

Table 72. Flash memory characteristics (continued)

Symbol	Parameter	Conditions	Typ	Max(1)	Unit
t_{prog_page}(2)	One 4-Kbyte page programming time	f_{AHB} = 64 MHz, normal mode	36.3	40.3	ms
		f_{AHB} = 64 MHz, burst mode	21.3	23.6	
t_{prog_flash}(2)	512-Kbyte programming time	f_{AHB} = 64 MHz, normal mode	4652	5164	
		f_{AHB} = 64 MHz, burst mode	2723	3023	
t_{ERASE}(2)	One 4-Kbyte page erase time	10 k endurance cycles	12.0	13.4	
		100 k endurance cycles	12.2	13.5	
t_{ME}(2)	Mass erase time (512 Kbytes)	10 k endurance cycles	36.3	40.3	
I_{DD}(3)	Average consumption from V_{DD}	Write mode	-	-	mA
		Erase mode	-	-	
	Maximum current (peak) from V_{DD}	Write mode	-	-	
		Erase mode	-	-	

1. Evaluated by characterization after cycling, not tested in production.
2. Specified by design, not tested in production, unless otherwise specified.
3. Evaluated by characterization, not tested in production, unless otherwise specified.

Table 73. Flash memory endurance and data retention(1)

Symbol	Parameter	Conditions		Min	Unit
N_{END}	Endurance	Whole user flash	T_A = –40 to 105 °C	10	kcycles
t_{RET}	Data retention(2)	Whole bank	T_A = 85 °C after 1 kcycles	30	
			T_A = 105 °C after 1 kcycles	15	
			T_A = 55 °C after 10 kcycles	30	
			T_A = 85 °C after 10 kcycles	15	
			T_A = 105 °C after 10 kcycles	10	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. Cycling performed over the whole temperature range.

6.3.14 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs as follows:

- ESD (electrostatic discharge), positive and negative: applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- FTB (fast transient voltage burst), positive and negative: applied to V_{DD} and V_{SS} pins through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 74*. They are based on the EMS levels and classes defined in AN1709 "*EMC design guide for STM8, STM32 and legacy MCUs*".

Table 74. EMS characteristics(1)

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to apply on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK1} = 64 MHz, UFQFPN48 conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to apply through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK1} = 64 MHz, UFQFPN48 conforming to IEC 61000-4-4	5A

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software.

Good EMC performance is highly dependent on the user application, and the software in particular. Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the requested EMC level.

Software recommendations

The software flow must include the management of runaway conditions, such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or on the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specified values. When an unexpected behavior is detected, the software can be hardened to prevent the occurrence of unrecoverable errors. See AN1015 "*Software techniques for improving microcontrollers EMC performance*" for more details.

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling two LEDs through the I/O ports). This emission test is compliant with the IEC 61967-2 standard, which specifies the test board and the pin loading.

Table 75. EMI characteristics for f_{HSE} = 32 MHz and f_{HCLK} = 64 MHz(1)

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak level(2)	V_{DD} = 3.6 V, T_A = 25 °C, all peripherals clocks ON, SMPS, UFQFPN48-SMPS-USB package compliant with IEC 61967-2	0.1 MHz to 30 MHz	7	dBµV
			30 MHz to 130 MHz	11	
			130 MHz to 1 GHz	3	
			1 GHz to 2 GHz	14	
	Level(3)		EMI level	3	-
	Peak level(2)	V_{DD} = 3.6 V, T_A = 25 °C, all peripherals clocks OFF, SMPS, UFQFPN48-SMPS-USB package compliant with IEC 61967-2	0.1 MHz to 30 MHz	6	dBµV
			30 MHz to 130 MHz	6	
			130 MHz to 1 GHz	2	
			1 GHz to 2 GHz	12	
	Level(3)		EMI level	3	-

1. Evaluated by characterization, not tested in production.
2. Refer to AN1709, “EMI radiated test” section.
3. Refer to AN1709, “EMI level classification” section.

6.3.15 Electrical sensitivity characteristics

Based on three different tests (ESD, latch-up) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 76. ESD absolute maximum ratings(1)

Symbol	Ratings	Conditions	Package	Class	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25 °C, conforming to ANSI/ESDA/JEDEC JS-001	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25 °C, conforming to ANSI/ESDA/JEDEC JS-002	UFQFPN32	C2a	500	
			UFQFPN48	C1	250	
			Thin WLCSP37	C2a	500	

1. Evaluated by characterization, not tested in production, unless otherwise specified.

Static latch-up

The following complementary static tests are required on three parts to assess the latch-up performance:

- a supply overvoltage is applied to each power supply pin
- a current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 77. Electrical sensitivity(1)

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_J = 130 °C conforming to JESD78E	2

1. Evaluated by characterization, not tested in production, unless otherwise specified.

6.3.16 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller if abnormal injection accidentally happens, some susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter, such as an ADC error above a certain limit (higher than 5 LSB ET), out of conventional limits of induced leakage current on adjacent pins (out of the -5 µA/0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in *Table 78*. The negative/positive induced leakage current is caused by the negative/positive injection.

Table 78. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on all pins	5	N/A	mA

1. Evaluated by characterization, not tested in production, unless otherwise specified.

6.3.17 I/O port characteristics

General input/output characteristics

The parameters given in *Table 79* are derived from tests performed at ambient temperature and under the supply voltage conditions summarized in *Table 34*. All I/Os are designed as CMOS- and TTL-compliant.

Note: For information on I/O configuration, refer to AN4899 “STM32 GPIO configuration for hardware settings and low-power consumption”.

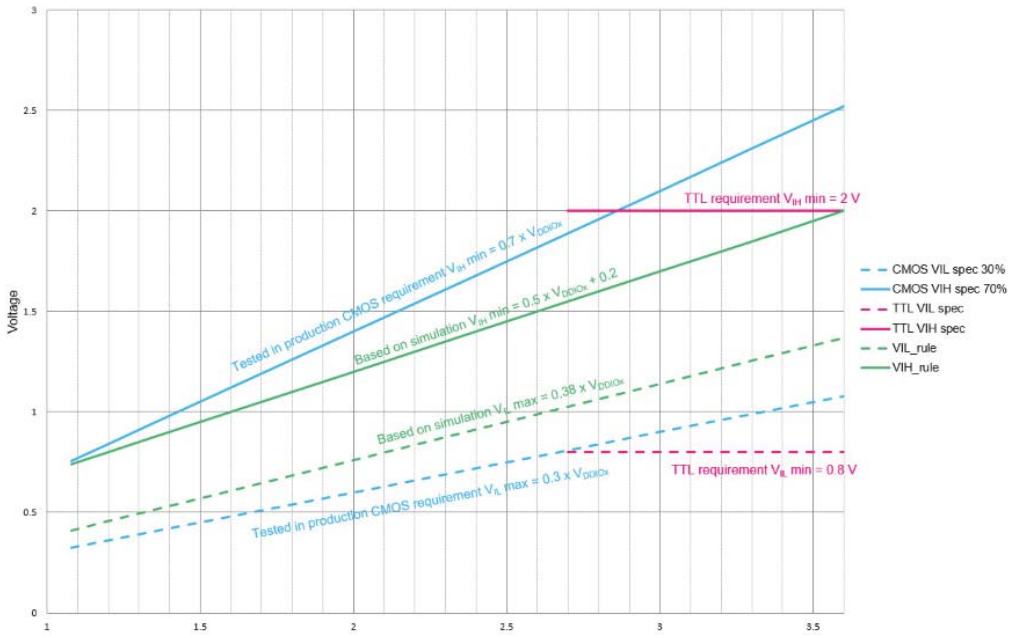
Table 79. I/O static characteristics

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage		1.58 V ≤ V_{DD} ≤ 3.6 V	-	-	0.3 x V_{DD}	V
V_{IH}	I/O input high level voltage			0.7 x V_{DD}	-	-	
V_{hys}(1)	Input hysteresis		-	-	250	-	mV
I_{lkg}(1)	I/O input leakage current(2)(3)	All I/Os except FT_u	V_{IN} ≤ Max(V_{DDx})	-	-	150	nA
			Max(V_{DDx}) < V_{IN} ≤ Max(V_{DDx}) + 1 V	-	-	2000	
			Max(V_{DDx}) + 1 V < V_{IN} ≤ 5.5 V(3)	-	-	500	
		FT_u I/Os	V_{IN} ≤ Max(V_{DDx})	-	-	200	
			Max(V_{DDx}) < V_{IN} ≤ Max(V_{DDx}) + 1 V	-	-	2500	
			Max(V_{DDx}) + 1 V < V_{IN} ≤ 5.5 V(3)	-	-	500	
R_{PU}	Weak pull-up equivalent resistor(4)		-	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(4)		-	30	40	50	
C_{IO}	I/O pin capacitance		-	-	5	-	pF

1. Specified by design, not tested in production.
2. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total\_Ileak\_max}$ = 10 µA + [number of I/Os where V_{IN} is applied on the pad] x I_{lkg} max.
3. To sustain a voltage higher than min (V_{DD}, V_{DDUSB}, V_{DDA}) + 0.3 V, the internal pull-up and pull-down resistors must be disabled.
4. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10%).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 24*.

Figure 24. I/O input characteristics (all I/Os except PH3)



Output driving current

The I/Os can sink or source up to ±8 mA, up to ±20 mA with a relaxed V_{OL} / V_{OH}.

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*.

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 31*).
- The sum of the currents sunk by all the I/Os on V_{SS}, plus the maximum consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 31*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 80* are at ambient temperature and under the supply voltage conditions summarized in *Table 34*. All I/Os are CMOS- and TTL-compliant.

Table 80. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage	$\|I_{IO}\|$ = 8 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage		V_{DD} - 0.4	-	
V_{OL}(2)	Output low level voltage	$\|I_{IO}\|$ = 20 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}(2)	Output high level voltage		V_{DD} - 1.3	-	
V_{OL}(2)	Output low level voltage	$\|I_{IO}\|$ = 4 mA, 1.58 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}(2)	Output high level voltage		V_{DD} - 0.4	-	
V_{OLFM+}(2)	Output low level voltage for an I/O pin in Fm+ mode	$\|I_{IO}\|$ = 20 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
		$\|I_{IO}\|$ = 10 mA, 1.58 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
		$\|I_{IO}\|$ = 2 mA, 1.08 V ≤ V_{DDIO2} ≤ 3.6 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 30*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings $\Sigma I_{(PIN)}$.
2. Specified by design, not tested in production.

Output AC characteristics

The definition of output AC characteristics is given in *Figure 25*, values in *Table 81* and *Table 80*. Unless otherwise specified, the parameters in these tables are at ambient temperature and under the supply voltage conditions summarized in *Table 34*.

Table 81. Output AC characteristics

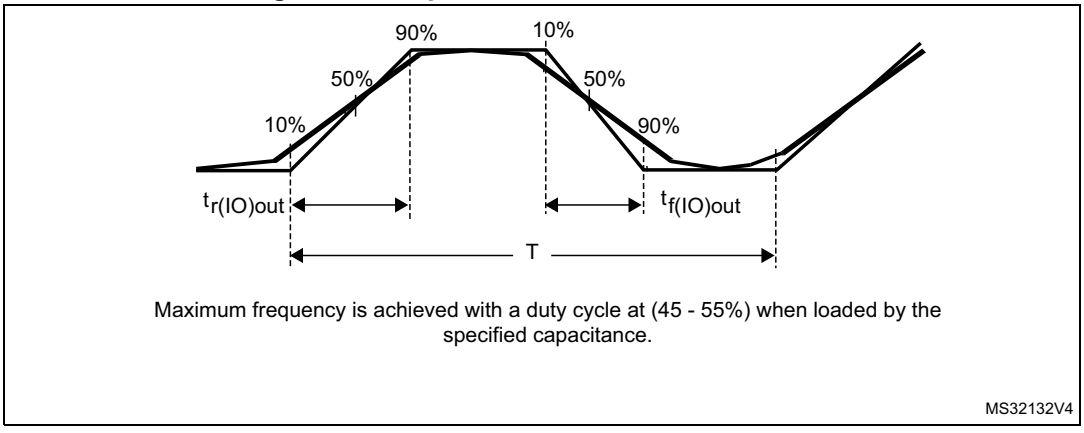
Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C_L = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.5	MHz
			C_L = 50 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	5	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.5	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	5	
	t_r/t_f	Output rise and fall time	C_L = 50 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	17	ns
			C_L = 50 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	33	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12.5	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	25	

Table 81. Output AC characteristics

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
01	Fmax	Maximum frequency	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	55	MHz
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	12.5	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	55	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	12.5	
	t_r/t_f	Output rise and fall time	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	5.8	ns
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	10	
			C_L = 30 pF, 1.08 V ≤ V_{DDIO2} < 1.58 V	-	18	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	4.2	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	7.5	
			C_L = 10 pF, 1.08 V ≤ V_{DDIO2} < 1.58 V	-	12	
10(1)	Fmax	Maximum frequency	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	64	MHz
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	33	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	64	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	40	
	t_r/t_f	Output rise and fall time	C_L = 30 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	3.3	ns
			C_L = 30 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	6.0	
			C_L = 10 pF, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	2.0	
			C_L = 10 pF, 1.58 V ≤ V_{DD} < 2.7 V	-	4.1	
Fm+	Fmax	Maximum frequency	C_L = 550 pF, 1.08 V ≤ V_{DD} ≤ 3.6 V	-	1	MHz
	t_f	Output fall time(2)	C_L = 550 pF, 1.58 V ≤ V_{DD} ≤ 3.6 V	-	64	ns
			C_L = 100 pF, 1.58 V ≤ V_{DD} < 3.6 V	-	50	

1. I/O compensation system enabled.
2. The fall time is defined between 70% and 30% of the output waveform, according to the I^2C specification.

Figure 25. Output AC characteristics definition



6.3.18 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

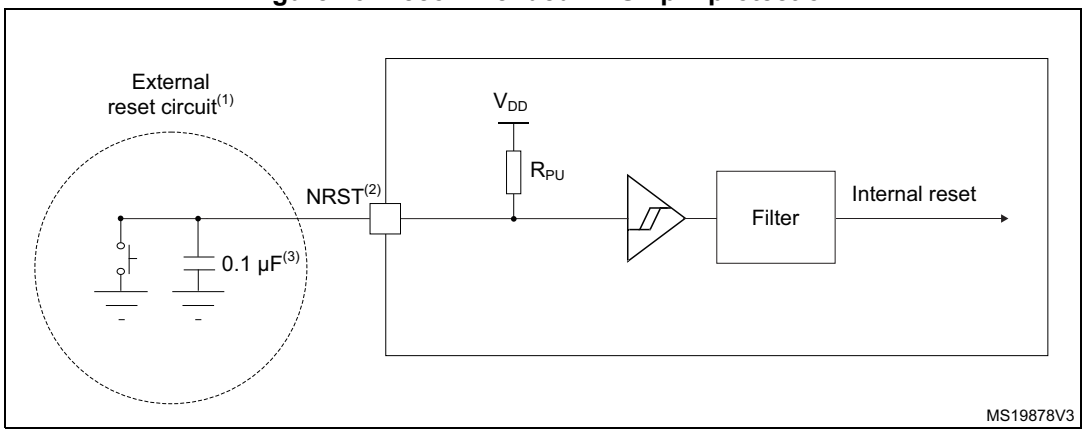
Unless otherwise specified, the parameters given in *Table 82* are at ambient temperature and under the supply voltage conditions summarized in *Table 34*.

Table 82. NRST pin characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	Input low level voltage	-	-	-	0.3 x V_{DD}	V
$V_{IH(NRST)}$	Input high level voltage	-	0.7 x V_{DD}	-	-	
$V_{hys(NRST)}$	Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$t_{F(NRST)}$	Input filtered pulse	-	-	-	50	ns
$t_{NF(NRST)}$	Input not-filtered pulse	1.71 V ≤ V_{DD} ≤ 3.6 V	330	-	-	
		1.58 V ≤ V_{DD} < 1.71 V	1000	-	-	

1. Specified by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS, whose contribution to the series resistance is minimal (~10%).

Figure 26. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ maximum level specified in *Table 82*, or the reset is not taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

6.3.19 Extended interrupt and event controller input (EXTI) characteristics

Pulses on the extended interrupt and event controller inputs must have a minimal length, to guarantee they are detected.

Table 83. EXTI input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(EXTI)}$	Pulse length to event controller	-	20	-	-	ns

1. Specified by design, not tested in production.

6.3.20 XSPI interface characteristics

Unless otherwise specified, the parameters given in *Table 84* and *Table 85* are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage conditions summarized in *Table 34*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- VOS range 1

Refer to *Section 6.3.17* for more details on the input/output alternate function characteristics.

Table 84. XSPI characteristics in SDR mode(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	XSPI clock frequency	2.7 V < V_{DD} < 3.6 V Voltage range 1 C_L = 15 pF			64	MHz
		1.71 V < V_{DD} < V, C_L = 15 pF	-	-	36	
		.71 V < V_{DD} < 3.6 V, C_L =15 pF	-	-	16	
$t_{w(CLKH)}$	XSPI clock high and low time, even division	PRESCALER[7:0] = n (= 0, 1, 3, 5,..., 255)	$t_{(CLK)}$ / 2 - 0.5	-	$t_{(CLK)}$ / 2 + 0.5	ns
$t_{w(CLKL)}$			$t_{(CLK)}$ / 2 - 0.5	-	$t_{(CK)}$ / 2 + 0.5	
$t_{w(CLKH)}$	XSPI clock high and low time, odd division	PRESCALER[7:0] = n (= 2, 4, 6, ..., 254)	(n / 2) * $t_{(CLK)}$ / (n + 1) - 0.5	-	(n / 2) * $t_{(CLK)}$ / (n + 1) + 0.5	
$t_{w(CLKL)}$			(n / 2 + 1) * $t_{(CLK)}$ / (n + 1) - 0.5	-	(n / 2 + 1) * $t_{(CLK)}$ / (n + 1) + 0.5	
$t_{s(IN)}$	Data input setup time	-	4	-	-	
$t_{h(IN)}$	Data input hold time	-	2.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	0.5	1.5	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

1. All values apply to Quad-SPI mode.
2. Evaluated by characterization - Not tested in production.

Figure 27. XSPI SDR read/write timing diagram

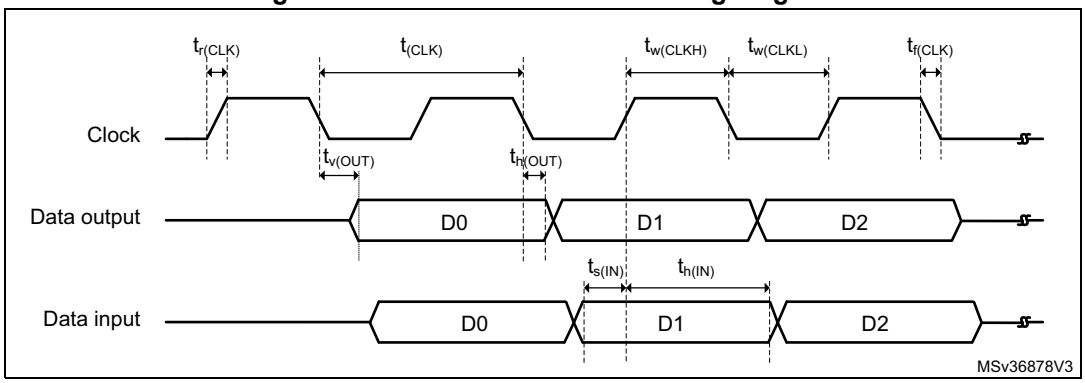


Table 85. XSPI characteristics in DTR mode (no DQS)(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CLK}	XSPI clock frequency	1.71 V < V_{DD} < 3.6 V, Voltage range 1 C_L = 15 pF	-	-	32	MHz
		1.71 V < V_{DD} < 3.6 V, Voltage range 2 C_L = 15 pF	-	-	16	
$t_{w(CLKH)}$	XSPI clock high and low time (even division)	PRESCALER[7:0] = n (= 0, 1, 3, 5, .., 255)	$t_{(CLK)}$ / 2 - 0.5	-	$t_{(CLK)}$ / 2 + 0.5	ns
$t_{w(CLKL)}$			$t_{(CLK)}$ / 2 - 0.5	-	$t_{(CLK)}$ / 2 + 0.5	
$t_{w(CLKH)}$	XSPI clock high and low time (odd division)	PRESCALER[7:0] = n (= 2, 4, 6, 8, ..., 254)	(n / 2) * $t_{(CLK)}$/ (n + 1) - 0.5	-	(n / 2) * $t_{(CLK)}$/ (n + 1) + 0.5	
$t_{w(CLKL)}$			(n / 2 + 1) * $t_{(CLK)}$/ (n + 1) - 0.5	-	(n / 2 + 1) * $t_{(CLK)}$/ (n + 1) + 0.5	
$t_{sr(IN)}$	Data input setup time on rising edge	-	4	-	-	
$t_{sf(IN)}$	Data input setup time on falling edge	-	3.5	-	-	
$t_{hr(IN)}$	Data input hold time on rising edge	-	2.5	-	-	
$t_{hf(IN)}$	Data input hold time on falling edge	-	3	-	-	
$t_{vr(OUT)}$	Data output valid time on rising Edge DHQC = 0	-	-	5	7	
$t_{vf(OUT)}$	Data output valid time on falling edge DHQC = 0	-	-	4.5	6.5	
$t_{hr(OUT)}$	Data output hold time on rising edge DHQC = 0	-	2.5	-	-	

Table 85. XSPI characteristics in DTR mode (no DQS)(1)(2)(3) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{hf(OUT)}$	Data output hold time on falling edge DHQC = 0	-	3.5	-	-	ns
$t_{vr(OUT)}$	Data output valid time on rising edge DHQC = 1	All prescaler values (except 0)	-	$t_{(CLK)}/4$	$t_{(CLK)}/4$ +2	
$t_{vf(OUT)}$	Data output valid time on falling edge DHQC = 1	All prescaler values (except 0)	-	$t_{(CLK)}/4$	$t_{(CLK)}/4$ +1.5	
$t_{hr(OUT)}$	Data output hold time on rising edge DHQC = 1	All prescaler values (except 0)	$t_{(CLK)}/4$ -1.5	-	-	
$t_{hf(OUT)}$	Data output hold time on falling edge DHQC = 1	All prescaler values (except 0)	$t_{(CLK)}/4$ -2	-	-	

1. DHQC must be set to reach the mentioned frequency.
2. Evaluated by characterization - Not tested in production.
3. Delay block bypassed.

Table 86. XSPI characteristics in DTR mode (with DQS)(1)(2)

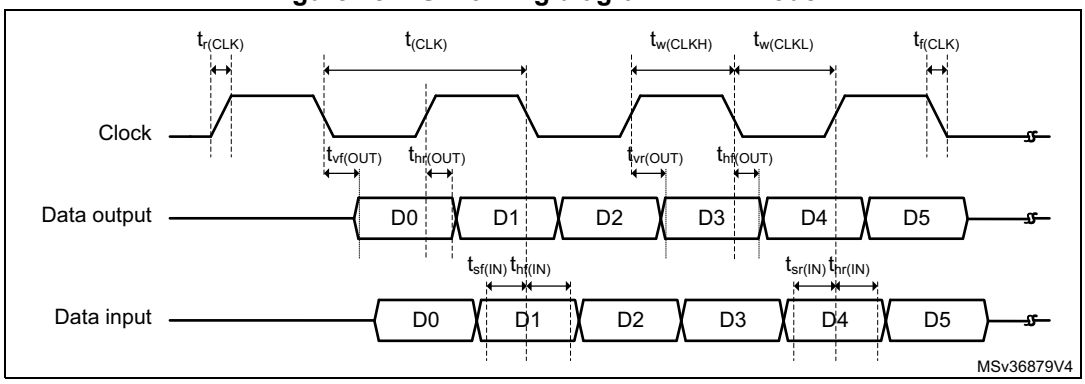
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CLK}	XSPI clock frequency	1.71 V < V_{DD} < 3.6V, Voltage range 1 C_L = 15 pF	-	-	32(3)(4)	MHz
		1.71 V < V_{DD} < 3.6 V, Voltage range 2 C_L = 15 pF	-	-	16(3)(4)	
$t_{w(CLKH)}$	XSPI clock high and low time (even division)	PRESCALER[7:0] = n = (0, 1, 3, 5, …, 255)	$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2$ - 0.5	-	$t_{(CLK)}/2$ + 0.5	
$t_{w(CLKH)}$	XSPI clock high and low time (odd division)	PRESCALER[7:0] = n = (2, 4, 6, 8, …, 254)	$(n/2)*t_{(CLK)}/(n+1)$ - 0.5	-	$(n/2)*t_{(CLK)}/(n+1)$ + 0.5	
$t_{w(CLKL)}$			$(n/2+1)*t_{(CLK)}/(n+1)$ - 0.5	-	$(n/2+1)*t_{(CLK)}/(n+1)$ + 0.5	
$t_{v(CLK)}$	Clock valid time	-	-	-	$t_{(CLK)}$ + 2	
$t_{h(CLK)}$	Clock hold time	-	$t_{(CLK)}/2$ - 1	-	-	
$t_{w(CS)}$	Chip select high time	-	3 * $t_{(CLK)}$	-	-	ns
$t_{v(DQ)}$	Data input valid time	-	0	-	-	
$t_{v(DS)}$	Data strobe input valid time	-	0	-	-	
$t_{h(DS)}$	Data strobe input hold time	-	0	-	-	
$t_{v(RWDS)}$	Data strobe output valid time	-	-	-	3 * $t_{(CLK)}$	

Table 86. XSPI characteristics in DTR mode (with DQS)(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sr(DQ)}$, $t_{sf(DQ)}$	Data input setup time	-	-1	-	-	ns
$t_{hr(DQ)}$, $t_{hf(DQ)}$	Data input hold time	-	6	-	-	
$t_{vr(OUT)}$ $t_{vf(OUT)}$	Data output valid time DHQC = 0	-	-	5	7	
	Data output valid time DHQC = 1	All prescaler values (except 0)	-	$t_{(CLK)}/4$	$t_{(CLK)}/4 + 2$	
$t_{hr(OUT)}$ $t_{hf(OUT)}$	Data output hold time DHQC = 0	-	2.5	-	-	
	Data output hold time DHQC = 1	All prescaler values (except 0)	$t_{(CLK)}/4 - 2$	-	-	

1. Evaluated by characterization - Not tested in production.
2. Delay block activated.
3. Maximum frequency value are given for a maximum RWDS to DQ skew of ± 1.0 ns.
4. DHQC must be set to reach the mentioned frequency.

Figure 28. XSPI timing diagram - DTR mode



6.3.21 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in *Table 87* are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DD} supply voltage summarized in *Table 34*.

Table 87. Delay block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-			2420	ps
t_{Δ}	Unit delay	-	32	40	64	ps

6.3.22 Wake-up pin (WKUP) characteristics

Pulses on the wake-up pin inputs must have a minimal length, to ensure their detection.

Table 88. WKUP input characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{(WKUP)}$	Pulse length to wake up	-	20	-	-	ns

1. Specified by design, not tested in production.

6.3.23 Analog switch booster

Table 89. Analog switches booster characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply voltage	1.6	1.8	3.6	V
$t_{SU(BOOST)}$	Booster startup time	-	-	50	µs
$I_{DD(BOOST)}$	Booster consumption	-	-	125	µA

1. Specified by design, not tested in production.

6.3.24 12-bit Analog-to-Digital converter (ADC4) characteristics

Unless otherwise specified, the parameters given in the following tables are derived at ambient temperature, and under the f_{HCLK} frequency and supply voltage conditions summarized in *Table 34*.

Note: It is recommended to perform a calibration after each power-up.

Table 90. 12-bit ADC4 characteristics (1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
f_{ADC}	ADC clock frequency	-	0.14	-	55	MHz
$DuCy_{ADC}$	ADC clock duty cycle	-	45	-	55	%
f_s	Sampling rate	Resolution 12 bits	0.010	-	2.75	Msps
		Resolution 10 bits	0.012	-	3.05	
		Resolution 8 bits	0.014	-	3.43	
		Resolution 6 bits	0.0175	-	3.92	
t_{TRIG}	External trigger period	Resolution 12 bits	16	-	-	$1/f_{ADC}$
V_{AIN}(3)	Conversion voltage range	-	0	-	V_{REF+}	V
R_{AIN}(4)	External input impedance	Resolution 12 bits, T_j = 130 °C	-	-	2.2	kΩ
		Resolution 10 bits, T_j = 130 °C	-	-	6.8	
		Resolution 8 bits, T_j = 130 °C	-	-	33.0	
		Resolution 6 bits, T_j = 130 °C	-	-	47.0	

Table 90. 12-bit ADC4 characteristics (1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
$t_{ADCVREG\_STUP}$	ADC voltage regulator startup time	-	-	-	25	µs
t_{STAB}	ADC power-up time	-	(3 x 1/f_{ADC}) + 1 conversion			cycle
t_{OFF_CAL}	Offset calibration time	-	82			1/f_{ADC}
t_{LATR}	Trigger conversion latency	WAIT = 0, AUTOFF = 0, DPD = 0, f_{ADC} = HCLK	4			
		WAIT = 0, AUTOFF = 1, DPD = 0, f_{ADC} = HCLK/2	4			
		WAIT = 0, AUTOFF = 1, DPD = 1, f_{ADC} = HCLK/4	3.75			
t_s	Sampling time	-	1.5	-	814.5	
t_{CONV}	Total conversion time (including sampling time)	Resolution = N bits, VREFPROTEN = 0	t_s + N + 0.5			
		Resolution = N bits, VREFPROTEN = 1, VREFSECSMP = 0	t_s + N + 0.5	-	t_s + N + 1.5	
		Resolution = N bits, VREFPROTEN = 1, VREFSECSMP = 1	t_s + N + 0.5	-	t_s + N + 2.5	
$I_{DDA(ADC)}$	ADC consumption on V_{DDA}	f_s = 2.5 Msps	-	378	-	µA
		f_s = 1 Msps	-	190	-	
		f_s = 10 ksps	-	10	-	
		AUTOFF = 1, DPD = 0, no conversion	-	9	-	
		AUTOFF = 1, DPD = 1, no conversion	-	0.11	-	

1. Specified by design, not tested in production.
2. The voltage booster on the ADC switches must be used when V_{DDA} < 2.4 V (embedded I/O switches).
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. The tolerance is two LSBs.

Table 91. Maximum R_{AIN} for 12-bit ADC4(1)(2)(3)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
12 bits	47	276	12.5	19.5
	68	288		
	100	306		
	150	336		

Table 91. Maximum R_{AIN} for 12-bit ADC4[(1)(2)(3)] (continued)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
12 bits (continued)	220	377	19.5	39.5
	330	442		
	470	526		
	680	650	39.5	
	1000	840		79.5
	1500	1134		
	2200	1643	79.5	814.5
	3300	2395	814.5	
	4700	3342		
	6800	4754		
	10000	6840		
	15000	9967		
	22000	14068		
	33000	19933		N/A
10 bits	47	86	3.5	7.5
	68	90		
	100	95		
	150	108	7.5	
	220	116		
	330	136		
	470	161		12.5
	680	212		
	1000	276	12.5	19.5
	1500	376	19.5	39.5
	2200	516		79.5
	3300	735	39.5	
	4700	1012		
	6800	1423	79.5	814.5
	10000	2040	814.5	814.5
	15000	2978		
	22000	4356		
	33000	6443		
	47000	8925		

Table 91. Maximum R_{AIN} for 12-bit ADC4[(1)(2)(3)] (continued)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
8 bits	47	45	3.5	3.5
	68	46		
	100	48		
	150	53		
	220	59		
	330	69		7.5
	470	81		
	680	101	7.5	
	1000	130		
	1500	177		12.5
	2200	242	12.5	19.5
	3300	345		
	4700	475	19.5	39.5
	6800	670	39.5	
	10000	963		79.5
	15000	1417	79.5	
	22000	2040		814.5
	33000	2995	814.5	
	47000	4158		
6 bits	47	32	1.5	3.5
	68	32		
	100	33		
	150	35		
	220	37		
	330	41		
	470	49	3.5	
	680	61		
	1000	79		7.5
	1500	106	7.5	
	2200	146		12.5
	3300	207		
	4700	286	12.5	19.5
	6800	404	19.5	39.5
	10000	584	39.5	

Table 91. Maximum R_{AIN} for 12-bit ADC4(1)(2)(3) (continued)

Resolution	R_{AIN} (Ω)	Sampling time (ns)	Sampling cycles at 35 MHz	Sampling cycles at 55 MHz
6 bits (continued)	22000	1250	79.5	79.5
	33000	1853		814.5
	47000	2607	814.5	

1. Specified by design, not tested in production.
2. BOOSTEN and ANASWVDD configured according to V_{DD} and V_{DDA} levels.
3. Values without external capacitance.

Table 92. 12-bit ADC4 accuracy(1)(2)(3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error	-	-	±3	±7.5	LSB
EO	Offset error		-	±2	±5.5	
EG	Gain error		-	±2	±6.5	
ED	Differential linearity error		-	-0.9/+1.0	-0.9/+1.5	
EL	Integral linearity error		-	±2	±3.5	
ENOB	Effective number of bits		9.9	10.9	-	bits
SINAD	Signal-to-noise and distortion ratio		61.4	67.4	-	dB
SNR	Signal-to-noise ratio		61.6	67.5	-	
THD	Total harmonic distortion		-	-74	-70	

1. Evaluated by characterization, not tested in production.
2. DC accuracy values are measured after internal calibration.
3. The I/O analog switch voltage booster is enabled when V_{DDA} < 2.4 V (resolution = 12 bits, no oversampling).

Figure 29. ADC accuracy characteristics

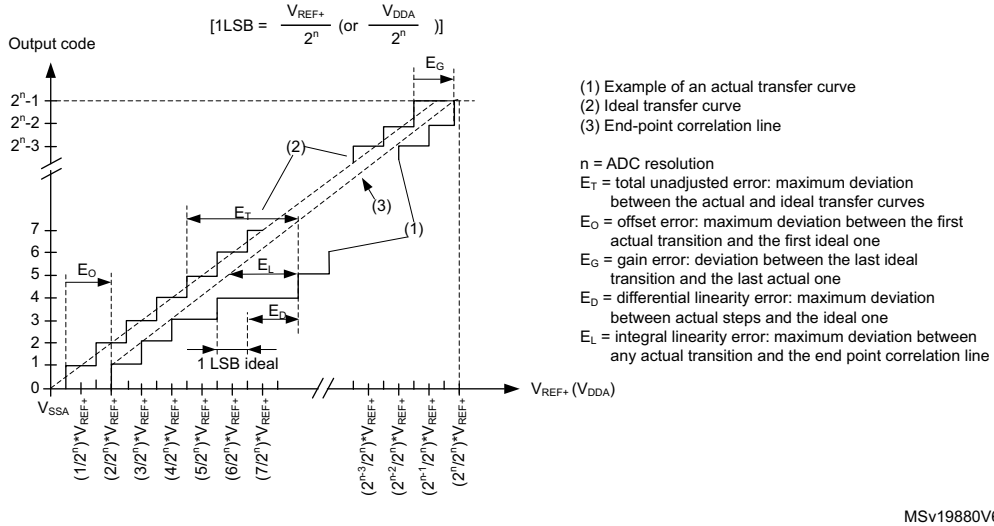
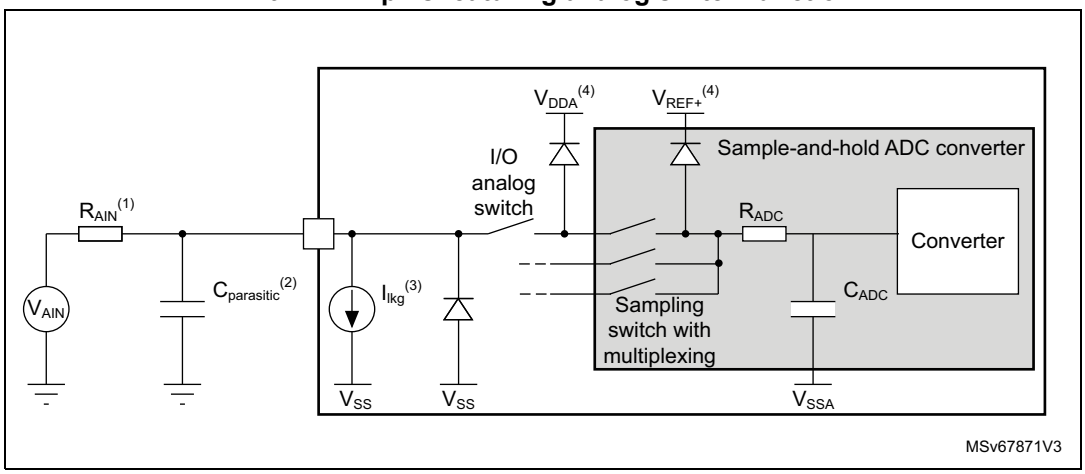


Figure 30. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



1. Refer to *Table 90* for the values of R_{AIN} and C_{ADC}.
2. $C_{parasitic}$ represents the PCB capacitance (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to *Table 79* for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades the conversion accuracy. As a remedy, reduce f_{ADC}.
3. Refer to *Table 79* for the values of I_{lkg}.
4. Refer to *Figure 18*, *Figure 19*, and *Figure 20*.

6.3.25 Temperature sensor characteristics

Table 93. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)(2)	V_{SENSE} linearity with temperature	-	-	1.3	°C
Avg_Slope(3)	Average slope	2	2.5	3.0	mV/ °C
$V_{SENSE30}$(4)	V_{SENSE} at V_{REF+} = V_{DDA} = 3.0 V (±10 mV) and 30 °C (±1 °C)	700	742	800	mV
($V_{continous0}$ - $V_{sampling}$)(2)	Voltage difference between continuous and sampling modes(5)	-10	-	+4	mV
$t_{START(TS\_BUF)}$(2)	Sensor buffer startup time	-	1	10	µs
t_{S_temp}(2)	ADC sampling time when reading the temperature	13	-	-	µs
$I_{DD(TS)}$(2)	Consumption from V_{DD}, when selected by ADC	-	14	20	µA

1. V_{SENSE} linearity depends upon calibration points. When using TS_CALx calibration points, linearity within the calibration limits is degraded by ±5 °C. Linearity outside the calibration limits is degraded more, due to the extrapolation.
2. Specified by design, not tested in production.
3. Evaluated by characterization, not tested in production, unless otherwise specified.
4. The $V_{SENSE30}$ ADC4 conversion result is stored in the TS_CAL1 field.
5. The temperature sensor is in continuous mode when the regulator is in range 1, in sampling mode when the regulator is in range 2 or the device is in Stop 1 mode.

6.3.26 V_{CORE} monitoring characteristics

Table 94. V_{CORE} monitoring characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
T_{S_VCORE}	ADC sampling time when reading the V_{CORE} voltage	1	-	-	µs

1. Specified by design, not tested in production.

6.3.27 Timer characteristics

The parameters given in *Table 95*, *Table 96*, and *Table 96* are specified by design. Refer to *Section 4.3* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 95. TIMx(1) characteristics(2)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	10	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 64 MHz	0	50	
Res_{TIM}	Timer resolution	TIM16, TIM17	-	16	bit
		TIM2	-	32	
$t_{COUNTER16}$	16-bit counter period	-	1	2^{16}	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 64 MHz	0.01	655.36	µs
$t_{COUNTER32}$	32-bit counter period	-	1	2^{32}	$t_{TIMxCLK}$
		$f_{TIM2CLK}$ = 64 MHz	0,01	42.94	s

1. TIMx is used as a general term, where x stands for 2, 16, or 17.
2. Specified by design, not tested in production.

Table 96. IWDG min/max timeout period at 32 kHz(1)(2)

Prescaler divider	PR[3:0] bits	Min timeout RL[11:0] = 0x002	Max timeout RL[11:0] = 0xFFF	Unit
/4	0	0.325	512	ms
/8	1	0.750	1024	
/16	2	1.500	2048	
/32	3	3.0	4096	
/64	4	6.0	8192	
/128	5	12.0	16384	
/256	6	24.0	32768	
/512	7	48.0	65536	
/1024	Others	96.0	131072	

1. The exact timings depend upon the phasing of the APB interface clock vs. the IWDG kernel clock, hence there is always a full kernel clock period of uncertainty.
2. Specified by design, not tested in production.

6.3.28 I2C interface characteristics

The I2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): bit rate up to 100 kbit/s
- Fast-mode (Fm): bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): bit rate up to 1 Mbit/s.

The I2C timings requirements are specified by design, not tested in production, when the I2C peripheral is properly configured (refer to product reference manual).

The SDA and SCL I/O requirements are met with the following restriction: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.17* for I2C I/O characteristics.

All I^2C SDA and SCL I/Os embed an analog filter, refer to *Table 97* for its characteristics.

Table 97. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes suppressed by the analog filter	50(2)	190(3)	ns

1. Specified by design, not tested in production.
2. Spikes with widths below t_{AF} min are filtered.
3. Spikes with widths above t_{AF} max are not filtered.

6.3.29 USART characteristics

Unless otherwise specified, the parameters given in *Table 98* are derived under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 34*, with the following configuration:

- Output speed set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30pF
- Measurement points are done at 0.5 V_{DD}
- I/O compensation cell activated
- Voltage scaling range 1

Refer to *Section 4.3* for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 98. USART characteristics(1)

Symbol	Parameter	Conditions	Min	Typ 3.3 V	Max	Unit
f_{CK}	USART clock frequency	Master mode, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	-	8	MHz
		Slave receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	-	21	
		Slave transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	21	
		Slave transmitter, 1.71 V ≤ V_{DD} < 2.7 V	-	-	21	
$t_{su(NSS)}$	NSS setup time	Slave mode	t_{ker}(2) + 2	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	4	-	-	
$t_{w(CKH)}$ $t_{w(CKL)}$	CK high and low time	Master mode	$(1/f_{CK}) / 2 - 1.5$	$(1/f_{CK}) / 2$	$(1/f_{CK}) / 2 + 1.5$	
$t_{su(RX)}$	Data input setup time	Master mode	20	-	-	
		Slave mode	23	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	1	-	-	
		Slave mode	1.5	-	-	
$t_{v(TX)}$	Data output valid time	Slave mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	12	15.5	
		Slave mode, 1.71 V ≤ V_{DD} < 2.7 V	-		22	
		Master mode	-	1	2	
$t_{h(TX)}$	Data output hold time	Slave mode	10	-	-	
		Master mode	0	-	-	

1. Evaluated by characterization, not tested in production, unless otherwise specified.
2. t_{ker} is the usart_ker_ck_pres clock period.

Figure 31. USART timing diagram in master mode

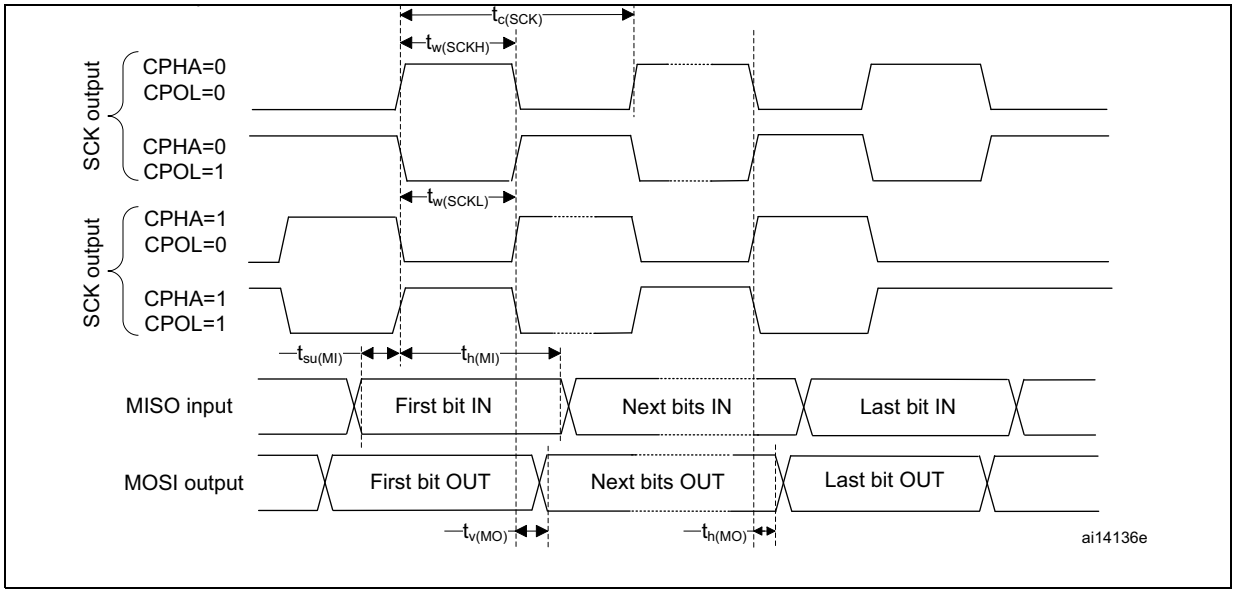
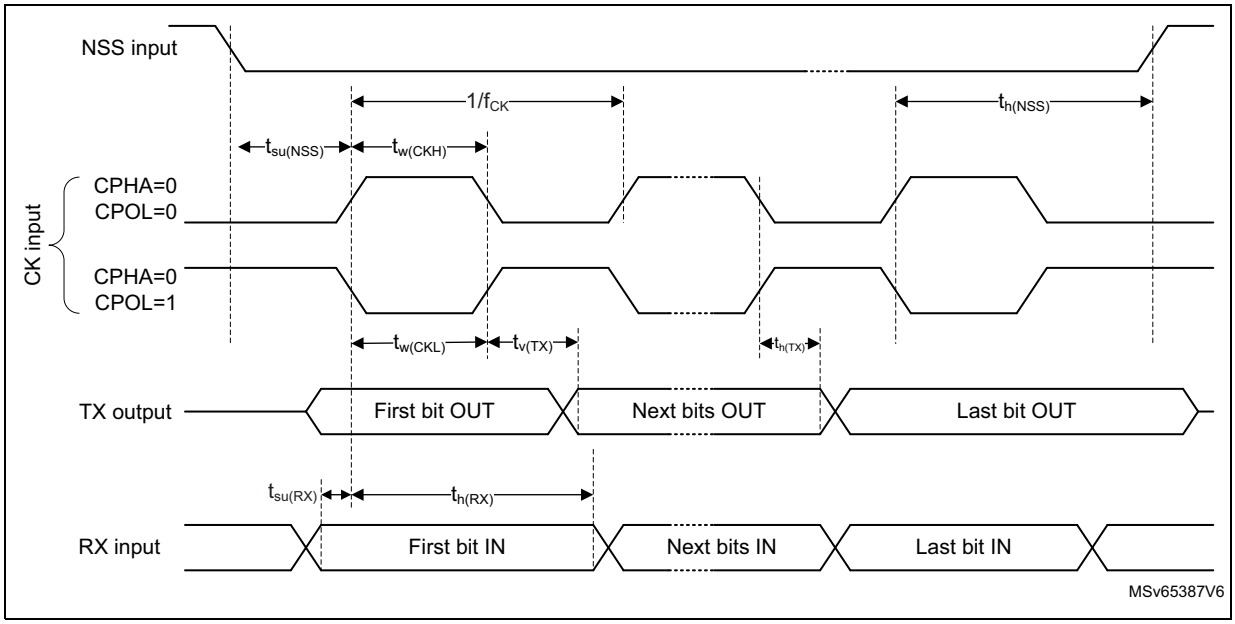


Figure 32. USART timing diagram in slave mode



6.3.30 SPI characteristics

Unless otherwise specified, the parameters given in *Table 99* are under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 34*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at 0.5 V_{DD}
- I/O compensation cell activated

Refer to *Section 4.3* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 99. SPI characteristics(1)

Symbol	Parameter	Conditions	Min	Typ 3.3 V	Max	Unit
f_{SCK}	Clock frequency	Master receiver mode 2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	32	MHz
		Master receiver mode 1.71 V ≤ V_{DD} < 2.7 V			32	
		Master transmitter mode 2.7 V ≤ V_{DD} < 3.6 V			32	
		Master transmitter mode 1.71 V ≤ V_{DD} < 2.7 V			32	
		Slave receiver mode 1.71 V ≤ V_{DD} ≤ 3.6 V			32	
		Slave transmitter mode 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 1			32(2)	
		Slave transmitter mode 1.71 V ≤ V_{DD} < 2.7 V, voltage range 1			20(2)	
		Slave transmitter mode 1.71 V ≤ V_{DD} ≤ 3.6 V, voltage range 2			16	
$t_{su(NSS)}$	NSS setup time	Slave mode	4 × T_{pclk}	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	2 × T_{pclk}	-	-	
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	t_{SCK}(3)/2 - 1	t_{SCK}(3)/2	t_{SCK}(3)/2 + 1	
$t_{su(MI)}$	Data input setup time	Master mode	4	-	-	ns
$t_{su(SI)}$		Slave mode	1.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	2	-	-	
$t_{h(SI)}$		Slave mode	1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9.5	14.5	25	
$t_{dis(SO)}$	Data output disable time		10.5	13	21	

Table 99. SPI characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ 3.3 V	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 1	-	10.5	15.5	ns
		Slave mode (after enable edge) 1.71 V ≤ V_{DD} < 2.7 V, voltage range 1	-	16.5	25	
		Slave mode (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 2	-	14	19	
		Slave mode (after enable edge) 1.71 V ≤ V_{DD} < 2.7 V, voltage range 2	-	21	30	
$t_{v(MO)}$		Master mode	-	1	2.5	
$t_{h(SO)}$	Data output hold time	Slave mode	7.5	-	-	
$t_{h(MO)}$		Master mode	0.5	-	-	

1. Evaluated by characterization, not tested in production.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$, which must fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when SPI communicates with a master having $t_{su(MI)}$ = 0 while $Duty_{(SCK)}$ = 50%.
3. $t_{SCK} = t_{spi\_ker\_ck}$ x baudrate prescaler

Figure 33. SPI timing diagram - Slave mode and CPHA = 0

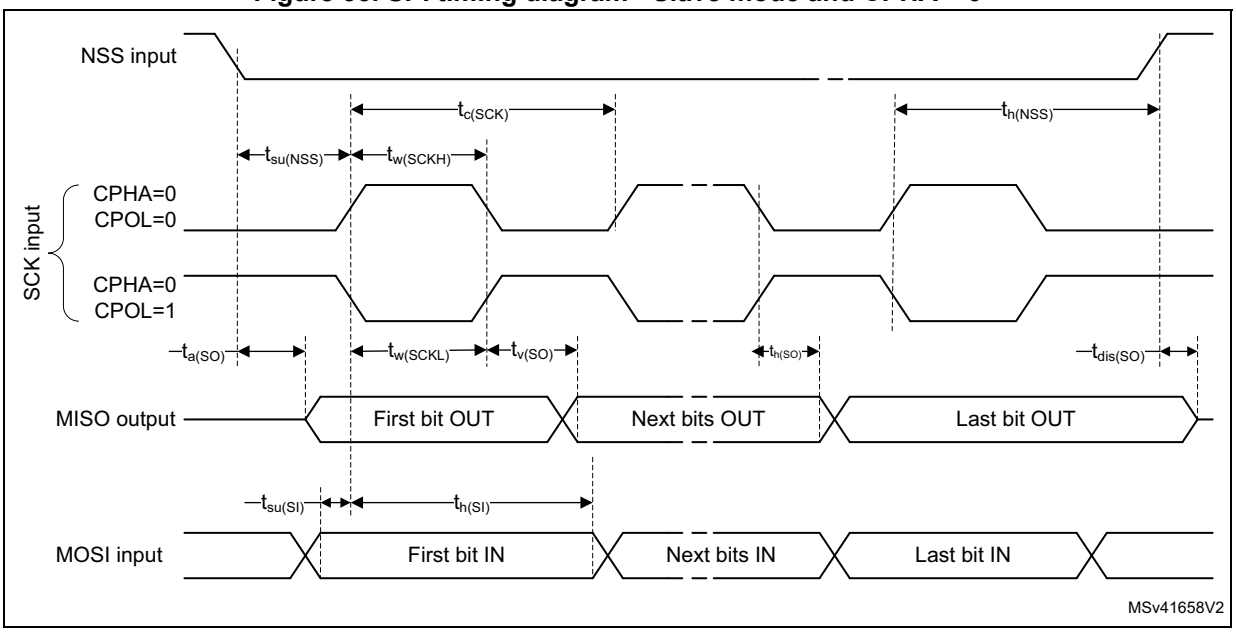


Figure 34. SPI timing diagram - Slave mode and CPHA = 1

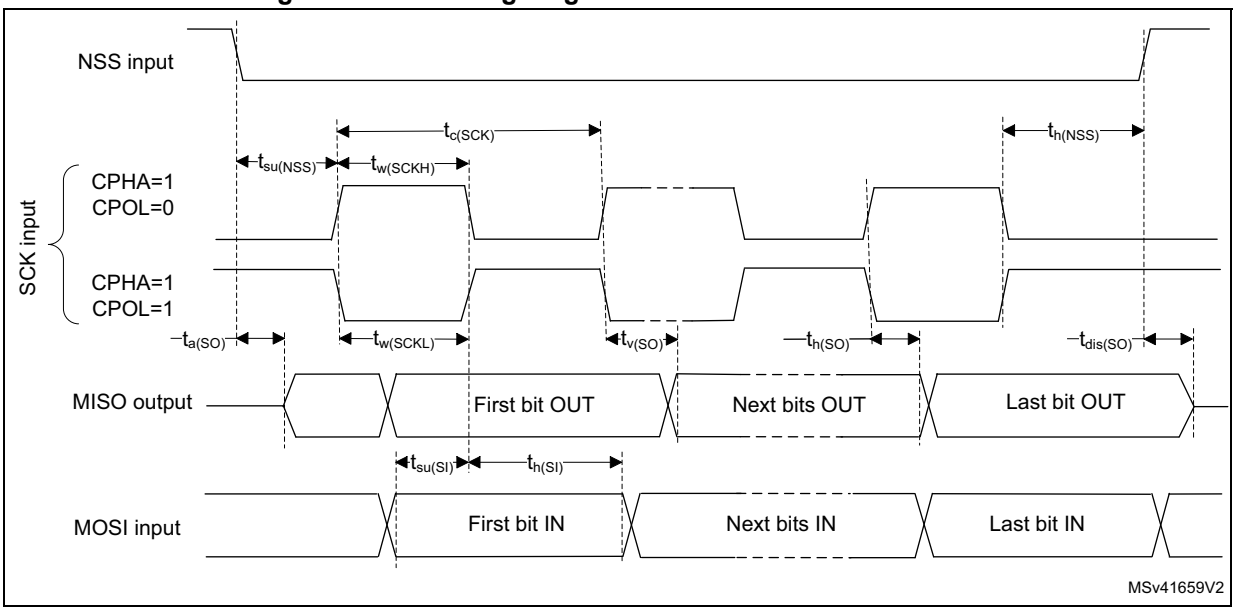
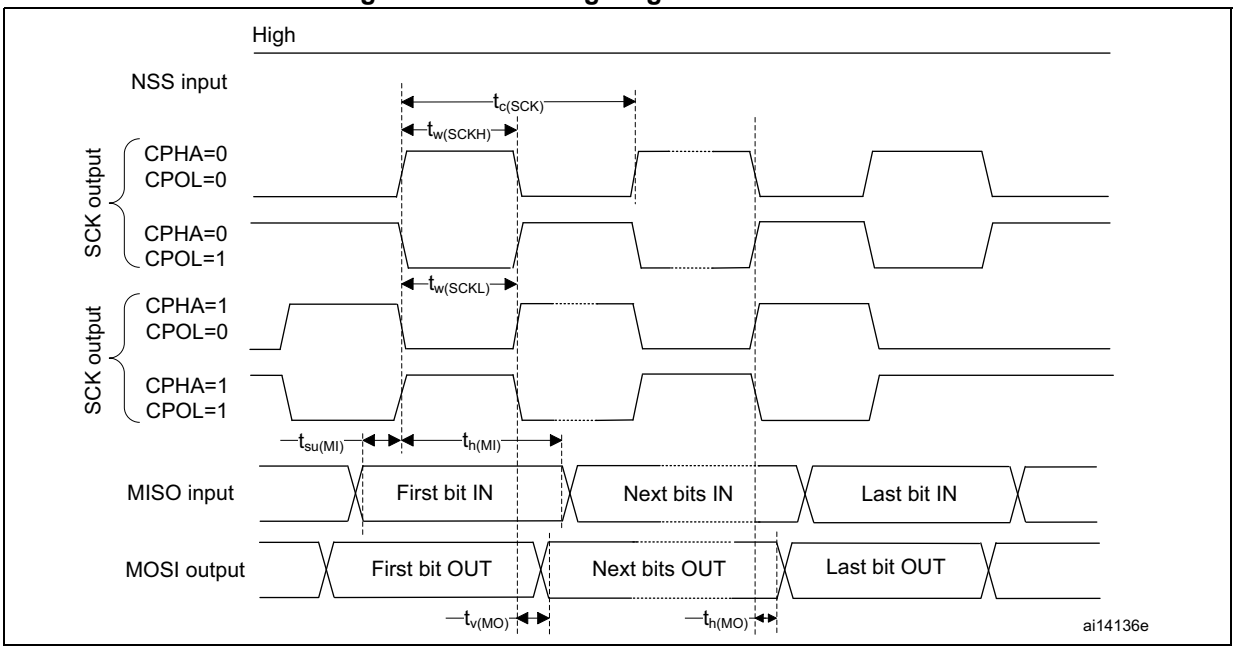


Figure 35. SPI timing diagram - Master mode



6.3.31 SAI characteristics

Unless otherwise specified, the parameters given in *Table 100* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 34*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- I/O compensation cell activated
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to *Section 4.3* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 100. SAI characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	Main clock output	-	-	50	MHz
f_{CK}	Clock frequency	Master transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	24	
		Master transmitter, 1.71 V ≤ V_{DD} < 2.7 V	-	17	
		Master receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	18	
		Slave transmitter, 2.7 V ≤ V_{DD} ≤ 3.6 V Voltage range 1	-	25.5	
		Slave transmitter, 1.71 V ≤ V_{DD} < 2.7 V Voltage range 1	-	18.5	
		Slave transmitter, 1.71 V ≤ V_{DD} ≤ 3.6 V Voltage range 2	-	12.5	
		Slave receiver, 1.71 V ≤ V_{DD} ≤ 3.6 V	-	50	
$t_{v(FS)}$	F_S valid time	Master mode, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	19.5	ns
		Master mode, 1.71 V ≤ V_{DD} < 2.7 V	-	27.5	
$t_{su(FS)}$	F_S setup time	Slave mode	10	-	
$t_{h(FS)}$	F_S hold time	Master mode	1	-	
		Slave mode	1	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	5	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	2.5	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	2	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	3	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge), 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 1	-	19.5	
		Slave transmitter (after enable edge), 1.71 V ≤ V_{DD} < 2.7 V, voltage range 1	-	27	
		Slave transmitter (after enable edge), 2.7 V ≤ V_{DD} ≤ 3.6 V, voltage range 2	-	31.5	
		Slave transmitter (after enable edge), 1.71 V ≤ V_{DD} < 2.7 V, voltage range 2	-	40	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge) Voltage range 1	10	-	
		Slave transmitter (after enable edge) Voltage range 2	21.5	-	

Table 100. SAI characteristics[1][2] (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V_{DD} ≤ 3.6 V	-	20.5	ns
		Master transmitter (after enable edge) 1.71 V ≤ V_{DD} < 2.7 V	-	30	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	9	-	

1. Evaluated by characterization - Not tested in production.
2. APB clock frequency must be at least two times the SAI clock frequency.

Figure 36. SAI master timing waveforms

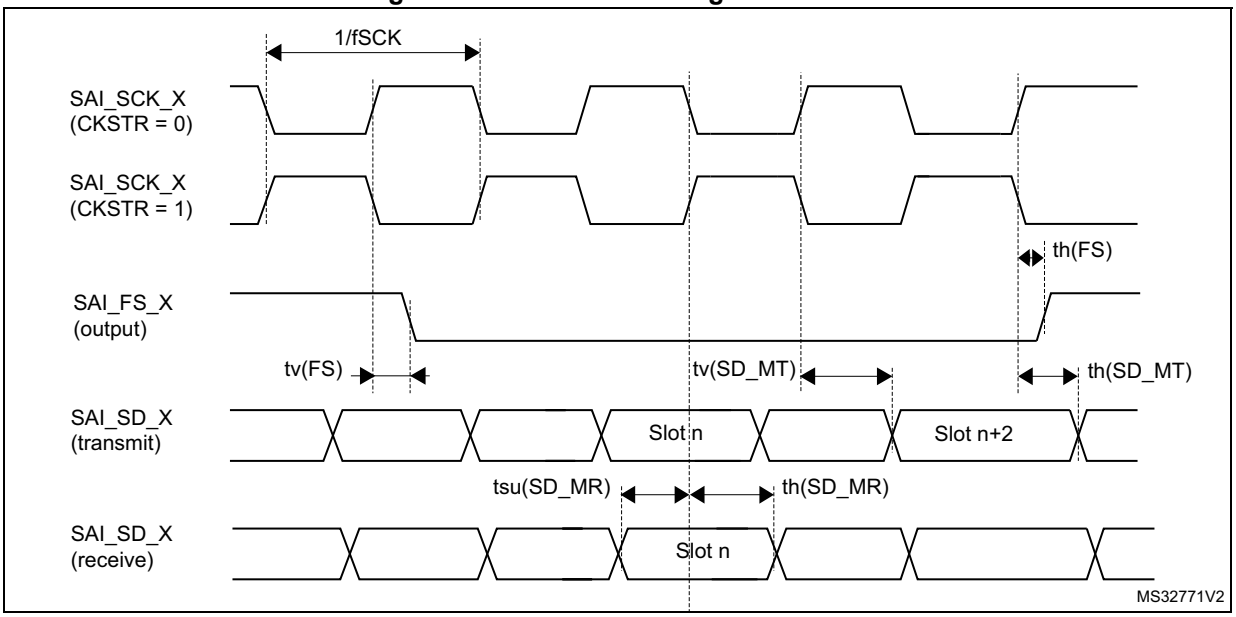
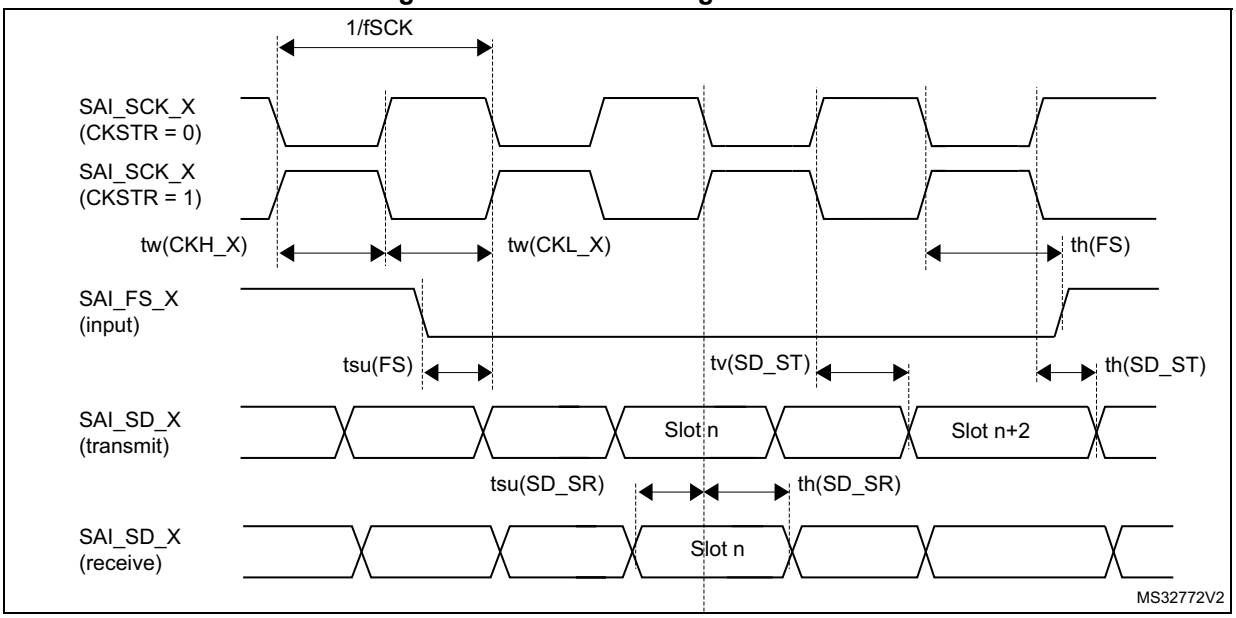


Figure 37. SAI slave timing waveforms



6.3.32 USB_FS characteristics

Table 101. USB_FS characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDUSB}	USB transceiver operating supply voltage	-	3.0(1)	-	3.6	V
$t_{STARTUP}$(2)	USB transceiver startup time	-	-	-	1	µs
R_{PUI}	Embedded USB_DP pullup value during idle	-	900	-	1575	Ω
R_{PUR}	Embedded USB_DP pullup value during reception	-	1425	-	3090	
Z_{DRV}	Output driver impedance(3)	High and low driver	28	36	44	

1. USB functionality is ensured down to 2.7 V, but some USB electrical characteristics are degraded in 2.7 to 3.0 V range.
2. Guaranteed by design.
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-). The matching impedance is already included in the embedded driver.

6.3.33 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 102* and *Table 103* are with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at 0.5 x V_{DD}
- I/O compensation cell disabled

Table 102. JTAG characteristics(1)

Symbol	Parameter	Conditions	Min	Typ 3.3 V	Max	Unit
f_{TCK}	TCK clock frequency	$2.7 \le V_{DD} \le 3.6$ V	-	-	21.5	MHz
		$1.71 \le V_{DD} < 2.7$ V	-	-	16.5	
$t_{isu(TMS)}$	TMS input setup time	-	1.5	-	-	ns
$t_{ih(TMS)}$	TMS input hold time	-	6	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	1.5	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	4	-	-	
$t_{ov(TDO)}$	TDO output valid time	$2.7 \le V_{DD} \le 3.6$ V	-	17	23	
		$1.71 \le V_{DD} < 2.7$ V	-	17	29.5	
$t_{oh(TDO)}$	TDO output hold time	-	13	-	-	

1. Evaluated by characterization, not tested in production.

Table 103. SWD characteristics(1)

Symbol	Parameter	Conditions	Min	Typ 3.3 V	Max	Unit
f_{SWCLK}	SWCLK clock frequency	$2.7 \le V_{DD} \le 3.6$ V	-	-	62.5	MHz
		$1.71 \le V_{DD} < 2.7$ V	-	-	34	
$t_{isu(SWDIO)}$	SWDIO input setup time	-	1.5	-	-	ns
$t_{ih(SWDIO)}$	SWDIO input hold time	-	3.5	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	$2.7 \le V_{DD} \le 3.6$ V	-	12	16	
		$1.71 \le V_{DD} < 2.7$ V	-	12	29	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	8.5	-	-	

1. Evaluated by characterization, not tested in production.

Figure 38. JTAG timing diagram

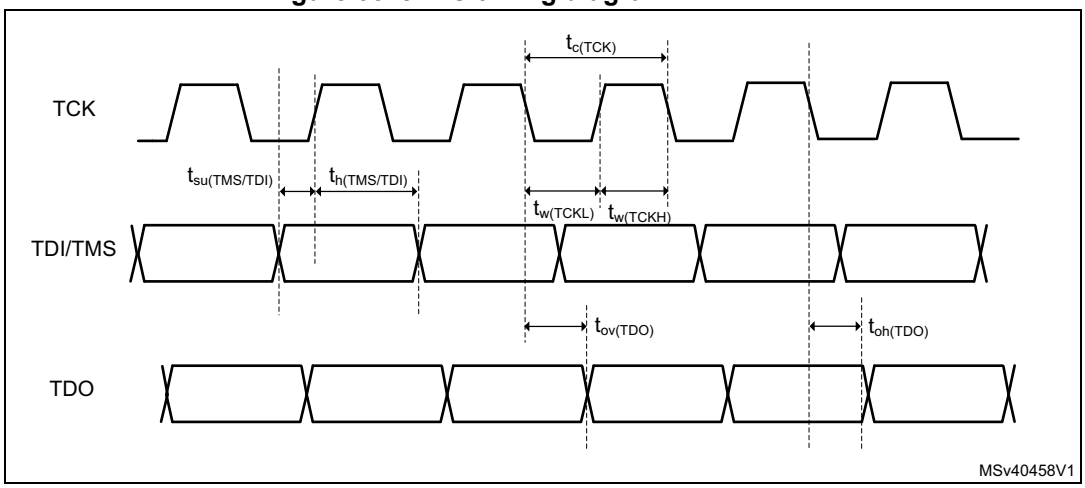
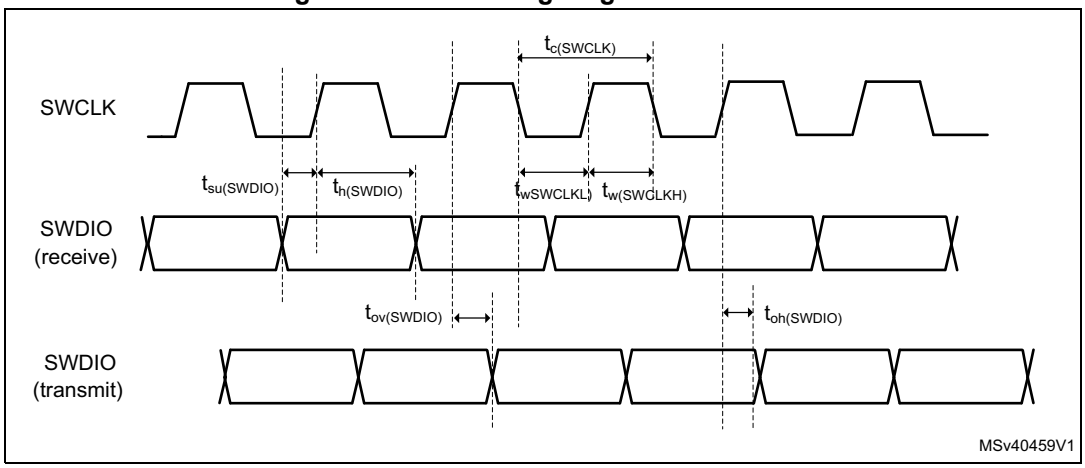


Figure 39. SWD timing diagram



7 Ordering information

Example: STM32 WB A25 C E U 6 TR

Device family

STM32 = Arm® based 32-bit microcontroller

Product type

WB = Wireless Bluetooth® LE

Device subfamily

A23 = Die A2, crossover

A25 = Die A2, full set of features, SMPS

Pin count

K = 32 pins

H = 37 pins

C = 48 pins

Flash memory size

E = 512 Kbytes

Package

U = UFQFPN

F = Thin WLCSP

Temperature range

6 = Industrial temperature range, -40 to 85 °C

7 = Industrial temperature range, -40 to 105 °C

Packing

TR = tape and reel

xxx = programmed parts

For a list of available options (memory, package, and so on), or for further information on any aspect of this device, contact your nearest ST sales office.

8 Important security notice

The STMicroelectronics group of companies (ST) places a high value on product security, which is why the ST product(s) identified in this documentation may be certified by various security certification bodies and/or may implement our own security measures as set forth herein. However, no level of security certification and/or built-in security measures can guarantee that ST products are resistant to all forms of attacks. As such, it is the responsibility of each of ST's customers to determine if the level of security provided in an ST product meets the customer needs both in relation to the ST product alone, as well as when combined with other components and/or software for the customer end product or application. In particular, take note that:

- ST products may have been certified by one or more security certification bodies, such as Platform Security Architecture (www.psacertified.org) and/or Security Evaluation standard for IoT Platforms (www.trustcb.com). For details concerning whether the ST product(s) referenced herein have received security certification along with the level and current status of such certification, either visit the relevant certification standards website or go to the relevant product page on *www.st.com* for the most up to date information. As the status and/or level of security certification for an ST product can change from time to time, customers should re-check security certification status/level as needed. If an ST product is not shown to be certified under a particular security standard, customers should not assume it is certified.
- Certification bodies have the right to evaluate, grant and revoke security certification in relation to ST products. These certification bodies are therefore independently responsible for granting or revoking security certification for an ST product, and ST does not take any responsibility for mistakes, evaluations, assessments, testing, or other activity carried out by the certification body with respect to any ST product.
- Industry-based cryptographic algorithms (such as AES, DES, or MD5) and other open standard technologies which may be used in conjunction with an ST product are based on standards which were not developed by ST. ST does not take responsibility for any flaws in such cryptographic algorithms or open technologies or for any methods which have been or may be developed to bypass, decrypt or crack such algorithms or technologies.
- While robust security testing may be done, no level of certification can absolutely guarantee protections against all attacks, including, for example, against advanced attacks which have not been tested for, against new or unidentified forms of attack, or against any form of attack when using an ST product outside of its specification or intended use, or in conjunction with other components or software which are used by customer to create their end product or application. ST is not responsible for resistance against such attacks. As such, regardless of the incorporated security features and/or any information or support that may be provided by ST, each customer is solely responsible for determining if the level of attacks tested for meets their needs, both in relation to the ST product alone and when incorporated into a customer end product or application.
- All security features of ST products (inclusive of any hardware, software, documentation, and the like), including but not limited to any enhanced security features added by ST, are provided on an "AS IS" BASIS. AS SUCH, TO THE EXTENT PERMITTED BY APPLICABLE LAW, ST DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, unless the applicable written and signed contract terms specifically provide otherwise.

9 Revision history

Table 104. Document revision history

Date	Revision	Changes
23-Feb-2026	1	Initial release.
24-Feb-2026	2	*Section: Features* updated.