STM32MP231C/F STM32MP233C/F STM32MP235C/F

Datasheet

Arm® based dual Cortex®-A35 1.5 GHz + Cortex®-M33 MPU, AI, 3D GPU, video decoder, TFT/DSI/LVDS, USB 2.0, crypto

TFBGA361 (16 × 16 mm) pitch 0.8 mm
VFBGA361 (10 × 10 mm) pitch 0.5 mm
VFBGA424 (14 × 14 mm) pitch 0.5 mm

Product summary	
STM32MP23xC/F	STM32MP231C, STM32MP231F, STM32MP233C, STM32MP233F, STM32MP235C, STM32MP235F

Features

Includes ST state-of-the-art patented technology.

Cores

- Up to 64-bit dual-core Arm® Cortex®-A35
  - Up to 1.5 GHz
  - 32-Kbyte I + 32-Kbyte D level 1 cache for each core
  - 512-Kbyte unified level 2 cache
  - Arm® NEON™ and Arm® TrustZone®
- 32-bit Arm® Cortex®-M33 with FPU/MPU
  - Up to 400 MHz
  - L1 16-Kbyte I / 16-Kbyte D
  - Arm® TrustZone®

Memories

- External DDR memory up to 4 Gbytes
  - Up to DDR3L-2133 16-bit
  - Up to DDR4-2400 16-bit
  - Up to LPDDR4-2400 16-bit
- 776-Kbyte internal SRAM: 256-Kbyte AXI SYSRAM, 128-Kbyte AXI video RAM or SYSRAM extension, 256-Kbyte AHB SRAM, 128-Kbyte AHB SRAM with ECC in backup domain, 8-Kbyte SRAM with ECC in backup domain
- Two Octo-SPI memory interfaces
- Flexible external memory controller with up to 16-bit data bus: parallel interface to connect external ICs, and SLC NAND memories with up to 8-bit ECC

Security/safety

- Secure boot, TrustZone® peripherals, active tamper, environmental monitors, display secure layers, hardware accelerators
- Complete resource isolation framework

Reset and power management

- 1.71 to 1.95 V and 2.7/3.0 to 3.6 V multiple section I/O supply
- POR, PDR, PVD, and BOR
- On-chip LDO and power-switches for RETRAM, BKPSRAM, V_{SW}, and SmartRun domains
- Dedicated supplies for Cortex®-A35 and GPU/NPU (if present)
- Internal temperature sensors
- Low-power modes: Sleep, Stop, and Standby
- DDR memory retention in Standby mode
- Controls for PMIC companion chip

Low-power consumption

Clock management

- Internal oscillators: 64 MHz HSI, 4/16 MHz MSI, 32 kHz LSI
- External oscillators: 16-48 MHz HSE, 32.768 kHz LSE
- Up to 8× PLLs with fractional mode

General-purpose inputs/outputs

- Up to 144 secure I/O ports with interrupt capability
  - Up to 6 wake-up inputs
  - Up to 7 tamper input pins + 5 active tampers output pins

Interconnect matrix

- Bus matrices
  - 128-, 64-, 32-bit STNoC interconnect, up to 600 MHz
  - 32-bit Arm® AMBA® AHB interconnect, up to 400 MHz

3 DMA controllers to unload the CPU

- 48 physical channels in total
- 3× dual master port, high-performance, general-purpose, direct memory access controller (HPDMA), 16 channels each

Up to 39 communication peripherals

- 4× I^2C FM+ (1 Mbit/s, SMBus/PMBus®)
- 3× I^3C (12.5 Mbit/s)
- 3× UART + 4× USART (12.5 Mbit/s, ISO7816 interface, LIN, IrDA, SPI) + 1× LPUART
- 6× SPI (50 Mbit/s, including 3 with full duplex I^2S audio class accuracy via internal audio PLL or external clock)(+2 with OCTOSPI + 4 with USART)
- 4× SAI (stereo audio: I^2S, PDM, SPDIF Tx)
- SPDIF Rx with 4 inputs
- 3× SDMMC up to 8-bit (SD/e•MMC™/SDIO)
- Up to 2× CAN controllers supporting CAN FD protocol, out of which one supports time-triggered CAN (TTCAN)
- 1× USB 2.0 high-speed Host with embedded 480 Mbits/s PHY
- 1× USB 2.0 high-speed dual role data with embedded 480 Mbits/s PHY
- 1× USB Type-C® Power Delivery control with two CC lines PHY
- Up to 2× Gigabit Ethernet interfaces
  - 1× Gigabit Ethernet GMAC with one external PHY interface (optional)
  - 1× Gigabit Ethernet GMAC with one external PHY interface
  - TSN, IEEE 1588v2 hardware, MII/RMII/RGMII
- Camera interface #1 (5 Mpixels at 30 fps)
  - MIPI CSI-2®, 2× data lanes up to 2.5 Gbit/s each
  - 8- to 16-bit parallel, up to 120 MHz
  - RGB, YUV, JPG, RawBayer with Lite-ISP
  - Lite-ISP, demosaicing, downscaling, cropping, 3 pixel pipelines

- Camera interface #2 (1 Mpixels at 15 fps)
  - 8- to 14-bit parallel, up to 80 MHz
  - RGB, YUV, JPG
  - Cropping
- Digital parallel interface up to 16-bit input or output

6 analog peripherals

- 3 × ADCs with 12-bit max. resolution (up to 5 Msps each, up to 23 channels)
- Internal temperature sensor (DTS)
- 1× multifunction digital filter (MDF) with up to 4 channels/4 filters
- Internal (VREFBUF) or external ADC reference V_{REF+}

Graphics

- Optional 3D GPU: VeriSilicon® - Up to 400 MHz
  - OpenGL® ES 3.1 - Vulkan 1.3
  - OpenCL™ 3.0, OpenVX™ 1.3
  - Up to 66.5 Mtriangle/s, 400 Mpixel/s
- LCD-TFT controller, up to 24-bit // RGB888
  - Up to FHD (1920 × 1080) at 60 fps
  - 3 layers including a secure layer
  - YUV support, 90° output rotation
- Optional MIPI DSI®, 4× data lanes, up to 2.5 Gbit/s each
  - Up to QXGA (2048 × 1536) at 60 fps
- Optional FPD-1 and OpenLDI JEIDA/VESA (LVDS), 4× data lanes, up to 1.1 Gbit/s per lane
  - Up to FHD (1920 × 1080) at 60 fps

Artificial intelligence

- Optional NPU: VeriSilicon® - Up to 400 MHz
  - TensorFlowLite - ONNX - Linux NN

Video processing

- Optional hardware video decoder up to 600 MHz
  - H264/VP8 up to FHD (1920×1080) at 60 fps
  - JPEG up to 500 Mpixel/s
  - 128 Kbytes of video RAM

Up to 32 timers and 5 watchdogs

- 4× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- 2× 16-bit advanced motor control timers
- 10× 16-bit general-purpose timers (including 2 basic timers without PWM)
- 5× 16-bit low-power timers
- Secure RTC with subsecond accuracy and hardware calendar
- Up to 2× 4 Cortex®-A35 system timers (secure, non-secure, virtual, hypervisor)
- 2× SysTick Cortex®-M33 timer (secure, non-secure)
- 5× watchdogs (4× independent and 1× window)

Hardware acceleration

- AES-128, -192, -256, DES/TDES
- Secure AES-256 with SCA
- RSA, ECC, ECDSA with SCA

- HASH (SHA-1, SHA-224, SHA-256, SHA3), HMAC
- True random number generator
- CRC calculation unit
- “On-the-fly” DDR encryption/decryption (AES-128)
- “On-the-fly” OTFDEC Octo-SPI flash memory decryption (AES-128)

Debug mode

- Arm® CoreSight™ trace and debug: SWD and JTAG interfaces

12288-bit fuses including 96-bit unique ID

All packages are ECOPACK2 compliant

1 Introduction

This document provides information on STM32MP23xC/F devices, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging and ordering information.

It must be read in conjunction with the STM32MP23/25xx reference manual (RM0457).

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32MP23xx/25xx device errata (ES0598).

For information on the Arm® Cortex®- M33 core, refer to the Cortex®- M33 Technical Reference Manual, available from the www.arm.com website.

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2 Description

STM32MP23xC/F devices are based on the high-performance single or dual-core Arm® Cortex®-A35 64-bit RISC core operating at up to 1.5 GHz. The Cortex®-A35 processor includes a 32-Kbyte L1 instruction cache for each CPU, a 32-Kbyte L1 data cache for each CPU, and a 512-Kbyte L2 cache. The Cortex®-A35 processor uses a highly efficient 8-stage in-order pipeline that has been extensively optimized to provide full Armv8-A features while maximizing area and power efficiency.

STM32MP23xC/F devices also embed a Cortex®-M33 32-bit RISC core operating at up to 400 MHz frequency. The Cortex®-M33 core features a floating point unit (FPU) single precision which supports Arm® single-precision data-processing instructions, and data types. The Cortex®-M33 supports a full set of DSP instructions, TrustZone®, and a memory protection unit (MPU) which enhances application security.

STM32MP23xC/F devices can also embed a 3D graphic processing unit (VeriSilicon®, OpenGL ES 3.1, Vulkan 1.3, OpenCL 3.0, OpenVX 1.3) running at up to 400 MHz, with performances up to 66.5 Mtriangle/s, 400 Mpixel/s.

The graphic processing unit can provide a neural processor unit (VeriSilicon®, TensorFlowLite, ONNX, Linux NN) running at up to 400 MHz.

STM32MP23xC/F devices provide an external SDRAM interface supporting external memories up to 32-Gbit density (4 Gbytes), 16-bit DDR3L up to 1066 MHz, 16-bit LPDDR4 or DDR4 up to 1200 MHz. The SDRAM content can be encrypted with AES-128.

The devices incorporate high-speed embedded memories: 776 Kbytes of internal SRAM (including 256-Kbyte AXI SYSRAM, 128-Kbyte AXI video SRAM (which can be used as general purpose), two banks of 128 Kbytes each of AHB SRAM, 128 Kbytes of AHB SRAM in backup domain, and 8 Kbytes of SRAM in backup domain), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, a 32-bit multi-AHB bus matrix, and a 128/64-bit multi-layer AXI interconnect supporting access to internal and external memories.

Each device offers three ADCs, a low-power secure RTC, 12 general-purpose 16-bit timers, 4 general-purpose 32-bit timers, two PWM timers for motor control, five low-power timers, and a true random number generator (RNG), and cryptographic acceleration cells.

STM32MP23xC/F devices offer a video decoder.

The devices support 4 multi-function digital filters.

The devices feature the following standard and advanced communication interfaces.

Standard peripherals

- four I2Cs
- three I3Cs
- four USARTs and three UARTs
- one low-power UART
- six SPIs, three I2Ss full-duplex master/slave. The I2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock.
- four SAI serial audio interfaces
- one SPDIF Rx interface
- three SDMMC interfaces
- an USB 2.0 Host with embedded Hi-Speed PHY
- an USB 2.0 dual-role data with Hi-Speed PHYs
- two FDCAN interfaces, including one supporting TTCAN mode (optional)
- two Gigabit Ethernet Interface, with TSN support (optional)

Advanced peripherals including

- a flexible memory control (FMC) interface
- two Octo-SPI flash memory interface, with on-the-fly content decryption
- two camera interfaces for CMOS sensors, one with basic ISP, demosaicing and parallel or MIPI CSI interface
- an LCD-TFT display interface
- a MIPI DSI display interface (optional)
- an LVDS display interface (optional)

A comprehensive set of power-saving mode allows the design of low-power applications.

STM32MP23xC/F devices are proposed in various packages up to 424 balls with 0.5 mm to 0.8 mm pitch. The set of included peripherals can change with the selected device.

These features make STM32MP23xC/F devices suitable for a wide range of consumer, industrial, white goods and medical applications.

Figure 1 shows the general block diagram of STM32MP23xC/F devices.

Table 1. STM32MP23xC/F features and peripheral counts

Features			STM32MP23xC/F
Package			TFBGA361 (16×16 pitch 0.8 mm), VFBGA361 (10×10 pitch 0.5 mm), VFBGA424 (14×14 pitch 0.5 mm)(1)
CPU processor			Up to dual-core Cortex-A35 FPU Neon TrustZone, up to 1500 MHz(1)
ROM			128 Kbytes (only for Cortex-A35)
GPU			Optional VeriSilicon GC8000UL up to 400 MHz(1)
NPU			
MCU processor		-	Cortex-M33 FPU TrustZone
		Caches size	16-Kbyte data cache
			16-Kbyte instruction cache
		Frequency	400 MHz
Video		Decoder (VDEC)	H264/VP8 up to 1080p60 JPEG 500 Mpixel/s(1)
		Video RAM	Up to 128 Kbytes(1)
Embedded SRAM (776 Kbytes)		CPU system	Up to 384 Kbytes(1)
		MCU system	256 Kbytes (128 Kbytes tamper protected)
		MCU retention	128 Kbytes
		Backup	8 Kbytes (tamper protected)
SDRAM	DDR3L	1066 MHz	Up to 4 Gbytes(1)
	DDR4	1200 MHz	
	LPDDR4	1200 MHz	
Backup registers			512 bytes (128 × 32-bits, tamper protected)
Timers	Advanced	16 bits	2
	General purpose	16 bits	8
		32 bits	4
	Basic	16 bits	2
	Low power	16 bits	5
	SysTick	24 bits	2 (Cortex-M33, secure and non-secure)
	Cortex-A35 (CNT)	64 bits	Up to 2 × 4 (secure, non-secure, Virtual, Hypervisor)(1)
	RTC		1
	Watchdog		5 (4× independent, 1× window)
Communication Peripherals	SPI	Total	6
		having I2S	3

Features			STM32MP23xC/F
Communication Peripherals	I2C (with SMB/PMB support)		4
	I3C		3
	USART (Smartcard, SPI, IrDA, LIN) + UART (IrDA, LIN)[2]		4 + 3
	LPUART		1
	SAI		4 (up to 8 audio channels), with I2S master/ slave, PCM input, SPDIF-TX
	USB	USB 2.0 Host (USBH)	1 port, embedded Hi-Speed PHY
		USB 2.0 Dual Role (USB3DR)[2]	Yes, embedded Hi-Speed
		Embedded PHYs	2× Hi-Speed
		Type-C support (UCPD)	Yes, includes two CC-lines embedded PHY
	SPDIFRX		4 inputs
	FDCAN		Up to 2[1]
SDMMC (SD, SDIO, e•MMC)[2]			3 (8 + 8 + 4 bits).
OCTOSPI[2]			2, with AES-128 (CTR) decryption (OTFDEC)
FMC	Parallel AD-Mux 8/16 bits		4× CS, up to 4x 64 Mbytes[1]
	NAND 8/16 bits[2]		Yes, 4 x CS, SLC, BCH4/8[1]
Gigabit Ethernet interfaces			Up to 2[1]
LCD-TFT (LTDC)		-	Up to 314 MHz pixel clock (when used with DSI or LVDS)
		Parallel interface	Up to 24-bits 150 MHz pixel clock (up to 1080p60)
Display serial interface (DSI)			4× data lanes 2.5 Gbit/s each (up to 1536p60)[1]
LVDS display interface (LVDS)			4× data lanes 1.1 Gbit/s each (up to 1080p60)[1]
Camera interface	-		CSI-2 + RGB/RawBayer parallel
	CSI-2 serial (CSI + DCMIPP)		2× data lanes 2.5 Gbit/s each, path shared with DCMIPP
	Parallel RGB/RawBayer (DCMIPP)		Up to 120 MHz, path shared with CSI.
	Image signal processing (ISP)		Yes, embedded inside DCMIPP
	Parallel RGB (DCMI)		Up to 80 MHz
Parallel interface (PSSI)			16-bit input or output, path shared with DCMI and DCMIPP
HPDMA			3 instances, 48 physical channels in total
Cryptography	CRYP (two instances)		DES/TDES (ECB, CBC), AES-256 (ECB, CBC, CTR, GCM, GMAC, CCM)
	Secure AES (SAES)		AES-256 (ECB, CBC, CTR, GCM, GMAC, CCM), hardware attack protections, keys sharing to CRYP
	Public key accelerator (PKA)		Public key primitives for RSA, DH, and ECC over GF(p). 64-bit core
Hash (HASH)			SHA-1, SHA-2 and SHA-3 (up to 512), MD5, HMAC
Random number generator (RNG)			True-RNG. FIPS 140-2 NDRNG (NIST SP800-90B certifiable)

Features		STM32MP23xC/F
Fuses (one-time programming)		12288 effective bits
Multi-function digital filter (MDF)		4 input channels with 4 filters
GPIOs	with interrupt (total count)	Up to 144[1]
	Wake-up pins	Up to 6[1]
	Tamper input/active output pins	Up to 7 inputs and 5 outputs[1]
Up to 12 bit ADC		3 (up to 5 Msps each)
-	ADC channels in total (differential)	Up to 23 channels (or 11 differential)[1]
	VREF generation (VREFBUF)	1.21 V, 1.5 V, or VREF+ input
	VREF+ input pin	Yes

1. *See next tables for details.*
2. *Can be a boot source.*

Table 2. STM32MP23xC/F differences per product lines

Feature			STM32MP231x	STM32MP233x	STM32MP235x
CPU	Cortex-A35 FPU Neon TrustZone		Single-core	Dual-core	
	Cache size	L1 data + instruction	32 + 32 Kbytes	2 x (32 + 32) Kbytes	
		L2 unified	512 Kbytes	512 Kbytes	
	Frequency	STM32MP23xC	Up to 1200 MHz		
		STM32MP23xF	Up to 1500 MHz		
GPU	For 3D graphics		No		VeriSilicon GC8000UL - Open GL ES 3.2.8 - Vulkan 1.2
	Performance[1] / frequency		-		400 MHz, up to 66.5 Mtriangle/s or 400 Mpixel/s
NPU	For AI processing		No		VeriSilicon GC8000UL - TensorFlowLite - ONNX - Linux NN
	Performance[1] / frequency		-		400 MHz, 0.6 TOPS
Video		Decoder (VDEC)	No		H264/VP8 up to 1080p60 - JPEG 500 Mpixel/s
		Frequency	-		600 MHz
Embedded SRAM		Video RAM	No		128 Kbytes[2]
		CPU system	256 + 128 Kbytes		256 Kbytes[2]
Timers	A35 (CNT)	64 bits	4 (S, NS, V, H)	2x 4 (secure, non-secure, Virtual, Hypervisor)	
FDCAN			No	2 (1x TT-FDCAN), 10-Kbyte shared buffer	
Gigabit Ethernet interfaces	External interfaces		1, R(G)MII, MII	2, R(G)MII, MII	
	GMAC (ETH), TSN, PTP, EEE		1	2	
Display serial interface (DSI)			No		4× data lanes 2.5 Gbit/s each (up to 1536p60)
LVDS display interface (LVDS)			No		4x data lanes 1.1 Gbit/s each (up to 1080p60)

1. *GPU and NPU share performance.*
2. *If VDEC is not used, the video RAM can be used as general purpose memory, thus giving a total of 384 Kbytes for CPU system.*

Table 3. STM32MP23xC/F differences per packages

Features			STM32MP23xxAJ	STM32MP23xxAL	STM32MP23xxAK
			TFBGA361	VFBGA361	VFBGA424
Packages		Body size (mm)	16×16	10×10	14×14
		Pitch (mm)	0.8	0.5	0.5
		Thickness (mm)	1.2	1	1
		Ball count	361	361	424
SDRAM	-		Up to 2 x 4.8 Gbytes/s internal buses . AES-128 encryption/decryption		
	DDR3L	16 bits 1066 MHz	Up to 1 Gbyte, single rank		
	DDR4	16 bits 1200 MHz	Up to 4 Gbytes, single rank		
	LPDDR4	16 bits 1200 MHz	Up to 2 Gbytes, single rank		
FMC	Parallel AD-mux 8/16-bits		4× CS, up to 4× 64 MBytes		
	NAND 8/16-bits [1]		Yes, 4× CS, SLC, BCH4/8		
GPIO	with interrupt (total count)		144	144	144
	Wake-up pins		6	6	6
	Tamper input/active output pins		7 + 5	7 + 5	7 + 5
ADC	ADC channels in total (differential)		23 (11)[2]	23 (11)[2]	21 (10)

1. *Can be a boot source.*
2. *Including 2 (or 1 differential) low-noise inputs on dedicated ANA0/ANA1 pins.*

Figure 1. STM32MP23xC/F block diagram

3 Functional overview

3.1 Dual-core Arm Cortex-A35 subsystem (CA35SS)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

3.1.1 Features

- Armv8-A architecture
- AArch32 for full backward compatibility with Armv7
- AArch64 for 64-bit support and new architectural features
- 32-Kbyte L1 instruction cache for each CPU
- 32-Kbyte L1 data cache for each CPU
- 512-Kbyte level2 cache
- Arm A64 + A32 + Thumb-2 instruction set
- Arm TrustZone security technology
- Arm NEON advanced SIMD
- DSP and SIMD extensions
- VFPv4 floating-point
- Hardware virtualization support
- Performance monitoring Uuit (PMU)
- Program trace macrocell (PTM) that supports instruction trace only
- Integrated generic interrupt controller (GIC) with 384 shared peripheral interrupts
- Integrated generic timer (CNT)

Note: The cryptographic extension is not supported.

3.1.2 Overview

The Cortex-A35 processor uses a highly-efficient 8-stage in-order pipeline that has been extensively optimized to provide full Armv8-A features while maximizing area and power efficiency.

3.1.2.1 Thumb-2 technology

Delivers the peak performance of traditional Arm code, while also providing up to a 30 % reduction in memory requirement for instructions storage.

3.1.2.2 TrustZone technology

Ensures reliable implementation of security applications ranging from digital rights management to electronic payment. Broad support from technology and industry partners.

3.1.2.3 PMU

The PMU provides six performance monitors that can be configured to gather statistics on the operation of each core and the memory system. The information can be used for debug and code profiling.

3.1.2.4 NEON and FPU

Advanced SIMD is a media and signal processing architecture that adds instructions primarily for audio, video, 3-D graphics, image, and speech processing. The floating-point architecture provides support for single-precision and double-precision floating-point operations.

All scalar floating-point instructions are available in the A64 instruction set. All VFP instructions are available in A32 and T32 instruction sets. The same advanced SIMD instructions are available in both A32 and T32 instruction sets. The A64 instruction set offers additional advanced SIMD instructions, including double-precision floating-point vector operations.

3.1.2.5 *Hardware virtualization*

Highly efficient hardware support for data management and arbitration, whereby multiple software environments and their applications are able to simultaneously access the system capabilities. This enables the realization of devices that are robust, with virtual environments that are well isolated from each other.

3.1.2.6 *Optimized L1 caches*

Performance and power optimized L1 caches combine minimal access latency techniques to maximize performance and minimize power consumption. There is also the option of cache coherence for enhanced inter-processor communication, or support of a rich SMP capable OS for simplified multicore software development.

3.1.2.7 *Integrated L2 cache controller*

Provides low-latency and high-bandwidth access to cached memory in high-frequency, or to reduce the power consumption associated with off-chip memory access.

3.1.2.8 *Snoop control unit (SCU)*

The SCU is responsible for managing the interconnect, arbitration, communication, cachetocache and system memory transfers, cache coherence and other capabilities for the processor.

This system coherence also reduces software complexity involved in maintaining software coherence within each OS driver.

3.1.2.9 *Generic interrupt controller (GIC)*

Implementing the standardized and architected interrupt controller, the GIC provides a rich and flexible approach to inter-processor communication, and the routing and prioritization of system interrupts.

Supporting up to 416 independent interrupts (including 384 shared interrupt), under software control, each interrupt can be distributed across Cortex-A35 cores, hardware prioritized, and routed between the operating system and TrustZone software management layer.

This routing flexibility and the support for virtualization of interrupts into the operating system, provide one of the key features required to enhance the capabilities of a solution utilizing an hypervisor.

3.2 Arm Cortex-M33 core with TrustZone and FPU (CM33)

The Arm Cortex-M33 core with TrustZone and FPU is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

It is comprised of:

- Arm TrustZone technology, using the Armv8-M main extension supporting secure and non-secure states
- Floating-point extension (FPU)
- Armv8-M DSP extension
- A nested vectored interrupt controller (NVIC) is closely integrated with the processor
- A memory system with memory protection unit (MPU) with up to 16 non-secure regions and 16 secure regions
- A security attribution unit (SAU) with up to eight regions
- An implementation defined attribution unit (IDAU)
- Debug components including breakpoints (BPU), data watchpoints (DWT), instrumentation, and processor trace (ITM/ETM), cross-trigger interface (CTI)
- 16-Kbyte instruction and 16-Kbyte data caches (ICACHE/DCACHE)

3.3 Graphic processing unit (GPU)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

STM32MP23xC/F devices include a 3D graphics engine (VeriSilicon GC8000UL).

The GPU is a dedicated graphics processing unit accelerating numerous 3D graphics applications such as graphical user interface (GUI), menu display or animations. It works together with an optimized software stack design for industry-standard APIs with support for Android™ and Linux® embedded development platforms.

The GPU is used to accelerate parallel computing (GPGPU), via the typical OpenCL or Vulkan API, or more image-based API like OpenVX or OpenCV. This wide support guarantees to be able to accelerate any application up to the most recent ones, with graphic performances reaching 12.8 GFlops.

The GPU is built in a separate power domain, which allows the GPU to be switched off when not used in the long-term, or even to play with dynamic voltage frequency scaling (DVFS).

The GPU graphic hardware acceleration is exposed through the following API:

- OpenVG 1.2 for 2D or curve drawing
- OpenGL/ES 3.1 for 3D apps (backward compatible: OES2.1 and OES1.1)
- Vulkan 1.3 for modern 3D apps
- OpenCL 3.0 for parallel programming
- OpenVX 1.3 for acceleration of computer vision applications

The GPU provides the following graphic theoretical performance (values for 400 MHz):

- Vertex: 100 MVtx/s
- Triangle: 66.5 MTrg/s
- Texel: 400 MTex/s
- Pixel: 400 MPix/s
- Float 16bit: 12.8 GFlops
- Float 32bit: 6.4 GFlops

3.4 Neural processor unit (NPU)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The NPU provides powerful hardware acceleration for neural network, to allow efficient artificial intelligence (AI) applications.

The NPU acceleration is implemented by hardware neural operator inserted into the GPU. As such, it benefits of both optimized hardware (the neural operator), and of the flexibility and efficiency of the existing GPU shaders.

The NPU neural hardware acceleration is exposed through the following API:

- TensorFlowLite-API
- ONNX
- Linux NN-API-Adapter

The NPU flexibility is used to optimally accelerate the following frameworks (nonexhaustive list)

- TensorFlow non-exhaustive hardware support
- TensorFlowLite full hardware support (including its SoftMax subset)
- Caffe, Caffe2
- CNTK, Torch, Theano, Darknet

The NPU provides the following neural theoretical performance, below values for 400 MHz:

- Integer operations: 0.6 TOPS (8-bit integer)

To reduce the required DDR bandwidth during neural computations, the NPU embeds natively 128 Kbytes of memory.

3.5 Memories

3.5.1 External SDRAM

STM32MP23xC/F devices embed a controller for the external SDRAM which supports the following devices

- DDR3L, 16-bit data, up to 1 Gbytes, up to DDR3L-2133 (1066 MHz clock)
- DDR4, 16-bit data, up to 4 Gbytes, up to DDR4-2400 (1200 MHz clock)
- LPDDR4, 16-bit data, up to 2 Gbytes, up to LPDDR4-2400 (1200 MHz clock)

3.5.2 Embedded SRAM

All devices feature:

- SYSRAM in MPU domain: 256 Kbytes with half/full hardware erase mechanism on reset

- VDERAM in MPU domain: 128 Kbytes (not usable when VDEC is used) with hardware erase mechanism on enable as general purpose RAM
- SRAM1 in MCU domain: 128 Kbytes with hardware erase mechanism on tamper detection
- SRAM2 in MCU domain: 128 Kbytes
- RETRAM (retention RAM): 128 Kbytes with hardware erase mechanism on reset
  The content of this area can be retained in Standby or V_{BAT} mode, and can be protected by ECC and CRC mechanisms.
- BKPSRAM (backup SRAM): 8 Kbytes with hardware erase mechanism on tamper detection
  The content of this area can be protected against possible unwanted accesses, and can be retained in Standby or V_{BAT} mode. The content can also be protected by ECC mechanism.

3.6 DDR3L/DDR4/LPDDR4 controller (DDRCTRL)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

DDRCTRL combined with DDRPHYC provides a complete 16-bit memory interface solution for DDR memory subsystem.

- JEDEC compliant LPDDR4 SDRAM up to 2400 MT/s
- JEDEC compliant DDR4 SDRAM up to 2400 MT/s with DLL on-range
- JEDEC compliant DDR3L SDRAM up to 2133 MT/s with DLL on-range
- 2 x 128-bit AXI4 ports
  - up to 16 QoS levels and up to 3 traffic classes are supported per direction.
  - CID-based firewalling function with poisoning output signaling
  - 1 port provided with AES- 128 encryption/decryption with programmable memory range (DDRMCE)

Low-power features:

- Linked with the RCC, ability to move the DDR memory subsystem in self refresh through automatic way, hardware way, or software way (ASR, HSR and SSR).

3.7 Boot modes

At startup, the boot source used by the internal boot ROM is selected by BOOT pins and OTP settings.

Table 4. Default interfaces

Unless otherwise mentioned in table below.

Boot source	When used by Cortex-A35	When used by Cortex-M33
SD-Card	SDMMC1	
e•MMC	SDMMC2	
Serial NOR, HyperFlash and serial NAND	OCTOSPIM port1	OCTOSPIM port2
SLC NAND	FMC	
USB	USB3DR (high-speed only)	-
UART	USART2/6 and UART5	-

Table 5. Boot sources

BOOT[3:0] pins	Alternate boot pins OTP value							
	0b00 (default)				0b01	0b10	0b11	
	Cortex-A35 master	Cortex-M33 master	Cortex-M33 master (1)		Cortex-A35 master	Cortex-M33 master	Cortex-M33 master (1)	
			Cortex-A35	Cortex-M33			Cortex-A35	Cortex-M33
0	UART and USB(2) (3)							
1	SD-Card	-	-	-	SD-Card	SD-Card	Serial NAND	Serial NOR
2	e•MMC	-	-	-	e•MMC	e•MMC	e•MMC	Serial NOR

BOOT[3:0] pins	Alternate boot pins OTP value							
	0b00 (default)				0b01	0b10	0b11	
	Cortex-A35 master	Cortex-M33 master	Cortex-M33 master (1)		Cortex-A35 master	Cortex-M33 master	Cortex-M33 master (1)	
			Cortex-A35	Cortex-M33			Cortex-A35	Cortex-M33
3	Development boot(2)							
4	Serial NOR	-	-	-	Serial NOR	Serial NOR	SLC NAND	Serial NOR
5	Serial NAND	-	-	-	-	-	e•MMC(4)	Serial NOR
6	SLC NAND	-	-	-	-	-	e•MMC(4)	HyperFlash™
7	-	SD-Card	-	-	HyperFlash™	HyperFlash™	Serial NAND	HyperFlash™
8	-	e•MMC	-	-	Serial NAND	Serial NAND	e•MMC	HyperFlash™
9	-	-	Serial NAND	Serial NOR	-	-	SD-Card(5)	Serial NOR
10	-	-	SLC NAND	Serial NOR	-	-	SD-Card(5)	HyperFlash™
11	-	Serial NOR	-	-	SLC NAND	SLC NAND	SLC NAND(6)	HyperFlash™
12	Development boot(2)							
13	-	-	e•MMC	Serial NOR	SD-Card(5)	SD-Card(5)	SD-Card	Serial NOR
14	-	-	SD-Card	Serial NOR	e•MMC(4)	e•MMC(4)	SD-Card	HyperFlash™
15	UART and USB(3)							

1. *Two flash memory config. Indirect Cortex-A35 boot (from Cortex-M33) or used during Cortex-A35 D1Standby exit*
2. *Cannot be override by OTP.*
3. *Wait incoming connection on USART2/6 or UART5/8/9 on default pins and USB high-speed device on USB3DR_DP/DM.*
4. *e•MMC on SDMMC1*
5. *SD-Card on SDMMC2*
6. *Only 8-bit memory is supported as some FMC and OCTOSPIM port2 pins are shared (usage of FMC in 16-bit mode is exclusive of usage of OCTOSPIM port2).*

The default pins used during boot are described in Table 6.

Note: There is few mutual exclusions with this default settings. SDMMC2 cannot be used with FMC. OCTOSPI Port2 cannot be used with FMC 16 bits. OCTOSPI port2 in 8-bit mode cannot be used with FMC.

Table 6. Minimum set of default pins used during boot ROM phase

Most can be changed using OTP settings. This table is for default OTP settings.

Interface	type		Signal	Pin	IO supply domain
FMC	SLC NAND 8-bits	SLC NAND 16-bits	FMC_NOE	PE15	V_{DDIO2}(1)
			FMC_RNB	PE13	
			FMC_NWE	PE14	
			FMC_NCE1	PE12	
			FMC_ALE	PE8	
			FMC_CLE	PE11	
			FMC_D0	PE9	
			FMC_D1	PE6	
			FMC_D2	PE7	
			FMC_D3	PD15	V_{DD}
			FMC_D4	PD14	

Interface	type			Signal	Pin	IO supply domain
FMC	SLC NAND 8-bits		SLC NAND 16-bits	FMC_D5	PB13	V_{DD}
				FMC_D6	PD12	
				FMC_D7	PB14	
	-			FMC_D8	PB5	V_{DDIO4} (2)
				FMC_D9	PB6	
				FMC_D10	PB7	
				FMC_D11	PD13	V_{DD}
				FMC_D12	PB8	V_{DDIO4} (2)
				FMC_D13	PB9	
				FMC_D14	PB11	
				FMC_D15	PB10	
OCTOSPIM Port1	Serial NOR,	Serial NAND	HyperFlash™	OCTOSPIM_P1_CLK	PD0	V_{DDIO3}
				OCTOSPIM_P1_NCS1	PD3	
				OCTOSPIM_P1_IO0	PD4	
				OCTOSPIM_P1_IO1	PD5	
	-			OCTOSPIM_P1_IO2	PD6	
				OCTOSPIM_P1_IO3	PD7	
				OCTOSPIM_P1_IO4	PD8	
				OCTOSPIM_P1_IO5	PD9	
				OCTOSPIM_P1_IO6	PD10	
				OCTOSPIM_P1_IO7	PD11	
				OCTOSPIM_P1_NCLK	PD1	
				OCTOSPIM_P1_DQS	PD2	
OCTOSPIM Port2	Serial NOR,	Serial NAND	HyperFlash™	OCTOSPIM_P2_CLK	PB10	V_{DDIO4} (2)
				OCTOSPIM_P2_NCS1	PB8	
				OCTOSPIM_P2_IO0	PB0	
				OCTOSPIM_P2_IO1	PB1	
	-			OCTOSPIM_P2_IO2	PB2	
				OCTOSPIM_P2_IO3	PB3	
				OCTOSPIM_P2_IO4	PB4	
				OCTOSPIM_P2_IO5	PB5	
				OCTOSPIM_P2_IO6	PB6	
				OCTOSPIM_P2_IO7	PB7	
				OCTOSPIM_P2_NCLK	PB11	
				OCTOSPIM_P2_DQS	PB9	
SDMMC1	SD-Card or eMMC			SDMMC1_CK	PE3	V_{DDIO1}
				SDMMC1_CMD	PE2	
				SDMMC1_D0 (3)	PE4	
SDMMC2	SD-Card or eMMC			SDMMC2_CK	PE14	V_{DDIO2} (1)
				SDMMC2_CMD	PE15	

Interface	type	Signal	Pin	IO supply domain
SDMMC2	SD-Card or eMMC	SDMMC2_D0[3]	PE13	V_{DDIO2}[1]
USART2		USART2_RX	PA8	V_{DD}
		USART2_TX	PA4	
UART5		UART5_RX	PB15	V_{DD}
		UART5_TX	PA0	
USART6		USART6_RX	PF4	V_{DD}
		USART6_TX	PF5	

1. *Some FMC and SDMMC2 pins are shared, this means that usage of FMC is exclusive of usage of SDMMC2.*
2. *Some FMC and OCTOSPIM port2 pins are shared, this means that usage of FMC in 16-bit mode is exclusive of usage of OCTOSPIM Port2.*
3. *Only used as input by boot ROM*

Although low-level boot is done using internal clocks, ST supplies software packages as well as major external interfaces (such as DDR or USB) require a crystal or an external oscillator to be connected on HSE pins.

See the product reference manual for constrains and recommendations regarding connection of HSE pins and supported frequencies.

3.8 Power supply management (PWR)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

3.8.1 Power supply scheme

The system requires supply on V_{DD}, $V_{DDA18AON}$, V_{DDCPU} and V_{DDCORE} to start, and to allow independent supplies for V_{DDGPU}, $V_{DDA18ADC}$, V_{BAT}, $V_{DD33USB}$, $V_{DD33UCPD}$, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, V_{DDIO1}, and V_{DDQDDR}.

- V_{DD} power supply input for I/Os (1.8 V or 3.3 V typical)
- $V_{DDA18AON}$ power supply input for system analog such as reset, power management, oscillators and OTP
- V_{BAT} optional power supply input for backup domain, and optionally D3 domain when V_{DD} is not present (V_{BAT} mode)
- V_{DDCORE} digital core domain supply, dependent on V_{DD} supply. V_{DD} must be present before V_{DDCORE}.
  - V_{DDCSI}, V_{DDDSI}, and V_{DDLVDS} are usually connected to V_{DDCORE}.
- V_{DDCPU} digital CPU domain supply (Cortex-A35), dependent on V_{DD} supply. V_{DD} must be present before V_{DDCPU}.
- V_{DDGPU} digital GPU domain supply, dependent on V_{DD} supply. V_{DD} must be present before V_{DDGPU}.
- V_{DDQDDR} DDR I/O supply
- $V_{DDA18ADC}$ analog power supply input for ADCs and voltage reference buffers, independent from any other supply
- V_{REF+} external reference voltage for ADCs, independent from any other supply
  - reference voltage output when the voltage reference buffer is enabled
  - independent external reference voltage input when the voltage reference buffer is disabled
- V_{SSA} separate analog and reference voltage ground
- $V_{DD33USB}$ supply input for USB HS PHY, independent from any other supply
- $V_{DD33UCPD}$ supply input for USB Type-C CC1 and CC2 pins, independent from any other supply
- V_{DDIO3} supply input, mostly for OCTOSPIM_P1 I/Os, independent from any other supply
- V_{DDIO4} supply input, mostly for OCTOSPIM_P2 I/Os, independent from any other supply
- V_{DDIO2} supply input, mostly for e.MMC I/Os, independent from any other supply
- V_{DDIO1} supply input, mostly for SD Card I/Os, independent from any other supply
- V_{SS} common ground for all supplies except for analog

3.8.2 Power-supply supervisor

The devices have an integrated power-on reset (POR) and power-down reset (PDR) circuitry, coupled with a brownout reset (BOR) circuitry:

- Power-on reset (POR)
  The POR supervisor monitors V_{DD} and $V_{DDA18AON}$ power supplies, and compares them to a fixed threshold. The devices remain in reset mode when V_{DD} and $V_{DDA18AON}$ are below this threshold.
- Power-down reset (PDR)
  The PDR supervisor monitors V_{DD} and $V_{DDA18AON}$ power supplies. A reset is generated when V_{DD} or $V_{DDA18AON}$ drops below a fixed threshold.
- Brownout reset (BOR)
  The BOR supervisor monitors V_{DD} power supply. A 2.7 V BOR thresholds can be enabled through option bytes. A reset is generated when V_{DD} drops below this threshold. The BOR must not be enabled when V_{DD} = 1.8 V typ. is used.
- Power-on reset V_{DDCORE} (POR_VDDCORE)
  The POR_VDDCORE supervisor monitors V_{DDCORE} power supply, and compares it to a fixed threshold. The V_{DDCORE} domain remains in reset mode when V_{DDCORE} is below this threshold,
- Power-down reset V_{DDCORE} (PDR_VDDCORE)
  The PDR_VDDCORE supervisor monitors V_{DDCORE} power supply. A V_{DDCORE} domain reset is generated when V_{DDCORE} drops below a fixed threshold.
- Power-on reset V_{DDCPU} (POR_VDDCPU)
  The POR_VDDCPU supervisor monitors V_{DDCPU} power supply, and compares it to a fixed threshold. The V_{DDCPU} domain remains in reset mode when V_{DDCPU} is below this threshold.
- Power-down reset V_{DDCPU} (PDR_VDDCPU)
  The PDR_VDDCPU supervisor monitors V_{DDCPU} power supply. A V_{DDCPU} domain reset is generated when V_{DDCPU} drops below a fixed threshold.
- Power-on reset V_{SW} (POR_VSW)
  The POR_VSW supervisor monitors V_{SW} power supply, and compares it to a fixed threshold. The V_{SW} domain remains in reset mode when V_{SW} is below this threshold.

The devices also include monitoring which can generate tamper events, interrupt, or wake-up:

- Programmable voltage detector (PVD)
  The PVD monitors the PVD_IN pin, and compares it to a fixed threshold. An interrupt or a wake-up can be generated when PVD_IN is below or above the threshold.
- V_{DDCORE} monitoring
  Monitors V_{DDCORE} power supply and compares it to a fixed threshold. A tamper event, an interrupt, or a wake-up can be generated when V_{DDCORE} is below or above the threshold.
- V_{DDCPU} monitoring
  Monitors V_{DDCPU} power supply, and compares it to a configurable threshold. A tamper event, an interrupt, or a wake-up can be generated when V_{DDCPU} is below or above the threshold.
- V_{DDGPU} monitoring
  Monitors V_{DDGPU} power supply and compares it to a configurable threshold. An interrupt or a wake-up can be generated when V_{DDGPU} is below or above the threshold. A GPU reset is also generated if V_{DDGPU} is below the threshold (VDDGPURDY = 0).
- Peripheral voltage monitoring
  Monitors independently V_{DDIO2}, V_{DDIO3}, V_{DDIO4}, V_{DDIO1}, $V_{DD33UCPD}$, $V_{DD33USB}$ and $V_{DDA18ADC}$ power supplies with fixed thresholds. An interrupt or a wake-up can be generated when supplies are below or above the thresholds.

3.9 Low-power strategy

Several low-power modes are available to save power when the Cortex-A35 and/or the Cortex-M33 do not need to execute code (when waiting for an external event). It is up to the user to select the mode that gives the best compromise between low-power consumption, short startup time, and available wake-up sources.

- Slowing down system clocks (see RCC section in the reference manual)
- Controlling individual peripheral clocks (see RCC section in the reference manual)

- Low-power modes:
  - CSleep (CPU clock stopped)
  - CStop (CPU subsystem clock stopped)
  - D1 DStop1 (CPU subsystem clock stopped, normal mode signaled to external regulator)
  - D1 DStandby (domain power down and wake up via reset)
  - Stop1, LP-Stop1, and LPLV-Stop1 (system clock stalled, normal, or low-power mode signaled to external regulator supplying the VDDCPU and the VDDCORE)
  - Stop2, LP-Stop2, and LPLV-Stop2 (system clock stalled, powered down mode signaled to external regulator supplying the VDDCPU, and normal or low-power mode signaled to external regulator supplying the VDDCORE)
  - Standby2 (system powered down, D3 domain also in power down)

3.10 Resource isolation framework (RIF)

The RIF is a comprehensive set of hardware blocks designed to enforce and manage the isolation of STM32 hardware resources like memory and peripherals.

Within a defined hardware execution compartment (eight are available), privileged, unprivileged, secure, and non-secure application softwares can assign their own embedded memory buffers, external memory regions, and peripherals thanks to the RIF hardware.

The RIF architectural framework extends to FMC, SYSCFG, IPCC, HSEM, DMA, RTC, TAMP, RCC, PWR, EXTI, or GPIO.

3.11 Reset and clock controller (RCC)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The RCC manages the generation of all clocks, as well as the clock gating and the control of system and peripheral resets. It provides a high flexibility in the choice of clock sources, and allows application of clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the peripheral activity rate.

3.11.1 Features

- RIF aware
- Reset part:
  - Generation of local and system reset
  - Bidirectional pad reset (NRST) to reset of external devices, or to reset the device
  - Output pad reset (NRSTC1MS) to reset of external mass-storage devices used by the Cortex-A35
- Clock generation part:
  - Generation and distribution of clocks for the complete system
  - 5 separate PLLs (excluding external Cortex-A35, DDRCTRL, and GPU ones):
    - Integer or fractional mode
    - Spread-spectrum function to reduce the amount of EMI peaks
    - Possibility to change on-the-fly the fractional ratios of the PLLs
  - Smart clock gating for reduction of power dissipation
  - 2 external oscillators:
    - HSE that supports a wide range of crystals: 16 to 48 MHz
    - LSE for 32.768 kHz crystals
  - 3 Internal oscillators:
    - HSI that runs around 64 MHz
    - MSI that runs around 16 MHz or 4 MHz
    - LSI that runs around 32 kHz
  - Buffered clock outputs for external devices
- Two independent interrupt interfaces (one dedicated to Cortex-A35, and one dedicated to Cortex-M33)
- Two independent failure events (HSE and LSE)
- Two independent events to wake up processors (one dedicated to Cortex-A35 and one dedicated to Cortex-M33)

3.11.2 Clock management

The RCC provides a high flexibility to the application in the choice of the clock generators:

- from HSI, high-speed internal oscillator (~ 64 MHz)
- from HSE, high-speed external oscillator (16 to 48 MHz)
- from LSE; low-speed external oscillator (32 kHz)
- from LSI, low-speed internal oscillator (~ 32 kHz)
- from MSI, low-power internal oscillator (~ 4 MHz or ~ 16 MHz)

The RCC offers a good flexibility for the application to select the appropriate clock for CPUs and peripherals. More especially for peripherals that need a specific clock like SPI(I2S), SAI, and SDMMC.

Each clock source can be switched on or off independently in order to optimize the power consumption.

There are mainly three clock paths:

- Cortex-A35 bus matrix
- Cortex-M33 and its bus matrix
- peripheral kernel clocks

The Cortex-A35, the GPU, and DDRCTRL clocking are derived locally because of high frequency use. The RCC manages only source clocks for their related local PLLs.

3.11.3 Reset sources

There are several sources able to generate a reset:

- supply monitors (V_{DD}, V_{DDCORE}, V_{DDCPU} , V_{DDGPU} or V_{SW}) lower than expected values
- independent watchdogs timeout
- D1 domain exit from DStandby state
- exit from Standby mode
- external signals driving the NRST pin

- software commands

The coverage (or scope) of the resets differ according to the source initiating the reset, with the following categories:

- power-on/off resets
- system resets
- local resets

An application reset can be generated from one of the following sources:

- reset from the NRST pin
- reset from low-voltage detection on VDD
- reset from the independent watchdogs
- software reset from RCC registers
- failure on HSE
- RETRAM CRC or ECC error

A system reset can be generated from one of the following sources:

- reset from application reset
- reset from low-voltage detection on V_{DDCORE}
- a reset from low-voltage detection on V_{DDCPU}

The NRST reset is activated by:

- low voltage on V_{DD}
- failure on HSE
- reset from the independent watchdogs
- software reset from RCC registers
- RETRAM CRC or ECC error
- assertion of NRST by an external source

3.12 Hardware semaphore (HSEM)

The hardware semaphore provides 16 (32-bit) register-based semaphores.

The semaphores can be used to ensure synchronization between different processes that run on a core and between different cores. The HSEM provides a non-blocking mechanism to lock semaphores in an atomic way. The following functions are provided:

- Locking a semaphore can be done in two ways:
  - 2-step lock: by writing CoreID and ProcessID to the semaphore, followed by a read check.
  - 1-step lock: by reading the CoreID from the semaphore
- Interrupt generation when a semaphore is freed
  - Each semaphore can generate an interrupt on one of the interrupt lines.
- Semaphore clear protection
  - A semaphore is only cleared when CoreID and ProcessID matches.
- Global semaphore clear per CoreID

3.13 Inter-processor communication controller (IPCC1)

The IPCC is used to communicate data between two processors. It provides a non-blocking signaling mechanism to post and retrieve communication data in an atomic way (signaling for 16 channels).

The IPCC communication data must be located in a common memory, which is not part of the IPCC.

3.13.1 Main features

- Status signaling for the four channels
  - Channel occupied/free flag, also used as lock
- Two interrupt lines per processor
  - One for RX channel occupied (communication data posted by sending processor)
  - One for TX channel free (communication data retrieved by receiving processor)

- Interrupt masking per channel
  - Channel occupied mask
  - Channel free mask
- Two channel operation modes
  - Simplex (each channel has its own communication data memory location)
  - Half duplex (a single channel in associated to a bidirectional communication data information memory location)

3.14 General-purpose input/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (with or without pull-up or pull-down), or as peripheral alternate function. Some of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/O registers.

Access to each GPIO configuration bits can be restricted to secure-only and/or privileged-only. These configuration bits can also be allocated to a specific CPU.

3.15 Bus-interconnect matrix

For more details on interconnect, see the reference manual (STM32MP23/25xx reference manual (RM0457)).

Figure 2. AXI STNoC multi-frequency network

Figure 3. MCU multi-Layer AHB 400 MHz

Figure 4. MCU multi-Layer AHB 200 MHz

Figure 5. **SmartRun multi-Layer AHB matrix**

3.16 High-performance DMA controllers (HPDMA1/2/3)

- AXI master and AHB master
- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Sleep and Stop modes
- Per channel event generation
- Per channel interrupt generation
- 16 concurrent DMA channels
- Per channel FIFO
- Linked-list support
- TrustZone support
- Privileged/unprivileged support
- Channel isolation support

3.17 Cortex-M33 nested vectored interrupt controller (NVIC)

The devices embed a NIC that can support up to 320 maskable interrupt channels, not including the Cortex®-M33 interrupt lines.

- 16 programmable priority levels
- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Tail chaining
- Processor context automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

NVIC registers are banked across secure and non-secure states.

The NVIC provides flexible interrupt management features with minimum interrupt latency.

3.18 Extended interrupt and event controller (EXTI1/2)

The EXTI manages individual CPU and system wake-up through configurable and direct event inputs. It provides wake-up requests to the power control, and generates an interrupt request to the CPU NVIC or GIC, and events to the CPU event inputs. For each CPU, an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to be woken up from Stop mode, and CPUs to be woken up from CStop and CStandby modes.

The interrupt request and event request generation can also be used in Run mode.

The EXTI also includes the EXTI I/Oport selection.

Each interrupt or event can be set as secure to restrict access to secure software only.

EXTI1 is shared between Cortex-A35 and Cortex-M33 while EXTI2 is shared between all cores.

3.19 Cyclic redundancy check calculation unit (CRC)

The CRC calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity.

The CRC calculation unit helps computing a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.20 Flexible memory controller (FMC)

The FMC main features are the following:

- Interface with static-memory mapped devices including:
  - NOR flash memory
  - Static or pseudo-static random access memory (SRAM, PSRAM)
  - NAND flash memory with 4-bit/8-bit BCH hardware ECC
- 8-,16-bit data bus width
- Independent chip-select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO

3.21 Octo-SPI memory interface (OCTOSPI1/2)

The OCTOSPI supports two protocols used by most external serial memories such as serial PSRAMs, serial NAND and serial NOR flash memories, HyperRAMs, and HyperFlash memories:

- Indirect mode: all the operations are performed using the OCTOSPI registers.
- Automatic status-polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting.
- Memory-mapped mode: the external memory is memory mapped ,and is seen by the system as if it was an internal memory supporting both read and write operations.

The OCTOSPI supports multiple protocols:

- XSPI protocol and its various flavors (such as XCELLA, OCTABUS, HyperBus™ as defined by memory providers)

3.22 On-the-fly decoder (OTFDEC1/2)

The OTFDEC is used to decrypt on-the-fly AHB traffic based on the read request address information. Four independent and non-overlapping encrypted regions can be defined in the OTFDEC.

The OTFDEC uses AES-128 in counter mode to achieve the lowest possible latency. Each time the content of an encrypted region is changed, the entire region must be re-encrypted with a different cryptographic context (key or initialization vector). This constraint makes the OTFDEC suitable to decrypt read-only data or code, stored in external NOR flash memory.

3.23 Octo-SPI I/O manager (OCTOSPIM)

The OCTOSPIM is an internal multiplexer:

- Efficient OCTOSPI pin assignment by allowing pin swapping
- Multiplexing two single-, dual-, quad, or octal-SPI interfaces over the same external bus: interfaces (with for example different security attributes) share then the same memory, or access two memories embedded in a multichip package.

3.24 Analog-to-digital converters (ADC1/2/3)

STM32MP23xC/F devices embed three analog-to-digital converters, which resolution can be configured to 12, 10, or 8 bits. Each ADC shares up to 20 channels, performing conversions in single-shot or scan mode. In scan mode, an automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- simultaneous ADC1/ADC2 conversion
- interleaved ADC1/ADC2 conversion

The ADC can be served by DMA, thus allows the automatic transfer of ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some, or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

In order to synchronize A/D conversion, the ADCs can be triggered by timers.

3.25 Digital temperature sensor (DTS)

The DTS is a high-precision low-power junction temperature sensor, based on a configurable controller plus one or multiple embedded temperature sensors. The sensor can operate in two distinct modes to provide temperature readings:

- first mode used to a provide calibrated accurate temperature
- second mode that does not require any calibration

Main features:

- Two programmable (rise or fall) hardware alarms incorporating hysteresis
- Status registers recording the minimum and maximum data values received
- A power-up timer with IRQ to support manual operation
- A calibration sequence requiring no knowledge of die temperature.

3.26 V_{BAT} operation

The V_{SW} domain supplies the RTC, the TAMP, the LSI, the LSE, the IWDG5, the backup registers, the retention RAM, and the backup SRAM.

In order to optimize the battery duration, this power domain is supplied by V_{DD} when available, or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} has dropped below the PDR level.

The voltage on VBAT pin can be provided by an external battery, by a supercapacitor, or directly by V_{DD}. In the later case, V_{BAT} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

Note: None of these events (external interrupts, watchdog reset, TAMP event, or RTC alarm/events) can directly restore the V_{DD} supply, and force the device out of the V_{BAT} operation. Nevertheless, watchdog reset (taken as a tamper event), TAMP events, and RTC alarm/events can be used to generate a signal to an external circuitry (typically a PMIC) that can restore the V_{DD} supply.

3.27 Voltage reference buffer (VREFBUF)

STM32MP23xC/F devices embed a voltage reference buffer which can be used as voltage reference for ADC, and as voltage reference for external components through VREF+ pin.

An external voltage reference must be provided through the VREF+ pin when the internal voltage reference buffer is off.

3.28 Multifunction digital filter (MDF1)

The MDF is a high-performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators.

3.28.1 Features

- 4 serial digital inputs:
  - configurable SPI interface to connect various digital sensors
  - configurable Manchester coded interface support
  - compatible with PDM interface to support digital microphones
- 2 common clocks input/output for ΣΔ modulator(s)
- Flexible matrix (BSMX) for connection between filters and digital inputs
- 2 inputs for connecting internal ADCs
- 4 flexible digital filter paths, including
  - A Configurable CIC filter:
    - Can be split into 2 CIC filters: high resolution filter, and out-off limit detector
    - Can be configured in $Sinc^4$ filter
    - Can be configured in $Sinc^5$ filter
    - Adjustable decimation ratio
  - A reshape filter to improve the out-off band rejection and in-band ripple
  - A high pass filter to cancel the DC offset
  - An offset error cancellation
  - Gain control
  - Saturation blocks
  - An out-off limit detector
- Short-circuit detector,
- Clock absence detector
- 16 or 24-bit signed output data resolution,
- Continuous or single conversion,
- Possibility to delay independently each bitstream
- Various trigger possibilities
- Break generation on out-of limit or short-circuit detector events
- Autonomous functionality in Stop modes
- DMA can be used to read the conversion data
- Interrupts services

Targeted applications:

- Audio: speech capture
- Motor control
- Metering

3.29 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8- to 14-bit parallel interface, to receive video data. The camera interface can support a resolution of 1 Mpixels at 15 fps.

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12-, or 14-bit
- 8-bit progressive video monochrome or RawBayer format, YC_bC_r 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.30 Parallel synchronous slave interface (PSSI)

The PSSI and the DCMI use the same circuitry. These two peripherals cannot be used at the same time: when using the PSSI, DCMI registers cannot be accessed, and vice versa.

The PSSI and the DCMI also share the same alternate functions and interrupt vector.

The PSSI is a generic synchronous 8/16-bit parallel data input/output slave interface. It enables the transmitter to send a data valid signal. This signal indicates when the data is valid, and the receiver to output a flow control signal that indicates when it is ready to sample the data.

Main features:

- Slave mode operation
- 8-bit or 16-bit parallel data input or output
- 8-word (32-byte) FIFO
- Data enable (PSSI_DE) alternate function input, and Ready (PSSI_RDY) alternate function output

3.31 Digital camera interface with pixel processing (DCMIPP)

- Parallel input interface:
  - Up to 16 bits at 120 MHz, up to 2 Mpixels sensors at 30 fps
  - Pixel format: RGB565, 888, YUV422, RawBayer/Mono 8/10/12/14
- When connected to CSI-2 input interface:
  - Up to 200 Mpixel/s, up to 5 Mpix sensors at 30 fps, supports MIPI CSI-2 v1.3
  - Pixel format: all MIPI CSI-2 v1.3: RGB565, 888, YUV422, RawBayer
  - Features: interleaved packets, 4 virtual channels
- Flow selection and frame control
- Byte-to-pixel conversion
- Statistic removal
- Bad pixel removal (automatic detection and correction of bad pixels from sensor array)
- Decimation of one pixel every 1/2/4/8
- Integrated image processing used to connect low-cost camera module without any embedded ISP
  - Color conversion to adapt to the sensor and tune the Illumination
  - Contrast enhancement
  - RawBayer to RGB conversion (demosaicing)
  - Exposure control
  - Statistics extraction
- Decimation on pipe 0 (pipe dump)
- Multiple pipelines for parallel applications:
  - Pipe0 (for data dump), for a direct dump without processing
  - Pipe1 (for main use), with downsize, color conversion, YUV-planar
  - Pipe2 (for ancillary use), with downsize, color conversion, YUV-planar
- Downsize
  - Box-filtering, with any decimal ratio, up to 8x8, on pipe1 and pipe2
- Gamma conversion
- RGB to YUV color conversion
- Output pixel format:
  - Pipe0: any data as is, Y/Rb: 8/10/12/14 statistics, bitstreams
  - Pipe2: RGB888, RGB565, YUV422-1, Y8, ARGB and RGBA (co-planar only)
  - Pipe1: Pipe2 formats + YUV422-2, YUV420-2, YUV420-3 (multi-planar possible)
- AXI master

3.32 Camera serial interface (CSI)

The CSI provides an interface between the system and the PHY, allowing communication with a CSI-2 compliant camera.

- Compliant with MIPI Alliance standard v1.3
- Up to two data lanes, up to 2.5 Gbit/s per lane in high-speed (HS) mode and 10 Mbit/s in low-power (LP) mode
- Data transmission in HS and LP modes
- Escape mode (ESC), and ultra-low-power state mode (ULPS)
- CSI-2 virtual channel and data type filtering supporting interleaved data
  - Up to 4 virtual channels
  - Support data formats specified into the MIPI Alliance standard for CSI-2 v1.3 (18 data formats, plus the user defined onces, up to 7 independent data types)
- Internal connection with the DCMIPP

3.33 LCD-TFT display controller (LTDC)

The LTDC handles display composition and rotation, with the following main features:

- 3 display layers with dedicated FIFO
- Input pixel flexible format, including YUV420 full-planar
- Secure layer: protected access to buffer and configuration registers
- Output rotation: 90 and 270 degrees
- Horizontal and vertical mirror
- Color lookup-table, color keying, gamma, and dithering on output

LTDC parallel interface:

- Provides a 24-bit parallel digital RGB, and delivers all signals to interface directly to a broad range of LCD and TFT panels.
- Up to 150 Mpixel/s, which correspond up to FHD (1920 × 1080) at 60 fps resolution with HDMI blankings
- Output pixel formats: RGB888, RGB666, RGB565, YUV422-16 bits

LTDC DSI interface:

- The LTDC provide pixels to the display serial interface (DSI).

LTDC LVDS interface:

- The LTDC provide pixels to the LVDS display interface (LVDS).

3.34 Display serial interface (DSI)

Note: Features may be limited or absent in some devices or packages (see Section 2: Description for details).

The DSI is part of a group of communication protocols defined by the MIPI Alliance. The MIPI DSI host controller is a digital core that implements all protocol functions defined in the MIPI DSI specification.

It provides an interface between the system and the MIPI D-PHY that allows the communication with a DSI-compliant display.

- Compliant with MIPI Alliance standards
- Interface with MIPI D-PHY
- Supports all commands defined in the MIPI Alliance specification for DCS
- Bidirectional communication and escape mode support through data lane 0
- Supports non-continuous clock in D-PHY clock lane for additional power saving
- Supports ultra-low-power mode with PLL disabled
- ECC and checksum capabilities
- Support for end of transmission packet (EoTp)
- Fault recovery schemes

- Configurable selection of system interfaces:
  - AMBA APB for control and optional support for generic and DCS commands
  - Video mode interface through LTDC
  - Adapted command mode interface through LTDC
  - Independently programmable virtual channel ID in video mode, adapted command mode and APB slave
- Video mode interfaces features:
  - LTDC interface color coding mappings into 16, 18 and 24-bit interface
  - Programmable polarity of all LTDC interface signals
- Adapted interface features:
  - Support for sending large amounts of data through the memory_write_start (WMS) and memory_write_continue (WMC) DCS commands
  - LTDC interface color coding mappings into 16, 18 and 24-bit interface
- Video mode pattern generator
- Up to 4 × data lanes, up to 2.5 Gbit/s each
- Up to QXGA (2048 × 1536) at 60 fps

3.35 LVDS display interface (LVDS)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The LVDS supports the following high-level features:

- FPD-Link-I and OpenLDI (v0.95) protocols
- Single-link operation
- Flexible bit-mapping, including JEIDA and VESA
- RGB888 or RGB666 output
- 4 data lanes, up to 1.1 Gbit/s per lane
  - FPD bitrate: 784 Mbit/s per lane (112 Mpixel/s)
  - OpenLDI bitrate: 1100 Mbit/s per lane (157 Mpixel/s)
- Up to WSXGA+ (1680 × 1050) at 60 fps with single FPD link (1080p60 supported with OpenLDI)

3.36 Video decoder (VDEC)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

- Video decode
  - H264 (MPEG4_Part10/AVC, baseline/main/high up to 5.2), VP8
  - Up to 1080p60 for H264/VP8
- Still-image decode
  - JPEG (baseline interleaved).
  - Up to 500 Mpixel/s for JPEG
- VDERAM
  - 128 Kbytes
  - Can be statically assigned to CPU as additional system RAM by SYSCFG setting

3.37 True random number generator (RNG)

All devices embed an RNG that deliver s 32-bit random numbers generated by an integrated analog circuit.

3.38 Hash processor (HASH)

The HASH is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-2 family, SHA-3 family), and the HMAC (keyed-hash message authentication code) algorithm. The HMAC is suitable for applications that require a message authentication.

The HASH computes FIPS (federal information processing Standards) approved digests of 160-, 224-, 256-, 384-, and 512-bit length, for messages of any length:

- less than 2^{64} bits (for SHA-1, SHA-224, and SHA-256)
- less than 2^{128} bits (for SHA-384, SHA-512)

3.39 Cryptographic processor (CRYP1/2)

The devices embed two cryptographic processor that can be used both to encrypt and decrypt data using the DES, triple-DES, or AES algorithms. The implementation if fully compliant with the following standards:

- DES and TDES are defined by FIPS (PUB 46-3, Oct 1999), and by the American National Standards Institute (ANSI X9.52)
- AES is defined by FIPS (FIPS PUB 197, Nov 2001)

Multiple key sizes and chaining modes are supported:

- DES/TDES chaining modes ECB and CBC, supporting standard 56-bit keys with 8-bit parity per key
- AES chaining modes ECB, CBC, CTR, GCM, GMAC, CCM for key sizes of 128, 192, or 256 bits

The CRYP in AES mode supports key sharing from SAES co-processor. It is a 32-bit AHB peripheral with DMA support for incoming and outgoing data.

The CRYP also includes input and output FIFOs (each 8 words deep) for better performance.

3.40 Secure AES (SAES)

The SAES encrypts or decrypts data, using an algorithm and implementation fully compliant with the AES standard. It implements embedded protection against differential power analysis (DPA) and related side-channel attacks.

The SAES supports CTR, GCM, GMAC, CCM, ECB, and CBC chaining modes for key sizes of 128 or 256 bits, as well as special modes such as hardware secret key encryption/decryption (wrapped-key mode) and key sharing with faster CRYP peripheral (shared-key mode).

The SAES can load directly two hardware master keys that are not directly accessible by any software. These keys can be used to encrypt random keys that are usable only on this device, and are not directly accessible by software.

The SAES supports DMA single transfers for incoming and outgoing data (two DMA channels required). It is connected by hardware to the RNG and to the CRYP1/2.

The SAES is an AMBA AHB slave peripheral.

3.41 Public key accelerator (PKA)

The PKA is intended for the computation of cryptographic public key primitives, specifically those related to RSA, Diffie-Hellmann, or ECC (elliptic curve cryptography) over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

For a given operation, all needed computations are performed within the accelerator: no further hardware/software elaboration is needed to process inputs or outputs.

3.42 Boot and security and OTP control (BSEC)

The BSEC is used to control an OTP (one-time programmable) fuse box, used for embedded non-volatile storage for device configuration and security parameters.

Embedded non-volatile secrets are stored in the BSEC upper area that is only accessible while BSEC is operating in a closed state. In open state those non-volatile secrets are permanently hidden.

The BSEC use is reserved to trusted domain CPU, and boot CPU following a BSEC reset (cold/warm or hot).

3.43 Timers and watchdogs

The devices include two advanced-control timers, twelve general-purpose timers, two basic timers, five low-power timers, seven watchdogs, two SysTick timers in Cortex-M33 , and four system timers in each Cortex-A35.

All timer counters can be frozen in debug mode.

The table below compares features of the different timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max[1] timer clock (MHz)
Advanced -control	TIM1, TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	6	4	200	200
General purpose	TIM2, TIM3, TIM4, TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No	200	200
	TIM10, TIM11, TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	200	200
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	200	200
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1	200	200
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1	200	200
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	200	200
Low-power	LPTIM1, LPTIM2	16-bit	Up, Up/down	1, 2, 4, 8, 16, 32, 64, 128	Yes	2[2]	No	200	100
	LPTIM3, LPTIM4	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	Yes	2[2]	No	200[3]	100
	LPTIM5	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	0	No	200[3]	100

1. *The maximum timer clock depends on RCC settings.*
2. *only compare channel.*
3. *16 MHz bus clock when supplied by the backup regulator (LP-Stop1/2, LPLV-Stop1/2).*

3.43.1 Advanced-control timers (TIM1/8)

The advanced-control timers can be seen as three-phase PWM generators multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge- or center-aligned modes)
- one-pulse mode output

If configured as standard 16-bit timers, the advanced-control timers have the same features as the general-purpose timers. If configured as 16-bit PWM generators, they have full modulation capability (0 to 100%).

The advanced-control timers can work together with general-purpose timers via the timer link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

3.43.2 General-purpose timers (TIM2/3/4/5/10/11/12/13/14/15/16/17)

There are twelve synchronizable general-purpose timers embedded in STM32MP23xC/F devices (see Section 3.43 for differences).

- **TIM2, TIM3, TIM4, TIM5**

These timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. They feature four independent channels for input capture/output compare, PWM, or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

These timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8, via the timer link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 have independent DMA request generation. They can handle quadrature (incremental) encoder signals, and the digital outputs from one to four halleffect sensors.

- **TIM10, TIM11, TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM, or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

3.43.3 Basic timers (TIM6/TIM7)

These timers are used as a generic 16-bit time base, and support independent DMA request generation.

3.43.4 Low-power timer (LPTIM1/2/3/4/5)

These low-power timers have an independent clock and run in Stop mode if they are clocked by LSE, LSI, or an external clock. They can wake up the device from Stop mode.

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/one-shot mode
- Selectable software/hardware input trigger
- Selectable clock source:
  - Internal clock source: LSE, LSI, HSI (RCC flexgen output)
  - External clock source over LPTIM input (working even with no internal clock source running, used by the pulse counter application)
- Programmable digital glitch filter
- Encoder mode (LPTIM1/2)

3.43.5 Independent watchdog (IWDG1/2/3/4)

The IWDG is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI). As it operates independently from the main clock, the IWDG can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.43.6 System window watchdog (WWDG1)

The WWDG is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.43.7 SysTick timer

This timer is embedded in the Cortex-M33 (two instances, secure and non-Secure) . It is dedicated to real-time operating systems, but can also be used as standard downcounter.

- 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0

- Programmable clock source

3.43.8 Cortex-A35 generic timers (CNT)

The Cortex-A35 generic timers are fed by value from system timing generation (STGEN). The Cortex-A35 processor provides a set of four timers for each processor:

- Physical timer for use in secure and non-secure modes. The registers for the physical timer are banked to provide secure and non-secure copies.
- Virtual timer for use in non-secure mode
- Physical timer for use in hypervisor mode

These generic timers are not memory-mapped peripherals: they are accessible only by specific Cortex-A35 coprocessor instructions (cp15).

3.44 System timer generation (STGEN)

The STGEN generates a time-count value that provides a consistent view of time for all Cortex-A35 generic timers.

- 64-bit wide to avoid roll-over issues
- Starts from zero or a programmable value
- control APB interface (STGENC) that enables the timer to be saved and restored across power-down events
- Read-only APB interface (STGENR) that enables the timer value to be read by nonsecure software and debug tools
- timer value incrementing that can be stopped during system debug

3.45 Real-time clock (RTC)

The RTC provides an automatic wake-up to manage all low-power modes. It is an independent BCD timer/counter that provides a time-of-day clock/calendar with programmable alarm interrupts.

The RTC includes also a periodic programmable wake-up flag with interrupt capability.

After backup domain reset, all RTC registers are protected against possible parasitic write accesses.

As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low-power mode, or under reset).

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), day (day of week), date (day of month), month, and year
- Daylight saving compensation programmable by software
- Programmable alarm with interrupt function. The alarm can be triggered by any combination of the calendar fields.
- Automatic wake-up unit that generates a periodic flag that triggers an automatic wake-up interrupt
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Accurate synchronization with an external clock using the subsecond shift feature
- Digital calibration circuit (periodic counter correction): 0.95 ppm accuracy, obtained in a calibration window of several seconds
- Timestamp function for event saving
- Maskable interrupts/events:
  - Alarm A
  - Alarm B
  - Wake-up interrupt
  - Timestamp
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wake-up timer and timestamp individual secure or non-secure configuration

3.46 Tamper and backup registers (TAMP)

The 128 x 32-bit backup registers are retained in all low-power modes, and in V_{BAT} mode. They can be used to store sensitive data as their content is protected by a tamper detection circuit. 12 tamper pins (seven input and five outputs), and 14 internal tampers are available for anti-tamper detection.

The seven external tamper pins can be configured for edge detection, edge and level, level detection with filtering, or up to five active tamper which increases the security level by auto-checking that tamper pins are not externally opened or shorted.

- 128 backup registers (TAMP_BKPxR) implemented in the RTC domain that remains powered-on by V_{BAT} when the V_{DD} power is switched off
- 7 external tamper detection events:
  - Each external event can be configured to be active or passive.
  - External passive tampers with configurable filter and internal pull-up
- 14 internal tamper events
- Any tamper detection can generate an RTC timestamp event.
- Any tamper detection erases backup registers.
- TrustZone support:
  - Tamper secure or non-secure configuration
  - Backup registers configuration in three configurable-size areas:
    - 1 read/write secure area
    - 1 write secure/read non-secure area
    - 1 read/write non-secure area
- Monotonic counter

3.47 Inter-integrated circuit interface (I2C1/2/7/8)

STM32MP23xC/F devices embed four I^2C interfaces that handle communications between the device and the serial I^2C bus. Each I^2C interface controls all I^2C bus-specific sequencing, protocol, arbitration, and timing.

The I^2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Controller and target modes, multi-controller capability
  - Standard-mode (Sm), with a bitrate up to 100 Kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 Kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit target addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources that allows the I^2C communication speed to be independent from the PCLK reprogramming
- Wake-up from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

3.48 Improved inter-integrated circuit (I3C1/2/4)

STM32MP23xC/F devices embed three I3C interfaces, that handle communication between the device and others that are all connected on an I^3C bus, like sensors and host processors.

The I3C peripheral implements all required features of the MIPI I3C specification v1.1. It can control all I^3C bus-specific sequencing, protocol, arbitration and timing, and can be acting as controller, or as target.

The I3C peripheral, acting as controller, improves the I^2C interface features still preserving some backward compatibility: it allows an I^2C target to operate on an I^3C bus in legacy I^2C fast-mode (Fm) or legacy I^2C fast-mode plus (Fm+), provided that this latter does not perform clock stretching.

The I3C peripheral can be used with DMA in order to off-load the CPU.

- MIPI I3C specification v1.1 (see I3C section in the reference manual), as:
  - I3C primary controller
  - I3C secondary controller
  - I3C target
- Registers configuration from the host application via the APB slave port
- Queued transfers:
  - Transmit FIFO (TX-FIFO) for data bytes/words to be transmitted on I^3C bus
  - Receive FIFO (RX-FIFO) for received data bytes/words on I^3C bus
  - Control FIFO (C-FIFO) for control words to be sent on I^3C bus, when controller
  - Status FIFO (S-FIFO) for status words as received on I^3C bus, when controller
  - For each FIFO, optional DMA mode with a dedicated DMA channel
- Messages:
  - Legacy I2C read/write messages to legacy I2C targets in Fm/Fm+
  - I3C SDR read/write private messages
  - I3C SDR (write) broadcast CCC messages
  - I3C SDR read/write direct CCC messages
- Frame-level management, when controller:
  - Software-triggered or hardware-triggered transfer
  - Optional C-FIFO and TX-FIFO preload
  - Multiple messages encapsulation
  - Optional arbitrable header
- Programmable bus timing, when controller
  - SCL high and low period
  - SDA hold time
  - Bus free (minimum) time (between a stop and a start)
  - Bus available/idle condition time, maximum clock stall time
  - Minimum clock stall time during 9th bit
- Target-initiated requests management:
  - In-band interrupts, with programmable IBI payload (up to 4 bytes)
  - Bus control request, with recovery flow support and hand-off delay
  - Hot-join mechanism
  - Pending read notification
- Bus error management
  - M0, M1, M2, and M3, when controller
  - S0, S1, S2, S3, S4, S5, and S6 when target
  - bus control switch error and recovery
  - target reset
- Separately programmed event/flag generation and management
  - Separated identification and clear control
  - Host application notification via event/flag polling, and/or via interrupt with a perevent programmable enable
  - Error type identification
- Autonomous mode and transfers during Sleep and Stop modes via DMA

- Autonomous wake-up on
  - Target request acknowledge, when controller
  - Missed start detection, when target
  - Reset pattern detection, when target

3.49 Universal synchronous asynchronous receiver transmitter (USART1/2/3/6, UART4/5/7)

STM32MP23xC/F devices embed four USART and three UART (see Table 8. USART/UART features for feature summary).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN master/slave capability. They provide hardware management of CTS and RTS signals, and RS485 driver enable. They can communicate at speeds of up to 10 Mbit/s.

The USARTs embed a 64-byte transmit FIFO (TXFIFO) and a 64-byte receive FIFO (RXFIFO). The FIFO mode is enabled by software, and is disabled by default.

All USARTs provide smartcard mode (ISO 7816 compliant) and SPI-like communication capability. They have a clock domain independent from the CPU clock: this allows the USARTx to wake up the device from Stop mode using baud rates up to 200 Kbaud. Wake-up events from Stop mode are programmable and can be one of the following:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USARTs can be served by the DMA controller.

Table 8. USART/UART features

Modes/features [1]	USART1/2/3/6	UART4/5/7
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous SPI mode (master/slave)	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wake-up from low-power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver enable	X	X
Data length	7, 8, and 9 bits	

1. *X = supported.*

3.50 Low-power universal asynchronous receiver transmitter (LPUART1)

The devices embed one LPUART that supports asynchronous serial communication with minimum power consumption. The LPUART supports half-duplex single-wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART embeds a transmit FIFO (TXFIFO) and a receive FIFO (RXFIFO). The FIFO mode is enabled by software, and is disabled by default.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode. The wake-up from Stop mode is programmable, and can be done on one of the following:

- a start bit detection
- any received data frame
- a specific programmed data frame
- specific TXFIFO/RXFIFO status when FIFO mode is enabled

Even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low-energy consumption.

3.51 Serial peripheral interface (SPI1/2/3/4/5/8) inter-integrated sound interfaces (I2S1/2/3)

The devices feature up to six SPIs that allow communication at up to 50 Mbit/s in master and slave modes, in half-duplex, full-duplex, and simplex modes. The 3-bit prescaler gives eight master mode frequencies, and the frame is configurable from 4 to 16 bits.

All SPI interfaces support NSS pulse mode, TI mode, hardware CRC calculation, and eight 8-bit embedded Rx and Tx FIFOs with DMA capability.

The standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) can be operated in master or slave mode, in full-duplex and half-duplex communication modes. They can be configured to operate with a 16-/32-bit resolution as an input or output channel.

Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I^2S interfaces support 16x 8bit embedded Rx and Tx FIFOs with DMA capability.

3.52 Serial audio interfaces (SAI1/2/3/4)

The devices embed four SAIs that are used to design many stereo or mono audio protocols such as I^2S, LSB or MSB-justified, PCM/DSP, TDM, or AC'97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio subblocks. Each block has it own clock generator and I/O line controller.

Audio sampling frequencies up to 192 kHz are supported.

Up to eight microphones can be supported thanks to an embedded PDM interface.

The SAI can work in master or slave configuration. The audio subblocks can be either receiver or transmitter, and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

3.53 SPDIF receiver interface (SPDIFRX)

The SPDIFRX is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby® or DTS® (up to 5.1).

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all necessary features to detect the symbol rate, and to decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal is available, the SPDIFRX re-samples the incoming signal, decodes the Manchester stream, and recognizes frames, sub-frames, and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate: this signal is used to compute the exact sample rate for clock drift algorithms.

3.54 Secure digital input/output MultiMediaCard interface (SDMMC1/2/3)

Three SDMMCs provide an interface between the AHB bus and SD memory cards, SDIO and e.MMC devices.

SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 5.1

Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit (HS200 speed limited by maximum allowed I/O speed, HS400 is not supported).

- Full compatibility with previous versions of MultiMediaCards (backward compatibility)
- Full compliance with SD memory card specifications version 6.0 (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI and UHS-II modes not supported)
- Full compliance with SDIO card specification version 4.0

Card support for two different databus modes: 1-bit (default) and 4-bit (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI and UHS-II modes not supported)

- Data transfer up to 208 Mbyte/s for the 8-bit mode (depending on the maximum allowed I/O speed)
- Data and command output enable signals to control external bidirectional drivers
- The SDMMC host interface embeds a dedicated DMA controller that allows high-speed transfers between the interface and the SRAM.
- IDMA linked list support

Each SDMMC is coupled with a delay block (DLYBSD) that supports an external data frequency above 100 MHz.

3.55 Controller area network (FDCAN1/2)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The CAN subsystem consists of two FDCANs, a shared message RAM, and a clock calibration unit.

All FDCANs are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B), and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TTCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10-Kbyte message RAM implements filters, receives FIFOs, receives buffers, transmits event FIFOs, transmits buffers (and triggers for TTCAN). This message RAM is shared between all FDCANs.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for FDCANs from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

3.56 Universal serial bus Hi-Speed host (USBH)

The devices embed one USB Hi-Speed host (up to 480 Mbit/s) with one physical port. USBH supports both low, full-speed (OHCI) as well as Hi-Speed (EHCI) operations. It integrates a physical interface (PHY) which can be used for either low-speed (1.2 Mbit/s), full-speed (12 Mbit/s) ,or Hi-Speed operation (480 Mbit/s).

The USBH is compliant with the USB 2.0 specification.

3.57 USB Type-C Power Delivery controller (UCPD1)

The devices embed one controller compliant with USB Type-C Rev.1.2 and USB Power Delivery Rev. 3.1 specifications.

The UCPD use specific I/Os supporting the USB Type-C and USB Power Delivery requirements, featuring:

- USB Type-C pull-up (Rp, all values) and pull-down (Rd) resistors
- USB Power Delivery message transmission and reception

The digital controller handles notably:

- USB Type-C level detection with de-bounce, generating interrupts
- byte-level interface for USB Power Delivery payload, generating interrupts (DMA compatible)
- USB Power Delivery timing dividers (including a clock pre-scaler)
- CRC generation/checking
- 4b5b encode/decode

- ordered sets (with a programmable ordered set mask at receive)
- frequency recovery in receiver during preamble

The interface offers low-power operation compatible with Stop mode, maintaining the capacity to detect incoming USB Power Delivery messages.

3.58 Universal serial bus 2.0 dual role data (USB3DR)

- xHCI model.
- Dual Role Data. The USB3DR can be configured statically as a Host or Device port.
- OTG is not supported:
  - Dynamic switch from Host (resp. Device) to Device (resp. Host) role is not supported.
  - Host Negotiation Protocol (HNP), Role Swap Protocol (RSP), Session Request Protocol (SRP), Attach Detection Protocol (ADP) are not supported.
- USB2 Low-Speed/Full-Speed/Hi-Speed modes (when Host) or USB2 Full-Speed/Hi-Speed modes (when Device).
- Descriptor caching and data pre-fetching to meet system performance.
- Variable FIFO buffer allocation for each endpoint.
- DMA engine
- Supports Battery Charging v1.2, with the exception of the Accessory Charger Adapter mode

The standards supported are:

- Universal Serial Bus Specification, Revision 2.0, USB Implementers Forum, Inc., April 27, 2000
- Errata for “USB Revision 2.0 April 27 2000” as of May 28, 2002, USB-IF
- eXtensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1, Intel Corp., December 20, 2013
- UTMI+ Specification, Revision 1.0, ULPI Working Group, February 25, 2004
- Battery Charging Specification, Revision 1.2, December 7, 2010

3.59 Gigabit Ethernet MAC interface (ETH1/2)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The devices embed two fully independent instances of a 10/100/1000 Ethernet MAC controller, that enable transmission and reception of data over Ethernet, in compliance with IEEE 802.3-2008.

Each Ethernet MAC controller is connected to an external Ethernet PHY via a standard media independent interface.

Features provided by the Ethernet controller include:

- 10, 100, and 1000 Mbit/s data transfer rates
- Full-duplex and half-duplex operations
- Standard or Jumbo Ethernet packets
- Two independent Rx queues and two independent Tx queues, with each queue associated to a (subset of) PCP code(s)
- Configurable media-independent interface to external PHY:
  - RGMII
  - MII
  - RMII
  - MDIO master interface for external PHY device configuration
  - Internal or external reference clocks
- Low-power support:
  - Energy Efficient Ethernet (EEE) compliant with IEEE 802.3az-2010;
  - Detection of LAN wake-up frames and “Magic Packet” frames

- Timing and synchronization:
  - compliance with IEEE 1588-2008 (PTP) and IEEE 802.1AS-Rev
  - hardware “auxiliary timestamp trigger” for accurate sampling of the “PTP system clock”
  - Internal or external system time
- Time-sensitive networking:
  - “Forwarding and Queuing Enhancements for Time-Sensitive Streams” compliant with IEEE 802.1Qav
  - “Enhancements to Scheduled Traffic” compliant with IEEE 802.1Qbv, with a gate control list depth up to 128
  - “Frame Preemption” compliant with IEEE 802.1Qbu and IEEE 802.3br
- Preamble and start-of-frame data insertion (for Tx) and deletion (for Rx)
- Option for automatic CRC generation (for Tx), checking and stripping (for Rx)
- Source address field insertion or replacement in transmitted packets
- Filtering options:
  - Perfect match with a given SA/DA (up to 3 MAC addresses are supported)
  - 64-bit Hash filter match
  - Several multicast/broadcast rules supported
  - Based on IEEE 802.1q ‘VLAN tag’ field (perfect match, hash filtering)
  - Support for different ‘VLAN tag’ filtering for each Rx queue
  - Based on TCP/UDP/IP address (perfect match, inverse filtering)
- TCP/IP offloading:
  - Checksum calculation and insertion in the transmit path
  - Checksum error detection in the receive path.
  - TCP segmentation offload (automatic split of a large TCP packet into smaller Ethernet frames)

3.60 Debug infrastructure

The devices offer a comprehensive set of debug and trace features to support software development and system integration.

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Serial-wire trace port
- Trace port
- Arm CoreSight debug and trace components

The debug can be controlled via a JTAG/serial-wire debug access port, using industry standard debugging tools.

A trace port allows data to be captured for logging and analysis.

4 Pinouts/ballouts, pin description, and alternate functions

4.1 Ballout schematics

Figure 6. STM32MP23xC/F TFBGA361 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	VSS	DSI_D3N	DSI_D2N	DSI_CKP	DSI_D1N	DSI_D0N	VDDDSI	PB10	PB0	PB5	PD8	PD1	PE0	PE6	PE11	PD12	DDR_DQ11	DDR_DQ9	VSS
B	VDDCSI	DSI_D3P	DSI_D2P	DSI_CKN	DSI_D1P	DSI_D0P	VDDA18DSI	PB7	PB6	PB4	PD0	PD15	PE1	PE7	PE9	PB12	DDR_DQ10	DDR_DQS1N	DDR_DQS1P
C	CSI_CKP	CSI_CKN	CSI_REXT	PI7	PI6	PG15	DSI_REXT	PB1	PB2	PD3	PD10	PI10	PE2	PE8	PB13	PI11	DDR_DQ8	DDR_DQ15	DDR_DQM1
D	CSI_D1P	CSI_D1N	VDDA18CSI	PG8	PI5	PI0	PB11	PB8	PD2	PD11	PD5	PD14	PE4	PE3	PE12	PD13	DDR_DQ14	DDR_DQ13	DDR_DQ12
E	CSI_D0N	CSI_D0P	PG14	PG9	PG10	PG11	PB9	PB3	PD9	PD4	PD7	PD6	PE5	PE10	PE13	PB14	DDR_RESETN	DDR_A9	DDR_A20
F	LVDS1_D0P	LVDS1_D0N	VDDLVDS	PI1	PF14	PG7	VDDA18PLL3	VDDA18PLL2	VDDIO4	VDDIO4	VDDIO3	VDDIO3	VDDIO2	VDDIO1	PE14	PE15	DDR_A0	DDR_A11	DDR_A21
G	LVDS1_D1P	LVDS1_D1N	VDDA18LVDS	PG12	PF15	PF13	VSS	VDDCORE	VSS	VDDCORE	VSS	VDDCPU	VSS	VDDQDDR	VSS	DDR_ZQ	DDR_A1	DDR_A10	DDR_A22
H	LVDS1_D2P	LVDS1_D2N	PG5	PI3	PG13	PI4	VDDCORE	VSS	VDDCORE	VSS	VDDCPU	VSS	VDDCPU	VSS	VDDA18PLL1	VSS	DDR_A25	DDR_A8	DDR_A23
J	LVDS1_D4P	LVDS1_D4N	PG6	PI9	PF12	PI2	VSS	VDDCORE	VSS	VDDCORE	VSS	VDDCPU	VSS	VDDQDDR	VSS	VDDA18DDR	DDR_A2	DDR_A13	DDR_A3
K	LVDS1_D3P	LVDS1_D3N	PZ8	PZ6	PC13	V08CAP	VDDCORE	VSS	VDDCORE	VSS	VDDGPU	VSS	VDDCPU	VSS	VDDQDDR	VSS	DDR_VREF	DDR_A14	DDR_A26
L	PZ9	PZ7	PZ2	PZ4	PZ0	VBAT	VSS	VDD	VSS	VDD	VSS	VDDGPU	VSS	VDDQDDR	VSS	VDDQDDR	DDR_A5	DDR_A15	DDR_A27
M	OSC32_OUT	OSC32_IN	PZ1	PZ5	PZ3	VDDA18AON	VSSAON	VSS	VDD	VSS	VDDGPU	VSS	VDDGPU	VSS	VDDQDDR	VSS	DDR_A4	DDR_A16	DDR_A28
N	NRST	PWR_CPU_ON	BOOT0	BOOT1	PI8	VDDA18ADC	VSSA	VDD	VSS	VDD	VSS	VDDGPU	VSS	VDDQDDR	VSS	VDDQDDR	DDR_A6	DDR_A17	DDR_A29
P	PDR_ON	NRSTC1MS	PWR_ON	BOOT3	PA0	PF10	PF5	PA14	PA13	PC0	PA6	PA7	PH2	PA1	Unused2	UCPD1_CC1	DDR_A7	DDR_A18	DDR_A30
R	OSC_IN	OSC_OUT	BOOT2	PF11	PF6	PF7	PC5	PA11	PA12	PF0	PF2	PH6	PH4	PH5	Unused4	VDD33USB	VDDA18USB	DDR_A12	DDR_A31
T	VREF-	VREF+	PG1	PG2	PF8	PC4	PC6	PH9	PF3	PA2	PA5	PH3	PA4	DNU	Unused1	USB3DR_TX RTUNE_	DDR_DQM0	DDR_DQ5	DDR_DQ4
U	JTDO-TRACESWO	NJTRST	PG3	PF9	PC11	PC7	PC10	PF1	PA15	PH7	PH8	PA3	PA8	Unused3	UCPD1_CC2	USBH_HS_TX RTUNE_	DDR_DQ3	DDR_DQ7	DDR_DQ6
V	JTCK-SWCLK	JTMS-SWDIO	PG4	PC12	PC3	PC8	PH12	PC2	PC1	PA9	DNU	DNU	DNU	ANA0	USBH_HS_DM	USB3DR_DM	DDR_DQ2	DDR_DQS0N	DDR_DQS0P
W	VSS	JTDI	PB15	PG0	PF4	PC9	PH13	PH11	PH10	PA10	DNU	DNU	DNU	ANA1	USBH_HS_DP	USB3DR_DP	DDR_DQ1	DDR_DQ0	VSS

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1. *The above figure shows the package top view.*
2. *VDDGPU, VDDA18DSI, VDDDSI, VDDA18LVDS, and VDDLVDS are DNU on product without the related feature (respectively GPU/NPU, DSI and LVDS) and must be connected to VSS. DSI_xxx and LVDSx_xxx are DNU on product without the related feature (respectively DSI and LVDS) and must be left open. See Section 2 for details on feature availability. Alternatively, for PCB compatibility purposes, those balls could be connected in same ways as for a product with enabled feature. Refer to AN5489 for additional details.*
3. *"Unusedx" represents a pin/ball that must be connected to V_{SS} at application level unless otherwise noted. For PCB compatibility within STM32MP2 series, Unusedx could be connected in same way than same pin/ball number defined for same package ballout of other STM32MP2 series.*

Figure 7. STM32MP23xC/F VFBGA361 ballout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	VSS	DSI_D3P	DSI_D2P	DSI_CKN	DSI_D0N	DSI_D1N	PB8	PB9	PB3	PD2	PD15	PD6	PD14	PE2	PE3	PE13	DDR_DQ11	DDR_DQ9	VSS
B	VDDCSI	DSI_D3N	DSI_D2N	DSI_CKP	DSI_D0P	DSI_D1P	PB11	PB0	PB5	PD11	PI10	PD5	PE0	PE4	PE8	PE11	DDR_DQ10	DDR_DQS1N	DDR_DQS1P
C	CSI_CKP	CSI_CKN	VSS	DSI_REXT	VDDA18DSI	VDDDSI	VSS	PB6	PB4	PD9	PD0	PD4	PE1	PE5	PE7	PE12	DDR_DQ8	DDR_DQ15	DDR_DQM1
D	CSI_D1P	CSI_D1N	VDDA18CSI	PI6	PI7	VDDIO4	PB7	PD3	PB1	VDDIO1	PD10	PD7	VSS	PE15	PE10	VDDA18DDR	DDR_DQ14	DDR_DQ13	DDR_DQ12
E	CSI_D0N	CSI_D0P	CSI_REXT	PG15	PG8	VDDIO4	PG7	VSS	PB2	VDDIO3	PD8	PB10	VDDCPU	PB12	VDDA18PLL1	VSS	DDR_RESETN	DDR_A9	DDR_A20
F	LVDS1_D0N	LVDS1_D0P	LVDS1_D1N	LVDS1_D1P	PG10	VSS	PG11	VDDIO2	PD1	VDDIO3	VSS	PI11	VSS	PE6	PE9	VDDQDDR	DDR_A0	DDR_A11	DDR_A21
G	PI4	PG9	LVDS1_D2N	LVDS1_D2P	PF15	VDDA18PLL2	PF14	VSS	PD13	VDDCORE	VSS	PH4	VDDCPU	PE14	PB13	DDR_ZQ	DDR_A1	DDR_A10	DDR_A22
H	PI0	PF13	LVDS1_D4N	LVDS1_D4P	PG14	VDDA18PLL3	PG12	VDD	PI3	VSS	VDDCORE	PG3	VSS	PD12	PB14	VSS	DDR_A25	DDR_A8	DDR_A23
J	VDDLVDS	LVDS1_D3N	LVDS1_D3P	VDDA18LVDS	PI2	VSS	PG13	VSS	PI1	VDDCORE	VSS	PA5	VDDCPU	VSS	PB15	VDDQDDR	DDR_A2	DDR_A13	DDR_A3
K	PG5	PG6	PZ6	VSS	VSS	PI9	PI5	VDD	PA8	VSS	VDDCORE	PA9	VSS	PH3	PA7	VSS	DDR_VREF	DDR_A14	DDR_A26
L	PZ7	PZ9	PZ8	PZ4	PZ0	VDD	PF12	VSS	PF10	VDDCORE	VSS	PH7	VDDCPU	PH2	PH6	VDDQDDR	DDR_A5	DDR_A15	DDR_A27
M	OSC32_OUT	OSC32_IN	PZ2	PZ1	PZ3	VSSAON	PG2	V08CAP	PH5	VSS	VDDGPU	PH8	VDDCPU	PA6	PA10	VDDQDDR	DDR_A4	DDR_A16	DDR_A28
N	PDR_ON	NRST	PZ5	PI8	VDDA18AON	VDDA18ADC	PG4	VDDCORE	PF0	VDDCORE	VSS	PA2	VSS	VDDGPU	PA1	VSS	DDR_A6	DDR_A17	DDR_A29
P	PWR_LP	PWR_CPU_ON	BOOT1	PC13	ANA1	VSSA	PF5	VSS	PF2	VSS	VDDGPU	PA4	VDDGPU	VSS	PA0	VDDQDDR	DDR_A7	DDR_A18	DDR_A30
R	OSC_IN	OSC_OUT	BOOT3	PG1	ANA0	VBAT	PC6	PA12	PA11	VDDGPU	VSS	PA3	Unused1	VDD33USB	USB3DR_TX RTUNE	VSS	DDR_A12	VSS	DDR_A31
T	NRST C1MS	BOOT0	BOOT2	PF11	PG0	PF9	PC5	PA14	PC2	PA15	PH11	DNU	VDDA18USB	Unused3	USBH_HS_TXR TUNE	VDDQDDR	DDR_DQM0	DDR_DQ5	DDR_DQ4
U	VREF-	VREF+	PWR_ON	PC3	PF6	PC8	PF8	PF1	PH13	PH10	VDD33UCPD	Unused2	DNU	DNU	DNU	DNU	DDR_DQ3	DDR_DQ7	DDR_DQ6
V	JTDO-TRACE SWO	NJTRST	PC4	PC12	PC11	PC9	PF7	PH12	PC0	PC1	USBH_HS_DM	USB3DR_DM	DNU	DNU	DNU	DNU	DDR_DQ2	DDR_DQS0N	DDR_DQS0P
W	VSS	JTMS-SWDIO	JTDI	JTCK-SWCLK	PC7	PC10	PF4	PH9	PA13	PF3	USBH_HS_DP	USB3DR_DP	UCPD1_CC1	UCPD1_CC2	DNU	Unused4	DDR_DQ1	DDR_DQ0	VSS

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1. *The above figure shows the package top view.*
2. *VDDGPU, VDDA18DSI, VDDDSI, VDDA18LVDS, and VDDLVDS are DNU on product without the related feature (respectively GPU/NPU, DSI and LVDS) and must be connected to VSS. DSI_xxx and LVDSx_xxx are DNU on product without the related feature (respectively DSI and LVDS) and must be left open. See Section 2 for details on feature availability. Alternatively, for PCB compatibility purposes, those balls could be connected in same ways as for a product with enabled feature. Refer to AN5489 for additional details.*
3. *"Unusedx" represents a pin/ball that must be connected to V_{SS} at application level unless otherwise noted. For PCB compatibility within STM32MP2 series, Unusedx could be connected in same way than same pin/ball number defined for same package ballout of other STM32MP2 series.*

Figure 8. STM32MP23xC/F VFBGA424 ballout

1. *The above figure shows the package top view.*
2. *VDDGPU, VDDA18DSI, VDDDSI, VDDA18LVDS, and VDDLVDS are DNU on product without the related feature (respectively GPU/NPU, DSI and LVDS) and must be connected to VSS. DSI_xxx and LVDSx_xxx are DNU on product without the related feature (respectively DSI and LVDS) and must be left open. See Section 2 for details on feature availability. Alternatively, for PCB compatibility purposes, those balls could be connected in same ways as for a product with enabled feature. Refer to AN5489 for additional details.*
3. *"Unusedx" represents a pin/ball that must be connected to V_{SS} at application level unless otherwise noted. For PCB compatibility within STM32MP2 series, Unusedx could be connected in same way than same pin/ball number defined for same package ballout of other STM32MP2 series.*

Table 9. I/O power domains

Supply pin	Pin names[1]
VDD	NRSTC1MS, PA0, PA1, PA10, PA11, PA12, PA13, PA14, PA15, PA2, PA3, PA4, PA5, PA6, PA7, PA8, PA9, PB12, PB13, PB14, PB15, PC0, PC1, PC10, PC11, PC12, PC2, PC6, PC7, PC8, PC9, PD12, PD13, PD14, PD15, PF0, PF1, PF10, PF11, PF12, PF13, PF14, PF15, PF2, PF3, PF4, PF5, PF8, PF9, PG0, PG10, PG11, PG12, PG13, PG14, PG15, PG2, PG4, PG5, PG6, PG7, PG8, PG9, PH10, PH11, PH12, PH13, PH2, PH3, PH4, PH5, PH6, PH7, PH8, PH9, PI0, PI1, PI10, PI11, PI2, PI3, PI4, PI5, PI6, PI7, PI9, PWR_CPU_ON, PWR_LP, PWR_ON, PZ7, PZ8, PZ9, JTCK-SWCLK, JTDI, JTDO-TRACESWO, JTMS-SWDIO, NJTRST, NRST
VDDIO1[2]	PE0, PE1, PE2, PE3, PE4, PE5
VDDIO2[3]	PE10, PE11, PE12, PE13, PE14, PE15, PE6, PE7, PE8, PE9
VDDIO3[4]	PD0, PD1, PD10, PD11, PD2, PD3, PD4, PD5, PD6, PD7, PD8, PD9
VDDIO4[5]	PB0, PB1, PB10, PB11, PB2, PB3, PB4, PB5, PB6, PB7, PB8, PB9
VDDA18AON	OSC_IN, OSC_OUT, PDR_ON
VSW[6]	OSC32_IN, OSC32_OUT, PC13, PI8, PZ0, PZ1, PZ2, PZ3, PZ4, PZ5, PZ6
VDD/VSW[6][7]	PC3, PC4, PC5, PF6, PF7, PG1, PG3

1. *Does not includes analog peripherals which have one or more dedicated supplies (for example PHYs).*
2. *Usually used for SD-Card using SDMMC1.*
3. *Usually used for e.MMC or SD-Card using SDMMC2.*
4. *Usually used for OCTOSPIM_P1.*
5. *Usually used for OCTOSPIM_P2.*
6. *VSW is supplied by V_{BAT} in absence of V_{DD}.*
7. *Pins with two supplies: V_{SW} supply for enabled TAMP_INx additional function, V_{DD} supply for GPIO and other alternate function.*

4.2 Ball description

Table 10. Legend/abbreviations used in the ballout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified, the function during and after reset is the same as the actual pin/ball name	
	DNU (do not use)	Represent a pin/ball that must be left unconnected (open) at application level unless otherwise noted. For PCB compatibility within STM32MP2 series, DNU could be connected in same way than same pin/ball number defined for same package ballout of other STM32MP2 series.
	Unusedx	Represent a pin/ball that must be connected to V_{SS} at application level unless otherwise noted. For PCB compatibility within STM32MP2 series, Unusedx could be connected in same way than same pin/ball number defined for same package ballout of other STM32MP2 series.
Pin type	S	Supply pin
	I	Input only pin
	O	Output only pin
	I/O	Input/output pin
	A	Analog or special level pin
I/O structure	TT(U/D/PD)	3.6 V capable I/O (with fixed pull-up/pull-down/programmable pull-down)[1]
	DDR	1.35 V, 1.2 V, or 1.1 V I/O for DDR3L, DDR4 or LPDDR4 interface
	A	Analog signal
	RST	Reset pin with weak pull-up resistor
	Option for TT I/Os	
	_f[2]	I3C option
	_a[2]	Analog option (supplied by $V_{DDA18ADC}$ for the analog part of the I/O)
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

1. *3.6 V capable only if related I/O supply is 3.3 V typ. and related VDDIOxVRSEL = 0.*
2. *The related I/O structures in table below are TT_f, TT_a and TT_af.*

Note: Alternate functions listed in following tables may be absent in some devices or packages (see Section 2 for details).

Table 11. STM32MP23xC/F ball definitions

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
V14	R5	-	ANA0	A	A	-	-	ADC1_INP0, ADC1_INN1, ADC2_INP0, ADC2_INN1, ADC3_INP0, ADC3_INN1
W14	P5	-	ANA1	A	A	-	-	ADC1_INP1, ADC2_INP1, ADC3_INP1
N3	T2	Y3	BOOT0	I	TTPD	(1)	-	-
N4	P3	AA3	BOOT1	I	TTPD	(1)	-	-
R3	T3	AB1	BOOT2	I	TTPD	(1)	-	-
P4	R3	AB2	BOOT3	I	TTPD	(1)	-	-
P16	W13	AB18	UCPD1_CC1	A	A	-	-	UCPD1_CC1
U15	W14	AA19	UCPD1_CC2	A	A	-	-	UCPD1_CC2
C2	C2	D4	CSI_CKN	A	A	-	-	-
C1	C1	C4	CSI_CKP	A	A	-	-	-
E1	E1	A3	CSI_D0N	A	A	-	-	-
E2	E2	B3	CSI_D0P	A	A	-	-	-
D2	D2	C5	CSI_D1N	A	A	-	-	-
D1	D1	B5	CSI_D1P	A	A	-	-	-
C3	E3	F6	CSI_REXT	A	A	-	-	-
F17	F17	U21	DDR_A0	O	DDR	-	-	-
G17	G17	AD25	DDR_A1	O	DDR	-	-	-
J17	J17	V24	DDR_A2	O	DDR	-	-	-
J19	J19	P22	DDR_A3	O	DDR	-	-	-
M17	M17	U23	DDR_A4	O	DDR	-	-	-
L17	L17	T24	DDR_A5	O	DDR	-	-	-
N17	N17	Y24	DDR_A6	O	DDR	-	-	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
P17	P17	AC25	DDR_A7	O	DDR	-	-	-
H18	H18	V22	DDR_A8	O	DDR	-	-	-
E18	E18	T22	DDR_A9	O	DDR	-	-	-
G18	G18	R23	DDR_A10	O	DDR	-	-	-
F18	F18	P24	DDR_A11	O	DDR	-	-	-
R18	R17	L23	DDR_A12	O	DDR	-	-	-
J18	J18	K24	DDR_A13	O	DDR	-	-	-
K18	K18	M24	DDR_A14	O	DDR	-	-	-
L18	L18	N23	DDR_A15	O	DDR	-	-	-
M18	M18	J23	DDR_A16	O	DDR	-	-	-
N18	N18	H24	DDR_A17	O	DDR	-	-	-
P18	P18	G23	DDR_A18	O	DDR	-	-	-
-	-	L21	DDR_A19	O	DDR	-	-	-
E19	E19	J21	DDR_A20	O	DDR	-	-	-
F19	F19	H22	DDR_A21	O	DDR	-	-	-
G19	G19	F22	DDR_A22	O	DDR	-	-	-
H19	H19	E23	DDR_A23	O	DDR	-	-	-
H17	H17	W21	DDR_A25	O	DDR	-	-	-
K19	K19	AB24	DDR_A26	O	DDR	-	-	-
L19	L19	AA23	DDR_A27	O	DDR	-	-	-
M19	M19	AC23	DDR_A28	O	DDR	-	-	-
N19	N19	Y22	DDR_A29	O	DDR	-	-	-
P19	P19	AA21	DDR_A30	O	DDR	-	-	-
R19	R19	W23	DDR_A31	O	DDR	-	-	-
T17	T17	AB25	DDR_DQM0	O	DDR	-	-	-
C19	C19	U26	DDR_DQM1	O	DDR	-	-	-
-	-	G27	DNU	-	-	-	-	-
-	-	M25	DNU	-	-	-	-	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
V18	V18	AA26	DDR_DQS0N	I/O	DDR	-	-	-
B18	B18	R25	DDR_DQS1N	I/O	DDR	-	-	-
-	-	F26	DNU	-	-	-	-	-
-	-	L27	DNU	-	-	-	-	-
V19	V19	AA25	DDR_DQS0P	I/O	DDR	-	-	-
B19	B19	T25	DDR_DQS1P	I/O	DDR	-	-	-
-	-	F27	DNU	-	-	-	-	-
-	-	L26	DNU	-	-	-	-	-
V17	V17	AB27	DDR_DQ2	I/O	DDR	-	-	-
U17	U17	AC27	DDR_DQ3	I/O	DDR	-	-	-
W17	W17	AC26	DDR_DQ1	I/O	DDR	-	-	-
W18	W18	AB26	DDR_DQ0	I/O	DDR	-	-	-
U18	U18	Y25	DDR_DQ7	I/O	DDR	-	-	-
U19	U19	W26	DDR_DQ6	I/O	DDR	-	-	-
T19	T19	W25	DDR_DQ4	I/O	DDR	-	-	-
T18	T18	W27	DDR_DQ5	I/O	DDR	-	-	-
D19	D19	V26	DDR_DQ12	I/O	DDR	-	-	-
C18	C18	U25	DDR_DQ15	I/O	DDR	-	-	-
D17	D17	V25	DDR_DQ14	I/O	DDR	-	-	-
D18	D18	V27	DDR_DQ13	I/O	DDR	-	-	-
A18	A18	R26	DDR_DQ9	I/O	DDR	-	-	-
C17	C17	R27	DDR_DQ8	I/O	DDR	-	-	-
A17	A17	P26	DDR_DQ11	I/O	DDR	-	-	-
B17	B17	P27	DDR_DQ10	I/O	DDR	-	-	-
-	-	J25	DNU	-	-	-	-	-
-	-	H25	DNU	-	-	-	-	-
-	-	G25	DNU	-	-	-	-	-
-	-	G26	DNU	-	-	-	-	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
-	-	E25	DNU	-	-	-	-	-
-	-	F25	DNU	-	-	-	-	-
-	-	F24	DNU	-	-	-	-	-
-	-	E26	DNU	-	-	-	-	-
-	-	P25	DNU	-	-	-	-	-
-	-	N26	DNU	-	-	-	-	-
-	-	L25	DNU	-	-	-	-	-
-	-	N25	DNU	-	-	-	-	-
-	-	K25	DNU	-	-	-	-	-
-	-	K26	DNU	-	-	-	-	-
-	-	K27	DNU	-	-	-	-	-
-	-	J26	DNU	-	-	-	-	-
K17	K17	G21	DDR_VREF	A	A	-	-	-
E17	E17	E21	DDR_RESETN	O	DDR	-	-	-
G16	G16	K22	DDR_ZQ	A	A	-	-	-
B4	A4	C8	DSI_CKN	A	A	(2)	-	-
A4	B4	C7	DSI_CKP	A	A	(2)	-	-
A6	A5	C9	DSI_D0N	A	A	(2)	-	-
B6	B5	B9	DSI_D0P	A	A	(2)	-	-
A5	A6	A10	DSI_D1N	A	A	(2)	-	-
B5	B6	B10	DSI_D1P	A	A	(2)	-	-
A3	B3	A7	DSI_D2N	A	A	(2)	-	-
B3	A3	B7	DSI_D2P	A	A	(2)	-	-
A2	B2	B6	DSI_D3N	A	A	(2)	-	-
B2	A2	A6	DSI_D3P	A	A	(2)	-	-
C7	C4	D6	DSI_REXT	A	A	(2)	-	-
V1	W4	AA5	JTCK-SWCLK	I	TTD	(1)	-	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
W2	W3	AE3	JTDI	I	TTU	(1)	-	-
U1	V1	AC2	JTDO-TRACESWO	O	TTU	(1)	-	-
V2	W2	AE2	JTMS-SWDIO	I/O	TTU	(1)	-	-
F2	F1	G3	LVDS1_D0N	A	A	(2)	-	-
F1	F2	G2	LVDS1_D0P	A	A	(2)	-	-
G2	F3	H4	LVDS1_D1N	A	A	(2)	-	-
G1	F4	H3	LVDS1_D1P	A	A	(2)	-	-
H2	G3	J2	LVDS1_D2N	A	A	(2)	-	-
H1	G4	J1	LVDS1_D2P	A	A	(2)	-	-
K2	J2	L3	LVDS1_D3N	A	A	(2)	-	-
K1	J3	L2	LVDS1_D3P	A	A	(2)	-	-
J2	H3	K2	LVDS1_D4N	A	A	(2)	-	-
J1	H4	K1	LVDS1_D4P	A	A	(2)	-	-
-	-	B2	DNU	-	-	-	-	-
-	-	B1	DNU	-	-	-	-	-
-	-	C3	DNU	-	-	-	-	-
-	-	C2	DNU	-	-	-	-	-
-	-	D3	DNU	-	-	-	-	-
-	-	E3	DNU	-	-	-	-	-
-	-	E2	DNU	-	-	-	-	-
-	-	E1	DNU	-	-	-	-	-
-	-	F2	DNU	-	-	-	-	-
-	-	F1	DNU	-	-	-	-	-
U2	V2	AF3	NJTRST	I	TTU	(1)	-	-
N1	N2	AE1	NRST	I/O	RST	(1)	-	-
P2	T1	W3	NRSTC1MS	O	TT	(3)	-	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
P5	P15	AF5	PA0	I/O	TT_a	(1)	LPTIM1_CH2, SPI5_RDY, SAI2_MCLK_B, UART5_TX(boot), USART3_TX, TIM3_ETR, TIM5_CH2, ETH2_MII_RXD2, FMC_NL, DCMI_D9/PSSI_D9/ DCMIPP_D9, EVENTOUT	WKUP1
P14	N15	AC19	PA1	I/O	TT_af	(1)	SAI3_SD_A, USART1_RTS/USART1_DE, USART6_CK, TIM4_CH2, LCD_R3, DCMI_D5/PSSI_D5/DCMIPP_D5, EVENTOUT	-
T10	N12	AF17	PA2	I/O	TT_af	(1)	LPTIM2_IN1, USART1_RX, I3C1_SDA, I2C1_SDA, LCD_B0, DCMI_D3/PSSI_D3/DCMIPP_D3, EVENTOUT	-
U12	R12	AD18	PA3	I/O	TT_af	(1)	LPTIM2_ETR, USART1_TX, I3C1_SCL, I2C7_SMBA, I2C1_SCL, LCD_B1, DCMI_D2/PSSI_D2/DCMIPP_D2, EVENTOUT	-
T13	P12	AG17	PA4	I/O	TT_a	(1)	USART2_TX(boot), FDCAN2_TX, TIM2_CH1, LCD_R1, ETH1_PTP_AUX_TS, EVENTOUT	-
T11	J12	AE17	PA5	I/O	TT	(1)	SPI4_MOSI, SAI2_MCLK_B, SAI2_SD_B, USART2_RTS/ USART2_DE, FDCAN2_RX, TIM2_CH4, LCD_G0, FMC_A0, DCMI_D13/PSSI_D13/DCMIPP_D13, EVENTOUT	-
P11	M14	AF18	PA6	I/O	TT	(1)	SPI4_SCK, SAI2_FS_B, USART2_CK, TIM13_CH1, TIM2_ETR, LCD_G4, FMC_NE1, DCMI_D12/PSSI_D12/ DCMIPP_D12, EVENTOUT	-
P12	K15	AE18	PA7	I/O	TT	(1)	AUDIOCLK, MDF1_CCK0, USART1_CTS/USART1_NSS, TIM4_ETR, I2C2_SMBA, LCD_B5, DCMI_D6/PSSI_D6/ DCMIPP_D6, EVENTOUT	-
U13	K9	AA17	PA8	I/O	TT_f	(1)	LPTIM2_CH2, SAI1_FS_B, USART1_CK, USART2_RX(boot), LCD_B2, DCMI_D4/PSSI_D4/ DCMIPP_D4, EVENTOUT	-
V10	K12	AF15	PA9	I/O	TT	(1)	SPI4_NSS, SAI2_SCK_B, USART2_CTS/USART2_NSS, LPTIM5_ETR, TIM2_CH3, ETH1_MDC, LCD_G7, PSSI_D14/DCMIPP_D14, EVENTOUT	-
W10	M15	AE15	PA10	I/O	TT	(1)	SPI4_MISO, SAI2_SD_B, USART2_RX, LPTIM5_IN1, TIM2_CH2, ETH1_MDIO, LCD_R6, PSSI_D15/ DCMIPP_D15, EVENTOUT	-
R8	R9	AD12	PA11	I/O	TT	(1)	SPI8_SCK, LPTIM2_CH1, SAI4_SD_B, ETH1_MII_RX_DV/ETH1_RGMII_RX_CTL/ ETH1_RMII_CRS_DV, EVENTOUT	-
R9	R8	AC13	PA12	I/O	TT_f	(1)	SAI3_FS_A, TIM4_CH1, ETH1_PHY_INTN, EVENTOUT	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
P9	W9	AD14	PA13	I/O	TT	(1)	SPI8_RDY, I2S3_MCK, LPTIM2_ETR, MDF1_CKI3, USART2_CTS/USART2_NSS, I2C7_SMBA, ETH1_MII_TX_EN/ETH1_RGMII_TX_CTL/ ETH1_RMII_TX_EN, EVENTOUT	-
P8	T8	AB12	PA14	I/O	TT	(1)	SPI8_NSS, LPTIM2_CH2, SAI4_FS_B, MDF1_CCK1, ETH1_MII_RX_CLK/ETH1_RGMII_RX_CLK/ ETH1_RMII_REF_CLK, EVENTOUT	-
U9	T10	AE13	PA15	I/O	TT_f	(1)	SPI3_MISO/I2S3_SDI, USART2_RX, I2C7_SDA, ETH1_MII_TXD0/ETH1_RGMII_TXD0/ETH1_RMII_TXD0, EVENTOUT	-
A9	B8	B13	PB0	I/O	TT	(4)	SPI2_SCK/I2S2_CK, USART1_CK, TIM16_CH1, OCTOSPIM_P2_IO0(boot), EVENTOUT	-
C8	D9	C12	PB1	I/O	TT	(4)	SPI3_NSS/I2S3_WS, TIM16_CH1N, OCTOSPIM_P2_IO1(boot), FMC_NCE4, EVENTOUT	-
C9	E9	A14	PB2	I/O	TT	(4)	SPI2_MOSI/I2S2_SDO, MDF1_CKI3, TIM17_BKIN, TIM16_BKIN, OCTOSPIM_P2_IO2(boot), EVENTOUT	-
E8	A9	B14	PB3	I/O	TT	(4)	SPI2_NSS/I2S2_WS, MDF1_SDI3, OCTOSPIM_P2_IO3(boot), FMC_NCE3, EVENTOUT	-
B10	C9	B15	PB4	I/O	TT_f	(4)	SPI2_RDY, UART4_CTS, SAI4_FS_B, TIM14_CH1, I2C2_SDA, OCTOSPIM_P2_IO4(boot), I3C2_SDA, EVENTOUT	-
A10	B9	C14	PB5	I/O	TT_f	(4)	I2S2_MCK, UART4_RTS/UART4_DE, SAI4_SD_B, I2C2_SCL, OCTOSPIM_P2_IO5(boot), FMC_AD8/ FMC_D8(boot), I3C2_SCL, SDMMC3_D123DIR, EVENTOUT	-
B9	C8	C13	PB6	I/O	TT	(4)	SPI2_MISO/I2S2_SDI, UART4_RX, SAI4_SCK_B, OCTOSPIM_P2_IO6(boot), FMC_AD9/FMC_D9(boot), SDMMC3_D0DIR, EVENTOUT	-
B8	D7	C11	PB7	I/O	TT	(4)	SPI3_SCK/I2S3_CK, UART4_TX, SAI4_MCLK_B, TIM12_CH1, OCTOSPIM_P2_IO7(boot), FMC_AD10/ FMC_D10(boot), SDMMC3_CDIR, EVENTOUT	-
D8	A7	D8	PB8	I/O	TT	(4)	SPI3_MOSI/I2S3_SDO, USART1_TX, TIM17_CH1, OCTOSPIM_P2_NCS1(boot), FMC_AD12/ FMC_D12(boot), EVENTOUT	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
E7	A8	F10	PB9	I/O	TT	(4)	SPI3_RDY, USART1_RTS/USART1_DE, FDCAN1_TX, TIM10_CH1, OCTOSPIM_P2_DQS(boot), OCTOSPIM_P2_NCS2, FMC_AD13/FMC_D13(boot), EVENTOUT	-
A8	E12	B11	PB10	I/O	TT	(4)	SPI3_MISO/I2S3_SDI, USART1_RX, TIM17_CH1N, OCTOSPIM_P2_CLK(boot), FMC_AD15/FMC_D15(boot), EVENTOUT	-
D7	B7	A11	PB11	I/O	TT	(4)	I2S3_MCK, USART1_CTS/USART1_NSS, FDCAN1_RX, TIM12_CH2, OCTOSPIM_P2_NCLK(boot), OCTOSPIM_P2_NCS2, FMC_AD14/FMC_D14(boot), OCTOSPIM_P1_NCS2, EVENTOUT	-
B16	E14	C26	PB12	I/O	TT_a	(1)	TIM13_CH1, DSI_TE, SDMMC3_D2, FMC_NWAIT, DCMI_D12/PSSI_D12/DCMIPP_D12, EVENTOUT	-
C15	G15	A26	PB13	I/O	TT_a	(1)	SAI1_SD_B, SDMMC3_CK, FMC_AD5/FMC_D5(boot), FMC_AD0/FMC_D0, EVENTOUT	-
E16	H15	C27	PB14	I/O	TT	(1)	SPI2_SCK/I2S2_CK, TIM4_CH2, SDMMC3_D0, FMC_AD7/FMC_D7(boot), FMC_AD2/FMC_D2, EVENTOUT	-
W3	J15	AE6	PB15	I/O	TT_a	(1)	LPTIM1_IN2, SPI5_SCK, SAI2_SD_B, UART5_RX(boot), TIM3_CH2, TIM5_CH1, ETH1_PPS_OUT, FMC_A18, LCD_R4, DCMI_D8/PSSI_D8/DCMIPP_D8, EVENTOUT	ADC1_INP15, ADC3_INP5
W13	V13	AE26	DNU	-	-	-	-	-
V13	U13	AE25	DNU	-	-	-	-	-
-	V14	AG26	DNU	-	-	-	-	-
-	U14	AF26	DNU	-	-	-	-	-
P10	V9	AB14	PC0	I/O	TT	(1)	LPTIM1_CH1, SAI3_MCLK_B, USART6_TX, DCMI_D0/ PSSI_D0/DCMIPP_D0, ETH2_MII_RX_CLK/ ETH2_RMII_REF_CLK, ETH1_MII_TX_CLK, ETH1_RGMII_GTX_CLK, LCD_G7, EVENTOUT	-
V9	V10	AG14	PC1	I/O	TT_f	(1)	SPI3_MOSI/I2S3_SDO, USART2_TX, I2C7_SCL, ETH1_MII_TXD1/ETH1_RGMII_TXD1/ETH1_RMII_TXD1, EVENTOUT	-
V8	T9	AE12	PC2	I/O	TT	(1)	SPI8_MOSI, LPTIM2_IN1, SAI4_MCLK_B, MDF1_SDI3, USART2_RTS/USART2_DE, ETH1_MII_RXD1/ ETH1_RGMII_RXD1/ETH1_RMII_RXD1, EVENTOUT	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
V5	U4	AA9	PC3	I/O	TT_a	(5)	LPTIM1_IN2, SPI3_NSS/I2S3_WS, USART6_RTS/ USART6_DE, FDCAN2_TX, ETH2_MII_RX_DV/ ETH2_RGMII_RX_CTL/ETH2_RMII_CRS_DV, ETH1_MII_RX_ER, LCD_G6, DCMI_D3/PSSI_D3/ DCMIPP_D3, EVENTOUT	ADC1_INP12, ADC1_INN10, ADC2_INP12, ADC2_INN10, ADC3_INP12, ADC3_INN10, TAMP_IN3
T6	V3	AC9	PC4	I/O	TT	(5)	SAI3_FS_B, ETH2_MII_TX_EN/ETH2_RGMII_TX_CTL/ ETH2_RMII_TX_EN, ETH1_RGMII_CLK125, LCD_R0, EVENTOUT	TAMP_IN1
R7	T7	AD10	PC5	I/O	TT_af	(5)	SPDIFRX1_IN1, MDF1_SDI1, TIM8_CH1N, ETH2_MDIO, ETH1_MII_COL, FMC_A25, ETH1_PPS_OUT, LCD_DE, EVENTOUT	ADC1_INP10, ADC2_INP10, ADC3_INP10, TAMP_IN6
T7	R7	AB10	PC6	I/O	TT_af	(1)	RTC_REFIN, SPDIFRX1_IN0, MDF1_CKI1, TIM8_CH1, ETH2_MDC, ETH1_MII_CRS, FMC_A24, ETH1_PHY_INTN, LCD_CLK, EVENTOUT	ADC1_INP9, ADC1_INN5, ADC2_INP9, ADC2_INN5
U6	W5	AF9	PC7	I/O	TT_a	(1)	SAI3_SD_B, TIM8_CH2N, ETH2_MII_TXD0/ ETH2_RGMII_TXD0/ETH2_RMII_TXD0, ETH1_MII_TXD2, LCD_B4, DCMI_D1/PSSI_D1/ DCMIPP_D1, EVENTOUT	ADC3_INP9, ADC3_INN5
V6	U6	AG9	PC8	I/O	TT_a	(1)	LPTIM1_ETR, SAI3_SCK_B, USART6_CTS/ USART6_NSS, TIM8_CH2, ETH2_MII_TXD1/ ETH2_RGMII_TXD1/ETH2_RMII_TXD1, ETH1_MII_TXD3, LCD_B3, DCMI_D2/PSSI_D2/ DCMIPP_D2, EVENTOUT	-
W6	V6	AE9	PC9	I/O	TT_a	(1)	MCO1, SPI3_MISO/I2S3_SDI, SAI2_SCK_A, TIM13_CH1, TIM8_CH4N, USBH_HS_OVRCUR, ETH2_MII_TXD2/ETH2_RGMII_TXD2, USB3DR_OVRCUR, FMC_A22, LCD_G2, DCMI_D7/ PSSI_D7/DCMIPP_D7, EVENTOUT	ADC1_INP8, ADC1_INN4, ADC2_INP8, ADC2_INN4
U7	W6	AG10	PC10	I/O	TT_a	(1)	SPI3_MOSI/I2S3_SDO, LPTIM4_ETR, TIM8_CH4, USBH_HS_VBUSEN, ETH2_MII_TXD3/ ETH2_RGMII_TXD3, USB3DR_VBUSEN, FMC_A23, LCD_G3, DCMI_D6/PSSI_D6/DCMIPP_D6, EVENTOUT	ADC1_INP5, ADC2_INP5

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
U5	V5	AD8	PC11	I/O	TT_a	(1)	LPTIM1_CH1, SPI5_NSS, SAI2_MCLK_A, UART5_RTS/ UART5_DE, USART3_RTS/USART3_DE, TIM3_CH1, TIM5_ETR, ETH2_MII_RXD3/ETH2_RGMII_RXD3, FMC_NBL1, LCD_R2, DCMI_D10/PSSI_D10/ DCMIPP_D10, EVENTOUT	ADC1_INP7, ADC1_INN3, ADC2_INP7, ADC2_INN3, ADC3_INP7, ADC3_INN3
V4	V4	AE7	PC12	I/O	TT_af	(1)	LPTIM1_CH2, MDF1_CKI2, TIM8_CH3, ETH2_MII_RXD1/ETH2_RGMII_RXD1/ ETH2_RMII_RXD1, ETH1_MII_RXD3, LCD_G1, DCMI_D5/PSSI_D5/DCMIPP_D5, EVENTOUT	ADC1_INP17
K5	P4	W7	PC13	I/O	TT	(6)	EVENTOUT	RTC_OUT1/ RTC_LSCO/ RTC_TS, TAMP_OUT1
M2	M2	AA2	OSC32_IN	I	A	(7)	-	OSC32_IN
M1	M1	AA1	OSC32_OUT	O	A	(8)	-	OSC32_OUT
P1	N1	W2	PDR_ON	I	-	(9)	-	-
B11	C11	B17	PD0	I/O	TT	(10)	TRACECLK, HDP0, SAI1_D2, SAI4_FS_A, UART7_RX, TIM15_CH2, SDVSEL1, OCTOSPIM_P1_CLK(boot), DCMI_PIXCLK/PSSI_PDCK/DCMIPP_PIXCLK, EVENTOUT	-
A12	F9	A19	PD1	I/O	TT	(10)	HDP1, SPI1_MISO/I2S1_SDI, SAI1_CK2, SAI4_SD_A, UART7_RTS/UART7_DE, TIM15_CH1, TIM1_BKIN, OCTOSPIM_P1_NCLK(boot), OCTOSPIM_P1_NCS2, OCTOSPIM_P2_NCS2, DCMI_HSYNC/PSSI_DE/ DCMIPP_HSYNC, EVENTOUT	-
D9	A10	D12	PD2	I/O	TT	(10)	HDP2, SPI1_NSS/I2S1_WS, SAI1_CK1, SAI4_SCK_A, UART7_CTS, TIM15_BKIN, TIM1_ETR, OCTOSPIM_P1_DQS(boot), OCTOSPIM_P1_NCS2, DCMI_VSYNC/PSSI_RDY/DCMIPP_VSYNC, EVENTOUT	-
C10	D8	G13	PD3	I/O	TT	(10)	SAI1_MCLK_A, SPI2_SCK/I2S2_CK, SAI1_D1, SAI4_MCLK_A, UART7_TX, TIM15_CH1N, TIM1_BKIN2, SDVSEL2, OCTOSPIM_P1_NCS1(boot), PSSI_D15/ DCMIPP_D15, EVENTOUT	-
E10	C12	C18	PD4	I/O	TT	(10)	TRACED0, SPI4_MISO, HDP3, SAI1_D3, SAI1_SD_B, TIM1_CH4N, TIM4_CH1, OCTOSPIM_P1_IO0(boot), PSSI_D14/DCMIPP_D14, EVENTOUT	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
D11	B12	B18	PD5	I/O	TT	(10)	TRACED1, SPI4_NSS, HDP4, SAI1_D4, SAI1_FS_B, TIM1_CH3N, TIM4_CH2, OCTOSPIM_P1_IO1(boot), DCMI_D13/PSSI_D13/DCMIPP_D13, EVENTOUT	-
E12	A12	A18	PD6	I/O	TT	(10)	TRACED2, SPI4_MOSI, HDP5, SAI1_SCK_B, MDF1_SDI2, TIM1_CH2N, TIM4_CH3, OCTOSPIM_P1_IO2(boot), DCMI_D12/PSSI_D12/ DCMIPP_D12, EVENTOUT	-
E11	D12	D20	PD7	I/O	TT	(10)	TRACED3, SPI4_SCK, SPI1_RDY, SAI1_MCLK_B, MDF1_CKI2, TIM1_CH1N, TIM4_CH4, OCTOSPIM_P1_IO3(boot), DCMI_D11/PSSI_D11/ DCMIPP_D11, EVENTOUT	-
A11	E11	C16	PD8	I/O	TT	(10)	TRACED4, SPI4_RDY, I2S1_MCK, SAI1_FS_A, UART4_CTS, MDF1_SDI1, TIM1_CH4, TIM4_ETR, OCTOSPIM_P1_IO4(boot), SDMMC1_D7, SDMMC1_D123DIR, DCMI_D10/PSSI_D10/ DCMIPP_D10, EVENTOUT	-
E9	C10	C15	PD9	I/O	TT	(10)	TRACED5, HDP6, SPI1_MOSI/I2S1_SDO, SAI1_SD_A, UART4_RTS/UART4_DE, MDF1_CKI1, TIM1_CH3, OCTOSPIM_P1_IO5(boot), SDMMC1_D6, SDMMC1_D0DIR, DCMI_D9/PSSI_D9/DCMIPP_D9, EVENTOUT	-
C11	D11	C17	PD10	I/O	TT_f	(10)	TRACED6, HDP7, SAI1_SCK_A, UART4_RX, MDF1_SDI0, TIM1_CH2, TIM14_CH1, OCTOSPIM_P1_IO6(boot), SDMMC1_D5, SDMMC1_CDIR, DCMI_D8/PSSI_D8/DCMIPP_D8, EVENTOUT	-
D10	B10	A15	PD11	I/O	TT_f	(10)	TRACED7, SPI1_SCK/I2S1_CK, SAI1_MCLK_A, UART4_TX, MDF1_CKI0, TIM1_CH1, SDVSEL1, OCTOSPIM_P1_IO7(boot), SDMMC1_D4, SDMMC1_CKIN, DCMI_D7/PSSI_D7/DCMIPP_D7, EVENTOUT	-
A16	H14	B26	PD12	I/O	TT_a	(1)	SPI2_MISO/I2S2_SDI, SPDIFRX1_IN2, TIM4_ETR, SDMMC3_CMD, FMC_AD6/FMC_D6(boot), FMC_AD1/ FMC_D1, EVENTOUT	-
D16	G9	D25	PD13	I/O	TT_a	(1)	SPI2_NSS/I2S2_WS, TIM4_CH4, SDMMC3_D1, FMC_AD11/FMC_D11(boot), FMC_NWE, EVENTOUT	-
D12	A13	E19	PD14	I/O	TT_af	(1)	I2S1_MCK, FDCAN1_RX, TIM11_CH1, I2C7_SDA, FMC_AD4/FMC_D4(boot), SDMMC3_D3, DCMI_D1/ PSSI_D1/DCMIPP_D1, EVENTOUT	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
B12	A11	E15	PD15	I/O	TT_af	(1)	SPI1_RDY, DSI_TE, FDCAN1_TX, TIM1_BKIN2, TIM5_ETR, I2C7_SCL, FMC_AD3/FMC_D3(boot), SDMMC3_CKIN, DCMI_D0/PSSI_D0/DCMIPP_D0, EVENTOUT	-
A13	B13	B19	PE0	I/O	TT	(11)	TRACED2, LPTIM2_CH1, SPI1_SCK/I2S1_CK, SPI3_RDY, USART3_CK, SDMMC1_D2, EVENTOUT	-
B13	C13	C19	PE1	I/O	TT	(11)	TRACED3, LPTIM2_CH2, I2S1_MCK, I2S3_MCK, USART3_RX, SDMMC1_D3, EVENTOUT	-
C13	A14	C20	PE2	I/O	TT	(11)	LPTIM2_ETR, SPI1_MISO/I2S1_SDI, SPI3_MOSI/ I2S3_SDO, SAI1_SCK_B, TIM10_CH1, SDMMC1_CMD(boot), EVENTOUT	-
D14	A15	C21	PE3	I/O	TT	(11)	TRACECLK, SPI1_RDY, SPI3_SCK/I2S3_CK, SAI1_MCLK_B, USART3_TX, TIM11_CH1, SDMMC1_CK(boot), EVENTOUT	-
D13	B14	B21	PE4	I/O	TT	(11)	TRACED0, LPTIM2_IN1, SPI1_MOSI/I2S1_SDO, SPI3_MISO/I2S3_SDI, SAI1_SD_B, USART3_CTS/ USART3_NSS, FDCAN1_TX, SDMMC1_D0(boot), EVENTOUT	-
E13	C14	C22	PE5	I/O	TT	(11)	TRACED1, LPTIM2_IN2, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SAI1_FS_B, USART3_RTS/ USART3_DE, FDCAN1_RX, SDMMC1_D1, EVENTOUT	-
A14	F14	A22	PE6	I/O	TT	(12)	SPI4_RDY, SPDIFRX1_IN2, USART1_TX, TIM1_ETR, FMC_AD1/FMC_D1(boot), SDMMC2_D6, SDMMC2_D0DIR, EVENTOUT	-
B14	C15	B22	PE7	I/O	TT	(12)	SAI4_D4, SPDIFRX1_IN3, USART1_RX, TIM1_CH4N, TIM14_CH1, FMC_AD2/FMC_D2(boot), SDMMC2_D7, SDMMC2_D123DIR, EVENTOUT	-
C14	B15	C23	PE8	I/O	TT	(12)	SPI4_MOSI, SAI4_CK1, SAI4_MCLK_A, MDF1_CKI0, TIM1_CH1, FMC_A17/FMC_ALE(boot), SDMMC2_D2, EVENTOUT	-
B15	F15	A23	PE9	I/O	TT	(12)	SPI4_MISO, SAI4_D2, SAI4_FS_A, USART1_CK, TIM1_CH4, FMC_AD0/FMC_D0(boot), SDMMC2_D5, SDMMC2_CDIR, EVENTOUT	-
E14	D15	D22	PE10	I/O	TT	(12)	SPI4_SCK, SAI4_D1, SAI4_SD_A, USART1_CTS/ USART1_NSS, TIM1_CH3, FMC_NE3, FMC_NCE2, SDMMC2_D4, SDMMC2_CKIN, EVENTOUT	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
A15	B16	B23	PE11	I/O	TT	(12)	SAI4_D3, SAI1_FS_A, TIM15_CH2, TIM1_CH3N, FMC_A16/FMC_CLE(boot), SDMMC2_D1, EVENTOUT	-
D15	C16	C25	PE12	I/O	TT	(12)	SPI4_NSS, SAI4_CK2, SAI4_SCK_A, MDF1_SDI0, USART1_RTS/USART1_DE, TIM1_CH2, FMC_NE2, FMC_NCE1(boot), SDMMC2_D3, EVENTOUT	-
E15	A16	C24	PE13	I/O	TT	(12)	SAI1_SD_A, TIM15_CH1, TIM1_CH2N, FMC_RNB(boot), SDMMC2_D0(boot), EVENTOUT	-
F15	G14	B25	PE14	I/O	TT	(12)	SAI1_MCLK_A, TIM15_BKIN, TIM1_BKIN, FMC_NWE(boot), SDMMC2_CK(boot), EVENTOUT	-
F16	D14	D24	PE15	I/O	TT	(12)	SAI1_SCK_A, TIM15_CH1N, TIM1_CH1N, FMC_NOE(boot), SDMMC2_CMD(boot), EVENTOUT	-
R10	N9	AA15	PF0	I/O	TT_af	(1)	SPI3_SCK/I2S3_CK, FDCAN2_RX, TIM12_CH2, I2C2_SDA, ETH1_MDC, ETH2_MII_CRS, I3C2_SDA, EVENTOUT	ADC1_INP11, ADC2_INP11, ADC3_INP11
U8	U8	AE11	PF1	I/O	TT	(1)	SPI8_MISO, LPTIM2_IN2, SAI4_SCK_B, USART2_CK, ETH1_MII_RXD0/ETH1_RGMII_RXD0/ ETH1_RMII_RXD0, EVENTOUT	-
R11	P9	AC15	PF2	I/O	TT_af	(1)	SPI3_RDY, TIM12_CH1, I2C2_SCL, ETH1_MDIO, ETH2_MII_COL, FMC_NE4, I3C2_SCL, EVENTOUT	ADC1_INP13, ADC1_INN11, ADC2_INP13, ADC2_INN11, ADC3_INP13, ADC3_INN11
T9	W10	AF11	PF3	I/O	TT_a	(1)	SAI2_SCK_B, MDF1_CCK0, TIM3_CH4, TIM8_BKIN2, ETH1_CLK, ETH2_PPS_OUT, FMC_A20, LCD_R6, DCMI_HSYNC/PSSI_DE/DCMIPP_HSYNC, EVENTOUT	ADC1_INP16, ADC1_INN15
W5	W7	AF10	PF4	I/O	TT	(1)	RTC_OUT2, SAI3_SCK_A, USART6_RX(boot), TIM4_CH4, ETH1_MDC, ETH2_CLK, ETH2_PPS_OUT, ETH1_PPS_OUT, LCD_B7, EVENTOUT	-
P7	P7	AA11	PF5	I/O	TT	(1)	SAI3_MCLK_A, USART6_TX(boot), TIM4_CH3, ETH1_MDIO, ETH1_CLK, ETH2_PHY_INTN, ETH1_PHY_INTN, LCD_B6, EVENTOUT	-
R5	U5	AC7	PF6	I/O	TT	(5)	RTC_OUT2, SAI3_MCLK_B, USART6_CK, TIM12_CH1, ETH2_MII_RX_CLK/ETH2_RGMII_RX_CLK/ ETH2_RMII_REF_CLK, LCD_B0, EVENTOUT	TAMP_IN5

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
R6	V7	AB8	PF7	I/O	TT	(5)	SPDIFRX1_IN1, SAI3_SD_A, TIM2_ETR, ETH2_RGMII_GTX_CLK, ETH2_MII_TX_CLK, LCD_R1, EVENTOUT	TAMP_IN2
T5	U7	AE10	PF8	I/O	TT	(1)	RTC_REFIN, SAI3_SCK_B, USART3_RX, TIM12_CH2, ETH1_CLK, ETH2_RGMII_CLK125, ETH2_MII_RX_ER, ETH2_MII_RX_DV/ETH2_RMII_CRS_DV, LCD_G0, EVENTOUT	-
U4	T6	AE8	PF9	I/O	TT	(1)	SAI3_SD_B, SAI2_SD_A, TIM2_CH2, ETH2_MII_RXD2/ ETH2_RGMII_RXD2, ETH2_MDIO, EVENTOUT	-
P6	L9	AE5	PF10	I/O	TT_a	(1)	MCO2, SPI3_RDY, SAI2_MCLK_A, TIM2_CH3, ETH2_MII_TXD2, EVENTOUT	ADC3_INP2
R4	T4	AE4	PF11	I/O	TT_a	(1)	MCO1, SPDIFRX1_IN0, SAI2_SCK_A, TIM2_CH4, ETH2_MII_TXD3, EVENTOUT	ADC3_INP6, ADC3_INN2
J5	L7	P4	PF12	I/O	TT	(1)	TRACECLK, SPI5_MISO, SPI1_MISO/I2S1_SDI, TIM5_CH1, LCD_CLK, DCMI_D0/PSSI_D0/DCMIPP_D0, EVENTOUT	-
G6	H2	P2	PF13	I/O	TT	(1)	TRACED0, HDP0, AUDIOCLK, USART6_TX, SPI2_NSS/ I2S2_WS, USART3_CTS/USART3_NSS, TIM3_CH3, LCD_R2, EVENTOUT	-
F5	G7	P3	PF14	I/O	TT	(1)	TRACED1, HDP1, USART6_RX, USART3_RTS/ USART3_DE, TIM3_CH4, LCD_R3, EVENTOUT	-
G5	G5	R2	PF15	I/O	TT	(1)	TRACED2, HDP2, SPI2_RDY, USART6_CTS/ USART6_NSS, SPI2_SCK/I2S2_CK, USART3_CK, TIM2_CH2, TIM3_ETR, LCD_R4, EVENTOUT	-
W4	T5	AF7	PG0	I/O	TT_af	(1)	LPTIM1_IN1, MDF1_SDI2, TIM8_CH3N, ETH2_MII_RXD0/ETH2_RGMII_RXD0/ ETH2_RMII_RXD0, ETH1_MII_RXD2, LCD_G5, DCMI_D4/PSSI_D4/DCMIPP_D4, EVENTOUT	ADC1_INP18, ADC1_INN17
T3	R4	AD4	PG1	I/O	TT_af	(5)	LPTIM1_IN1, I2S3_MCK, SAI2_SD_A, UART5_CTS, USART3_CTS/USART3_NSS, TIM5_CH4, ETH2_MII_RX_ER, ETH2_MII_RXD3, FMC_NBL0, LCD_VSYNC, DCMI_D11/PSSI_D11/DCMIPP_D11, EVENTOUT	WKUP3, ADC1_INP6, ADC1_INN2, ADC2_INP6, ADC2_INN2, TAMP_IN4
T4	M7	AG5	PG2	I/O	TT_af	(1)	RTC_REFIN, I2S3_MCK, SAI2_FS_A, USART3_CK, TIM5_CH3, ETH2_MII_TX_CLK, ETH2_RGMII_CLK125, FMC_CLK, LCD_HSYNC, EVENTOUT	WKUP5, ADC1_INP2, ADC2_INP2

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
U3	H12	AA7	PG3	I/O	TT_a	(5)	LPTIM1_ETR, SPI5_MOSI, SAI2_FS_B, TIM3_CH3, TIM8_ETR, ETH2_CLK, ETH2_PHY_INTN, FMC_A19, LCD_R5, DCMI_PIXCLK/PSSI_PDCK/DCMIPP_PIXCLK, EVENTOUT	WKUP6, ADC1_INP3, ADC2_INP3, ADC3_INP3, TAMP_IN7
V3	N7	AD6	PG4	I/O	TT_a	(1)	SPI5_MISO, SAI3_FS_B, LPTIM4_IN1, TIM8_BKIN, ETH2_PPS_OUT, ETH2_MDC, FMC_A21, LCD_R7, DCMI_VSYNC/PSSI_RDY/DCMIPP_VSYNC, EVENTOUT	PVD_IN, ADC1_INP4, ADC2_INP4
H3	K1	R3	PG5	I/O	TT_f	(1)	TRACED3, HDP3, USART6_RTS/USART6_DE, TIM2_CH3, LCD_R5, DCMI_PIXCLK/PSSI_PDCK/ DCMIPP_PIXCLK, EVENTOUT	-
J3	K2	T3	PG6	I/O	TT_f	(1)	TRACED4, HDP4, SPI5_SCK, SPI1_SCK/I2S1_CK, TIM2_CH4, LCD_R6, DCMI_HSYNC/PSSI_DE/ DCMIPP_HSYNC, EVENTOUT	-
F6	E7	U2	PG7	I/O	TT	(1)	TRACED5, HDP5, SPI5_NSS, SPI1_NSS/I2S1_WS, TIM5_ETR, LCD_R7, DCMI_VSYNC/PSSI_RDY/ DCMIPP_VSYNC, EVENTOUT	-
D4	E5	L5	PG8	I/O	TT	(1)	TRACED6, HDP6, SPI5_RDY, SPI1_RDY, USART6_CK, UART5_RTS/UART5_DE, TIM5_CH3, LCD_G2, DCMI_D2/PSSI_D2/DCMIPP_D2, EVENTOUT	-
E4	G2	M3	PG9	I/O	TT	(1)	TRACED7, UART5_TX, TIM5_CH4, LCD_G3, DCMI_D3/ PSSI_D3/DCMIPP_D3, EVENTOUT	-
E5	F5	M4	PG10	I/O	TT	(1)	TRACED8, HDP0, UART5_RX, TIM8_CH4N, LCD_G4, DCMI_D4/PSSI_D4/DCMIPP_D4, EVENTOUT	-
E6	F7	N2	PG11	I/O	TT	(1)	TRACED9, HDP1, FDCAN1_TX, TIM8_CH4, LCD_G5, DCMI_D5/PSSI_D5/DCMIPP_D5, EVENTOUT	-
G4	H7	N3	PG12	I/O	TT	(1)	TRACED10, HDP2, FDCAN1_RX, TIM8_CH1N, LCD_G6, DCMI_D6/PSSI_D6/DCMIPP_D6, EVENTOUT	-
H5	J7	P1	PG13	I/O	TT_f	(1)	TRACED11, HDP3, TIM8_CH2N, I2C1_SCL, I3C1_SCL, LCD_G7, DCMI_D7/PSSI_D7/DCMIPP_D7, EVENTOUT	-
E3	H5	N1	PG14	I/O	TT	(1)	TRACED12, HDP4, USART1_TX, TIM8_BKIN2, LCD_B1, DCMI_D9/PSSI_D9/DCMIPP_D9, EVENTOUT	-
C6	E4	K6	PG15	I/O	TT	(1)	TRACED13, HDP5, LPTIM1_CH2, USART1_RX, TIM8_ETR, LCD_B2, DCMI_D10/PSSI_D10/ DCMIPP_D10, EVENTOUT	-
R1	R1	AG2	OSC_IN	I	A	(13)	-	OSC_IN

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
R2	R2	AF2	OSC_OUT	I/O	A	(14)	-	OSC_OUT
P13	L14	AC17	PH2	I/O	TT_f	(1)	LPTIM2_CH1, SPDIFRX1_IN3, SAI1_SCK_B, TIM16_CH1, EVENTOUT	-
T12	K14	AE19	PH3	I/O	TT_f	(1)	SPI1_NSS/I2S1_WS, UART7_RX, TIM17_CH1N, TIM5_CH3, I2C7_SCL, EVENTOUT	-
R13	G12	AB16	PH4	I/O	TT	(1)	UART7_TX, TIM17_BKIN, TIM5_CH2, LCD_R0, USB3DR_OVRCUR, USBH_HS_OVRCUR, ETH1_PTP_AUX_TS, EVENTOUT	BOOTFAILN
R14	M9	AG18	PH5	I/O	TT	(1)	SAI2_FS_A, TIM2_CH1, UART7_RX, LCD_G1, USB3DR_VBUSEN, USBH_HS_VBUSEN, ETH2_PTP_AUX_TS, EVENTOUT	WKUP2
R12	L15	AF19	PH6	I/O	TT_f	(1)	LPTIM2_IN2, SAI1_MCLK_B, TIM16_CH1N, I2C1_SMBA, EVENTOUT	-
U10	L12	AE16	PH7	I/O	TT_f	(1)	SPI1_MOSI/I2S1_SDO, UART4_TX, UART7_RTS/ UART7_DE, TIM17_CH1, TIM5_CH4, I2C7_SDA, EVENTOUT	-
U11	M12	AD16	PH8	I/O	TT	(1)	SPI1_MISO/I2S1_SDI, SPDIFRX1_IN3, UART4_RX, UART7_CTS, TIM5_CH1, EVENTOUT	-
T8	W8	AA13	PH9	I/O	TT_a	(1)	SAI3_MCLK_A, USART6_RX, TIM15_CH1N, ETH1_RGMII_CLK125, ETH1_MII_RX_ER, EVENTOUT	ADC3_INP4
W9	U10	AF14	PH10	I/O	TT_a	(1)	SPI1_SCK/I2S1_CK, SAI3_SCK_A, TIM15_CH1, ETH2_MDC, ETH1_MII_TXD2/ETH1_RGMII_TXD2, EVENTOUT	ADC3_INP8, ADC3_INN4
W8	T11	AE14	PH11	I/O	TT_a	(1)	SAI3_FS_A, TIM15_CH2, ETH2_MDIO, ETH1_MII_TXD3/ ETH1_RGMII_TXD3, EVENTOUT	-
V7	V8	AF13	PH12	I/O	TT	(1)	SPI3_NSS/I2S3_WS, TIM10_CH1, ETH1_MII_RXD2/ ETH1_RGMII_RXD2, EVENTOUT	-
W7	U9	AG13	PH13	I/O	TT	(1)	SPI3_SCK/I2S3_CK, TIM15_BKIN, TIM11_CH1, ETH1_MII_RXD3/ETH1_RGMII_RXD3, EVENTOUT	-
D6	H1	L7	PI0	I/O	TT	(1)	TRACED14, HDP6, LPTIM1_IN1, SAI4_MCLK_B, USART1_CK, TIM8_BKIN, LCD_B3, DCMI_D11/ PSSI_D11/DCMIPP_D11, EVENTOUT	-
F4	J9	M6	PI1	I/O	TT_f	(1)	TRACED15, HDP7, TIM8_CH3N, I2C1_SDA, I3C1_SDA, LCD_B4, DCMI_D8/PSSI_D8/DCMIPP_D8, EVENTOUT	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
J6	J5	N5	PI2	I/O	TT	(1)	LPTIM1_ETR, SAI4_SCK_B, USART1_RTS/ USART1_DE, TIM8_CH1, LCD_B5, DCMI_D13/ PSSI_D13/DCMIPP_D13, EVENTOUT	-
H4	H9	N7	PI3	I/O	TT	(1)	LPTIM1_IN2, SAI4_SD_B, USART1_CTS/USART1_NSS, TIM8_CH2, LCD_B6, PSSI_D14/DCMIPP_D14, EVENTOUT	-
H6	G1	P6	PI4	I/O	TT	(1)	LPTIM1_CH1, SAI4_FS_B, TIM8_CH3, LCD_B7, PSSI_D15/DCMIPP_D15, EVENTOUT	-
D5	K7	K4	PI5	I/O	TT	(1)	SPI5_MOSI, SPI1_MOSI/I2S1_SDO, UART5_CTS, TIM5_CH2, LCD_DE, DCMI_D1/PSSI_D1/DCMIPP_D1, EVENTOUT	-
C5	D4	J3	PI6	I/O	TT	(1)	MCO1, USART3_TX, TIM2_ETR, TIM3_CH1, LCD_VSYNC, EVENTOUT	WKUP4
C4	D5	J5	PI7	I/O	TT	(1)	USART3_RX, TIM2_CH1, TIM3_CH2, LCD_HSYNC, EVENTOUT	-
N5	N4	U5	PI8	I/O	TT	(6)	EVENTOUT	RTC_OUT2/ RTC_LSCO, TAMP_IN1/ TAMP_OUT2
J4	K6	U1	PI9	I/O	TT	(1)	SPI2_MOSI/I2S2_SDO, FDCAN2_TX, TIM16_BKIN, SDVSEL2, FMC_NWAIT, DSI_TE, LCD_B0, EVENTOUT	-
C12	B11	D16	PI10	I/O	TT	(1)	SAI1_SCK_A, SPI1_SCK/I2S1_CK, SPDIFRX1_IN0, FDCAN2_RX, MDF1_CCK0, TIM4_CH1, SDVSEL1, FMC_AD12/FMC_D12, DSI_TE, EVENTOUT	-
C16	F12	B27	PI11	I/O	TT	(1)	I2S2_MCK, TIM4_CH3, SDMMC3_D3, FMC_AD15/ FMC_D15, EVENTOUT	-
N2	P2	AB4	PWR_CPU_ON	O	TT	(1)	-	-
-	P1	AF1	PWR_LP	O	TT	(1)	-	-
P3	U3	AD3	PWR_ON	O	TT	(1)	-	-
L5	L5	T4	PZ0	I/O	TT_f	(15)	LPTIM3_IN1, SPI8_MOSI, TIM8_CH1, LPUART1_TX, LPTIM5_OUT, I2C8_SDA, LPTIM3_CH2, I3C4_SDA, EVENTOUT	TAMP_OUT3
M3	M4	U7	PZ1	I/O	TT_f	(15)	LPTIM3_CH1, SPI8_MISO, TIM8_CH2, LPUART1_RX, LPTIM5_ETR, I2C8_SCL, I2C8_SMBA, I3C4_SCL, EVENTOUT	TAMP_OUT5

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
L3	M3	W5	PZ2	I/O	TT_f	(15)	LPTIM3_CH1, SPI8_SCK, LPUART1_RTS/LPUART1_DE, LPTIM4_ETR, I2C8_SCL, I3C4_SCL, EVENTOUT	TAMP_IN3
M5	M5	Y6	PZ3	I/O	TT_f	(15)	DBTRGI, DBTRGO, LPTIM3_ETR, SPI8_NSS, LPUART1_CTS, LPTIM4_IN1, I2C8_SDA, LPTIM4_CH2, I3C4_SDA, EVENTOUT	TAMP_OUT4
L4	L4	V3	PZ4	I/O	TT_f	(15)	DBTRGI, DBTRGO, MCO2, SPI8_RDY, MDF1_CCK1, LPUART1_RX, LPTIM4_CH1, I2C8_SCL, I3C4_SCL, EVENTOUT	TAMP_IN5
M4	N3	R5	PZ5	I/O	TT	(15)	MCO1, LPTIM3_ETR, SPI8_SCK, LPUART1_RTS/ LPUART1_DE, LPTIM5_IN1, LPTIM4_CH2, EVENTOUT	-
K4	K3	V4	PZ6	I/O	TT	(15)	DBTRGI, DBTRGO, SPI8_NSS, TIM8_CH3, LPUART1_CTS, LPTIM5_OUT, LPTIM4_CH2, EVENTOUT	-
L2	L1	V2	PZ7	I/O	TT	(1)	SPI8_MOSI, MDF1_CCK1, LPUART1_TX, LPTIM5_IN1, LPTIM3_CH2, EVENTOUT	-
K3	L3	V1	PZ8	I/O	TT	(1)	LPTIM3_IN1, SPI8_MISO, LPUART1_RX, LPTIM4_CH1, I2C8_SMBA, LPTIM5_ETR, EVENTOUT	-
L1	L2	U3	PZ9	I/O	TT_f	(1)	MCO2, SPI8_RDY, LPUART1_TX, LPTIM4_ETR, I2C8_SDA, LPTIM3_CH2, I3C4_SDA, EVENTOUT	-
V15	V11	AG21	USBH_HS_DM	A	A	-	-	-
V16	V12	AG22	USB3DR_DM	A	A	-	-	-
W15	W11	AF21	USBH_HS_DP	A	A	-	-	-
W16	W12	AF22	USB3DR_DP	A	A	-	-	-
U16	T15	AE20	USBH_HS_TXRT UNE	A	A	-	-	-
T16	R15	AF23	USB3DR_TXRTU NE	A	A	-	-	-
-	T12	AD20	DNU	-	-	-	-	-
T14	W15	AF27	DNU	-	-	-	-	-
W12	V16	AF25	DNU	-	-	-	-	-
V12	U16	AG25	DNU	-	-	-	-	-
W11	V15	AD24	DNU	-	-	-	-	-
V11	U15	AE24	DNU	-	-	-	-	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
T1	U1	AF6	VREF-	A	A	-	-	-
T2	U2	AG6	VREF+	A	A	-	-	-
L6	R6	T6	VBAT	S	-	-	-	-
L8	H8	1L1	VDD	S	-	-	-	-
L10	K8	1L3	VDD	S	-	-	-	-
M9	L6	1L5	VDD	S	-	-	-	-
N8	-	1M2	VDD	S	-	-	-	-
N10	-	1M4	VDD	S	-	-	-	-
N6	N6	AB6	VDDA18ADC	S	-	-	-	-
D3	D3	G7	VDDA18CSI	S	-	-	-	-
J16	D16	F20	VDDA18DDR	S	-	-	-	-
B7	C5	G9	VDDA18DSI	S	-	(2)	-	-
G3	J4	G5	VDDA18LVDS	S	-	(2)	-	-
H15	E15	G19	VDDA18PLL1	S	-	-	-	-
F7	H6	1E1	VDDA18PLL3	S	-	-	-	-
F8	G6	H6	VDDA18PLL2	S	-	-	-	-
T15	R13	AE23	Unused1	-	-	-	-	-
R17	T13	AD22	VDDA18USB	S	-	-	-	-
G8	G10	1C1	VDDCORE	S	-	-	-	-
G10	H11	1C3	VDDCORE	S	-	-	-	-
H7	J10	1C5	VDDCORE	S	-	-	-	-
H9	K11	1D2	VDDCORE	S	-	-	-	-
J8	L10	1D4	VDDCORE	S	-	-	-	-
J10	N8	1E3	VDDCORE	S	-	-	-	-
K7	N10	1E5	VDDCORE	S	-	-	-	-
K9	-	1F2	VDDCORE	S	-	-	-	-
-	-	1F4	VDDCORE	S	-	-	-	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
G12	E13	F18	VDDCPU	S	-	-	-	-
H11	G13	G15	VDDCPU	S	-	-	-	-
H13	J13	G17	VDDCPU	S	-	-	-	-
J12	L13	1C7	VDDCPU	S	-	-	-	-
K13	M13	1C9	VDDCPU	S	-	-	-	-
-	-	1D6	VDDCPU	S	-	-	-	-
-	-	1D8	VDDCPU	S	-	-	-	-
-	-	1D10	VDDCPU	S	-	-	-	-
G14	F16	1C11	VDDQDDR	S	-	-	-	-
J14	J16	1D12	VDDQDDR	S	-	-	-	-
K15	L16	1E11	VDDQDDR	S	-	-	-	-
L14	M16	M22	VDDQDDR	S	-	-	-	-
L16	P16	1F12	VDDQDDR	S	-	-	-	-
M15	T16	N21	VDDQDDR	S	-	-	-	-
N14	-	R21	VDDQDDR	S	-	-	-	-
N16	-	1L11	VDDQDDR	S	-	-	-	-
-	-	1M12	VDDQDDR	S	-	-	-	-
F13	F8	D18	VDDIO2	S	-	-	-	-
-	-	E17	VDDIO2	S	-	-	-	-
K11	M11	1G7	VDDGPU	S	-	(2)	-	-
L12	N14	1G9	VDDGPU	S	-	(2)	-	-
M11	P11	1H6	VDDGPU	S	-	(2)	-	-
M13	P13	1H8	VDDGPU	S	-	(2)	-	-
N12	R10	1H10	VDDGPU	S	-	(2)	-	-
-	-	1L7	VDDGPU	S	-	(2)	-	-
-	-	1L9	VDDGPU	S	-	(2)	-	-
-	-	1M6	VDDGPU	S	-	(2)	-	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
-	-	1M8	VDDGPU	S	-	(2)	-	-
-	-	1M10	VDDGPU	S	-	(2)	-	-
F11	E10	D10	VDDIO3	S	-	-	-	-
F12	F10	E11	VDDIO3	S	-	-	-	-
F9	D6	E9	VDDIO4	S	-	-	-	-
F10	E6	G11	VDDIO4	S	-	-	-	-
F14	D10	D14	VDDIO1	S	-	-	-	-
-	-	E13	VDDIO1	S	-	-	-	-
-	U11	AE22	VDD33UCPD	S	-	-	-	-
B1	B1	E5	VDDCSI	S	-	-	-	-
A7	C6	F8	VDDDSI	S	-	(2)	-	-
F3	J1	F4	VDDLVDS	S	-	(2)	-	-
P15	U12	AC21	Unused2	-	-	-	-	-
U14	T14	AB20	Unused3	-	-	-	-	-
R15	W16	AB22	Unused4	-	-	-	-	-
M6	N5	AB3	VDDA18AON	S	-	-	-	-
R16	R14	AE21	VDD33USB	S	-	-	-	-
A1	A1	A1	VSS	S	-	-	-	-
A19	A19	A2	VSS	S	-	-	-	-
G7	C3	A27	VSS	S	-	-	-	-
G9	C7	AC11	VSS	S	-	-	-	-
G11	D13	AG1	VSS	S	-	-	-	-
G13	E8	AG27	VSS	S	-	-	-	-
G15	E16	C6	VSS	S	-	-	-	-
H8	F6	C10	VSS	S	-	-	-	-
H10	F11	E7	VSS	S	-	-	-	-
H12	F13	F3	VSS	S	-	-	-	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
H14	G8	F12	VSS	S	-	-	-	-
H16	G11	F14	VSS	S	-	-	-	-
J7	H10	F16	VSS	S	-	-	-	-
J9	H13	1A1	VSS	S	-	-	-	-
J11	H16	1A3	VSS	S	-	-	-	-
J13	J6	1A5	VSS	S	-	-	-	-
J15	J8	1A7	VSS	S	-	-	-	-
K8	J11	1A9	VSS	S	-	-	-	-
K10	J14	1A11	VSS	S	-	-	-	-
K12	K4	J7	VSS	S	-	-	-	-
K14	K5	1B2	VSS	S	-	-	-	-
K16	K10	1B4	VSS	S	-	-	-	-
L7	K13	1B6	VSS	S	-	-	-	-
L9	K16	1B8	VSS	S	-	-	-	-
L11	L8	1B10	VSS	S	-	-	-	-
L13	L11	1B12	VSS	S	-	-	-	-
L15	M10	K3	VSS	S	-	-	-	-
M8	N11	1E7	VSS	S	-	-	-	-
M10	N13	1E9	VSS	S	-	-	-	-
M12	N16	1F6	VSS	S	-	-	-	-
M14	P8	1F8	VSS	S	-	-	-	-
M16	P10	1F10	VSS	S	-	-	-	-
N9	P14	1G1	VSS	S	-	-	-	-
N11	R11	1G3	VSS	S	-	-	-	-
N13	R16	1G5	VSS	S	-	-	-	-
N15	R18	1G11	VSS	S	-	-	-	-
W1	W1	1H2	VSS	S	-	-	-	-
W19	W19	1H4	VSS	S	-	-	-	-

Pin Number			Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
TFBGA361	VFBGA361	VFBGA424						
-	-	1H12	VSS	S	-	-	-	-
-	-	1J1	VSS	S	-	-	-	-
-	-	1J3	VSS	S	-	-	-	-
-	-	1J5	VSS	S	-	-	-	-
-	-	1J7	VSS	S	-	-	-	-
-	-	1J9	VSS	S	-	-	-	-
-	-	1J11	VSS	S	-	-	-	-
-	-	1K2	VSS	S	-	-	-	-
-	-	1K4	VSS	S	-	-	-	-
-	-	1K6	VSS	S	-	-	-	-
-	-	1K8	VSS	S	-	-	-	-
-	-	1K10	VSS	S	-	-	-	-
-	-	1K12	VSS	S	-	-	-	-
-	-	V6	VSS	S	-	-	-	-
-	-	Y4	VSS	S	-	-	-	-
N7	P6	AC5	VSSA	S	-	-	-	-
M7	M6	AC3	VSSAON	S	-	-	-	-
K6	M8	R7	V08CAP	A	-	-	-	-

1. *Power supply is V_{DD}.*
2. *Pin is DNU in some part numbers.*
3. *Power supply is V_{DD} - used in open drain with external pull up.*
4. *Power supply is V_{DDIO4}.*
5. *Power supply is V_{DD} or V_{SW} - input only in V_{SW}.*
6. *Power supply is V_{SW}.*
7. *Power supply is V_{SW} - OSC32_IN pin is also used as digital input in LSE bypass mode and tied to GPIO PC14 input (for test purpose only).*
8. *Power supply is V_{SW} - OSC32_OUT pin is also tied to GPIO PC15 input (for test purpose only).*
9. *Power supply is $V_{DDA18AON}$ - Must be always connected at board level to $V_{DDA18AON}$.*
10. *Power supply is V_{DDIO3}.*
11. *Power supply is V_{DDIO1}.*

12. *Power supply is V_{DDIO2}.*
13. *Power supply is $V_{DDA18AON}$ - OSC_IN pin is also used as digital input in HSE bypass mode and tied to GPIO PH0 input (for test purpose only).*
14. *Power supply is $V_{DDA18AON}$ - OSC_OUT pin is also tied to GPIO PH1 input, used by BOOTROM to auto-detect HSE bypass mode.*
15. *Power supply is V_{DD} or V_{SW}.*

4.3 Alternate functions

Table 12. Alternate functions AF0 to AF7

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5 / SYS	LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/8 / UART4 / USART6	FDCAN2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	DSI / MDF1 / SAI2/4 / UART5 / USART1/6	LPUART1 / TIM14/17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port A	PA0	-	LPTIM1_CH2	SPI5_RDY	-	SAI2_MCLK_B	UART5_TX	USART3_TX	TIM3_ETR
	PA1	-	-	-	-	SAI3_SD_A	USART1_RTS/ USART1_DE	USART6_CK	TIM4_CH2
	PA2	-	LPTIM2_IN1	-	-	-	-	USART1_RX	-
	PA3	-	LPTIM2_ETR	-	-	-	-	USART1_TX	-
	PA4	-	-	-	-	-	-	USART2_TX	FDCAN2_TX
	PA5	-	-	-	SPI4_MOSI	SAI2_MCLK_B	SAI2_SD_B	USART2_RTS/USART2_DE	FDCAN2_RX
	PA6	-	-	-	SPI4_SCK	SAI2_FS_B	-	USART2_CK	TIM13_CH1
	PA7	-	-	AUDIOCLK	-	-	MDF1_CCK0	USART1_CTS/USART1_NSS	TIM4_ETR
	PA8	-	LPTIM2_CH2	-	-	SAI1_FS_B	-	USART1_CK	-
	PA9	-	-	-	SPI4_NSS	SAI2_SCK_B	-	USART2_CTS/USART2_NSS	LPTIM5_ETR
	PA10	-	-	-	SPI4_MISO	SAI2_SD_B	-	USART2_RX	LPTIM5_IN1
	PA11	-	SPI8_SCK	LPTIM2_CH1	-	SAI4_SD_B	-	-	-
	PA12	-	-	-	-	SAI3_FS_A	-	-	TIM4_CH1
	PA13	-	SPI8_RDY	I2S3_MCK	LPTIM2_ETR	-	MDF1_CKI3	USART2_CTS/USART2_NSS	-
	PA14	-	SPI8_NSS	LPTIM2_CH2	-	SAI4_FS_B	MDF1_CCK1	-	-
	PA15	-	-	SPI3_MISO/ I2S3_SDI	-	-	-	USART2_RX	-
Port B	PB0	-	-	SPI2_SCK/I2S2_CK	-	-	-	USART1_CK	TIM16_CH1
	PB1	-	SPI3_NSS/I2S3_WS	-	-	-	-	-	TIM16_CH1N
	PB2	-	-	SPI2_MOSI/ I2S2_SDO	-	-	MDF1_CKI3	TIM17_BKIN	TIM16_BKIN
	PB3	-	-	SPI2_NSS/I2S2_WS	-	-	MDF1_SDI3	-	-
	PB4	-	-	SPI2_RDY	UART4_CTS	SAI4_FS_B	-	TIM14_CH1	-
	PB5	-	-	I2S2_MCK	UART4_RTS/UART4_DE	SAI4_SD_B	-	-	-
	PB6	-	-	SPI2_MISO/ I2S2_SDI	UART4_RX	SAI4_SCK_B	-	-	-

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5 / SYS	LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/8 / UART4 / USART6	FDCAN2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	DSI / MDF1 / SAI2/4 / UART5 / USART1/6	LPUART1 / TIM14/17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port B	PB7	-	SPI3_SCK/I2S3_CK	-	UART4_TX	SAI4_MCLK_B	-	-	-
	PB8	-	SPI3_MOSI/ I2S3_SDO	-	-	-	-	USART1_TX	TIM17_CH1
	PB9	-	SPI3_RDY	-	-	-	-	USART1_RTS/USART1_DE	FDCAN1_TX
	PB10	-	SPI3_MISO/ I2S3_SDI	-	-	-	-	USART1_RX	TIM17_CH1N
	PB11	-	I2S3_MCK	-	-	-	-	USART1_CTS/USART1_NSS	FDCAN1_RX
	PB12	-	-	-	-	-	-	-	TIM13_CH1
	PB13	-	-	-	-	SAI1_SD_B	-	-	-
	PB14	-	-	SPI2_SCK/I2S2_CK	-	-	-	-	-
	PB15	-	LPTIM1_IN2	SPI5_SCK	-	SAI2_SD_B	UART5_RX	-	TIM3_CH2
Port C	PC0	-	LPTIM1_CH1	-	-	SAI3_MCLK_B	USART6_TX	-	-
	PC1	-	-	SPI3_MOSI/ I2S3_SDO	-	-	-	USART2_TX	-
	PC2	-	SPI8_MOSI	LPTIM2_IN1	-	SAI4_MCLK_B	MDF1_SDI3	USART2_RTS/USART2_DE	-
	PC3	-	LPTIM1_IN2	SPI3_NSS/I2S3_WS	-	-	-	USART6_RTS/USART6_DE	FDCAN2_TX
	PC4	-	-	-	-	SAI3_FS_B	-	-	-
	PC5	-	-	SPDIFRX1_IN1	-	-	MDF1_SDI1	-	-
	PC6	-	RTC_REFIN	SPDIFRX1_IN0	-	-	MDF1_CKI1	-	-
	PC7	-	-	-	-	SAI3_SD_B	-	-	-
	PC8	-	LPTIM1_ETR	-	-	SAI3_SCK_B	-	USART6_CTS/USART6_NSS	-
	PC9	-	MCO1	SPI3_MISO/ I2S3_SDI	-	SAI2_SCK_A	-	-	TIM13_CH1
	PC10	-	-	SPI3_MOSI/ I2S3_SDO	-	-	-	-	LPTIM4_ETR
	PC11	-	LPTIM1_CH1	SPI5_NSS	-	SAI2_MCLK_A	UART5_RTS/UART5_DE	USART3_RTS/USART3_DE	TIM3_CH1
	PC12	-	LPTIM1_CH2	-	-	-	MDF1_CKI2	-	-
	PC13	-	-	-	-	-	-	-	-
Port D	PD0	TRACECLK	HDP0	-	SAI1_D2	-	SAI4_FS_A	UART7_RX	TIM15_CH2
	PD1	-	HDP1	SPI1_MISO/ I2S1_SDI	SAI1_CK2	-	SAI4_SD_A	UART7_RTS/UART7_DE	TIM15_CH1
	PD2	-	HDP2	SPI1_NSS/I2S1_WS	SAI1_CK1	-	SAI4_SCK_A	UART7_CTS	TIM15_BKIN
	PD3	-	SAI1_MCLK_A	SPI2_SCK/I2S2_CK	SAI1_D1	-	SAI4_MCLK_A	UART7_TX	TIM15_CH1N
	PD4	TRACED0	SPI4_MISO	HDP3	SAI1_D3	SAI1_SD_B	-	-	-
	PD5	TRACED1	SPI4_NSS	HDP4	SAI1_D4	SAI1_FS_B	-	-	-
	PD6	TRACED2	SPI4_MOSI	HDP5	-	SAI1_SCK_B	MDF1_SDI2	-	-
	PD7	TRACED3	SPI4_SCK	SPI1_RDY	-	SAI1_MCLK_B	MDF1_CKI2	-	-

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5 / SYS	LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/8 / UART4 / USART6	FDCAN2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	DSI / MDF1 / SAI2/4 / UART5 / USART1/6	LPUART1 / TIM14/17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port D	PD8	TRACED4	SPI4_RDY	I2S1_MCK	SAI1_FS_A	UART4_CTS	MDF1_SDI1	-	-
	PD9	TRACED5	HDP6	SPI1_MOSI/ I2S1_SDO	SAI1_SD_A	UART4_RTS/UART4_DE	MDF1_CKI1	-	-
	PD10	TRACED6	HDP7	-	SAI1_SCK_A	UART4_RX	MDF1_SDI0	-	-
	PD11	TRACED7	-	SPI1_SCK/I2S1_CK	SAI1_MCLK_A	UART4_TX	MDF1_CKI0	-	-
	PD12	-	-	SPI2_MISO/ I2S2_SDI	SPDIFRX1_IN2	-	-	-	-
	PD13	-	-	SPI2_NSS/I2S2_WS	-	-	-	-	-
	PD14	-	-	I2S1_MCK	-	-	-	-	FDCAN1_RX
	PD15	-	SPI1_RDY	-	-	-	DSI_TE	-	FDCAN1_TX
Port E	PE0	TRACED2	LPTIM2_CH1	SPI1_SCK/I2S1_CK	SPI3_RDY	-	-	USART3_CK	-
	PE1	TRACED3	LPTIM2_CH2	I2S1_MCK	I2S3_MCK	-	-	USART3_RX	-
	PE2	-	LPTIM2_ETR	SPI1_MISO/ I2S1_SDI	SPI3_MOSI/I2S3_SDO	SAI1_SCK_B	-	-	-
	PE3	TRACECLK	-	SPI1_RDY	SPI3_SCK/I2S3_CK	SAI1_MCLK_B	-	USART3_TX	-
	PE4	TRACED0	LPTIM2_IN1	SPI1_MOSI/ I2S1_SDO	SPI3_MISO/I2S3_SDI	SAI1_SD_B	-	USART3_CTS/USART3_NSS	FDCAN1_TX
	PE5	TRACED1	LPTIM2_IN2	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	SAI1_FS_B	-	USART3_RTS/USART3_DE	FDCAN1_RX
	PE6	-	SPI4_RDY	-	-	SPDIFRX1_IN2	-	USART1_TX	-
	PE7	-	-	-	SAI4_D4	SPDIFRX1_IN3	-	USART1_RX	-
	PE8	-	SPI4_MOSI	-	SAI4_CK1	SAI4_MCLK_A	MDF1_CKI0	-	-
	PE9	-	SPI4_MISO	-	SAI4_D2	SAI4_FS_A	-	USART1_CK	-
	PE10	-	SPI4_SCK	-	SAI4_D1	SAI4_SD_A	-	USART1_CTS/USART1_NSS	-
	PE11	-	-	-	SAI4_D3	SAI1_FS_A	-	-	TIM15_CH2
	PE12	-	SPI4_NSS	-	SAI4_CK2	SAI4_SCK_A	MDF1_SDI0	USART1_RTS/USART1_DE	-
	PE13	-	-	-	-	SAI1_SD_A	-	-	TIM15_CH1
	PE14	-	-	-	-	SAI1_MCLK_A	-	-	TIM15_BKIN
	PE15	-	-	-	-	SAI1_SCK_A	-	-	TIM15_CH1N
Port F	PF0	-	-	SPI3_SCK/I2S3_CK	-	-	-	-	FDCAN2_RX
	PF1	-	SPI8_MISO	LPTIM2_IN2	-	SAI4_SCK_B	-	USART2_CK	-
	PF2	-	-	SPI3_RDY	-	-	-	-	-
	PF3	-	-	-	-	SAI2_SCK_B	MDF1_CCK0	-	TIM3_CH4
	PF4	-	RTC_OUT2	-	-	SAI3_SCK_A	-	USART6_RX	TIM4_CH4
	PF5	-	-	-	-	SAI3_MCLK_A	-	USART6_TX	TIM4_CH3
	PF6	-	RTC_OUT2	-	SAI3_MCLK_B	-	-	USART6_CK	TIM12_CH1
	PF7	-	-	SPDIFRX1_IN1	-	SAI3_SD_A	-	-	TIM2_ETR

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5 / SYS	LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/8 / UART4 / USART6	FDCAN2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	DSI / MDF1 / SAI2/4 / UART5 / USART1/6	LPUART1 / TIM14/17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port F	PF8	-	RTC_REFIN	-	SAI3_SCK_B	-	-	USART3_RX	TIM12_CH2
	PF9	-	-	-	SAI3_SD_B	SAI2_SD_A	-	-	TIM2_CH2
	PF10	-	MCO2	SPI3_RDY	-	SAI2_MCLK_A	-	-	TIM2_CH3
	PF11	-	MCO1	SPDIFRX1_IN0	-	SAI2_SCK_A	-	-	TIM2_CH4
	PF12	TRACECLK	-	SPI5_MISO	SPI1_MISO/I2S1_SDI	-	-	-	-
	PF13	TRACED0	HDP0	AUDIOCLK	USART6_TX	SPI2_NSS/I2S2_WS	-	USART3_CTS/USART3_NSS	-
	PF14	TRACED1	HDP1	-	USART6_RX	-	-	USART3_RTS/USART3_DE	-
	PF15	TRACED2	HDP2	SPI2_RDY	USART6_CTS/ USART6_NSS	SPI2_SCK/I2S2_CK	-	USART3_CK	TIM2_CH2
Port G	PG0	-	LPTIM1_IN1	-	-	-	MDF1_SDI2	-	-
	PG1	-	LPTIM1_IN1	I2S3_MCK	-	SAI2_SD_A	UART5_CTS	USART3_CTS/USART3_NSS	-
	PG2	-	RTC_REFIN	I2S3_MCK	-	SAI2_FS_A	-	USART3_CK	-
	PG3	-	LPTIM1_ETR	SPI5_MOSI	-	SAI2_FS_B	-	-	TIM3_CH3
	PG4	-	-	SPI5_MISO	SAI3_FS_B	-	-	-	LPTIM4_IN1
	PG5	TRACED3	HDP3	-	USART6_RTS/ USART6_DE	-	-	-	TIM2_CH3
	PG6	TRACED4	HDP4	SPI5_SCK	SPI1_SCK/I2S1_CK	-	-	-	TIM2_CH4
	PG7	TRACED5	HDP5	SPI5_NSS	SPI1_NSS/I2S1_WS	-	-	-	-
	PG8	TRACED6	HDP6	SPI5_RDY	SPI1_RDY	USART6_CK	UART5_RTS/UART5_DE	-	-
	PG9	TRACED7	-	-	-	-	UART5_TX	-	-
	PG10	TRACED8	HDP0	-	-	-	UART5_RX	-	-
	PG11	TRACED9	HDP1	-	-	-	-	-	FDCAN1_TX
	PG12	TRACED10	HDP2	-	-	-	-	-	FDCAN1_RX
	PG13	TRACED11	HDP3	-	-	-	-	-	-
	PG14	TRACED12	HDP4	-	-	-	-	USART1_TX	-
	PG15	TRACED13	HDP5	-	LPTIM1_CH2	-	-	USART1_RX	-
Port H	PH2	-	LPTIM2_CH1	-	SPDIFRX1_IN3	SAI1_SCK_B	-	-	TIM16_CH1
	PH3	-	-	SPI1_NSS/I2S1_WS	-	-	-	UART7_RX	TIM17_CH1N
	PH4	-	-	-	-	-	-	UART7_TX	TIM17_BKIN
	PH5	-	-	-	-	SAI2_FS_A	-	-	TIM2_CH1
	PH6	-	LPTIM2_IN2	-	-	SAI1_MCLK_B	-	-	TIM16_CH1N
	PH7	-	-	SPI1_MOSI/ I2S1_SDO	-	UART4_TX	-	UART7_RTS/UART7_DE	TIM17_CH1
	PH8	-	-	SPI1_MISO/ I2S1_SDI	SPDIFRX1_IN3	UART4_RX	-	UART7_CTS	-
	PH9	-	-	-	-	SAI3_MCLK_A	-	USART6_RX	TIM15_CH1N

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/8 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/5 / SYS	LPTIM1/2 / SAI1/2/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/8 / UART4 / USART6	FDCAN2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	DSI / MDF1 / SAI2/4 / UART5 / USART1/6	LPUART1 / TIM14/17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port H	PH10	-	-	SPI1_SCK/I2S1_CK	-	SAI3_SCK_A	-	-	TIM15_CH1
	PH11	-	-	-	-	SAI3_FS_A	-	-	TIM15_CH2
	PH12	-	-	SPI3_NSS/I2S3_WS	-	-	-	-	-
	PH13	-	-	SPI3_SCK/I2S3_CK	-	-	-	-	TIM15_BKIN
Port I	PI0	TRACED14	HDP6	-	LPTIM1_IN1	SAI4_MCLK_B	-	USART1_CK	-
	PI1	TRACED15	HDP7	-	-	-	-	-	-
	PI2	-	-	-	LPTIM1_ETR	SAI4_SCK_B	-	USART1_RTS/USART1_DE	-
	PI3	-	-	-	LPTIM1_IN2	SAI4_SD_B	-	USART1_CTS/USART1_NSS	-
	PI4	-	-	-	LPTIM1_CH1	SAI4_FS_B	-	-	-
	PI5	-	-	SPI5_MOSI	SPI1_MOSI/I2S1_SDO	-	UART5_CTS	-	-
	PI6	-	MCO1	-	-	-	-	USART3_TX	TIM2_ETR
	PI7	-	-	-	-	-	-	USART3_RX	TIM2_CH1
	PI8	-	-	-	-	-	-	-	-
	PI9	-	-	SPI2_MOSI/ I2S2_SDO	-	FDCAN2_TX	-	-	-
	PI10	-	SAI1_SCK_A	SPI1_SCK/I2S1_CK	SPDIFRX1_IN0	FDCAN2_RX	MDF1_CCK0	-	-
	PI11	-	-	I2S2_MCK	-	-	-	-	-
Port Z	PZ0	-	-	LPTIM3_IN1	SPI8_MOSI	TIM8_CH1	-	LPUART1_TX	LPTIM5_OUT
	PZ1	-	-	LPTIM3_CH1	SPI8_MISO	TIM8_CH2	-	LPUART1_RX	LPTIM5_ETR
	PZ2	-	-	LPTIM3_CH1	SPI8_SCK	-	-	LPUART1_RTS/LPUART1_DE	LPTIM4_ETR
	PZ3	DBTRGI	DBTRGO	LPTIM3_ETR	SPI8_NSS	-	-	LPUART1_CTS	LPTIM4_IN1
	PZ4	DBTRGI	DBTRGO	MCO2	SPI8_RDY	MDF1_CCK1	-	LPUART1_RX	LPTIM4_CH1
	PZ5	-	MCO1	LPTIM3_ETR	SPI8_SCK	-	-	LPUART1_RTS/LPUART1_DE	LPTIM5_IN1
	PZ6	DBTRGI	DBTRGO	-	SPI8_NSS	TIM8_CH3	-	LPUART1_CTS	LPTIM5_OUT
	PZ7	-	-	-	SPI8_MOSI	MDF1_CCK1	-	LPUART1_TX	LPTIM5_IN1
	PZ8	-	-	LPTIM3_IN1	SPI8_MISO	-	-	LPUART1_RX	LPTIM4_CH1
	PZ9	-	MCO2	-	SPI8_RDY	-	-	LPUART1_TX	LPTIM4_ETR

Table 13. Alternate functions AF8 to AF15

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/8 / I3C1 / TIM1/2/3/4/5/8/10 /11/12/16 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I2C1/2/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I3C4 / LCD / OCTOSPIM_P 1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / FMC / LCD / SDMMC3	SYS
Port A	PA0	TIM5_CH2	-	ETH2_MII_RXD2	-	FMC_NL	-	DCMI_D9/PSSI_D9/ DCMIPP_D9	EVENT OUT
	PA1	-	-	-	LCD_R3	-	DCMI_D5/PSSI_D5/ DCMIPP_D5	-	EVENT OUT
	PA2	I3C1_SDA	-	I2C1_SDA	LCD_B0	-	DCMI_D3/PSSI_D3/ DCMIPP_D3	-	EVENT OUT
	PA3	I3C1_SCL	I2C7_SMBA	I2C1_SCL	LCD_B1	-	DCMI_D2/PSSI_D2/ DCMIPP_D2	-	EVENT OUT
	PA4	TIM2_CH1	-	LCD_R1	-	-	ETH1_PTP_AUX_TS	-	EVENT OUT
	PA5	TIM2_CH4	-	LCD_G0	-	FMC_A0	DCMI_D13/PSSI_D13/ DCMIPP_D13	-	EVENT OUT
	PA6	TIM2_ETR	-	LCD_G4	-	FMC_NE1	DCMI_D12/PSSI_D12/ DCMIPP_D12	-	EVENT OUT
	PA7	I2C2_SMBA	-	LCD_B5	-	-	DCMI_D6/PSSI_D6/ DCMIPP_D6	-	EVENT OUT
	PA8	USART2_RX	-	-	-	LCD_B2	DCMI_D4/PSSI_D4/ DCMIPP_D4	-	EVENT OUT
	PA9	TIM2_CH3	-	ETH1_MDC	-	LCD_G7	PSSI_D14/DCMIPP_D14	-	EVENT OUT
	PA10	TIM2_CH2	-	ETH1_MDIO	-	LCD_R6	PSSI_D15/DCMIPP_D15	-	EVENT OUT
	PA11	-	-	ETH1_MII_RX_DV/ETH1_RGMII_RX_CTL/ ETH1_RMII_CRS_DV	-	-	-	-	EVENT OUT
	PA12	-	-	ETH1_PHY_INTN	-	-	-	-	EVENT OUT
	PA13	-	I2C7_SMBA	ETH1_MII_TX_EN/ETH1_RGMII_TX_CTL/ ETH1_RMII_TX_EN	-	-	-	-	EVENT OUT
	PA14	-	-	ETH1_MII_RX_CLK/ETH1_RGMII_RX_CLK/ ETH1_RMII_REF_CLK	-	-	-	-	EVENT OUT
	PA15	-	I2C7_SDA	ETH1_MII_TXD0/ETH1_RGMII_TXD0/ ETH1_RMII_TXD0	-	-	-	-	EVENT OUT
Port B	PB0	-	-	OCTOSPIM_P2_IO0	-	-	-	-	EVENT OUT
	PB1	-	-	OCTOSPIM_P2_IO1	-	FMC_NCE4	-	-	EVENT OUT
	PB2	-	-	OCTOSPIM_P2_IO2	-	-	-	-	EVENT OUT
	PB3	-	-	OCTOSPIM_P2_IO3	-	FMC_NCE3	-	-	EVENT OUT
	PB4	-	I2C2_SDA	OCTOSPIM_P2_IO4	-	-	I3C2_SDA	-	EVENT OUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/8 / I3C1 / TIM1/2/3/4/5/8/10 /11/12/16 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I2C1/2/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I3C4 / LCD / OCTOSPIM_P 1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / FMC / LCD / SDMMC3	SYS
Port B	PB5	-	I2C2_SCL	OCTOSPIM_P2_IO5	-	FMC_AD8/FMC_D8	I3C2_SCL	SDMMC3_D123DIR	EVENT OUT
	PB6	-	-	OCTOSPIM_P2_IO6	-	FMC_AD9/FMC_D9	-	SDMMC3_D0DIR	EVENT OUT
	PB7	-	TIM12_CH1	OCTOSPIM_P2_IO7	-	FMC_AD10/FMC_D10	-	SDMMC3_CDIR	EVENT OUT
	PB8	-	-	OCTOSPIM_P2_NCS1	-	FMC_AD12/FMC_D12	-	-	EVENT OUT
	PB9	-	TIM10_CH1	OCTOSPIM_P2_DQS	OCTOSPIM_P 2_NCS2	FMC_AD13/FMC_D13	-	-	EVENT OUT
	PB10	-	-	OCTOSPIM_P2_CLK	-	FMC_AD15/FMC_D15	-	-	EVENT OUT
	PB11	-	TIM12_CH2	OCTOSPIM_P2_NCLK	OCTOSPIM_P 2_NCS2	FMC_AD14/FMC_D14	OCTOSPIM_P1_NCS2	-	EVENT OUT
	PB12	-	DSI_TE	SDMMC3_D2	FMC_NWAIT	-	-	DCMI_D12/PSSI_D12/ DCMIPP_D12	EVENT OUT
	PB13	-	-	SDMMC3_CK	FMC_AD5/ FMC_D5	FMC_AD0/FMC_D0	-	-	EVENT OUT
	PB14	-	TIM4_CH2	SDMMC3_D0	FMC_AD7/ FMC_D7	FMC_AD2/FMC_D2	-	-	EVENT OUT
	PB15	TIM5_CH1	-	ETH1_PPS_OUT	-	FMC_A18	LCD_R4	DCMI_D8/PSSI_D8/ DCMIPP_D8	EVENT OUT
Port C	PC0	-	DCMI_D0/PSSI_D0/ DCMIPP_D0	ETH2_MII_RX_CLK/ETH2_RMII_REF_CLK	ETH1_MII_TX _CLK	ETH1_RGMII_GTX_CLK	LCD_G7	-	EVENT OUT
	PC1	-	I2C7_SCL	ETH1_MII_TXD1/ETH1_RGMII_TXD1/ ETH1_RMII_TXD1	-	-	-	-	EVENT OUT
	PC2	-	-	ETH1_MII_RXD1/ETH1_RGMII_RXD1/ ETH1_RMII_RXD1	-	-	-	-	EVENT OUT
	PC3	-	-	ETH2_MII_RX_DV/ETH2_RGMII_RX_CTL/ ETH2_RMII_CRS_DV	ETH1_MII_RX _ER	-	LCD_G6	DCMI_D3/PSSI_D3/ DCMIPP_D3	EVENT OUT
	PC4	-	-	ETH2_MII_TX_EN/ETH2_RGMII_TX_CTL/ ETH2_RMII_TX_EN	-	ETH1_RGMII_CLK125	LCD_R0	-	EVENT OUT
	PC5	TIM8_CH1N	-	ETH2_MDIO	ETH1_MII_CO L	FMC_A25	ETH1_PPS_OUT	LCD_DE	EVENT OUT
	PC6	TIM8_CH1	-	ETH2_MDC	ETH1_MII_CR S	FMC_A24	ETH1_PHY_INTN	LCD_CLK	EVENT OUT
	PC7	TIM8_CH2N	-	ETH2_MII_TXD0/ETH2_RGMII_TXD0/ ETH2_RMII_TXD0	ETH1_MII_TX D2	-	LCD_B4	DCMI_D1/PSSI_D1/ DCMIPP_D1	EVENT OUT
	PC8	TIM8_CH2	-	ETH2_MII_TXD1/ETH2_RGMII_TXD1/ ETH2_RMII_TXD1	ETH1_MII_TX D3	-	LCD_B3	DCMI_D2/PSSI_D2/ DCMIPP_D2	EVENT OUT
	PC9	TIM8_CH4N	USBH_HS_OVRCUR	ETH2_MII_TXD2/ETH2_RGMII_TXD2	USB3DR_OVR CUR	FMC_A22	LCD_G2	DCMI_D7/PSSI_D7/ DCMIPP_D7	EVENT OUT
	PC10	TIM8_CH4	USBH_HS_VBUSEN	ETH2_MII_TXD3/ETH2_RGMII_TXD3	USB3DR_VBU SEN	FMC_A23	LCD_G3	DCMI_D6/PSSI_D6/ DCMIPP_D6	EVENT OUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/8 / I3C1 / TIM1/2/3/4/5/8/10 /11/12/16 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I2C1/2/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I3C4 / LCD / OCTOSPIM_P 1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / FMC / LCD / SDMMC3	SYS
Port C	PC11	TIM5_ETR	-	ETH2_MII_RXD3/ETH2_RGMII_RXD3	-	FMC_NBL1	LCD_R2	DCMI_D10/PSSI_D10/ DCMIPP_D10	EVENT OUT
	PC12	TIM8_CH3	-	ETH2_MII_RXD1/ETH2_RGMII_RXD1/ ETH2_RMII_RXD1	ETH1_MII_RX D3	-	LCD_G1	DCMI_D5/PSSI_D5/ DCMIPP_D5	EVENT OUT
	PC13	-	-	-	-	-	-	-	EVENT OUT
Port D	PD0	-	SDVSEL1	OCTOSPIM_P1_CLK	-	-	DCMI_PIXCLK/PSSI_PDCK/ DCMIPP_PIXCLK	-	EVENT OUT
	PD1	TIM1_BKIN	-	OCTOSPIM_P1_NCLK	OCTOSPIM_P 1_NCS2	OCTOSPIM_P2_NCS2	DCMI_HSYNC/PSSI_DE/ DCMIPP_HSYNC	-	EVENT OUT
	PD2	TIM1_ETR	-	OCTOSPIM_P1_DQS	OCTOSPIM_P 1_NCS2	-	DCMI_VSYNC/PSSI_RDY/ DCMIPP_VSYNC	-	EVENT OUT
	PD3	TIM1_BKIN2	SDVSEL2	OCTOSPIM_P1_NCS1	-	-	PSSI_D15/DCMIPP_D15	-	EVENT OUT
	PD4	TIM1_CH4N	TIM4_CH1	OCTOSPIM_P1_IO0	-	-	PSSI_D14/DCMIPP_D14	-	EVENT OUT
	PD5	TIM1_CH3N	TIM4_CH2	OCTOSPIM_P1_IO1	-	-	DCMI_D13/PSSI_D13/ DCMIPP_D13	-	EVENT OUT
	PD6	TIM1_CH2N	TIM4_CH3	OCTOSPIM_P1_IO2	-	-	DCMI_D12/PSSI_D12/ DCMIPP_D12	-	EVENT OUT
	PD7	TIM1_CH1N	TIM4_CH4	OCTOSPIM_P1_IO3	-	-	DCMI_D11/PSSI_D11/ DCMIPP_D11	-	EVENT OUT
	PD8	TIM1_CH4	TIM4_ETR	OCTOSPIM_P1_IO4	SDMMC1_D7	SDMMC1_D123DIR	DCMI_D10/PSSI_D10/ DCMIPP_D10	-	EVENT OUT
	PD9	TIM1_CH3	-	OCTOSPIM_P1_IO5	SDMMC1_D6	SDMMC1_D0DIR	DCMI_D9/PSSI_D9/ DCMIPP_D9	-	EVENT OUT
	PD10	TIM1_CH2	TIM14_CH1	OCTOSPIM_P1_IO6	SDMMC1_D5	SDMMC1_CDIR	DCMI_D8/PSSI_D8/ DCMIPP_D8	-	EVENT OUT
	PD11	TIM1_CH1	SDVSEL1	OCTOSPIM_P1_IO7	SDMMC1_D4	SDMMC1_CKIN	DCMI_D7/PSSI_D7/ DCMIPP_D7	-	EVENT OUT
	PD12	-	TIM4_ETR	SDMMC3_CMD	FMC_AD6/ FMC_D6	FMC_AD1/FMC_D1	-	-	EVENT OUT
	PD13	-	TIM4_CH4	SDMMC3_D1	FMC_AD11/ FMC_D11	FMC_NWE	-	-	EVENT OUT
	PD14	TIM11_CH1	-	I2C7_SDA	FMC_AD4/ FMC_D4	SDMMC3_D3	DCMI_D1/PSSI_D1/ DCMIPP_D1	-	EVENT OUT
	PD15	TIM1_BKIN2	TIM5_ETR	I2C7_SCL	FMC_AD3/ FMC_D3	SDMMC3_CKIN	DCMI_D0/PSSI_D0/ DCMIPP_D0	-	EVENT OUT
Port E	PE0	-	-	SDMMC1_D2	-	-	-	-	EVENT OUT
	PE1	-	-	SDMMC1_D3	-	-	-	-	EVENT OUT
	PE2	TIM10_CH1	-	SDMMC1_CMD	-	-	-	-	EVENT OUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/8 / I3C1 / TIM1/2/3/4/5/8/10 /11/12/16 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I2C1/2/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I3C4 / LCD / OCTOSPIM_P 1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / FMC / LCD / SDMMC3	SYS
Port E	PE3	TIM11_CH1	-	SDMMC1_CK	-	-	-	-	EVENT OUT
	PE4	-	-	SDMMC1_D0	-	-	-	-	EVENT OUT
	PE5	-	-	SDMMC1_D1	-	-	-	-	EVENT OUT
	PE6	TIM1_ETR	-	-	FMC_AD1/ FMC_D1	SDMMC2_D6	SDMMC2_D0DIR	-	EVENT OUT
	PE7	TIM1_CH4N	-	TIM14_CH1	FMC_AD2/ FMC_D2	SDMMC2_D7	SDMMC2_D123DIR	-	EVENT OUT
	PE8	TIM1_CH1	-	-	FMC_A17/ FMC_ALE	SDMMC2_D2	-	-	EVENT OUT
	PE9	TIM1_CH4	-	-	FMC_AD0/ FMC_D0	SDMMC2_D5	SDMMC2_CDIR	-	EVENT OUT
	PE10	TIM1_CH3	-	FMC_NE3	FMC_NCE2	SDMMC2_D4	SDMMC2_CKIN	-	EVENT OUT
	PE11	TIM1_CH3N	-	-	FMC_A16/ FMC_CLE	SDMMC2_D1	-	-	EVENT OUT
	PE12	TIM1_CH2	-	FMC_NE2	FMC_NCE1	SDMMC2_D3	-	-	EVENT OUT
	PE13	TIM1_CH2N	-	-	FMC_RNB	SDMMC2_D0	-	-	EVENT OUT
	PE14	TIM1_BKIN	-	-	FMC_NWE	SDMMC2_CK	-	-	EVENT OUT
	PE15	TIM1_CH1N	-	-	FMC_NOE	SDMMC2_CMD	-	-	EVENT OUT
Port F	PF0	TIM12_CH2	I2C2_SDA	ETH1_MDC	ETH2_MII_CR S	-	I3C2_SDA	-	EVENT OUT
	PF1	-	-	ETH1_MII_RXD0/ETH1_RGMII_RXD0/ ETH1_RMII_RXD0	-	-	-	-	EVENT OUT
	PF2	TIM12_CH1	I2C2_SCL	ETH1_MDIO	ETH2_MII_CO L	FMC_NE4	I3C2_SCL	-	EVENT OUT
	PF3	TIM8_BKIN2	ETH1_CLK	ETH2_PPS_OUT	-	FMC_A20	LCD_R6	DCMI_HSYNC/PSSI_DE/ DCMIPP_HSYNC	EVENT OUT
	PF4	ETH1_MDC	ETH2_CLK	ETH2_PPS_OUT	ETH1_PPS_O UT	-	LCD_B7	-	EVENT OUT
	PF5	ETH1_MDIO	ETH1_CLK	ETH2_PHY_INTN	ETH1_PHY_IN TN	-	LCD_B6	-	EVENT OUT
	PF6	-	-	ETH2_MII_RX_CLK/ETH2_RGMII_RX_CLK/ ETH2_RMII_REF_CLK	-	-	LCD_B0	-	EVENT OUT
	PF7	-	-	ETH2_RGMII_GTX_CLK	ETH2_MII_TX _CLK	-	LCD_R1	-	EVENT OUT
	PF8	-	ETH1_CLK	ETH2_RGMII_CLK125	ETH2_MII_RX _ER	ETH2_MII_RX_DV/ ETH2_RMII_CRS_DV	LCD_G0	-	EVENT OUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/8 / I3C1 / TIM1/2/3/4/5/8/10 /11/12/16 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I2C1/2/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I3C4 / LCD / OCTOSPIM_P 1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / FMC / LCD / SDMMC3	SYS
Port F	PF9	-	-	ETH2_MII_RXD2/ETH2_RGMII_RXD2	ETH2_MDIO	-	-	-	EVENT OUT
	PF10	-	-	ETH2_MII_TXD2	-	-	-	-	EVENT OUT
	PF11	-	-	ETH2_MII_TXD3	-	-	-	-	EVENT OUT
	PF12	TIM5_CH1	-	-	-	-	LCD_CLK	DCMI_D0/PSSI_D0/ DCMIPP_D0	EVENT OUT
	PF13	TIM3_CH3	-	-	-	-	LCD_R2	-	EVENT OUT
	PF14	TIM3_CH4	-	-	-	-	LCD_R3	-	EVENT OUT
	PF15	TIM3_ETR	-	-	-	-	LCD_R4	-	EVENT OUT
Port G	PG0	TIM8_CH3N	-	ETH2_MII_RXD0/ETH2_RGMII_RXD0/ ETH2_RMII_RXD0	ETH1_MII_RX D2	-	LCD_G5	DCMI_D4/PSSI_D4/ DCMIPP_D4	EVENT OUT
	PG1	TIM5_CH4	-	ETH2_MII_RX_ER	ETH2_MII_RX D3	FMC_NBL0	LCD_VSYNC	DCMI_D11/PSSI_D11/ DCMIPP_D11	EVENT OUT
	PG2	TIM5_CH3	-	ETH2_MII_TX_CLK	ETH2_RGMII_ CLK125	FMC_CLK	LCD_HSYNC	-	EVENT OUT
	PG3	TIM8_ETR	ETH2_CLK	ETH2_PHY_INTN	-	FMC_A19	LCD_R5	DCMI_PIXCLK/PSSI_PDCK/ DCMIPP_PIXCLK	EVENT OUT
	PG4	TIM8_BKIN	-	ETH2_PPS_OUT	ETH2_MDC	FMC_A21	LCD_R7	DCMI_VSYNC/PSSI_RDY/ DCMIPP_VSYNC	EVENT OUT
	PG5	-	-	-	-	-	LCD_R5	DCMI_PIXCLK/PSSI_PDCK/ DCMIPP_PIXCLK	EVENT OUT
	PG6	-	-	-	-	-	LCD_R6	DCMI_HSYNC/PSSI_DE/ DCMIPP_HSYNC	EVENT OUT
	PG7	TIM5_ETR	-	-	-	-	LCD_R7	DCMI_VSYNC/PSSI_RDY/ DCMIPP_VSYNC	EVENT OUT
	PG8	TIM5_CH3	-	-	-	-	LCD_G2	DCMI_D2/PSSI_D2/ DCMIPP_D2	EVENT OUT
	PG9	TIM5_CH4	-	-	-	-	LCD_G3	DCMI_D3/PSSI_D3/ DCMIPP_D3	EVENT OUT
	PG10	TIM8_CH4N	-	-	-	-	LCD_G4	DCMI_D4/PSSI_D4/ DCMIPP_D4	EVENT OUT
	PG11	TIM8_CH4	-	-	-	-	LCD_G5	DCMI_D5/PSSI_D5/ DCMIPP_D5	EVENT OUT
	PG12	TIM8_CH1N	-	-	-	-	LCD_G6	DCMI_D6/PSSI_D6/ DCMIPP_D6	EVENT OUT
	PG13	TIM8_CH2N	I2C1_SCL	I3C1_SCL	-	-	LCD_G7	DCMI_D7/PSSI_D7/ DCMIPP_D7	EVENT OUT
	PG14	TIM8_BKIN2	-	-	-	-	LCD_B1	DCMI_D9/PSSI_D9/ DCMIPP_D9	EVENT OUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/8 / I3C1 / TIM1/2/3/4/5/8/10 /11/12/16 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I2C1/2/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I3C4 / LCD / OCTOSPIM_P 1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / FMC / LCD / SDMMC3	SYS
Port G	PG15	TIM8_ETR	-	-	-	-	LCD_B2	DCMI_D10/PSSI_D10/ DCMIPP_D10	EVENT OUT
Port H	PH2	-	-	-	-	-	-	-	EVENT OUT
	PH3	-	TIM5_CH3	I2C7_SCL	-	-	-	-	EVENT OUT
	PH4	-	TIM5_CH2	LCD_R0	USB3DR_OVR CUR	USBH_HS_OVRCUR	ETH1_PTP_AUX_TS	-	EVENT OUT
	PH5	UART7_RX	-	LCD_G1	USB3DR_VBU SEN	USBH_HS_VBUSEN	ETH2_PTP_AUX_TS	-	EVENT OUT
	PH6	-	-	I2C1_SMBA	-	-	-	-	EVENT OUT
	PH7	-	TIM5_CH4	I2C7_SDA	-	-	-	-	EVENT OUT
	PH8	-	TIM5_CH1	-	-	-	-	-	EVENT OUT
	PH9	-	-	ETH1_RGMII_CLK125	ETH1_MII_RX _ER	-	-	-	EVENT OUT
	PH10	-	ETH2_MDC	ETH1_MII_TXD2/ETH1_RGMII_TXD2	-	-	-	-	EVENT OUT
	PH11	-	ETH2_MDIO	ETH1_MII_TXD3/ETH1_RGMII_TXD3	-	-	-	-	EVENT OUT
	PH12	TIM10_CH1	-	ETH1_MII_RXD2/ETH1_RGMII_RXD2	-	-	-	-	EVENT OUT
	PH13	TIM11_CH1	-	ETH1_MII_RXD3/ETH1_RGMII_RXD3	-	-	-	-	EVENT OUT
Port I	PI0	TIM8_BKIN	-	-	-	-	LCD_B3	DCMI_D11/PSSI_D11/ DCMIPP_D11	EVENT OUT
	PI1	TIM8_CH3N	I2C1_SDA	I3C1_SDA	-	-	LCD_B4	DCMI_D8/PSSI_D8/ DCMIPP_D8	EVENT OUT
	PI2	TIM8_CH1	-	-	-	-	LCD_B5	DCMI_D13/PSSI_D13/ DCMIPP_D13	EVENT OUT
	PI3	TIM8_CH2	-	-	-	-	LCD_B6	PSSI_D14/DCMIPP_D14	EVENT OUT
	PI4	TIM8_CH3	-	-	-	-	LCD_B7	PSSI_D15/DCMIPP_D15	EVENT OUT
	PI5	TIM5_CH2	-	-	-	-	LCD_DE	DCMI_D1/PSSI_D1/ DCMIPP_D1	EVENT OUT
	PI6	TIM3_CH1	-	-	-	-	LCD_VSYNC	-	EVENT OUT
	PI7	TIM3_CH2	-	-	-	-	LCD_HSYNC	-	EVENT OUT
	PI8	-	-	-	-	-	-	-	EVENT OUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/8 / I3C1 / TIM1/2/3/4/5/8/10 /11/12/16 / UART7 / USART2	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I2C1/2/7/8 / LPTIM5 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/7 / I3C1/2 / LCD / LPTIM3/4 / OCTOSPIM_P1/2 / SDMMC1/3 / TIM14	ETH1/2 / FMC / I3C4 / LCD / OCTOSPIM_P 1/2 / SDMMC1 / USB3DR	DSI / ETH1/2 / FMC / LCD / OCTOSPIM_P2 / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / DSI / ETH1/2 / I3C2 / LCD / OCTOSPIM_P1 / SDMMC2	DCMI / PSSI / DCMIPP / FMC / LCD / SDMMC3	SYS
Port I	PI9	TIM16_BKIN	SDVSEL2	FMC_NWAIT	-	DSI_TE	LCD_B0	-	EVENT OUT
	PI10	TIM4_CH1	SDVSEL1	-	-	FMC_AD12/FMC_D12	DSI_TE	-	EVENT OUT
	PI11	-	TIM4_CH3	SDMMC3_D3	FMC_AD15/ FMC_D15	-	-	-	EVENT OUT
Port Z	PZ0	I2C8_SDA	-	LPTIM3_CH2	I3C4_SDA	-	-	-	EVENT OUT
	PZ1	I2C8_SCL	I2C8_SMBA	-	I3C4_SCL	-	-	-	EVENT OUT
	PZ2	I2C8_SCL	-	-	I3C4_SCL	-	-	-	EVENT OUT
	PZ3	I2C8_SDA	-	LPTIM4_CH2	I3C4_SDA	-	-	-	EVENT OUT
	PZ4	I2C8_SCL	-	-	I3C4_SCL	-	-	-	EVENT OUT
	PZ5	-	-	LPTIM4_CH2	-	-	-	-	EVENT OUT
	PZ6	-	-	LPTIM4_CH2	-	-	-	-	EVENT OUT
	PZ7	-	-	LPTIM3_CH2	-	-	-	-	EVENT OUT
	PZ8	I2C8_SMBA	LPTIM5_ETR	-	-	-	-	-	EVENT OUT
	PZ9	I2C8_SDA	-	LPTIM3_CH2	I3C4_SDA	-	-	-	EVENT OUT

5 Memory mapping

Refer to the product line reference manual (STM32MP23/25xx reference manual (RM0457)) for details on the memory mapping as well as the boundary addresses for all peripherals.

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with an junction temperature at T_J = 25 ° C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V, V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V, V_{DDGPU} = 0.8 V. They are given only as design guidelines and are not tested in production.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 9 .

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 10 .

Figure 9. Pin loading conditions

Figure 10. Pin input voltage

6.1.6 Power supply scheme

Figure 11. Power supply scheme

Caution: *Each power supply pair (V_{DD}/V_{SS}, V_{DDCORE}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.*

The number of needed capacitances and their values are provided in AN5489 "Getting started with STM32MP25x lines hardware development" available from the ST website www.st.com.

6.1.7 Current consumption measurement

Figure 12. Current consumption measurement scheme

6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 14. Voltage characteristics, Table 15. Current characteristics, and Table 16. Thermal characteristics may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 14. Voltage characteristics

Specified by design, not tested in production.
All powers and grounds pins must always be connected to an external power supply, in the permitted range.

Symbols	Ratings	Min	Max	Unit
V_{DDX} - V_{SS} range 1.8 V	External supply voltage (including V_{DD}, V_{DDIOx}, V_{BAT})	-0.3	2	V
V_{DDX} - V_{SS} range 3.3 V	External supply voltage (including V_{DD}, V_{DDIOx}, V_{BAT}, $V_{DD33USB}$, $V_{DD33UCPD}$)	-0.3	3.7	
$V_{DDCORE} – V_{SS}$	External core supply voltage (including V_{DDCORE}, V_{DDCPU}, V_{DDGPU}, V_{DDCSI}, V_{DDDSI}, V_{DDLVDS})	-0.3	0.99	
$V_{DDQDDR} – V_{SS}$	DDR IO supply voltage	-0.3	1.575	
$V_{DDA18} – V_{SS}$	1.8 V supply voltage (including $V_{DDA18AON}$, $V_{DDA18PLL1}$, $V_{DDA18PLL2}$, $V_{DDA18PLL3}$, $V_{DDA18DSI}$, $V_{DDA18CSI}$, $V_{DDA18LVDS}$, $V_{DDA18DDR}$, $V_{DDA18USB}$, $V_{DDA18ADC}$)	-0.3	1.98	
V_{IN}[1]	Input voltage on TT_xx pins (VDDIOxVRSEL = 0)	V_{SS} - 0.3	min(V_{DDIOx} + 0.3, 3.6)	
	Input voltage on TT_xx pins (VDDIOxVRSEL = 1)		min(V_{DDIOx} + 0.3, 1.98)	
	Input voltage on UCPD pins		V_{DD3V3_UCPD} + 1.935	
	Input voltage on USB3DR or USBH_HS DP/DM pins		min(V_{DD3V3_USB} + 0.3, 3.6)[2]	
	Input voltage on CSI pins		1.35	
$\|\Delta V_{DDx}\|$	Variations between different VDDX power pins of the same domain	-	50	mV
$\|V_{SSx}-V_{SS}\|$	Variations between all the different ground pins	-	50	

1. *V_{IN} maximum must always be respected. Refer to next table for the maximum allowed injected current values.*
2. *When the supply is not present, the IOs tolerate being pulled to 3.5 V maximum through external resistors.*

Table 15. Current characteristics

Specified by design, not tested in production.

Symbols	Ratings	Condition	Max	Unit
I_{IO}	Output current sunk/source by any I/O and control pin	T_J > 110 °C	4	mA
		90 °C < T_J ≤ 110 °C	10	
		-40 °C < T_J ≤ 90 °C	20	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)[1]		±25	

1. *When several inputs are submitted to a current injection, the maximum ∑IINJ(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values).*

Table 16. Thermal characteristics

Specified by design, not tested in production.

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (suffix 3)	125	

6.3 Operating conditions

6.3.1 General operating conditions

Table 17. General operating conditions

Voltages in this table represent DC value at ball level.

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
F_{cpu1}	Clock frequency of Cortex-A35		0	-	1200	MHz
$F_{cpu1_overdrive}$[1]	Clock frequency of Cortex-A35 in overdrive	STM32MP23xF only	0	-	1500	MHz
F_{gpu}[1]	Clock frequency of GPU/NPU		0	-	400	MHz
$F_{ddrctrl}$	Clock frequency of DDR memory[2]	DDR3L DLL ON	300	-	1066	MHz
		DDR3L DLL OFF	0	-	125	MHz
		DDR4 DLL ON	625	-	1200	MHz
		DDR4 DLL OFF	20	-	125	MHz
		LPDDR4	10	-	1200	MHz
$F_{ck_icn_hs_mcu}$	Clock frequency of Cortex-M33, MCU MLAHB memory		0	-	400	MHz
$F_{ck_icn_m_gpu}$[1]	Clock frequency of GPU/NPU bus		0	-	600	MHz
$F_{ck_icn_ddr}$	Clock frequency of Cortex-A35 AXI buses, DDRCTRL AXI buses		0	-	600	MHz
$F_{ck_icn_hsl}$	Clock frequency of USB3DR, USBH, ETH1, ETH2 buses		0	-	300	MHz
$F_{ck_icn_ls_mcu}$	Clock frequency of MCU MLAHB, MCU and SmartRun domain peripherals buses	In Run mode	0	-	200	MHz
$F_{ck_icn_sdmmc}$	Clock frequency of MPU AHB5		0	-	200	MHz
$F_{ck_icn_nic}$	Clock frequency of MPU GIC and BOOTROM		0	-	400	MHz
$F_{ck_icn_vid}$[1]	Clock frequency of MPU VDEC bus		0	-	600	MHz
$V_{DDA18AON}$[3]	Internal analog supply voltage		1.75[4]	1.8	1.89[5]	V
V_{DD}[3]	I/Os supply voltage	1.8 V range	1.71	1.8	1.89[5]	V
		3.3 V range[6]	3	3.3	3.6	V
V_{DDIO1}, V_{DDIO2}, V_{DDIO3}, V_{DDIO4}[7]	Specific I/Os supply voltage	1.8 V range	1.71	1.8	1.89[5]	V
		3 V / 3.3 V range[8] .	2.7	3.3	3.6	V
V_{DDCORE}, V_{DDCSI}, V_{DDDSI}, V_{DDLVDS}[9]	Main digital logic supply voltage	Run1/2 mode	0.79	0.82	0.842	V
		Stop1/2, LP-Stop1/2 mode	0.79	0.82	0.842	V
		LPLV-Stop1/2 mode	0.64	0.67	0.842[10]	V
		Standby2 mode	0	0	0.48	V
V_{DDCPU}	Cortex-A35 supply voltage	Run1, Stop1 or LP-Stop1 mode, $F_{cpu1_overdrive}$ range[1]	0.87	0.91	0.935	V
		Run1, Stop1 or LP-Stop1 mode, F_{cpu1} range	0.765	0.8	0.842	V

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DDCPU}	Cortex-A35 supply voltage	LPLV-Stop1 (LPCFG_D1 = 0)	0.64	0.67	0.842[10]	V
		Run2, Stop2, LP-Stop2 , LPLV-Stop2 or Standby2 mode	0	0	0.48	V
V_{DDGPU}[1]	GPU supply voltage	When connected to V_{DDCPU}	V_{DDCPU}			V
		Dedicated supply	0.76	0.8	0.839	V
$V_{DDA18PLL1}$, $V_{DDA18PLL2}$, $V_{DDA18PLL3}$, $V_{DDA18DSI}$, $V_{DDA18CSI}$, $V_{DDA18LVDS}$[9][11]	1.8 V analog supply for PLLs, DSI/CSI/LVDS PHYs		1.71	1.8	1.89[5]	V
$V_{DDA18DDR}$[12]	1.8 V analog supply for DDRPHY		1.71	1.8	1.89	V
$V_{DDA18USB}$[12]	1.8 V analog supply for USBPHY		1.75	1.8	1.89[5]	V
$V_{DD33USB}$, $V_{DD33UCPD}$	3.3V USB supply		3.07	3.3	3.6	V
$V_{DDA18ADC}$	ADC operating voltage		1.62	1.8	1.89[5]	V
V_{REF+}	ADC reference voltage		1.1	-	$V_{DDA18ADC}$	V
V_{BAT}	Backup operating voltage		2.3[13]	-	3.6	V
V_{DDQDDR}	DDR PHY supply voltage[2]	DDR3L memory	1.283	1.35	1.45	V
		DDR4 memory	1.14	1.2	1.26	
		LPDDR4 memory	1.06	1.1	1.17	
V_{08CAP}	Backup regulator output voltage[14]		0.72	0.8	0.88	V
VIN	I/O Input voltage	I/O	-0.3	-	V_{DDxx} + 0.3 [15]	V
		I/O when ADC is used			$V_{DDA18ADC}$ + 0.3	
		ANA0/ANA1				
		I/O when PVD_IN is used			$V_{DDA18AON}$ + 0.3	
		UCPD IOs			V_{DD3V3_UCPD} + 1.935	
		DDR I/O			V_{DDQDDR}	
T_J	Junction temperature range	Suffix 3 version	-40	-	125	° C

1. *Feature might be limited or absent in some devices or packages. See Section 2 for details.*
2. *Values depend on the external memory device choice.*
3. *$V_{DDA18AON}$ and V_{DD} must be present before any other supply.*
4. *Functional down to 1.71 V if UCPD is not used.*
5. *Static condition. 1.98 V allowed during transients.*
6. *Requires VDDIOVRSEL = 0.*
7. *These supplies are independent, that means each one could be in any of the following voltage ranges: 0 V (OFF), 1.8 V, 3 V or 3.3 V.*
8. *Requires VDDIOxVRSEL = 0*
9. *All these supplies are usually connected together.*

10. *This is the max allowed voltage, however LPLV-Stop mode is relevant only to save power, so requires voltage as low as possible (that is external regulator set for typical value, then the maximum voltage is few percent above the typical due to regulator accuracy).*
11. *The $V_{DDA18PLLx}$ must be connected together.*
12. *Could be connected to other $V_{DDA18xx}$ supplies if min/max range fullfilled.*
13. *Except when connected to V_{DD} where lower limit is then 1.71 V.*
14. *This pin is used only to connect a decoupling capacitor for internal backup regulator, this pin must never be used externally for other purposes.*
15. *V_{DDxx} stands for V_{DD}, V_{DDIO1}, V_{DDIO2}, V_{DDIO3} or V_{DDIO4}.*

6.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions.

Constraints on power supply sequences:

- $V_{DDA18AON}$ and V_{DD} must be present before any other supply (except V_{BAT}) and kept present whenever any other supply is present (except V_{BAT}). Damage could occur if not ensured.
- $V_{DDA18AON}$ and V_{DD} should ramp up and ramp down together (within a 1 ms time windows). Damage could occur if not ensured.
- $V_{DDA18USB}$ should be present whenever $V_{DD33USB}$ is present. Damage could occur if not ensured.
- V_{DDCORE} should be present whenever $V_{DDA18USB}$ and/or $V_{DDA33USB}$ are present. If not ensured, leakage could occur on these supplies until V_{DDCORE} is present.

Table 18. Operating conditions at power-up / power-down

Symbol	Parameter	Operating conditions	Min	Max	Unit
$t_{VDDA18AON}$	$V_{DDA18AON}$ transitions	Rise time rate	20	1500	µs/V
		Fall time rate	20	1500	
t_{VDD}	$V_{DD/VDDIOx}$ transitions	Rise time rate	20	1500	
		Fall time rate	20	1500	
$t_{VDDCORE}$	V_{DDCORE} transitions	Rise time rate	20	1500	
		Fall time rate	25	1500	
t_{VDDCPU}, t_{VDDGPU}, t_{VDDCSI}, t_{VDDSI}, $t_{VDDLVDS}$	V_{DDCPU}, V_{DDGPU}, V_{DDCSI}, V_{DDDSI}, V_{DDLVDS} transitions	Rise time rate	10	1500	
		Fall time rate	10	1500	
t_{VDDA18}	$V_{DDA18PLL1}$, $V_{DDA18PLL2}$, $V_{DDA18PLL3}$, $V_{DDA18DSI}$, $V_{DDA18CSI}$, $V_{DDA18LVDS}$, $V_{DDA18DDR}$, $V_{DDA18USB}$, $V_{DDA18ADC}$ transitions	Rise time rate	10	1500	
		Fall time rate	10	1500	
t_{VDD33}	$V_{DD33USB}$, $V_{DD33UCPD}$ transitions	Rise time rate	10	1500	
		Fall time rate	10	1500	
$t_{VDDQDDR}$	V_{DDQDDR} transitions	Rise time rate	10	1500	
		Fall time rate	10	1500	
t_{VBAT}	V_{BAT} transitions	Rise time rate	20	∞	
		Fall time rate	10	1500	

6.3.3 Embedded reset and power control block characteristics

The parameters given in Table 19 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions.

Table 19. Embedded reset and power control block characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{RSTTEMPO}$	Reset temporization	After POR released		-	440	-	µs
$V_{DDA18AON}$ thresholds							
V_{POR_ANA}(1)	Power-on reset threshold	Rising edge		1.62	1.67	1.71	V
V_{PDR_ANA}(1)	Power-down reset threshold	Falling edge		1.58	1.63	1.67	
$V_{hyst_POR_ANA}$	Hysteresis voltage of POR/PDR	-		-	40	-	mV
$I_{POR_PDR(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON		-	1.25	-	µA
V_{DD} thresholds							
V_{POR}(1)	Power-on reset threshold	Rising edge		1.62	1.67	1.71	V
V_{PDR}(1)	Power-down reset threshold	Falling edge		1.58	1.63	1.67	
V_{hyst_POR}	Hysteresis voltage of POR/PDR	-		-	40	-	mV
$I_{POR_PDR(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON		-	0.75	-	µA
$I_{POR_PDR(VDD)}$	Supply current on V_{DD}	Always ON	V_{DD} = 1.8 V	-	0.5	-	µA
			V_{DD} = 3.3 V	-	0.92	-	
V_{BOR0}(1)	Brown-out reset threshold 0	Rising edge		1.62	1.67	1.71	V
		Falling edge		1.58	1.63	1.67	
V_{BOR1}(1)	Brown-out reset threshold 1	Falling edge		-	-	2.97	V
V_{hyst_BOR0}	Hysteresis voltage of BOR0	-		-	40	-	mV
V_{hyst_BOR1}	Hysteresis voltage of BOR1	-		-	80	-	mV
$I_{BOR(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	BOR enabled in OTP		-	0.75	-	µA
V_{DDCPU} thresholds							
V_{RDY_VDDCPU}(1)	Threshold on rising edge	Normal modes		0.63	0.66	0.69	V
		LPLV modes		0.55	0.58	0.61	
V_{hyst_VDDCPU}	Hysteresis on falling edge	-		-	23	-	mV
T_{delay_VDDCPU}	Delay after detection	Rising edge		180	400	750	µs
		Falling edge		-	0	-	
$I_{RDY_VDDCPU(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON		-	1.2	-	µA
V_{DDCORE} thresholds							
$V_{RDY_VDDCORE}$(1)	Threshold on rising edge	Normal modes		0.63	0.66	0.69	V
		LPLV modes		0.55	0.58	0.61	
$V_{hyst_VDDCORE}$	Hysteresis on falling edge	-		-	23	-	mV
$T_{delay_VDDCORE}$	Delay after detection	Rising edge		180	400	750	µs
		Falling edge		-	0	-	
$I_{RDY_VDDCORE(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON		-	1.2	-	µA

1. *Guaranteed by test in production.*

6.3.4 Embedded reference voltage

The parameters given in Table 20 and Table 21 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 17. General operating conditions .

Table 20. Embedded reference voltage characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}[(1)]	Internal reference voltages	-40 °C < T_J < 125 °C	0.792	0.8	0.808	V
$t_{S_VREFINT}$[(2)]	ADC sampling time when reading the internal reference voltage	-	34	-	-	ns
DV_{REFINT}	Internal reference voltage spread over the temperature range	-40 °C < T_J < 125 °C	-4	-	+4	mV
T_{coeff}	Average temperature coefficient	-40 °C < T_J < 125 °C	-	-	43	ppm/°C
$V_{DDcoeff}$	Average voltage coefficient	1.71 < $V_{DDA18AON}$ < 1.89	-	-	1250	ppm/V

1. *Guaranteed by test in production.*
2. *Specified by design, not tested in production.*

Table 21. Embedded reference voltage calibration value

Symbol	Parameter	Memory address
VREFINT_CAL	Raw data acquired on ADC1 at temperature of 30 °C, $V_{DDA18ADC}$ = V_{REF+} = 1.8 V	0x4400 01B8[11:0][(1)(2)]

1. *This is BSEC_FVR110 register which is not automatically shadowed with OTP content, so a fuse read sequence must be issued to get the register updated once (clear after reading). Refer to product reference manual - BSEC section "Operations on fuses".*
2. *Must be read in 32-bit words and relevant masking and shifting must be performed to isolate the required bits.*

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in Figure 12. Current consumption measurement scheme.

All the Run mode current consumption measurements given in this section are performed with a CoreMark code unless otherwise specified.

Supply current characteristics are evaluated by characterization, not tested in production unless otherwise specified.

6.3.5.1 Typical and maximum current consumption

The device is placed under the following conditions:

- All I/O pins are in analog input mode except when explicitly mentioned
- All peripherals are disabled except when explicitly mentioned
- RTC/LSE are disabled, unless otherwise specified
- BKPSRAM, RETRAM backup supplies in low-power modes (such as LPLV-Stop, Standby and V_{BAT} modes) are disabled, unless otherwise specified

- Unless otherwise specified, the typical values are obtained for:
  - V_{DD} / V_{DDIOx}/V_{BAT} = 3.3 V
  - V_{DDCORE} = 0.82 V
  - V_{DDCPU} = 0.8 V
  - V_{DDGPU} = 0.8 V
  - V_{DDA18} / $V_{DDA18AON}$ = 1.8 V
    and the maximum values are obtained for:
  - V_{DD} / V_{DDIOx} / V_{BAT} = 3.6 V
  - V_{DDCORE} = 0.842 V
  - V_{DDCPU} = 0.842 V
  - V_{DDGPU} = 0.839 V
  - V_{DDA18} / $V_{DDA18AON}$ = 1.89 V

The parameters given in Table 22 to Table 32 are derived from tests performed under supply voltage conditions summarized in Table 17. General operating conditions .

Table 22. Current consumption (I_{DDCORE}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions									Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}[3]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	400[6]	170	240	510	690	1100	mA
							1200	600	-	400	170	240	510	680	1100	
							750	600	-	400	170	240	500	680	1100	
							600	600	-	400	170	240	500	680	1100	
I_{DDCORE}[7]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	170	240	510	680	1100	mA
							1200	600	-	-	170	240	500	680	1100	
							750	600	-	-	170	240	500	680	1100	
							600	600	-	-	170	240	500	680	1100	
I_{DDCORE}[8]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	160	230	490	670	1000	mA
							1200	600	-	-	160	230	490	670	1000	
							750	600	-	-	160	230	490	670	1000	
							600	600	-	-	160	230	490	670	1000	
I_{DDCORE}[9]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1	HSE + HSI + PLL	1500[5]	600	400	400[6]	97	160	420	600	940	mA
							1200	600	400	400	97	160	420	600	940	
							750	600	400	400	96.5	160	420	600	940	
							600	600	400	400	96.5	160	420	600	930	
I_{DDCORE}[10]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1	HSE + HSI + PLL	1500[5]	600	400	-	97	160	420	600	930	mA
							1200	600	400	-	97	160	420	600	930	
							750	600	400	-	96.5	160	420	600	930	
							600	600	400	-	96.5	160	420	600	930	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (CRun)	SRun1	HSE + HSI + PLL	1500[5]	600	400	-	97	160	420	600	930	mA
							1200	600	400	-	97	160	420	600	930	
							750	600	400	-	96.5	160	420	600	930	
							600	600	400	-	96.5	160	420	600	930	

Symbol	Parameter	Conditions									Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}[10]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	49.5	100	370	540	870	mA
							1200	600	-	-	49	100	370	540	870	
							750	600	-	-	49	100	360	540	870	
							600	600	-	-	48.5	100	360	540	870	
							300	300	-	-	43.5	94	360	530	860	
							150	150	-	-	41	91	350	530	860	
						HSI	HSI 64	HSI 64	-	-	36.5	86	350	520	850	
						HSE + HSI	HSE 40	HSE 40	-	-	35.5	84	350	520	850	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	49	100	370	540	870	mA
							1200	600	-	-	49	100	360	540	870	
							750	600	-	-	48.5	100	360	540	870	
							600	600	-	-	48.5	100	360	540	870	
							300	300	-	-	43.5	94	360	530	860	
							150	150	-	-	41	91	350	530	860	
						HSI	HSI 64	HSI 64	-	-	36.5	86	350	520	850	
						HSE + HSI	HSE 40	HSE 40	-	-	35.5	84	350	520	850	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CRun)	SRun1	HSE + HSI + PLL	-	HSI 64	400	-	83	140	400	580	910	mA
							-	HSI 64	200	-	56	110	370	550	870	
							-	HSI 64	100	-	43	92	360	530	860	
						HSI	-	HSI 64	HSI 64	-	38.5	89	350	520	850	
						HSE + HSI	-	HSI 64	HSE 40	-	34	82	350	520	850	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStandby[11] [12] (CStandby)	Run2 (CRun)	SRun1	HSE + HSI + PLL	-	HSI 64	400	-	83	160	400	580	910	mA
							-	HSI 64	200	-	56	120	370	550	870	
							-	HSI 64	100	-	43	95	360	530	860	
						HSI	-	HSI 64	HSI 64	-	38.5	90	350	520	850	
						HSE + HSI	-	HSI 64	HSE 40	-	34	83	350	520	840	

Symbol	Parameter	Conditions									Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun (CSleep)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	49	100	360	540	870	mA
							1200	600	-	-	49	100	360	540	870	
							750	600	-	-	48.5	100	360	540	870	
							600	600	-	-	48.5	100	360	540	870	
							300	300	-	-	43.5	94	360	530	860	
							150	150	-	-	41	91	350	530	860	
						HSI	HSI 64	HSI 64	-	-	36.5	86	350	520	850	
						HSE + HSI	HSE 40	HSE 40	-	-	35.5	84	350	520	850	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun[13] (eCSleep)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	48.5	99	360	540	870	mA
							1200	600	-	-	48.5	99	360	540	870	
							750	600	-	-	48.5	99	360	540	870	
							600	600	-	-	48.5	99	360	540	870	
							300	300	-	-	43.5	94	360	530	860	
							150	150	-	-	41	91	350	530	860	
						HSI	HSI 64	HSI 64	-	-	36.5	86	350	520	850	
						HSE + HSI	HSE 40	HSE 40	-	-	35.5	84	350	520	850	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CSleep)	SRun1	HSE + HSI + PLL	-	HSI 64	400	-	65.5	120	380	560	890	mA
							-	HSI 64	200	-	47.5	97	360	540	860	
							-	HSI 64	100	-	38.5	87	350	530	850	
						HSI	-	HSI 64	HSI 64	-	35.5	85	350	520	850	
						HSE + HSI	-	HSI 64	HSE 40	-	32.5	80	340	520	850	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStandby (CStandby)[11] [12]	Run2 (CSleep)	SRun1	HSE + HSI + PLL	-	HSI 64	400	-	65.5	130	380	560	880	mA
							-	HSI 64	200	-	47.5	110	360	540	860	
							-	HSI 64	100	-	38.5	88	350	530	850	
						HSI	-	HSI 64	HSI 64	-	35.5	86	350	520	850	
						HSE + HSI	-	HSI 64	HSE 40	-	32.5	80	340	520	840	

1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*
2. *ck_icn_ddr.*
3. *Values for STM32MP235x.*
4. *Activity on peripherals and bus masters other than processors, could lead to additional power consumption above these values, largely dependent on the amount of initialized peripherals and their activity.*
5. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
6. *Typical value given with V_{DDGPU} = 0.91 V, maximum values given with V_{DDGPU} = 0.935 V.*
7. *Values for STM32MP233x.*
8. *Values for STM32MP231x.*
9. *Values for STM32MP235x.*
10. *Not relevant for STM32MP231x.*
11. *CStandby = CStop and PDDS_D1 = 1.*
12. *V_{DDCPU} is shutdown.*
13. *eCSleep mean CPU1 in enhanced CSleep with PLL1 automatically stopped (RCC_C1SREQSETR.ESLPREQ=1).*

Table 23. Current consumption (I_{DDCPU}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions									Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCPU}[3]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	400[6]	245	290	360	410	510	mA
							1200	600	-	400	165	210	270	320	410	
							750	600	-	400	105	130	200	240	330	
							600	600	-	400	84.5	110	170	220	310	
I_{DDCPU}[7]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	245	290	360	410	530	mA
							1200	600	-	-	165	210	270	320	420	
							750	600	-	-	105	130	200	240	330	
							600	600	-	-	84	110	170	220	300	
I_{DDCPU}[8]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	130	160	230	270	380	mA
							1200	600	-	-	89.5	120	180	220	310	
							750	600	-	-	57	73	140	180	270	
							600	600	-	-	46	61	130	170	260	
I_{DDCPU}[9]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1	HSE + HSI + PLL	1500[5]	600	400	-	245	290	360	410	510	mA
							1200	600	400	-	165	210	270	320	410	
							750	600	400	-	105	130	200	240	330	
							600	600	400	-	84	110	170	220	310	
I_{DDCPU}[8]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (CRun)	SRun1	HSE + HSI + PLL	1500[5]	600	400	-	130	160	230	280	370	mA
							1200	600	400	-	89.5	120	180	220	310	
							750	600	400	-	57	73	140	190	270	
							600	600	400	-	46	60	130	170	260	
I_{DDCPU}[9]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	245	290	360	410	510	mA
							1200	600	-	-	165	210	270	320	410	
							750	600	-	-	105	130	200	240	330	
							600	600	-	-	84	110	170	220	310	
							300	300	-	-	43.5	58	120	170	250	

Symbol	Parameter	Conditions									Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCPU}[9]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	150	150	-	-	22.5	34	95	140	230	mA
						HSI	HSI 64	HSI 64	-	-	11	23	81	130	220	
						HSE + HSI	HSE 40	HSE 40	-	-	7.45	16	77	130	210	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	130	160	230	280	370	mA
							1200	600	-	-	89.5	120	180	220	310	
							750	600	-	-	57	73	140	180	270	
							600	600	-	-	46	61	130	170	260	
							300	300	-	-	24	35	97	150	230	
							150	150	-	-	13	23	84	130	220	
						HSI	HSI 64	HSI 64	-	-	6.85	17	76	120	210	
						HSE + HSI	HSE 40	HSE 40	-	-	5	14	74	120	210	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CRun)	SRun1	HSE + HSI + PLL	-	HSI 64	400	-	2.25	10	71	120	200	mA
							-	HSI 64	200	-	2.3	9.9	71	120	200	
							-	HSI 64	100	-	2.25	9.9	71	120	200	
							-	HSI 64	HSI 64	-	2.25	9.9	71	120	200	
							-	HSI 64	HSE 40	-	2.25	9.9	71	120	200	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun (CSleep)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	19	29	93	140	230	mA
							1200	600	-	-	13.5	23	84	130	220	
							750	600	-	-	9.15	18	79	130	210	
							600	600	-	-	7.75	17	77	130	210	
							300	300	-	-	5.05	14	74	120	210	
							150	150	-	-	3.65	12	72	120	210	
						HSI	HSI 64	HSI 64	-	-	2.85	11	71	120	200	
						HSE + HSI	HSE 40	HSE 40	-	-	2.6	11	71	120	200	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun[10] (eCSleep)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1500[5]	600	-	-	3.35	12	76	130	210	mA

Symbol	Parameter	Conditions									Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun[10] (eCSleep)	Run1 (Cstop)	SRun1	HSE + HSI + PLL	1200	600	-	-	2.85	11	72	120	200	mA
							750	600	-	-	2.85	11	72	120	200	
							600	600	-	-	2.85	11	72	120	200	
							300	300	-	-	2.85	11	72	120	200	
							150	150	-	-	2.85	11	72	120	200	
						HSI	HSI 64	HSI 64	-	-	2.8	11	72	120	200	
						HSE + HSI	HSE 40	HSE 40	-	-	2.65	11	71	120	200	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CSleep)	SRun1	HSE + HSI + PLL	-	HSI 64	400	-	2.3	9.9	71	120	200	mA
							-	HSI 64	200	-	2.25	9.9	71	120	200	
							-	HSI 64	100	-	2.25	9.9	71	120	200	
						HSI	-	HSI 64	HSI 64	-	2.25	9.9	71	120	200	
						HSE + HSI	-	HSI 64	HSE 40	-	2.25	9.9	71	120	200	

1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*
2. *ck_icn_ddr.*
3. *Values for STM32MP235x.*
4. *Activity on peripherals and bus masters other than processors, could lead to additional power consumption above these values, largely dependent on the amount of initialized peripherals and their activity.*
5. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
6. *Typical value given with V_{DDGPU} = 0.91 V, maximum values given with V_{DDGPU} = 0.935 V.*
7. *Values for STM32MP233x.*
8. *Values for STM32MP231x.*
9. *Not relevant for STM32MP231x.*
10. *eCSleep mean CPU1 in enhanced CSleep (RCC_C1SREQSETR.ESLPREQ = 1).*

Table 24. Current consumption (I_{DDGPU}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.
Not relevant for STM32MP251x and STM32MP253x.
Value are without GPU activity.

Symbol	Parameter	Conditions										Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	CPU3 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDGPU}[3]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	400[6]	14	35	160	240	390	mA
							1200	600	400	200	400	11.5	31	150	220	370	
							750	600	400	200	400	11.5	31	150	220	370	
							600	600	400	200	400	11.5	31	150	220	370	
I_{DDGPU}[7]	Supply current in Run mode	All peripherals Enabled[4]	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	400[6]	14	35	160	240	390	mA
							1200	600	400	200	400	11.5	31	150	220	370	
							750	600	400	200	400	11.5	31	150	220	370	
							600	600	400	200	400	11.5	31	150	220	370	
I_{DDGPU}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[5]	600	400	200	400[6]	6.65	27	150	230	380	mA
							1200	600	400	200	400	6.05	24	140	210	360	
							750	600	400	200	400	6.05	24	140	210	360	
							600	600	400	200	400	6	24	140	210	360	

1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*
2. *ck_icn_ddr.*
3. *Values for STM32MP257x.*
4. *Activity on peripherals and bus masters other than processors, could lead to additional power consumption above these values, largely dependent on the amount of initialized peripherals and their activity.*
5. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
6. *Typical value given with V_{DDGPU} = 0.9 V, maximum values given with V_{DDGPU} = 0.961 V.*
7. *Values for STM32MP255x.*

Table 25. Current consumption (I_{DD}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions									Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DD\ (3V3)}$[3]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1	HSE + HSI + PLL	1500[4]	600	400	400[5]	2.7	3.2	3.3	3.4	3.7	mA
							1200	600	400	400	2.7	3.2	3.3	3.4	3.7	
							750	600	400	400	2.7	3.2	3.3	3.4	3.7	
							600	600	400	400	2.7	3.2	3.3	3.4	3.7	
$I_{DD\ (1V8)}$[6]						HSE + HSI + PLL	1500[4]	600	400	400[5]	1.25	1.6	1.6	1.6	1.7	mA
							1200	600	400	400	1.25	1.6	1.6	1.6	1.7	
							750	600	400	400	1.25	1.6	1.6	1.6	1.7	
							600	600	400	400	1.25	1.6	1.6	1.6	1.7	
$I_{DD\ (3V3)}$[3]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1	HSE + HSI + PLL	1500[4]	600	400	-	2.7	3.2	3.3	3.4	3.7	mA
							1200	600	400	-	2.7	3.2	3.3	3.4	3.7	
							750	600	400	-	2.7	3.2	3.3	3.4	3.7	
							600	600	400	-	2.7	3.2	3.3	3.4	3.7	
$I_{DD\ (1V8)}$[6]						HSE + HSI + PLL	1500[4]	600	400	-	1.25	1.6	1.6	1.6	1.7	mA
							1200	600	400	-	1.25	1.6	1.6	1.6	1.7	
							750	600	400	-	1.25	1.6	1.6	1.6	1.7	
							600	600	400	-	1.25	1.6	1.6	1.6	1.7	
$I_{DD\ (3V3)}$[3]	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (CStop)	SRun1	HSI	HSI 64	HSI 64	-	-	2.65	3.2	3.3	3.4	3.6	mA
						HSE + HSI	HSE 40	HSE 40	-	-	2.65	3.2	3.3	3.4	3.6	
$I_{DD\ (1V8)}$[6]						HSI	HSI 64	HSI 64	-	-	1.25	1.5	1.6	1.6	1.7	mA
						HSE + HSI	HSE 40	HSE 40	-	-	1.25	1.5	1.6	1.6	1.7	
$I_{DD\ (3V3)}$[3]	Supply current in Run mode	All peripherals Disabled	DStandby[7] [8] (CStandby)	Run2 (CRun)	SRun1	HSI	-	HSI 64	HSI 64	-	2.65	3.3	3.3	3.4	3.6	mA
$I_{DD\ (1V8)}$[6]						HSI	-	HSI 64	HSI 64	-	1.25	1.6	1.6	1.6	1.7	mA

1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*

2. *ck_icn_ddr.*
3. *Typical value given with V_{DD} = 3.3 V, maximum value given with V_{DD} = 3.6 V.*
4. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
5. *Typical value given with V_{DDGPU} = 0.91 V, maximum values given with V_{DDGPU} = 0.935 V.*
6. *Typical value given with V_{DD} = 1.8 V, maximum value given with V_{DD} = 1.89 V.*
7. *CStandby = CStop and PDDS_D1 = 1.*
8. *V_{DDCPU} is shutdown.*

Table 26. Current consumption (I_{DDA18}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions									Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 (CPU3) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDA18}	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[3]	600	400	400[4]	4.35	5	5.1	5.2	6	mA
							1200	600	400	400	3.85	4.5	4.6	4.7	4.9	
							750	600	400	400	3.25	3.9	4	4.1	4.2	
							600	600	400	400	3.1	3.7	3.8	3.9	4	
I_{DDA18}	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[3]	600	400	400[4]	4.35	5	5.1	5.2	5.4	mA
							1200	600	400	400	3.85	4.5	4.6	4.7	4.9	
							750	600	400	400	3.25	3.9	4	4.1	4.2	
							600	600	400	400	3.1	3.7	3.8	3.9	4	
I_{DDA18}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1 (CRun)	HSE + HSI + PLL	1500[3]	600	400	-	4.35	5.2	5.5	5.7	6.1	mA
							1200	600	400	-	3.9	4.7	5.1	5.2	5.6	
							750	600	400	-	3.3	4.1	4.4	4.5	4.9	
							600	600	400	-	3.15	3.9	4.3	4.3	4.7	
I_{DDA18}	Supply current in Run mode	All peripherals Disabled	DRun (CRun: P0)	Run1 (CStop)	SRun1 (CStop)	HSI	HSI 64	HSI 64	-	-	1.25	2	2.3	2.4	2.8	mA
						HSE + HSI	HSE 40	HSE 40	-	-	1.25	1.9	2.3	2.4	2.8	
I_{DDA18}	Supply current in Run mode	All peripherals Disabled	DStandby[5] [6] (CStandby)	Run2 (CRun)	SRun1 (CRun)	HSI	-	HSI 64	HSI 64	-	1.2	1.8	2	2.2	2.9	mA

1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*
2. *ck_icn_ddr.*
3. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
4. *Typical value given with V_{DDGPU} = 0.9 V, maximum values given with V_{DDGPU} = 0.961 V.*
5. *CStandby = CStop and PDDS_D1 = 1.*
6. *V_{DDCPU} is shutdown.*

Table 27. Current consumption ($I_{DDA18AON}$) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions									Typ	Max				Unit
		-	D1 (CPU1)[1] mode	D2 (CPU2) mode	D3 mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) [2]	CPU2 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1	HSE + HSI + PLL	1500[3]	600	400	400[4]	4.4	5.9	5.4	5.3	5.9	mA
							1200	600	400	400	4.4	5.9	5.4	5.3	5.1	
							750	600	400	400	4.4	5.9	5.4	5.3	5.1	
							600	600	400	400	4.4	5.9	5.4	5.3	5.1	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1	HSE + HSI + PLL	1500[3]	600	400	400[4]	4.35	5.8	5.4	5.3	5.1	mA
							1200	600	400	400	4.35	5.8	5.4	5.3	5.1	
							750	600	400	400	4.35	5.8	5.4	5.3	5.1	
							600	600	400	400	4.35	5.8	5.4	5.3	5.1	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1	HSE + HSI + PLL	1500[3]	600	400	-	4.4	5.9	5.4	5.3	5.1	mA
							1200	600	400	-	4.4	5.9	5.4	5.3	5.1	
							750	600	400	-	4.4	5.9	5.4	5.3	5.1	
							600	600	400	-	4.4	5.9	5.4	5.3	5.1	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DRun (CRun: P0&P1)	Run1 (CRun)	SRun1	HSE + HSI + PLL	1500[3]	600	400	-	4.35	5.8	5.4	5.3	5.1	mA
							1200	600	400	-	4.35	5.8	5.4	5.3	5.1	
							750	600	400	-	4.35	5.8	5.4	5.3	5.1	
							600	600	400	-	4.35	5.8	5.4	5.3	5.1	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DRun (CRun: P0)	Run1 (CStop)	SRun1	HSI	HSI 64	HSI 64	-	-	480	570	590	610	640	µA
						HSE + HSI	HSE 40	HSE 40	-	-	4.4	5.9	5.4	5.3	5.1	mA
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DRun (CRun: P0)	Run1 (CStop)	SRun1	HSI	HSI 64	HSI 64	-	-	445	530	550	560	600	µA
						HSE + HSI	HSE 40	HSE 40	-	-	4.35	5.8	5.4	5.3	5.1	mA
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DStandby[5] [6] (CStandby)	Run2 (CRun)	SRun1	HSI	-	HSI 64	HSI 64	-	490	580	590	610	640	µA

Symbol	Parameter	Conditions									Typ	Max				Unit
		-	D1 (CPU1)(1) mode	D2 (CPU2) mode	D3 mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz) (2)	CPU2 clk (MHz)	GPU clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DStandby (CStandby)(5) (6)	Run2 (CRun)	SRun1	HSI	-	HSI 64	HSI 64	-	455	530	550	560	600	µA

1. *P0 and P1 are state of cores inside CPU1 when in CRun state. 'P0&P1' indicate that both cores are executing a test software. 'P0' indicate that only P0 is executing a test software while other core is clock gated (either in WFI or WFE or not present in the device).*
2. *ck_icn_ddr.*
3. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.935 V.*
4. *Typical value given with V_{DDGPU} = 0.91 V, maximum values given with V_{DDGPU} = 0.935 V.*
5. *CStandby = CStop and PDDS_D1 = 1.*
6. *V_{DDCPU} is shutdown.*

Table 28. Current consumption (I_{BAT}) in Run modes

Evaluated by characterization, not tested in production unless otherwise specified.
V_{SW} supplied by V_{DD}.

Symbol	Parameter	Conditions	Typ	Max				Unit
		V_{BAT} voltage	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{BAT}	Supply current in Run mode (V_{DD} = 1.8 V)	V_{BAT} = 3.0 V	5	5.2	6.1	7.1	9.4	µA
		V_{BAT} = 3.3 V	5.75	5.9	6.9	8	11	
I_{BAT}	Supply current in Run mode (V_{DD}= 3.3 V)	V_{BAT} = 3.0 V	5	5.1	4.3	3.4	1.3	µA
		V_{BAT} = 3.3 V	5.7	5.8	6	6	6.1	

Table 29. Current consumption in Stop modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V

Symbol	Parameter	Conditions				Typ				Max				Unit
		D1 (CPU1) mode	D2 (CPU2) mode	D3 mode	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in Stop1 mode	DStop1 (CStop)	Stop1 (CStop)	SSTop1	-	16.5	105	180	295	58	290	430	710	mA
I_{DDCPU}						2.25	25.5	47	82.5	9.9	71	120	200	mA
I_{DDGPU}(1)						4.95	40	69.5	115	21	120	170	290	mA
I_{DD}					V_{DD} = 3.3 V(2)	2.6	2.65	2.7	2.8	3.2	3.3	3.4	3.6	mA
					V_{DD} = 1.8 V(3)	1.2	1.2	1.25	1.3	1.5	1.5	1.6	1.7	mA
I_{DDA18}					-	1.2	1.3	1.35	1.4	1.8	1.9	2	2.2	mA
$I_{DDA18AON}$					V_{DD} = 3.3 (2)	250	270	275	285	320	330	340	390	µA
					V_{DD} = 1.8 V(3)	280	300	305	315	370	370	380	430	µA
I_{DDCORE}	Supply current in Stop2 mode	DStandby (CStandby)(4) (5)	Stop2 (CStop)	SSTop1	-	16.5	105	175	295	58	290	430	700	mA
I_{DDCPU}						-(6)								-
I_{DDGPU}(1)						-(6)								-
I_{DD}					V_{DD} = 3.3 V(2)	2.65	2.7	2.7	2.8	3.2	3.3	3.4	3.5	mA
					V_{DD} = 1.8 V(3)	1.25	1.25	1.25	1.3	1.5	1.5	1.6	1.6	mA
I_{DDA18}					-	1.2	1.35	1.4	1.5	1.8	2	2.2	3	mA
$I_{DDA18AON}$					V_{DD} = 3.3 V(2)	250	265	275	285	320	320	340	380	µA
					V_{DD} = 1.8 V(3)	280	295	305	315	370	370	380	430	µA

1. *Not relevant for STM32MP231x.*
2. *typical values given for V_{DD} = 3.3 V, maximum values for V_{DD} = 3.6 V.*
3. *typical values given for V_{DD} = 1.8 V, maximum values for V_{DD} = 1.89 V.*
4. *CStandby = CStop and PDDS_D1 = 1.*
5. *V_{DDCPU} is shutdown.*
6. *Supply is OFF.*

Table 30. Current consumption in LPLV-Stop modes

Evaluated by characterization, not tested in production unless otherwise specified.
Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V and V_{DDGPU} = 0.8 V, maximum values given with V_{DDCORE} = 0.842 V, V_{DDCPU} = 0.842 V and V_{DDGPU} = 0.839 V.

Symbol	Parameter	Conditions				Typ				Max				Unit
		D1 (CPU1) mode	D2 (CPU2) mode	D3[1] mode	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in LPLV-Stop1 mode	DStop3[2] (CStop)	LPLV-Stop1[2] (CStop)	SStop2	-	16	110	190	315	120	320	490	820	mA
I_{DDCPU}						2.25	25.5	47	82.5	9.9	71	120	200	mA
I_{DDGPU}[3]						-[4]								-
I_{DD}					V_{DD} = 3.3 V[5]	2.95	5.5	7.85	12	4.6	11	15	35	mA
					V_{DD} = 1.8 V[6]	1.6	4.1	6.45	10.5	3	8.7	14	34	mA
I_{DDA18}					-	-[4]								-
$I_{DDA18AON}$					V_{DD} = 3.3 V[5]	250	270	275	285	580	330	340	650	µA
					V_{DD} = 1.8 V[6]	280	300	305	320	630	370	390	680	µA
I_{DDCORE}	Supply current in LPLV-Stop2 mode	DStandby (CStandby)[7]	LPLV-Stop2 (CStop)[2]	SStop2	-	16	110	190	315	110	320	490	810	mA
I_{DDCPU}						-[4]								-
I_{DDGPU}[3]						-[4]								-
I_{DD}					V_{DD} = 3.3 V[5]	2.9	5.45	7.8	12	4.5	11	15	35	mA
					V_{DD} = 1.8 V[6]	1.55	4.05	6.4	10.5	3	8.7	14	34	mA
I_{DDA18}					-	-[4]								-
$I_{DDA18AON}$					V_{DD} = 3.3 V[5]	250	270	275	285	580	330	340	360	µA
					V_{DD} = 1.8 V[6]	280	300	305	320	520	370	390	440	µA

1. *Domain clocked by MSI 4 MHz.*
2. *Typical value given with V_{DDCORE} = 0.67 V, maximum values given with V_{DDCORE} = 0.71 V.*
3. *Not relevant for STM32MP231x.*
4. *Supply is OFF.*

5. *Typical values given for V_{DD} = 3.3 V, maximum values for V_{DD} = 3.6 V.*
6. *Typical values given for V_{DD} = 1.8 V, maximum values for V_{DD} = 1.89 V.*
7. *CStandby = CStop and PDDS_D1 = 1.*

Table 31. Current consumption in Standby2 mode

Evaluated by characterization, not tested in production unless otherwise specified.
V_{DDCORE}, V_{DDCPU} and V_{DDGPU} are shutdown.
D3 in CStop (SStandby).

Symbol	Parameter	Conditions				Typ				Max				Unit
		RTC/LSE	BKPSRAM	RETRAM	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD}	Supply current in Standby2 mode	OFF	OFF	OFF	V_{DD} = 3.3 V(1)	2.45	4	5.55	8.25	3.2	7.4	11	17	mA
		RTC ON, LSE ON(2)				2.05	2.2	2.45	2.8	3.4	3.4	3.7	18	mA
			ON			2.05	2.3	2.5	2.9	3.3	3.3	3.8	18	mA
			OFF	ON		2.05	2.5	3.1	4.1	3.2	3.9	4.8	17	mA
			ON	ON		2.05	2.55	3.25	4.35	3.2	4.2	5.1	17	mA
	Supply current in Standby2 mode	OFF	OFF	OFF	V_{DD} = 1.8 V(3)	960	2600	4100	6750	1800	5700	8500	15000	µA
		RTC ON, LSE ON(2)				560	955	1050	1400	1700	1900	1900	17000	µA
			ON			560	960	1150	1500	1700	1800	2300	16000	µA
			OFF	ON		575	1300	1750	2700	1700	2400	3200	15000	µA
			ON	ON		600	1350	1850	2950	1700	2600	3600	15000	µA
$I_{DDA18AON}$	Supply current in Standby2 mode	OFF	OFF	OFF	V_{DD} = 3.3 V(1)	31.5	41	55.5	60	79	91	130	140	µA
					V_{DD} = 1.8 V(3)	60	80	80	90.5	110	150	160	180	µA
		RTC ON, LSE ON(2)	ON	ON	V_{DD} = 3.3 V(1)	30.5	41.5	56	60	79	93	130	140	µA
					V_{DD} = 1.8 V(3)	60	80	80	86	110	150	160	190	µA

1. *Typical values given for V_{DD} = 3.3 V, maximum values for V_{DD} = 3.6 V.*
2. *LSE is set to medium-high drive.*
3. *typical values given for V_{DD} = 1.8 V, maximum values for V_{DD} = 1.89 V.*

Table 32. Current consumption in VBAT2 mode

Evaluated by characterization, not tested in production unless otherwise specified.
D3 in CStop (SStandby).

Symbol	Parameter	Conditions				Typ				Max				Unit
		RTC/LSE	BKPSRAM	RETRAM	V_{BAT} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{BAT}	Supply current in VBAT2 mode	OFF	OFF	OFF	V_{BAT} = 2.4 V	14.5	37	47	56.5	20	69	150	210	µA
		RTC ON, LSE ON(1)				14.5	37.5	54.5	60.5	20	70	150	215	µA
			ON			17.5	66.5	100	190	27	150	310	440	µA
			OFF	ON		38.5	330	660	1250	82	780	1600	2900	µA
			ON	ON		44	385	770	1450	97	910	1800	3300	µA
I_{BAT}	Supply current in VBAT2 mode	OFF	OFF	OFF	V_{BAT} = 3.0 V	17.5	40.5	49.5	58.5	23	73	150	215	µA
		RTC ON, LSE ON(1)				17.5	41	58	64.5	23	74	160	220	µA
			ON			20.5	69.5	105	195	31	150	310	440	µA
			OFF	ON		41.5	335	665	1300	85	780	1600	2900	µA
			ON	ON		47	385	775	1500	100	910	1800	3300	µA
I_{BAT}	Supply current in VBAT2 mode	OFF	OFF	OFF	V_{BAT} = 3.3 V	20	43.5	52	60	26	76	160	220	µA
		RTC ON, LSE ON(1)				20	43.5	61	67.5	25	76	160	230	µA
			ON			22.5	72.5	110	200	33	160	320	450	µA
			OFF	ON		43.5	335	670	1300	87	780	1600	2900	µA
			ON	ON		49	390	775	1500	110	920	1800	3300	µA
I_{BAT}	Supply current in VBAT2 mode	OFF	OFF	OFF	V_{BAT} = 3.6 V	24	47.5	58	67.5	30	92	190	260	µA
		RTC ON, LSE ON(1)				24.5	47.5	61	73	30	91	190	270	µA
			ON			27	87.5	135	240	37	170	350	490	µA
			OFF	ON		48.5	350	690	1300	92	800	1600	2900	µA
			ON	ON		53.5	405	800	1500	110	930	1800	3400	µA

1. *LSE is set to medium-high drive.*

6.3.5.2 *I/O system current consumption*

The current consumption of the I/O system has two components: static and dynamic.

6.3.5.3 *I/O static current consumption*

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in .

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: *Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.*

6.3.5.4 *I/O dynamic current consumption*

The I/Os used by an application contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin.

The theoretical formula is provided below:

$$I_{SW} = V_{DD} \times f_{SW} \times C_L$$

where

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DDx} is the MCU supply voltage
- f_{SW} is the I/O switching frequency
- C_L is the total capacitance seen by the I/O pin: C = CINT + CEXT

6.3.6 Wake-up time from low-power modes

The wake-up times given in Table 33 , Table 34 and Table 35 are measured starting from the wake-up event trigger up to the first instruction executed by the CPU1 or CPU2:

- the CPU1 or CPU2 goes in low-power mode after WFI (wait for interrupt) instruction.
- For CSleep modes:
  - Interrupt to GIC or NVIC is used to wake-up from low-power modes.
- For CStop modes (except Standby and V_{BAT}):
  - For CPU1 and CPU2: EXTI1[x] is used to wake-up from low-power modes.
- For Standby modes:
  - WKUPx is used to wake up from low-power modes.
- For V_{BAT} modes
  - TAMP_INx is used to wake up from low-power modes.
- System mode is equal to D2 domain mode

All timings are derived from tests performed under ambient temperature and V_{DD} = 3.3 V.

General conditions unless otherwise noted:

- CPU1 software in SYSRAM
- CPU2 software in SRAMx
- HSE is 40 MHz
- When HSI is used, HSIKERON = 0
- PWRLP_DLY = 0

- LPLVDLY_D2 = 187 µs
- $t_{WUCSleep}$ values are measured with internal interrupt
- $t_{WUCStop}$ and $t_{WULPLV\text{-}Stop}$ values are measured with EXTI pin
- $t_{WUStandby}$ values are measured with WKUP pin through PWR
- When V_{DDCORE} or V_{DDCPU} are shutdown or reduces, wake-up time value depend on supply characteristics.
  - Wake-up time in following tables are measured with 200 µs V_{DDCORE} and V_{DDCPU} setup time
  - Longer V_{DDCPU} or V_{DDCORE} startup time than 200 µs should be added to the wake-up time value
  - When voltage is reduced, V_{DDCORE} is assumed to be back to nominal value before LPLVDLY_D2 expiration. Otherwise, LPLVDLY_D2 value should be increased accordingly and this directly impact wake-up time value.

Table 33. D1 (CPU1) low-power mode wake-up timings

Evaluated by characterization, not tested in production. Unless otherwise noted.

Symbol	D1 (CPU1) mode	D2 (CPU2) mode	D3 (CPU3) mode	Conditions for wake-up domain	Typ	Max	Unit
$t_{WUCSleep_CPU1}$	DRun (CSleep)	Run1 (CStop)	(Reset)	SEV between CPU1 cores	-	15	CPU1 clock cycles
				HSI	-	12 + 20	$T_{ck_icn_nic}$ + $T_{ck_cpu1_ext}2f$
				HSE + PLL1	-	12 + 20	$T_{ck_icn_nic}$ + T_{PLL1}
	DRun (eCSleep)(1)	Run1 (CStop)	(Reset)	HSE + PLL1	-	12 + 20	$T_{ck_icn_nic}$ + $T_{ck_cpu1_ext}2f$
$t_{WUCStop_CPU1}$	DStop1 (CStop)	Run1 (CRun)	(Reset)	HSI 64 MHz	8.2	10	µs
				HSE + PLL1 1200 MHz	180	-	µs
	DStop1 (CStop)(2)	Stop1 (CStop)(2)	(Reset)	HSI 64 MHz(3)	3.3	15	µs
				HSI 64 MHz	8.2	10	µs
				HSE + PLL1 1200 MHz	180	-	µs
	DStandby (CStop)(4)	Stop2 (CStop)(2)	(Reset)	HSI 64 MHz(3)(5)	660	-	µs
$t_{WULPLV\text{-}Stop_CPU1}$	DStop3 (CStop)(2)(6)	LPLV-Stop1 (CStop)(2)(6)	(Reset)	HSI 64 MHz, PWRLP_DLY = 100 us	1000	1200	µs
	DStandby (CStop)(4)(6)	LPLV-Stop2 (CStop)(2)(6)	(Reset)	HSI 64 MHz(5)	1500 (1000)	-	µs(7)

1. *eCSleep mean CPU1 in enhanced CSleep with PLL1 automatically stopped (RCC_C1SREQSETR.ESLPREQ = 1). In this mode, CPU1 wake on ck_cpu1_ext2f, then CPU1 switch back automatically to PLL1 after PLL lock time.*
2. *PDDS_Dx = 0.*
3. *HSI active (HSIKERON = 1).*
4. *PDDS_Dx = 1.*
5. *CPU1 wake-up address register points to SYSRAM code.*
6. *LPDS_Dx=1 and LVDS_Dx = 1.*
7. *Value in parenthesis is for wake-up using WKUP pin through PWR.*

Table 34. D2 (CPU2) low-power mode wake-up timings

Evaluated by characterization, not tested in production. Unless otherwise noted.

Symbol	D1 (CPU1) mode	D2 (CPU2) mode	D3 (CPU3) mode	Conditions for wake-up domain	Typ	Max	Unit
$t_{WUCSleep_CPU2}$[1]	DStop1 (CStop)	Run1 (CSleep)	(Reset)	-	-	14	CPU2 clock cycles
$t_{WUCStop_CPU2}$	DRun (CRun)	Run1 (CStop)	(Reset)	HSI 64 MHz	-	1.2	µs
				HSE + PLL 400 MHz	180	-	µs
	DStop1 (CStop)[2]	Stop1 (CStop)[2]	(Reset)	HSI 64 MHz[3]	2.7	6.2	µs
				HSI 64 MHz	7.6	-	µs
				HSE + PLL 400 MHz	180	-	µs
$t_{WULPLV\text{-}Stop_CPU2}$	DStop3 (CStop)[2][4]	LPLV-Stop1 (CStop)[2][4]	(Reset)	HSI 64 MHz[5]	900	1200	µs
				HSI 64 MHz[6]	1000	1300	µs
	DStandby (CStop)[4][7]	LPLV-Stop2 (CStop)[2][4]	(Reset)	HSI 64 MHz	1500 (900)[8]	-	µs
$t_{WUStandby_CPU2}$	DStandby (CStop)[9]	Standby2 (CStop)[9]	(Reset)[9]	HSI 64 MHz, RETRAM	1700 (800)[10]	-	µs

1. *Specified by design, not tested in production.*
2. *PDDS_Dx = 0.*
3. *HSI active (HSIKERON = 1).*
4. *LPDS_Dx = 1 and LVDS_Dx = 1.*
5. *CPU2TMPSKP = 1 or PWRLP_DLY = 0.*
6. *CPU2TMPSKP = 0 and PWRLP_DLY = 100 µs.*
7. *PDDS_Dx = 1*
8. *Value in parenthesis is for wake-up using WKUP pin through PWR or wake-up using EXTI without simultaneous CPU1 wake-up.*
9. *PDDS_Dx = 1.*
10. *Value in parenthesis is for RAMCFG_RETRAMCCR1.CRCBS[2:0] = 0 (only 16 Kbytes RETRAM CRC check).*

Table 35. Wake-up time using USART/LPUART

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wake-up time needed to calculate the maximum USART/ LPUART baud rate allowing the wake-up from low-power mode	Stop1/2 HSI clock with HSIKERON = 0	-	6.4	µs
$t_{WULPUART_LPLV}$	Wake-up time needed to calculate the maximum LPUART baud rate allowing the wake-up from low-power mode	LPLV-Stop1/2 MSI clock with MSIKERON = 0	-	580	µs

6.3.7 External clock source characteristics

6.3.7.1 High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

Digital and analog bypass modes are available.

The external clock signal has to respect the Table 59. I/O static characteristics. However, the recommended clock input waveform is shown in Figure 13 for digital bypass mode and in Figure 14 for analog bypass mode. In analog bypass mode the clock can be a sinusoidal waveform.

Table 36. High-speed external (HSE) user clock characteristics (digital bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	-	16	40	48	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	-	$0.7 \times V_{DDA18AON}$	-	$V_{DDA18AON}$	V
V_{HSEL}	OSC_IN input pin low level voltage	-	-	V_{SS}	-	$0.3 \times V_{DDA18AON}$	
$t_{W(HSE)}$	OSC_IN high or low time	-	-	7	-	-	ns

Figure 13. High-speed external clock source AC timing diagram (digital bypass)

Table 37. High-speed external (HSE) user clock characteristics (analog bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	16	40	48	MHz
	Input duty cycle (square wave)	-	45	50	55	%
	duty cycle deterioration[1]	-	-	± 10[2]	±30[3]	%
V_{HSE}	Absolute input range	-	0	-	$V_{DDA18AON}$	V
V_{PP}	OSC_IN peak-to-peak amplitude	-	0.2[4]	-	$0.67 \times V_{DDA18AON}$	
$t_{SU(HSE)}$	Time to start[5]	-	-	1	10[6]	µs
$tr/tf_{(HSE)}$	Rise and Fall time (10% to 90% threshold levels of the input peak-to-peak amplitude)	-	$0.05 \times T_{HSE}$	-	$0.3 \times T_{HSE}$	ns

1. *Specified by design, not tested in production.*
2. *With a square wave signal (at 25 °C, $V_{DDA18AON}$ = 1.8 V / VPP = 400 mV / VDC = 0.8 V) where VDC is the DC component of the input signal.*
3. *With a square wave signal (at 25 °C, $V_{DDA18AON}$ = 1.71 V / VPP = 200 mV / VDC = 0.8 V) where VDC is the DC component of the input signal.*
4. *Minimum peak-to-peak amplitude (at 25 °C, 0.1 < VDC < $V_{DDA18AON}$ - 0.1 V) where VDC is the DC component of the input signal.*
5. *Startup time measured from the moment it is enabled (by software) to a stabilized analog bypass clock interface is reached.*
6. *Maximum start-up time is obtained with 200 mV peak-to-peak amplitude.*

Figure 14. High-speed external clock source AC timing diagram (analog bypass)

6.3.7.2 *Low-speed external user clock generated from an external source*

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the Table 59. I/O static characteristics. However, the recommended clock input waveform is shown in Figure 15 for digital bypass and Figure 16 for analog bypass.

Table 38. Low-speed external (LSE) user clock characteristics (digital bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}(1)	User external clock source frequency	-	-	32.768	-	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.75 × V_{SW}	-	V_{SW}(2)	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.25 × V_{SW}	
$t_{W(LSE)}$	OSC32_IN high or low time	-	250	-	-	ns

1. *Specified by design, not tested in production.*
2. *V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*

Figure 15. Low-speed external clock source AC timing diagram (digital bypass)

Table 39. Low-speed external (LSE) user clock characteristics (analog bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}[1]	User external clock source frequency	-	-	32.768	-	kHz
V_{LSE}	Absolute input range	-	0	-	V_{SW}[2]	V
V_{PP}	OSC32_IN peak-to-peak amplitude	-	0.2[3]	1	-	

1. *Specified by design, not tested in production.*
2. *V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*
3. *Minimum peak-to-peak amplitude (at 25 °C, 0.1 < VDC < V_{SW} - 0.1 V) where VDC is the DC component of the input signal.*

Figure 16. Low-speed external clock source AC timing diagram (analog bypass)

6.3.7.3 *High-speed external clock generated from a crystal/ceramic resonator*

The high-speed external (HSE) clock can be supplied with a 16 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 40 . In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. High-speed external (HSE) oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}[1]	Crystal frequency	-	16	40	48	MHz
R_F[1]	Internal feedback equivalent resistor	-	-	250	-	kΩ
$I_{VDDA18AON(HSE)}$	HSE current consumption on $V_{DDA18AON}$	During startup	-	-	10	mA
		Rm = 80 Ω, CL = 6 pF at 40 MHz[3]	-	4.6	-	
$Gm_{critmax}$[1]	Maximum critical crystal gm	Startup	-	-	1.95	mA/V
t_{SU}	Start-up time[4]	-	-	2	-	ms

1. *Specified by design, not tested in production.*
2. *This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.*
3. *Resonator characteristics given by the crystal/ceramic resonator manufacturer.*

4. *Measured from the moment it is enabled (by software) to a stabilized 40 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 17). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. The PCB and pin capacitance must be included (4 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

Figure 17. Typical application with a 40 MHz crystal

6.3.7.4 *Low-speed external clock generated from a crystal/ceramic resonator*

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 41 . In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 41. Low-speed external (LSE) oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE} (1)	Oscillator frequency	-	-	32.768	-	kHz
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 10, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 01, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU} (2)	Startup time	V_{SW} is stabilized	-	2	-	s

1. *Specified by design, not tested in production.*
2. *t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal

1. *Adding an external resistor between OSC32_IN and OSC32_OUT is forbidden.*

6.3.8 External clock source security characteristics

Table 42. High-speed external user clock security system (HSE CSS)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DCM(HSE_CSS)}$	Time to detect clock missing	f_{HSE} = 48 MHz	-	1	2	µs

Table 43. Low-speed external user clock security system (LSE CSS)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DCM(LSE_CSS)}$	Time to detect clock missing	-	-	-	300	µs
$f_{MAX(LSE_CSS)}$	Cut-off frequency	-	-	-	2	MHz

6.3.9 Internal clock source characteristics

The parameters given in Table 44 , Table 45 and Table 46 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions .

6.3.9.1 64 MHz high-speed internal RC oscillator (HSI)

Table 44. HSI oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}[(1)]	HSI frequency	$V_{DDA18AON}$ = 1.8 V, T_J = 30 °C	63.68	64	64.32	MHz
TRIM	HSI trimming step	-	-	0.25	0.5	%
DuCy(HSI)	Duty Cycle	-	40	-	60	%
$\Delta V_{DDA18AON(HSI)}$ + ΔT_J(HSI)	HSI oscillator frequency drift over voltage and temperature variation (after factory calibration)[(2)]	T_J = -40 to 125 °C	-8.5	-	+8.5	%
$t_{su(HSI)}$	HSI oscillator start-up time (Time between Enable rising and First output clock edge.)	-	-	-	3	µs
$t_{stab(HSI)}$	HSI oscillator stabilization time	At 1% of target frequency	-	-	5	µs
$I_{VDDCORE(HSI)}$	HSI supply current on V_{DDCORE}	-	-	-	10	µA
$I_{VDD18AON(HSI)}$	HSI supply current on $V_{DDA18AON}$	-	-	300	400	µA

1. *Guaranteed by test in production.*

2. *If better tolerance is needed (for example for UART kernel clock usage), the HSI could be trimmed during run time by measuring its frequency with a better reference like HSE crystal. The HSI trimming should be done regularly or whenever there is significant variation on supply voltage or temperature.*

6.3.9.2 *4/16 MHz low-power internal RC oscillator (MSI)*

Table 45. MSI oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	CSI frequency	V_{DDCORE} = 0.82 V, T_J = 30 °C	MSIFREQSEL=0[1]	3.956	4	4.044	MHz
			MSIFREQSEL=1	15.824	16	16.176	
TRIM	MSI trimming step	Trimming Code is not a multiple of 32		-	0.8	1.1	%
		Trimming Code is a multiple of 32		-	-2.5	-3.8	
DuCy(MSI)	Duty Cycle	At trimmed frequency		45	-	55	%
ΔT_J(MSI)	MSI oscillator frequency drift over temperature	T_J = -40 °C to 70 °C		-5	-	+5	%
		T_J = -40 °C to 125 °C		-6	-	+6	
$t_{su(MSI)}$	MSI oscillator start-up time	-		-	-	3.5	µs
$I_{VDDCORE(MSI)}$	MSI Supply current on V_{DDCORE}	at 4 MHz	MSIFREQSEL = 0	-	20	22	µA
		at 16 MHz	MSIFREQSEL = 1	-	60	68	

1. *Guaranteed by test in production.*

6.3.9.3 *32 kHz low-speed internal (LSI) RC oscillator*

Table 46. LSI oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	T_J = 30 °C[1]	30.5	32	33.5	kHz
		T_J= -40 to 125° C	28.8	32	33.6	
$t_{su(LSI)}$	LSI oscillator start-up time (time between enable rising and first output clock edge.)	-	-	-	180	µs
$I_{VSW(LSI)}$	LSI supply current on V_{SW}[2]	-	-	250	500	nA

1. *Guaranteed by test in production.*
2. *V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*

6.3.10 PLL characteristics

The parameters given in Table 47 , Table 48 , Table 49 and Table 50. PLL_LVDS characteristics are derived from tests performed under temperature and supply voltage conditions summarized in Table 17. General operating conditions .

Table 47. PLL1 to PLL8 characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Normal mode	5	-	64	MHz
		Sigma delta mode	10	-	64	
-	PLL input clock duty cycle	-	TBD	-	TBD	%

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PFD}	PFD input clock	Normal mode		5	f_{PLL_IN}/ FREFDIV	50	MHz
		Sigma delta mode		10	-	min(50, f_{VCO}/20)	
$f_{FOUTPOSTDIV}$	Divided output clock	-		16.32	-	3200	MHz
	Divided output clock duty cycle	Division by 1		48	50	52	%
		Even Division		48	50	52	
		Odd Division		47	50	53	
f_{VCO}	PLL VCO output	-		800	-	3200	MHz
t_{LOCK}	PLL lock time	Frequency lock		-	-	400	1/f_{PFD} cycles
		f_{PFD} = 40 MHz (f_{PLL_IN} = 40 MHz, FREFDIV = 1)		-	-	10	µs
Jitter	RMS period jitter	f_{VCO} = 3200 MHz		-	-	0.26	+/_ps
	RMS integrated jitter (10 kHz - 20 MHz)	f_{VCO} = 3200 MHz, F_{PFD} = 25 MHz	Integer divider	-	±2.7	±6.6	ps
			fracN divider	-	-	±11.9	
$I_{VDDA18PLL}$[1]	PLL supply current on $V_{DDA18PLL}$ (Analog)	f_{VCO} = 3200 MHz	FBDIV < 256	-	5750	6850	µA
			FBDIV > 255	-	7050	8450	
		f_{VCO} = 800 MHz	FBDIV < 256	-	715	860	
$I_{VDDCORE(PLL)}$[1]	PLL supply current on V_{DDCORE} (Digital)	f_{VCO} = 3200 MHz	V_{DDCORE} = 0.82 V	-	1200	3650	
		f_{VCO} = 800 MHz		-	295	910	

1. *Evaluated by characterization, not tested in production.*

Table 48. PLL_USB characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Only those 3 values (min, typ or max) are possible	19.2	20	38.4	MHz
f_{PLL_OUT}	PLL output clock	-	-	480	-	MHz

Table 49. PLL_DSI characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	-	2	-	64	MHz
f_{PLL_INFIN}	PFD input clock	-	-	2	-	24	
f_{PLL_OUT}	PLL output clock	-	-	40	-	1250	
f_{VCO_OUT}	PLL VCO output	-	-	320	-	1250	
t_{LOCK}	PLL lock time[1]	-	-	-	-	150	µs
t_{PDN}	PLL power down time	-	-	0.1	-	-	

1. *Evaluated by characterization, not tested in production.*

Table 50. PLL_LVDS characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-	-	3	-	24	MHz
f_{PLL_INFIN}	PFD input clock	-	-	3	-	24	
f_{PLL_OUT}	PLL output clock	-	-	-	-	1100	
f_{VCO_OUT}	PLL VCO output	-	-	1800	2200	3000	
t_{LOCK}(1)	PLL lock time	-	-	-	-	355	µs
f_{Mod}	Modulation frequency	-	-	-	33	-	kHz
md	Modulation depth	-	-	-	0.25	5	%
$I_{VDDA18LVDS}$(1)	PLL supply current on $V_{DDA18LVDS}$	-	-	-	4.9	-	mA
$I_{VDDLVDS}$(1)	PLL supply current on V_{DDLVDS}	-	-	-	1.4	-	mA

1. *Evaluated by characterization, not tested in production.*

6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows the reduction of electromagnetic interferences (see Section 6.3.13.4). It is available only on the PLL2 to PLL8.

Table 51. PLL2 to PLL8 SSCG parameters constraints

Specified by design, not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
F_{MOD}	Modulation frequency	5.2	-	391	kHz
M_D	Peak modulation depth	0.1	-	3.1	%

6.3.12 Memory characteristics

6.3.12.1 OTP characteristics

The characteristics are given at T_J = -40 to 125 °C unless otherwise specified.

Table 52. OTP characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OTP(VDDA18AON)}$	OTP supply current on $V_{DDA18AON}$	Programming	-	3.8	10	mA
		Reading	-	0.66	1.13	
		PowerDown	-	5	132	µA
$I_{OTP(VDDCORE)}$	OTP supply current on V_{DDCORE}	Programming	-	0.09	0.45	mA
		Reading	-	1.8	3.6	
		PowerDown	-	8	500	µA

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

6.3.13.1 Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: a burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in Table 53 . They are based on the EMS levels and classes defined in application note AN1709 available from the ST website www.st.com.

Table 53. EMS characteristics

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, TA = +25 °C, largest package, F_{PLL1} = 1200 or 1500 MHz, $F_{ck_icn_hs_mcu}$ = 400 MHz, Cortex-M33 core not running, conforms to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance		5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the device pins exposed to noise (connected to tracks longer than 50 mm on PCB).

6.3.13.2 *Designing hardened software to avoid noise problems*

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

6.3.13.3 *Software recommendations*

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (such as control registers)

See also application note AN1015.

6.3.13.4 *Electromagnetic Interference (EMI)*

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 54. EMI characteristics for f_{HSE} = 40 MHz and F_{PLL1} = 1200 MHz

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak[1]	V_{DD} = 3.6 V, TA = 25 °C, largest package, $F_{ck_icn_hs_mcu}$ = 400 MHz, Cortex-M33 core not running, conforming to IEC61967-2	0.1 MHz to 30 MHz	14	dBµV
			30 MHz to 130 MHz	9	
			130 MHz to 1 GHz	21	
			1 GHz to 2 GHz	8	
	Level[2]		0.1 MHz to 2 GHz	3	-

1. *Refer to AN1709 "EMI radiated test" section.*
2. *Refer to AN1709 "EMI level classification" section.*

Table 55. EMI characteristics for f_{HSE} = 40 MHz and F_{PLL1} = 1500 MHz

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak[1]	V_{DD} = 3.6 V, TA = 25 °C, largest package, $F_{ck_icn_hs_mcu}$ = 400 MHz, Cortex-M33 cores not running, conforming to IEC61967-2	0.1 MHz to 30 MHz	-	dBµV
			30 MHz to 130 MHz	-	
			130 MHz to 1 GHz	-	
			1 GHz to 2 GHz	-	
	Level[2]		0.1 MHz to 2 GHz	-	-

1. *Refer to AN1709 "EMI radiated test" section.*
2. *Refer to AN1709 "EMI level classification" section.*

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

6.3.14.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 56. ESD absolute maximum ratings

Evaluated by characterization, not tested in production.

Symbol	Ratings	Conditions	Packages	Class	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001.	All	2	2000[1]	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All	C1	250	V

1. *330 V for UCPD IOs.*

6.3.14.2 Static latchup

Two complementary static tests are required on three parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Table 57. Electrical sensitivities

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Class
LU	Static latchup class	T_A = +25 °C conforming to JESD78	II level A

6.3.15 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} should be avoided during the normal product operation. However, in order to give an indication of the robustness of the device in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

6.3.15.1 *Functional susceptibility to I/O current injection*

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter:

- ADC error above a certain limit: higher than 5 LSB total unadjusted error (TUE),
- Out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range)
- Other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 58. I/O current injection susceptibility

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Description	Negative Injection	Positive Injection	Unit
IINJ	ANA0, ANA1	5	0	mA
	OSC32_IN, OSC32_OUT, PC13, PI8, PZ0, PZ1, PZ2, PZ3, PZ4, PZ5, PZ6, PC3, PC4, PC5, PF6, PF7, PG1, PG3	0	NA	
	All other digital I/Os	5	NA	

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 59. I/O static characteristics are derived from tests performed under the conditions summarized in Table 17. General operating conditions. All I/Os are CMOS and TTL compliant.

Table 59. I/O static characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low voltage	2.7 < V_{DDx} < 3.6 V	-	-	0.3 × V_{DDx}	V
		1.71 <V_{DDx} < 1.89 V	-	-	0.35 × V_{DDx}	V
V_{IH}(1)	I/O input high voltage	2.7 < V_{DDx} < 3.6 V	0.7 × V_{DDx}	-	-	V
		1.71 < V_{DDx} < 1.89 V	0.65 × V_{DDx}	-	-	V
V_{IL}(2)	I/O input low voltage	2.7 < V_{DDx} < 3.6 V	-	-	0.4 × V_{DDx} - 0.27	V
		1.71 < V_{DDx} < 1.89 V	-	-	0.36 × V_{DDx}	V
V_{IH}(2)	I/O input high voltage	2.7 <V_{DDx} < 3.6 V	0.52 × V_{DDx} - 0.11	-	-	V
		1.71 < V_{DDx} < 1.89 V	0.62 × V_{DDx}	-	-	V
VHYS	I/O input hysteresis	2.7 < V_{DDx} < 3.6 V	-	0.44	-	V
		1.71 <V_{DDx} < 1.89 V	-	0.44	-	V
I_{leak}	TT_x input leakage		-	50	10000	nA
I_{VDDx}	Static current consumption on V_{DDx}		-	40	2000	nA
$I_{VDDA18AON}$	Static current consumption on $V_{DDA18AON}$		-	2	80	nA
$I_{VDDCORE}$	Static current consumption on V_{DDCORE}		-	1	180	nA
R_{PU}	Weak pull-up equivalent resistor(3)	2.7 < V_{DDx} < 3.6 V	30	40	50	kΩ
		1.71 < V_{DDx} < 1.89 V	30	40	50	kΩ

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{PD}	Weak pull-down equivalent resistor[3]	$2.7 < V_{DDx} < 3.6$ V	30	40	50	kΩ
		$1.71 < V_{DDx} < 1.89$ V	30	40	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. *Guaranteed by testing.*
2. *Specified by design, not tested in production.*
3. *The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).*

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for TT I/Os is shown in Figure 19.

Figure 19. V_{IL}/V_{IH} for TT I/Os

6.3.16.1 *Output driving current*

The GPIOs (general purpose input/outputs) can sink or source up to ±20 mA (depending on speed setup, supply voltage range and temperature).

In the user application, I/O drive current must be limited to respect the absolute maximum rating specified in Section 6.2, in particular:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run mode consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see Table 15).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run mode consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see Table 15).

6.3.16.2 *Output voltage levels*

Unless otherwise specified, the parameters given in Table 60 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions. All I/Os are CMOS and TTL compliant.

Table 60. Output voltage characteristics for all I/Os

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions[1] [2] [3] [4]	Min	Max	Unit
V_{OL}	Output low level voltage (3.3 V range, 2.7 < V_{DDx} < 3.6 V)	I_{IO} = 6.5 mA, Speed = 0b00	-	0.4	V
		I_{IO} = 10 mA, Speed = 0b01	-	0.4	
		I_{IO} = 13 mA, Speed = 0b10	-	0.4	
		I_{IO} = 20 mA, Speed = 0b11	-	0.4	
V_{OH}	Output high level voltage (3.3 V range, 2.7 < V_{DDx} < 3.6 V)	I_{IO} = 6.5 mA, Speed = 0b00	V_{DDx} - 0.4	-	V
		I_{IO} = 10 mA, Speed = 0b01	V_{DDx} - 0.4	-	V
		I_{IO} = 13 mA, Speed = 0b10	V_{DDx} - 0.4	-	V
		I_{IO} = 20 mA, Speed = 0b11	V_{DDx} - 0.4	-	V
V_{OL}	Output low level voltage (1.8 V range, 1.71 < V_{DDx} < 1.89 V)	I_{IO} = 5.5 mA, Speed = 0b00	-	0.4	V
		I_{IO} = 8 mA, Speed = 0b01	-	0.4	V
		I_{IO} = 11 mA, Speed = 0b10	-	0.4	V
		I_{IO} = 16 mA, Speed = 0b11	-	0.4	V
V_{OH}	Output high level voltage (1.8 V range, 1.71 < V_{DDx} < 1.89 V)	I_{IO} = 5.5 mA, Speed = 0b00	V_{DDx} - 0.4	-	V
		I_{IO} = 8m A, Speed = 0b01	V_{DDx} - 0.4	-	V
		I_{IO} = 11 mA, Speed = 0b10	V_{DDx} - 0.4	-	V
		I_{IO} = 16 mA, Speed = 0b11	V_{DDx} - 0.4	-	V

1. *110 <T_J < 120: 4 mA.*
2. *90 < T_J < 110: 10 mA.*
3. *T_J < 90: 20 mA.*
4. *Maximum current depend on temperature.*

6.3.16.3 *Output buffer timing characteristics*

Table 61. Output timing characteristics (V_{DD} = 3.0 - 3.6 V or V_{DDIOx} = 2.7 - 3.6 V, VDDIOxVRSEL = 0)

Evaluated by characterization, not tested in production unless otherwise specified.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax[1]	Maximum frequency	C = 50 pF	-	30	MHz
			C = 40 pF	-	35	
			C = 30 pF	-	45	
			C = 20 pF	-	67	
			C = 10 pF	-	110	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	11.7	ns
			C = 40 pF	-	9.5	
			C = 30 pF	-	7.3	
			C = 20 pF	-	5.2	
			C = 10 pF	-	3	
0b01	Fmax[1]	Maximum frequency	C = 50 pF	-	45	MHz
			C = 40 pF	-	55	
			C = 30 pF	-	70	

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b01	Fmax[1]	Maximum frequency	C = 20 pF	-	100	MHz
			C = 10 pF	-	166	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	8.1	ns
			C = 40 pF	-	6.7	
			C = 30 pF	-	5.2	
			C = 20 pF	-	3.6	
			C = 10 pF	-	2.2	
0b10[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	60	MHz
			C = 40 pF	-	75	
			C = 30 pF	-	100	
			C = 20 pF	-	133	
			C = 10 pF	-	190	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	6.3	ns
			C = 40 pF	-	5.1	
			C = 30 pF	-	4	
			C = 20 pF	-	2.9	
			C = 10 pF	-	1.8	
0b11[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	80	MHz
			C = 40 pF	-	100	
			C = 30 pF	-	120	
			C = 20 pF	-	166	
			C = 10 pF	-	220	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	4.4	ns
			C = 40 pF	-	3.7	
			C = 30 pF	-	2.9	
			C = 20 pF	-	2.2	
			C = 10 pF	-	1.5	

1. *The maximum frequency is defined with the following conditions : (Tr + Tf) ≤ 2/3 T and Skew ≤ 1/20 T and 45% < Duty cycle < 55%.*
2. *The fall and rise time are defined respectively between 90% and 10%, and between 10% and 90% of the output waveform.*
3. *IO compensation enabled.*

Table 62. Output timing characteristics (V_{DD}/V_{DDIOx} = 1.71 - 1.89 V, VDDIOxVRSEL = 1)

Evaluated by characterization, not tested in production unless otherwise specified.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax[1]	Maximum frequency	C = 50 pF	-	30	MHz
			C = 40 pF	-	35	
			C = 30 pF	-	45	
			C = 20 pF	-	67	
			C = 10 pF	-	110	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	11	ns
			C = 40 pF	-	9	

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 30 pF	-	7	ns
			C = 20 pF	-	5	
			C = 10 pF	-	3	
0b01	Fmax[1]	Maximum frequency	C = 50 pF	-	45	MHz
			C = 40 pF	-	55	
			C = 30 pF	-	70	
			C = 20 pF	-	100	
			C = 10 pF	-	166	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	7.4	ns
			C = 40 pF	-	6.1	
			C = 30 pF	-	4.7	
			C = 20 pF	-	3.4	
			C = 10 pF	-	2.1	
0b10[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	60	MHz
			C = 40 pF	-	75	
			C = 30 pF	-	100	
			C = 20 pF	-	133	
			C = 10 pF	-	200	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	5.7	ns
			C = 40 pF	-	4.7	
			C = 30 pF	-	3.7	
			C = 20 pF	-	2.7	
			C = 10 pF	-	1.7	
0b11[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	80	MHz
			C = 40 pF	-	100	
			C = 30 pF	-	120	
			C = 20 pF	-	166	
			C = 10 pF	-	250	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	4.1	ns
			C = 40 pF	-	3.4	
			C = 30 pF	-	2.7	
			C = 20 pF	-	2	
			C = 10 pF	-	1.3	

1. *The maximum frequency is defined with the following conditions : (Tr + Tf) ≤ 2/3 T and Skew ≤ 1/20 T and 45% < Duty cycle < 55%.*
2. *The fall and rise time are defined respectively between 90% and 10%, and between 10% and 90% of the output waveform.*
3. *IO compensation enabled.*

Table 63. Output timing characteristics (V_{DD}/V_{DDIOx} = 1.71 - 1.89 V, VDDIOxVRSEL = 0 degraded mode)

Evaluated by characterization, not tested in production unless otherwise specified.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax[1]	Maximum frequency	C 50 pF	-	10	MHz

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax[1]	Maximum frequency	C = 40 pF	-	15	MHz
			C = 30 pF	-	20	
			C = 20 pF	-	33	
			C = 10 pF	-	45	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	30.2	ns
			C = 40 pF	-	24.4	
			C = 30 pF	-	18.7	
			C = 20 pF	-	13	
			C = 10 pF	-	7.4	
0b01	Fmax[1]	Maximum frequency	C = 50 pF	-	15	MHz
			C = 40 pF	-	20	
			C = 30 pF	-	25	
			C = 20 pF	-	37	
			C = 10 pF	-	60	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	21.1	ns
			C = 40 pF	-	17.2	
			C = 30 pF	-	13.3	
			C = 20 pF	-	9.4	
			C = 10 pF	-	5.5	
0b10[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	20	MHz
			C = 40 pF	-	25	
			C = 30 pF	-	30	
			C = 20 pF	-	45	
			C = 10 pF	-	75	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	17	ns
			C = 40 pF	-	13.9	
			C = 30 pF	-	10.8	
			C = 20 pF	-	7.8	
			C = 10 pF	-	4.5	
0b11[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	30	MHz
			C = 40 pF	-	35	
			C = 30 pF	-	45	
			C = 20 pF	-	60	
			C = 10 pF	-	85	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	11.8	ns
			C = 40 pF	-	9.8	
			C = 30 pF	-	7.9	
			C = 20 pF	-	5.8	
			C = 10 pF	-	3.8	

1. *The maximum frequency is defined with the following conditions : (Tr + Tf) ≤ 2/3 T and Skew ≤ 1/20 T and 45% < Duty cycle < 55%.*
2. *The fall and rise time are defined respectively between 90% and 10%, and between 10% and 90% of the output waveform.*

3. IO compensation enabled.

Table 64. GPIO advance config delay characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	0	-	0.05	ps
t_{Δ}	Unit Delay	-	-	0.25	-	

6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see Table 59. I/O static characteristics).

Unless otherwise specified, the parameters given in Table 65 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions.

Table 65. NRST pin characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RPU(1)	Weak pull-up equivalent resistor	-	30	40	50	kΩ
tGEN	NRST minimum generated output pulse	-	17.5	-	-	µs
TFILT	NRST input filtered pulse	-	-	-	50	ns
TNFILT	NRST input not filtered pulse	-	150	-	-	ns

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 20. Recommended NRST pin protection

1. The reset network protects the device against parasitic resets.

2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 65. Otherwise the reset is not taken into account by the device.

6.3.18 DDR IOs characteristics

Refer to JEDEC standards for more details and characteristics

- DDR3L: JESD79-3F with addendum JESD79-3-1A
- DDR4: JESD79-4D
- LPDDR4: JESD209-4D

6.3.19 FMC characteristics

Unless otherwise specified, the parameters given in Table 66 to Table 79 for the FMC interface are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 × V_{DD}

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output characteristics.

6.3.19.1 Asynchronous waveforms and timings

Figure 21 through Figure 24 represent asynchronous waveforms and Table 66 through Table 73 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- DataHoldTime = 0x1 (1 × $T_{fmc_ker_ck}$ for read operations and 2 × $T_{fmc_ker_ck}$ for write operations)
- ByteLaneSetup = 0x1
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all the timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

Table 66. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck}$ - 1	-	$3T_{fmc_ker_ck}$ + 0.5	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	-	1	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc_ker_ck}$ - 1	-	$2T_{fmc_ker_ck}$ + 1	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck}$ - 0.5	-	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	-	1	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	Address held until next read operation			
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$2T_{fmc_ker_ck}$ + 14	-	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	15	-	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	-	$T_{fmc_ker_ck}$ + 0.5	

Table 67. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings

Evaluated by characterization, not tested in production unless otherwise specified.
NWAIT pulse width is equal to 1 clock cycle.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck}$ - 0.5	-	$8T_{fmc_ker_ck}$ + 0.5	ns
$t_{w(NOE)}$	FMC_NWE low time	$7T_{fmc_ker_ck}$ - 0.5	-	$7T_{fmc_ker_ck}$ + 0.5	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc_ker_ck}$	-	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck}$ + 15	-	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck}$ + 13	-	-	

Figure 21. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

1. *Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.*

Table 68. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck}$ - 1	-	$3T_{fmc_ker_ck}$ + 1	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck}$ - 1	-	$T_{fmc_ker_ck}$ + 0.5	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc_ker_ck}$ - 0.5	-	$T_{fmc_ker_ck}$ + 0.5	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck}$ - 0.5	-	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	-	0	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$3T_{fmc_ker_ck}$ - 1	-	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	-	0.5	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$3T_{fmc_ker_ck}$ + 1	-	-	
$t_{v(Data_NE)}$	Data to FMC_NEx low to Data valid	-	-	2	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$3T_{fmc_ker_ck}$ - 1	-	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	-	$T_{fmc_ker_ck}$ + 1	

Table 69. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings

Evaluated by characterization, not tested in production unless otherwise specified.
NWAIT pulse width is equal to 1 clock cycle.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck}$ - 1	-	$8T_{fmc_ker_ck}$ + 0.5	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc_ker_ck}$ - 1	-	$6T_{fmc_ker_ck}$ + 0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck}$ + 15	-	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck}$ + 13	-	-	

Figure 22. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

1. *Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.*

Table 70. Asynchronous multiplexed PSRAM/NOR read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck}$ - 1	-	$4T_{fmc_ker_ck}$ + 0.5	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc_ker_ck}$ - 1	-	$2T_{fmc_ker_ck}$ + 0.5	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc_ker_ck}$ - 1	-	$T_{fmc_ker_ck}$ + 0.5	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck}$	-	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	-	2	

Symbol	Parameter	Min	Typ	Max	Unit
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	-	0.5	ns
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck}$ - 1	-	$T_{fmc_ker_ck}$ + 0.5	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck}$ - 3	-	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	Address held until next read operation			
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck}$ + 14	-	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	15	-	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	-	

Table 71. Asynchronous multiplexed PSRAM/NOR read - NWAIT timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc_ker_ck}$ - 1	-	$9T_{fmc_ker_ck}$ + 0.5	ns
$t_{w(NOE)}$	FMC_NWE low time	$6T_{fmc_ker_ck}$ - 1	-	$6T_{fmc_ker_ck}$ + 0.5	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck}$ + 15	-	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck}$ + 13	-	-	

Figure 23. Asynchronous multiplexed PSRAM/NOR read waveforms

Table 72. Asynchronous multiplexed PSRAM/NOR write timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck} - 1$	-	$4T_{fmc_ker_ck} + 1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck} - 1$	-	$T_{fmc_ker_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc_ker_ck} - 0.5$	-	$2T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck} - 0.5$	-	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	-	1.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 1$	-	$T_{fmc_ker_ck} + 1$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck} - 1$	-	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$3T_{fmc_ker_ck} - 1$	-	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$3T_{fmc_ker_ck} + 1$	-	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	-	0	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	-	$T_{fmc_ker_ck} + 1$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$3T_{fmc_ker_ck} - 1$	-	-	

Table 73. Asynchronous multiplexed PSRAM/NOR write - NWAIT timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc_ker_ck} - 1$	-	$9T_{fmc_ker_ck} + 0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{fmc_ker_ck} - 1$	-	$7T_{fmc_ker_ck} + 0.5$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 15$	-	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$6T_{fmc_ker_ck} + 13$	-	-	

Figure 24. Asynchronous multiplexed PSRAM/NOR write waveforms

6.3.19.2 *Synchronous waveforms and timings*

Figure 25 through Figure 28 represent synchronous waveforms and Table 74 through Table 77 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period, with the following FMC_CLK maximum values:

- For 3.0 V < V_{DD} < 3.6 V, FMC_CLK = 70 MHz at 20 pF (66 MHz when using FMC_NWAIT)
- For 1.71 V < V_{DD} < 1.89 V, FMC_CLK = 70 MHz at 20 pF (66 MHz when using FMC_NWAIT)

Table 74. Synchronous non-multiplexed NOR/PSRAM read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	R × $T_{fmc_ker_ck}$ - 0.5[(1)]	-	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	2.5	

Symbol	Parameter	Min	Typ	Max	Unit
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	$R \times T_{fmc_ker_ck} / 2 + 1.5$[1]	-	-	ns
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 0..25)	-	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 0..25)	$R \times T_{fmc_ker_ck} / 2 + 0.5$[1]	-	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	-	0	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R \times T_{fmc_ker_ck} / 2 + 1$[1]	-	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	3.5	-	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	2	-	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	-	
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT valid (x = 0..2)	-	-	$((DATLAT + 2.5) \times t_{w(CLK)}) - 9$	

1. *Clock ratio R = (FMC_CLK period / fmc_ker_ck period).*

Figure 25. Synchronous non-multiplexed NOR/PSRAM read timings

Table 75. Synchronous non-multiplexed PSRAM write timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{(CLK)}$	FMC_CLK period	$R \times T_{fmc_ker_ck}$ -0.5[(1)]	-	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	1.5	
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	$R \times T_{fmc_ker_ck} / 2 + 0.5$[(1)]	-	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	1.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 0..25)	-	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 0..25)	$R \times T_{fmc_ker_ck} / 2 + 0.5$[(1)]	-	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	-	1	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$R \times T_{fmc_ker_ck} / 2$[(1)]	-	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	-	0	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R \times T_{fmc_ker_ck} / 2 + 2$[(1)]	-	-	

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	-	ns
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	-	
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT valid (x = 0..2)	-	-	((DATLAT + 2.5) × $t_{w(CLK)}$) - 9	

1. Clock ratio R = (FMC_CLK period / fmc_ker_ck period).

Figure 26. Synchronous non-multiplexed PSRAM write timings

Table 76. Synchronous multiplexed NOR/PSRAM read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	R × $T_{fmc_ker_ck}$ - 0.5[(1)]	-	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	R × $T_{fmc_ker_ck}$ / 2 + 1.5[(1)]	-	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16..25)	-	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16..25)	R × $T_{fmc_ker_ck}$ / 2 + 0.5[(1)]	-	-	

Symbol	Parameter	Min	Typ	Max	Unit
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	-	0	ns
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R \times T_{fmc_ker_ck} / 2 + 1$[1]	-	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0.5	-	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	3.5	-	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	2	-	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	-	
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT valid (x = 0..2)	-	-	$((DATLAT + 2.5) \times t_{w(CLK)}) - 9$	

1. *Clock ratio R = (FMC_CLK period / fmc_ker_ck period).*

Figure 27. Synchronous multiplexed NOR/PSRAM read timings

Table 77. Synchronous multiplexed PSRAM write timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R \times T_{fmc_ker_ck} - 0.5$[1]	-	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	1.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	$R \times T_{fmc_ker_ck} / 2 + 0.5$[1]	-	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	2	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16..25)	-	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16..25)	$R \times T_{fmc_ker_ck} / 2 + 0.5$[1]	-	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	-	1	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	$R \times T_{fmc_ker_ck} / 2$[1]	-	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	-	3	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0.5	-	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	0	-	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	$R \times T_{fmc_ker_ck} / 2 + 2$[1]	-	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	-	
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT valid (x = 0..2)	-	-	$((DATLAT + 2.5) \times t_{w(CLK)}) - 9$	

1. *Clock ratio R = (FMC_CLK period / fmc_ker_ck period).*

Figure 28. Synchronous multiplexed PSRAM write timings

6.3.19.3 *NAND controller waveforms and timings*

Figure 29 and Figure 30 represent synchronous waveforms, and Table 78 and Table 79 provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- FMC_SetupTime = 0x01
- FMC_WaitSetupTime = 0x03
- FMC_HoldSetupTime = 0x02
- FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- C_L = 30-pF

In all timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

Table 78. NAND flash read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc_ker_ck}$ - 0.5	-	$4T_{fmc_ker_ck}$ + 0.5	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	12.5	-	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	-	$2T_{fmc_ker_ck}$ + 1.5	

Symbol	Parameter	Min	Typ	Max	Unit
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{fmc_ker_ck}$ - 1	-	-	ns

Figure 29. NAND controller waveforms for read access

1. *y = 7 or 15 depending on the NAND flash memory interface.*

Table 79. NAND flash write timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc_ker_ck}$ - 1	-	$4T_{fmc_ker_ck}$ + 1	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$5T_{fmc_ker_ck}$ - 1	-	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$4T_{fmc_ker_ck}$ - 1	-	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	-	$2T_{fmc_ker_ck}$ + 1.5	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3T_{fmc_ker_ck}$ - 1	-	-	

Figure 30. NAND controller waveforms for write access

1. *y = 7 or 15 depending on the NAND flash memory interface.*

6.3.20 OCTOSPI interface characteristics

Unless otherwise specified, the parameters given in Table 80, Table 81 and Table 82 for OCTOSPI are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- IO compensation cell activated
- VDDIOxVRSEL = 1 for V_{DDIOx} < 2.7 V

Refer to Table 17. General operating conditions for more details on the input/output alternate function characteristics.

Table 80. OCTOSPI characteristics in SDR mode

Evaluated by characterization, not tested in production unless otherwise specified.
Values in the table applies to octal and quad SPI mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	Clock frequency	3 < V_{DDIOx} < 3.6, C_L = 20 pF, OCTOSPIM port1	-	-	120	MHz
		3 < V_{DDIOx} < 3.6, C_L = 20 pF, OCTOSPIM port2	-	-	133	
		2.7 < V_{DDIOx} < 3.6, C_L = 20 pF, OCTOSPIM port1	-	-	100	
		2.7 < V_{DDIOx} < 3.6, C_L = 20 pF, OCTOSPIM port2	-	-	110	
		1.71 < V_{DDIOx} < 1.89, C_L = 20 pF	-	-	133	
$t_{w(CLKH)}$	Clock high and low time - Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}$ / 2	-	$t_{(CLK)}$/2 +1	ns
$t_{w(CLKL)}$			$t_{(CLK)}$/2 - 1	-	$t_{(CLK)}$/2	
$t_{w(CLKH)}$	Clock high and low time - Odd division	PRESCALER[7:0] = n = 2,4,6,8	(n/2) × $t_{(CLK)}$ / (n+1)	-	(n/2) × $t_{(CLK)}$ / (n+1) + 1	
$t_{w(CLKL)}$			(n/2+1) × $t_{(CLK)}$ / (n+1) - 1	-	(n/2+1) × $t_{(CLK)}$ / (n+1)	
$t_{s(IN)}$	Data input setup time	-	2.5	-	-	
$t_{h(IN)}$	Data input hold time	-	1.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	0.5	1	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

Figure 31. OCTOSPI timing diagram - SDR mode

Table 81. OCTOSPI characteristics in DTR mode (without DQS)

Evaluated by characterization, not tested in production unless otherwise specified.
Values in the table applies to octal and quad SPI mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	Clock frequency	$2.7 < V_{DDIOx} < 3.6$, $C_L = 20$ pF	-	-	100	MHz
		$1.71 < V_{DDIOx} < 1.89$, $C_L = 20$ pF	-	-	100	
$t_{w(CLKH)}$	Clock high and low time - Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)} / 2$	-	$t_{(CLK)} / 2 + 1$	ns
$t_{w(CLKL)}$			$t_{(CLK)} / 2 - 1$	-	$t_{(CLK)} / 2$	
$t_{w(CLKH)}$	Clock high and low time - Odd division	PRESCALER[7:0] = n = 2,4,6,8	$(n/2) \times t_{(CLK)} / (n+1)$	-	$(n/2) \times t_{(CLK)} / (n+1) + 1$	
$t_{w(CLKL)}$			$(n/2+1) \times t_{(CLK)} / (n+1) - 1$	-	$(n/2+1) \times t_{(CLK)} / (n+1)$	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	-	2	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	-	1.5	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$ (1)	Data output valid time	-	-	$1 + t_{(CLK)} / 4$	$1.5 + t_{(CLK)} / 4$	
			-	1	1.5	
$t_{hr(OUT)}$, $t_{hf(OUT)}$ (1)	Data output hold time	-	$t_{(CLK)} / 4 - 0.5$	-	-	
			0	-	-	

1. *When PRESCALER = 0 the DLL must be used for TX delay.*

Figure 32. OCTOSPI timing diagram - DTR mode

Table 82. OCTOSPI characteristics in DTR mode (with DQS or HyperBus)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	Clock frequency	$2.7 < V_{DDIOx} < 3.6$, $C_L = 20$ pF	-	-	133	MHz
		$1.71 < V_{DDIOx} < 1.89$, $C_L = 20$ pF	-	-	133	
$t_{w(CLKH)}$	Clock high and low time - Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)} / 2$	-	$t_{(CLK)} / 2 + 1$	ns
$t_{w(CLKL)}$			$t_{(CLK)} / 2 - 1$	-	$t_{(CLK)} / 2$	
$t_{w(CLKH)}$	Clock high and low time - Odd division	PRESCALER[7:0] = n = 2,4,6,8	$(n/2) \times t_{(CLK)} / (n+1)$	-	$(n/2) \times t_{(CLK)} / (n+1) + 1$	
$t_{w(CLKL)}$			$(n/2+1) \times t_{(CLK)} / (n+1) - 1$	-	$(n/2+1) \times t_{(CLK)} / (n+1)$	
$t_{w(CS)}$	Chip select high time	-	$3 \times t_{(CLK)}$	-	-	
$t_{v(CK)}$	CS to Clock valid time	-	-	-	$t_{(CLK)} + 1$	
$t_{h(CK)}$	Clock to CS high hold time	-	$3.5 \times t_{(CLK)}$	-	-	
$V_{ODr(CK)}$	CK,CK# crossing level on CK rising edge	$V_{DDIOx} = 1.8$ V	1157	-	1389	
$V_{ODf(CK)}$	CK,CK# crossing level on CK falling edge	$V_{DDIOx} = 1.8$ V	1087	-	1312	
$t_{sr(DQ)}$, $t_{sf(DQ)}$	Data input setup time	$F_{(CLK)} > 50$ MHz(1)	$1.5 - t_{(CLK)} / 4$	-	-	
		$F_{(CLK)} < 50$ MHz(2)	-1	-	-	
$t_{hrDQN)}$, $t_{hf(DQ)}$	Data input hold time	$F_{(CLK)} > 50$ MHz(1)	$1.5 + t_{(CLK)} / 4$	-	-	
		$F_{(CLK)} < 50$ MHz(2)	3	-	-	
$t_{v(DS)}$	Data strobe input valid time	-	0	-	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(DS)}$	Data strobe input hold time	-	0	-	-	ns
$t_{v(RWDS)}$	Data strobe output valid time	-	-	-	$3 \times t_{(CLK)}$	
$t_{vr(OUT)}$, $t_{vf(OUT)}$[3]	Data output valid time	-	-	$1 + t_{(CLK)} / 4$	$1.5 + t_{(CLK)} / 4$	
			-	1	1.5	
$t_{hr(OUT)}$, $t_{hf(OUT)}$[3]	Data output hold time	-	$t_{(CLK)} / 4 - 0.5$	-	-	
			0	-	-	

1. *DLL enabled in lock mode (SYSCFG_DLYBOSxCR.EN = 1) with 25% delay (SYSCFG_DLYBOSxCR.RX_TAP_SEL[5:0] = 0x8).*
2. *DLL enabled in bypass mode (SYSCFG_DLYBOSxCR.BYP_EN = 1) with typical settings (SYSCFG_DLYBOSxCR.RX_TAP_SEL[5:0] = 0x2 and SYSCFG_DLYBOSxCR.BYP_CMD[4:0] = 0x18).*
3. *When PRESCALER = 0 the DLL must be used for TX delay.*

Figure 33. OCTOSPI HyperBus clock

Figure 34. OCTOSPI HyperBus read

Figure 35. OCTOSPI HyperBus read with double latency

Figure 36. OCTOSPI HyperBus write

6.3.21 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in Table 83 for the delay block are derived from tests performed under the ambient temperature and V_{DD} supply voltage summarized in Table 17. General operating conditions.

Table 83. DLYB characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	Bypass mode	100	150	300	ps
t_{Δ}	Unit delay	Bypass mode	30	31	49	
		Lock mode	-	T / 32[(1)]	-	
			-1	-	+15	%

1. *T is the period of the DLL clock.*

6.3.22 12-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 84 are derived from tests performed under the ambient temperature, frequency and V_{DDA} supply voltage conditions summarized in Table 17. General operating conditions.

Table 84. ADC characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC adc_ker_ck clock frequency (clock after ADC prescaler)	-	0.7	-	70	MHz
f_s	Sampling rate	resolution = 12 bits	0.0467	-	4.666	MSps
		resolution = 10 bits	0.0538	-	5.384	
		resolution = 8 bits	0.07	-	7	
		resolution = 6 bits	0.0875	-	8.75	
tc(1)	Conversion cycle	resolution = 12 bits	-	13.5	-	1 / f_{ADC}
		resolution = 10 bits	-	11.5	-	
		resolution = 8 bits	-	8.5	-	
		resolution = 6 bits	-	6.5	-	
f_{TRIG}	External trigger frequency	f_{ADC} = 70 MHz, Resolution = 12 bits	-	-	3.888	MHz
			18	-	-	1 / f_{ADC}
V_{AIN}(1)	Conversion voltage range(2)	Single ended	0	-	V_{REF+}	V
		Differential	$-V_{REF+}$	-	V_{REF+}	
V_{CMIV}(1)	Common mode input voltage	Differential	-	V_{REF+} / 2	-	V
C_{ADC}	Internal sample and hold capacitor	-	-	2.56	-	pF
t_{STAB}	ADC power-up time	DEEPPWD from 1 to 0	-	5	-	µs
t_{EN}	ADC enable time	ADEN from 0 to 1	-	5	-	1 / f_{ADC}
t_{LATR}(1)	Trigger conversion latency regular and injected channels without conversion abort	CKMODE = 0	2.5	-	3.5	1 / f_{ADC}
		CKMODE = 1	-	3	-	
$t_{LATRINJ}$(1)	Trigger conversion latency regular injected channels aborting a regular conversion	CKMODE = 0	3.5	-	4.5	1 / f_{ADC}
		CKMODE = 1	-	4	-	
t_S(1)	Sampling time	-	1.5	-	1499.5	1 / f_{ADC}
$I_{ADC(VDDA18ADC)}$	ADC supply current on $V_{DDA18ADC}$	f_s = 4.666 Msps, resolution = 12 bits	-	315	-	µA
		f_s = 5.384 Msps, resolution = 10 bits	-	330	-	
		Power down, ADEN = 0	-	2.05	-	
		Deep power down, ADEN = 0, DEEPPWD = 1	-	1.65	-	

1. *Specified by design, not tested in production.*
2. *All analog inputs must be between V_{SSA} and $V_{DDA18ADC}$. When offset calibration is used, the result of the conversion could be clipped few percent below V_{REF+}. Refer to reference manual for details.*

Table 85. ADC accuracy

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error (TUE)	Single ended with dedicated ANA input	-	4.6	40	+/- LSB
		Differential with dedicated ANA input	-	5.2	22	
		Single ended with general purpose IO (GPIO) input	-	13	24	+/- LSB
		Differential with general purpose IO (GPIO) input	-	6.3	18	
ED	Differential linearity error (DNL)	Single ended with dedicated ANA input	-	0.9	2	+/- LSB
		Differential with dedicated ANA input	-	0.8	2	
		Single ended with general purpose IO (GPIO) input	-	0.9	2	+/- LSB
		Differential with general purpose IO (GPIO) input	-	0.9	2	
EL	Integral linearity error (INL)	Single ended with dedicated ANA input	-	2	6	+/- LSB
		Differential with dedicated ANA input	-	2	5	
		Single ended with general purpose IO (GPIO) input	-	4	6	+/- LSB
		Differential with general purpose IO (GPIO) input	-	3	8	
ENOB	Effective number of bits	Single ended with dedicated ANA input	-	9.9	-	Bits
		Differential with dedicated ANA input	-	10.5	-	
		Single ended with general purpose IO (GPIO) input	-	9.35	-	Bits
		Differential with general purpose IO (GPIO) input	-	10.5	-	
SINAD	Signal-to-noise and distortion ratio[1]	Single ended with dedicated ANA input	-	61.5	-	dB
		Differential with dedicated ANA input	-	66	-	
		Single ended with general purpose IO (GPIO) input	-	58	-	dB
		Differential with general purpose IO (GPIO) input	-	64	-	
SNR	Signal-to-noise ratio	Single ended with dedicated ANA input	-	61.5	-	dB
		Differential with dedicated ANA input	-	66.5	-	
		Single ended with general purpose IO (GPIO) input	-	58.5	-	dB
		Differential with general purpose IO (GPIO) input	-	65	-	
THD	Total harmonic distortion	Single ended with dedicated ANA input	-	-76	-	dB
		Differential with dedicated ANA input	-	-79	-	
		Single ended with general purpose IO (GPIO) input	-	-74.5	-	dB
		Differential with general purpose IO (GPIO) input	-	-73.5	-	
EG	Gain error	Versus V_{REF+} value with dedicated ANA input	-1	-	+1	%Full-Scale
		Versus V_{REF+} value with general purpose IO (GPIO) input	-1	-	+1	
EO	Offset error	Without calibration with ANA input	-1	-	+1	%Full-Scale
		After calibration with ANA input	-2	-	+2	LSB
		Without calibration with general purpose IO (GPIO) input	-1	-	+1	%Full-Scale
		After calibration with general purpose IO (GPIO) input	-2	-	+2	LSB

1. *Value measured with a -0.5dBFS input signal and then extrapolated to full scale.*

Figure 37. ADC accuracy characteristics

1. *Refer to Table 86 for the values of R_{AIN}, R_{ADC} and C_{ADC}.*
2. *$C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to Table 59. I/O static characteristics). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.*
3. *Refer to Table 59. I/O static characteristics for value of I_{lkg}.*
4. *Refer to Section 6.1.6: Power supply scheme.*

Table 86. Minimum sampling time versus RAIN

Specified by design, not tested in production.

Symbol	Parameter	Conditions (Resolution / R_{AIN} in ohms)		Min	Typ	Max	Unit
t_{s_min}	Minimum sampling time	12 bits	47	32	-	-	ns
			68	33	-	-	
			100	34	-	-	
			150	36	-	-	
			220	38	-	-	
			330	42	-	-	
			470	47	-	-	
			680	55	-	-	
			1000(1)	70	-	-	
t_{s_min}	Minimum sampling time	10 bits	47	23	-	-	ns
			68	24	-	-	
			100	25	-	-	
			150	26	-	-	
			220	28	-	-	
			330	30	-	-	
			470	33	-	-	
			680	38	-	-	
			1000	45	-	-	

Symbol	Parameter	Conditions (Resolution / R_{AIN} in ohms)		Min	Typ	Max	Unit
t_{s_min}	Minimum sampling time	10 bits	1500	55	-	-	ns
			2200	71	-	-	
			3300	97	-	-	
			4700	133	-	-	
			6800[1]	238	-	-	
t_{s_min}	Minimum sampling time	8 bits	47	17	-	-	ns
			68	17	-	-	
			100	18	-	-	
			150	19	-	-	
			220	20	-	-	
			330	22	-	-	
			470	25	-	-	
			680	28	-	-	
			1000	34	-	-	
			1500	42	-	-	
			2200	53	-	-	
			3300	70	-	-	
			4700	94	-	-	
			6800	128	-	-	
			10000	183	-	-	
			15000	277	-	-	
			22000[1]	435	-	-	

1. *Maximum external input impedance value authorized for the given Resolution.*

Figure 38. Typical connection diagram using the ADC with TT pins featuring analog switch function

6.3.22.1 *General PCB design guidelines*

PCB design guidelines are provided in AN5489 "Getting started with STM32MP25xx lines hardware development" available from the ST website www.st.com.

6.3.23 Voltage reference buffer (VREFBUF) characteristics

Table 87. VREFBUF characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DDA18ADC}$	Analog supply voltage	-	VRS = 000	1.62	1.8	1.89[1]	V
			VRS = 001	1.75	1.8	1.89[1]	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	At 30 °C, at I_{LOAD} = 10 µA, $V_{DDA18ADC}$ = 1.8 V	VRS = 000	1.203	1.21	1.216	
			VRS = 001	1.491	1.5	1.506	
TRIM	Trim step resolution	-		-	±0.05	±0.1	%
C_L	Load Capacitor	-		0.5	1.1	1.5	µF
esr	Equivalent Serial Resistor of C_L	-		-	-	1	Ω
I_{LOAD}	External DC load current	All ADCs ON		-	-	0.8	mA
		All ADCs OFF		-	-	2	
I_{LINE_REG}	Line regulation	$V_{DDA18ADC}$ range according to VRS value. T_J = +30 °C.		-	7500	11000	ppm/V
I_{LOAD_REG}	Load regulation	100 µA ≤ I_{LOAD} ≤ 800 µA. T_J = +30 °C.		-	4700	6000	ppm/mA
T_{coeff}	Temperature coefficient	-40 °C < T_J < +30 °C		+89	-	+305	ppm/°C
		+30 °C < T_J < +125 °C		-15	-	+68	
A_{coeff}	Long term stability	1000 hours, T_J = 125 °C		-2000	-	+2000	ppm
PSRR	Power supply rejection	DC		-	76	-	dB
		100 kHz		-	60	-	
t_{START}	Start-up time	-		-	260	388	µs
I_{INRUSH}	Control of max. DC current drive on V_{REFBUF_OUT} during start-up phase (t_{START})			-	-	10	mA
$I_{VDDA18ADC(VREFBUF)}$	VREFBUF supply current $V_{DDA18ADC}$ (excluding internal and external load)	ENVR = 1	I_{LOAD} = 0.8 mA DC	-	9	21	µA
			Peak during 2 × ADC conversion	-	48	60	
		ENVR = 0		-	3	6.5	µA

1. *Static condition. 1.98 V allowed during transients.*

6.3.24 Digital Temperature Sensor (DTS) characteristics

Table 88. DTS characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}	Operating frequency	-	4	-	8	MHz
Res	Resolution	-	8	10	12	Bits
Step	Step size	For respectively 8, 10 and 12 bits resolution	0.86	0.22	0.06	°C
t_{conv}	Conversion time	For respectively 8, 10 and 12 bits resolution	512	2048	8192	1 / f_{DTS}
t_{pwrup}	Power up time	-	-	-	256	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_A	Accuracy	From -20 to +125 °C	-	-	3[1]	°C
		From -40° C to -20 °C	-	-	6	
G	G constant	Refer to reference manual for the formula	58.5			°C
H	H constant	Refer to reference manual for the formula	201.2			°C
J	J constant	Refer to reference manual for the formula	0			°C / MHz
Cal5	Cal5 constant	Refer to reference manual for the formula	4094			-
TS_{loc}	Sensor location	TS0 sensor	Inside padring[2]			-
		TS1 sensor	Inside device logic[2]			-
$I_{DTS(VDDA18AON)}$	DTS supply current on $V_{DDA18AON}$	f_{DTS} = 8 MHz, continuous measurements, single sensor	-	120	160	µA
		At 1 measurement/s	-	-	1	
		f_{DTS} clock stopped	-	-	1	
$I_{DTS(VDDCORE)}$	DTS supply current on V_{DDCORE}	f_{DTS} = 8 MHz	-	-	15	µA

1. *Guaranteed by test in production.*
2. *Temperature in padring sensor (side of the silicon die) is usually slightly lower than device logic sensor as most heat is generated inside device logic.*

6.3.25 V_{BAT}, V_{DDCPU}, V_{DDCORE}, V_{DDGPU} ADC measurement characteristics

Table 89. V_{BAT}, V_{DDCPU}, V_{DDCORE}, V_{DDGPU} ADC measurement characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	-	130	-	kΩ
Q	Ratio on V_{BAT} measurement	-	-	4	-	-
E_r	Error on Q	-	-1	-	+1	%
t_{S_VBAT}[1]	ADC sampling time when reading the V_{BAT}	-	34	-	-	ns
t_{S_VDDCPU}[1]	ADC sampling time when reading the V_{DDCPU}	-	34	-	-	ns
$t_{S_VDDCORE}$[1]	ADC sampling time when reading the V_{DDCORE}	-	34	-	-	ns
t_{S_VDDGPU}[1]	ADC sampling time when reading the V_{DDGPU}	-	34	-	-	ns

1. *Specified by design, not tested in production.*

6.3.26 Temperature and V_{BAT} monitoring characteristic for tamper detection

Table 90. TEMP and V_{BAT} Monitoring characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TEMPH	High T_J temperature monitoring	-	110	-	125	° C
TEMPL	Low T_J temperature monitoring	-	-40	-	-30	
V08CAPH	High V_{08CAP} supply monitoring[1]	-	0.88	-	1	V
V08CAPL	Low V_{08CAP} supply monitoring[1]	-	0.6	-	0.72	-
V08CAP_filter	V_{08CAP} supply monitoring glitch filter[1]	-	-	-	1	µs

1. *V08CAP is an internal regulator supplied by V_{SW}. V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*

6.3.27 Voltage monitoring characteristics

Table 91. Voltage monitoring characteristics (V_{DDCORE}, V_{DDCPU}, V_{DDGPU}, PVD_IN, $V_{DDA18ADC}$, $V_{DDIO1/2/3/4}$, $V_{DD33USB}$, $V_{DD33UCPD}$)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDCORE} monitoring							
V_{OV_VDCORE}	Threshold on rising edge	To set VCOREH bit (overvoltage)		0.88[1]	-	-	V
$V_{UV_VDDCORE}$	Threshold on falling edge	To set VCOREL bit (undervoltage)		0.72	-	0.78[1]	
$V_{hyst_VDDCORE}$	Hysteresis on monitoring	To clear VCOREL or VCOREH bit		-	20	-	mV
$I_{UV_OV_VDDCORE(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	VCOREMONEN = 1		-	0.75	-	µA
V_{DDCPU} monitoring							
V_{OV_VDDCPU}	Threshold on rising edge	To set VCPUH bit (overvoltage)		0.99[1]	-	-	V
V_{UV_VDDCPU}	Threshold on falling edge	To set VCPUL bit (undervoltage)	VCPULLS = 0	0.72	-	0.78[1]	
			VCPULLS = 1	0.81	-	0.87	
V_{hyst_VDDCPU}	Hysteresis on monitoring	To clear VCPUL or VCPUH bit		-	20	-	mV
$I_{UV_OV_VDDCPU(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	VCPUMONEN = 1		-	0.75	-	µA
V_{DDGPU} monitoring							
$V_{RDY_VDDDGPU}$	Threshold on rising edge	To set VDDGPURDY bit	GPULVTEN = 0	0.63[1]	-	-	V
			GPULVTEN = 1	0.55	-	-	
V_{hyst_VDDGPU}	Hysteresis on falling edge	To clear VDDGPURDY bit		-	23	-	mV
T_{delay_VDDGPU}	Delay after detection	To set VDDGPURDY bit		180	400	750	µs
		To clear VDDGPURDY bit		-	0	-	
$I_{RDY_VDDGPU(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	GPUVMEN = 1		-	0.75	-	µA
PVD_IN monitoring							
V_{PVD_IN}	Threshold on rising edge	-		-	0.815	-	V
V_{hyst_PVD}	Hysteresis on monitoring	-		-	30	-	mV
$I_{PVD(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	PVDEN = 1		-	0.75	-	µA
$V_{DDA18ADC}$ monitoring							
$V_{RDY_VDDA18ADC}$	Threshold on rising edge	-		-	-	1.55[1]	V
$V_{hyst_VDDA18ADC}$	Hysteresis on monitoring	-		-	40	-	mV

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{RDY_VDDA18ADC(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	AVMEN = 1		-	0.75	-	µA
$I_{RDY_VDDA18ADC}$	Supply current on $V_{DDA18ADC}$	AVMEN = 1		-	1	-	µA
V_{DDIO1} monitoring							
V_{RDY_VDDIO1}	Threshold on rising edge	-		-	-	1.55(1)	V
V_{hyst_VDDIO1}	Hysteresis on monitoring	-		-	40	-	mV
$I_{RDY_VDDIO1(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	VDDIO1VMEN = 1		-	0.75	-	µA
I_{RDY_VDDIO1}	Supply current on V_{DDIO1}	Always ON	VDDIO1 = 1.8 V	-	0.5	-	µA
			VDDIO1 = 3.3 V	-	1	-	
V_{DDIO2} monitoring							
V_{RDY_VDDIO2}	Threshold on rising edge	-		-	-	1.55(1)	V
V_{hyst_VDDIO2}	Hysteresis on monitoring	-		-	40	-	mV
$I_{RDY_VDDIO2(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	VDDIO2VMEN = 1		-	0.75	-	µA
I_{RDY_VDDIO2}	Supply current on V_{DDIO2}	Always ON	VDDIO2 = 1.8 V	-	0.5	-	µA
			VDDIO2 = 3.3 V	-	1	-	
V_{DDIO3} monitoring							
V_{RDY_VDDIO3}	Threshold on rising edge	-		-	-	1.55(1)	V
V_{hyst_VDDIO3}	Hysteresis on monitoring	-		-	40	-	mV
$I_{RDY_VDDIO3(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	VDDIO3VMEN = 1		-	0.75	-	µA
I_{RDY_VDDIO3}	Supply current on V_{DDIO3}	Always ON	VDDIO3 = 1.8 V	-	0.5	-	µA
			VDDIO3 = 3.3 V	-	1	-	
V_{DDIO4} monitoring							
V_{RDY_VDDIO4}	Threshold on rising edge	-		-	-	1.55(1)	V
V_{hyst_VDDIO4}	Hysteresis on monitoring	-		-	40	-	mV
$I_{RDY_VDDIO4(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	VDDIO4VMEN = 1		-	0.75	-	µA
I_{RDY_VDDIO4}	Supply current on V_{DDIO4}	Always ON	VDDIO4 = 1.8 V	-	0.5	-	µA
			VDDIO4 = 3.3 V	-	1	-	
$V_{DD33USB}$ monitoring							
$V_{RDY_VDD33USB}$	Threshold on rising edge	-		-	-	1.55(1)	V
$V_{hyst_VDD33USB}$	Hysteresis on monitoring	-		-	40	-	mV
$I_{RDY_VDD33USB(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	USB33VMEN = 1		-	0.75	-	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{RDY_VDD33USB}$	Supply current on $V_{DD33USB}$	Always ON	-	1	-	µA
$V_{DD33UCPD}$ monitoring						
$V_{RDY_VDD33UCPD}$	Threshold on rising edge	-	-	-	1.55(1)	V
$V_{hyst_VDD33UCPD}$	Hysteresis on monitoring	-	-	40	-	mV
$I_{RDY_VDD33UCPD(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	UCPDVMEN = 1	-	0.75	-	µA
$I_{RDY_VDD33UCPD}$	Supply current on $V_{DD33UCPD}$	Always ON	-	1	-	µA

1. *Guaranteed by test in production.*

6.3.28 Compensation cell characteristics

Table 92. Compensation cell characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{COMPCELL}$	$V_{DDA18AON}$ current consumption during code calculation	Using a 8 MHz clock (HSI / 8)	-	250	-	µA
Tready	Time needed to have the first code calculation after enabling		-	96	-	µs
Tmeasure	Time needed to update the code		-	832	-	

6.3.29 Multi-function digital filter (MDF) characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Capacitive load C_L = 30 pF
- Measurement points done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell activated
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 93. MDF characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CKI}	Input clock frequency via MDF_CKIx pin, in SLAVE SPI mode	-	-	-	25	MHz
f_{CCKI}	Input clock frequency via MDF_CCK[1:0] pin, in SLAVE SPI mode	-	-	-	25	
f_{CCKO}	Output clock frequency in MASTER SPI mode	-	-	-	25	
f_{CCKOLF}	Output clock frequency in LF_MASTER SPI mode	-	-	-	5	
f_{SYMB}	Input symbol rate in Manchester mode	-	-	-	20	
t_{HCKI} t_{LCKI}	MDF_CKIx input clock high and low time	In SLAVE SPI mode	2 × $T_{mdf_proc_ck}$(1)	-	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{HCCKI} t_{LCCKI}	MDF_CCK[1:0] input clock high and low time	In SLAVE SPI mode	2 × $T_{mdf_proc_ck}$(1)	-	-	ns
t_{HCCKO} t_{LCCKO}	MDF_CCK[1:0] output clock high and low time	In MASTER SPI mode	2 × $T_{mdf_proc_ck}$(1)	-	-	
$t_{HCCKOLF}$ $t_{LCCKOLF}$	MDF_CCK[1:0] output clock high and low time	In LF_MASTER SPI mode	$T_{mdf_proc_ck}$(1)	-	-	
t_{SUCKI}	Data setup time with respect to MDF_CKIx input	In SLAVE SPI mode, measured on rising and falling edge	7.5	-	-	
t_{HDCKI}	Data hold time with respect to MDF_CKIx input		0.5	-	-	
t_{SUCCKI}	Data setup time with respect to MDF_CCK[1:0] input	In SLAVE SPI mode: MDF_CCK[1:0] configured in input, measured on rising and falling edge	8.5	-	-	
t_{HDCCKI}	Data hold time with respect to MDF_CCK[1:0] input		0.5	-	-	
t_{SUCCKO}	Data setup time with respect to MDF_CCK[1:0] output	In MASTER SPI mode: MDF_CCK[1:0] configured in output, measured on rising and falling edge	8.5	-	-	
t_{HDCCKO}	Data hold time with respect to MDF_CCK[1:0] output		0.5	-	-	
$t_{SUCCKOLF}$	Data setup time with respect to MDF_CCK[1:0] output	In LF_MASTER SPI mode, MDF_CCK[1:0] configured in output, measured on rising and falling edge	14.5	-	-	
$t_{HDCCKOLF}$	Data hold time with respect to MDF_CCK[1:0] output		0.5	-	-	

1. *Tmdf_proc_ck is the period of the MDF processing clock.*

Figure 39. MDF timing diagram

6.3.30 Camera interface (DCMI) characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C_L = 30 pF
- Measurement points done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell activated
- VDDxVRSEL activated when V_{DDx} ≤ 2.7 V

Table 94. DCMI characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
clock_ratio	Frequency ratio DCMI_PIXCLK / f_{HCLK}	-	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	-	80	MHz
D_{PIXEL}	Pixel clock input duty cycle	30	-	70	%
$t_{su(DATA)}$	Data input setup time	3	-	-	ns
$t_{h(DATA)}$	Data hold time	1	-	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC and DCMI_VSYNC input setup times	3	-	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC and DCMI_VSYNC input hold times	1	-	-	

Figure 40. DCMI timing diagram

6.3.31 Camera interface (DCMIPP) characteristics

Unless otherwise specified, the parameters given in Table 95 for DCMIPP are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- DCMIPP_PIXCLK polarity: falling (refer to AN5489 "Getting started with STM32MP25xx lines hardware development") available from the ST website www.st.com.
- DCMIPP_VSYNC and DCMIPP_HSYNC polarity: high
- Data formats: 16 bits
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell activated
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 95. DCMIPP characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DCMIPP_PIXCLK	Pixel clock input	-	-	-	120	MHz
DPixel	Pixel clock input duty cycle	-	30	-	70	%
$t_{su(DATA)}$	Data input setup time	-	2	-	-	ns
$t_{h(DATA)}$	Data input hold time	-	4	-	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMIPP_HSYNC / DCMIPP_VSYNC input setup time	-	2	-	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMIPP_HSYNC / DCMIPP_VSYNC input hold time	-	4	-	-	

Figure 41. DCMIPP timing diagram

6.3.32 Parallel interface (PSSI) characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- PSSI_PDCK polarity: falling
- PSSI_RDY and PSSI_DE polarity: low
- Bus width: 16 lines
- Data width: 32 bits
- Capacitive load C_L = 30 pF
- Measurement points done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell activated
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 96. PSSI transmit characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
clock_ratio	Frequency ratio DCMI_PDCK/f_{HCLK}	-	-	-	0.4	-
PSSI_PDCK	PSSI clock input	-	-	-	74(1)	MHz
D_{PIXEL}	PSSI clock input duty cycle	-	30	-	70	%
$t_{OV(DATA)}$	Data output valid time	-	-	-	13.5	ns
$t_{OH(DATA)}$	Data output hold time	-	5.5	-	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{OV(DE)}$	DE output valid time	-	-	-	10	ns
$t_{OH(DE)}$	DE output hold time		6.5	-	-	
$t_{SU(RDY)}$	RDY input setup time	-	0	-	-	
$t_{H(RDY)}$	RDY input hold time		5.5	-	-	

1. *This maximal frequency does not consider receiver setup and hold timings.*

Figure 42. PSSI transmit timing diagram

Table 97. PSSI receive characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
clock_ratio	Frequency ratio DCMI_PDCK/f_{HCLK}	-	-	-	0.4	-
PSSI_PDCK	PSSI clock input	-	-	-	80	MHz
D_{PIXEL}	PSSI clock input duty cycle	-	30	-	70	%
$t_{SU(DATA)}$	Data input setup time	-	2.5	-	-	ns
$t_{H(DATA)}$	Data input hold time	-	1.5	-	-	
$t_{SU(DE)}$	DE input setup time	-	1.5	-	-	
$t_{H(DE)}$	DE input hold time	-	1	-	-	
$t_{OV(RDY)}$	RDY output valid time	-	-	-	11.5	
$t_{OH(RDY)}$	RDY output hold time	-	8	-	-	

Figure 43. PSSI receive timing diagram

6.3.33 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in Table 98 for the LTDC interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- LCD_CLK polarity: low (signals change on CLK rising edge)
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to:
  - LTDC Clock: OSPEEDRy[1:0] = 11
  - Other LTDC signals: OSPEEDRy[1:0] = 01
- Advanced I/O configurations:
  - LTDC Clock: RET = 0, INVCLK = 0, DE = 0, DLYPATH = 0
  - Other LTDC signals: RET = 1, INVCLK = 0, DE = 0, DLYPATH = 0
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 98. LTDC characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLK}	LTDC clock output frequency	C = 20 pF	-	-	148.5	MHz
		C = 30 pF			120	
D_{CLK}	LTDC clock output duty cycle	-	45	-	55	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock high time, low time	-	$t_{w(CLK)}$ / 2 - 0.5	-	$t_{w(CLK)}$ / 2 + 0.5	ns
$t_{v(DATA)}$	Data output valid time	-	-	-	4	
$t_{h(DATA)}$	Data output hold time	-	1	-	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time	-	-	-	3.5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC / VSYNC / DE output hold time	-	0.5	-	-	

Figure 44. LCD-TFT horizontal timing diagram

Figure 45. LCD-TFT vertical timing diagram

6.3.34 Timer characteristics

The parameters given in Table 99 are specified by design, not tested in production.

Refer to Section 6.3.16: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 99. TIMx characteristics

TIMx is used as a general term to refer to the TIM1 to TIM20 timers.
Specified by design, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{TIMxCLK}$	Timer kernel clock	0	200	MHz
f_{EXT}	Timer external clock frequency on CH1 to CH4	0	$f_{TIMxCLK}$ / 2	
Res_{TIM}	Timer resolution	-	16	bit
	Timer resolution (TIM2 to TIM5)	-	32	
t_{MAX_COUNT}	Maximum possible count with 16-bit counters	-	65536	$t_{TIMxCLK}$
	Maximum possible count with 32-bit counter (TIM2 to TIM5)	-	65536 × 65536	

Table 100. LPTIMx characteristics

LPTIMx is used as a general term to refer to the LPTIM1 to LPTIM5 timers.
Specified by design, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{res(LPTIM)}$	Timer resolution time	1	-	$t_{LPTIMxCLK}$
$f_{LPTIMxCLK}$	Timer kernel clock	0	100	MHz
	Timer kernel clock (autonomous mode)	0	32768	Hz
f_{EXT}	Timer external clock frequency on IN1 and IN2	0	$f_{LPTIMxCLK/2}$	MHz
Res_{LPTIM}	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65536	$t_{LPTIMxCLK}$

6.3.35 Communications interfaces

6.3.35.1 *I2C interface characteristics*

The I2C interface meets the timings requirements of the I^2C-bus specification for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are specified by design, not tested in production, when the I2C peripheral is properly configured (refer to product reference manual):

The SDA and SCL I/O requirements are met with the following restriction:

- The SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

All I2C SDA and SCL I/Os embed an analog filter. Refer to Table 101 for the analog filter characteristics:

Table 101. I2C analog filter characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbols	Parameters	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(1)	260(2)	ns

1. *Spikes with widths below t_{AF}(min) are filtered. At T_J = -40 °C, the guaranteed minimum is 40 ns.*
2. *Spikes with widths above t_{AF}(max) are not filtered.*

6.3.35.2 *I3C interface characteristics*

The I3C timings are in line with timings requirements of the MIPI® I3C specification v1.1, except for the ones given in Table 102. This can be mitigated by increasing the corresponding SCL low duration in the I3C_TIMINGR0 register.

The I3C peripheral supports:

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

Unless otherwise specified, the parameters given in Table 102 for the I3C interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 102. I3C specific timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SU_OD}	SDA data setup time during Open-Drain mode	Controller	19.5	-	-	ns
t_{SU_PP}	SDA sata setup time in Push-Pull mode	Controller	15	-	-	ns

Table 103. I3C pin characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$R_{PU(I3C)}$	I3C pull-up	1600	2200	2800	Ω
$R_{HK(I3C)}$	I3C high keeper (weak pull-up)	125	160	195	kΩ

6.3.35.3 *SPI interface characteristics*

Unless otherwise specified, the parameters given in Table 104 for the SPI interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when V_{DDx} ≤ 2.7 V

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 104. SPI characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode 1.71 V < V_{DD} < 1.89 V	-	-	115	MHz
		Master mode 3.0 V < V_{DD} < 3.6 V	-	-	105	
		Slave receiver mode	-	-	100	
		Slave mode transmitter/full duplex	-	-	41.5(1)	
$t_{su(NSS)}$	NSS setup time	Slave mode	4	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	1	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{sck2}(2) - 1	T_{sck2}(2)	T_{sck2}(2) + 1	
$t_{su(MI)}$	Data input setup time	Master mode	4.5	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	1	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	11	15	15	
$t_{dis(SO)}$	Data output disable time	Slave mode	12.5	14.5	17.5	
$t_{v(MO)}$	Data output valid time	Master mode	-	3	3.5	
$t_{v(SO)}$		Slave mode	-	11.5	12	
$t_{h(MO)}$	Data output hold time	Master mode	2	-	-	
$t_{h(SO)}$		Slave mode	10	-	-	

1. *Maximum frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%.*
2. *T_{sck2} = T_{pclk} × prescaler / 2.*

Figure 46. SPI timing diagram - master mode

Figure 47. SPI timing diagram - slave mode and CPHA = 0

Figure 48. SPI timing diagram - slave mode and CPHA = 1

6.3.35.4 *I2S interface characteristics*

Unless otherwise specified, the parameters given in Table 105 for the I2S interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 01
- Capacitive load C= 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 105. I2S characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCK}	I2S main clock output	-	-	-	50	MHz
f_{CK}	I2S clock frequency	Master mode	-	-	50	MHz
		Slave transmit mode	-	-	23	
		Slave receive mode	-	-	50	
$t_{v(WS)}$	WS valid time	Master mode	-	-	3.5	ns
$t_{h(WS)}$	WS hold time	Master mode	2.5	-	-	
$t_{su(WS)}$	WS setup time	Slave mode	3.5	-	-	
$t_{h(WS)}$	WS hold time	Slave mode	3	-	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	4	-	-	
$t_{su(SD_SR)}$		Slave receiver	3	-	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	2.5	-	-	
$t_{h(SD_SR)}$		Slave receiver	1.5	-	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	-	13	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	-	3.5	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8.5	-	-	ns
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	0	-	-	

Figure 49. I2S slave timing diagram (Philips protocol)

1. *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*

Figure 50. I2S master timing diagram (Philips protocol)

1. *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*

6.3.35.5 *SAI interface characteristics*

Unless otherwise specified, the parameters given in Table 106 for SAI are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are performed at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 106. SAI characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCK}	SAI main clock output	-	-	-	50	MHz
f_{CK}	SAI bit clock frequency[(1)]	Master transmitter	-	-	38	MHz
		Master receiver	-	-	34	
		Slave transmitter	-	-	40	
		Slave receiver	-	-	50	
$t_{v(FS)}$	FS valid time	Master mode	-	-	13	ns
$t_{su(FS)}$	FS setup time	Slave mode	9	-	-	
$t_{h(FS)}$	FS hold time	Master mode	5.5	-	-	
		Slave mode	1	-	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	5.5	-	-	
$t_{su(SD_B_SR)}$		Slave receiver	5.5	-	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	1	-	-	
$t_{h(SD_B_SR)}$		Slave receiver	1	-	-	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	-	12.5	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8	-	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	-	12.5	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	8.8	-	-	

1. *APB clock frequency must be at least twice SAI clock frequency.*

Figure 51. SAI master timing waveforms

Figure 52. SAI slave timing waveforms

6.3.35.6 *SD/SDIO MMC card host interface (SDMMC) characteristics*

Unless otherwise specified, the parameters given in Table 107 for the SDIO/MMC interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set as table below
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output characteristics.

Table 107. SDMMC GPIO OSPEEDR settings for timing measurements

Voltage range (V)	Max clock frequency (MHz)	OSPEEDRy[1:0]	
		Clock	Data
1.71 - 1.89 and 2.7 - 3.6	26/25	00	00

Voltage range (V)	Max clock frequency (MHz)	OSPEEDRy[1:0]	
		Clock	Data
1.71 - 1.89 and 2.7 - 3.6	52/50	01	00
	DDR 52/50	01	01
	100	01	00
2.7 - 3.6[(1)]	120	11	10
1.71 - 1.89[(1)]	166	11	10

1. *With 20 pF load.*

Table 108. SDMMC characteristics for SD-Card or SDIO usage

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode. 20 pF load.	V_{DDIOx} = 2.7 V to 3.6 V	0	-	120	MHz
		V_{DDIOx} = 1.71 V to 1.89 V	0	-	166	
clock_ratio	SDMMC_CK / f_{pclk} frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 52 MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in High-Speed/SDR/DDR mode[(1)]						
t_{ISU}	Input setup time HS	-	2	-	-	ns
t_{IH}	Input hold time HS	-	2	-	-	
t_{IDW}[(2)]	Input valid window (variable window)	-	2.5	-	-	
CMD, D outputs (referenced to CK) in high-speed/SDR/DDR mode[(1)]						
t_{OV}	Output valid time HS	-	-	7.5	8	ns
t_{OH}	Output hold time HS	-	4.5	-	-	
CMD, D inputs (referenced to CK) in default mode						
t_{ISUD}	Input setup time SD	-	2.5	-	-	ns
t_{IHD}	Input hold time SD	-	2	-	-	
CMD, D outputs (referenced to CK) in default mode						
t_{OVD}	Output valid default time SD	-	-	1	2	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. *SD-Card 3 V / 1.8 V support on SDMMC3 requires an external voltage translator for which timings should be taken into account.*
2. *The minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

Table 109. SDMMC characteristics for e•MMC usage

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode. 20 pF load.	V_{DDIOx} = 2.7 V to 3.6 V	0	-	120	MHz
		V_{DDIOx} = 1.71 V to 1.89 V	0	-	166	
clock_ratio	SDMMC_CK/f_{pclk} frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	-	8.5	9.5	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK)						
t_{ISU}	Input setup time HS	-	2	-	-	ns
t_{IH}	Input hold time HS	-	2	-	-	
t_{IDW}[1]	Input valid window (variable window)	-	2.5	-	-	
CMD, D outputs (referenced to CK)						
t_{OV}	Output valid time HS	-	-	7.5	8	ns
t_{OH}	Output hold time HS	-	4.5	-	-	

1. *The minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

Figure 53. SD high-speed mode

Figure 54. SD default mode

Figure 55. SDMMC DDR mode

6.3.35.7 *FDCAN (controller area network) interface*

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (FDCANx_TX and FDCANx_RX).

6.3.35.8 *Ethernet (ETH) characteristics*

Unless otherwise specified, the parameters given in Table 111, Table 112, Table 113, Table 114, and Table 115 for ETH interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 00 (MII or RMII timings), 11 (MDIO/SMA, RGMII or RGMII-ID timings). OSPEEDRy[1:0] = 11 could be reduced to 10 if the experiment gives better signal integrity (for example, to reduce overshoot or undershoot on a light load).
- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled. For RGMII and RGMII-ID, the I/O compensation is fixed to RAPSRC = 8 and RANSRC = 7.
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output characteristics.

Table 110. GPIO advance configuration settings used for RGMII and RGMII-ID characterisation

Interface	Mode	Signals	GPIOx_ADVCFGR bits				GPIOx_DELAY field
			RET	INVCLK	DE	DLYPATH	DLY[3:0]
ETH1, ETH2	RGMII	ETHx_RGMII_RX_CTL	1	0	1	0	0b0000
		ETHx_RGMII_RXD[3:0]					
		ETHx_RGMII_TX_CTL					
		ETHx_RGMII_TXD[3:0]					
		Other ETHx_	0	0	0	0	0b0000
	RGMII_ID (GMAC side internal delays)(1)	ETHx_RGMII_RX_CLK	0	0	0	1	0b1101
		ETH1_RGMII_GTX_CLK	0	0	0	0	0b1100
		ETH2_RGMII_GTX_CLK	0	0	0	0	0b1011
		ETHx_RGMII_RX_CTL	1	0	1	0	0b0000
		ETHx_RGMII_RXD[3:0]					
		ETHx_RGMII_TX_CTL					
		ETHx_RGMII_TXD[3:0]					
		Other ETHx_	0	0	0	0	0b0000

1. *Use these settings only if a 2 ns internal delay is needed for RGMII timings. The delay values can be slightly tuned if required.*

Table 111. Ethernet MAC timings for MDIO/SMA

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (2.5 MHz)	-	-	400	-	ns
$t_{d(MDIO)}$	Write data valid time	-	0	1	2	
$t_{su(MDIO)}$	Read data setup time	-	8	-	-	
$t_{h(MDIO)}$	Read data hold time	-	0	-	-	

Figure 56. Ethernet MDIO/SMA timing diagram

Table 112. Ethernet MAC timings for RMII

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	-	2.5	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	-	1.5	-	-	
$t_{su(CRS)}$	Carrier sense setup time	-	1.5	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	-	1.5	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	-	7.5	11.5	12.5	
$t_{d(TXD)}$	Transmit data valid delay time	-	7.5	11.5	12.5	

Figure 57. Ethernet RMII timing diagram

Table 113. Ethernet MAC timings for MII

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	-	3.5	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	-	1	-	-	
$t_{su(DV)}$	Data valid setup time	-	2	-	-	
$t_{ih(DV)}$	Data valid hold time	-	1	-	-	
$t_{su(ER)}$	Error setup time	-	1	-	-	
$t_{ih(ER)}$	Error hold time	-	1	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	-	7.5	11	12	
$t_{d(TXD)}$	Transmit data valid delay time	-	7.5	11	12	

Figure 58. Ethernet MII timing diagram

Table 114. Ethernet MAC timings for RGMII

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{cyc}	Clock cycle duration	-	7.2	8	8.8	ns
D_{CLK}	GTX_CLK duty cycle	-	45	-	55	%
$t_{su(RXD)}$	Receive data setup time to RX_CLK falling edge	(1)	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time from RX_CLK falling edge	(1)	1	-	-	
$t_{su(RX_CTL)}$	Receive control valid setup time to RX_CLK falling edge	(1)	1	-	-	
$t_{ih(RX_CTL)}$	Receive control valid hold time from RX_CLK falling edge	(1)	1	-	-	
$t_{skew(TX_CTL)}$	Transmit control valid delay time from GTX_CLK rising edge	-	-0.5	0.25	0.5	
$t_{skew(TXD)}$	Transmit data valid delay time from GTX_CLK rising edge	-	-0.5	0.25	0.5	

1. *Test done at 100 MHz with signal rise and fall time < 1.8 ms.*

Figure 59. Ethernet RGMII timing diagram

Table 115. Ethernet MAC timings for RGMII_ID

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
t_{cyc}	Clock cycle duration	-	7.2	8	8.8	ns
D_{CLK}	GTX_CLK duty cycle	-	45	-	55	%
$t_{su(RXD)}$	Receive data setup time to RX_CLK falling edge	(1)	1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time from RX_CLK falling edge	(1)	-	-	0.5	
$t_{su(RX_CTL)}$	Receive control valid setup time to RX_CLK falling edge	(1)	-1	-	-	
$t_{ih(RX_CTL)}$	Receive control valid hold time from RX_CLK falling edge	(1)	-	-	0.5	
$t_{suT(TX_CTL)}$	Transmit control valid setup time to GTX_CLK falling edge	-	1.2	-	-	
$t_{suT(TXD)}$	Transmit data valid setup time to GTX_CLK falling edge	-	1.2	-	-	
$t_{hT(TX_CTL)}$	Transmit control valid hold time from GTX_CLK rising edge	-	1.2	-	-	
$t_{hT(TXD)}$	Transmit data valid hold time from GTX_CLK rising edge	-	1.2	-	-	

1. *Test done at 100 MHz with signal rise and fall time < 1.8 ns.*

Figure 60. Ethernet RGMII-ID timing diagram

6.3.35.9 *USART (SPI mode) interface characteristics*

Unless otherwise specified, the parameters given in Table 116 for USART are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 116, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Refer to Section 6.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 116. USART (SPI mode) characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	SPI master mode	-	-	16.5	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	SPI slave mode	-	-	33	MHz
		SPI slave receiver mode	-	-	44	
$t_{su(NSS)}$	NSS setup time	SPI slave mode	t_{ker} + 4[(1)]	-	-	ns
$t_{h(NSS)}$	NSS hold time	SPI slave mode	1	-	-	ns
$t_{w(CKH)}$, $t_{w(CKL)}$	CK high and low time	SPI master mode	1 / f_{CK} / 2 - 1	1 / f_{CK} / 2	1 / f_{CK} / 2 + 1	ns
$t_{su(RX)}$	Data input setup time	SPI master mode	13	-	-	ns
		SPI slave mode	5	-	-	
$t_{h(RX)}$	Data input hold time	SPI master mode	0	-	-	ns
		SPI slave mode	0.5	-	-	
$t_{v(TX)}$	Data output valid time	SPI slave mode	-	13.5	14	ns
		SPI master mode	-	4	4.5	
$t_{h(TX)}$	Data output hold time	SPI slave mode	7	-	-	ns
		SPI master mode	1	-	-	

1. *t_{ker} is the usart_ker_ck_pres clock period defined in the product reference manual.*

Figure 61. USART timing diagram in SPI master mode

Figure 62. USART timing diagram in SPI slave mode

6.3.36 Embedded PHYs characteristics

6.3.36.1 DDR PHY characteristics

Table 117. DDR PHY characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ZQ}	External resistor on DDR_ZQ	-	237.6	240	242.4	Ω
DDR4, 2400 Mbit/s, 32-bit, 10 ACx4, 1 Rank, DBI off						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	135	235	mA
		Write	-	175	290	
		Idle	-	80.5	165	
		DFI_LP	-	26	97.5	
		Inactive	-	3.65	70	
		Retention[2]	OFF			
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]	OFF			
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	415	490	mA
		Write	-	310	360	
		Idle	-	72	84.5	
		DFI_LP	-	2.85	5.5	
		Inactive	-	0.12	1.9	
		Retention[2]	-	0.017	1.7	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DDR4, 2400 Mbit/s, 16-bit, 10 ACx4, 1 Rank, DBI off						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	93.5	160	mA
		Write	-	115	190	
		Idle	-	65	125	
		DFI_LP	-	22	70	
		Inactive	-	3.65	70	
		Retention[2]	OFF			
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]	OFF			
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	235	275	mA
		Write	-	180	215	
		Idle	-	37	43	
		DFI_LP	-	1.9	3.6	
		Inactive	-	0.12	1.35	
		Retention[2]	-	0.017	1.2	
DDR3L, 2133 Mbit/s, 32-bit, 10 ACx4, 1 Rank						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	130	210	mA
		Write	-	170	275	
		Idle	-	76.5	150	
		DFI_LP	-	25	86.5	
		Inactive	-	3.6	60	
		Retention[2]	OFF			
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]	OFF			
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	420	475	mA
		Write	-	475	530	
		Idle	-	71.5	79.5	
		DFI_LP	-	3.25	5.85	
		Inactive	-	0.135	2	
		Retention[2]	-	0.0225	1.75	
DDR3L, 2133 Mbit/s, 16-bit, 10 ACx4, 1 Rank						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	88.5	145	mA
		Write	-	110	175	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Idle	-	62.5	115	mA
		DFI_LP	-	21	62.5	
		Inactive	-	3.6	60	
		Retention[2]	OFF			
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]	OFF			
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	245	275	mA
		Write	-	270	305	
		Idle	-	39.5	44.5	
		DFI_LP	-	2.15	3.85	
		Inactive	-	0.135	1.4	
		Retention[2]	-	0.0225	1.2	
LPDDR4, 2400 Mbit/s, 32-bit, 10 ACx4, 1 Rank, DBI off						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	140	245	mA
		Write	-	165	285	
		Idle	-	73	160	
		DFI_LP	-	25	99	
		Inactive	-	3.65	70.5	
		Retention[2]	OFF			
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]	OFF			
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	125	150	mA
		Write	-	480	545	
		Idle	-	49.5	57.5	
		DFI_LP	-	2.6	4.85	
		Inactive	-	0.11	1.75	
		Retention[2]	-	0.0185	1.55	
LPDDR4, 2400 Mbit/s, 16-bit, 10 ACx4, 1 Rank, DBI off						
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Read	-	91	160	mA
		Write	-	110	185	
		Idle	-	59.5	120	
		DFI_LP	-	22	70	
		Inactive	-	3.65	70.5	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDDCORE(DDRPHY)}$[1]	Supply current on V_{DDCORE}	Retention[2]	OFF			mA
$I_{VDDA18DDR}$[1]	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention[2]	OFF			
$I_{VDDQDDR}$[1]	Supply current on V_{DDQDDR}	Read	-	110	125	mA
		Write	-	285	325	
		Idle	-	48.5	56	
		DFI_LP	-	1.7	3.2	
		Inactive	-	0.11	1.25	
		Retention[2]	-	0.0185	1.1	
Low-power exit latency						
t_{EXIT}	Exit latency from DFI_LP state	-	-	2	-	DFI_CLK
	Exit latency from inactive state	DDR3L, DDR4	-	3	-	µs
		LPDDR4	-	3 + 2560 DDR_CLK	-	
	Exit latency from retention state after supplies restored	DDR3L, DDR4	-	3	-	
		LPDDR4	-	3 + 2560 DDR_CLK	-	

1. *Evaluated by characterization, not tested in production.*
2. *V_{DDCORE} OFF, $V_{DDA18DDR}$ OFF.*

6.3.36.2 DSI PHY characteristics

Table 118. DSI PHY characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{CK}	DSI link clock frequency	High-Speed mode (HS)		40	-	1250	MHz
rate	Data rate per lane	High-Speed mode (HS)		80	-	2500	Mbit/s
UI	Unit interval	equal to 0.5 / f_{CK} (HS)		0.4	-	12.5	ns
R_{EXT}	External resistor on REXT	Connected to ground		198	200	202	Ω
$I_{VDDCORE(DSIPHY)}$[1]	Supply current on V_{DDCORE}[2]	High-Speed Transmit[3]	4 lanes at 1 Gbit/s	-	1.55	9.6	mA
			4 lanes at 1.5 Gbit/s	-	2.05	11	
			4 lanes at 2 Gbit/s	-	2.55	11.5	
			4 lanes at 2.5 Gbit/s	-	3.05	12.5	
		LP Transmit	Lane 0 at 10 Mbit/s, PLL at 2.5 Gbit/s	-	2.05	10.5	
		ULPS Transmit	PLL disabled	-	0.155	8.05	
$I_{VDDA18DSI}$	Supply current on $V_{DDA18DSI}$[2]	High-Speed Transmit[3]	4 lanes	-	5.35	9.55	mA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{VDDA18DSI}$	Supply current on $V_{DDA18DSI}$[2]	LP Transmit	Lane 0 at 10 Mbit/s, PLL at 2.5 Gbit/s	-	3.85	5.05	mA
		ULPS Transmit	PLL disabled	-	0.0155	0.0385	
I_{VDDDSI}	Supply current on V_{DDDSI}	High-Speed Transmit[3]	4 lanes at 1 Gbit/s	-	14.5	19	mA
			4 lanes at 1.5 Gbit/s	-	17	23	
			4 lanes at 2 Gbit/s	-	19.5	26.5	
			4 lanes at 2.5 Gbit/s	-	22.5	30	
		LP Transmit	Lane 0 at 10 Mbit/s, PLL at 2.5 Gbit/s	-	7.45	10.5	
		ULPS Transmit	PLL disabled	-	0.0505	0.805	

1. *Evaluated by characterization, not tested in production.*
2. *values includes PLL power consumption.*
3. *HS mode: assume PRBS9 pattern on data lanes and 100% occupation; that is, continuous HS.*

6.3.36.3 CSI PHY characteristics

Table 119. CSI PHY characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{EXT}	External resistor on REXT	Connected to ground		198	200	202	Ω
$I_{VDDCORE(CSIPHY)}$[1]	Supply current on V_{DDCORE}	High-speed receive[2]	2 lanes at 1 Gbit/s	-	2.8	12	mA
			2 lanes at 1.5 Gbit/s	-	3.7	13	
			2 lanes at 2 Gbit/s	-	4.7	14.5	
			2 lanes at 2.5 Gbit/s	-	5.7	15.5	
		LP receive	Lane 0 at 10 Mbit/s	-	0.71	8	
		ULPS receive	ck_ker_csi2phy stopped	-	0.35	8.4	
$I_{VDDA18CSI}$[1]	Supply current on $V_{DDA18CSI}$	High-speed receive[2]	2 lanes at 1 Gbit/s	-	2.2	2.85	mA
			2 lanes at 1.5 Gbit/s	-	2.3	3	
			2 lanes at 2 Gbit/s	-	2.6	3.35	
			2 lanes at 2.5 Gbit/s	-	2.6	3.35	
		LP receive	Lane 0 at 10 Mbit/s	-	1.7	2.3	
		ULPS receive	ck_ker_csi2phy stopped	-	0.015	0.1	
I_{VDDCSI}[1]	Supply current on V_{DDCSI}	High-speed receive[2]	2 lanes at 1 Gbit/s	-	3.95	5.1	mA
			2 lanes at 1.5 Gbit/s	-	4.5	5.8	
			2 lanes at 2 Gbit/s	-	3.8	5.5	
			2 lanes at 2.5 Gbit/s	-	4.3	6	
		LP receive	Lane 0 at 10 Mbit/s	-	0.9	1.5	
		ULPS receive	ck_ker_csi2phy stopped	-	0.04	0.6	

1. *Evaluated by characterization, not tested in production.*
2. *HS mode: assume PRBS9 pattern on data lanes and 100% occupation; that is, continuous HS.*

6.3.36.4 LVDS PHY characteristics

Table 120. LVDS PHY characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
LVDS lane characteristics							
V_{OH}	Output voltage high	-(1)		1350	1400	1450	mV
V_{OL}	Output voltage low	-(1)		995	1000	1050	mV
$\|V_{OD}\|$	Output differential voltage	-(1)		340	370	420	mV
V_{OS}	Output offset voltage	-(1)		1150	1200	1250	mV
R_O	Output impedance, single ended	-(1)		44	60.5	76.5	Ω
ΔR_O	Ro mismatch between P and N output	-		-	-	8	%
$\|\Delta V_{OD}\|$	Change in $\|V_{OD}\|$ between 0 and 1	-		0.42	-	2.6	mV
ΔV_{OS}	Change in V_{OS} between 0 and 1	-(1)		0.22	2.55	26	mV
Is	Output current (drawn from $V_{DDA18LVDS}$)	Static current on 100Ω differential load		2.6	3.3	3.6	mA
		Outputs shorted to ground		11	15	24	mA
		Outputs shorted together		2.25	3.25	8.05	mA
t_f	V_{OD} fall time, 20 – 80%(3)(4)	-(1)		205	245	320	ps
t_r	V_{OD} rise time, 20 – 80%(3)(4)	-(1)		205	255	320	ps
ppV_{OD}	Dynamic output signal balance(3)(4)	-(2)		41	72	125	mV
LVDS bandgap characteristics							
$I_{VDDA18LVDS}$	Bandgap supply current on $V_{DDA18LVDS}$	-	-	-	0.805	1.25	mA
$I_{VDDLVDS}$	Bandgap supply current on V_{DDLVDS}	-	-	-	3.25	3.95	mA

1. *Steady state (~ DC level) at lowest possible data rate (2 Mbit/s) with both voltage and current driver enabled.*
2. *At maximum speed with both voltage and current driver enabled.*
3. *Loading conditions are: two 50Ω resistors, two 2.5 pF caps at each output, one 2.5 pF cap at middle point.*
4. *Specification for default configuration (no pre-emphasis).*

6.3.36.5 USB2PHY characteristics

Table 121. USB high-speed PHY characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{TXRTUNE}$	External resistor on TXRTUNE	Connected to ground	198	200	202	Ω
$I_{VDDCORE(USB2PHY)}$(1)	Supply current on V_{DDCORE}	HS transmit, maximum transition density(2)	-	10	27	mA
		HS transmit, minimum transition density(3)	-	8.15	23.5	
		HS idle(4)	-	9.25	23	
		FS transmit, maximum transition density(5)	-	9.2	27.5	
		LS transmit, maximum transition density(6)	-	7.85	20	
		Suspend(7)	-	0.038	6.05	
		Sleep(8)	-	2.45	13	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{VDDCORE(USB2PHY)}$[1]	Supply current on V_{DDCORE}	Battery charging	VDATDETENB = 0, VDATSRCENB = 1[9]	-	2.4	11.5	mA
			VDATDETENB = 1, VDATSRCENB = 1	-	4.75	15.5	
$I_{VDDA18USB}$[1]	Supply current on $V_{DDA1V8USB}$	HS transmit, maximum transition density[2]		-	16.5	18.5	mA
		HS transmit, minimum transition density[3]		-	14.5	15.5	
		HS idle[4]		-	4.9	5.85	
		FS transmit, maximum transition density[5]		-	4.9	5.9	
		LS transmit, maximum transition density[6]		-	5.1	6.15	
		Suspend[7]		-	0.024	0.0945	
		Sleep[8]		-	0.031	0.0945	
		Battery charging	VDATDETENB = 0, VDATSRCENB = 1[9]	-	3.55	4.55	
			VDATDETENB = 1, VDATSRCENB = 1	-	4.3	5.4	
$I_{VDD33USB}$[1]	Supply current on $V_{DD33USB}$	HS transmit, maximum transition density[2]		-	3.05	3.2	mA
		HS transmit, minimum transition density[3]		-	2.2	2.55	
		HS idle[4]		-	2.1	2.4	
		FS transmit, maximum transition density[5]		-	12.5	16	
		LS transmit, maximum transition density[6]		-	12	16.5	
		Suspend[7]		-	0.029	0.0785	
		Sleep[8]		-	0.067	0.115	
		Battery charging	VDATDETENB = 0, VDATSRCENB = 1[9]	-	2.1	2.4	
			VDATDETENB = 1, VDATSRCENB = 1	-	2.1	2.4	

1. *Evaluated by characterization, not tested in production.*
2. *Packet transmission by one transceiver operating in device mode while driving all 0s data (constant JKJK on DP/DM). Loading of 10 pF. Transfers do not include any interpacket delay.*
3. *Packet transmission by one transceiver operating in device mode while driving all 1s data (alternating 7-bit strings of J, then K on DP/DM). Loading of 10 pF. Transfers do not include any interpacket delay.*
4. *HS receive mode with no traffic on the line.*
5. *Packet transmission by one transceiver operating in device mode while driving all 0s data (constant JKJK on DP/DM). Loading of 50 pF. Transfers do not include any interpacket delay.*
6. *Packet transmission by one transceiver operating in host mode while driving all 0s data (constant JKJK on DP/DM). Loading of 600 pF. Transfers do not include any interpacket delay.*
7. *Suspend when operating in device mode with no far-side host termination on DP/DM during measurements. Measurements taken when COMMONONN (SYSCFG_USB2PHYxCR.USB2PHYxCMN) is deasserted.*
8. *Sleep mode when operating in device mode with no far-side host termination on DP/DM during measurements.*
9. *PHY is in suspend (with clocks turned OFF), non-driving mode and operating as a portable device in the 'dead battery' condition.*

6.3.36.6 *UCPDPHY characteristics*

Table 122. UCPDPHY characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{BITRATE}$	Bit rate (ensured by adequate RCC and UCPD settings)		270	300	330	Kbps

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{RECEIVER}$	Local capacitance added on PCB on each CC line		200	470	600	pF
TRANSMITTER						
V_{SWING}	Voltage swing applies on CC pin to both no load condition and under the load condition.		1.05	1.125	1.2	V
Z_{DRIVER}	TX output impedance. Source output impedance at the Nyquist frequency of USB2.0 low speed (750 kHz) while the source is driving the CC line.		33	-	75	Ω
T_r / T_f	Rise / Fall Time. 10% to 90% / 90% to 10% amplitude points, minimum is under an unloaded condition. Maximum set by TX mask.		300	-	735	ns
DCYCLE	TX duty cycle at 0.5625 V (see Y5Tx , BMC Tx 'ONE' mask and BMC Tx 'ZERO' mask in the PD Specification)(1)		47	-	53	%
RECEIVER						
V_{IL}	Rx receive input thresholds. The position of the center line of the inner mask is dependent on whether the receiver is sourcing or sinking power or is power neutral(1)	sourcing power	-	-	0.4825	V
V_{IH}			0.8925	-	-	
V_{IL}		sinking power	-	-	0.2325	V
V_{IH}			0.6425	-	-	
Hysteresis	Rx receive input hysteresis		0.15	-	-	
N_{COUNT}(2)	Number of transitions for signal detection (number to count to detect non-idle bus).		3	-	-	-
$t_{TRANWIN}$(2)	Time window for detecting non-idle bus.		12	-	20	µs
Z_{BMCRX}(3)	Receiver input impedance		1	-	-	MΩ

1. *Refer to the "USB Power Delivery (PD) Specification" Revision 3.1, Version 1.8.*
2. *BMC packet collision is avoided by the detection of signal transitions at the receiver. Detection is active when a minimum of NCOUNT transitions occur at the receiver within a time window of $t_{TRANWIN}$. After waiting $t_{TRANWIN}$ without detecting NCOUNT transitions, the bus is declared idle. This times are informative for UCPDPHY as it is done digitally inside UCPD Peripheral.*
3. *Does not include pull-up or pull-down resistance from cable detect. Transmitter is Hi-Z.*

6.3.37 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in Table 123 and Table 124 for JTAG/SWD are derived from tests performed under the ambient temperature, frequency and V_{DD} supply voltage summarized in Table 17. General operating conditions , with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}

Refer to I/O port characteristics for more details on the input/output characteristics.

Table 123. JTAG dynamic characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp}	TCK clock frequency	-	-	-	45	MHz
$1/t_{c(TCK)}$						
$t_{isu(TMS)}$	TMS input setup time	-	2	-	-	ns
$t_{ih(TMS)}$	TMS input hold time	-	1	-	-	
$t_{isu(TDI)}$	TDI input setup time	-	3	-	-	
$t_{ih(TDI)}$	TDI input hold time	-	0.5	-	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{ov\ (TDO)}$	TDO output valid time	-	-	9	11	ns
$t_{oh(TDO)}$	TDO output hold time	-	7	-	-	

Figure 63. JTAG timing diagram

Table 124. SWD dynamic characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp} $1/t_{c(SWCLK)}$	SWCLK clock frequency	-	-	-	80	MHz
$t_{isu(SWDIO)}$	SWDIO input setup time	-	1.5	-	-	ns
$t_{ih(SWDIO)}$	SWDIO input hold time	-	2.5	-	-	
$t_{ov\ (SWDIO)}$	SWDIO output valid time	-	-	9	12.5	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	5	-	-	

Figure 64. SWD timing diagram

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 Device marking

Refer to technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use.

In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

7.2 TFBGA361 package information (B0N8)

This TFBGA is a 361-ball, 16 x 16 mm thin fine pitch ball grid array package.

Figure 65. TFBGA361 - Outline

1. *Drawing is not to scale.*

Table 125. TFBGA361 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.20	-	-	0.0472
A1[3]	0.24	-	-	0.0094	-	-
A2	-	0.70	-	-	0.0276	-
b[4]	0.38	0.43	0.48	0.0150	0.0169	0.0189
D	16.00 BSC[5]			0.6299 BSC		
D1	14.40 BSC			0.5669 BSC		
E	16.00 BSC			0.6299 BSC		
E1	14.40 BSC			0.5669 BSC		
e[6]	0.80 BSC			0.0315 BSC		
N[7]	361					
SD	0.80 BSC			0.0315 BSC		
SE	0.80 BSC			0.0315 BSC		
aaa[8]	0.15 BSC			0.0059 BSC		
ccc[8]	0.20 BSC			0.0079 BSC		
ddd[8]	0.15 BSC			0.0059 BSC		
eee[8]	0.15 BSC			0.0059 BSC		
fff[8]	0.08 BSC			0.0031 BSC		

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
3. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance.*
6. *e represents the solder ball grid pitch.*
7. *N represents the total number of balls on the BGA.*
8. *Tolerance of form and position definitions.*

7.3 VFBGA361 package information (B09U)

This VFBGA is a 361-ball, 10 x 10 mm, very thin fine pitch ball grid array package.

Figure 66. VFBGA361 - Outline

Table 126. VFBGA361 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.00	-	-	0.0394
A1[3]	0.155	-	-	0.0061	-	-
b[4]	0.260	0.310	0.360	0.0102	0.0122	0.0142
D[5]	10.00 BSC			0.3937 BSC		
D1	9.000 BSC			0.3543 BSC		
E	10.00 BSC			0.3937 BSC		
E1	9.000 BSC			0.3543 BSC		
e[6]	0.500 BSC			0.0197 BSC		
N[7]	361					
SD[8]	0.500			0.0197		
SE[8]	0.500			0.0197		
aaa[9]	0.150			0.0059		
ccc[9]	0.200			0.0079		
ddd[9]	0.080			0.0031		
eee[9]	0.150			0.0059		
fff[9]	0.050			0.0020		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane*
3. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table*
6. *e(x) represents the solder ball grid pitch(es).*
7. *N represents the total number of balls on the BGA.*
8. *Basic dimensions SD(x) & SE(y) are defined with respect to datums A and B. They define the position of the centre ball(s) of the ball matrix.*
9. *Tolerance of form and position drawing.*

7.4 VFBGA424 package information (B0MP)

This VFBGA is a 424-ball, 14 x 14 mm, very thin fine pitch ball grid array package.

Figure 67. **VFBGA424 - Outline**

1. *Drawing is not to scale.*
2. *Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.*

3. *The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.*

Table 127. VFBGA424 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.000	-	-	0.0394
A1[3]	0.155	-	-	0.0061	-	-
b[4]	0.260	0.310	0.360	0.0102	0.0122	0.0142
D[5]	14.000 BSC			0.5512 BSC		
D1[5]	13.000 BSC			0.5118 BSC		
E[5]	14.000 BSC			0.5512 BSC		
E1[5]	13.000 BSC			0.5118 BSC		
e[5][6]	0.500 BSC			0.0197 BSC		
e1[5][6]	1.000 BSC			0.0394 BSC		
N[7]	424					
SD[5][8]	0.500 BSC			0.0197 BSC		
SE[5][8]	0.500 BSC			0.0197 BSC		
SD1[5][8]	0.250 BSC			0.0098 BSC		
SE1[5][8]	0.250 BSC			0.0098 BSC		
aaa[9]	0.150			0.0059		
ccc[9]	0.200			0.0079		
ddd[9]	0.100			0.0031		
eee[9]	0.150			0.0059		
fff[9]	0.050			0.0020		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane*
3. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table*
6. *e(x) represents the solder ball grid pitch(es).*
7. *N represents the total number of balls on the BGA.*
8. *Basic dimensions SD(x) & SE(y) are defined with respect to datums A and B. They define the position of the centre ball(s) of the ball matrix.*
9. *Tolerance of form and position drawing.*

7.5 Package thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, can be calculated using the following equation:

$$T_J \max = T_A \max + \left(P_D \max \times \Theta_{JA}\right)$$

where:

- T_A max is the maximum ambient temperature in °C.

- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W.
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max:

$$P_D \max = P_{INT} \max + P_{I/O} \max)$$

- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins:

$$P_{I/O} \max = \sum \left(V_{OL} \times I_{OL}\right) + \sum \left(\left(V_{DDIOx} - V_{OH}\right) \times I_{OH}\right)$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 128. Package thermal characteristics

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	TFBGA361 16×16 mm	20.2	°C/W
		VFBGA361 10×10 mm	23.1	
		VFBGA424 14×14 mm	20.9	
Θ_{JB}	Thermal resistance junction-board	TFBGA361 16×16 mm	11.7	
		VFBGA361 10×10 mm	9.5	
		VFBGA424 14×14 mm	11.8	
Θ_{JC}	Thermal resistance junction-top case	TFBGA361 16×16 mm	5.5	
		VFBGA361 10×10 mm	5.7	
		VFBGA424 14×14 mm	5.5	

7.5.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air) available on www.jedec.org.
- For information on thermal management, refer to application note *"Guidelines for thermal management on STM32 applications" (AN5036)* available on www.st.com.

8 Ordering information

Example: STM32 MP 235 F AK 3 ␣ T

Device family

STM32 = Arm® -based 32- or 64-bit processor

Product type

MP = MPU product

Device subfamily

231 = STM32MP231 line

233 = STM32MP233 line

235 = STM32MP235 line

Security option

C = Secure boot, cryptography hardware, 1.2 GHz CPU1, 400 MHz GPU[(1)]

F = Secure boot, cryptography hardware, 1.5 GHz CPU1, 400 MHz GPU[(1)]

Package and ball count

AJ = TFBGA361 16x16, 361 balls pitch 0.8 mm

AL = VFBGA361 10x10, 361 balls pitch 0.5 mm

AK = VFBGA424 14x14, 424 balls pitch 0.5 mm

Junction temperature range

3 = -40 °C < T_J < +125 °C

Options

␣ (absent) = no options

Packing

T = Tape and reel

No character = tray or tube

1. *GPU is absent in some devices (see Section 2 for details).*

Note: For a list of available options (such as speed and package) or for further information on any aspect of this device, contact your nearest ST sales office.

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Revision history

Table 129. Document revision history

Date	Revision	Changes
16-Sep-2024	1	Initial release.
25-Oct-2024	2	Updated number of watchdogs on cover page and Table 1. STM32MP23xC/F features and peripheral counts. Updated Section 1: Introduction. Updated Section 2: Description. Deleted IWDG, WWDG and IPCC indexes in Figure 1. STM32MP23xC/F block diagram. Updated Section 3.13: Inter-processor communication controller (IPCC1). Updated Section 3.15: Bus-interconnect matrix. Updated title of Section 3.43.5: Independent watchdog (IWDG1/2/3/4) and Section 3.43.6: System window watchdog (WWDG1). Updated Figure 11. Power supply scheme. Replaced some DNU pins/balls by "Unusedx" in: • Figure 6. STM32MP23xC/F TFBGA361 ballout • Figure 7. STM32MP23xC/F VFBGA361 ballout • Figure 8. STM32MP23xC/F VFBGA424 ballout • Table 10. Legend/abbreviations used in the ballout table • Table 11. STM32MP23xC/F ball definitions Updated Table 37. High-speed external (HSE) user clock characteristics (analog bypass). Updated Section 6.3.7.3: High-speed external clock generated from a crystal/ceramic resonator. Updated Table 40. High-speed external (HSE) oscillator characteristics. Replaced HSE by HSI in footnote of Table 44. HSI oscillator characteristics. Updated Table 56. ESD absolute maximum ratings. Updated I_{leak} in Table 59. I/O static characteristics. Updated Table 88. DTS characteristics. Updated Table 107. SDMMC GPIO OSPEEDR settings for timing measurements. Updated Table 108. SDMMC characteristics for SD-Card or SDIO usage. Updated Table 109. SDMMC characteristics for e•MMC usage.
14-Apr-2025	3	Updated Table 14. Voltage characteristics. Updated footnote in Table 84. ADC characteristics. Updated Section 6.3.35.8: Ethernet (ETH) characteristics including the addition of: • GPIO advance configuration settings used for RGMII and RGMII-ID characterisation • Ethernet MAC timings for RGMII • Figure 59. Ethernet RGMII timing diagram • Ethernet MAC timings for RGMII_ID • Figure 60. Ethernet RGMII-ID timing diagram Updated Figure 65. TFBGA361 - Outline.

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