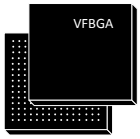
STM32MP211C/F STM32MP213C/F STM32MP215C/F

Datasheet

Arm® based Cortex®-A35 1.5 GHz + Cortex®-M33 MPU with TFT, 2× USB 2.0, crypto



VFBGA225 (8x8 pitch 0.5 mm)
VFBGA273 (11x11 pitch 0.5 mm)
TFBGA289 (14x14 pitch 0.8 mm)
VFBGA361 (10x10 pitch 0.5 mm)

Product summary	
STM32MP21xC/F	STM32MP211C, STM32MP211F, STM32MP213C, STM32MP213F, STM32MP215C, STM32MP215F

Features

Includes ST state-of-the-art patented technology.

Cores

- 64-bit single-core Arm® Cortex®-A35
  - Up to 1.5 GHz
  - 32-Kbyte I + 32-Kbyte D level 1 cache for each core
  - 128-Kbyte level 2 cache
  - Arm® NEON™ and Arm® TrustZone®
- 32-bit Arm® Cortex®-M33 with FPU/MPU
  - Up to 300 MHz
  - L1 16-Kbyte I / 16-Kbyte D
  - Arm® TrustZone®

Memories

- External DDR memory up to 4 Gbytes
  - DDR3L-1600 16-bit
  - DDR4-1600 16-bit
  - LPDDR4-1600 16-bit
- 456-Kbyte internal SRAM: 256-Kbyte AXI SYSRAM, 64-Kbyte AHB SRAM, 128-Kbyte AHB SRAM with ECC in backup domain, 8-Kbyte SRAM with ECC in backup domain
- One Octo-SPI memory interfaces
- Flexible external memory controller with up to 16-bit data bus: parallel interface to connect external ICs, and SLC NAND memories with up to 8-bit ECC

Security/safety

- Secure boot, TrustZone® peripherals, active tamper, environmental monitors, display secure layer, hardware accelerators
- Complete resource isolation framework

Reset and power management

- 1.71 to 1.95 V and 2.7/3.0 to 3.6 V multiple section I/O supply
- POR, PDR, PVD, and BOR
- On-chip LDO and power-switches for RETRAM, BKPSRAM, and VSW
- Dedicated supplies for Cortex®-A35
- Internal temperature sensor
- Low-power modes: Sleep, Stop, and Standby
- DDR memory retention in Standby mode
- Controls for PMIC companion chip

Low-power consumption

Clock management

- Internal oscillators: 64 MHz HSI, 16 MHz MSI, 32 kHz LSI
- External oscillators: 16-48 MHz HSE, 32.768 kHz LSE
- Up to 7× PLLs with fractional mode

General-purpose inputs/outputs

- Up to 123 secure I/O ports with interrupt capability
  - Up to six wake-up inputs
  - Up to seven tamper input pins + 5 active tampers output pins

Interconnect matrix

- Bus matrices
  - 128-, 64-, 32-bit STNoC interconnect, up to 600 MHz
  - 32-bit Arm® AMBA® AHB interconnect, up to 300 MHz

3 DMA controllers to unload the CPU

- 48 physical channels in total
- 3× dual master port, high-performance, general-purpose, direct memory access controller (HPDMA), 16 channels each

Up to 37 communication peripherals

- 3× I^2C FM+ (1 Mbit/s, SMBus/PMBus®)
- 3× I^3C (12.5 Mbit/s)
- 3× UART + 4× USART (12.5 Mbit/s, ISO7816 interface, LIN, IrDA, SPI) + 1× LPUART
- 6× SPI (50 Mbit/s, including 3 with full duplex I^2S audio class accuracy via internal audio PLL or external clock)(+1 with OCTOSPI + 4 with USART)
- 4× SAI (stereo audio: I^2S, PDM, SPDIF Tx)
- SPDIF Rx with four inputs
- 3× SDMMC up to 8-bit (SD/e•MMC™/SDIO)
- Up to 2× CAN controllers supporting CAN FD protocol, out of which one supports time-triggered CAN (TTCAN)
- 1× USB 2.0 high-speed Host with embedded 480 Mbits/s PHY
- 1× USB 2.0 high-speed dual role data with embedded 480 Mbits/s PHY
- Up to 2× Gigabit Ethernet interfaces
  - TSN, IEEE 1588v2 hardware, MII/RMII/RGMII
- Camera interface #1 (5 Mpixels at 30 fps)
  - MIPI CSI-2®, 2× data lanes up to 2.5 Gbit/s each
  - 8- to 16-bit parallel, up to 120 MHz
  - RGB, YUV, JPG, RawBayer with light ISP
  - Lite-ISP, demosaicing, downscaling, cropping, 3 pixel pipelines
- Camera interface #2 (1 Mpixels at 15 fps)
  - 8- to 14-bit parallel, up to 80 MHz
  - RGB, YUV, JPG
  - Cropping
- Digital parallel interface up to 16-bit input or output

5 analog peripherals

- 2 × ADCs with 12-bit max. resolution (up to 5 Msps each, up to 23 channels)
- Internal temperature sensor (DTS)
- 1× multifunction digital filter (MDF) with up to 4 channels/4 filters
- Internal (VREFBUF) or external ADC reference V_{REF+}

Graphics

- LCD-TFT controller, up to 24-bit // RGB888
  - Up to FHD (1920 × 1080) at 60 fps
  - 3 layers including a secure layer
  - YUV support

Up to 28 timers and 5 watchdogs

- 4× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input
- 2× 16-bit advanced motor control timers
- 10× 16-bit general-purpose timers (including 2 basic timers without PWM)
- 5× 16-bit low-power timers
- Secure RTC with subsecond accuracy and hardware calendar
- 4 Cortex®-A35 system timers (secure, nonsecure, virtual, hypervisor)
- 2× SysTick Cortex®-M33 timer (secure, nonsecure)
- 5× watchdogs (4× independent and 1× window)

Hardware acceleration

- 2x cryptographic processors (CRYP), AES-128, -192, -256, DES/TDES
- Secure AES-256 with SCA
- RSA, ECC, ECDSA with SCA
- 2x HASH (SHA-1, SHA-224, SHA-256, SHA3), HMAC
- 2x true random number generator
- CRC calculation unit
- “On-the-fly” DDR encryption/decryption (AES-128, AES-256)
- “On-the-fly” OTFDEC Octo-SPI flash memory decryption (AES-128)

Debug mode

- Arm® CoreSight™ trace and debug: SWD and JTAG interfaces

12288-bit fuses including 96-bit unique ID

All packages are ECOPACK2 compliant

1 Introduction

This document provides information on STM32MP21xC/F devices, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging and ordering information.

It must be read in conjunction with the STM32MP21xx reference manual (RM0506).

For information on the device errata with respect to the datasheet and reference manual, refer to the STM32MP21xC/F errata sheet (ES0628).

For information on the Arm® Cortex®- M33 core, refer to the Cortex®- M33 Technical Reference Manual, available from the www.arm.com website.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Description

STM32MP21xC/F devices are based on the high-performance core Arm® Cortex®-A35 64-bit RISC core operating at up to 1.5 GHz. The Cortex®-A35 processor includes a 32-Kbyte L1 instruction cache, a 32-Kbyte L1 data cache, and a 128-Kbyte L2 cache. The Cortex®-A35 processor uses a highly efficient 8-stage in-order pipeline that has been extensively optimized to provide full Armv8-A features while maximizing area and power efficiency.

STM32MP21xC/F devices also embed a Cortex®-M33 32-bit RISC core operating at up to 300 MHz frequency. The Cortex®-M33 core features a floating-point unit (FPU) single precision which supports Arm® single-precision data-processing instructions, and data types. The Cortex®-M33 supports a full set of DSP instructions, TrustZone®, and a memory protection unit (MPU) which enhances application security.

STM32MP21xC/F devices provide an external SDRAM interface supporting external memories up to 4 Gbytes, 16-bit DDR3L up to 800 MHz, 16-bit LPDDR4, or DDR4 up to 800 MHz. The SDRAM content can be encrypted with AES-128 or AES-256 with SCA protection.

The devices incorporate high-speed embedded memories: 456 Kbytes of internal SRAM (including 256-Kbyte AXI SYSRAM), one bank of 64 Kbytes of AHB SRAM, 128 Kbytes of AHB SRAM in backup domain, and 8 Kbytes of SRAM in backup domain), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, a 32-bit multi-AHB bus matrix, and a 128/64-bit multilayer AXI interconnect supporting access to internal and external memories.

Each device offers two ADCs, a low-power secure RTC, 12 general-purpose 16-bit timers, four general-purpose 32-bit timers, two PWM timers for motor control, five low-power timers, two true random number generator (RNG), two cryptographic acceleration cells and secure AES coprocessor with side channel attack (SCA) protection.

The devices support four multifunction digital filters (MDF)

The devices feature the following standard and advanced communication interfaces.

Standard peripherals

- Three I2Cs
- Three I3Cs
- Four USARTs and three UARTs
- One low-power UART
- Six SPIs, three I2Ss full-duplex master/slave. The I2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock.
- Four SAI serial audio interfaces
- One SPDIF Rx interface
- Three SDMMC interfaces
- A USB 2.0 Host with embedded Hi-Speed PHY
- A USB 2.0 dual-role data with Hi-Speed PHYs
- Two FDCAN interfaces, including one supporting TTCAN mode
- Two Gigabit Ethernet Interface, with TSN support

Advanced peripherals including

- A flexible memory control (FMC) interface
- One Octo-SPI flash memory interface , with on-the-fly content decryption
- Two camera interfaces for CMOS sensors, one with basic ISP, demosaicing and parallel or MIPI CSI interface
- An LCD-TFT display interface

A comprehensive set of power-saving mode allows the design of low-power applications.

STM32MP21xC/F devices are proposed in various packages up to 361 balls with 0.5 mm to 0.8 mm pitch.

These features make STM32MP21xC/F devices suitable for a wide range of consumer, industrial, white goods and medical applications.

Table 1. **STM32MP21xC/F features and peripheral counts**

Features			STM32MP21x
Package			VFBGA225 (8x8 pitch 0.5 mm) VFBGA273 (11x11 pitch 0.5 mm) TFBGA289 (14x14 pitch 0.8 mm) VFBGA361 (10x10 pitch 0.5 mm)
CPU processor			Single-Core Cortex® -A35 FPU Neon TrustZone®, up to 1500 MHz
	Size of cache		32-Kbyte L1 data cache
			32-Kbyte L1 instruction cache
			128-Kbyte L2 cache
	Frequency		Up to 1200 MHz Up to 1500 MHz (overdrive)
ROM			196 Kbytes
MCU processor			Cortex® -M33 FPU TrustZone®
	Size of caches		16-Kbyte data cache
			16-Kbyte instruction cache
	Frequency		300 MHz
Embedded SRAM	CPU system		256 Kbytes
	MCU system		64 Kbytes (tamper protected)
	MCU retention		128 Kbytes
	Backup		8 Kbytes (tamper protected)
SDRAM			Securable and on-the-fly data encryption (AES-128, AES-256) (1)
	DDR3L	800 MHz	1 Gbyte
	DDR4	800 MHz	4 Gbytes
	LPDDR4	800 MHz	2 Gbytes
Backup registers			512 Bytes (128x32-bits, tamper protected)
Timers	Advanced	16 bits	2
	General purpose	16 bits	Up to 8
		32 bits	4
	Basic	16 bits	2
	LP timer	16 bits	Up to 5
	Systick	24 bits	2 (Cortex® -M33, secure and nonsecure)
	Cortex-A35 (CNT)	64 bits	2 x 4 (secure, nonsecure, virtual, hypervisor)
	RTC		1
	Watchdog		5 (4 x independent, 1 x window)
Communication peripherals	SPI	Total	Up to 6
		having I2S	Up to 3
	I2C (with SMB/PMB support)		3
	I3C		3

Features			STM32MP21x
Communication peripherals	USART (Smartcard, SPI, IrDA, LIN) + UART (IrDA, LIN)		4 + up to 3
	LPUART		Up to 1
	SAI		4 (up to 8 audio channels), with I2S master/slave, PCM input, SPDIF-TX
	USB	USB 2.0 EHCI/OHCI host (USBH)	1 port
		USB 2.0 Host/Device	1 port
		Embedded PHYs	Up to 2 x Hi-Speed
	SPDIFRX		4 inputs
	FDCAN		Up to x2
SDMMC (SD, SDIO, eMMC)			Up to 3 (8 + 8 + 4 bits)
OCTOSPI			1
FMC	Parallel AD-Mux 16-bits		Up to 4 x CS, up to 4 x 64 Mbytes
	NAND 8		Yes, 4 x CS, SLC, BCH4/8
Gigabit Ethernet interfaces			Up to 2 x (R(G)MII, MII) with TSN support
LCD-TFT (LTDC)	**3** layers (incl 1 secure)		Up to 314 MHz pixel clock
	Parallel interface		Up to 24-bits 150 MHz pixel clock (up to 1080p60)
Camera interface			CSI-2 + RGB / RawBayer Parallel
	CSI-2 serial (CSI2 + DCMIPP)		2 x data lanes 2.5 Gbit/s each. Path shared with DCMIPP
	Parallel RGB/RawBayer (DCMIPP)		Up to 120 MHz. Path shared with CSI
	Image signal processing (ISP)		Yes, embedded inside DCMIPP
	Parallel RGB (DCMI)		Up to 60 MHz
Parallel interface (PSSI)			16-bit input or output, path shared with DCMI and DCMIPP
HPDMA			3 instances, 48 physical channels in total
Cryptography	CRYP (two instances)		DES/TDES (ECB, CBC), AES-128/192/256 (ECB, CBC, CTR, GCM, GMAC, CCM)
	SAES (with SCA)		AES-128/192/256 (ECB, CBC, CTR, GCM, GMAC, CCM), hardware attack protections, keys sharing to one instance of CRYP
	Public key accelerator (PKA) (with DPA protection)		Public key primitives for RSA, DH and ECC over GF(p). 64-bit core
Hash (HASH) (two instances)			SHA-1, SHA-2 and SHA-3 (up to 512), MD5, HMAC
Random number generator (RNG) (two instances)			True-RNG. FIPS 140-2 NDRNG (NIST SP800-90B certifiable)
CRC			x 1
Fuses (One time programming)			12288 effective bits
Multifonction digital filter (MDF)			4 input channels with 4 filters and sound activity detection
GPIOs	**with interrupt (total count)**		Up to 123

Features		STM32MP21x
	Wake-up pins	Up to 6
	Tamper input/active output pins	Up to 7 inputs and 5 outputs
Up to 12 bit ADC		2 (up to 4.8 Msps)
-	ADC channels in total (differential)	Up to 23 channels (or 11 differential)
	VREF generation (VREFBUF)	1.21 V, 1.5 V, or VREF+ input
	VREF+ input pin	Yes

1. *AES-128 for fast encryption, AES-256 with SCA protection for higher security protection on lower bandwidth code or data.*

Table 2. STM32MP21xx differences per product lines

Feature		STM32MP211x	STM32MP213x	STM32MP215x
Communication	FDCAN	No	2 (1 x TT-FDCAN), 10-Kbyte shared buffer	2 (1 x TT-FDCAN), 10-Kbyte shared buffer
Gigabit Ethernet interfaces	**External interfaces**	1, R(G)MII, MII	2, R(G)MII, MII	2, R(G)MII, MII
	GMAC (ETH), TSN, PTP and EEE	1	2	2
CSI-2 serial (1)		No	No	Up to 2x data lanes 2.5 Gbit/s each. Path shared with DCMIPP
LCD-TFT (LTDC) 24-bit parallel interface		No	No	Yes
CRYPTO	STM32MP21xC/F	Yes	Yes	Yes

1. *CSI-2 serial is used with DCMIPP. DCMIPP parallel interface is available on all product lines.*

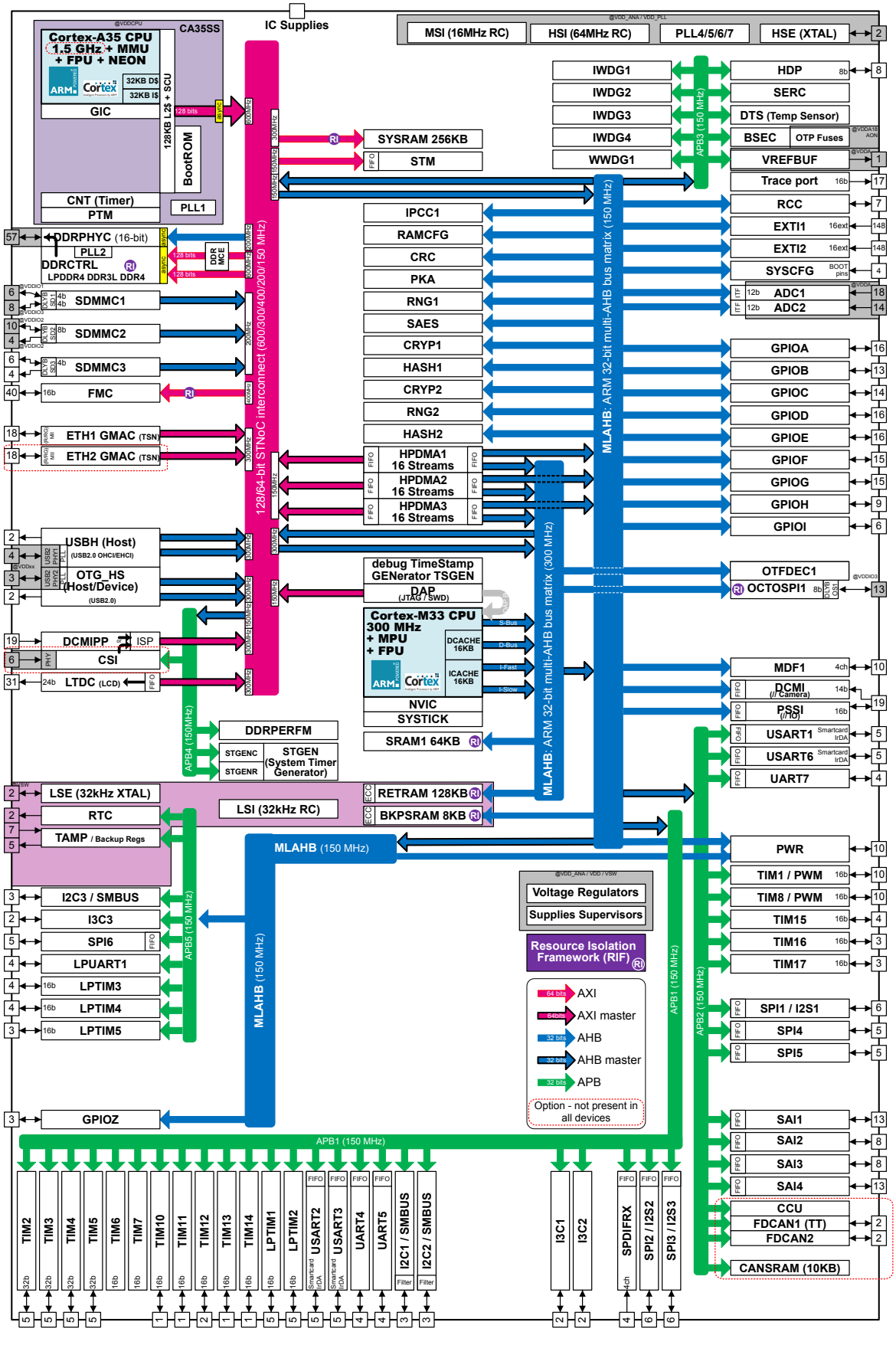
Table 3. STM32MP21xx differences per packages

Features		STM32MP21xxAO	STM32MP21xxAN	STM32MP21xxAM	STM32MP21xxAL
		VFBGA225	VFBGA273	TFBGA289	VFBGA361
Packages	Body size (mm)	8×8	11×11	14x14	10×10
	Pitch (mm)	0.5	0.5	0.8	0.5
	Thickness (mm)	1.0	1.0	1.2	1.0
	Ball count	225	273	289	361
GPIO	**with interrupt (total count)**	**98**	**123**	**123**	**123**
Limitations per package	CSI	No	Yes (1)	Yes (1)	Yes (1)
	FMC	8-bit, no FMC NOR	16-bit with D12 remapped	16-bit with D12 remapped	16-bit with D12 remapped(2)
	ADC ANA0/ ANA1 channels	No	Yes	Yes	Yes
	Tamper (in/out)	7/1	7/5	7/5	7/5
	Wake-up pins	5	6	6	6
	RTC_OUT	Only RTC1	x2	x2	x2
	LPUART1	No	Yes	Yes	Yes
	SPI2/I2S2	Yes, with signal remapped.	Yes	Yes	Yes
	TIM16/17	No	Yes	Yes	Yes
	LPTIM3/4/5	No	Yes	Yes	Yes
	SDMMC2(3)	4-bits No external level shifter control. Signal CK remapped. SDMMC2 not a boot source.	Full	Full	Full
	SDMMC3	No external level shifter control.	Full	Full	Full
	SAI4	Missing D1 (PDM)	Full	Full	Full
	TRACED	Missing TRACED [13, 12, 11, 8]	Full	Full	Full

1. *Yes only applies to STM32MP215 according to Table 2.*
2. *FMC 8-bit compatible with STM32MP25x 10x10 package.*
3. *SDMMC2 is not a boot source.*

Figure 1 shows the general block diagram of STM32MP21xC/F devices.

Figure 1. **STM32MP21xC/F block diagram**



3 Functional overview

3.1 Arm Cortex-A35 subsystem (CA35SS)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

3.1.1 Features

- Armv8-A architecture
- AArch32 for full backward compatibility with Armv7
- AArch64 for 64-bit support and new architectural features
- 32-Kbyte L1 instruction cache
- 32-Kbyte L1 data cache
- 128-Kbyte level2 cache
- Arm A64 + A32 + Thumb-2 instruction set
- Arm TrustZone security technology
- Arm NEON advanced SIMD
- DSP and SIMD extensions
- VFPv4 floating-point
- Hardware virtualization support
- Performance monitoring Unit (PMU)
- Program trace macrocell (PTM) that supports instruction trace only
- Integrated generic interrupt controller (GIC) with 384 peripheral interrupts
- Integrated generic timer (CNT)

Note: The cryptographic extension is not supported.

3.1.2 Overview

The Cortex-A35 processor uses a highly-efficient 8-stage in-order pipeline that has been extensively optimized to provide full Armv8-A features while maximizing area and power efficiency.

3.1.2.1 Thumb-2 technology

Delivers the peak performance of traditional Arm code, while also providing up to a 30 % reduction in memory requirement for instructions storage.

3.1.2.2 TrustZone technology

Ensures reliable implementation of security applications ranging from digital rights management to electronic payment. Broad support from technology and industry partners.

3.1.2.3 PMU

The PMU provides six performance monitors that can be configured to gather statistics on the operation of the core and the memory system. The information can be used for debug and code profiling.

3.1.2.4 NEON and FPU

Advanced SIMD is a media and signal processing architecture that adds instructions primarily for audio, video, 3-D graphics, image, and speech processing. The floating-point architecture provides support for single-precision and double-precision floating-point operations.

All scalar floating-point instructions are available in the A64 instruction set. All VFP instructions are available in A32 and T32 instruction sets. The same advanced SIMD instructions are available in both A32 and T32 instruction sets. The A64 instruction set offers additional advanced SIMD instructions, including double-precision floating-point vector operations.

3.1.2.5 *Hardware virtualization*

Highly efficient hardware support for data management and arbitration, whereby multiple software environments and their applications are able to simultaneously access the system capabilities. This enables the realization of devices that are robust, with virtual environments that are well isolated from each other.

3.1.2.6 *Optimized L1 caches*

Performance and power optimized L1 caches combine minimal access latency techniques to maximize performance and minimize power consumption. There is also the option of cache coherence for enhanced inter-processor communication.

3.1.2.7 *Integrated L2 cache controller*

Provides low-latency and high-bandwidth access to cached memory in high-frequency, or to reduce the power consumption associated with off-chip memory access.

3.1.2.8 *Generic interrupt controller (GIC)*

Implementing the standardized and architected interrupt controller, the GIC provides a rich and flexible approach to inter-processor communication, and the routing and prioritization of system interrupts.

Supporting up to 416 independent interrupts, under software control, each interrupt can be hardware prioritized, and routed between the operating system and TrustZone software management layer.

This routing flexibility and the support for virtualization of interrupts into the operating system, provide one of the key features required to enhance the capabilities of a solution utilizing an hypervisor.

3.2 Arm Cortex-M33 core with TrustZone and FPU (CM33)

The Arm Cortex-M33 core with TrustZone and FPU is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

It is comprised of:

- Arm TrustZone technology, using the Armv8-M main extension supporting secure and non-secure states
- Floating-point extension (FPU)
- Armv8-M DSP extension
- A nested vectored interrupt controller (NVIC) is closely integrated with the processor
- A memory system with memory protection unit (MPU) with up to 16 non-secure regions and 16 secure regions
- A security attribution unit (SAU) with up to eight regions
- An implementation defined attribution unit (IDAU)
- Debug components including breakpoints (BPU), data watchpoints (DWT), instrumentation, and processor trace (ITM/ETM), cross-trigger interface (CTI)
- 16-Kbyte instruction and 16-Kbyte data caches (ICACHE/DCACHE)

3.3 Memories

3.3.1 External SDRAM

STM32MP21xC/F devices embed a controller for the external SDRAM which supports the following devices

- DDR3L, 16- bit data, up to 1 Gbytes, up to DDR3L-1600 (800 MHz clock)
- DDR4, 16- bit data, up to 4 Gbytes, up to DDR4-1600 (800 MHz clock)
- LPDDR4, 16- bit data, up to 2 Gbytes, up to LPDDR4-1600 (800 MHz clock)

3.3.2 Embedded SRAM

All devices feature:

- SYSRAM in MPU domain: 256 Kbytes with half/full hardware erase mechanism on reset
- SRAM1 in MCU domain: 64 Kbytes with hardware erase mechanism on tamper detection

- RETRAM (retention RAM): 128 Kbytes with hardware erase mechanism on reset
  The content of this area can be retained in Standby or V_{BAT} mode, and can be protected by ECC and CRC mechanisms.
- BKPSRAM (backup SRAM): 8 Kbytes with hardware erase mechanism on tamper detection
  The content of this area can be protected against possible unwanted accesses, and can be retained in Standby or V_{BAT} mode. The content can also be protected by ECC mechanism.

3.4 DDR3L/DDR4/LPDDR4 controller (DDRCTRL)

DDRCTRL combined with DDRPHYC provides a complete 16-bit memory interface solution for DDR memory subsystem.

- JEDEC compliant LPDDR4 SDRAM up to 1600 MT/s
- JEDEC compliant DDR4 SDRAM up to 1600 MT/s with DLL on-range
- JEDEC compliant DDR3L SDRAM up to 1600 MT/s with DLL on-range
- 2 x 128-bit AXI4 ports
  - up to 16 QoS levels and up to 3 traffic classes are supported per direction.
  - CID-based firewalling function with poisoning output signaling
  - 1 port provided with AES- encryption/decryption with programmable memory range (DDRMCE)

Low-power features:

- Linked with the RCC, ability to move the DDR memory subsystem in self-refresh through automatic way, hardware way, or software way (ASR, HSR, and SSR).

3.5 Boot modes

At startup, the boot source used by the internal boot ROM is selected by BOOT pins and OTP settings.

Table 4. Default interfaces

Unless otherwise mentioned in the table below.

Boot source	When used by Cortex-A35	When used by Cortex-M33
SD card	SDMMC1	
e•MMC	SDMMC2 (1)	
Serial NOR, HyperFlash, and serial NAND	OCTOSPI1	
SLC NAND	FMC (2)	
USB	OTG (high-speed only)	-
UART	USART2, UART5, USART6	-

1. *SDMMC2 is not a boot source for the 8×8 VFBGA225 package.*
2. *FMC_NWE boot GPIO is different for the 8×8 VFBGA225 package.*

Table 5. Boot sources

BOOTx pins	Alternate boot pins OTP value							
	0b00 (default)				0b01	0b10	0b11	
	Cortex-A35 master	Cortex-M33 master	Cortex-M33 master (1)		Cortex-A35 master	Cortex-M33 master	Cortex-M33 master (1)	
			Cortex-A35	Cortex-M33			Cortex-A35	Cortex-M33
0	UART and USB (2) (3)							
1	SD card	-	-	-	SD card	SD card	-	-
2	*e*•MMC	-	-	-	*e*•MMC	*e*•MMC	*e*•MMC	Serial NOR
3	Development boot (3)							
4	Serial NOR	-	-	-	Serial NOR	Serial NOR	SLC NAND	Serial NOR
5	Serial NAND	-					*e*•MMC (4)	Serial NOR
6	SLC NAND	-					*e*•MMC (3)	HyperFlash
7	-	SD card	-	-	HyperFlash	HyperFlash	-	-
8	-	*e*•MMC	-	-	Serial NAND	Serial NAND	*e*•MMC	HyperFlash
9	-		Serial NAND	Serial NOR	-		SD card(5)	Serial NOR
10	-		SLC NAND	Serial NOR	-		SD card(5)	HyperFlash
11	-	Serial NOR	-	-	SLC NAND	SLC NAND	SLC NAND	HyperFlash
12	Development boot (3)							
13	-	-	*e*•MMC	Serial NOR	SD card(5)	SD card(5)	SD card	Serial NOR
14	-	-	SD card	Serial NOR	*e*•MMC (4)	*e*•MMC (4)	SD card	HyperFlash
15	UART and USB not found							

1. *Two flash configuration indirect Cortex-A35 boot (from Cortex-M33) or used during Cortex-A35 D1Standby exit.*
2. *Cannot be overridden by OTP.*
3. *Wait incoming connection on USART2, UART5 on default pins, and USB high-speed device on OTG_HSDP/HSDM.*
4. *e•MMC on SDMMC1.*
5. *SD card on SDMMC2.*

The pins used during boot are described in Table 3.

Note: There are few mutual exclusions with this default setting. SDMMC2 cannot be used with FMC.

Table 6. Minimum set of default pins used during boot ROM phase

Most can be changed using OTP settings. This table is for default OTP settings.

Interface	Type		Signal	Pin	I/O supply domain
FMC	SLC NAND 8 bits	SLC NAND 16 bits	FMC_NOE	PE15	V_{DDIO2} (1)
			FMC_RNB	PE13	
			FMC_NWE (2)	PE14	
			FMC_NCE1	PE12	
			FMC_ALE	PE8	
			FMC_CLE	PE11	
			FMC_D0	PE9	V_{DD}
			FMC_D1	PE6	
			FMC_D2	PE7	
			FMC_D3	PD15	

Interface	Type			Signal	Pin	I/O supply domain
FMC	SLC NAND 8 bits		SLC NAND 16 bits	FMC_D4	PD14	V_{DD}
				FMC_D5	PB13	
				FMC_D6	PD12	
				FMC_D7	PB14	
	-			FMC_D8	PB5	
				FMC_D9	PB6	
				FMC_D10	PB7	
				FMC_D11	PD13	
				FMC_D12	PB2	
				FMC_D13	PB9	
				FMC_D14	PB11	
				FMC_D15	PB10	
OCTOSPI1 Port1	Serial NOR	Serial NAND	HyperFlash	OCTOSPI1_CLK	PD0	V_{DDIO3}
				OCTOSPI1_NCS1	PD3	
				OCTOSPI1_IO0	PD4	
				OCTOSPI1_IO1	PD5	
	-			OCTOSPI1_IO2	PD6	
				OCTOSPI1_IO3	PD7	
				OCTOSPI1_IO4	PD8	
				OCTOSPI1_IO5	PD9	
				OCTOSPI1_IO6	PD10	
				OCTOSPI1_IO7	PD11	
				OCTOSPI1_NCLK	PD1	
				OCTOSPI1_DQS	PD2	
SDMMC1 (3)	SD card or *e*•MMC			SDMMC1_CK	PE3	V_{DDIO1}
				SDMMC1_CMD	PE2	
				SDMMC1_D0 (4)	PE4	
SDMMC2 (5)	SD card or *e*•MMC			SDMMC2_CK	PE14	V_{DDIO2} (1)
				SDMMC2_CMD	PE15	
				SDMMC2_D0 (4)	PE13	
USART2				USART2_RX	PA8	V_{DD}
				USART2_TX	PA4	
UART5				UART5_RX	PB15	V_{DD}
				UART5_TX	PA0	
USART6				USART6_RX	PF4	V_{DD}
				USART6_TX	PF5	

1. *Some FMC and SDMMC2 pins are shared: use of FMC is exclusive of use of SDMMC2.*
2. *On VFBGA225 FMC_NWE is mapped on GPIO PD13.*
3. *e•MMC can be connected to SDMMC1 as follows:*
   - *4-bit e•MMC: can be connected to SDMMC1 assigning four bits on V_{DDIO1} supply.*
   - *8-bit e•MMC: can be connected to SDMMC1 assigning four bits on V_{DDIO1} and four bits on V_{DDIO3} supplies. Beware that if SDMMC1 is used as 1.8 V 8-bit e•MMC then all I/Os on V_{DDIO3} are 1.8 V.*
4. *Only used as input by boot ROM.*

5. On the 8×8 VBGA225 package, SDMMC2 is not a boot source.

Although low-level boot is done using internal clocks, ST supplies software packages as well as major external interfaces (such as DDR or USB) that require a crystal or an external oscillator to be connected on HSE pins.

See the product reference manual for constrains and recommendations regarding connection of HSE pins and supported frequencies.

3.6 Power supply management (PWR)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

3.6.1 Power supply scheme

The system requires supply on V_{DD}, $V_{DDA18AON}$, V_{DDCPU} and V_{DDCORE} to start, and to allow independent supplies for $V_{DDA18ADC}$, V_{BAT}, $V_{DD33USB}$, V_{DDIO2}, V_{DDIO3}, V_{DDIO1}, and V_{DDQDDR}.

- V_{DD} power supply input for I/Os (1.8 V or 3.3 V typical)
- $V_{DDA18AON}$ power supply input for system analog such as reset, power management, oscillators and OTP
- V_{BAT} optional power supply input for backup domain when V_{DD} is not present (V_{BAT} mode)
- V_{DDCORE} digital core domain supply, dependent on V_{DD} supply. V_{DD} must be present before V_{DDCORE}.
  - V_{DDCSI} is usually connected to V_{DDCORE}.
- V_{DDCPU} digital CPU domain supply (Cortex-A35), dependent on V_{DD} supply. V_{DD} must be present before V_{DDCPU}.
- V_{DDQDDR} DDR I/O supply
- $V_{DDA18ADC}$ analog power supply input for ADCs and voltage reference buffers, independent from any other supply
- V_{REF+} external reference voltage for ADCs, independent from any other supply
  - reference voltage output when the voltage reference buffer is enabled
  - independent external reference voltage input when the voltage reference buffer is disabled
- V_{SSA} separate analog and reference voltage ground
- $V_{DD33USB}$ supply input for USB HS PHY, independent from any other supply
- V_{DDIO3} supply input, mostly for OCTOSPI1 I/Os, independent from any other supply
- V_{DDIO2} supply input, mostly for e.MMC I/Os, independent from any other supply
- V_{DDIO1} supply input, mostly for SD Card I/Os, independent from any other supply
- V_{SS} common ground for all supplies except for analog

3.6.2 Power-supply supervisor

The devices have an integrated power-on reset (POR) and power-down reset (PDR) circuitry, coupled with a brownout reset (BOR) circuitry:

- Power-on reset (POR)
  The POR supervisor monitors V_{DD} and $V_{DDA18AON}$ power supplies, and compares them to a fixed threshold. The devices remain in reset mode when V_{DD} and $V_{DDA18AON}$ are below this threshold.
- Power-down reset (PDR)
  The PDR supervisor monitors V_{DD} and $V_{DDA18AON}$ power supplies. A reset is generated when V_{DD} or $V_{DDA18AON}$ drops below a fixed threshold.
- Brownout reset (BOR)
  The BOR supervisor monitors V_{DD} power supply. A 2.7 V BOR thresholds can be enabled through option bytes. A reset is generated when V_{DD} drops below this threshold. The BOR must not be enabled when V_{DD} = 1.8 V typ. is used.
- Power-on reset V_{DDCORE} (POR_VDDCORE)
  The POR_VDDCORE supervisor monitors V_{DDCORE} power supply, and compares it to a fixed threshold. The V_{DDCORE} domain remains in reset mode when V_{DDCORE} is below this threshold,
- Power-down reset V_{DDCORE} (PDR_VDDCORE)
  The PDR_VDDCORE supervisor monitors V_{DDCORE} power supply. A V_{DDCORE} domain reset is generated when V_{DDCORE} drops below a fixed threshold.
- Power-on reset V_{DDCPU} (POR_VDDCPU)
  The POR_VDDCPU supervisor monitors V_{DDCPU} power supply, and compares it to a fixed threshold. The V_{DDCPU} domain remains in reset mode when V_{DDCPU} is below this threshold.

- Power-down reset V_{DDCPU} (PDR_VDDCPU)
  The PDR_VDDCPU supervisor monitors V_{DDCPU} power supply. A V_{DDCPU} domain reset is generated when V_{DDCPU} drops below a fixed threshold.
- Power-on reset V_{SW} (POR_VSW)
  The POR_VSW supervisor monitors V_{SW} power supply, and compares it to a fixed threshold. The V_{SW} domain remains in reset mode when V_{SW} is below this threshold.
- Power-down reset V_{SW} (PDR_VSW)
  The PDR_VSW supervisor monitors V_{SW} power supply. The V_{SW} domain reset is generated when V_{SW} drops below a fixed threshold.

The devices also include monitoring which can generate interrupt, or wake-up:

- Programmable voltage detector (PVD)
  The PVD monitors the PVD_IN pin, and compares it to a fixed threshold. An interrupt or a wake-up can be generated when PVD_IN is below or above the threshold.
- Peripheral voltage monitoring
  Monitors independently V_{DDIO2}, V_{DDIO3}, V_{DDIO1}, $V_{DD33USB}$ and $V_{DDA18ADC}$ power supplies with fixed thresholds. An interrupt or a wake-up can be generated when supplies are below or above the thresholds.

3.7 Low-power strategy

Several low-power modes are available to save power when the Cortex-A35 and/or the Cortex-M33 do not need to execute code (when waiting for an external event). It is up to the user to select the mode that gives the best compromise between low-power consumption, short startup time, and available wake-up sources.

- Slowing down system clocks (see RCC section in the reference manual)
- Controlling individual peripheral clocks (see RCC section in the reference manual)
- Low-power modes:
  - CSleep (CPU clock stopped)
  - CStop (CPU subsystem clock stopped)
  - D1 DStop1 (CPU subsystem clock stopped, normal mode signaled to external regulator)
  - D1 DStandby (domain power down and wake up via reset)
  - Stop1, LP-Stop1, and LPLV-Stop1 (system clock stalled, normal, or low-power mode signaled to external regulator supplying the VDDCPU and the VDDCORE)
  - Stop2, LP-Stop2, and LPLV-Stop2 (system clock stalled, powered down mode signaled to external regulator supplying the VDDCPU, and normal or low-power mode signaled to external regulator supplying the VDDCORE)
  - Standby (system powered down and V_{SW} domain in autonomous mode running with local clocks)

3.8 Resource isolation framework (RIF)

The RIF is a comprehensive set of hardware blocks designed to enforce and manage the isolation of STM32 hardware resources like memory and peripherals.

Within a defined hardware execution compartment (eight are available), privileged, unprivileged, secure, and non-secure application software can assign their own embedded memory buffers, external memory regions, and peripherals thanks to the RIF hardware.

The RIF architectural framework extends to FMC, SYSCFG, IPCC, DMA, RTC, TAMP, RCC, PWR, or GPIO.

3.9 Reset and clock controller (RCC)

The RCC manages the generation of all clocks, as well as the clock gating and the control of system and peripheral resets. It provides a high flexibility in the choice of clock sources, and allows application of clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the peripheral activity rate.

3.9.1 Features

- RIF aware
- Reset part:
  - Generation of local and system reset
  - Bidirectional pad reset (NRST) to reset of external devices, or to reset the device
  - Output pad reset (NRSTC1MS) to reset of external mass-storage devices used by the Cortex-A35
- Clock generation part:
  - Generation and distribution of clocks for the complete system
  - 5 separate PLLs (excluding external Cortex-A35, DDRCTRL):
    - Integer or fractional mode
    - Spread-spectrum function to reduce the amount of EMI peaks
    - Possibility to change on-the-fly the fractional ratios of the PLLs
  - Smart clock gating for reduction of power dissipation
  - 2 external oscillators:
    - HSE that supports a wide range of crystals: 16 to 48 MHz
    - LSE for 32.768 kHz crystals
  - 3 Internal oscillators:
    - HSI that runs around 64 MHz
    - MSI that runs around 16 MHz
    - LSI that runs around 32 kHz
  - Buffered clock outputs for external devices
  - 1 external CK_IN external kernel clock input for digital audio interfaces: SPI/I2S, SAI, and MDF or any PLL input.
- Two independent interrupt interfaces (one dedicated to Cortex-A35, and one dedicated to Cortex-M33)
- Two independent failure events (HSE and LSE)
- Two independent events to wake up processors (one dedicated to Cortex-A35 and one dedicated to Cortex-M33)

3.9.2 Clock management

The RCC provides a high flexibility to the application in the choice of the clock generators:

- From HSI, high-speed internal oscillator (~ 64 MHz)
- From HSE, high-speed external oscillator (16 to 48 MHz)
- From LSE; low-speed external oscillator (32 kHz)
- From LSI, low-speed internal oscillator (~ 32 kHz)
- From MSI, low-power internal oscillator (~ 16 MHz)
- From CK_IN, digital external input clock

The RCC offers a good flexibility for the application to select the appropriate clock for CPUs and peripherals. More especially for peripherals that need a specific clock like SPI(I2S), SAI, and SDMMC.

Each clock source can be switched on or off independently to optimize the power consumption.

There are mainly three clock paths:

- Cortex-A35 bus matrix
- Cortex-M33 and its bus matrix
- Peripheral kernel clocks

The Cortex-A35 and DDRCTRL clocking are derived locally because of high frequency use. The RCC manages only source clocks for their related local PLLs.

3.9.3 Reset sources

There are several sources able to generate a reset:

- Supply monitors (V_{DD}, V_{DDCORE}, V_{DDCPU} or V_{SW}) lower than expected values
- Independent watchdog timeout

- D1 domain exit from DStandby state
- Exit from Standby mode
- External signals driving the NRST pin
- Software commands

The coverage (or scope) of the resets differ according to the source initiating the reset, with the following categories:

- Power-on/off resets
- System resets
- Local resets

An application reset can be generated from one of the following sources:

- Reset from the NRST pin
- Reset from low-voltage detection on VDD
- Reset from the independent watchdogs
- Software reset from RCC registers
- Failure on HSE
- RETRAM CRC or ECC error

A system reset can be generated from one of the following sources:

- Reset from application reset
- Reset from low-voltage detection on V_{DDCORE}
- A reset from low-voltage detection on V_{DDCPU}

The NRST reset is activated by:

- Low voltage on V_{DD}
- Failure on HSE
- Reset from the independent watchdogs
- Software reset from RCC registers
- RETRAM CRC or ECC error
- Assertion of NRST by an external source

3.10 Inter-processor communication controller (IPCC1)

The IPCC is used to communicate data between two processors. It provides a non-blocking signaling mechanism to post and retrieve communication data in an atomic way (signaling for 16 channels).

The IPCC communication data must be in a common memory, which is not part of the IPCC.

3.10.1 Main features

- Status signaling for the four channels
  - Channel occupied/free flag, also used as lock
- Two interrupt lines per processor
  - One for RX channel occupied (communication data posted by sending processor)
  - One for TX channel free (communication data retrieved by receiving processor)
- Interrupt masking per channel
  - Channel occupied mask
  - Channel free mask
- Two channel operation modes
  - Simplex (each channel has its own communication data memory location)
  - Half duplex (a single channel in associated to a bidirectional communication data information memory location)

3.11 General-purpose input/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (with or without pull-up or pull-down), or as peripheral alternate function. Some of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/O registers.

Access to each GPIO configuration bits can be restricted to secure-only and/or privileged-only. These configuration bits can also be allocated to a specific CPU.

3.12 Bus-interconnect matrix

For more details on interconnect, see the reference manual (STM32MP21xx reference manual (RM0506)).

Figure 2. AXI STNoC multi-frequency network

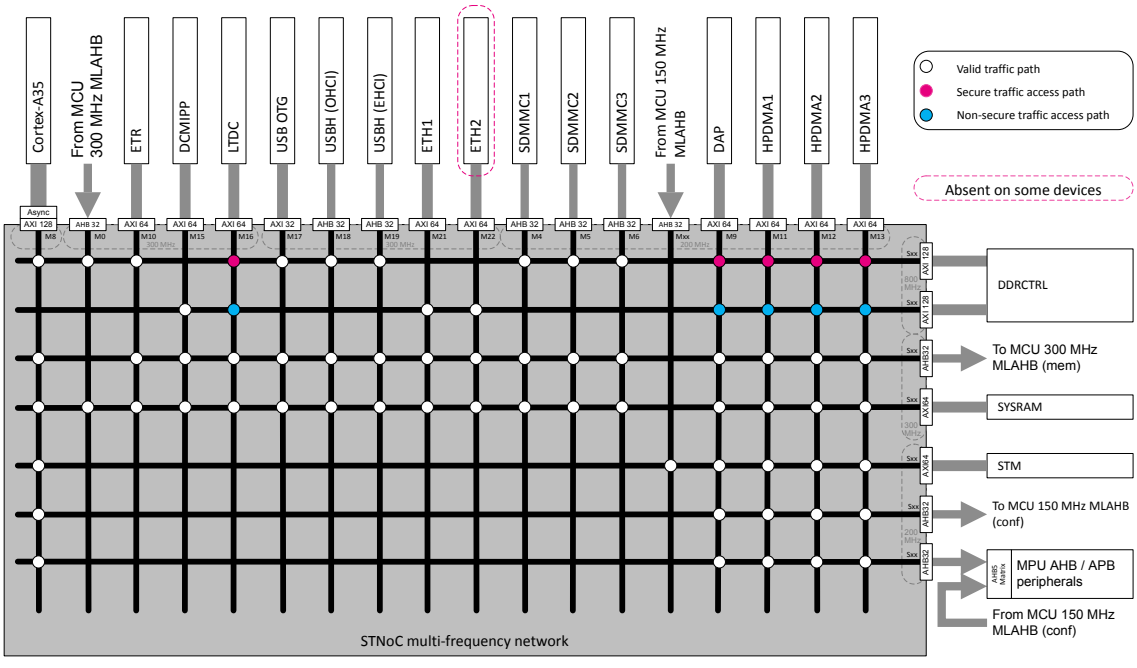


Figure 3. **MCU multi-Layer AHB 300 MHz**

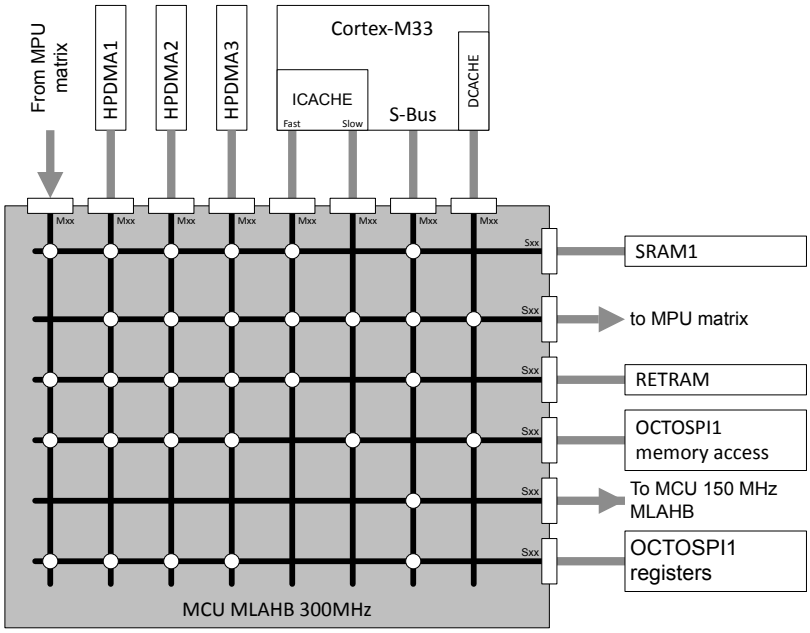


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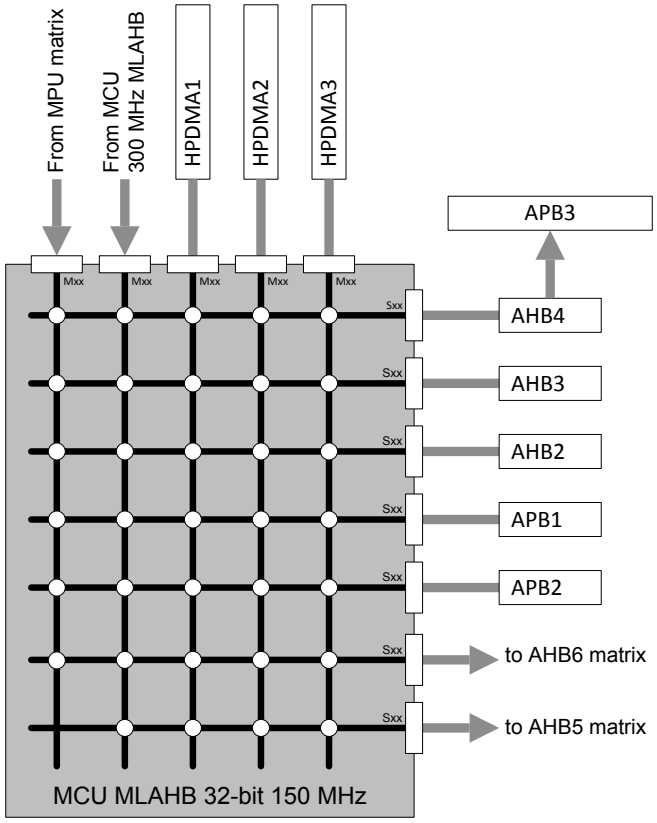
Figure 4. **MCU multi-Layer AHB 150 MHz**



DT73135V2

3.13 High-performance DMA controllers (HPDMA1/2/3)

- AXI master and AHB master

- Memory-mapped data transfers from a source to a destination:
  - Peripheral-to-memory
  - Memory-to-peripheral
  - Memory-to-memory
  - Peripheral-to-peripheral
- Autonomous data transfers during Sleep and Stop modes
- Per channel event generation
- Per channel interrupt generation
- 16 concurrent DMA channels
- Per channel FIFO
- Linked-list support
- TrustZone support
- Privileged/unprivileged support
- Channel isolation support

3.14 Extended interrupt and event controller (EXTI1/2)

The EXTI manages individual CPU and system wake-up through configurable and direct event inputs. It provides wake-up requests to the power control, and generates an interrupt request to the CPU NVIC or GIC, and events to the CPU event inputs. For each CPU, an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wake-up requests allow the system to be woken up from Stop mode, and CPUs to be woken up from CStop and CStandby modes.

The interrupt request and event request generation can also be used in Run mode.

The EXTI also includes the EXTI I/Oport selection.

Each interrupt or event can be set as secure to restrict access to secure software only.

EXTI1/2 are shared between Cortex-A35 and Cortex-M33.

3.15 Cyclic redundancy check calculation unit (CRC)

The CRC calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity.

The CRC calculation unit helps computing a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.16 Flexible memory controller (FMC)

The FMC main features are the following:

- Interface with static-memory mapped devices including:
  - NOR flash memory
  - Static or pseudo-static random-access memory (SRAM, PSRAM)
  - NAND flash memory with 4-bit/8-bit BCH hardware ECC
- 8-,16-bit data bus width
- Independent chip-select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO

3.17 Octo-SPI memory interface (OCTOSPI1)

The OCTOSPI supports two protocols used by most external serial memories such as serial PSRAMs, serial NAND and serial NOR flash memories, HyperRAMs, and HyperFlash memories:

- Indirect mode: all the operations are performed using the OCTOSPI registers.
- Automatic status-polling mode: the external memory status register is periodically read, and an interrupt can be generated in case of flag setting.

- Memory-mapped mode: the external memory is memory mapped, and is seen by the system as if it was an internal memory supporting both read and write operations.

The OCTOSPI supports multiple protocols:

- XSPI protocol and its various flavors (such as XCELLA, OCTABUS, HyperBus™ as defined by memory providers)

3.18 On-the-fly decoder (OTFDEC1)

The OTFDEC is used to decrypt on-the-fly AHB traffic based on the read request address information. Four independent and non-overlapping encrypted regions can be defined in the OTFDEC.

The OTFDEC uses AES-128 in counter mode to achieve the lowest possible latency. Each time the content of an encrypted region is changed, the entire region must be re-encrypted with a different cryptographic context (key or initialization vector). This constraint makes the OTFDEC suitable to decrypt read-only data or code, stored in external NOR flash memory.

3.19 Analog-to-digital converters (ADC1, ADC2)

STM32MP21xC/F devices embed two analog-to-digital converters, which resolution can be configured to 12, 10, or 8 bits. Each ADC shares up to 20 channels, performing conversions in single-shot or scan mode. In scan mode, an automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by DMA, thus allows the automatic transfer of ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some, or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

In order to synchronize A/D conversion, the ADCs can be triggered by timers.

3.20 Digital temperature sensor (DTS)

The DTS is a high-precision low-power junction temperature sensor, based on a configurable controller plus one or multiple embedded temperature sensors. The sensor can operate in two distinct modes to provide temperature readings:

- First mode used to a provide calibrated accurate temperature
- Second mode that does not require any calibration

Main features:

- Two programmable (rise or fall) hardware alarms incorporating hysteresis
- Status registers recording the minimum and maximum data values received
- A power-up timer with IRQ to support manual operation
- A calibration sequence requiring no knowledge of die temperature.

3.21 V_{BAT} operation

The V_{SW} domain supplies the RTC, the TAMP, the LSI, the LSE, the backup registers, the retention RAM, and the backup SRAM.

In order to optimize the battery duration, this power domain is supplied by V_{DD} when available, or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} has dropped below the PDR level.

The voltage on VBAT pin can be provided by an external battery, by a supercapacitor, or directly by V_{DD}. In the latter case, V_{BAT} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

Note: None of these events (external interrupts, watchdog reset, TAMP event, or RTC alarm/events) can directly restore the V_{DD} supply, and force the device out of the V_{BAT} operation. Nevertheless, watchdog reset (taken as a tamper event), TAMP events, and RTC alarm/events can be used to generate a signal to an external circuitry (typically a PMIC) that can restore the V_{DD} supply.

3.22 Voltage reference buffer (VREFBUF)

STM32MP21xC/F devices embed a voltage reference buffer which can be used as voltage reference for ADC, and as voltage reference for external components through VREF+ pin.

An external voltage reference must be provided through the VREF+ pin when the internal voltage reference buffer is off.

3.23 Multifunction digital filter (MDF1)

The MDF is a high-performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators.

3.23.1 Features

- 4 serial digital inputs:
  - Configurable SPI interface to connect various digital sensors
  - Configurable Manchester coded interface support
  - Compatible with PDM interface to support digital microphones
- 2 common clocks input/output for ΣΔ modulator(s)
- Flexible matrix (BSMX) for connection between filters and digital inputs
- 2 inputs for connecting internal ADCs
- 4 flexible digital filter paths, including
  - A Configurable CIC filter:
    - Can be split into 2 CIC filters: high resolution filter, and out-off limit detector
    - Can be configured in $Sinc^4$ filter
    - Can be configured in $Sinc^5$ filter
    - Adjustable decimation ratio
  - A reshape filter to improve the out-off band rejection and in-band ripple
  - A high pass filter to cancel the DC offset
  - An offset error cancellation
  - Gain control
  - Saturation blocks
  - An out-off limit detector
- Short-circuit detector,
- Clock absence detector
- 16 or 24-bit signed output data resolution,
- Continuous or single conversion,
- Possibility to delay independently each bitstream
- Various trigger possibilities
- Break generation on out-of limit or short-circuit detector events
- Autonomous functionality in Stop modes
- DMA can be used to read the conversion data
- Interrupts services

Targeted applications:

- Audio: speech capture
- Motor control
- Metering

3.24 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8- to 14-bit parallel interface, to receive video data. The camera interface can support a resolution of 1 Mpixel at 15 fps.

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12-, or 14-bit

- 8-bit progressive video monochrome or RawBayer format, YC_bC_r 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Continuous mode or snapshot (a single frame) mode
- Capability to automatically crop the image

3.25 Parallel synchronous slave interface (PSSI)

The PSSI and the DCMI use the same circuitry. These two peripherals cannot be used at the same time: when using the PSSI, DCMI registers cannot be accessed, and vice versa.

The PSSI and the DCMI also share the same alternate functions and interrupt vector.

The PSSI is a generic synchronous 8/16-bit parallel data input/output slave interface. It enables the transmitter to send a data valid signal. This signal indicates when the data is valid, and the receiver to output a flow control signal that indicates when it is ready to sample the data.

Main features:

- Slave mode operation
- 8-bit or 16-bit parallel data input or output
- 8-word (32-byte) FIFO
- Data enable (PSSI_DE) alternate function input, and Ready (PSSI_RDY) alternate function output

3.26 Digital camera interface with pixel processing (DCMIPP)

- Parallel input interface:
  - Up to 16 bits at 120 MHz, up to 2 Mpixel sensors at 30 fps
  - Pixel format: RGB565, 888, YUV422, RawBayer/Mono 8/10/12/14
- When connected to CSI-2 input interface:
  - Up to 200 Mpixel/s, up to 5 Mpixel sensors at 30 fps, supports MIPI CSI-2 v1.3
  - Pixel format: all MIPI CSI-2 v1.3: RGB565, 888, YUV422, RawBayer
  - Features: interleaved packets, 4 virtual channels
- Flow selection and frame control
- Byte-to-pixel conversion
- Statistic removal
- Bad pixel removal (automatic detection and correction of bad pixels from sensor array)
- Decimation of one pixel every 1/2/4/8
- Integrated image processing used to connect low-cost camera module without any embedded ISP
  - Color conversion to adapt to the sensor and tune the Illumination
  - Contrast enhancement
  - RawBayer to RGB conversion (demosaicing)
  - Exposure control
  - Statistics extraction
- Decimation on pipe 0 (pipe dump)
- Multiple pipelines for parallel applications:
  - Pipe0 (for data dump), for a direct dump without processing
  - Pipe1 (for main use), with downsize, color conversion, YUV-planar
  - Pipe2 (for ancillary use), with downsize, color conversion, YUV-planar
- Downsize
  - Box-filtering, with any decimal ratio, up to 8x8, on pipe1 and pipe2
- Gamma conversion
- RGB to YUV color conversion
- Output pixel format:
  - Pipe0: any data as is, Y/Rb: 8/10/12/14 statistics, bitstreams
  - Pipe2: RGB888, RGB565, YUV422-1, Y8, ARGB and RGBA (co-planar only)
  - Pipe1: Pipe2 formats + YUV422-2, YUV420-2, YUV420-3 (multi-planar possible)

- AXI master

3.27 Camera serial interface (CSI)

The CSI provides an interface between the system and the PHY, allowing communication with a CSI-2 compliant camera.

- Compliant with MIPI Alliance standard v1.3
- Up to two data lanes, up to 2.5 Gbit/s per lane in high-speed (HS) mode and 10 Mbit/s in low-power (LP) mode
- Data transmission in HS and LP modes
- Escape mode (ESC), and ultra-low-power state mode (ULPS)
- CSI-2 virtual channel and data type filtering supporting interleaved data
  - Up to 4 virtual channels
  - Support data formats specified in the MIPI Alliance standard for CSI-2 v1.3 (18 data formats, plus the user defined one, up to 7 independent data types)
- Internal connection with the DCMIPP

3.28 LCD-TFT display controller (LTDC)

The LTDC handles display composition, with the following main features:

- 3 display layers with dedicated FIFO
- Input pixel flexible format
- Secure layer: protected access to buffer and configuration registers
- Horizontal and vertical mirror
- Color lookup-table, color keying, gamma, and dithering on output

LTDC parallel interface:

- Provides a 24-bit parallel digital RGB, and delivers all signals to interface directly to a broad range of LCD and TFT panels.
- Up to 150 Mpixel/s, which correspond up to FHD (1920 × 1080) at 60 fps resolution with HDMI blankings
- Output pixel formats: RGB888, RGB666, RGB565, YUV422-16 bits

3.29 True random number generator (RNG 1/2)

All devices embed two RNG that deliver 32-bit random numbers generated by an integrated analog circuit.

3.30 Hash processor (HASH 1/2)

The HASH is a fully compliant implementation of the secure hash algorithm (SHA-1, SHA-2 family, SHA-3 family), and the HMAC (keyed-hash message authentication code) algorithm. The HMAC is suitable for applications that require a message authentication.

The HASH computes FIPS (federal information processing Standards) approved digests of 160-, 224-, 256-, 384-, and 512-bit length, for messages of any length:

- less than 2^{64} bits (for SHA-1, SHA-224, and SHA-256)
- less than 2^{128} bits (for SHA-384, SHA-512)

3.31 Cryptographic processor (CRYP1/2)

The devices embed two cryptographic processor that can be used both to encrypt and decrypt data using the DES, triple-DES, or AES algorithms. The implementation if fully compliant with the following standards:

- DES and TDES are defined by FIPS (PUB 46-3, Oct 1999), and by the American National Standards Institute (ANSI X9.52)
- AES is defined by FIPS (FIPS PUB 197, Nov 2001)

Multiple key sizes and chaining modes are supported:

- DES/TDES chaining modes ECB and CBC, supporting standard 56-bit keys with 8-bit parity per key

- AES chaining modes ECB, CBC, CTR, GCM, GMAC, CCM for key sizes of 128, 192, or 256 bits

The CRYP in AES mode supports key sharing from SAES co-processor. It is a 32-bit AHB peripheral with DMA support for incoming and outgoing data.

The CRYP also includes input and output FIFOs (each 8 words deep) for better performance.

3.32 Secure AES (SAES)

The SAES encrypts or decrypts data, using an algorithm and implementation fully compliant with the AES standard. It implements embedded protection against differential power analysis (DPA) and related side-channel attacks.

The SAES supports CTR, GCM, GMAC, CCM, ECB, and CBC chaining modes for key sizes of 128 or 256 bits, as well as special modes such as hardware secret key encryption/decryption (wrapped-key mode) and key sharing with faster CRYP peripheral (shared-key mode).

The SAES can load directly two hardware master keys that are not directly accessible by any software. These keys can be used to encrypt random keys that are usable only on this device, and are not directly accessible by software.

The SAES supports DMA single transfers for incoming and outgoing data (two DMA channels required). It is connected by hardware to the RNG1 and to the CRYP1 .

The SAES is an AMBA AHB slave peripheral.

3.33 Public key accelerator (PKA)

The PKA is intended for the computation of cryptographic public key primitives, specifically those related to RSA, Diffie-Hellmann, or ECC (elliptic curve cryptography) over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.

For a given operation, all needed computations are performed within the accelerator: no further hardware/ software elaboration is needed to process inputs or outputs.

3.34 Boot and security and OTP control (BSEC)

The BSEC is used to control an OTP (one-time programmable) fuse box, used for embedded non-volatile storage for device configuration and security parameters.

Embedded non-volatile secrets are stored in the BSEC upper area that is only accessible while BSEC is operating in a closed state. In open state those non-volatile secrets are permanently hidden.

The BSEC use is reserved to trusted domain CPU, and boot CPU following a BSEC reset (cold/warm or hot).

3.35 Timers and watchdogs

The devices include two advanced-control timers, twelve general-purpose timers, two basic timers, five low-power timers, five watchdogs, two SysTick timers in Cortex-M33 , and four system timers in each Cortex-A35.

All timer counters can be frozen in debug mode.

The table below compares features of the different timers.

Table 7. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max(1) timer clock (MHz)
Advanced -control	TIM1, TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	6	4	150	150
General purpose	TIM2, TIM3, TIM4,	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No	150	150

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary output	Max interface clock (MHz)	Max(1) timer clock (MHz)
General purpose	TIM5								
	TIM10, TIM11, TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No	150	150
	TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No	150	150
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1	150	150
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1	150	150
Basic	TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	150	150
Low-power	LPTIM1, LPTIM2	16-bit	Up, Up/down	1, 2, 4, 8, 16, 32, 64, 128	Yes	2(2)	No	150	100
	LPTIM3, LPTIM4	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	Yes	2(2)	No	150(3)	100(4)
	LPTIM5	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	0	No	150(3)	100

1. *The maximum timer clock depends on RCC settings.*
2. *Only compare channel.*
3. *16 MHz bus clock when supplied by the backup regulator (LP-Stop1/2, LPLV-Stop1/2 or Standby).*
4. *32 kHz timer clock in autonomous mode (Stop1/2, LP-Stop1/2, LPLV-Stop1/2 or Standby).*

3.35.1 Advanced-control timers (TIM1/8)

The advanced-control timers can be seen as three-phase PWM generators multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge- or center-aligned modes)
- one-pulse mode output

If configured as standard 16-bit timers, the advanced-control timers have the same features as the general-purpose timers. If configured as 16-bit PWM generators, they have full modulation capability (0 to 100%).

The advanced-control timers can work together with general-purpose timers via the timer link feature for synchronization or event chaining.

3.35.2 General-purpose timers (TIM2/3/4/5/10/11/12/13/14/15/16/17)

There are twelve synchronizable general-purpose timers embedded in STM32MP21xC/F devices (see Section 3.35 for differences).

- **TIM2, TIM3, TIM4, TIM5**

These timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. They feature four independent channels for input capture/output compare, PWM, or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

These timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8, via the timer link feature for synchronization or event chaining.

Any of these general-purpose timers can be used to generate PWM outputs.

TIM2, TIM3, TIM4, TIM5 have independent DMA request generation. They can handle quadrature (incremental) encoder signals, and the digital outputs from one to four halleffect sensors.

- **TIM10, TIM11, TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM, or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

3.35.3 Basic timers (TIM6/TIM7)

These timers are used as a generic 16-bit time base, and support independent DMA request generation.

3.35.4 Low-power timer (LPTIM1/2/3/4/5)

These low-power timers have an independent clock and run in Stop mode if they are clocked by LSE, LSI, or an external clock. They can wake up the device from Stop mode.

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/one-shot mode
- Selectable software/hardware input trigger
- Selectable clock source:
  - Internal clock source: LSE, LSI, HSI (RCC flexgen output)
  - External clock source over LPTIM input (working even with no internal clock source running, used by the pulse counter application)
- Programmable digital glitch filter
- Encoder mode (LPTIM1/2)

3.35.5 Independent watchdog (IWDG1/2/3/4)

The IWDG is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC (LSI). As it operates independently from the main clock, the IWDG can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.35.6 System window watchdog (WWDG1)

The WWDG is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.35.7 SysTick timer

This timer is embedded in the Cortex-M33 (two instances, secure and non-Secure) . It is dedicated to real-time operating systems, but can also be used as standard downcounter.

- 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.35.8 Cortex-A35 generic timers (CNT)

The Cortex-A35 generic timers are fed by value from system timing generation (STGEN). The Cortex-A35 processor provides a set of four timers for each processor:

- Physical timer for use in secure and non-secure modes. The registers for the physical timer are banked to provide secure and non-secure copies.
- Virtual timer for use in non-secure mode
- Physical timer for use in hypervisor mode

These generic timers are not memory-mapped peripherals: they are accessible only by specific Cortex-A35 coprocessor instructions (cp15).

3.36 System timer generation (STGEN)

The STGEN generates a time-count value that provides a consistent view of time for all Cortex-A35 generic timers.

- 64-bit wide to avoid roll-over issues
- Starts from zero or a programmable value
- control APB interface (STGENC) that enables the timer to be saved and restored across power-down events
- Read-only APB interface (STGENR) that enables the timer value to be read by nonsecure software and debug tools
- Timer value incrementing that can be stopped during system debug

3.37 Real-time clock (RTC)

The RTC provides an automatic wake-up to manage all low-power modes. It is an independent BCD timer/counter that provides a time-of-day clock/calendar with programmable alarm interrupts.

The RTC includes also a periodic programmable wake-up flag with interrupt capability.

After backup domain reset, all RTC registers are protected against possible parasitic write accesses.

As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low-power mode, or under reset).

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), day (day of week), date (day of month), month, and year
- Daylight saving compensation programmable by software
- Programmable alarm with interrupt function. The alarm can be triggered by any combination of the calendar fields.
- Automatic wake-up unit that generates a periodic flag that triggers an automatic wake-up interrupt
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Accurate synchronization with an external clock using the subsecond shift feature
- Digital calibration circuit (periodic counter correction): 0.95 ppm accuracy, obtained in a calibration window of several seconds
- Timestamp function for event saving
- Maskable interrupts/events:
  - Alarm A
  - Alarm B
  - Wake-up interrupt
  - Timestamp
- TrustZone support:
  - RTC fully securable
  - Alarm A, alarm B, wake-up timer and timestamp individual secure or non-secure configuration

3.38 Tamper and backup registers (TAMP)

The 128 x 32-bit backup registers are retained in all low-power modes, and in V_{BAT} mode. They can be used to store sensitive data as their content is protected by a tamper detection circuit. 12 tamper pins (seven input and five outputs), and 16 internal tampers are available for anti-tamper detection.

The external tamper pins can be configured for edge detection, edge and level, level detection with filtering, or up to five active tamper which increases the security level by auto-checking that tamper pins are not externally opened or shorted.

- 128 backup registers (TAMP_BKPxR) implemented in the RTC domain that remains powered-on by V_{BAT} when the V_{DD} power is switched off
- 5 external active tampers detection events with configurable filter

- 7 external passive tampers detection events with configurable filter and internal pull-up
- 16 internal tamper events
- Any tamper detection can generate an RTC timestamp event.
- Any tamper detection erases backup registers.
- TrustZone support:
  - Tamper secure or non-secure configuration
  - Backup registers configuration in three configurable-size areas:
    - 1 read/write secure area
    - 1 write secure/read non-secure area
    - 1 read/write non-secure area
- Monotonic counter

3.39 Inter-integrated circuit interface (I2C1/2/3)

STM32MP21xC/F devices embed three I^2C interfaces that handle communications between the device and the serial I^2C bus. Each I^2C interface controls all I^2C bus-specific sequencing, protocol, arbitration, and timing.

The I^2C peripheral supports:

- I^2C-bus specification and user manual rev. 5 compatibility:
  - Controller and target modes, multi-controller capability
  - Standard-mode (Sm), with a bitrate up to 100 Kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 Kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit target addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power system management protocol (PMBus) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources that allows the I^2C communication speed to be independent from the PCLK reprogramming
- Wake-up from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

3.40 Improved inter-integrated circuit (I3C1/2/3)

STM32MP21xC/F devices embed three I3C interfaces, that handle communication between the device and others that are all connected on an I^3C bus, like sensors and host processors.

The I3C peripheral implements all required features of the MIPI I3C specification v1.1. It can control all I^3C bus-specific sequencing, protocol, arbitration and timing, and can be acting as controller, or as target.

The I3C peripheral, acting as controller, improves the I^2C interface features still preserving some backward compatibility: it allows an I^2C target to operate on an I^3C bus in legacy I^2C fast-mode (Fm) or legacy I^2C fast-mode plus (Fm+), provided that this latter does not perform clock stretching.

The I3C peripheral can be used with DMA in order to off-load the CPU.

- MIPI I3C specification v1.1 (see I3C section in the reference manual), as:
  - I3C primary controller
  - I3C secondary controller
  - I3C target
- Registers configuration from the host application via the APB slave port

- Queued transfers:
  - Transmit FIFO (TX-FIFO) for data bytes/words to be transmitted on I^3C bus
  - Receive FIFO (RX-FIFO) for received data bytes/words on I^3C bus
  - Control FIFO (C-FIFO) for control words to be sent on I^3C bus, when controller
  - Status FIFO (S-FIFO) for status words as received on I^3C bus, when controller
  - For each FIFO, optional DMA mode with a dedicated DMA channel
- Messages:
  - Legacy I2C read/write messages to legacy I2C targets in Fm/Fm+
  - I3C SDR read/write private messages
  - I3C SDR (write) broadcast CCC messages
  - I3C SDR read/write direct CCC messages
- Frame-level management, when controller:
  - Software-triggered or hardware-triggered transfer
  - Optional C-FIFO and TX-FIFO preload
  - Multiple messages encapsulation
  - Optional arbitrable header
- Programmable bus timing, when controller
  - SCL high and low period
  - SDA hold time
  - Bus free (minimum) time (between a stop and a start)
  - Bus available/idle condition time, maximum clock stall time
  - Minimum clock stall time during 9^{th} bit
- Target-initiated requests management:
  - In-band interrupts, with programmable IBI payload (up to 4 bytes)
  - Bus control request, with recovery flow support and hand-off delay
  - Hot-join mechanism
  - Pending read notification
- Bus error management
  - M0, M1, M2, and M3, when controller
  - S0, S1, S2, S3, S4, S5, and S6 when target
  - bus control switch error and recovery
  - target reset
- Separately programmed event/flag generation and management
  - Separated identification and clear control
  - Host application notification via event/flag polling, and/or via interrupt with a programmable enable
  - Error type identification
- Autonomous mode and transfers during Sleep and Stop modes via DMA
- Autonomous wake-up on
  - Target request acknowledge, when controller
  - Missed start detection, when target
  - Reset pattern detection, when target

3.41 Universal synchronous asynchronous receiver transmitter (USART1/2/3/6, UART4/5/7)

STM32MP21xC/F devices embed four USART and three UART (see Table 8. USART/UART features for feature summary).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN master/slave capability. They provide hardware management of CTS and RTS signals, and RS485 driver enable. They can communicate at speeds of up to 12.5 Mbit/s.

The USARTs embed a 64-byte transmit FIFO (TXFIFO) and a 64-byte receive FIFO (RXFIFO). The FIFO mode is enabled by software, and is disabled by default.

All USARTs provide smartcard mode (ISO 7816 compliant) and SPI-like communication capability. They have a clock domain independent from the CPU clock: this allows the USARTx to wake up the device from Stop mode using baud rates up to 200 Kbaud. Wake-up events from Stop mode are programmable and can be one of the following:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USARTs can be served by the DMA controller.

Table 8. USART/UART features

Modes/features (1)	USART1/2/3/6	UART4/5/7
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (master/slave)	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wake-up from low-power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver enable	X	X
Data length	7, 8, and 9 bits	

1. *X = supported.*

3.42 Low-power universal asynchronous receiver transmitter (LPUART1)

The devices embed one LPUART that supports asynchronous serial communication with minimum power consumption. The LPUART supports half-duplex single-wire communication. It allows multiprocessor communication.

Warning: *The STM32MP21x LPUART1 does not support hardware flow control for modem (no GPIO for RTS signal).*

The LPUART embeds a transmit FIFO (TXFIFO) and a receive FIFO (RXFIFO). The FIFO mode is enabled by software, and is disabled by default.

The LPUART has a clock domain independent from the CPU clock, and can wake up the system from Stop mode. The wake-up from Stop mode is programmable, and can be done on one of the following:

- A start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled

Even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low-energy consumption.

3.43 Serial peripheral interface (SPI1/2/3/4/5/6) inter-integrated sound interfaces (I2S1/2/3)

The devices feature up to six SPIs that allow communication at up to 50 Mbit/s in master and slave modes, in half-duplex, full-duplex, and simplex modes. The 3-bit prescaler gives eight master mode frequencies, and the frame is configurable from 4 to 16 bits.

All SPI interfaces support NSS pulse mode, TI mode, hardware CRC calculation, and eight 8-bit embedded Rx and Tx FIFOs with DMA capability.

The standard I^2S interfaces (multiplexed with SPI1, SPI2 and SPI3) can be operated in master or slave mode, in full-duplex and half-duplex communication modes. They can be configured to operate with a 16-/32-bit resolution as an input or output channel.

Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All I^2S interfaces support 16x 8bit embedded Rx and Tx FIFOs with DMA capability.

3.44 Serial audio interfaces (SAI1/2/3/4)

The devices embed four SAIs that are used to design many stereo or mono audio protocols such as I^2S, LSB or MSB-justified, PCM/DSP, TDM, or AC'97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio subblocks. Each block has it own clock generator and I/O line controller.

Audio sampling frequencies up to 192 kHz are supported.

Up to eight microphones can be supported thanks to an embedded PDM interface.

The SAI can work in master or slave configuration. The audio subblocks can be either receiver or transmitter, and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

3.45 SPDIF receiver interface (SPDIFRX)

The SPDIFRX is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby® or DTS® (up to 5.1).

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all necessary features to detect the symbol rate, and to decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal is available, the SPDIFRX re-samples the incoming signal, decodes the Manchester stream, and recognizes frames, sub-frames, and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate: this signal is used to compute the exact sample rate for clock drift algorithms.

3.46 Secure digital input/output MultiMediaCard interface (SDMMC1/2/3)

Three SDMMCs provide an interface between the AHB bus and SD memory cards, SDIO and e.MMC devices.

SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 5.1

Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit (HS200 speed limited by maximum allowed I/O speed, HS400 is not supported).

- Full compatibility with previous versions of MultiMediaCards (backward compatibility)

- Full compliance with SD memory card specifications version 6.0 (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI and UHS-II modes not supported)
- Full compliance with SDIO card specification version 4.0

Card support for two different databus modes: 1-bit (default) and 4-bit (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI and UHS-II modes not supported)

- Data transfer up to 208 Mbyte/s for the 8-bit mode (depending on the maximum allowed I/O speed)
- Data and command output enable signals to control external bidirectional drivers
- The SDMMC host interface embeds a dedicated DMA controller that allows high-speed transfers between the interface and the SRAM.
- IDMA linked list support

Each SDMMC is coupled with a delay block (DLYBSD) that supports an external data frequency above 100 MHz.

3.47 Controller area network (FDCAN1/2)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The CAN subsystem consists of two FDCANs, a shared message RAM, and a clock calibration unit.

All FDCANs are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B), and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TTCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10-Kbyte message RAM implements filters, receives FIFOs, receives buffers, transmits event FIFOs, transmits buffers (and triggers for TTCAN). This message RAM is shared between all FDCANs.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for FDCANs from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

3.48 Universal serial bus Hi-Speed host (USBH)

The devices embed one USB Hi-Speed host (up to 480 Mbit/s) with one physical port. USBH supports both low, full-speed (OHCI) as well as Hi-Speed (EHCI) operations. It integrates a physical interface (PHY) which can be used for either low-speed (1.2 Mbit/s), full-speed (12 Mbit/s), or Hi-Speed operation (480 Mbit/s).

The USBH is compliant with the USB 2.0 specification.

3.49 Universal serial bus 2.0 OTG high speed (OTG)

The devices embed one USB OTG high speed (up to 480 Mbit/s) device/host/OTG peripheral. OTG supports both full-speed and high-speed operations.

- Can be configured statically as a host or a device (dual role)
- Dynamic switching between the two roles is not supported: host negotiation protocol (HNP) and session request protocol (SRP) are not supported.
- Embedded PHY which supports high speed (HS), full speed (FS), and low speed (LS) modes (note: LS mode is not supported when configured as a device).
- Supports LPM (link power management)
- DMA engine with local 8-Kbyte buffer
- Supports battery charging v1.2, with the exception of the accessory charger adapter mode
- Supports suspend, sleep, resume, and remote wake-up operations
- Provides electrical parameter override bits for optimal interoperability
- No dedicated VBUS ball connected to the USB2 PHY
- No dedicated ID ball connected to the USB2 PHY

- The standards supported are:
  - Universal Serial Bus Specification, Revision 2.0, USB Implementers Forum, Inc., April 27, 2000
  - Engineering Change Notice: USB2.0 Link Power Management Addendum, July 16, 2007
  - UTMI+ Specification, Revision 1.0, Philips Semiconductor, February 25, 2004
  - Battery Charging Specification, Revision 1.2, December 7, 2010
  - AMBA specification (Revision 2.0, May 13, 1999)

3.50 Gigabit Ethernet MAC interface (ETH1/2)

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

The devices embed two fully independent instances of a 10/100/1000 Ethernet MAC controller, that enable transmission and reception of data over Ethernet, in compliance with IEEE 802.3-2008.

Each Ethernet MAC controller is connected to an external Ethernet PHY via a standard media independent interface.

Features provided by the Ethernet controller include:

- 10, 100, and 1000 Mbit/s data transfer rates
- Full-duplex and half-duplex operations
- Standard or Jumbo Ethernet packets
- Two independent Rx queues and two independent Tx queues, with each queue associated to a (subset of) PCP code(s)
- Configurable media-independent interface to external PHY:
  - RGMII
  - MII
  - RMII
  - MDIO master interface for external PHY device configuration
  - Internal or external reference clocks
- Low-power support:
  - Energy Efficient Ethernet (EEE) compliant with IEEE 802.3az-2010;
  - Detection of LAN wake-up frames and “Magic Packet” frames
- Timing and synchronization:
  - Compliance with IEEE 1588-2008 (PTP) and IEEE 802.1AS-Rev
  - Hardware “auxiliary timestamp trigger” for accurate sampling of the “PTP system clock”
  - Internal or external system time
- Time-sensitive networking:
  - “Forwarding and Queuing Enhancements for Time-Sensitive Streams” compliant with IEEE 802.1Qav
  - “Enhancements to Scheduled Traffic” compliant with IEEE 802.1Qbv, with a gate control list depth up to 128
  - “Frame Preemption” compliant with IEEE 802.1Qbu and IEEE 802.3br
- Preamble and start-of-frame data insertion (for Tx) and deletion (for Rx)
- Option for automatic CRC generation (for Tx), checking and stripping (for Rx)
- Source address field insertion or replacement in transmitted packets
- Filtering options:
  - Perfect match with a given SA/DA (up to 3 MAC addresses are supported)
  - 64-bit Hash filter match
  - Several multicast/broadcast rules supported
  - Based on IEEE 802.1q ‘VLAN tag’ field (perfect match, hash filtering)
  - Support for different ‘VLAN tag’ filtering for each Rx queue
  - Based on TCP/UDP/IP address (perfect match, inverse filtering)

- TCP/IP offloading:
  - Checksum calculation and insertion in the transmit path
  - Checksum error detection in the receive path.
  - TCP segmentation offload (automatic split of a large TCP packet into smaller Ethernet frames)

3.51 Debug infrastructure

The devices offer a comprehensive set of debug and trace features to support software development and system integration.

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Serial-wire trace port
- Trace port
- Arm CoreSight debug and trace components

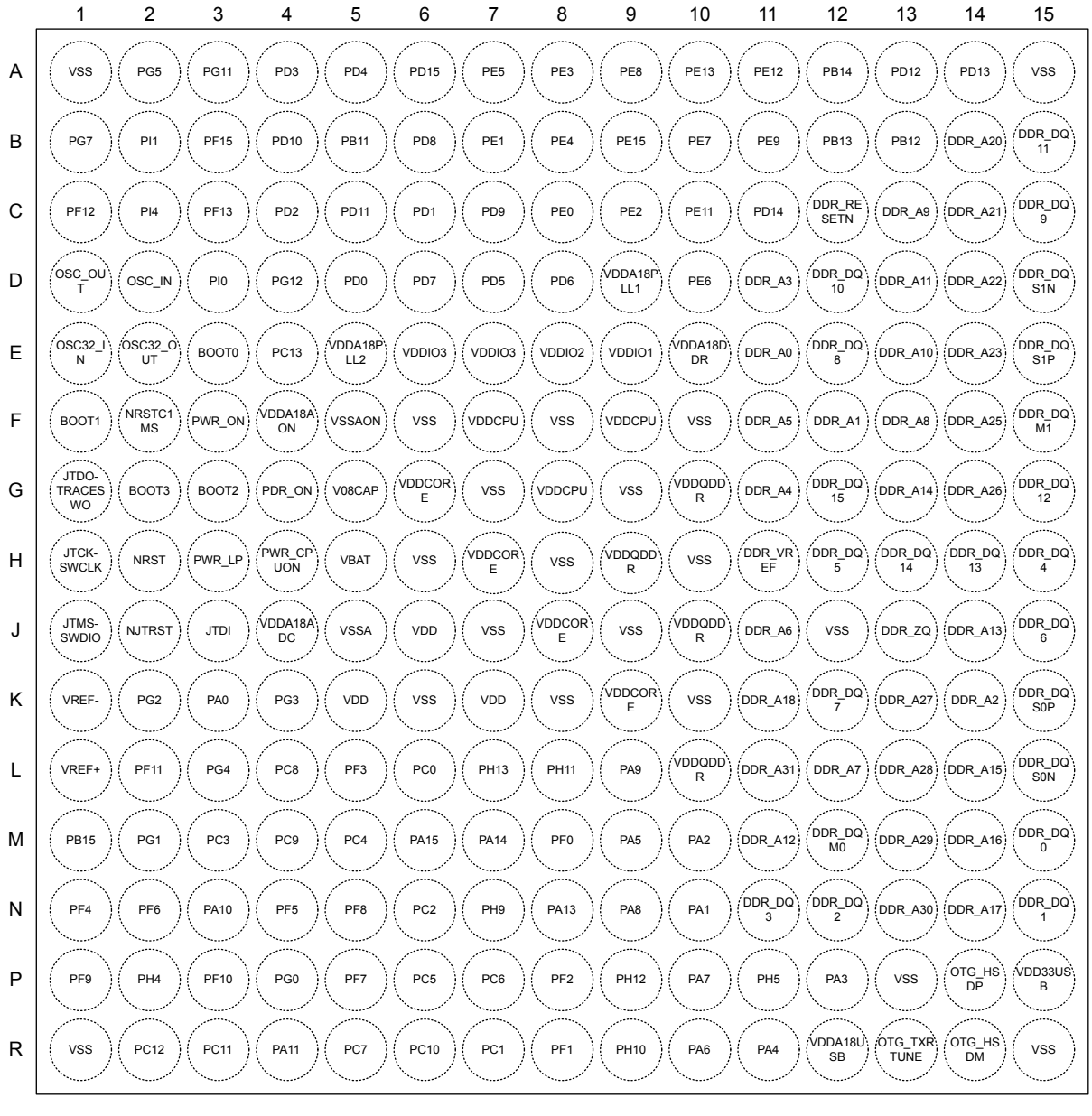
The debug can be controlled via a JTAG/serial-wire debug access port, using industry standard debugging tools.

A trace port allows data to be captured for logging and analysis.

4 Pinouts/ballouts, pin description, and alternate functions

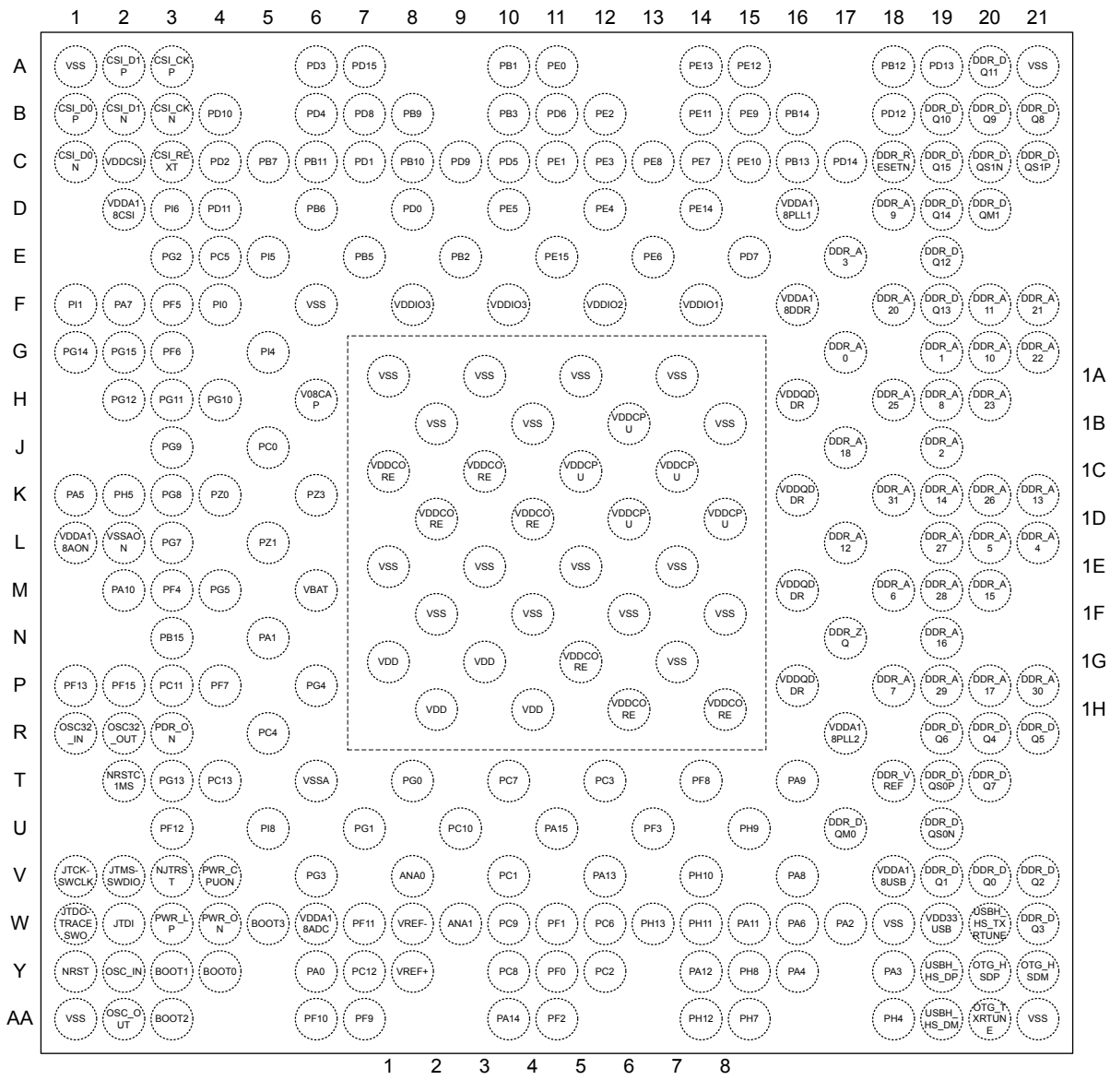
4.1 Ballout schematics

Figure 5. STM32MP21xC/F VFBGA225 ballout



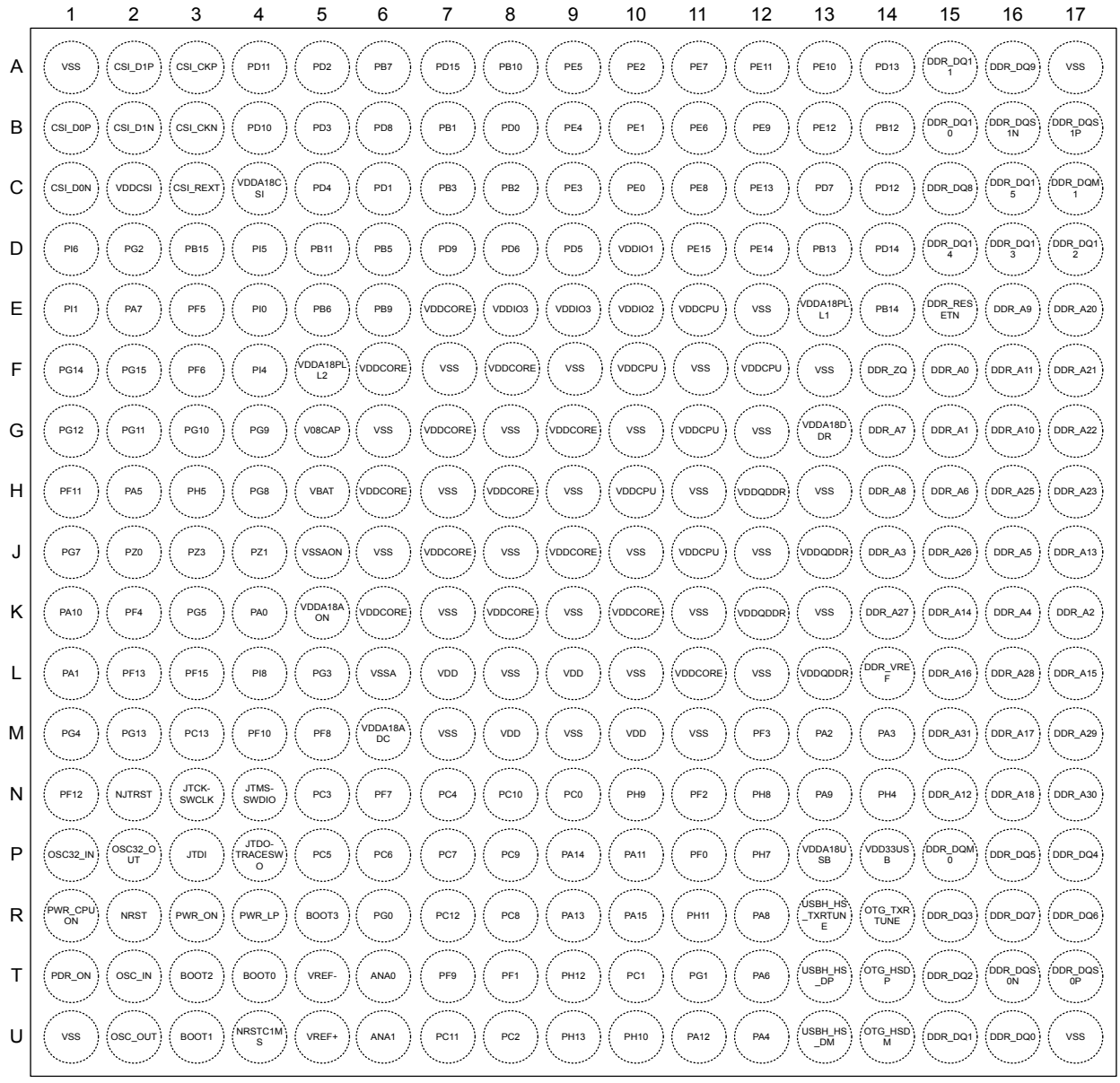
DT74176V2

Figure 6. STM32MP21xC/F VFBGA273 ballout



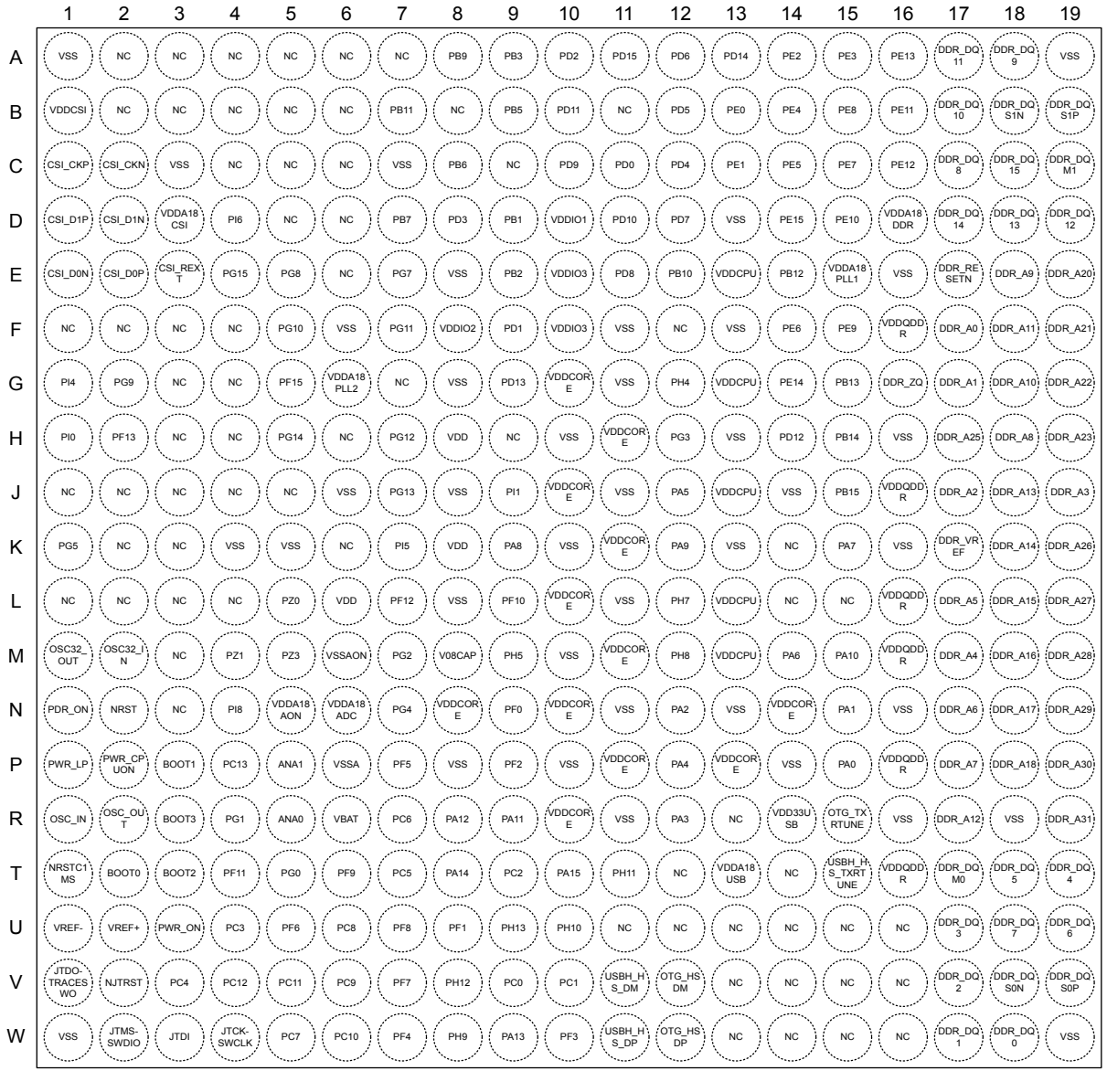
1. *The above figure shows the package top view.*

Figure 7. STM32MP21xC/F TFBGA289 ballout



1. *The above figure shows the package top view.*

Figure 8. STM32MP21xC/F VFBGA361 ballout



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1. *The above figure shows the package top view.*

Table 9. I/O power domains

Supply pin	Pin names(1)
VDD	JTCK-SWCLK, JTDI, JTDO-TRACESWO, JTMS-SWDIO, NJTRST, NRST, NRSTC1MS, PA0, PA1, PA2, PA3, PA4, PA5, PA6, PA7, PA8, PA9, PA10, PA11, PA12, PA13, PA14, PA15, PB1, PB2, PB3, PB5, PB6, PB7, PB9, PB10, PB11, PB12, PB13, PB14, PB15, PC0, PC1, PC2, PC6, PC7, PC8, PC9, PC10, PC11, PC12, PD12, PD13, PD14, PD15, PF0, PF1, PF2, PF3, PF4, PF5, PF8, PF9, PF10, PF11, PF12, PF13, PF15, PG0, PG2, PG4, PG5, PG7, PG8, PG9, PG10, PG11, PG12, PG13, PG14, PG15, PH4, PH5, PH7, PH8, PH9, PH10, PH11, PH12, PH13, PI0, PI1, PI4, PI5, PI6, PWR_CPU_ON, PWR_LP, PWR_ON,
VDDIO1(2)	PE0, PE1, PE2, PE3, PE4, PE5
VDDIO2(3)	PE6, PE7, PE8, PE9, PE10, PE11, PE12, PE13, PE14, PE15
VDDIO3(4)	PD0, PD1, PD2, PD3, PD4, PD5, PD6, PD7, PD8, PD9, PD10, PD11
VSW(5)	PC13, PI8, PZ0, PZ1, PZ3
VDD/VSW(5)(6)	PC3, PC4, PC5, PF6, PF7, PG1, PG3

1. *Does not include analog peripherals which have one or more dedicated supplies (for example PHYs).*
2. *Usually used for SD-Card using SDMMC1.*
3. *Usually used for e•MMC or SD-Card using SDMMC2. On VFBGA225 8×8 package, SDMMC2 is not a boot source.*
4. *Usually used for OCTOSPI1.*
5. *V_{SW} is supplied by V_{BAT} in absence of V_{DD}.*
6. *Pins with two supplies: V_{SW} supply for enabled TAMP_INx additional functions, V_{DD} supply for GPIO and other alternate functions.*

4.2 Ball description

Table 10. Legend/abbreviations used in the ballout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified, the ball function during and after reset is the same as the actual ball name	
	NC	Those balls are not connected inside the package
Pin type	S	Supply pin
	I	Input only pin
	O	Output only pin
	I/O	Input/output pin
	A	Analog or special level pin
I/O structure	TT(U/D/PD)	3.6 V capable I/O (with fixed pull-up/pull-down/programmable pull-down)(1)
	18T	1.8 V tolerant I/O
	DDR	1.35 V, 1.2 V, or 1.1 V I/O for DDR3L, DDR4 or LPDDR4 interface
	CSI	1.8 V I/O for CSI interface
	A	Analog signal
	RST	Reset pin with weak pull-up resistor
	Option for TT I/Os	
	_f(2)	I3C option
	_a(2)	Analog option (supplied by $V_{DDA18ADC}$ for the analog part of the I/O)
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

1. *3.6 V capable only if related I/O supply is 3.3 V typ. and related VDDIOxVRSEL = 0.*
2. *The related I/O structures in table below are TT_f, TT_a and TT_af.*

Note: Alternate functions listed in following tables may be absent in some devices or packages (see Section 2 for details).

Table 11. **STM32MP21xC/F ball definitions**

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
-	V8	T6	R5	ANA0	A	18T	-	-	ADC1_INP0, ADC1_INN1, ADC2_INP0, ADC2_INN1
-	W9	U6	P5	ANA1	A	18T	-	-	ADC1_INP1, ADC2_INP1
E3	Y4	T4	T2	BOOT0	I	TTPD	(1)	-	-
F1	Y3	U3	P3	BOOT1	I	TTPD	(1)	-	-
G3	AA3	T3	T3	BOOT2	I	TTPD	(1)	-	-
G2	W5	R5	R3	BOOT3	I	TTPD	(1)	-	-
-	B3	B3	C2	CSI_CKN	CSI	18T	-	-	-
-	A3	A3	C1	CSI_CKP	CSI	18T	-	-	-
-	C1	C1	E1	CSI_D0N	CSI	18T	-	-	-
-	B1	B1	E2	CSI_D0P	CSI	18T	-	-	-
-	B2	B2	D2	CSI_D1N	CSI	18T	-	-	-
-	A2	A2	D1	CSI_D1P	CSI	18T	-	-	-
-	C3	C3	E3	CSI_REXT	A	-	-	-	-
E11	G17	F15	F17	DDR_A0	O	DDR	-	-	-
F12	G19	G15	G17	DDR_A1	O	DDR	-	-	-
K14	J19	K17	J17	DDR_A2	O	DDR	-	-	-
D11	E17	J14	J19	DDR_A3	O	DDR	-	-	-
G11	L21	K16	M17	DDR_A4	O	DDR	-	-	-
F11	L20	J16	L17	DDR_A5	O	DDR	-	-	-
J11	M18	H15	N17	DDR_A6	O	DDR	-	-	-
L12	P18	G14	P17	DDR_A7	O	DDR	-	-	-
F13	H19	H14	H18	DDR_A8	O	DDR	-	-	-
C13	D18	E16	E18	DDR_A9	O	DDR	-	-	-
E13	G20	G16	G18	DDR_A10	O	DDR	-	-	-
D13	F20	F16	F18	DDR_A11	O	DDR	-	-	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
M11	L17	N15	R17	DDR_A12	O	DDR	-	-	-
J14	K21	J17	J18	DDR_A13	O	DDR	-	-	-
G13	K19	K15	K18	DDR_A14	O	DDR	-	-	-
L14	M20	L17	L18	DDR_A15	O	DDR	-	-	-
M14	N19	L15	M18	DDR_A16	O	DDR	-	-	-
N14	P20	M16	N18	DDR_A17	O	DDR	-	-	-
K11	J17	N16	P18	DDR_A18	O	DDR	-	-	-
B14	F18	E17	E19	DDR_A20	O	DDR	-	-	-
C14	F21	F17	F19	DDR_A21	O	DDR	-	-	-
D14	G21	G17	G19	DDR_A22	O	DDR	-	-	-
E14	H20	H17	H19	DDR_A23	O	DDR	-	-	-
F14	H18	H16	H17	DDR_A25	O	DDR	-	-	-
G14	K20	J15	K19	DDR_A26	O	DDR	-	-	-
K13	L19	K14	L19	DDR_A27	O	DDR	-	-	-
L13	M19	L16	M19	DDR_A28	O	DDR	-	-	-
M13	P19	M17	N19	DDR_A29	O	DDR	-	-	-
N13	P21	N17	P19	DDR_A30	O	DDR	-	-	-
L11	K18	M15	R19	DDR_A31	O	DDR	-	-	-
M12	U17	P15	T17	DDR_DQM0	O	DDR	-	-	-
F15	D20	C17	C19	DDR_DQM1	O	DDR	-	-	-
L15	U19	T16	V18	DDR_DQS0N	I/O	DDR	-	-	-
D15	C20	B16	B18	DDR_DQS1N	I/O	DDR	-	-	-
K15	T19	T17	V19	DDR_DQS0P	I/O	DDR	-	-	-
E15	C21	B17	B19	DDR_DQS1P	I/O	DDR	-	-	-
N12	V21	T15	V17	DDR_DQ2	I/O	DDR	-	-	-
N11	W21	R15	U17	DDR_DQ3	I/O	DDR	-	-	-
N15	V19	U15	W17	DDR_DQ1	I/O	DDR	-	-	-
M15	V20	U16	W18	DDR_DQ0	I/O	DDR	-	-	-
K12	T20	R16	U18	DDR_DQ7	I/O	DDR	-	-	-
J15	R19	R17	U19	DDR_DQ6	I/O	DDR	-	-	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
H15	R20	P17	T19	DDR_DQ4	I/O	DDR	-	-	-
H12	R21	P16	T18	DDR_DQ5	I/O	DDR	-	-	-
G15	E19	D17	D19	DDR_DQ12	I/O	DDR	-	-	-
G12	C19	C16	C18	DDR_DQ15	I/O	DDR	-	-	-
H13	D19	D15	D17	DDR_DQ14	I/O	DDR	-	-	-
H14	F19	D16	D18	DDR_DQ13	I/O	DDR	-	-	-
C15	B20	A16	A18	DDR_DQ9	I/O	DDR	-	-	-
E12	B21	C15	C17	DDR_DQ8	I/O	DDR	-	-	-
B15	A20	A15	A17	DDR_DQ11	I/O	DDR	-	-	-
D12	B19	B15	B17	DDR_DQ10	I/O	DDR	-	-	-
H11	T18	L14	K17	DDR_VREF	A	-	-	-	-
C12	C18	E15	E17	DDR_RESETN	O	DDR	-	-	-
J13	N17	F14	G16	DDR_ZQ	A	-	-	-	-
H1	V1	N3	W4	JTCK-SWCLK	I	TTD	(1)	-	-
J3	W2	P3	W3	JTDI	I	TTU	(1)	-	-
G1	W1	P4	V1	JTDO-TRACESWO	O	TTU	(1)	-	-
J1	V2	N4	W2	JTMS-SWDIO	I/O	TTU	(1)	-	-
J2	V3	N2	V2	NJTRST	I	TTU	(1)	-	-
H2	Y1	R2	N2	NRST	I/O	RST	(1)	-	-
F2	T2	U4	T1	NRSTC1MS	O	TT	(2)	-	-
K3	Y6	K4	P15	PA0	I/O	TT_a	(1)	LPTIM1_CH2, SPI5_RDY, SAI2_MCLK_B, UART5_TX(boot), USART3_TX, TIM3_ETR, TIM5_CH2, ETH2_MII_RXD2, FMC_NL, DCMI_D9/PSSI_D9/DCMIPP_D9, EVENTOUT	WKUP1
N10	N5	L1	N15	PA1	I/O	TT_af	(1)	SPI6_MISO, SAI3_SD_A, USART1_RTS/ USART1_DE, USART6_CK, TIM4_CH2, I2C1_SDA, LCD_R3, DCMI_D5/PSSI_D5/ DCMIPP_D5, EVENTOUT	-
M10	W17	M13	N12	PA2	I/O	TT_af	(1)	LPTIM2_IN1, USART1_RX, I3C1_SDA, I2C1_SDA, LCD_B0, DCMI_D3/PSSI_D3/ DCMIPP_D3, EVENTOUT	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
P12	Y18	M14	R12	PA3	I/O	TT_af	(1)	LPTIM2_ETR, USART1_TX, I3C1_SCL, I2C3_SMBA, I2C1_SCL, LCD_B1, DCMI_D2/ PSSI_D2/DCMIPP_D2, EVENTOUT	-
R11	Y16	U12	P12	PA4	I/O	TT_a	(1)	USART2_TX(boot), FDCAN2_TX, TIM2_CH1, LCD_R1, ETH1_PTP_AUX_TS, EVENTOUT	-
M9	K1	H2	J12	PA5	I/O	TT	(1)	SPI4_MOSI, SAI2_MCLK_B, SAI2_SD_B, USART2_RTS/USART2_DE, FDCAN2_RX, TIM2_CH4, LCD_G0, DCMI_D13/PSSI_D13/ DCMIPP_D13, EVENTOUT	-
R10	W16	T12	M14	PA6	I/O	TT	(1)	SPI4_SCK, SAI2_FS_B, USART2_CK, TIM13_CH1, TIM2_ETR, LCD_G4, FMC_NE1, DCMI_D12/PSSI_D12/DCMIPP_D12, EVENTOUT	-
P10	F2	E2	K15	PA7	I/O	TT	(1)	CK_IN, SPI6_RDY, MDF1_CCK0, USART1_CTS/USART1_NSS, TIM4_ETR, I2C2_SMBA, LCD_B5, I2C3_SMBA, I2C1_SMBA, DCMI_D6/PSSI_D6/DCMIPP_D6, EVENTOUT	-
N9	V16	R12	K9	PA8	I/O	TT_f	(1)	LPTIM2_CH2, SAI1_FS_B, USART1_CK, USART2_RX(boot), I2C2_SCL, LCD_B2, DCMI_D4/PSSI_D4/DCMIPP_D4, EVENTOUT	-
L9	T16	N13	K12	PA9	I/O	TT	(1)	SPI4_NSS, SAI2_SCK_B, USART2_CTS/ USART2_NSS, LPTIM5_ETR, TIM2_CH3, ETH1_MDC, LCD_G7, PSSI_D14/ DCMIPP_D14, EVENTOUT	-
N3	M2	K1	M15	PA10	I/O	TT	(1)	SPI4_MISO, SAI2_SD_B, USART2_RX, LPTIM5_IN1, TIM2_CH2, ETH1_MDIO, LCD_R6, PSSI_D15/DCMIPP_D15, EVENTOUT	-
R4	W15	P10	R9	PA11	I/O	TT	(1)	SPI6_SCK, LPTIM2_CH1, SAI4_SD_B, ETH1_MII_RX_DV/ETH1_RGMII_RX_CTL/ ETH1_RMII_CRS_DV, EVENTOUT	-
-	Y14	U11	R8	PA12	I/O	TT_f	(1)	SPI6_MOSI, SAI3_FS_A, TIM4_CH1, I2C1_SCL, ETH1_PHY_INTN, EVENTOUT	-
N8	V12	R9	W9	PA13	I/O	TT	(1)	SPI6_RDY, I2S3_MCK, LPTIM2_ETR, MDF1_CKI3, USART2_CTS/USART2_NSS, I2C3_SMBA, ETH1_MII_TX_EN/ ETH1_RGMII_TX_CTL/ETH1_RMII_TX_EN, EVENTOUT	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
M7	AA10	P9	T8	PA14	I/O	TT	(1)	SPI6_NSS, LPTIM2_CH2, SAI4_FS_B, MDF1_CCK1, ETH1_MII_RX_CLK/ ETH1_RGMII_RX_CLK/ETH1_RMII_REF_CLK, EVENTOUT	-
M6	U11	R10	T10	PA15	I/O	TT_f	(1)	SPI3_MISO/I2S3_SDI, USART2_RX, I2C3_SDA, ETH1_MII_TXD0/ ETH1_RGMII_TXD0/ETH1_RMII_TXD0, EVENTOUT	-
-	A10	B7	D9	PB1	I/O	TT	(1)	SPI3_NSS/I2S3_WS, TIM16_CH1N, FMC_NCE4, EVENTOUT	-
-	E9	C8	E9	PB2	I/O	TT	(1)	SPI2_MOSI/I2S2_SDO, MDF1_CKI3, TIM17_BKIN, TIM16_BKIN, FMC_AD12/ FMC_D12(boot), EVENTOUT	-
-	B10	C7	A9	PB3	I/O	TT	(1)	SPI2_NSS/I2S2_WS, MDF1_SDI3, FMC_NCE3, EVENTOUT	-
-	E7	D6	B9	PB5	I/O	TT_f	(1)	I2S2_MCK, UART4_RTS/UART4_DE, SAI4_SD_B, I2C2_SCL, FMC_AD8/ FMC_D8(boot), I3C2_SCL, SDMMC3_D123DIR, EVENTOUT	-
-	D6	E5	C8	PB6	I/O	TT	(1)	SPI2_MISO/I2S2_SDI, UART4_RX, SAI4_SCK_B, FMC_AD9/FMC_D9(boot), SDMMC3_D0DIR, EVENTOUT	-
-	C5	A6	D7	PB7	I/O	TT	(1)	SPI3_SCK/I2S3_CK, UART4_TX, SAI4_MCLK_B, TIM12_CH1, FMC_AD10/ FMC_D10(boot), SDMMC3_CDIR, EVENTOUT	-
-	B8	E6	A8	PB9	I/O	TT	(1)	SPI3_RDY, USART1_RTS/USART1_DE, FDCAN1_TX, TIM10_CH1, FMC_AD13/ FMC_D13(boot), EVENTOUT	-
-	C8	A8	E12	PB10	I/O	TT	(1)	SPI3_MISO/I2S3_SDI, USART1_RX, TIM17_CH1N, FMC_AD15/FMC_D15(boot), EVENTOUT	-
-	C6	D5	B7	PB11	I/O	TT	(3)	I2S3_MCK, USART1_CTS/USART1_NSS, FDCAN1_RX, TIM12_CH2, FMC_AD14/ FMC_D14(boot), OCTOSPI1_NCS2, EVENTOUT	-
B5	-	-	-	PB11	I/O	TT	(3)	I2S3_MCK, USART1_CTS/USART1_NSS, FDCAN1_RX, TIM12_CH2, FMC_AD14/ FMC_D14, OCTOSPI1_NCS2, EVENTOUT	-
B13	A18	B14	E14	PB12	I/O	TT_a	(1)	TIM13_CH1, SDMMC3_D2, FMC_NWAIT, DCMI_D12/PSSI_D12/DCMIPP_D12, EVENTOUT	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
B12	C16	D13	G15	PB13	I/O	TT_a	(1)	SPI2_MOSI/I2S2_SDO, SAI1_SD_B, SDMMC3_CK, FMC_AD5/FMC_D5(boot), EVENTOUT	-
A12	B16	E14	H15	PB14	I/O	TT	(1)	SPI2_SCK/I2S2_CK, TIM4_CH2, SDMMC3_D0, FMC_AD7/FMC_D7(boot), EVENTOUT	-
M1	N3	D3	J15	PB15	I/O	TT_a	(1)	LPTIM1_IN2, SPI5_SCK, SAI2_SD_B, UART5_RX(boot), TIM3_CH2, TIM5_CH1, ETH1_PPS_OUT, FMC_A18, LCD_R4, DCMI_D8/PSSI_D8/DCMIPP_D8, EVENTOUT	ADC1_INP15, ADC2_INP5
L6	J5	N9	V9	PC0	I/O	TT	(1)	LPTIM1_CH1, SPI6_SCK, SAI3_MCLK_B, USART6_TX, DCMI_D0/PSSI_D0/ DCMIPP_D0, ETH2_MII_RX_CLK/ ETH2_RMII_REF_CLK, ETH1_MII_TX_CLK, ETH1_RGMII_GTX_CLK, LCD_G7, EVENTOUT	-
R7	V10	T10	V10	PC1	I/O	TT_f	(1)	SPI3_MOSI/I2S3_SDO, USART2_TX, I2C3_SCL, ETH1_MII_TXD1/ ETH1_RGMII_TXD1/ETH1_RMII_TXD1, EVENTOUT	-
N6	Y12	U8	T9	PC2	I/O	TT	(1)	SPI6_MOSI, LPTIM2_IN1, SAI4_MCLK_B, MDF1_SDI3, USART2_RTS/USART2_DE, ETH1_MII_RXD1/ETH1_RGMII_RXD1/ ETH1_RMII_RXD1, EVENTOUT	-
M3	T12	N5	U4	PC3	I/O	TT_a	(4)	LPTIM1_IN2, SPI3_NSS/I2S3_WS, SPI6_RDY, USART6_RTS/USART6_DE, FDCAN2_TX, ETH2_MII_RX_DV/ETH2_RGMII_RX_CTL/ ETH2_RMII_CRS_DV, ETH1_MII_RX_ER, LCD_G6, DCMI_D3/PSSI_D3/DCMIPP_D3, EVENTOUT	ADC1_INP12, ADC1_INN10, ADC2_INP12, ADC2_INN10, TAMP_IN3
M5	R5	N7	V3	PC4	I/O	TT	(4)	SPI6_MISO, SAI3_FS_B, ETH2_MII_TX_EN/ ETH2_RGMII_TX_CTL/ETH2_RMII_TX_EN, ETH1_RGMII_CLK125, LCD_R0, EVENTOUT	TAMP_IN1
P6	E4	P5	T7	PC5	I/O	TT_af	(4)	SPDIFRX1_IN1, MDF1_SDI1, TIM8_CH1N, I2C1_SDA, ETH2_MDIO, ETH1_MII_COL, FMC_A25, ETH1_PPS_OUT, LCD_DE, EVENTOUT	ADC1_INP10, ADC2_INP10, TAMP_IN6
P7	W12	P6	R7	PC6	I/O	TT_af	(1)	RTC_REFIN, SPDIFRX1_IN0, MDF1_CKI1, TIM8_CH1, I2C1_SCL, ETH2_MDC, ETH1_MII_CRS, FMC_A24, ETH1_PHY_INTN, LCD_CLK, EVENTOUT	ADC1_INP9, ADC1_INN5

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
R5	T10	P7	W5	PC7	I/O	TT_a	(1)	SPI6_MOSI, SAI3_SD_B, TIM8_CH2N, ETH2_MII_TXD0/ETH2_RGMII_TXD0/ ETH2_RMII_TXD0, ETH1_MII_TXD2, LCD_B4, DCMI_D1/PSSI_D1/DCMIPP_D1, EVENTOUT	ADC2_INP9, ADC2_INN5
L4	Y10	R8	U6	PC8	I/O	TT_a	(1)	LPTIM1_ETR, SPI6_NSS, SAI3_SCK_B, USART6_CTS/USART6_NSS, TIM8_CH2, ETH2_MII_TXD1/ETH2_RGMII_TXD1/ ETH2_RMII_TXD1, ETH1_MII_TXD3, LCD_B3, DCMI_D2/PSSI_D2/DCMIPP_D2, EVENTOUT	-
M4	W10	P8	V6	PC9	I/O	TT_a	(1)	MCO1, SPI3_MISO/I2S3_SDI, SAI2_SCK_A, TIM13_CH1, TIM8_CH4N, USBH_HS_OVRCUR, ETH2_MII_TXD2/ ETH2_RGMII_TXD2, FMC_A22, LCD_G2, DCMI_D7/PSSI_D7/DCMIPP_D7, EVENTOUT	ADC1_INP8, ADC1_INN4
R6	U9	N8	W6	PC10	I/O	TT_a	(1)	SPI3_MOSI/I2S3_SDO, LPTIM4_ETR, TIM8_CH4, USBH_HS_VBUSEN, ETH2_MII_TXD3/ETH2_RGMII_TXD3, DCMI_D0/PSSI_D0/DCMIPP_D0, FMC_A23, LCD_G3, DCMI_D6/PSSI_D6/DCMIPP_D6, EVENTOUT	ADC1_INP5
R3	P3	U7	V5	PC11	I/O	TT_a	(1)	LPTIM1_CH1, SPI5_NSS, SAI2_MCLK_A, UART5_RTS/UART5_DE, USART3_RTS/ USART3_DE, TIM3_CH1, TIM5_ETR, DCMI_HSYNC/PSSI_DE/DCMIPP_HSYNC, ETH2_MII_RXD3/ETH2_RGMII_RXD3, FMC_NBL1, LCD_R2, DCMI_D10/PSSI_D10/ DCMIPP_D10, EVENTOUT	ADC1_INP7, ADC1_INN3, ADC2_INP7, ADC2_INN3
R2	Y7	R7	V4	PC12	I/O	TT_af	(1)	LPTIM1_CH2, I3C3_SCL, I3C2_SCL, MDF1_CKI2, TIM8_CH3, I2C3_SCL, ETH2_MII_RXD1/ETH2_RGMII_RXD1/ ETH2_RMII_RXD1, ETH1_MII_RXD3, LCD_G1, DCMI_D5/PSSI_D5/DCMIPP_D5, EVENTOUT	ADC1_INP17
E4	T4	M3	P4	PC13	I/O	TT	(5)	EVENTOUT	RTC_OUT1/ RTC_LSCO/ RTC_TS, TAMP_OUT1
E1	R1	P1	M2	OSC32_IN	I	18T	(6)	-	OSC32_IN
E2	R2	P2	M1	OSC32_OUT	O	18T	(7)	-	OSC32_OUT
G4	R3	T1	N1	PDR_ON	I	TT	(8)	-	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
D5	D8	B8	C11	PD0	I/O	TT	(9)	TRACECLK, HDP0, SAI1_D2, SAI4_FS_A, UART7_RX, TIM15_CH2, SDVSEL1, OCTOSPI1_CLK(boot), DCMI_PIXCLK/ PSSI_PDCK/DCMIPP_PIXCLK, EVENTOUT	-
C6	C7	C6	F9	PD1	I/O	TT	(9)	HDP1, SPI1_MISO/I2S1_SDI, SAI1_CK2, SAI4_SD_A, UART7_RTS/UART7_DE, TIM15_CH1, TIM1_BKIN, OCTOSPI1_NCLK(boot), OCTOSPI1_NCS2, DCMI_HSYNC/PSSI_DE/DCMIPP_HSYNC, EVENTOUT	-
C4	C4	A5	A10	PD2	I/O	TT	(9)	HDP2, SPI1_NSS/I2S1_WS, SAI1_CK1, SAI4_SCK_A, UART7_CTS, TIM15_BKIN, TIM1_ETR, OCTOSPI1_DQS(boot), OCTOSPI1_NCS2, DCMI_VSYNC/PSSI_RDY/ DCMIPP_VSYNC, EVENTOUT	-
A4	A6	B5	D8	PD3	I/O	TT	(9)	SAI1_MCLK_A, SPI2_SCK/I2S2_CK, SAI1_D1, SAI4_MCLK_A, UART7_TX, TIM15_CH1N, TIM1_BKIN2, SDVSEL2, OCTOSPI1_NCS1(boot), PSSI_D15/ DCMIPP_D15, EVENTOUT	-
A5	B6	C5	C12	PD4	I/O	TT	(9)	TRACED0, SPI4_MISO, HDP3, SAI1_D3, SAI1_SD_B, TIM1_CH4N, TIM4_CH1, OCTOSPI1_IO0(boot), PSSI_D14/ DCMIPP_D14, EVENTOUT	-
D7	C10	D9	B12	PD5	I/O	TT	(9)	TRACED1, SPI4_NSS, HDP4, SAI1_D4, SAI1_FS_B, TIM1_CH3N, TIM4_CH2, OCTOSPI1_IO1(boot), DCMI_D13/PSSI_D13/ DCMIPP_D13, EVENTOUT	-
D8	B11	D8	A12	PD6	I/O	TT	(9)	TRACED2, SPI4_MOSI, HDP5, SAI1_SCK_B, MDF1_SDI2, TIM1_CH2N, TIM4_CH3, OCTOSPI1_IO2(boot), DCMI_D12/PSSI_D12/ DCMIPP_D12, EVENTOUT	-
D6	E15	C13	D12	PD7	I/O	TT	(9)	TRACED3, SPI4_SCK, SPI1_RDY, SAI1_MCLK_B, MDF1_CKI2, TIM1_CH1N, TIM4_CH4, OCTOSPI1_IO3(boot), DCMI_D11/ PSSI_D11/DCMIPP_D11, EVENTOUT	-
B6	B7	B6	E11	PD8	I/O	TT	(9)	TRACED4, SPI4_RDY, I2S1_MCK, SAI1_FS_A, UART4_CTS, MDF1_SDI1, TIM1_CH4, TIM4_ETR, OCTOSPI1_IO4(boot), SDMMC1_D7, SDMMC1_D123DIR, DCMI_D10/PSSI_D10/DCMIPP_D10, EVENTOUT	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
C7	C9	D7	C10	PD9	I/O	TT	(9)	TRACED5, HDP6, SPI1_MOSI/I2S1_SDO, SAI1_SD_A, UART4_RTS/UART4_DE, MDF1_CKI1, TIM1_CH3, OCTOSPI1_IO5(boot), SDMMC1_D6, SDMMC1_D0DIR, DCMI_D9/PSSI_D9/ DCMIPP_D9, EVENTOUT	-
B4	B4	B4	D11	PD10	I/O	TT_f	(9)	TRACED6, HDP7, SAI1_SCK_A, UART4_RX, MDF1_SDI0, I2C1_SDA, TIM1_CH2, TIM14_CH1, OCTOSPI1_IO6(boot), SDMMC1_D5, SDMMC1_CDIR, DCMI_D8/ PSSI_D8/DCMIPP_D8, EVENTOUT	-
C5	D4	A4	B10	PD11	I/O	TT_f	(9)	TRACED7, SPI1_SCK/I2S1_CK, SAI1_MCLK_A, UART4_TX, MDF1_CKI0, I2C1_SCL, TIM1_CH1, SDVSEL1, OCTOSPI1_IO7(boot), SDMMC1_D4, SDMMC1_CKIN, DCMI_D7/PSSI_D7/ DCMIPP_D7, EVENTOUT	-
A13	B18	C14	H14	PD12	I/O	TT_a	(1)	SPI2_MISO/I2S2_SDI, SPDIFRX1_IN2, TIM4_ETR, SDMMC3_CMD, FMC_AD6/ FMC_D6(boot), EVENTOUT	-
-	A19	A14	G9	PD13	I/O	TT_a	(1)	SPI2_NSS/I2S2_WS, TIM4_CH4, SDMMC3_D1, FMC_AD11/FMC_D11(boot), FMC_NWE, EVENTOUT	-
A14	-	-	-	PD13	I/O	TT_a	(1)	SPI2_NSS/I2S2_WS, TIM4_CH4, SDMMC3_D1, FMC_AD11/FMC_D11, FMC_NWE(boot), EVENTOUT	-
C11	C17	D14	A13	PD14	I/O	TT_af	(1)	I2S2_MCK, I2S1_MCK, FDCAN1_RX, TIM11_CH1, FMC_AD4/FMC_D4(boot), SDMMC3_D3, DCMI_D1/PSSI_D1/ DCMIPP_D1, EVENTOUT	-
A6	A7	A7	A11	PD15	I/O	TT_af	(1)	SPI1_RDY, I2C2_SDA, FDCAN1_TX, TIM1_BKIN2, TIM5_ETR, FMC_AD3/ FMC_D3(boot), SDMMC3_CKIN, DCMI_D0/ PSSI_D0/DCMIPP_D0, EVENTOUT	-
C8	A11	C10	B13	PE0	I/O	TT	(10)	TRACED2, LPTIM2_CH1, SPI1_SCK/I2S1_CK, SPI3_RDY, USART3_CK, SDMMC1_D2, EVENTOUT	-
B7	C11	B10	C13	PE1	I/O	TT	(10)	TRACED3, LPTIM2_CH2, I2S1_MCK, I2S3_MCK, USART3_RX, SDMMC1_D3, EVENTOUT	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
C9	B12	A10	A14	PE2	I/O	TT	(10)	LPTIM2_ETR, SPI1_MISO/I2S1_SDI, SPI3_MOSI/I2S3_SDO, SAI1_SCK_B, TIM10_CH1, SDMMC1_CMD(boot), EVENTOUT	-
A8	C12	C9	A15	PE3	I/O	TT	(10)	TRACECLK, SPI1_RDY, SPI3_SCK/I2S3_CK, SAI1_MCLK_B, USART3_TX, TIM11_CH1, SDMMC1_CK(boot), EVENTOUT	-
B8	D12	B9	B14	PE4	I/O	TT	(10)	TRACED0, LPTIM2_IN1, SPI1_MOSI/ I2S1_SDO, SPI3_MISO/I2S3_SDI, SAI1_SD_B, USART3_CTS/USART3_NSS, FDCAN1_TX, SDMMC1_D0(boot), EVENTOUT	-
A7	D10	A9	C14	PE5	I/O	TT	(10)	TRACED1, LPTIM2_IN2, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SAI1_FS_B, USART3_RTS/USART3_DE, FDCAN1_RX, SDMMC1_D1, EVENTOUT	-
D10	E13	B11	F14	PE6	I/O	TT	(11)	SPI4_RDY, SPDIFRX1_IN2, USART1_TX, TIM1_ETR, FMC_AD1/FMC_D1(boot), SDMMC2_D6, SDMMC2_D0DIR, SDMMC2_CK, EVENTOUT	-
B10	C14	A11	C15	PE7	I/O	TT	(11)	SAI4_D4, SPDIFRX1_IN3, USART1_RX, TIM1_CH4N, TIM14_CH1, FMC_AD2/ FMC_D2(boot), SDMMC2_D7, SDMMC2_D123DIR, EVENTOUT	-
A9	C13	C11	B15	PE8	I/O	TT	(11)	SPI4_MOSI, SAI4_CK1, SAI4_MCLK_A, MDF1_CKI0, TIM1_CH1, FMC_A17/ FMC_ALE(boot), SDMMC2_D2, EVENTOUT	-
B11	B15	B12	F15	PE9	I/O	TT	(11)	SPI4_MISO, SAI4_D2, SAI4_FS_A, USART1_CK, TIM1_CH4, FMC_AD0/ FMC_D0(boot), SDMMC2_D5, SDMMC2_CDIR, EVENTOUT	-
-	C15	A13	D15	PE10	I/O	TT	(11)	SPI4_SCK, SAI4_D1, SAI4_SD_A, USART1_CTS/USART1_NSS, TIM1_CH3, FMC_NE3, FMC_NCE2, SDMMC2_D4, SDMMC2_CKIN, EVENTOUT	-
C10	B14	A12	B16	PE11	I/O	TT	(11)	SAI4_D3, SAI1_FS_A, TIM15_CH2, TIM1_CH3N, FMC_A16/FMC_CLE(boot), SDMMC2_D1, EVENTOUT	-
A11	A15	B13	C16	PE12	I/O	TT	(11)	SPI4_NSS, SAI4_CK2, SAI4_SCK_A, MDF1_SDI0, USART1_RTS/USART1_DE, TIM1_CH2, FMC_NE2, FMC_NCE1(boot), SDMMC2_D3, EVENTOUT	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
-	A14	C12	A16	PE13	I/O	TT	(11)	SAI1_SD_A, TIM15_CH1, TIM1_CH2N, FMC_RNB(boot), SDMMC2_D0(boot), EVENTOUT	-
A10	-	-	-	PE13	I/O	TT	(11)	SAI1_SD_A, TIM15_CH1, TIM1_CH2N, FMC_RNB(boot), SDMMC2_D0, EVENTOUT	-
-	D14	D12	G14	PE14	I/O	TT	(11)	SAI1_MCLK_A, TIM15_BKIN, TIM1_BKIN, FMC_NWE(boot), SDMMC2_CK(boot), EVENTOUT	-
-	E11	D11	D14	PE15	I/O	TT	(11)	SAI1_SCK_A, TIM15_CH1N, TIM1_CH1N, FMC_NOE(boot), SDMMC2_CMD(boot), EVENTOUT	-
B9	-	-	-	PE15	I/O	TT	(11)	SAI1_SCK_A, TIM15_CH1N, TIM1_CH1N, FMC_NOE(boot), SDMMC2_CMD, EVENTOUT	-
M8	Y11	P11	N9	PF0	I/O	TT_af	(1)	SPI3_SCK/I2S3_CK, FDCAN2_RX, TIM12_CH2, I2C2_SDA, ETH1_MDC, ETH2_MII_CRS, I3C2_SDA, EVENTOUT	ADC1_INP11, ADC2_INP11
R8	W11	T8	U8	PF1	I/O	TT	(1)	SPI6_MISO, LPTIM2_IN2, SAI4_SCK_B, USART2_CK, ETH1_MII_RXD0/ ETH1_RGMII_RXD0/ETH1_RMII_RXD0, EVENTOUT	-
P8	AA11	N11	P9	PF2	I/O	TT_af	(1)	SPI3_RDY, I2C1_SMBA, TIM12_CH1, I2C2_SCL, ETH1_MDIO, ETH2_MII_COL, FMC_NE4, I3C2_SCL, EVENTOUT	ADC1_INP13, ADC1_INN11, ADC2_INP13, ADC2_INN11
L5	U13	M12	W10	PF3	I/O	TT_a	(1)	SAI2_SCK_B, MDF1_CCK0, TIM3_CH4, TIM8_BKIN2, ETH1_CLK, ETH2_PPS_OUT, FMC_A20, LCD_R6, DCMI_HSYNC/PSSI_DE/ DCMIPP_HSYNC, EVENTOUT	ADC1_INP16, ADC1_INN15
N1	M3	K2	W7	PF4	I/O	TT	(1)	RTC_OUT2, SPI6_NSS, SAI3_SCK_A, USART6_RX(boot), TIM4_CH4, ETH1_MDC, ETH2_CLK, ETH2_PPS_OUT, ETH1_PPS_OUT, LCD_B7, EVENTOUT	-
N4	F3	E3	P7	PF5	I/O	TT	(1)	SPI6_SCK, SAI3_MCLK_A, USART6_TX(boot), TIM4_CH3, ETH1_MDIO, ETH1_CLK, ETH2_PHY_INTN, ETH1_PHY_INTN, LCD_B6, EVENTOUT	-
N2	G3	F3	U5	PF6	I/O	TT	(4)	RTC_OUT2, SAI3_MCLK_B, USART6_CK, TIM12_CH1, I2C3_SMBA, ETH2_MII_RX_CLK/ ETH2_RGMII_RX_CLK/ETH2_RMII_REF_CLK, LCD_B0, EVENTOUT	TAMP_IN5

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
P5	P4	N6	V7	PF7	I/O	TT	(4)	SPDIFRX1_IN1, SPI6_SCK, SAI3_SD_A, TIM2_ETR, ETH2_RGMII_GTX_CLK, ETH2_MII_TX_CLK, LCD_R1, EVENTOUT	TAMP_IN2
N5	T14	M5	U7	PF8	I/O	TT	(1)	RTC_REFIN, SAI3_SCK_B, USART3_RX, TIM12_CH2, ETH1_CLK, ETH2_RGMII_CLK125, ETH2_MII_RX_ER, ETH2_MII_RX_DV/ETH2_RMII_CRS_DV, LCD_G0, EVENTOUT	-
P1	AA7	T7	T6	PF9	I/O	TT	(1)	SAI3_SD_B, SAI2_SD_A, TIM2_CH2, ETH2_MII_RXD2/ETH2_RGMII_RXD2, ETH2_MDIO, EVENTOUT	-
P3	AA6	M4	L9	PF10	I/O	TT_a	(1)	MCO2, SPI3_RDY, SAI2_MCLK_A, TIM2_CH3, ETH2_MII_TXD2, EVENTOUT	ADC2_INP2
L2	W7	H1	T4	PF11	I/O	TT_a	(1)	MCO1, SPDIFRX1_IN0, SPI6_RDY, SAI2_SCK_A, TIM2_CH4, ETH2_MII_TXD3, EVENTOUT	ADC2_INP6, ADC2_INN2
C1	U3	N1	L7	PF12	I/O	TT	(1)	TRACECLK, SPI5_MISO, SPI1_MISO/ I2S1_SDI, TIM5_CH1, LCD_CLK, DCMI_D0/ PSSI_D0/DCMIPP_D0, EVENTOUT	-
C3	P1	L2	H2	PF13	I/O	TT	(1)	TRACED0, HDP0, CK_IN, USART6_TX, SPI2_NSS/I2S2_WS, USART3_CTS/ USART3_NSS, TIM3_CH3, LCD_R2, EVENTOUT	-
B3	P2	L3	G5	PF15	I/O	TT	(1)	TRACED2, HDP2, SPI2_RDY, USART6_CTS/ USART6_NSS, SPI2_SCK/I2S2_CK, USART3_CK, TIM2_CH2, TIM3_ETR, LCD_R4, EVENTOUT	-
P4	T8	R6	T5	PG0	I/O	TT_af	(1)	LPTIM1_IN1, I3C3_SDA, I3C2_SDA, MDF1_SDI2, TIM8_CH3N, I2C3_SDA, ETH2_MII_RXD0/ETH2_RGMII_RXD0/ ETH2_RMII_RXD0, ETH1_MII_RXD2, LCD_G5, DCMI_D4/PSSI_D4/DCMIPP_D4, EVENTOUT	ADC1_INP18, ADC1_INN17
M2	U7	T11	R4	PG1	I/O	TT_af	(4)	LPTIM1_IN1, I2S3_MCK, I3C3_SCL, SAI2_SD_A, UART5_CTS, USART3_CTS/ USART3_NSS, TIM5_CH4, I2C3_SCL, ETH2_MII_RX_ER, ETH2_MII_RXD3, FMC_NBL0, LCD_VSYNC, DCMI_D11/ PSSI_D11/DCMIPP_D11, EVENTOUT	WKUP3, ADC1_INP6, ADC1_INN2, TAMP_IN4

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
K2	E3	D2	M7	PG2	I/O	TT_af	(1)	RTC_REFIN, I2S3_MCK, I3C3_SDA, SAI2_FS_A, USART3_CK, TIM5_CH3, I2C3_SDA, ETH2_MII_TX_CLK, ETH2_RGMII_CLK125, FMC_CLK, LCD_HSYNC, EVENTOUT	WKUP5, ADC1_INP2
K4	V6	L5	H12	PG3	I/O	TT_a	(4)	LPTIM1_ETR, SPI5_MOSI, SAI2_FS_B, TIM3_CH3, TIM8_ETR, ETH2_CLK, ETH2_PHY_INTN, FMC_A19, LCD_R5, DCMI_PIXCLK/PSSI_PDCK/DCMIPP_PIXCLK, EVENTOUT	WKUP6, ADC1_INP3, ADC2_INP3, TAMP_IN7
L3	P6	M1	N7	PG4	I/O	TT_a	(1)	SPI5_MISO, SAI3_FS_B, LPTIM4_IN1, TIM8_BKIN, ETH2_PPS_OUT, ETH2_MDC, FMC_A21, LCD_R7, DCMI_VSYNC/ PSSI_RDY/DCMIPP_VSYNC, EVENTOUT	PVD_IN, ADC1_INP4
A2	M4	K3	K1	PG5	I/O	TT_f	(1)	TRACED3, HDP3, USART6_RTS/USART6_DE, TIM2_CH3, LCD_R5, DCMI_PIXCLK/ PSSI_PDCK/DCMIPP_PIXCLK, EVENTOUT	-
B1	L3	J1	E7	PG7	I/O	TT	(1)	TRACED5, HDP5, SPI5_NSS, SPI1_NSS/ I2S1_WS, TIM5_ETR, LCD_R7, DCMI_VSYNC/PSSI_RDY/DCMIPP_VSYNC, EVENTOUT	-
-	K3	H4	E5	PG8	I/O	TT	(1)	TRACED6, HDP6, SPI5_RDY, SPI1_RDY, USART6_CK, UART5_RTS/UART5_DE, TIM5_CH3, LCD_G2, DCMI_D2/PSSI_D2/ DCMIPP_D2, EVENTOUT	-
-	J3	G4	G2	PG9	I/O	TT	(1)	TRACED7, UART5_TX, TIM5_CH4, LCD_G3, DCMI_D3/PSSI_D3/DCMIPP_D3, EVENTOUT	-
-	H4	G3	F5	PG10	I/O	TT	(1)	TRACED8, HDP0, UART5_RX, TIM8_CH4N, LCD_G4, DCMI_D4/PSSI_D4/DCMIPP_D4, EVENTOUT	-
A3	H3	G2	F7	PG11	I/O	TT	(1)	TRACED9, HDP1, FDCAN1_TX, TIM8_CH4, LCD_G5, DCMI_D5/PSSI_D5/DCMIPP_D5, EVENTOUT	-
D4	H2	G1	H7	PG12	I/O	TT	(1)	TRACED10, HDP2, FDCAN1_RX, TIM8_CH1N, LCD_G6, DCMI_D6/PSSI_D6/DCMIPP_D6, EVENTOUT	-
-	T3	M2	J7	PG13	I/O	TT_f	(1)	TRACED11, HDP3, TIM8_CH2N, I2C1_SCL, I3C1_SCL, LCD_G7, DCMI_D7/PSSI_D7/ DCMIPP_D7, EVENTOUT	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
-	G1	F1	H5	PG14	I/O	TT	(1)	TRACED12, HDP4, USART1_TX, TIM8_BKIN2, LCD_B1, DCMI_D9/PSSI_D9/DCMIPP_D9, EVENTOUT	-
-	G2	F2	E4	PG15	I/O	TT	(1)	TRACED13, HDP5, LPTIM1_CH2, USART1_RX, TIM8_ETR, LCD_B2, DCMI_D10/PSSI_D10/DCMIPP_D10, EVENTOUT	-
D2	Y2	T2	R1	OSC_IN	I	18T	(12)	-	OSC_IN
D1	AA2	U2	R2	OSC_OUT	O	18T	(13)	-	OSC_OUT
P2	AA18	N14	G12	PH4	I/O	TT	(1)	DBTRGI, DBTRGO, UART7_TX, TIM17_BKIN, TIM5_CH2, LCD_R0, USBH_HS_OVRCUR, ETH1_PTP_AUX_TS, EVENTOUT	BOOTFAILN
P11	K2	H3	M9	PH5	I/O	TT	(1)	DBTRGO, DBTRGI, SAI2_FS_A, TIM2_CH1, UART7_RX, LCD_G1, USBH_HS_VBUSEN, ETH2_PTP_AUX_TS, EVENTOUT	WKUP2
-	AA15	P12	L12	PH7	I/O	TT_f	(1)	SPI1_MOSI/I2S1_SDO, UART4_TX, UART7_RTS/UART7_DE, TIM17_CH1, TIM5_CH4, EVENTOUT	-
-	Y15	N12	M12	PH8	I/O	TT	(1)	SPI1_MISO/I2S1_SDI, SPDIFRX1_IN3, UART4_RX, UART7_CTS, TIM5_CH1, I2C3_SMBA, I2C2_SMBA, EVENTOUT	-
N7	U15	N10	W8	PH9	I/O	TT_a	(1)	SPI6_NSS, SAI3_MCLK_A, USART6_RX, TIM15_CH1N, ETH1_RGMII_CLK125, ETH1_MII_RX_ER, EVENTOUT	ADC2_INP4
R9	V14	U10	U10	PH10	I/O	TT_a	(1)	SPI1_SCK/I2S1_CK, SPI6_MOSI, SAI3_SCK_A, TIM15_CH1, ETH2_MDC, ETH1_MII_TXD2/ETH1_RGMII_TXD2, EVENTOUT	ADC2_INP8, ADC2_INN4
L8	W14	R11	T11	PH11	I/O	TT_a	(1)	SPI6_MISO, SAI3_FS_A, TIM15_CH2, ETH2_MDIO, ETH1_MII_TXD3/ ETH1_RGMII_TXD3, EVENTOUT	-
P9	AA14	T9	V8	PH12	I/O	TT	(1)	SPI3_NSS/I2S3_WS, SPI6_MISO, TIM10_CH1, ETH1_MII_RXD2/ETH1_RGMII_RXD2, EVENTOUT	-
L7	W13	U9	U9	PH13	I/O	TT	(1)	SPI3_SCK/I2S3_CK, SPI6_MOSI, TIM15_BKIN, TIM11_CH1, ETH1_MII_RXD3/ ETH1_RGMII_RXD3, EVENTOUT	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
D3	F4	E4	H1	PI0	I/O	TT	(1)	TRACED14, HDP6, LPTIM1_IN1, SAI4_MCLK_B, USART1_CK, TIM8_BKIN, LCD_B3, DCMI_D11/PSSI_D11/DCMIPP_D11, EVENTOUT	-
B2	F1	E1	J9	PI1	I/O	TT_f	(1)	TRACED15, HDP7, TIM8_CH3N, I2C1_SDA, I3C1_SDA, LCD_B4, DCMI_D8/PSSI_D8/ DCMIPP_D8, EVENTOUT	-
C2	G5	F4	G1	PI4	I/O	TT	(1)	LPTIM1_CH1, SAI4_FS_B, TIM8_CH3, LCD_B7, PSSI_D15/DCMIPP_D15, EVENTOUT	-
-	E5	D4	K7	PI5	I/O	TT	(1)	SPI5_MOSI, SPI1_MOSI/I2S1_SDO, UART5_CTS, TIM5_CH2, LCD_DE, DCMI_D1/ PSSI_D1/DCMIPP_D1, EVENTOUT	-
-	D3	D1	D4	PI6	I/O	TT	(1)	MCO1, USART3_TX, TIM2_ETR, TIM3_CH1, LCD_VSYNC, EVENTOUT	WKUP4
-	U5	L4	N4	PI8	I/O	TT	(5)	EVENTOUT	RTC_OUT2/ RTC_LSCO, TAMP_IN1/ TAMP_OUT2
H4	V4	R1	P2	PWR_CPU_ON	O	TT	(1)	-	-
H3	W3	R4	P1	PWR_LP	O	TT	(1)	-	-
F3	W4	R3	U3	PWR_ON	O	TT	(1)	-	-
-	K4	J2	L5	PZ0	I/O	TT_f	(5)	LPTIM3_IN1, SPI6_MOSI, TIM8_CH1, LPUART1_TX, LPTIM5_OUT, I2C3_SDA, LPTIM3_CH2, I3C3_SDA, EVENTOUT	TAMP_OUT3
-	L5	J4	M4	PZ1	I/O	TT_f	(5)	LPTIM3_CH1, SPI6_MISO, TIM8_CH2, LPUART1_RX, LPTIM5_ETR, I2C3_SCL, I2C3_SMBA, I3C3_SCL, EVENTOUT	TAMP_OUT5
-	K6	J3	M5	PZ3	I/O	TT_f	(5)	DBTRGI, DBTRGO, LPTIM3_ETR, SPI6_NSS, MDF1_SDI3, LPUART1_CTS, LPTIM4_IN1, I2C3_SDA, LPTIM4_CH2, I3C3_SDA, EVENTOUT	TAMP_OUT4
-	AA19	U13	V11	USBH_HS_DM	A	18T_u	-	-	-
R14	Y21	U14	V12	OTG_HSDM	A	18T_u	-	-	-
-	Y19	T13	W11	USBH_HS_DP	A	18T_u	-	-	-
P14	Y20	T14	W12	OTG_HSDP	A	18T_u	-	-	-
-	W20	R13	T15	USBH_HS_TXRTUNE	A	-	-	-	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
R13	AA20	R14	R15	OTG_TXRTUNE	A	-	-	-	-
K1	W8	T5	U1	VREF-	A	-	-	-	-
L1	Y8	U5	U2	VREF+	A	-	-	-	-
H5	M6	H5	R6	VBAT	S	-	-	-	-
K5	1G1	L7	H8	VDD	S	-	-	-	-
J6	1H2	M8	K8	VDD	S	-	-	-	-
K7	1G3	L9	L6	VDD	S	-	-	-	-
-	1H4	M10	-	VDD	S	-	-	-	-
J4	W6	M6	N6	VDDA18ADC	S	-	-	-	-
-	D2	C4	D3	VDDA18CSI	S	-	-	-	-
E10	F16	G13	D16	VDDA18DDR	S	-	-	-	-
D9	D16	E13	E15	VDDA18PLL1	S	-	-	-	-
E5	R17	F5	G6	VDDA18PLL2	S	-	-	-	-
R12	V18	P13	T13	VDDA18USB	S	-	-	-	-
G6	1C1	F6	G10	VDDCORE	S	-	-	-	-
H7	1D2	H6	H11	VDDCORE	S	-	-	-	-
J8	1C3	K6	J10	VDDCORE	S	-	-	-	-
K9	1D4	E7	K11	VDDCORE	S	-	-	-	-
-	1G5	G7	L10	VDDCORE	S	-	-	-	-
-	1H6	J7	M11	VDDCORE	S	-	-	-	-
-	1H8	F8	N8	VDDCORE	S	-	-	-	-
-	-	H8	N10	VDDCORE	S	-	-	-	-
-	-	K8	N14	VDDCORE	S	-	-	-	-
-	-	G9	P11	VDDCORE	S	-	-	-	-
-	-	J9	P13	VDDCORE	S	-	-	-	-
-	-	K10	R10	VDDCORE	S	-	-	-	-
-	-	L11	-	VDDCORE	S	-	-	-	-
F7	1C5	F10	E13	VDDCPU	S	-	-	-	-
G8	1B6	H10	G13	VDDCPU	S	-	-	-	-
F9	1D6	E11	J13	VDDCPU	S	-	-	-	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
-	1C7	G11	L13	VDDCPU	S	-	-	-	-
-	1D8	J11	M13	VDDCPU	S	-	-	-	-
-	-	F12	-	VDDCPU	S	-	-	-	-
H9	H16	H12	F16	VDDQDDR	S	-	-	-	-
G10	K16	K12	J16	VDDQDDR	S	-	-	-	-
J10	M16	J13	L16	VDDQDDR	S	-	-	-	-
L10	P16	L13	M16	VDDQDDR	S	-	-	-	-
-	-	-	P16	VDDQDDR	S	-	-	-	-
-	-	-	T16	VDDQDDR	S	-	-	-	-
E8	F12	E10	F8	VDDIO2	S	-	-	-	-
E6	F8	E8	E10	VDDIO3	S	-	-	-	-
E7	F10	E9	F10	VDDIO3	S	-	-	-	-
E9	F14	D10	D10	VDDIO1	S	-	-	-	-
-	C2	C2	B1	VDDCSI	S	-	-	-	-
F4	L1	K5	N5	VDDA18AON	S	-	-	-	-
P15	W19	P14	R14	VDD33USB	S	-	-	-	-
A1	A1	A1	A1	VSS	S	-	-	-	-
R1	A21	U1	A19	VSS	S	-	-	-	-
F6	F6	G6	C3	VSS	S	-	-	-	-
H6	1A1	J6	C7	VSS	S	-	-	-	-
K6	1E1	F7	D13	VSS	S	-	-	-	-
G7	1B2	H7	E8	VSS	S	-	-	-	-
J7	1F2	K7	E16	VSS	S	-	-	-	-
F8	1A3	M7	F6	VSS	S	-	-	-	-
H8	1E3	G8	F11	VSS	S	-	-	-	-
K8	1B4	J8	F13	VSS	S	-	-	-	-
G9	1F4	L8	G8	VSS	S	-	-	-	-
J9	1A5	F9	G11	VSS	S	-	-	-	-
F10	1E5	H9	H10	VSS	S	-	-	-	-
H10	1F6	K9	H13	VSS	S	-	-	-	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
K10	1A7	M9	H16	VSS	S	-	-	-	-
J12	1E7	G10	J6	VSS	S	-	-	-	-
A15	1G7	J10	J8	VSS	S	-	-	-	-
R15	1B8	L10	J11	VSS	S	-	-	-	-
P13	1F8	F11	J14	VSS	S	-	-	-	-
-	W18	H11	K4	VSS	S	-	-	-	-
-	AA1	K11	K5	VSS	S	-	-	-	-
-	AA21	M11	K10	VSS	S	-	-	-	-
-	-	E12	K13	VSS	S	-	-	-	-
-	-	G12	K16	VSS	S	-	-	-	-
-	-	J12	L8	VSS	S	-	-	-	-
-	-	L12	L11	VSS	S	-	-	-	-
-	-	F13	M10	VSS	S	-	-	-	-
-	-	H13	N11	VSS	S	-	-	-	-
-	-	K13	N13	VSS	S	-	-	-	-
-	-	A17	N16	VSS	S	-	-	-	-
-	-	U17	P8	VSS	S	-	-	-	-
-	-	-	P10	VSS	S	-	-	-	-
-	-	-	P14	VSS	S	-	-	-	-
-	-	-	R11	VSS	S	-	-	-	-
-	-	-	R16	VSS	S	-	-	-	-
-	-	-	R18	VSS	S	-	-	-	-
-	-	-	W1	VSS	S	-	-	-	-
-	-	-	W19	VSS	S	-	-	-	-
J5	T6	L6	P6	VSSA	S	-	-	-	-
-	-	-	U14	NC	-	-	-	-	-
-	-	-	V13	NC	-	-	-	-	-
-	-	-	T12	NC	-	-	-	-	-
-	-	-	V14	NC	-	-	-	-	-
-	-	-	R13	NC	-	-	-	-	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
-	-	-	V15	NC	-	-	-	-	-
-	-	-	W15	NC	-	-	-	-	-
-	-	-	U16	NC	-	-	-	-	-
-	-	-	V16	NC	-	-	-	-	-
-	-	-	W16	NC	-	-	-	-	-
-	-	-	T14	NC	-	-	-	-	-
-	-	-	U15	NC	-	-	-	-	-
-	-	-	U12	NC	-	-	-	-	-
-	-	-	U13	NC	-	-	-	-	-
-	-	-	U11	NC	-	-	-	-	-
-	-	-	A7	NC	-	-	-	-	-
-	-	-	C9	NC	-	-	-	-	-
-	-	-	B8	NC	-	-	-	-	-
-	-	-	G7	NC	-	-	-	-	-
-	-	-	K2	NC	-	-	-	-	-
-	-	-	L14	NC	-	-	-	-	-
-	-	-	K14	NC	-	-	-	-	-
-	-	-	L15	NC	-	-	-	-	-
-	-	-	J5	NC	-	-	-	-	-
-	-	-	H9	NC	-	-	-	-	-
-	-	-	D5	NC	-	-	-	-	-
-	-	-	K6	NC	-	-	-	-	-
-	-	-	B11	NC	-	-	-	-	-
-	-	-	F12	NC	-	-	-	-	-
-	-	-	M3	NC	-	-	-	-	-
-	-	-	L4	NC	-	-	-	-	-
-	-	-	N3	NC	-	-	-	-	-
-	-	-	K3	NC	-	-	-	-	-
-	-	-	L1	NC	-	-	-	-	-
-	-	-	L3	NC	-	-	-	-	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
-	-	-	L2	NC	-	-	-	-	-
-	-	-	J1	NC	-	-	-	-	-
-	-	-	J2	NC	-	-	-	-	-
-	-	-	J3	NC	-	-	-	-	-
-	-	-	J4	NC	-	-	-	-	-
-	-	-	H3	NC	-	-	-	-	-
-	-	-	H4	NC	-	-	-	-	-
-	-	-	G3	NC	-	-	-	-	-
-	-	-	G4	NC	-	-	-	-	-
-	-	-	F1	NC	-	-	-	-	-
-	-	-	F2	NC	-	-	-	-	-
-	-	-	F3	NC	-	-	-	-	-
-	-	-	F4	NC	-	-	-	-	-
-	-	-	C4	NC	-	-	-	-	-
-	-	-	C5	NC	-	-	-	-	-
-	-	-	C6	NC	-	-	-	-	-
-	-	-	B2	NC	-	-	-	-	-
-	-	-	B3	NC	-	-	-	-	-
-	-	-	B4	NC	-	-	-	-	-
-	-	-	B5	NC	-	-	-	-	-
-	-	-	B6	NC	-	-	-	-	-
-	-	-	A2	NC	-	-	-	-	-
-	-	-	A3	NC	-	-	-	-	-
-	-	-	A4	NC	-	-	-	-	-
-	-	-	A5	NC	-	-	-	-	-
-	-	-	A6	NC	-	-	-	-	-
F5	L2	J5	-	VSSAON	S	-	-	-	-
-	-	-	M6	VSSAON	S	-	-	-	-
G5	H6	G5	M8	V08CAP	A	-	-	-	-
-	-	-	D6	NC	-	-	-	-	-

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
VFBGA225	VFBGA273	TFBGA289	VFBGA361						
-	-	-	E6	NC	-	-	-	-	-
-	-	-	H6	NC	-	-	-	-	-
-	-	-	W13	NC	-	-	-	-	-
-	-	-	W14	NC	-	-	-	-	-

1. *Power supply is V_{DD}.*
2. *Power supply is V_{DD} - used in open drain with external pull up.*
3. *Power supply is V_{DD} - FMC signal on this GPIO not available for VFBGA225 package.*
4. *Power supply is V_{DD} or V_{SW} - input only in V_{SW}.*
5. *Power supply is V_{SW}.*
6. *Power supply is V_{SW} - OSC32_IN pin is also used as digital input in LSE bypass mode and tied to GPIO PC14 input (for test purpose only).*
7. *Power supply is V_{SW} - OSC32_OUT pin is also tied to GPIO PC15 input (for test purpose only).*
8. *Power supply is $V_{DDA18AON}$, must be always connected at board level to VDDA18AON.*
9. *Power supply is V_{DDIO3}.*
10. *Power supply is V_{DDIO1}.*
11. *Power supply is V_{DDIO2}.*
12. *Power supply is $V_{DDA18AON}$ - OSC_IN pin is also used as digital input in HSE bypass mode and tied to GPIO PH0 input (for test purpose only).*
13. *Power supply is $V_{DDA18AON}$ - OSC_OUT pin is also tied to GPIO PH1 input, used by boot ROM to autodetect HSE bypass mode.*

4.3 Alternate functions

Table 12. Alternate functions AF0 to AF7

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/6 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI5/6	I3C3 / LPTIM1/2 / SAI1/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6 / UART4 / USART6	I3C2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	MDF1/ SAI2/4 / UART5 / USART1/6	I2C1/2 / LPUART1 / TIM17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port A	PA0	-	LPTIM1_CH2	SPI5_RDY	-	SAI2_MCLK_B	UART5_TX	USART3_TX	TIM3_ETR
	PA1	-	-	SPI6_MISO	-	SAI3_SD_A	USART1_RTS/ USART1_DE	USART6_CK	TIM4_CH2
	PA2	-	LPTIM2_IN1	-	-	-	-	USART1_RX	-
	PA3	-	LPTIM2_ETR	-	-	-	-	USART1_TX	-

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/6 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI5/6	I3C3 / LPTIM1/2 / SAI1/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6 / UART4 / USART6	I3C2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	MDF1/ SAI2/4 / UART5 / USART1/6	I2C1/2 / LPUART1 / TIM17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port A	PA4	-	-	-	-	-	-	USART2_TX	FDCAN2_TX
	PA5	-	-	-	SPI4_MOSI	SAI2_MCLK_B	SAI2_SD_B	USART2_RTS/ USART2_DE	FDCAN2_RX
	PA6	-	-	-	SPI4_SCK	SAI2_FS_B	-	USART2_CK	TIM13_CH1
	PA7	-	-	CK_IN	SPI6_RDY	-	MDF1_CCK0	USART1_CTS/ USART1_NSS	TIM4_ETR
	PA8	-	LPTIM2_CH2	-	-	SAI1_FS_B	-	USART1_CK	-
	PA9	-	-	-	SPI4_NSS	SAI2_SCK_B	-	USART2_CTS/ USART2_NSS	LPTIM5_ETR
	PA10	-	-	-	SPI4_MISO	SAI2_SD_B	-	USART2_RX	LPTIM5_IN1
	PA11	-	SPI6_SCK	LPTIM2_CH1	-	SAI4_SD_B	-	-	-
	PA12	-	-	SPI6_MOSI	-	SAI3_FS_A	-	-	TIM4_CH1
	PA13	-	SPI6_RDY	I2S3_MCK	LPTIM2_ETR	-	MDF1_CKI3	USART2_CTS/ USART2_NSS	-
	PA14	-	SPI6_NSS	LPTIM2_CH2	-	SAI4_FS_B	MDF1_CCK1	-	-
	PA15	-	-	SPI3_MISO/ I2S3_SDI	-	-	-	USART2_RX	-
Port B	PB1	-	SPI3_NSS/ I2S3_WS	-	-	-	-	-	TIM16_CH1N
	PB2	-	-	SPI2_MOSI/ I2S2_SDO	-	-	MDF1_CKI3	TIM17_BKIN	TIM16_BKIN
	PB3	-	-	SPI2_NSS/ I2S2_WS	-	-	MDF1_SDI3	-	-
	PB5	-	-	I2S2_MCK	UART4_RTS/ UART4_DE	SAI4_SD_B	-	-	-
	PB6	-	-	SPI2_MISO/ I2S2_SDI	UART4_RX	SAI4_SCK_B	-	-	-
	PB7	-	SPI3_SCK/ I2S3_CK	-	UART4_TX	SAI4_MCLK_B	-	-	-

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/6 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI5/6	I3C3 / LPTIM1/2 / SAI1/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6 / UART4 / USART6	I3C2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	MDF1/ SAI2/4 / UART5 / USART1/6	I2C1/2 / LPUART1 / TIM17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port B	PB9	-	SPI3_RDY	-	-	-	-	USART1_RTS/ USART1_DE	FDCAN1_TX
	PB10	-	SPI3_MISO/ I2S3_SDI	-	-	-	-	USART1_RX	TIM17_CH1N
	PB11	-	I2S3_MCK	-	-	-	-	USART1_CTS/ USART1_NSS	FDCAN1_RX
	PB12	-	-	-	-	-	-	-	TIM13_CH1
	PB13	-	-	SPI2_MOSI/ I2S2_SDO	-	SAI1_SD_B	-	-	-
	PB14	-	-	SPI2_SCK/ I2S2_CK	-	-	-	-	-
	PB15	-	LPTIM1_IN2	SPI5_SCK	-	SAI2_SD_B	UART5_RX	-	TIM3_CH2
Port C	PC0	-	LPTIM1_CH1	-	SPI6_SCK	SAI3_MCLK_B	USART6_TX	-	-
	PC1	-	-	SPI3_MOSI/ I2S3_SDO	-	-	-	USART2_TX	-
	PC2	-	SPI6_MOSI	LPTIM2_IN1	-	SAI4_MCLK_B	MDF1_SDI3	USART2_RTS/ USART2_DE	-
	PC3	-	LPTIM1_IN2	SPI3_NSS/ I2S3_WS	SPI6_RDY	-	-	USART6_RTS/ USART6_DE	FDCAN2_TX
	PC4	-	-	-	SPI6_MISO	SAI3_FS_B	-	-	-
	PC5	-	-	SPDIFRX1_IN1	-	-	MDF1_SDI1	-	-
	PC6	-	RTC_REFIN	SPDIFRX1_IN0	-	-	MDF1_CKI1	-	-
	PC7	-	-	-	SPI6_MOSI	SAI3_SD_B	-	-	-
	PC8	-	LPTIM1_ETR	-	SPI6_NSS	SAI3_SCK_B	-	USART6_CTS/ USART6_NSS	-
	PC9	-	MCO1	SPI3_MISO/ I2S3_SDI	-	SAI2_SCK_A	-	-	TIM13_CH1
	PC10	-	-	SPI3_MOSI/ I2S3_SDO	-	-	-	-	LPTIM4_ETR

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/6 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI5/6	I3C3 / LPTIM1/2 / SAI1/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6 / UART4 / USART6	I3C2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	MDF1/ SAI2/4 / UART5 / USART1/6	I2C1/2 / LPUART1 / TIM17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port C	PC11	-	LPTIM1_CH1	SPI5_NSS	-	SAI2_MCLK_A	UART5_RTS/ UART5_DE	USART3_RTS/ USART3_DE	TIM3_CH1
	PC12	-	LPTIM1_CH2	-	I3C3_SCL	I3C2_SCL	MDF1_CKI2	-	-
	PC13	-	-	-	-	-	-	-	-
Port D	PD0	TRACECLK	HDP0	-	SAI1_D2	-	SAI4_FS_A	UART7_RX	TIM15_CH2
	PD1	-	HDP1	SPI1_MISO/ I2S1_SDI	SAI1_CK2	-	SAI4_SD_A	UART7_RTS/ UART7_DE	TIM15_CH1
	PD2	-	HDP2	SPI1_NSS/ I2S1_WS	SAI1_CK1	-	SAI4_SCK_A	UART7_CTS	TIM15_BKIN
	PD3	-	SAI1_MCLK_A	SPI2_SCK/ I2S2_CK	SAI1_D1	-	SAI4_MCLK_A	UART7_TX	TIM15_CH1N
	PD4	TRACED0	SPI4_MISO	HDP3	SAI1_D3	SAI1_SD_B	-	-	-
	PD5	TRACED1	SPI4_NSS	HDP4	SAI1_D4	SAI1_FS_B	-	-	-
	PD6	TRACED2	SPI4_MOSI	HDP5	-	SAI1_SCK_B	MDF1_SDI2	-	-
	PD7	TRACED3	SPI4_SCK	SPI1_RDY	-	SAI1_MCLK_B	MDF1_CKI2	-	-
	PD8	TRACED4	SPI4_RDY	I2S1_MCK	SAI1_FS_A	UART4_CTS	MDF1_SDI1	-	-
	PD9	TRACED5	HDP6	SPI1_MOSI/ I2S1_SDO	SAI1_SD_A	UART4_RTS/ UART4_DE	MDF1_CKI1	-	-
	PD10	TRACED6	HDP7	-	SAI1_SCK_A	UART4_RX	MDF1_SDI0	I2C1_SDA	-
	PD11	TRACED7	-	SPI1_SCK/ I2S1_CK	SAI1_MCLK_A	UART4_TX	MDF1_CKI0	I2C1_SCL	-
	PD12	-	-	SPI2_MISO/ I2S2_SDI	SPDIFRX1_IN2	-	-	-	-
	PD13	-	-	SPI2_NSS/ I2S2_WS	-	-	-	-	-
	PD14	-	I2S2_MCK	I2S1_MCK	-	-	-	-	FDCAN1_RX
	PD15	-	SPI1_RDY	-	-	-	-	I2C2_SDA	FDCAN1_TX
Port E	PE0	TRACED2	LPTIM2_CH1	SPI1_SCK/ I2S1_CK	SPI3_RDY	-	-	USART3_CK	-

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/6 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI5/6	I3C3 / LPTIM1/2 / SAI1/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6 / UART4 / USART6	I3C2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	MDF1/ SAI2/4 / UART5 / USART1/6	I2C1/2 / LPUART1 / TIM17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port E	PE1	TRACED3	LPTIM2_CH2	I2S1_MCK	I2S3_MCK	-	-	USART3_RX	-
	PE2	-	LPTIM2_ETR	SPI1_MISO/ I2S1_SDI	SPI3_MOSI/ I2S3_SDO	SAI1_SCK_B	-	-	-
	PE3	TRACECLK	-	SPI1_RDY	SPI3_SCK/ I2S3_CK	SAI1_MCLK_B	-	USART3_TX	-
	PE4	TRACED0	LPTIM2_IN1	SPI1_MOSI/ I2S1_SDO	SPI3_MISO/ I2S3_SDI	SAI1_SD_B	-	USART3_CTS/ USART3_NSS	FDCAN1_TX
	PE5	TRACED1	LPTIM2_IN2	SPI1_NSS/ I2S1_WS	SPI3_NSS/ I2S3_WS	SAI1_FS_B	-	USART3_RTS/ USART3_DE	FDCAN1_RX
	PE6	-	SPI4_RDY	-	-	SPDIFRX1_IN2	-	USART1_TX	-
	PE7	-	-	-	SAI4_D4	SPDIFRX1_IN3	-	USART1_RX	-
	PE8	-	SPI4_MOSI	-	SAI4_CK1	SAI4_MCLK_A	MDF1_CKI0	-	-
	PE9	-	SPI4_MISO	-	SAI4_D2	SAI4_FS_A	-	USART1_CK	-
	PE10	-	SPI4_SCK	-	SAI4_D1	SAI4_SD_A	-	USART1_CTS/ USART1_NSS	-
	PE11	-	-	-	SAI4_D3	SAI1_FS_A	-	-	TIM15_CH2
	PE12	-	SPI4_NSS	-	SAI4_CK2	SAI4_SCK_A	MDF1_SDI0	USART1_RTS/ USART1_DE	-
	PE13	-	-	-	-	SAI1_SD_A	-	-	TIM15_CH1
	PE14	-	-	-	-	SAI1_MCLK_A	-	-	TIM15_BKIN
	PE15	-	-	-	-	SAI1_SCK_A	-	-	TIM15_CH1N
Port F	PF0	-	-	SPI3_SCK/ I2S3_CK	-	-	-	-	FDCAN2_RX
	PF1	-	SPI6_MISO	LPTIM2_IN2	-	SAI4_SCK_B	-	USART2_CK	-
	PF2	-	-	SPI3_RDY	-	-	-	I2C1_SMBA	-
	PF3	-	-	-	-	SAI2_SCK_B	MDF1_CCK0	-	TIM3_CH4
	PF4	-	RTC_OUT2	SPI6_NSS	-	SAI3_SCK_A	-	USART6_RX	TIM4_CH4
	PF5	-	-	SPI6_SCK	-	SAI3_MCLK_A	-	USART6_TX	TIM4_CH3

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/6 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI5/6	I3C3 / LPTIM1/2 / SAI1/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6 / UART4 / USART6	I3C2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	MDF1/ SAI2/4 / UART5 / USART1/6	I2C1/2 / LPUART1 / TIM17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port F	PF6	-	RTC_OUT2	-	SAI3_MCLK_B	-	-	USART6_CK	TIM12_CH1
	PF7	-	-	SPDIFRX1_IN1	SPI6_SCK	SAI3_SD_A	-	-	TIM2_ETR
	PF8	-	RTC_REFIN	-	SAI3_SCK_B	-	-	USART3_RX	TIM12_CH2
	PF9	-	-	-	SAI3_SD_B	SAI2_SD_A	-	-	TIM2_CH2
	PF10	-	MCO2	SPI3_RDY	-	SAI2_MCLK_A	-	-	TIM2_CH3
	PF11	-	MCO1	SPDIFRX1_IN0	SPI6_RDY	SAI2_SCK_A	-	-	TIM2_CH4
	PF12	TRACECLK	-	SPI5_MISO	SPI1_MISO/ I2S1_SDI	-	-	-	-
	PF13	TRACED0	HDP0	CK_IN	USART6_TX	SPI2_NSS/ I2S2_WS	-	USART3_CTS/ USART3_NSS	-
	PF15	TRACED2	HDP2	SPI2_RDY	USART6_CTS/ USART6_NSS	SPI2_SCK/ I2S2_CK	-	USART3_CK	TIM2_CH2
Port G	PG0	-	LPTIM1_IN1	-	I3C3_SDA	I3C2_SDA	MDF1_SDI2	-	-
	PG1	-	LPTIM1_IN1	I2S3_MCK	I3C3_SCL	SAI2_SD_A	UART5_CTS	USART3_CTS/ USART3_NSS	-
	PG2	-	RTC_REFIN	I2S3_MCK	I3C3_SDA	SAI2_FS_A	-	USART3_CK	-
	PG3	-	LPTIM1_ETR	SPI5_MOSI	-	SAI2_FS_B	-	-	TIM3_CH3
	PG4	-	-	SPI5_MISO	SAI3_FS_B	-	-	-	LPTIM4_IN1
	PG5	TRACED3	HDP3	-	USART6_RTS/ USART6_DE	-	-	-	TIM2_CH3
	PG7	TRACED5	HDP5	SPI5_NSS	SPI1_NSS/ I2S1_WS	-	-	-	-
	PG8	TRACED6	HDP6	SPI5_RDY	SPI1_RDY	USART6_CK	UART5_RTS/ UART5_DE	-	-
	PG9	TRACED7	-	-	-	-	UART5_TX	-	-
	PG10	TRACED8	HDP0	-	-	-	UART5_RX	-	-
	PG11	TRACED9	HDP1	-	-	-	-	-	FDCAN1_TX
	PG12	TRACED10	HDP2	-	-	-	-	-	FDCAN1_RX

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		DBG	DBG / HDP / LPTIM1/2 / RTC / SAI1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI4/6 / SYS	HDP / I2S / LPTIM2/3 / SPDIFRX1 / SPI1 / I2S1 / SPI2 / I2S2 / SPI3 / I2S3 / SPI5/6	I3C3 / LPTIM1/2 / SAI1/3/4 / SPDIFRX1 / SPI1 / I2S1 / SPI3 / I2S3 / SPI4/6 / UART4 / USART6	I3C2 / MDF1 / SAI1/2/3/4 / SPDIFRX1 / SPI2 / I2S2 / TIM8 / UART4 / USART6	MDF1/ SAI2/4 / UART5 / USART1/6	I2C1/2 / LPUART1 / TIM17 / UART7 / USART1/2/3/6	FDCAN1/2 / LPTIM4/5 / TIM2/3/4/12/13/15/16/17
Port G	PG13	TRACED11	HDP3	-	-	-	-	-	-
	PG14	TRACED12	HDP4	-	-	-	-	USART1_TX	-
	PG15	TRACED13	HDP5	-	LPTIM1_CH2	-	-	USART1_RX	-
Port H	PH4	DBTRGI	DBTRGO	-	-	-	-	UART7_TX	TIM17_BKIN
	PH5	DBTRGO	DBTRGI	-	-	SAI2_FS_A	-	-	TIM2_CH1
	PH7	-	-	SPI1_MOSI/ I2S1_SDO	-	UART4_TX	-	UART7_RTS/ UART7_DE	TIM17_CH1
	PH8	-	-	SPI1_MISO/ I2S1_SDI	SPDIFRX1_IN3	UART4_RX	-	UART7_CTS	-
	PH9	-	-	-	SPI6_NSS	SAI3_MCLK_A	-	USART6_RX	TIM15_CH1N
	PH10	-	-	SPI1_SCK/ I2S1_CK	SPI6_MOSI	SAI3_SCK_A	-	-	TIM15_CH1
	PH11	-	-	-	SPI6_MISO	SAI3_FS_A	-	-	TIM15_CH2
	PH12	-	-	SPI3_NSS/ I2S3_WS	SPI6_MISO	-	-	-	-
	PH13	-	-	SPI3_SCK/ I2S3_CK	SPI6_MOSI	-	-	-	TIM15_BKIN
Port I	PI0	TRACED14	HDP6	-	LPTIM1_IN1	SAI4_MCLK_B	-	USART1_CK	-
	PI1	TRACED15	HDP7	-	-	-	-	-	-
	PI4	-	-	-	LPTIM1_CH1	SAI4_FS_B	-	-	-
	PI5	-	-	SPI5_MOSI	SPI1_MOSI/ I2S1_SDO	-	UART5_CTS	-	-
	PI6	-	MCO1	-	-	-	-	USART3_TX	TIM2_ETR
	PI8	-	-	-	-	-	-	-	-
Port Z	PZ0	-	-	LPTIM3_IN1	SPI6_MOSI	TIM8_CH1	-	LPUART1_TX	LPTIM5_OUT
	PZ1	-	-	LPTIM3_CH1	SPI6_MISO	TIM8_CH2	-	LPUART1_RX	LPTIM5_ETR
	PZ3	DBTRGI	DBTRGO	LPTIM3_ETR	SPI6_NSS	MDF1_SDI3	-	LPUART1_CTS	LPTIM4_IN1

Table 13. **Alternate functions AF8 to AF15**

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/3 / I3C1 / IC21 / TIM1/2/3/5/8/10/11/12 / UART7 / USART2	DCMI / PSSI / DCMIPP / ETH1/2 / I2C1/2/3 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3 / I3C1 / LCD / LPTIM3/4 / OCTOSPI1 / SDMMC1/3 / TIM14	DCMI / PSSI / DCMIPP / ETH1/2 / FMC / I2C2/3 / I3C3 / LCD / OCTOSPI1 / SDMMC1	ETH1/2 / FMC / I2C1 / LCD / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / ETH1/2 / I3C2 / LCD / OCTOSPI1 / SDMMC2	DCMI / PSSI / DCMIPP / LCD / SDMMC2/3	SYS
Port A	PA0	TIM5_CH2	-	ETH2_MII_RXD2	-	FMC_NL	-	DCMI_D9/ PSSI_D9/ DCMIPP_D9	EVENTOUT
	PA1	I2C1_SDA	-	-	LCD_R3	-	DCMI_D5/ PSSI_D5/ DCMIPP_D5	-	EVENTOUT
	PA2	I3C1_SDA	-	I2C1_SDA	LCD_B0	-	DCMI_D3/ PSSI_D3/ DCMIPP_D3	-	EVENTOUT
	PA3	I3C1_SCL	I2C3_SMBA	I2C1_SCL	LCD_B1	-	DCMI_D2/ PSSI_D2/ DCMIPP_D2	-	EVENTOUT
	PA4	TIM2_CH1	-	LCD_R1	-	-	ETH1_PTP_AUX_TS	-	EVENTOUT
	PA5	TIM2_CH4	-	LCD_G0	-	-	DCMI_D13/ PSSI_D13/ DCMIPP_D13	-	EVENTOUT
	PA6	TIM2_ETR	-	LCD_G4	-	FMC_NE1	DCMI_D12/ PSSI_D12/ DCMIPP_D12	-	EVENTOUT
	PA7	I2C2_SMBA	-	LCD_B5	I2C3_SMBA	I2C1_SMBA	DCMI_D6/ PSSI_D6/ DCMIPP_D6	-	EVENTOUT
	PA8	USART2_RX	I2C2_SCL	-	-	LCD_B2	DCMI_D4/ PSSI_D4/ DCMIPP_D4	-	EVENTOUT
	PA9	TIM2_CH3	-	ETH1_MDC	-	LCD_G7	PSSI_D14/ DCMIPP_D14	-	EVENTOUT
	PA10	TIM2_CH2	-	ETH1_MDIO	-	LCD_R6	PSSI_D15/ DCMIPP_D15	-	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/3 / I3C1 / IC21 / TIM1/2/3/5/8/10/11/12 / UART7 / USART2	DCMI / PSSI / DCMIPP / ETH1/2 / I2C1/2/3 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3 / I3C1 / LCD / LPTIM3/4 / OCTOSPI1 / SDMMC1/3 / TIM14	DCMI / PSSI / DCMIPP / ETH1/2 / FMC / I2C2/3 / I3C3 / LCD / OCTOSPI1 / SDMMC1	ETH1/2 / FMC / I2C1 / LCD / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / ETH1/2 / I3C2 / LCD / OCTOSPI1 / SDMMC2	DCMI / PSSI / DCMIPP / LCD / SDMMC2/3	SYS
Port A	PA11	-	-	ETH1_MII_RX_DV/ ETH1_RGMII_RX_CTL/ ETH1_RMII_CRS_DV	-	-	-	-	EVENTOUT
	PA12	I2C1_SCL	-	ETH1_PHY_INTN	-	-	-	-	EVENTOUT
	PA13	-	I2C3_SMBA	ETH1_MII_TX_EN/ ETH1_RGMII_TX_CTL/ ETH1_RMII_TX_EN	-	-	-	-	EVENTOUT
	PA14	-	-	ETH1_MII_RX_CLK/ ETH1_RGMII_RX_CLK/ ETH1_RMII_REF_CLK	-	-	-	-	EVENTOUT
	PA15	-	I2C3_SDA	ETH1_MII_TXD0 / ETH1_RGMII_TXD0/ ETH1_RMII_TXD0	-	-	-	-	EVENTOUT
Port B	PB1	-	-	-	-	FMC_NCE4	-	-	EVENTOUT
	PB2	-	-	-	-	FMC_AD12/ FMC_D12	-	-	EVENTOUT
	PB3	-	-	-	-	FMC_NCE3	-	-	EVENTOUT
	PB5	-	I2C2_SCL	-	-	FMC_AD8/ FMC_D8	I3C2_SCL	SDMMC3_D123DIR	EVENTOUT
	PB6	-	-	-	-	FMC_AD9/ FMC_D9	-	SDMMC3_D0DIR	EVENTOUT
	PB7	-	TIM12_CH1	-	-	FMC_AD10/ FMC_D10	-	SDMMC3_CDIR	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/3 / I3C1 / IC21 / TIM1/2/3/5/8/10/11/12 / UART7 / USART2	DCMI / PSSI / DCMIPP / ETH1/2 / I2C1/2/3 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3 / I3C1 / LCD / LPTIM3/4 / OCTOSPI1 / SDMMC1/3 / TIM14	DCMI / PSSI / DCMIPP / ETH1/2 / FMC / I2C2/3 / I3C3 / LCD / OCTOSPI1 / SDMMC1	ETH1/2 / FMC / I2C1 / LCD / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / ETH1/2 / I3C2 / LCD / OCTOSPI1 / SDMMC2	DCMI / PSSI / DCMIPP / LCD / SDMMC2/3	SYS
Port B	PB9	-	TIM10_CH1	-	-	FMC_AD13/ FMC_D13	-	-	EVENTOUT
	PB10	-	-	-	-	FMC_AD15/ FMC_D15	-	-	EVENTOUT
	PB11	-	TIM12_CH2	-	-	FMC_AD14/ FMC_D14	OCTOSPI1_NCS2	-	EVENTOUT
	PB12	-	-	SDMMC3_D2	FMC_NWAIT	-	-	DCMI_D12/ PSSI_D12/ DCMIPP_D12	EVENTOUT
	PB13	-	-	SDMMC3_CK	FMC_AD5/ FMC_D5	-	-	-	EVENTOUT
	PB14	-	TIM4_CH2	SDMMC3_D0	FMC_AD7/ FMC_D7	-	-	-	EVENTOUT
	PB15	TIM5_CH1	-	ETH1_PPS_OUT	-	FMC_A18	LCD_R4	DCMI_D8/ PSSI_D8/ DCMIPP_D8	EVENTOUT
Port C	PC0	-	DCMI_D0/ PSSI_D0/ DCMIPP_D0	ETH2_MII_RX_CLK/ ETH2_RMII_REF_CLK	ETH1_MII_TX_CLK	ETH1_RGMII_GTX_CLK	LCD_G7	-	EVENTOUT
	PC1	-	I2C3_SCL	ETH1_MII_TXD1 / ETH1_RGMII_TXD1/ ETH1_RMII_TXD1	-	-	-	-	EVENTOUT
	PC2	-	-	ETH1_MII_RXD1 / ETH1_RGMII_RXD1/ ETH1_RMII_RXD1	-	-	-	-	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/3 / I3C1 / IC21 / TIM1/2/3/5/8/10/11/12 / UART7 / USART2	DCMI / PSSI / DCMIPP / ETH1/2 / I2C1/2/3 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3 / I3C1 / LCD / LPTIM3/4 / OCTOSPI1 / SDMMC1/3 / TIM14	DCMI / PSSI / DCMIPP / ETH1/2 / FMC / I2C2/3 / I3C3 / LCD / OCTOSPI1 / SDMMC1	ETH1/2 / FMC / I2C1 / LCD / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / ETH1/2 / I3C2 / LCD / OCTOSPI1 / SDMMC2	DCMI / PSSI / DCMIPP / LCD / SDMMC2/3	SYS
Port C	PC3	-	-	ETH2_MII_RX_DV/ ETH2_RGMII_RX_CTL/ ETH2_RMII_CRS_DV	ETH1_MII_RX_ER	-	LCD_G6	DCMI_D3/ PSSI_D3/ DCMIPP_D3	EVENTOUT
	PC4	-	-	ETH2_MII_TX_EN/ ETH2_RGMII_TX_CTL/ ETH2_RMII_TX_EN	-	ETH1_RGMII_CLK125	LCD_R0	-	EVENTOUT
	PC5	TIM8_CH1N	I2C1_SDA	ETH2_MDIO	ETH1_MII_COL	FMC_A25	ETH1_PPS_OUT	LCD_DE	EVENTOUT
	PC6	TIM8_CH1	I2C1_SCL	ETH2_MDC	ETH1_MII_CRS	FMC_A24	ETH1_PHY_INTN	LCD_CLK	EVENTOUT
	PC7	TIM8_CH2N	-	ETH2_MII_TXD0 / ETH2_RGMII_TXD0/ ETH2_RMII_TXD0	ETH1_MII_TXD2	-	LCD_B4	DCMI_D1/ PSSI_D1/ DCMIPP_D1	EVENTOUT
	PC8	TIM8_CH2	-	ETH2_MII_TXD1 / ETH2_RGMII_TXD1/ ETH2_RMII_TXD1	ETH1_MII_TXD3	-	LCD_B3	DCMI_D2/ PSSI_D2/ DCMIPP_D2	EVENTOUT
	PC9	TIM8_CH4N	USBH_HS_OVRCUR	ETH2_MII_TXD2 / ETH2_RGMII_TXD2	-	FMC_A22	LCD_G2	DCMI_D7/ PSSI_D7/ DCMIPP_D7	EVENTOUT
	PC10	TIM8_CH4	USBH_HS_VBUSEN	ETH2_MII_TXD3 / ETH2_RGMII_TXD3	DCMI_D0/ PSSI_D0/ DCMIPP_D0	FMC_A23	LCD_G3	DCMI_D6/ PSSI_D6/ DCMIPP_D6	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/3 / I3C1 / IC21 / TIM1/2/3/5/8/10/11/12 / UART7 / USART2	DCMI / PSSI / DCMIPP / ETH1/2 / I2C1/2/3 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3 / I3C1 / LCD / LPTIM3/4 / OCTOSPI1 / SDMMC1/3 / TIM14	DCMI / PSSI / DCMIPP / ETH1/2 / FMC / I2C2/3 / I3C3 / LCD / OCTOSPI1 / SDMMC1	ETH1/2 / FMC / I2C1 / LCD / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / ETH1/2 / I3C2 / LCD / OCTOSPI1 / SDMMC2	DCMI / PSSI / DCMIPP / LCD / SDMMC2/3	SYS
Port C	PC11	TIM5_ETR	DCMI_HSYNC/ PSSI_DE/ DCMIPP_HSYNC	ETH2_MII_RXD3 / ETH2_RGMII_RXD3	-	FMC_NBL1	LCD_R2	DCMI_D10/ PSSI_D10/ DCMIPP_D10	EVENTOUT
	PC12	TIM8_CH3	I2C3_SCL	ETH2_MII_RXD1 / ETH2_RGMII_RXD1/ ETH2_RMII_RXD1	ETH1_MII_RXD3	-	LCD_G1	DCMI_D5/ PSSI_D5/ DCMIPP_D5	EVENTOUT
	PC13	-	-	-	-	-	-	-	EVENTOUT
Port D	PD0	-	SDVSEL1	OCTOSPI1_CLK	-	-	DCMI_PIXCLK/ PSSI_PDCK/ DCMIPP_PIXCLK	-	EVENTOUT
	PD1	TIM1_BKIN	-	OCTOSPI1_NCLK	OCTOSPI1_NCS2	-	DCMI_HSYNC/ PSSI_DE/ DCMIPP_HSYNC	-	EVENTOUT
	PD2	TIM1_ETR	-	OCTOSPI1_DQS	OCTOSPI1_NCS2	-	DCMI_VSYNC/ PSSI_RDY/ DCMIPP_VSYNC	-	EVENTOUT
	PD3	TIM1_BKIN2	SDVSEL2	OCTOSPI1_NCS1	-	-	PSSI_D15/ DCMIPP_D15	-	EVENTOUT
	PD4	TIM1_CH4N	TIM4_CH1	OCTOSPI1_IO0	-	-	PSSI_D14/ DCMIPP_D14	-	EVENTOUT
	PD5	TIM1_CH3N	TIM4_CH2	OCTOSPI1_IO1	-	-	DCMI_D13/ PSSI_D13/ DCMIPP_D13	-	EVENTOUT
	PD6	TIM1_CH2N	TIM4_CH3	OCTOSPI1_IO2	-	-	DCMI_D12/ PSSI_D12/ DCMIPP_D12	-	EVENTOUT
	PD7	TIM1_CH1N	TIM4_CH4	OCTOSPI1_IO3	-	-	DCMI_D11/ PSSI_D11/ DCMIPP_D11	-	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/3 / I3C1 / IC21 / TIM1/2/3/5/8/10/11/12 / UART7 / USART2	DCMI / PSSI / DCMIPP / ETH1/2 / I2C1/2/3 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3 / I3C1 / LCD / LPTIM3/4 / OCTOSPI1 / SDMMC1/3 / TIM14	DCMI / PSSI / DCMIPP / ETH1/2 / FMC / I2C2/3 / I3C3 / LCD / OCTOSPI1 / SDMMC1	ETH1/2 / FMC / I2C1 / LCD / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / ETH1/2 / I3C2 / LCD / OCTOSPI1 / SDMMC2	DCMI / PSSI / DCMIPP / LCD / SDMMC2/3	SYS
Port D	PD8	TIM1_CH4	TIM4_ETR	OCTOSPI1_IO4	SDMMC1_D7	SDMMC1_D123DIR	DCMI_D10/ PSSI_D10/ DCMIPP_D10	-	EVENTOUT
	PD9	TIM1_CH3	-	OCTOSPI1_IO5	SDMMC1_D6	SDMMC1_D0DIR	DCMI_D9/ PSSI_D9/ DCMIPP_D9	-	EVENTOUT
	PD10	TIM1_CH2	TIM14_CH1	OCTOSPI1_IO6	SDMMC1_D5	SDMMC1_CDIR	DCMI_D8/ PSSI_D8/ DCMIPP_D8	-	EVENTOUT
	PD11	TIM1_CH1	SDVSEL1	OCTOSPI1_IO7	SDMMC1_D4	SDMMC1_CKIN	DCMI_D7/ PSSI_D7/ DCMIPP_D7	-	EVENTOUT
	PD12	-	TIM4_ETR	SDMMC3_CMD	FMC_AD6/ FMC_D6	-	-	-	EVENTOUT
	PD13	-	TIM4_CH4	SDMMC3_D1	FMC_AD11/ FMC_D11	FMC_NWE	-	-	EVENTOUT
	PD14	TIM11_CH1	-	-	FMC_AD4/ FMC_D4	SDMMC3_D3	DCMI_D1/ PSSI_D1/ DCMIPP_D1	-	EVENTOUT
	PD15	TIM1_BKIN2	TIM5_ETR	-	FMC_AD3/ FMC_D3	SDMMC3_CKIN	DCMI_D0/ PSSI_D0/ DCMIPP_D0	-	EVENTOUT
Port E	PE0	-	-	SDMMC1_D2	-	-	-	-	EVENTOUT
	PE1	-	-	SDMMC1_D3	-	-	-	-	EVENTOUT
	PE2	TIM10_CH1	-	SDMMC1_CMD	-	-	-	-	EVENTOUT
	PE3	TIM11_CH1	-	SDMMC1_CK	-	-	-	-	EVENTOUT
	PE4	-	-	SDMMC1_D0	-	-	-	-	EVENTOUT
	PE5	-	-	SDMMC1_D1	-	-	-	-	EVENTOUT
	PE6	TIM1_ETR	-	-	FMC_AD1/ FMC_D1	SDMMC2_D6	SDMMC2_D0DIR	SDMMC2_CK	EVENTOUT
	PE7	TIM1_CH4N	-	TIM14_CH1	FMC_AD2/ FMC_D2	SDMMC2_D7	SDMMC2_D123DIR	-	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/3 / I3C1 / IC21 / TIM1/2/3/5/8/10/11/12 / UART7 / USART2	DCMI / PSSI / DCMIPP / ETH1/2 / I2C1/2/3 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3 / I3C1 / LCD / LPTIM3/4 / OCTOSPI1 / SDMMC1/3 / TIM14	DCMI / PSSI / DCMIPP / ETH1/2 / FMC / I2C2/3 / I3C3 / LCD / OCTOSPI1 / SDMMC1	ETH1/2 / FMC / I2C1 / LCD / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / ETH1/2 / I3C2 / LCD / OCTOSPI1 / SDMMC2	DCMI / PSSI / DCMIPP / LCD / SDMMC2/3	SYS
Port E	PE8	TIM1_CH1	-	-	FMC_A17/ FMC_ALE	SDMMC2_D2	-	-	EVENTOUT
	PE9	TIM1_CH4	-	-	FMC_AD0/ FMC_D0	SDMMC2_D5	SDMMC2_CDIR	-	EVENTOUT
	PE10	TIM1_CH3	-	FMC_NE3	FMC_NCE2	SDMMC2_D4	SDMMC2_CKIN	-	EVENTOUT
	PE11	TIM1_CH3N	-	-	FMC_A16/ FMC_CLE	SDMMC2_D1	-	-	EVENTOUT
	PE12	TIM1_CH2	-	FMC_NE2	FMC_NCE1	SDMMC2_D3	-	-	EVENTOUT
	PE13	TIM1_CH2N	-	-	FMC_RNB	SDMMC2_D0	-	-	EVENTOUT
	PE14	TIM1_BKIN	-	-	FMC_NWE	SDMMC2_CK	-	-	EVENTOUT
	PE15	TIM1_CH1N	-	-	FMC_NOE	SDMMC2_CMD	-	-	EVENTOUT
Port F	PF0	TIM12_CH2	I2C2_SDA	ETH1_MDC	ETH2_MII_CRS	-	I3C2_SDA	-	EVENTOUT
	PF1	-	-	ETH1_MII_RXD0 / ETH1_RGMII_RXD0/ ETH1_RMII_RXD0	-	-	-	-	EVENTOUT
	PF2	TIM12_CH1	I2C2_SCL	ETH1_MDIO	ETH2_MII_COL	FMC_NE4	I3C2_SCL	-	EVENTOUT
	PF3	TIM8_BKIN2	ETH1_CLK	ETH2_PPS_OUT	-	FMC_A20	LCD_R6	DCMI_HSYNC/ PSSI_DE/ DCMIPP_HSYNC	EVENTOUT
	PF4	ETH1_MDC	ETH2_CLK	ETH2_PPS_OUT	ETH1_PPS_OUT	-	LCD_B7	-	EVENTOUT
	PF5	ETH1_MDIO	ETH1_CLK	ETH2_PHY_INTN	ETH1_PHY_INTN	-	LCD_B6	-	EVENTOUT
	PF6	-	I2C3_SMBA	ETH2_MII_RX_CLK/ ETH2_RGMII_RX_CLK/ ETH2_RMII_REF_CLK	-	-	LCD_B0	-	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/3 / I3C1 / IC21 / TIM1/2/3/5/8/10/11/12 / UART7 / USART2	DCMI / PSSI / DCMIPP / ETH1/2 / I2C1/2/3 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3 / I3C1 / LCD / LPTIM3/4 / OCTOSPI1 / SDMMC1/3 / TIM14	DCMI / PSSI / DCMIPP / ETH1/2 / FMC / I2C2/3 / I3C3 / LCD / OCTOSPI1 / SDMMC1	ETH1/2 / FMC / I2C1 / LCD / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / ETH1/2 / I3C2 / LCD / OCTOSPI1 / SDMMC2	DCMI / PSSI / DCMIPP / LCD / SDMMC2/3	SYS
Port F	PF7	-	-	ETH2_RGMII_GTX_CLK	ETH2_MII_TX_CLK	-	LCD_R1	-	EVENTOUT
	PF8	-	ETH1_CLK	ETH2_RGMII_CLK125	ETH2_MII_RX_ER	ETH2_MII_RX_DV/ ETH2_RMII_CRS_DV	LCD_G0	-	EVENTOUT
	PF9	-	-	ETH2_MII_RXD2 / ETH2_RGMII_RXD2	ETH2_MDIO	-	-	-	EVENTOUT
	PF10	-	-	ETH2_MII_TXD2	-	-	-	-	EVENTOUT
	PF11	-	-	ETH2_MII_TXD3	-	-	-	-	EVENTOUT
	PF12	TIM5_CH1	-	-	-	-	LCD_CLK	DCMI_D0/ PSSI_D0/ DCMIPP_D0	EVENTOUT
	PF13	TIM3_CH3	-	-	-	-	LCD_R2	-	EVENTOUT
	PF15	TIM3_ETR	-	-	-	-	LCD_R4	-	EVENTOUT
Port G	PG0	TIM8_CH3N	I2C3_SDA	ETH2_MII_RXD0 / ETH2_RGMII_RXD0/ ETH2_RMII_RXD0	ETH1_MII_RXD2	-	LCD_G5	DCMI_D4/ PSSI_D4/ DCMIPP_D4	EVENTOUT
	PG1	TIM5_CH4	I2C3_SCL	ETH2_MII_RX_ER	ETH2_MII_RXD3	FMC_NBL0	LCD_VSYNC	DCMI_D11/ PSSI_D11/ DCMIPP_D11	EVENTOUT
	PG2	TIM5_CH3	I2C3_SDA	ETH2_MII_TX_CLK	ETH2_RGMII_CLK125	FMC_CLK	LCD_HSYNC	-	EVENTOUT
	PG3	TIM8_ETR	ETH2_CLK	ETH2_PHY_INTN	-	FMC_A19	LCD_R5	DCMI_PIXCLK/ PSSI_PDCK/ DCMIPP_PIXCLK	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/3 / I3C1 / IC21 / TIM1/2/3/5/8/10/11/12 / UART7 / USART2	DCMI / PSSI / DCMIPP / ETH1/2 / I2C1/2/3 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3 / I3C1 / LCD / LPTIM3/4 / OCTOSPI1 / SDMMC1/3 / TIM14	DCMI / PSSI / DCMIPP / ETH1/2 / FMC / I2C2/3 / I3C3 / LCD / OCTOSPI1 / SDMMC1	ETH1/2 / FMC / I2C1 / LCD / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / ETH1/2 / I3C2 / LCD / OCTOSPI1 / SDMMC2	DCMI / PSSI / DCMIPP / LCD / SDMMC2/3	SYS
Port G	PG4	TIM8_BKIN	-	ETH2_PPS_OUT	ETH2_MDC	FMC_A21	LCD_R7	DCMI_VSYNC/ PSSI_RDY/ DCMIPP_VSYNC	EVENTOUT
	PG5	-	-	-	-	-	LCD_R5	DCMI_PIXCLK/ PSSI_PDCK/ DCMIPP_PIXCLK	EVENTOUT
	PG7	TIM5_ETR	-	-	-	-	LCD_R7	DCMI_VSYNC/ PSSI_RDY/ DCMIPP_VSYNC	EVENTOUT
	PG8	TIM5_CH3	-	-	-	-	LCD_G2	DCMI_D2/ PSSI_D2/ DCMIPP_D2	EVENTOUT
	PG9	TIM5_CH4	-	-	-	-	LCD_G3	DCMI_D3/ PSSI_D3/ DCMIPP_D3	EVENTOUT
	PG10	TIM8_CH4N	-	-	-	-	LCD_G4	DCMI_D4/ PSSI_D4/ DCMIPP_D4	EVENTOUT
	PG11	TIM8_CH4	-	-	-	-	LCD_G5	DCMI_D5/ PSSI_D5/ DCMIPP_D5	EVENTOUT
	PG12	TIM8_CH1N	-	-	-	-	LCD_G6	DCMI_D6/ PSSI_D6/ DCMIPP_D6	EVENTOUT
	PG13	TIM8_CH2N	I2C1_SCL	I3C1_SCL	-	-	LCD_G7	DCMI_D7/ PSSI_D7/ DCMIPP_D7	EVENTOUT
	PG14	TIM8_BKIN2	-	-	-	-	LCD_B1	DCMI_D9/ PSSI_D9/ DCMIPP_D9	EVENTOUT
	PG15	TIM8_ETR	-	-	-	-	LCD_B2	DCMI_D10/ PSSI_D10/ DCMIPP_D10	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/3 / I3C1 / IC21 / TIM1/2/3/5/8/10/11/12 / UART7 / USART2	DCMI / PSSI / DCMIPP / ETH1/2 / I2C1/2/3 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3 / I3C1 / LCD / LPTIM3/4 / OCTOSPI1 / SDMMC1/3 / TIM14	DCMI / PSSI / DCMIPP / ETH1/2 / FMC / I2C2/3 / I3C3 / LCD / OCTOSPI1 / SDMMC1	ETH1/2 / FMC / I2C1 / LCD / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / ETH1/2 / I3C2 / LCD / OCTOSPI1 / SDMMC2	DCMI / PSSI / DCMIPP / LCD / SDMMC2/3	SYS
Port H	PH4	-	TIM5_CH2	LCD_R0	-	USBH_HS_OVRCUR	ETH1_PTP_AUX_TS	-	EVENTOUT
	PH5	UART7_RX	-	LCD_G1	-	USBH_HS_VBUSEN	ETH2_PTP_AUX_TS	-	EVENTOUT
	PH7	-	TIM5_CH4	-	-	-	-	-	EVENTOUT
	PH8	-	TIM5_CH1	I2C3_SMBA	I2C2_SMBA	-	-	-	EVENTOUT
	PH9	-	-	ETH1_RGMII_CLK125	ETH1_MII_RX_ER	-	-	-	EVENTOUT
	PH10	-	ETH2_MDC	ETH1_MII_TXD2 / ETH1_RGMII_TXD2	-	-	-	-	EVENTOUT
	PH11	-	ETH2_MDIO	ETH1_MII_TXD3 / ETH1_RGMII_TXD3	-	-	-	-	EVENTOUT
	PH12	TIM10_CH1	-	ETH1_MII_RXD2 / ETH1_RGMII_RXD2	-	-	-	-	EVENTOUT
	PH13	TIM11_CH1	-	ETH1_MII_RXD3 / ETH1_RGMII_RXD3	-	-	-	-	EVENTOUT
Port I	PI0	TIM8_BKIN	-	-	-	-	LCD_B3	DCMI_D11/ PSSI_D11/ DCMIPP_D11	EVENTOUT
	PI1	TIM8_CH3N	I2C1_SDA	I3C1_SDA	-	-	LCD_B4	DCMI_D8/ PSSI_D8/ DCMIPP_D8	EVENTOUT
	PI4	TIM8_CH3	-	-	-	-	LCD_B7	PSSI_D15/ DCMIPP_D15	EVENTOUT
	PI5	TIM5_CH2	-	-	-	-	LCD_DE	DCMI_D1/ PSSI_D1/ DCMIPP_D1	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ETH1 / I2C2/3 / I3C1 / IC21 / TIM1/2/3/5/8/10/11/12 / UART7 / USART2	DCMI / PSSI / DCMIPP / ETH1/2 / I2C1/2/3 / SDMMC1/2 / TIM4/5/10/12/14 / USBH_HS	ETH1/2 / FMC / I2C1/3 / I3C1 / LCD / LPTIM3/4 / OCTOSPI1 / SDMMC1/3 / TIM14	DCMI / PSSI / DCMIPP / ETH1/2 / FMC / I2C2/3 / I3C3 / LCD / OCTOSPI1 / SDMMC1	ETH1/2 / FMC / I2C1 / LCD / SDMMC1/2/3 / USBH_HS	DCMI / PSSI / DCMIPP / ETH1/2 / I3C2 / LCD / OCTOSPI1 / SDMMC2	DCMI / PSSI / DCMIPP / LCD / SDMMC2/3	SYS
Port I	PI6	TIM3_CH1	-	-	-	-	LCD_VSYNC	-	EVENTOUT
	PI8	-	-	-	-	-	-	-	EVENTOUT
Port Z	PZ0	I2C3_SDA	-	LPTIM3_CH2	I3C3_SDA	-	-	-	EVENTOUT
	PZ1	I2C3_SCL	I2C3_SMBA	-	I3C3_SCL	-	-	-	EVENTOUT
	PZ3	I2C3_SDA	-	LPTIM4_CH2	I3C3_SDA	-	-	-	EVENTOUT

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with a junction temperature at T_J = 25 ° C and $T_J = T_{Jmax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25 °C, V_{DD} = 3.3 V, V_{DDCORE} = 0.82 V, V_{DDCPU} = 0.8 V. They are given only as design guidelines and are not tested in production.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

5.1.3 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 9. Pin loading conditions.

5.1.4 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 10.

Figure 9. Pin loading conditions

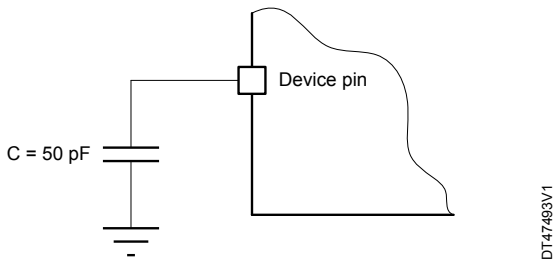
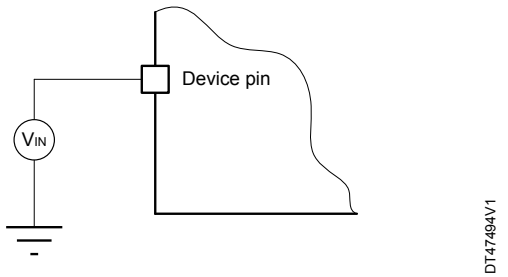
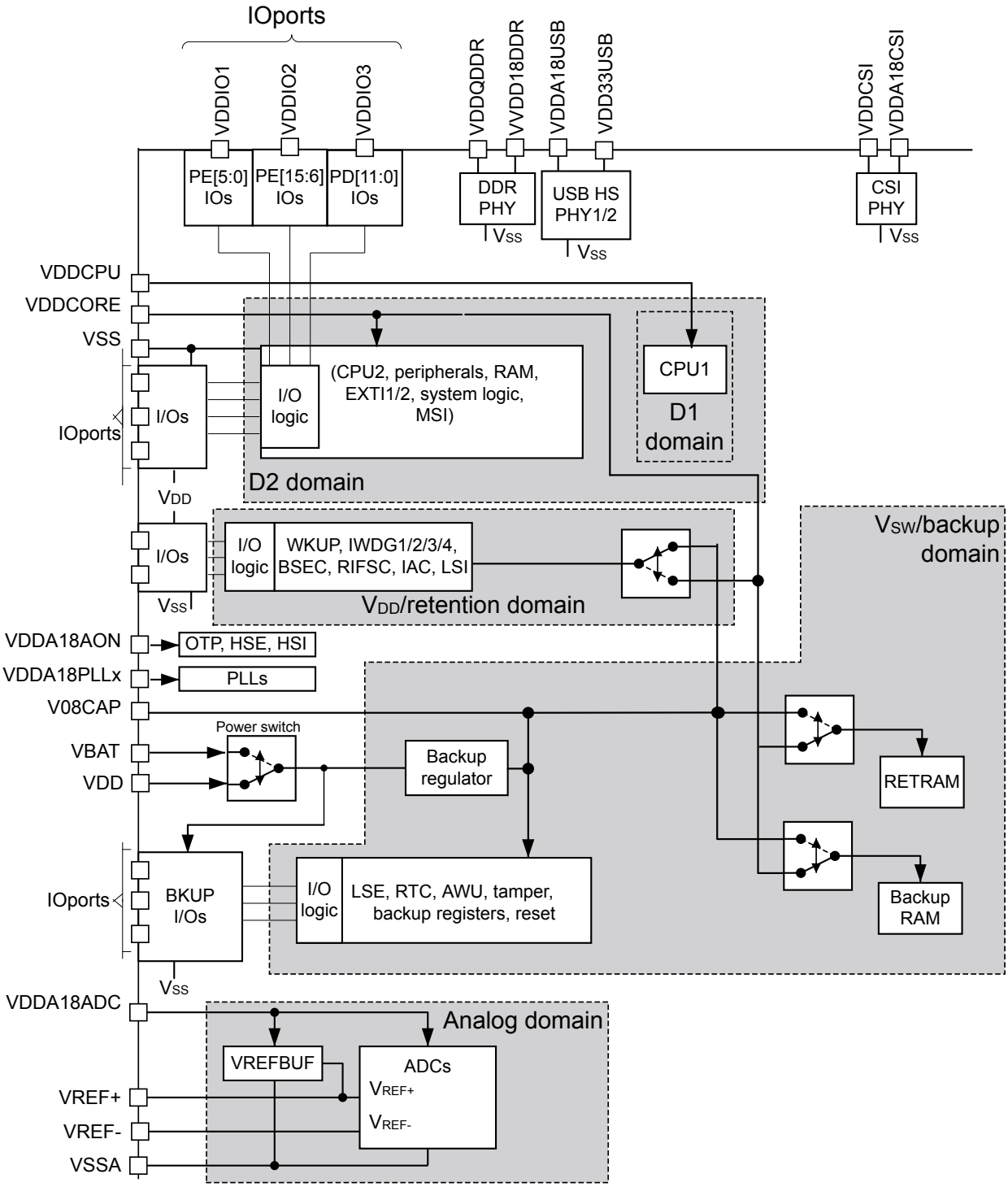


Figure 10. Pin input voltage



5.1.5 Power supply scheme

Figure 11. Power supply scheme

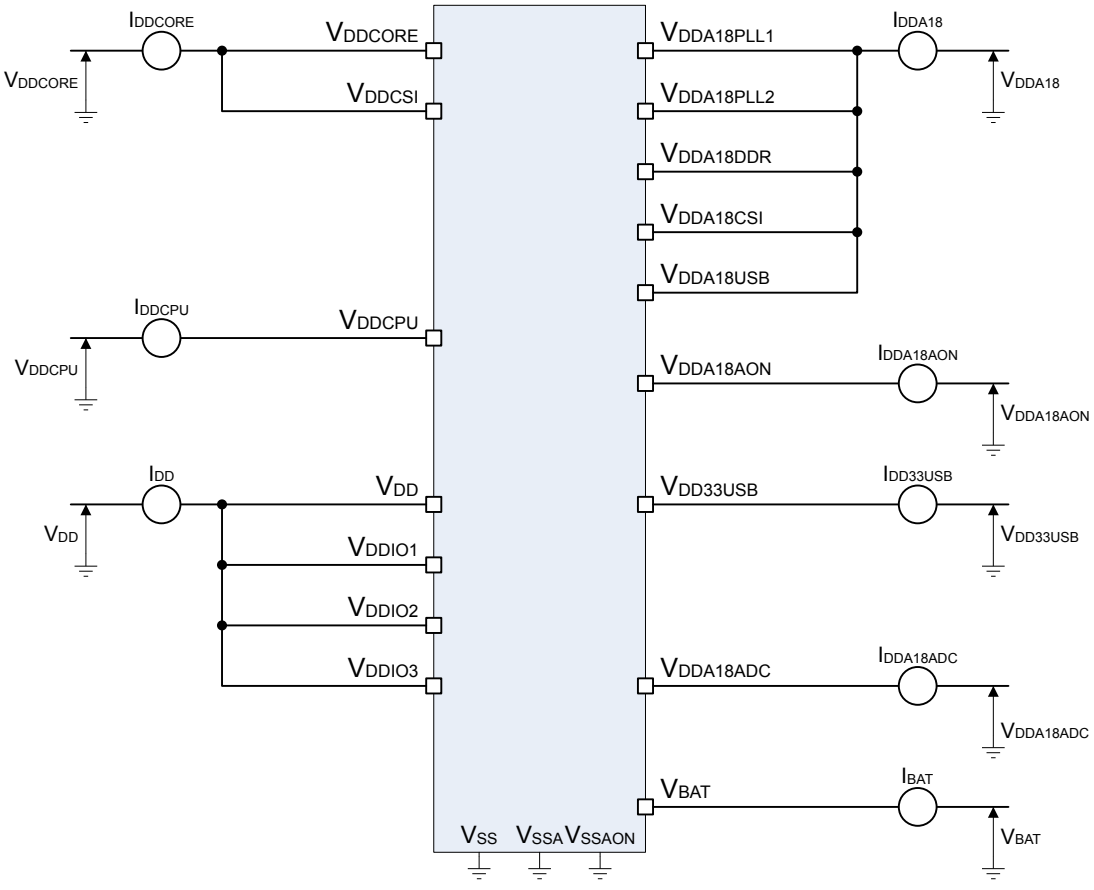


Caution: *Each power supply pair (V_{DD}/V_{SS}, V_{DDCORE}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.*

The number of needed capacitances and their values are provided in AN6055 Getting started with STM32MP21x MPUs hardware development available from the ST website www.st.com.

5.1.6 Current consumption measurement

Figure 12. Current consumption measurement scheme



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 14, Table 15, and Table 16 may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 qualification standard, extended mission profiles are available on demand.

Table 14. Voltage characteristics

Specified by design, not tested in production.
All powers and grounds pins must always be connected to an external power supply, in the permitted range.

Symbols	Ratings	Min	Max	Unit
V_{DDX} - V_{SS} range 1.8 V	External supply voltage (including V_{DD}, V_{DDIOx}, V_{BAT})	-0.3	2	V
V_{DDX} - V_{SS} range 3.3 V	External supply voltage (including V_{DD}, V_{DDIOx}, V_{BAT}, $V_{DD33USB}$)	-0.3	3.7	

Symbols	Ratings	Min	Max	Unit
$V_{DDCORE} - V_{SS}$	External core supply voltage (including V_{DDCORE}, V_{DDCPU}, V_{DDCSI})	-0.3	0.99	V
$V_{DDQDDR} - V_{SS}$	DDR IO supply voltage	-0.3	1.575	
$V_{DDA18} - V_{SS}$	1.8 V supply voltage (including $V_{DDA18AON}$, $V_{DDA18PLL1}$, $V_{DDA18PLL2}$, $V_{DDA18CSI}$, $V_{DDA18DDR}$, $V_{DDA18USB}$, $V_{DDA18ADC}$)	-0.3	1.98	
V_{IN}(1)	Input voltage on TT_xx pins (VDDIOxVRSEL = 0)	V_{SS} - 0.3	min(V_{DDIOx} + 0.3, 3.6)	
	Input voltage on TT_xx pins (VDDIOxVRSEL = 1)		min(V_{DDIOx} + 0.3, 1.98)	
	Input voltage on COMBOPHY pins		min($V_{DDCOMBOPHY}$ + 0.3, 0.99)	
$\lvert\Delta V_{DDx}\rvert$	Variations between different VDDX power pins of the same domain	-	50	mV
$\lvert V_{SSx}-V_{SS}\rvert$	Variations between all the different ground pins	-	50	

1. *V_{IN} maximum must always be respected. Refer to next table for the maximum allowed injected current values.*

Table 15. Current characteristics

Specified by design, not tested in production.

Symbols	Ratings	Condition	Max	Unit
I_{IO}	Output current sunk/source by any I/O and control pin	T_J > 110 °C	4	mA
		90 °C < T_J ≤ 110 °C	10	
		-40 °C < T_J ≤ 90 °C	20	
ΣI_{INJ}(PIN)	Total injected current (sum of all I/Os and control pins)		±25	

1. *When several inputs are submitted to a current injection, the maximum ΣI_{INJ}(PIN) is the absolute sum of the positive and negative injected currents (instantaneous values).*

Table 16. Thermal characteristics

Specified by design, not tested in production.

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature (suffix 3)	125	

5.3 Operating conditions

5.3.1 General operating conditions

Note: Features may be limited or absent in some devices or packages (see Section 2 for details).

Table 17. General operating conditions

Voltages in this table represent DC value at ball level.

Symbol	Parameter	Operating conditions	Min.	Typ.	Max.	Unit
F_{cpu1}	Cortex-A35 clock frequency	-	0	-	1200	MHz
$F_{cpu1\_overdrive}$	Cortex-A35 clock frequency in overdrive	STM32MP21xF only	0	-	1500	
$F_{ddrctrl}$	DDR memory clock frequency(1)	DDR3L DLL on	300	-	800	

Symbol	Parameter	Operating conditions	Min.	Typ.	Max.	Unit
$F_{ddrctrl}$	DDR memory clock frequency(1)	DDR3L DLL off	20	-	125	MHz
		DDR4 DLL on	625	-	800	
		DDR4 DLL off	20	-	125	
		LPDDR4	10	-	800	
$F_{ck\_icn\_hs\_mcu}$	Cortex-M33, MCU MLAHB memory clock frequency		0	-	300	
$F_{ck\_icn\_ddr}$	Clock frequency of Cortex-A35 AXI and DDRCTRL AXI buses		0	-	600	
$F_{ck\_icn\_hsl}$	Clock frequency of OTG, USBH, ETH1, and ETH2 buses		0	-	300	
$F_{ck\_icn\_ls\_mcu}$	Clock frequency of MCU MLAHB and MCU domain peripheral buses	in Run mode	0	-	150	
$F_{ck\_icn\_sdmmc}$	Clock frequency of MPU AHB5		0	-	200	
$F_{ck\_icn\_nic}$	Clock frequency of MPU GIC and BOOTROM		0	-	400	
$V_{DDA18AON}$(2)	Internal analog supply voltage		1.71	1.8	1.89(3)	V
V_{DD} (2)	I/O supply voltage	1.8 V range	1.71	1.8	1.89 (3)	
		3.3 V range(4)	3	3.3	3.6	
V_{DDIO1}, V_{DDIO2}, V_{DDIO3}(5)	Specific I/O supply voltage	1.8 V range	1.71	1.8	1.89 (3)	V
		3 V/3.3 V range(6)	2.7	3.3	3.6	
V_{DDCORE}, V_{DDCSI}(7)	Main digital logic supply voltage	Run1/2 mode	0.792	0.82	0.839	
		Stop1/2, LP-Stop1/2 modes	0.792	0.82	0.839	
		LPLV-Stop1/2 modes	0.64	0.67	0.839(8)	
		Standby1/2 modes	0	0	0.48	
V_{DDCPU}	Cortex-A35 supply voltage	Run1, Stop1, or LP-Stop1 mode, $F_{cpu1\_overdrive}$ range	0.859	0.91	0.968	
		Run1, Stop1 or LP-Stop1 mode, F_{cpu1} range	0.768	0.80	0.837	
		Run2, Stop2 or LP-Stop2 mode	0.768	0.80	0.837	
		LPLV-Stop1 (LPCFG_D1 = 0)	0.64	0.67	0.837 (8)	
		LPLV-Stop2 (LPCFG_D1 = 0) or Standby1/2 mode	0	0	0.48	
$V_{DDA18PLL1}$, $V_{DDA18PLL2}$, $V_{DDA18CSI}$(9)	1.8 V analog supply for PLLs, CSI PHY		1.71	1.8	1.89 (3)	
$V_{DDA18DDR}$(10)	1.8 V analog supply for DDRPHY		1.71	1.8	1.89	
$V_{DDA18USB}$ (10)	1.8 V analog supply for USBPHY		1.75	1.8	1.93	
$V_{DD33USB}$	3.3 V USB supply		3.07	3.3	3.6	
$V_{DDA18ADC}$	ADC operating voltage		1.62	1.8	1.89 (3)	
VREF+	ADC reference voltage		1.1	-	$V_{DDA18ADC}$	
V_{BAT}	Backup operating voltage		2.0(11)	-	3.6	
V_{DDQDDR}	DDR PHY supply voltage	DDR3L memory	1.283	1.35	1.45	
		DDR4 memory	1.14	1.2	1.26	
		LPDDR4 memory	1.06	1.1	1.17	
V_{08CAP}	Backup regulator output voltage(12)		0.72	0.8	0.88	

Symbol	Parameter	Operating conditions	Min.	Typ.	Max.	Unit
V_{IN}	I/O input voltage	I/O	-0.3	-	V_{DDxx} +0.3 (13)	V
		I/O when ADC is used	-0.3	-	$V_{DDA18ADC}$ +0.3 V	
		I/O when PVD_IN is used	-0.3	-	$V_{DD18AON}$ +0.3 V	
		DDR I/O	-0.3	-	V_{DDQDDR}	
T_J	Junction temperature range	Suffix 3 version	-40	-	125	°C

1. *Values depend on the external memory device choice.*
2. *$V_{DDA18AON}$ and V_{DD} must be present before any of other supplies.*
3. *Static condition. 1.98 V allowed during transients.*
4. *Requires $V_{DDIOVRSEL}$ = 0.*
5. *These supplies are independent: each can be in any voltage between 0 V (off), 1.8 V, 3 V, or 3.3 V range.*
6. *Requires $V_{DDIOxVRSEL}$ = 0.*
7. *All these supplies are usually connected together.*
8. *This is the max allowed voltage. However LPLV-Stop mode is relevant only to save power, so requires voltage as low as possible (external regulator set for typical value, then the maximum voltage is few percent above the typical due to the regulator accuracy).*
9. *VDDA18PLLx must be connected together.*
10. *Can be connected to other $V_{DDA18xx}$ supplies if min/max range fulfilled.*
11. *Except when connected to V_{DD}, where the lower limit is 1.71 V.*
12. *The V08CAP pin is only to connect a decoupling capacitor for internal backup regulator. It must never be used externally for other purposes.*
13. *V_{DDxx} must be replaced for I/O respectively supplied by V_{DD}, V_{DDIO1}, V_{DDIO2}, V_{DDIO3}*

5.3.2 Operating conditions at power-up/power-down

Subject to general operating conditions.

Constraints on power supply sequences:

- $V_{DDA18AON}$ and V_{DD} must be present before any other supply (except V_{BAT}) and kept present whenever any other supply is present (except V_{BAT}). Damage could occur if not ensured.
- $V_{DDA18AON}$ and V_{DD} must ramp up and ramp down together (within a 1 ms time windows). Damage could occur if not ensured.
- $V_{DDA18USB}$ must be present whenever $V_{DD33USB}$ is present or 1 ms maximum after $V_{DD33USB}$. Damage could occur if not ensured.
- V_{DDCORE} must be present whenever $V_{DDA18USB}$ and/or $V_{DDA33USB}$ are present. If not ensured, leakage could occur on these supplies until V_{DDCORE} is present.

Table 18. Operating conditions at power-up/power-down

$V_{DDA18AON}$ and V_{DD} must be present before other supplies.

Symbol	Parameter	Operating conditions	Min	Max	Unit
$t_{VDDA18AON}$ (1)	$V_{DDA18AON}$ transitions	Rise time rate	20	1500	µs/V
		Fall time rate	20	1500	
t_{VDD} (1)	$V_{DD/VDDIOx}$ transitions	Rise time rate	20	1500	
		Fall time rate	20	1500	
$t_{VDDCORE}$	V_{DDCORE} transitions	Rise time rate	20	1500	
		Fall time rate	25	1500	

Symbol	Parameter	Operating conditions	Min	Max	Unit
t_{VDDCPU}, t_{VDDCSI}	V_{DDCPU}, V_{DDCSI} transitions	Rise time rate	10	1500	µs/V
		Fall time rate	10	1500	
t_{VDDA18}	$V_{DDA18PLL1}$, $V_{DDA18PLL2}$, $V_{DDA18CSI}$, $V_{DDA18DDR}$, $V_{DDA18USB}$, $V_{DDA18ADC}$ transitions	Rise time rate	10	1500	
		Fall time rate	10	1500	
t_{VDD33}	$V_{DD33USB}$ transitions	Rise time rate	10	1500	
		Fall time rate	10	1500	
$t_{VDDQDDR}$	V_{DDQDDR} transitions	Rise time rate	10	1500	
		Fall time rate	10	1500	
t_{VBAT}	V_{BAT} transitions	Rise time rate	20	∞	
		Fall time rate	10	1500	

1. *$V_{DDA18AON}$ and V_{DD} must be present before any other supply.*

5.3.3 Embedded reset and power control block characteristics

The parameters given in Table 19 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions.

Table 19. Embedded reset and power control block characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{RSTTEMPO}$	Reset temporization	After POR released		-	440	-	µs
$V_{DDA18AON}$ thresholds							
V_{POR_ANA}(1)	Power-on reset threshold	Rising edge		1.62	1.67	1.71	V
V_{PDR_ANA}(1)	Power-down reset threshold	Falling edge		1.58	1.63	1.67	
$V_{hyst\_POR\_ANA}$	Hysteresis voltage of POR/PDR	-		-	40	-	mV
$I_{POR\_PDR(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON		-	1.25	-	µA
V_{DD} thresholds							
V_{POR}(1)	Power-on reset threshold	Rising edge		1.62	1.67	1.71	V
V_{PDR}(1)	Power-down reset threshold	Falling edge		1.58	1.63	1.67	
V_{hyst_POR}	Hysteresis voltage of POR/PDR	-		-	40	-	mV
$I_{POR\_PDR(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON		-	0.75	-	µA
$I_{POR\_PDR(VDD)}$	Supply current on V_{DD}	Always ON	V_{DD} = 1.8 V	-	0.5	-	µA
			V_{DD} = 3.3 V	-	0.92	-	
V_{BOR0}(1)	Brown-out reset threshold 0	Rising edge		1.62	1.67	1.71	V
		Falling edge		1.58	1.63	1.67	
V_{BOR1}(1)	Brown-out reset threshold 1	Falling edge		-	-	2.97	V
V_{hyst_BOR0}	Hysteresis voltage of BOR0	-		-	40	-	mV
V_{hyst_BOR1}	Hysteresis voltage of BOR1	-		-	80	-	mV
$I_{BOR(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	BOR enabled in OTP		-	0.75	-	µA
V_{DDCPU} thresholds							
V_{RDY_VDDCPU}(1)	Threshold on rising edge	Normal modes		0.63	0.66	0.69	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RDY_VDDCPU}[1]	Threshold on rising edge	LPLV modes	0.55	0.58	0.61	V
V_{hyst_VDDCPU}	Hysteresis on falling edge	-	-	23	-	mV
T_{delay_VDDCPU}	Delay after detection	Rising edge	180	400	750	µs
		Falling edge	-	0	-	
$I_{RDY\_VDDCPU(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON	-	1.2	-	µA
V_{DDCORE} thresholds						
$V_{RDY\_VDDCORE}$[1]	Threshold on rising edge	Normal modes	0.63	0.66	0.69	V
		LPLV modes	0.55	0.58	0.61	
$V_{hyst\_VDDCORE}$	Hysteresis on falling edge	-	-	23	-	mV
$T_{delay\_VDDCORE}$	Delay after detection	Rising edge	180	400	750	µs
		Falling edge	-	0	-	
$I_{RDY\_VDDCORE(VDDA18AON)}$	Supply current on $V_{DDA18AON}$	Always ON	-	1.2	-	µA

1. *Guaranteed by test in production.*

5.3.4 Embedded reference voltage

The parameters given in Table 20 and Table 21 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Table 17. General operating conditions.

Table 20. Embedded reference voltage characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}[1]	Internal reference voltages	-40 °C < T_J < 125 °C	0.792	0.8	0.808	V
$t_{S\_VREFINT}$[2]	ADC sampling time when reading the internal reference voltage	-	34	-	-	ns
DV_{REFINT}	Internal reference voltage spread over the temperature range	-40 °C < T_J < 125 °C	-4	-	+4	mV
T_{coeff}	Average temperature coefficient	Average temperature coefficient	-	-	43	ppm/°C
$V_{DDcoeff}$	Average voltage coefficient	1.71 V < $V_{DDA18AON}$ < 1.89 V	-	-	1250	ppm/V

1. *Guaranteed by test in production.*
2. *Specified by design, not tested in production.*

Table 21. Embedded reference voltage calibration value

Symbol	Parameter	Memory address
VREFINT_CAL	Raw data acquired on ADC1 at temperature of 30 °C, $V_{DDA18ADC}$ = V_{REF+} = 1.8 V	0x4400 01B8[11:0][1][2]

1. *This is BSEC_FVR110 register which is not automatically shadowed with OTP content, so a fuse read sequence must be issued to get the register updated once (clear after reading). Refer to product reference manual - BSEC section "Operations on fuses".*
2. *Must be read in 32-bit words and relevant masking and shifting must be performed to isolate the required bits.*

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in Figure 12. Current consumption measurement scheme.

All the Run mode current consumption measurements given in this section are performed with a CoreMark code unless otherwise specified.

Supply current characteristics are evaluated by characterization, not tested in production unless otherwise specified.

5.3.5.1 Typical and maximum current consumption

The device is placed under the following conditions:

- All I/O pins are in analog input mode except when explicitly mentioned
- All peripherals are disabled except when explicitly mentioned
- RTC/LSE are disabled, unless otherwise specified
- BKPSRAM, RETRAM backup supplies in low-power modes (such as LPLV-Stop, Standby and V_{BAT} modes) are disabled, unless otherwise specified
- Unless otherwise specified, the typical values are obtained for:
  - V_{DD} / V_{DDIOx}/V_{BAT} = 3.3 V
  - V_{DDCORE} = 0.82 V
  - V_{DDCPU} = 0.80 V
  - V_{DDA18} / $V_{DDA18AON}$ = 1.8 V
    and the maximum values are obtained for:
  - V_{DD} / V_{DDIOx} / V_{BAT} = 3.6 V
  - V_{DDCORE} = 0.839 V
  - V_{DDCPU} = 0.837 V
  - V_{DDA18} / $V_{DDA18AON}$ = 1.89 V

The parameters given in Table 22 to Table 31 are derived from tests performed under supply voltage conditions summarized in Section 5.3.1: General operating conditions.

Table 22. Current consumption (I_{DDCORE}) in Run modes

Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V and V_{DDCPU} = 0.80 V, maximum values given with V_{DDCORE} = 0.839 V and V_{DDCPU} = 0.837 V.

Symbol	Parameter	Conditions							Typ	Max				Unit
		-	D1 (CPU1) mode	D2 (CPU2) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz)(1)	CPU2 clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in Run mode	All peripherals Enabled(2)	DRun (CRun)	Run1 (CRun)	HSE + HSI + PLL	1500(3)	600	300	84.5	130	210	280	390	mA
						1200	600	300	84.5	130	210	280	380	
						750	600	300	84.5	130	210	280	380	
						600	600	300	84.5	130	210	280	380	
I_{DDCORE}	Supply current in Run mode	All peripherals Enabled(2)	DRun (CRun)	Run1 (Cstop)	HSE + HSI + PLL	1500(3)	600	-	71.5	110	190	260	360	mA
						1200	600	-	71.5	110	190	260	360	
						750	600	-	71.5	110	190	260	360	
						600	600	-	71.5	110	190	260	360	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun (CRun)	Run1 (CRun)	HSE + HSI + PLL	1500(3)	600	300	73.5	110	190	270	370	mA
						1200	600	300	73.5	110	190	270	370	
						750	600	300	73.5	110	190	260	370	
						600	600	300	73.5	110	190	260	370	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun (CRun)	Run1 (Cstop)	HSE + HSI + PLL	1500(3)	600	-	40.5	61.0	140	210	320	mA
						1200	600	-	40.5	61.0	140	210	320	
						750	600	-	40.5	61.0	140	210	320	
						600	600	-	40.5	61.0	140	210	320	
						300	300	-	32.0	48.0	130	200	300	
						150	150	-	27.5	41.0	120	190	300	
					HSI	HSI 64	HSI 64	-	23.0	33.0	120	180	290	
					HSE + HSI	HSE 40	HSE 40	-	23.0	33.0	120	180	290	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CRun)	HSE + HSI + PLL	-	HSI 64	300	53.0	80.0	160	230	340	mA
						-	HSI 64	200	42.0	63.0	150	220	320	
						-	HSI 64	100	31.0	45.0	130	200	300	
					HSI	-	HSI 64	HSI 64	24.0	35.0	120	190	290	
					HSE + HSI	-	HSI 64	HSE 40	24.0	35.0	120	190	290	

Symbol	Parameter	Conditions							Typ	Max				Unit
		-	D1 (CPU1) mode	D2 (CPU2) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz)(1)	CPU2 clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStandby(4) (5) (CStandby)	Run2 (CRun)	HSE + HSI + PLL	-	HSI 64	300	47.5	80.0	160	230	340	mA
						-	HSI 64	200	36.0	63.0	150	220	320	
						-	HSI 64	100	24.5	45.0	130	200	300	
					HSI	-	HSI 64	HSI 64	17.5	35.0	120	190	290	
					HSE + HSI	-	HSI 64	HSE 40	17.5	35.0	120	190	290	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun (CSleep)	Run1 (Cstop)	HSE + HSI + PLL	1500(3)	600	-	40.0	60.0	140	210	320	mA
						1200	600	-	40.0	60.0	140	210	320	
						750	600	-	40.0	60.0	140	210	320	
						600	600	-	40.0	60.0	140	210	320	
						300	300	-	31.5	47.0	130	200	300	
						150	150	-	27.0	40.0	120	190	300	
					HSI	HSI 64	HSI 64	-	22.5	33.0	120	180	290	
					HSE + HSI	HSE 40	HSE 40	-	22.5	33.0	120	180	290	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DRun(6) (eCSleep)	Run1 (Cstop)	HSE + HSI + PLL	1500(3)	600	-	39.5	59.0	140	210	320	mA
						1200	600	-	39.5	59.0	140	210	320	
						750	600	-	39.5	59.0	140	210	320	
						600	600	-	39.5	59.0	140	210	320	
						300	300	-	31.5	46.0	130	200	300	
						150	150	-	27.0	40.0	120	190	300	
					HSI	HSI 64	HSI 64	-	22.5	33.0	120	180	290	
					HSE + HSI	HSE 40	HSE 40	-	22.5	33.0	120	180	290	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CSleep)	HSE + HSI + PLL	-	HSI 64	300	42.5	63.0	150	220	320	mA
						-	HSI 64	200	35.0	51.0	130	200	310	
						-	HSI 64	100	27.5	39.0	120	190	290	
					HSI	-	HSI 64	HSI 64	23.0	33.0	120	180	290	
					HSE + HSI	-	HSI 64	HSE 40	23.0	33.0	120	180	290	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStandby (CStandby)(4)(5)	Run2 (CSleep)	HSE + HSI + PLL	-	HSI 64	300	36.5	63.0	150	210	320	mA
						-	HSI 64	200	28.5	51.0	130	200	310	

Symbol	Parameter	Conditions							Typ	Max				Unit
		-	D1 (CPU1) mode	D2 (CPU2) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz)(1)	CPU2 clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in Run mode	All peripherals Disabled	DStandby (CStandby)(4)(5)	Run2 (CSleep)	HSE + HSI + PLL	-	HSI 64	100	21.0	39.0	120	190	290	mA
					HSI	-	HSI 64	HSI 64	16.0	32.0	120	180	290	
					HSE + HSI	-	HSI 64	HSE 40	16.0	32.0	120	180	290	

1. *ck_icn_ddr.*
2. *Activity on peripherals and bus masters other than processors, could lead to additional power consumption above these values, largely dependent on the amount of initialized peripherals and their activity.*
3. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.968 V.*
4. *CStandby = CStop and PDDS_D1 = 1.*
5. *V_{DDCPU} is shutdown.*
6. *eCSleep mean CPU1 in enhanced CSleep with PLL1 automatically stopped (RCC_C1SREQSETR.ESLPREQ=1).*

Table 23. Current consumption (I_{DDCPU}) in Run modes

Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V and V_{DDCPU} = 0.80 V, maximum values given with V_{DDCORE} = 0.839 V and V_{DDCPU} = 0.837 V.

Symbol	Parameter	Conditions							Typ	Max				Unit
		-	D1 (CPU1) mode	D2 (CPU2) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz)(1)	CPU2 clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCPU}	Supply current in Run mode	All peripherals Enabled(2)	DRun (CRun)	Run1 (CRun)	HSE + HSI + PLL	1500(3)	600	300	57.0	95.0	130	150	190	mA
						1200	600	300	40.5	65.0	90.0	120	150	
						750	600	300	27.0	43.0	68.0	89.0	130	
						600	600	300	22.5	36.0	60.0	82.0	120	
I_{DDCPU}	Supply current in Run mode	All peripherals Enabled(2)	DRun (CRun)	Run1 (Cstop)	HSE + HSI + PLL	1500(3)	600	-	57.0	95.0	130	150	190	mA
						1200	600	-	40.5	65.0	90.0	120	150	
						750	600	-	27.0	43.0	68.0	89.0	130	
						600	600	-	22.5	36.0	60.0	82.0	120	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun (CRun)	Run1 (CRun)	HSE + HSI + PLL	1500(3)	600	-	57.0	95.0	130	150	190	mA
						1200	600	-	40.5	65.0	90.0	120	150	
						750	600	-	27.0	43.0	68.0	89.0	130	
						600	600	-	22.5	36.0	60.0	82.0	120	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun (CRun)	Run1 (Cstop)	HSE + HSI + PLL	1500(3)	600	-	54.0	92.0	120	150	180	mA
						1200	600	-	38.5	62.0	87.0	110	150	
						750	600	-	24.5	41.0	66.0	86.0	120	
						600	600	-	20.5	34.0	58.0	79.0	120	
						300	300	-	12.0	20.0	44.0	65.0	96.0	
						150	150	-	7.35	13.0	36.0	57.0	88.0	
					HSI	HSI 64	HSI 64	-	3.80	6.80	31.0	51.0	82.0	
					HSE + HSI	HSE 40	HSE 40	-	3.80	6.80	31.0	51.0	82.0	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CRun)	HSE + HSI + PLL	-	HSI 64	300	2.50	4.50	28.0	49.0	80.0	mA
						-	HSI 64	200	2.50	4.50	28.0	49.0	80.0	
						-	HSI 64	100	2.50	4.50	28.0	49.0	80.0	
						-	HSI 64	HSI 64	2.50	4.50	28.0	49.0	80.0	
						-	HSI 64	HSE 40	2.50	4.50	28.0	49.0	80.0	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun (CSleep)	Run1 (Cstop)	HSE + HSI + PLL	1500(3)	600	-	16.0	27.0	53.0	75.0	110	mA

Symbol	Parameter	Conditions							Typ	Max				Unit
		-	D1 (CPU1) mode	D2 (CPU2) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz)(1)	CPU2 clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun (CSleep)	Run1 (Cstop)	HSE + HSI + PLL	1200	600	-	11.5	19.0	43.0	64.0	95.0	mA
						750	600	-	8.20	14.0	37.0	58.0	90.0	
						600	600	-	7.00	12.0	36.0	57.0	88.0	
						300	300	-	4.80	8.10	32.0	53.0	84.0	
						150	150	-	3.65	6.30	30.0	51.0	82.0	
					HSI	HSI 64	HSI 64	-	2.75	5.00	29.0	50.0	80.0	
					HSE + HSI	HSE 40	HSE 40	-	2.75	5.00	29.0	50.0	80.0	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DRun(4) (eCSleep)	Run1 (Cstop)	HSE + HSI + PLL	1500(3)	600	-	3.15	5.70	31.0	54.0	87.0	mA
						1200	600	-	2.75	5.00	29.0	50.0	81.0	
						750	600	-	2.75	5.00	29.0	50.0	81.0	
						600	600	-	2.75	5.00	29.0	50.0	81.0	
						300	300	-	2.75	5.00	29.0	50.0	81.0	
						150	150	-	2.75	5.00	29.0	50.0	81.0	
					HSI	HSI 64	HSI 64	-	2.75	5.00	29.0	50.0	81.0	
					HSE + HSI	HSE 40	HSE 40	-	2.75	5.00	29.0	50.0	81.0	
I_{DDCPU}	Supply current in Run mode	All peripherals Disabled	DStop1 (CStop)	Run1 (CSleep)	HSE + HSI + PLL	-	HSI 64	300	2.50	4.50	28.0	49.0	80.0	mA
						-	HSI 64	200	2.50	4.50	28.0	49.0	80.0	
						-	HSI 64	100	2.50	4.50	28.0	49.0	80.0	
					HSI	-	HSI 64	HSI 64	2.50	4.50	28.0	49.0	80.0	
					HSE + HSI	-	HSI 64	HSE 40	2.50	4.50	28.0	49.0	80.0	

1. *ck_icn_ddr.*
2. *Activity on peripherals and bus masters other than processors, could lead to additional power consumption above these values, largely dependent on the amount of initialized peripherals and their activity.*
3. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.968 V.*
4. *eCSleep mean CPU1 in enhanced CSleep (RCC_C1SREQSETR.ESLPREQ = 1).*

Table 24. Current consumption (I_{DD}) in Run modes

Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V and V_{DDCPU} = 0.80 V, maximum values given with V_{DDCORE} = 0.839 V and V_{DDCPU} = 0.837 V.

Symbol	Parameter	Conditions							Typ	Max				Unit
		-	D1 (CPU1) mode	D2 (CPU2) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz)(1)	CPU2 clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DD\ (3V3)}$(2)	Supply current in Run mode	All peripherals Disabled	DRun (CRun)	Run1 (CRun)	HSE + HSI + PLL	1500(3)	600	300	2.35	2.70	2.80	2.90	2.90	mA
						1200	600	300	2.35	2.70	2.80	2.90	2.90	
						750	600	300	2.35	2.70	2.80	2.90	2.90	
						600	600	300	2.35	2.70	2.80	2.90	2.90	
$I_{DD\ (1V8)}$(4)					HSE + HSI + PLL	1500(3)	600	300	1.15	1.40	1.40	1.40	1.50	mA
						1200	600	300	1.15	1.40	1.40	1.40	1.50	
						750	600	300	1.15	1.40	1.40	1.40	1.50	
						600	600	300	1.15	1.40	1.40	1.40	1.50	
$I_{DD\ (3V3)}$(2)	Supply current in Run mode	All peripherals Disabled	DRun (CRun)	Run1 (CStop)	HSI	HSI 64	HSI 64	-	2.35	2.70	2.80	2.90	2.90	mA
					HSE + HSI	HSE 40	HSE 40	-	2.35	2.70	2.80	2.90	2.90	
$I_{DD\ (1V8)}$(4)					HSI	HSI 64	HSI 64	-	1.15	1.40	1.40	1.40	1.50	mA
					HSE + HSI	HSE 40	HSE 40	-	1.15	1.40	1.40	1.40	1.50	
$I_{DD\ (3V3)}$(2)	Supply current in Run mode	All peripherals Disabled	DStandby(5) (6) (CStandby)	Run2 (CRun)	HSI	-	HSI 64	HSI 64	2.25	2.60	2.70	2.70	2.80	mA
$I_{DD\ (1V8)}$(4)					HSI	-	HSI 64	HSI 64	2.25	2.60	2.70	2.70	2.80	mA

1. *ck_icn_ddr.*
2. *Typical value given with V_{DD} = 3.3 V, maximum value given with V_{DD} = 3.6 V.*
3. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.968 V.*
4. *Typical value given with V_{DD} = 1.8 V, maximum value given with V_{DD} = 1.89 V.*
5. *CStandby = CStop and PDDS_D1 = 1.*
6. *V_{DDCPU} is shutdown.*

Table 25. Current consumption (I_{DDA18}) in Run modes

Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V and V_{DDCPU} = 0.80 V, maximum values given with V_{DDCORE} = 0.839 V and V_{DDCPU} = 0.837 V.

Symbol	Parameter	Conditions							Typ	Max				Unit
		-	D1 (CPU1) mode	D2 (CPU2) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz)(1)	CPU2 clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDA18}	Supply current in Run mode	All peripherals Disabled	DRun (CRun)	Run1 (CRun)	HSE + HSI + PLL	1500(2)	600	300	2.20	3.30	3.30	3.30	3.40	mA
						1200	600	300	1.90	2.80	2.80	2.80	2.90	
						750	600	300	1.50	2.20	2.20	2.20	2.20	
						600	600	300	1.35	2.00	2.00	2.00	2.00	
I_{DDA18}	Supply current in Run mode	All peripherals Disabled	DRun (CRun)	Run1 (CStop)	HSI	HSI 64	HSI 64	-	59.0	84.0	120	130	150	µA
					HSE + HSI	HSE 40	HSE 40	-	59.0	84.0	120	130	150	
I_{DDA18}	Supply current in Run mode	All peripherals Disabled	DStandby(3) (4) (CStandby)	Run2 (CRun)	HSI	-	HSI 64	HSI 64	170	220	250	260	290	µA

1. *ck_icn_ddr.*
2. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.968 V.*
3. *CStandby = CStop and PDDS_D1 = 1.*
4. *V_{DDCPU} is shutdown.*

Table 26. Current consumption ($I_{DDA18AON}$) in Run modes

Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V and V_{DDCPU} = 0.80 V, maximum values given with V_{DDCORE} = 0.839 V and V_{DDCPU} = 0.837 V.

Symbol	Parameter	Conditions							Typ	Max				Unit
		-	D1 (CPU1) mode	D2 (CPU2) mode	Osc.	CPU1 clk (MHz)	AXI clk (MHz)(1)	CPU2 clk (MHz)	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DRun (CRun)	Run1 (CRun)	HSE + HSI + PLL	1500(2)	600	300	3.15	5.30	4.80	4.70	4.60	mA
						1200	600	300	3.15	5.30	4.80	4.70	4.60	
						750	600	300	3.15	5.30	4.80	4.60	4.60	
						600	600	300	3.15	5.30	4.80	4.70	4.60	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DRun (CRun)	Run1 (CRun)	HSE + HSI + PLL	1500(2)	600	300	3.15	5.30	4.80	4.70	4.60	mA
						1200	600	300	3.15	5.30	4.80	4.70	4.60	
						750	600	300	3.15	5.30	4.80	4.70	4.60	
						600	600	300	3.15	5.30	4.80	4.70	4.60	
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DRun (CRun)	Run1 (CStop)	HSI	HSI 64	HSI 64	-	445	510	540	550	570	µA
					HSE + HSI	HSE 40	HSE 40	-	3.15	5.30	4.80	4.70	4.60	mA
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DRun (CRun)	Run1 (CStop)	HSI	HSI 64	HSI 64	-	445	510	540	550	570	µA
					HSE + HSI	HSE 40	HSE 40	-	3.15	5.30	4.80	4.70	4.60	mA
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 1.8 V)	All peripherals Disabled	DStandby(3) (4) (CStandby)	Run2 (CRun)	HSI	-	HSI 64	HSI 64	445	510	540	550	570	µA
$I_{DDA18AON}$	Supply current in Run mode (V_{DD} = 3.3 V)	All peripherals Disabled	DStandby (CStandby)(3)(4)	Run2 (CRun)	HSI	-	HSI 64	HSI 64	445	510	540	550	570	µA

1. *ck_icn_ddr.*
2. *Typical value given with V_{DDCPU} = 0.91 V, maximum values given with V_{DDCPU} = 0.968 V.*
3. *CStandby = CStop and PDDS_D1 = 1.*
4. *V_{DDCPU} is shutdown.*

Table 27. Current consumption (I_{BAT}) in Run modes

V_{SW} supplied by V_{DD}.

Symbol	Parameter	Conditions	Typ	Max				Unit
		V_{BAT} voltage	T_J = 25 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{BAT}	Supply current in Run mode (V_{DD} = 1.8 V)	V_{BAT} = 3.0 V	7.65	TBD	TBD	TBD	TBD	µA
		V_{BAT} = 3.3 V	10.5	12.0	23.0	32.0	TBD	
I_{BAT}	Supply current in Run mode (V_{DD}= 3.3 V)	V_{BAT} = 3.0 V	4.90	TBD	TBD	TBD	TBD	µA
		V_{BAT} = 3.3 V	5.70	6.30	5.80	4.80	3.10	

Table 28. Current consumption in Stop modes

Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V and V_{DDCPU} = 0.80 V, maximum values given with V_{DDCORE} = 0.839 V and V_{DDCPU} = 0.837 V

Symbol	Parameter	Conditions			Typ				Max				Unit
		D1 (CPU1) mode	D2 (CPU2) mode	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in Stop1 mode	DStop1 (CStop)	Stop1 (CStop)	-	5.60	53.8	82.0	135	14.0	82.0	150	230	mA
I_{DDCPU}					1.80	14.5	25.0	42.0	4.50	28.0	49.0	79.0	mA
I_{DD}				V_{DD} = 3.3 V(1)	2.35	2.35	2.40	2.45	3.10	TBD	TBD	TBD	mA
				V_{DD} = 1.8 V(2)	1.15	1.150	1.15	1.20	1.30	1.40	1.40	1.50	mA
I_{DDA18}				-	64.0	82.0	93.0	105	96.0	130	140	170	µA
$I_{DDA18AON}$				V_{DD} = 3.3 (1)	45.0	TBD	TBD	TBD	58.0	78.0	87.0	100	µA
				V_{DD} = 1.8 V(2)	47.0	TBD	TBD	TBD	60.0	79.0	89.0	110	µA
I_{DDCORE}	Supply current in Stop2 mode	DStandby(3) (4) (CStandby)	Stop2 (CStop)	-	5.50	45.5	75.5	130	17.0	82.0	150	230	mA
I_{DDCPU}					-(5)								-
I_{DD}				V_{DD} = 3.3 V(1)	2.25	2.25	2.30	2.35	3.10	TBD	TBD	TBD	mA
				V_{DD} = 1.8 V(2)	1.05	1.05	1.05	1.05	1.10	1.30	1.30	1.30	mA
I_{DDA18}				-	180	200	210	220	230	260	270	300	µA
$I_{DDA18AON}$				V_{DD} = 3.3 V(1)	44.0	TBD	TBD	TBD	61.0	76.0	89.0	100	µA
				V_{DD} = 1.8 V(2)	46.0	TBD	TBD	TBD	63.0	81.0	94.0	110	µA

1. *typical values given for V_{DD} = 3.3 V, maximum values for V_{DD} = 3.6 V.*
2. *typical values given for V_{DD} = 1.8 V, maximum values for V_{DD} = 1.89 V.*
3. *CStandby = CStop and PDDS_D1 = 1.*
4. *V_{DDCPU} is shutdown.*
5. *Supply is OFF.*

Table 29. Current consumption in LPLV-Stop modes

Except otherwise noted, typical values given with V_{DDCORE} = 0.82 V and V_{DDCPU} = 0.80 V, maximum values given with V_{DDCORE} = 0.839 V and V_{DDCPU} = 0.837 V.

Symbol	Parameter	Conditions			Typ				Max				Unit
		D1 (CPU1) mode	D2 (CPU2) mode	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DDCORE}	Supply current in LPLV-Stop1 mode	DStop3[1] (CStop)	LPLV-Stop1[1] (CStop)	-	5.50	47.0	79.5	135	15.0	94.0	160	270	mA
I_{DDCPU}					2.20	13.5	23.5	40.0	4.50	29.0	49.0	80.0	mA
I_{DD}				V_{DD} = 3.3 V[2]	2.35	3.05	3.75	5.00	3.10	TBD	TBD	TBD	mA
				V_{DD} = 1.8 V[3]	1.15	1.85	2.50	3.75	1.60	3.50	5.30	8.30	mA
I_{DDA18}				-	-[5]								-
$I_{DDA18AON}$				V_{DD} = 3.3 V[2]	TBD	TBD	TBD	TBD	57.0	77.0	86.0	100	µA
				V_{DD} = 1.8 V[3]	TBD	TBD	TBD	TBD	59.0	79.0	88.0	110	µA
I_{DDCORE}	Supply current in LPLV-Stop2 mode	DStandby (CStandby)	LPLV-Stop2[1] (CStop)	-	5.40	42.0	74.0	130	15.0	93.0	160	260	mA
I_{DDCPU}					-[5]								-
I_{DD}				V_{DD} = 3.3 V[2]	2.25	3.00	3.700	4.95	3.00	TBD	TBD	TBD	mA
				V_{DD} = 1.8 V[3]	1.10	1.75	2.45	3.65	1.50	3.50	5.30	8.30	mA
I_{DDA18}				-	-[5]								-
$I_{DDA18AON}$				V_{DD} = 3.3 V[2]	TBD	TBD	TBD	TBD	57.0	78.0	87.0	100	µA
				V_{DD} = 1.8 V[3]	TBD	TBD	TBD	TBD	59.0	79.0	89.0	110	µA

1. *Typical value given with V_{DDCORE} = 0.67 V, maximum values given with V_{DDCORE} = 0.71 V.*
2. *Typical values given for V_{DD} = 3.3 V, maximum values for V_{DD} = 3.6 V.*
3. *Typical values given for V_{DD} = 1.8 V, maximum values for V_{DD} = 1.89 V.*
4. *CStandby = CStop and PDDS_D1 = 1.*
5. *Supply is OFF.*

Table 30. Current consumption in Standby mode

Evaluated by characterization, not tested in production unless otherwise specified.
V_{DDCORE} and V_{DDCPU} are shutdown.

Symbol	Parameter	Conditions				Typ				Max				Unit
		RTC/LSE	BKPSRAM	RETRAM	V_{DD} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{DD}	Supply current in Standby mode	OFF	OFF	OFF	V_{DD} = 3.3 V(1)	2.05	2.35	2.70	3.25	2.60	3.00	3.40	4.00	mA
		RTC ON, LSE ON(2)				2.05	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
			ON			2.05	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
			OFF	ON		2.05	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
			ON	ON		2.05	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
	Supply current in Standby mode	OFF	OFF	OFF	V_{DD} = 1.8 V(3)	0.92	1.20	1.50	2.05	1.10	1.50	1.90	2.40	mA
		RTC ON, LSE ON(2)				0.92	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
			ON			0.92	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
			OFF	ON		0.92	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
			ON	ON		0.92	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
$I_{DDA18AON}$	Supply current in Standby mode	OFF	OFF	OFF	V_{DD} = 3.3 V(1)	44.0	57.0	64.0	72.5	57.0	75.0	85.0	98.0	mA
					V_{DD} = 1.8 V(3)	45.5	58.5	65.5	74.0	59.0	77.0	87.0	99.0	mA
		RTC ON, LSE ON(2)	ON	ON	V_{DD} = 3.3 V(1)	44.0	57.0	64.0	72.5	57.0	75.0	85.0	98.0	mA
					V_{DD} = 1.8 V(3)	45.5	58.5	65.5	74.0	59.0	77.0	87.0	99.0	mA

1. *Typical values given for V_{DD} = 3.3 V, maximum values for V_{DD} = 3.6 V.*
2. *LSE is set to medium-high drive.*
3. *typical values given for V_{DD} = 1.8 V, maximum values for V_{DD} = 1.89 V.*

Table 31. **Current consumption in V_{BAT} mode**

Symbol	Parameter	Conditions				Typ				Max				Unit
		RTC/LSE	BKPSRAM	RETRAM	V_{BAT} voltage	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 125 °C	
I_{BAT}	Supply current in V_{BAT} mode	OFF	OFF	OFF	V_{BAT} = 1.8 V	10.0	15.0	16.0	19.0	12.0	17.0	19.0	85.0	µA
		RTC ON, LSE ON(1)	OFF	OFF		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON			TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			OFF	ON		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON	ON		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{BAT}	Supply current in V_{BAT} mode	OFF	OFF	OFF	V_{BAT} = 2.4 V	12.5	17.5	18.5	20.5	14.0	20.0	22.0	84.0	µA
		RTC ON, LSE ON(1)	OFF	OFF		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON			TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			OFF	ON		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON	ON		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{BAT}	Supply current in V_{BAT} mode	OFF	OFF	OFF	V_{BAT} = 3.0 V	16.0	21.5	23.5	26.5	18.0	25.0	27.0	90.0	µA
		RTC ON, LSE ON(1)	OFF	OFF		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON			TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			OFF	ON		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON	ON		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{BAT}	Supply current in V_{BAT} mode	OFF	OFF	OFF	V_{BAT} = 3.3 V	25.5	38.0	47.5	61.0	27.0	42.0	53.0	130	µA
		RTC ON, LSE ON(1)	OFF	OFF		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON			TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			OFF	ON		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON	ON		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
I_{BAT}	Supply current in V_{BAT} mode	OFF	OFF	OFF	V_{BAT} = 3.6 V	33.3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
		RTC ON, LSE ON(1)	OFF	OFF		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON			TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			OFF	ON		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA
			ON	ON		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	µA

1. *LSE is set to medium-high drive.*

5.3.5.2 I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

5.3.5.3 I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in Table 55. I/O static characteristics.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which must be configured as analog inputs.

Caution: *Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.*

5.3.5.4 I/O dynamic current consumption

The I/Os used by an application contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin.

The theoretical formula is provided below:

$$I_{SW} = V_{DD} \times f_{SW} \times C_L$$

where

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DDx} is the MCU supply voltage
- f_{SW} is the I/O switching frequency
- C_L is the total capacitance seen by the I/O pin: C = CINT + CEXT

5.3.6 Wake-up time from low-power modes

The wake-up times given in Table 32 and Table 33 are measured starting from the wake-up event trigger up to the first instruction executed by the CPU1 or CPU2:

- the CPU1 or CPU2 goes in low-power mode after WFI (wait for interrupt) instruction.
- For CSleep modes:
  - Interrupt to GIC or NVIC is used to wake-up from low-power modes.
- For CStop modes (except Standby and V_{BAT}):
  - For CPU1 and CPU2: EXTI1[x] is used to wake-up from low-power modes.
- For Standby modes:
  - WKUPx is used to wake-up from low-power modes.
- For V_{BAT} modes
  - TAMP_INx is used to wake-up from low-power modes.
- System mode is equal to D2 domain mode

All timings are derived from tests performed under ambient temperature and V_{DD} = 3.3 V.

General conditions unless otherwise noted:

- CPU1 software in SYSRAM
- CPU2 software in SRAMx
- HSE is 40 MHz
- When HSI is used, HSIKERON = 0
- PWRLP_DLY = 0

- LPLVDLY_D2 = 187 µs
- $t_{WUCSleep}$ values are measured with internal interrupt
- $t_{WUCStop}$ and $t_{WULPLV-Stop}$ values are measured with EXTI pin
- $t_{WUStandby}$ values are measured with WKUP pin through PWR
- When V_{DDCORE} or V_{DDCPU} is shutdown or reduced, the wake-up time value depends on the supply characteristics.
  - Wake-up time in the following tables is measured with a 200 µs V_{DDCORE} and V_{DDCPU} setup time
  - V_{DDCPU} or V_{DDCORE} startup time longer than 200 µs must be added to the wake-up time value
  - When voltage is reduced, V_{DDCORE} is assumed to be back to nominal value before LPLVDLY_D2 expiration. Otherwise, LPLVDLY_D2 value must be increased accordingly and this directly impact wake-up time value.

Table 32. D1 (CPU1) low-power mode wake-up timings

Evaluated by characterization, not tested in production. Unless otherwise noted.

Symbol	D1 (CPU1) mode	D2 (CPU2) mode	Conditions for wake-up domain	Typ	Max	Unit
$t_{WUCSleep\_CPU1}$	DRun (CSleep)	Run1 (CStop)	SEV between CPU1 cores	-	15	CPU1 clock cycles
			HSI	-	12 + 20	$T_{ck\_icn\_nic}$ + $T_{ck\_cpu1\_ext2f}$
			HSE + PLL1	-	12 + 20	$T_{ck\_icn\_nic}$ + T_{PLL1}
	DRun (eCSleep) (1)	Run1 (CStop)	HSE + PLL1	-	12 + 20	$T_{ck\_icn\_nic}$ + $T_{ck\_cpu1\_ext2f}$
$t_{WUCStop\_CPU1}$	DStop1 (CStop)	Run1 (CRun)	HSI 64 MHz	8	10	µs
			HSE + PLL1 1200 MHz	180	-	µs
	DStop1 (CStop) (2)	Stop1 (CStop) (2)	HSI 64 MHz(3)	4	15	µs
			HSI 64 MHz	8	10	µs
			HSE + PLL1 1200 MHz	180	-	µs
	DStandby (CStop)(4)	Stop2 (CStop) (2)	HSI 64 MHz(3)(5)	660	-	µs
$t_{WULPLV-Stop\_CPU1}$	DStop3 (CStop) (2)(6)	LPLV-Stop1 (CStop)(2)(6)	HSI 64 MHz, PWRLP_DLY = 100 µs	1000	1200	µs
	DStandby (CStop)(4)(6)	LPLV-Stop2 (CStop)(2)(6)	HSI 64 MHz(5)	1500 (1000)	-	µs(7)

1. *eCSleep mean CPU1 in enhanced CSleep with PLL1 automatically stopped (RCC_C1SREQSETR.ESLPREQ = 1). In this mode, CPU1 wake on ck_cpu1_ext2f, then CPU1 switch back automatically to PLL1 after PLL lock time.*
2. *PDDS_Dx = 0.*
3. *HSI active (HSIKERON = 1).*
4. *PDDS_Dx = 1.*
5. *CPU1 wake-up address register points to SYSRAM code.*
6. *LPDS_Dx=1 and LVDS_Dx = 1.*
7. *Value in parenthesis is for wake-up using WKUP pin through PWR.*

Table 33. D2 (CPU2) low-power mode wake-up timings

Evaluated by characterization, not tested in production. Unless otherwise noted.

Symbol	D1 (CPU1) mode	D2 (CPU2) mode	Conditions for wake-up domain	Typ	Max	Unit
$t_{WUCSleep\_CPU2}$(1)	DStop1 (CStop)	Run1 (CSleep)	-	-	14	CPU2 clock cycles

Symbol	D1 (CPU1) mode	D2 (CPU2) mode	Conditions for wake-up domain	Typ	Max	Unit
$t_{WUCStop\_CPU2}$	DRun (CRun)	Run1 (CStop)	HSI 64 MHz	-	1.3	µs
			HSE + PLL 300 MHz	180	-	µs
	DStop1 (CStop)(2)	Stop1 (CStop)(2)	HSI 64 MHz(3)	3	6.5	µs
			HSI 64 MHz	4.6	-	µs
			HSE + PLL 300 MHz	180	-	µs
$t_{WULPLV-Stop\_CPU2}$	DStop3 (CStop)(2)(4)	LPLV-Stop1 (CStop)(2)(4)	HSI 64 MHz(5)	900	1100	µs
			HSI 64 MHz(6)	1.1	1.3	ms
	DStandby (CStop)(4)(7)	LPLV-Stop2 (CStop)(2)(4)	(Reset) HSI 64 MHz	1500 (900)	-	µs(8)
$t_{WUStandby\_CPU2}$	DStandby (CStop)(9)	Standby2 (CStop)(9)	HSI 64 MHz, RETRAM	1700 (800)	-	ms

1. *Specified by design, not tested in production.*
2. *PDDS_Dx = 0.*
3. *HSI active (HSIKERON = 1).*
4. *LPDS_Dx = 1 and LVDS_Dx = 1.*
5. *CPU2TMPSKP = 1 or PWRLP_DLY = 0.*
6. *CPU2TMPSKP = 0 and PWRLP_DLY = 100 µs.*
7. *PDDS_Dx = 1*
8. *Value in parenthesis is for wake-up using WKUP pin through PWR or wake-up using EXTI without simultaneous CPU1 wake-up.*
9. *PDDS_Dx = 1.*

Table 34. Wake-up time using USART/LPUART

Specified by design, not tested in production.

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUUSART}$ $t_{WULPUART}$	Wake-up time needed to calculate the maximum USART/ LPUART baud rate allowing the wake-up from low-power mode	Stop1/2 HSI clock with HSIKERON = 0	-	6.4	µs
$t_{WULPUART\_LPLV}$	Wake-up time needed to calculate the maximum LPUART baud rate allowing the wake-up from low-power mode	LPLV-Stop1/2 MSI clock with MSIKERON = 0	-	580	µs

5.3.7 External clock source characteristics

5.3.7.1 *High-speed external user clock generated from an external source*

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

Digital and analog bypass modes are available.

The external clock signal must respect the Table 1. However, the recommended clock input waveform is shown in Figure 13 for digital bypass mode and in Figure 14 for analog bypass mode. In analog bypass mode the clock can be a sinusoidal waveform.

Table 35. High-speed external (HSE) user clock characteristics (digital bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	-	16	40	48	MHz
V_{HSEH}	OSC_IN input pin high level voltage	-	-	0.7 × $V_{DDA18AON}$	-	$V_{DDA18AON}$	V
V_{HSEL}	OSC_IN input pin low level voltage	-	-	V_{SS}	-	0.3 × $V_{DDA18AON}$	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{W(HSE)}$	OSC_IN high or low time	-	-	7	-	-	ns

Figure 13. High-speed external clock source AC timing diagram (digital bypass)

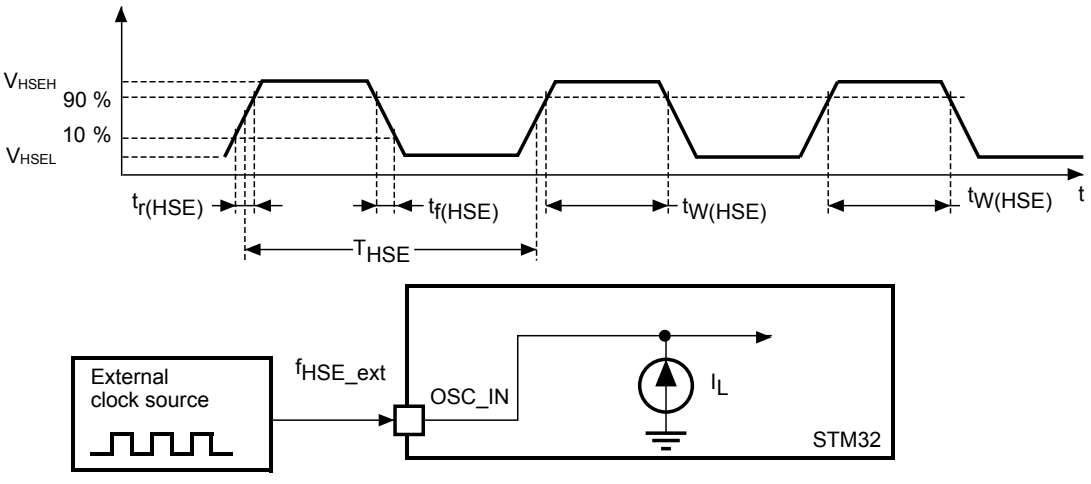


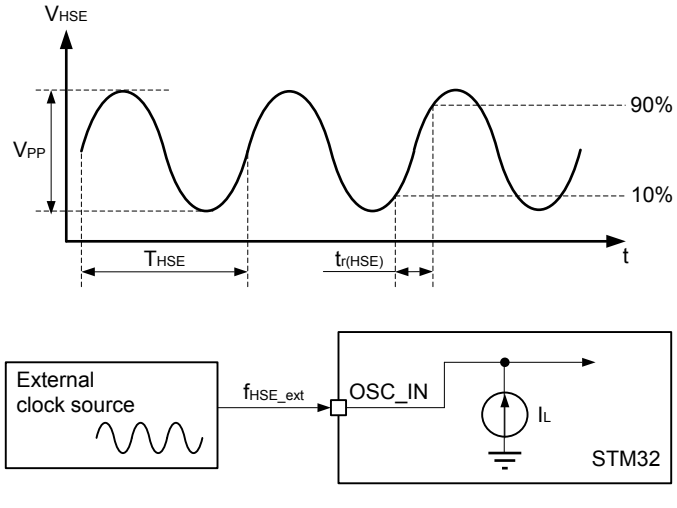
Table 36. High-speed external (HSE) user clock characteristics (analog bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	16	40	48	MHz
	duty cycle (Square wave)	-	45	50	55	%
	duty cycle deterioration(1)	-	-	± 10(2)	±30(3)	%
V_{HSE}	Absolute input range	-	0	-	$V_{DDA18AON}$	V
V_{PP}	OSC_IN peak-to-peak amplitude	-	0.2(4)	-	0.67 × $V_{DD18AON}$	
$t_{SU(HSE)}$	Time to start(5)	-	-	1	10(6)	µs
$tr/tf_{(HSE)}$	Rise and Fall time (10% to 90% threshold levels of the input peak-to-peak amplitude)	-	0.05 × T_{HSE}	-	0.3 × T_{HSE}	ns

1. *Specified by design, not tested in production.*
2. *With a square wave signal (at 25 °C, $V_{DDA18AON}$ = 1.8 V / VPP = 400 mV / VDC = 0.8 V) where VDC is the DC component of the input signal.*
3. *With a square wave signal (at 25 °C, $V_{DDA18AON}$ = 1.71 V / VPP = 200 mV / VDC = 0.8 V) where VDC is the DC component of the input signal.*
4. *Minimum peak-to-peak amplitude (at 25 °C, 0.1 < VDC < $V_{DDA18AON}$ - 0.1 V) where VDC is the DC component of the input signal.*
5. *Startup time measured from the moment it is enabled (by software) to a stabilized analog bypass clock interface is reached.*
6. *Maximum start-up time is obtained with 200 mV peak-to-peak amplitude.*

Figure 14. High-speed external clock source AC timing diagram (analog bypass)



5.3.7.2 *Low-speed external user clock generated from an external source*

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal must respect the Table 1. However, the recommended clock input waveform is shown in Figure 15 for digital bypass and Figure 16 for analog bypass.

Table 37. Low-speed external (LSE) user clock characteristics (digital bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}(1)	User external clock source frequency	-	-	32.768	-	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.75 × V_{SW}	-	V_{SW}(2)	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.25 × V_{SW}	
$t_{W(LSE)}$	OSC32_IN high or low time	-	250	-	-	ns

1. *Specified by design, not tested in production.*
2. *V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*

Figure 15. Low-speed external clock source AC timing diagram (digital bypass)

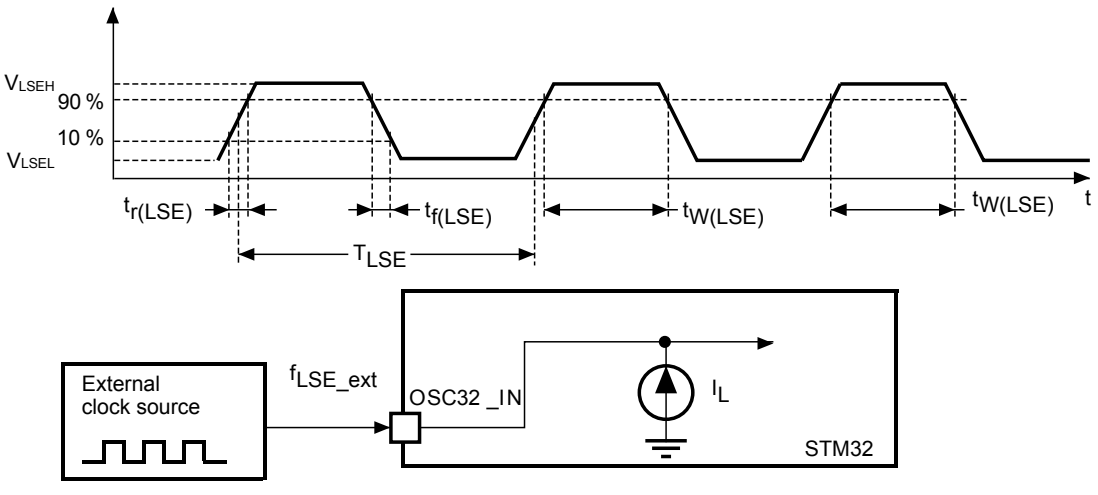


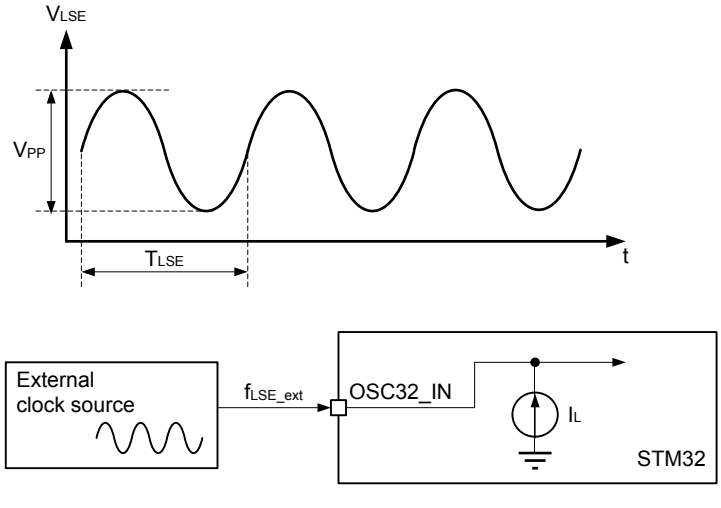
Table 38. Low-speed external (LSE) user clock characteristics (analog bypass)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}(1)	User external clock source frequency	-	-	32.768	-	kHz
V_{LSE}	Absolute input range	-	0	-	V_{SW}(2)	V
V_{PP}	OSC32_IN peak-to-peak amplitude	-	0.2(3)	1	-	

1. *Specified by design, not tested in production.*
2. *V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*
3. *Minimum peak-to-peak amplitude (at 25 °C, 0.1 < VDC < V_{SW} - 0.1 V) where VDC is the DC component of the input signal.*

Figure 16. Low-speed external clock source AC timing diagram (analog bypass)



5.3.7.3 *High-speed external clock generated from a crystal/ceramic resonator*

The high-speed external (HSE) clock can be supplied with a 16 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 39. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 39. High-speed external (HSE) oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}(1)	Crystal frequency	-	16	40	48	MHz
R_F(1)	Internal feedback equivalent resistor	-	-	250	-	kΩ
$I_{VDDA18AON(HSE)}$	HSE current consumption on $V_{DDA18AON}$	During startup	-	-	10	mA
		Rm = 80 Ω, CL = 6 pF at 40 MHz(3)	-	4.6	-	
$Gm_{critmax}$(1)	Maximum critical crystal gm	Startup	-	-	1.95	mA/V
t_{SU}	Start-up time(4)	-	-	2	-	ms

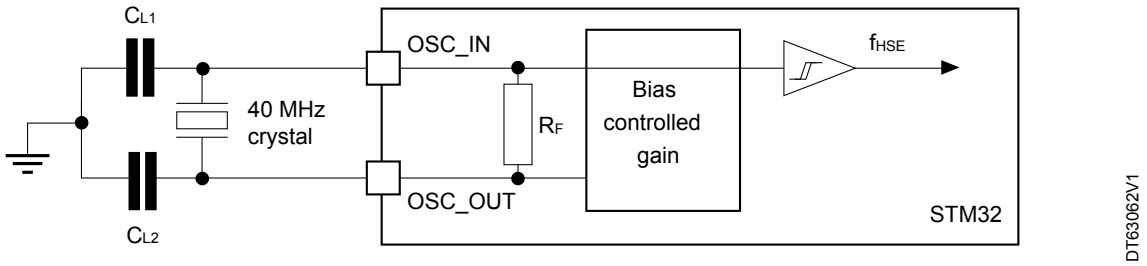
1. *Specified by design, not tested in production.*
2. *This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.*
3. *Resonator characteristics given by the crystal/ceramic resonator manufacturer.*

4. *Measured from the moment it is enabled (by software) to a stabilized 40 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 17). The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. The PCB and pin capacitance must be included (4 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

Figure 17. Typical application with a 40 MHz crystal



5.3.7.4 *Low-speed external clock generated from a crystal/ceramic resonator*

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Section 5.3.7.4. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. Low-speed external (LSE) oscillator characteristics

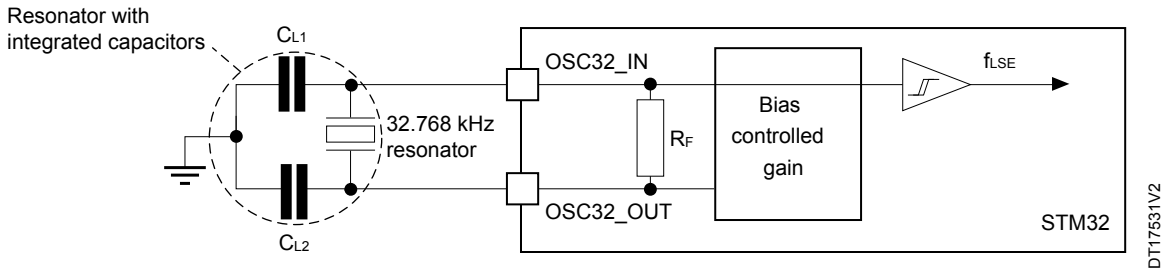
Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}(1)	Oscillator frequency	-	-	32.768	-	kHz
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00, Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 10, Medium Low drive capability	-	-	0.75	
		LSEDRV[1:0] = 01, Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11, High drive capability	-	-	2.7	
t_{SU}(2)	Startup time	V_{SW} is stabilized	-	2	-	s

1. *Specified by design, not tested in production.*
2. *t_{SU} is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs" available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



1. *Adding an external resistor between OSC32_IN and OSC32_OUT is forbidden.*

5.3.8 External clock source security characteristics

Table 41. High-speed external user clock security system (HSE CSS)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DCM(HSE\_CSS)}$	Time to detect clock missing	f_{HSE} = 48 MHz	-	1	2	µs

Table 42. Low-speed external user clock security system (LSE CSS)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{DCM(LSE\_CSS)}$	Time to detect clock missing	-	-	-	300	µs
$f_{MAX(LSE\_CSS)}$	Cut-off frequency	-	-	-	2	MHz

5.3.9 Internal clock source characteristics

The parameters given in Table 43 and Table 45 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions.

5.3.9.1 64 MHz high-speed internal RC oscillator (HSI)

Table 43. HSI oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}(1)	HSI frequency	$V_{DDA18AON}$ = 1.8 V, T_J = 30 °C	63.68	64	64.32	MHz
TRIM	HSI trimming step	-	-	0.25	0.5	%
DuCy(HSI)	Duty Cycle	-	40	-	60	%
$\Delta V_{DDA18AON(HSI)}$ + ΔT_J(HSI)	HSI oscillator frequency drift over voltage and temperature variation (after factory calibration)(2)	T_J = -40 to 125 °C	-8.5	-	+8.5	%
$t_{su(HSI)}$	HSI oscillator start-up time (Time between Enable rising and First output clock edge.)	-	-	-	3	µs
$t_{stab(HSI)}$	HSI oscillator stabilization time	At 1% of target frequency	-	-	5	µs
$I_{VDDCORE(HSI)}$	HSI supply current on V_{DDCORE}	-	-	-	10	µA
$I_{VDD18AON(HSI)}$	HSI supply current on $V_{DDA18AON}$	-	-	300	400	µA

1. *Guaranteed by test in production.*

2. *If better tolerance is required (for example, for UART kernel clock usage), the HSI can be trimmed during runtime by measuring its frequency with a better reference, such as the HSE crystal. The HSI trimming must be performed regularly or whenever there is a significant variation in supply voltage or temperature.*

5.3.9.2 4/16 MHz low-power internal RC oscillator (MSI)

Table 44. MSI oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{MSI}	CSI frequency	V_{DDCORE} = 0.82 V, T_J = 30 °C	MSIFREQSEL=0(1)	3.956	4	4.044	MHz
			MSIFREQSEL=1	15.824	16	16.176	
TRIM	MSI trimming step	Trimming Code is not a multiple of 32		-	0.8	1.1	%
		Trimming Code is a multiple of 32		-	-2.5	-3.8	
DuCy(MSI)	Duty Cycle	At trimmed frequency		45	-	55	%
ΔT_J(MSI)	MSI oscillator frequency drift over temperature	T_J = -40 °C to 70 °C		-5	-	+5	%
		T_J = -40 °C to 125 °C		-6	-	+6	
$t_{su(MSI)}$	MSI oscillator start-up time	-		-	-	3.5	µs
$I_{VDDCORE(MSI)}$	MSI Supply current on V_{DDCORE}	at 4 MHz	MSIFREQSEL = 0	-	20	22	µA
		at 16 MHz	MSIFREQSEL = 1	-	60	68	

1. *Guaranteed by test in production.*

5.3.9.3 32 kHz low-speed internal (LSI) RC oscillator

Table 45. LSI oscillator characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	T_J = 30 °C(1)	30.5	32	33.5	kHz
		T_J= -40 to 125° C	28.8	32	33.6	
$t_{su(LSI)}$	LSI oscillator start-up time (time between enable rising and first output clock edge.)	-	-	-	180	µs
$I_{VSW(LSI)}$	LSI supply current on V_{SW}(2)	-	-	250	500	nA

1. *Guaranteed by test in production.*
2. *V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*

5.3.10 PLL characteristics

The parameters given in Table 46 and Table 47 are derived from tests performed under temperature and supply voltage conditions summarized in Table 17. General operating conditions.

Table 46. PLL1 to PLL7 characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Normal mode	5	-	64	MHz
		Sigma delta mode	10	-	64	
f_{PFD}	PFD input clock	Normal mode	5	f_{PLL_IN}/ FREFDIV	50	MHz
		Sigma delta mode	10	-	min(50, f_{VCO}/20)	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{FOUTPOSTDIV}$	Divided output clock	-		16.32	-	3200	MHz
	Divided output clock duty cycle	Division by 1		48	50	52	%
		Even Division		48	50	52	
		Odd Division		47	50	53	
f_{VCO}	PLL VCO output	-		800	-	3200	MHz
t_{LOCK}	PLL lock time	Frequency lock		-	-	400	$1/f_{PFD}$ cycles
		f_{PFD} = 40 MHz (f_{PLL_IN} = 40 MHz, FREFDIV = 1)		-	-	10	µs
Jitter	RMS period jitter	f_{VCO} = 3200 MHz		-	-	0.26	+/_ps
	RMS integrated jitter (10 kHz - 20 MHz)	f_{VCO} = 3200 MHz, F_{PFD} = 25 MHz	Integer divider	-	±2.7	±6.6	ps
			fracN divider	-	-	±11.9	
$I_{VDDA18PLL}$ [1]	PLL supply current on $V_{DDA18PLL}$ (Analog)	f_{VCO} = 3200 MHz	FBDIV < 256	-	5750	6850	µA
			FBDIV > 255	-	7050	8450	
		f_{VCO} = 800 MHz	FBDIV < 256	-	715	860	
$I_{VDDCORE(PLL)}$ [1]	PLL supply current on V_{DDCORE} (Digital)	f_{VCO} = 3200 MHz	V_{DDCORE} = 0.82 V	-	1200	3650	
		f_{VCO} = 800 MHz		-	295	910	

1. *Evaluated by characterization, not tested in production.*

Table 47. PLL_USB characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	Only those 3 values (min, typ or max) are possible	19.2	20	38.4	MHz
f_{PLL_OUT}	PLL output clock	-	-	480	-	MHz

5.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows the reduction of electromagnetic interferences (see Section 5.3.13.4: Electromagnetic Interference (EMI)). It is available only on the PLL2 to PLL7.

Table 48. PLL2 to PLL7 SSCG parameters constraints

Specified by design, not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
F_{MOD}	Modulation frequency	5.2	-	391	kHz
M_D	Peak modulation depth	0.1	-	3.1	%

5.3.12 Memory characteristics

5.3.12.1 OTP characteristics

The characteristics are given at T_J = -40 to 125 °C unless otherwise specified.

Table 49. OTP characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{OTP(VDDA18AON)}$	OTP supply current on $V_{DDA18AON}$	Programming	-	3.8	10	mA
		Reading	-	0.66	1.13	
		PowerDown	-	5	132	µA
$I_{OTP(VDDCORE)}$	OTP supply current on V_{DDCORE}	Programming	-	0.09	0.45	mA
		Reading	-	1.8	3.6	
		PowerDown	-	8	500	µA

5.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

5.3.13.1 *Functional EMS (electromagnetic susceptibility)*

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: a burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in Table 50. They are based on the EMS levels and classes defined in application note AN1709 available from the ST website www.st.com.

Table 50. EMS characteristics

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, TA = +25 °C, VFBGA273 package, F_{PLL1} = 1200 or 1500 MHz, $F_{ck\_icn\_hs\_mcu}$ = 300 MHz, Cortex-M33 cores not running, conforms to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to be applied through 100 pF on VDD and VSS pins to induce a functional disturbance		5A

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the device pins exposed to noise (connected to tracks longer than 50 mm on PCB).

5.3.13.2 *Designing hardened software to avoid noise problems*

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It must be noted that good EMC performance is highly dependent on the user application and the software.

Therefore, it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

5.3.13.3 *Software recommendations*

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (such as control registers)

See also application note AN1015.

5.3.13.4 *Electromagnetic Interference (EMI)*

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 51. EMI characteristics for f_{HSE} = 24 MHz and F_{PLL1} = 1500 MHz

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Monitored frequency band	Value	Unit
S_{EMI}	Peak[1]	V_{DD} = 3.6 V, TA = 25 °C, VFBGA273 package, $F_{ck\_icn\_hs\_mcu}$ = 300 MHz, Cortex-M33 cores not running, conforming to IEC61967-2	0.1 MHz to 30 MHz	7	dBµV
			30 MHz to 130 MHz	15	
			130 MHz to 1 GHz	14	
			1 GHz to 2 GHz	10	
	Level[2]		0.1 MHz to 2 GHz	3	-

1. *Refer to AN1709 "EMI radiated test" section.*
2. *Refer to AN1709 "EMI level classification" section.*

5.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

5.3.14.1 *Electrostatic discharge (ESD)*

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 52. ESD absolute maximum ratings

Evaluated by characterization, not tested in production.

Symbol	Ratings	Conditions	Packages	Class	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-001	All	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESDA/JEDEC JS-002	All	C1	250	V

5.3.14.2 *Static latchup*

Two complementary static tests are required on three parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

Table 53. Electrical sensitivities

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Class
LU	Static latchup class	T_A = +25 °C conforming to JESD78	II level A

5.3.15 I/O current injection characteristics

As a rule, a current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} must be avoided during the normal product operation. However, in order to give an indication of the robustness of the device in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

5.3.15.1 *Functional susceptibility to I/O current injection*

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter:

- ADC error above a certain limit: higher than 5 LSB total unadjusted error (TUE),
- Out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range)
- Other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

Table 54. I/O current injection susceptibility

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Description	Negative injection	Positive Injection	Unit
I_{INJ}	PC3, PC4, PF1, PH0_OSC_IN, PH1_OSC_OUT, PC14_OSC32_IN, PC15_OSC32_OUT	0	0	mA
	All other FTxx I/Os	5	NA	

5.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 55 are derived from tests performed under the conditions summarized in Table 17. General operating conditions. All I/Os are CMOS and TTL compliant.

Table 55. I/O static characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

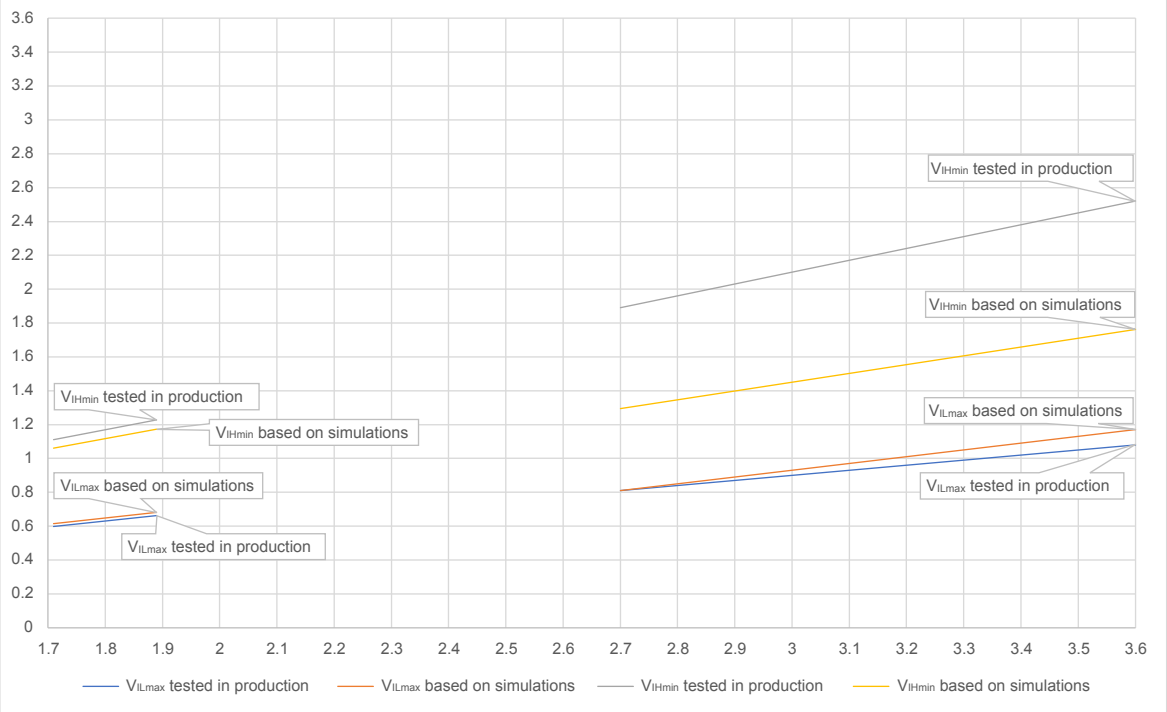
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}(1)	I/O input low voltage	2.7 < V_{DDx} < 3.6 V	-	-	0.3 × V_{DDx}	V
		1.71 <V_{DDx} < 1.89 V	-	-	0.35 × V_{DDx}	V
V_{IH}(1)	I/O input high voltage	2.7 < V_{DDx} < 3.6 V	0.7 × V_{DDx}	-	-	V
		1.71 < V_{DDx} < 1.89 V	0.65 × V_{DDx}	-	-	V
V_{IL}(2)	I/O input low voltage	2.7 < V_{DDx} < 3.6 V	-	-	0.4 × V_{DDx} - 0.27	V
		1.71 < V_{DDx} < 1.89 V	-	-	0.36 × V_{DDx}	V
V_{IH}(2)	I/O input high voltage	2.7 <V_{DDx} < 3.6 V	0.52 × V_{DDx} - 0.11	-	-	V
		1.71 < V_{DDx} < 1.89 V	0.62 × V_{DDx}	-	-	V
VHYS	I/O input hysteresis	2.7 < V_{DDx} < 3.6 V	-	0.44	-	V
		1.71 <V_{DDx} < 1.89 V	-	0.44	-	V
I_{leak}	TT_x input leakage		-	50	10000	nA
I_{VDDx}	Static current consumption on V_{DDx}		-	40	2000	nA
$I_{VDDA18AON}$	Static current consumption on $V_{DDA18AON}$		-	2	80	nA

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{VDDCORE}$	Static current consumption on V_{DDCORE}		-	1	180	nA
R_{PU}	Weak pull-up equivalent resistor(3)	2.7 < V_{DDx} < 3.6 V	30	40	50	kΩ
		1.71 < V_{DDx} < 1.89 V	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)	2.7 < V_{DDx} < 3.6 V	30	40	50	kΩ
		1.71 < V_{DDx} < 1.89 V	30	40	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. *Guaranteed by testing.*
2. *Specified by design, not tested in production.*
3. *The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).*

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for TT I/Os is shown in Figure 19.

Figure 19. V_{IL}/V_{IH} for TT I/Os



5.3.16.1 *Output driving current*

The GPIOs (general purpose input/outputs) can sink or source up to ±20 mA (depending on speed setup, supply voltage range and temperature).

In the user application, I/O drive current must be limited to respect the absolute maximum rating specified in Section 5.2: Absolute maximum ratings, in particular:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run mode consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating ΣI_{VDD} (see Table 14. Voltage characteristics).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run mode consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see Table 15. Current characteristics).

5.3.16.2 *Output voltage levels*

Unless otherwise specified, the parameters given in Table 56 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions. All I/Os are CMOS and TTL compliant.

Table 56. Output voltage characteristics for all I/Os

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions(1) (2) (3) (4)	Min	Max	Unit
V_{OL}	Output low level voltage (3.3 V range, 2.7 < V_{DDx} < 3.6 V)	I_{IO} = 6.5 mA, Speed = 0b00	-	0.4	V
		I_{IO} = 10 mA, Speed = 0b01	-	0.4	
		I_{IO} = 13 mA, Speed = 0b10	-	0.4	
		I_{IO} = 20 mA, Speed = 0b11	-	0.4	
V_{OH}	Output high level voltage (3.3 V range, 2.7 < V_{DDx} < 3.6 V)	I_{IO} = 6.5 mA, Speed = 0b00	V_{DDx} - 0.4	-	V
		I_{IO} = 10 mA, Speed = 0b01	V_{DDx} - 0.4	-	V
		I_{IO} = 13 mA, Speed = 0b10	V_{DDx} - 0.4	-	V
		I_{IO} = 20 mA, Speed = 0b11	V_{DDx} - 0.4	-	V
V_{OL}	Output low level voltage (1.8 V range, 1.71 < V_{DDx} < 1.89 V)	I_{IO} = 5.5 mA, Speed = 0b00	-	0.4	V
		I_{IO} = 8 mA, Speed = 0b01	-	0.4	V
		I_{IO} = 11 mA, Speed = 0b10	-	0.4	V
		I_{IO} = 16 mA, Speed = 0b11	-	0.4	V
V_{OH}	Output high level voltage (1.8 V range, 1.71 < V_{DDx} < 1.89 V)	I_{IO} = 5.5 mA, Speed = 0b00	V_{DDx} - 0.4	-	V
		I_{IO} = 8m A, Speed = 0b01	V_{DDx} - 0.4	-	V
		I_{IO} = 11 mA, Speed = 0b10	V_{DDx} - 0.4	-	V
		I_{IO} = 16 mA, Speed = 0b11	V_{DDx} - 0.4	-	V

1. *110 <T_J < 120: 4 mA.*
2. *90 < T_J < 110: 10 mA.*
3. *T_J < 90: 20 mA.*
4. *Maximum current depends on temperature.*

5.3.16.3 *Output buffer timing characteristics*

Table 57. Output timing characteristics (V_{DD} = 3.0 - 3.6 V or V_{DDIOx} = 2.7 - 3.6 V, VDDIOxVRSEL = 0)

Evaluated by characterization, not tested in production unless otherwise specified.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax(1)	Maximum frequency	C = 50 pF	-	30	MHz
			C = 40 pF	-	35	
			C = 30 pF	-	45	
			C = 20 pF	-	67	
			C = 10 pF	-	110	
	Tr/Tf(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	11.7	ns
			C = 40 pF	-	9.5	
			C = 30 pF	-	7.3	
			C = 20 pF	-	5.2	

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 10 pF	-	3	ns
0b01	Fmax[1]	Maximum frequency	C = 50 pF	-	45	MHz
			C = 40 pF	-	55	
			C = 30 pF	-	70	
			C = 20 pF	-	100	
			C = 10 pF	-	166	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	8.1	ns
			C = 40 pF	-	6.7	
			C = 30 pF	-	5.2	
			C = 20 pF	-	3.6	
			C = 10 pF	-	2.2	
0b10[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	60	MHz
			C = 40 pF	-	75	
			C = 30 pF	-	100	
			C = 20 pF	-	133	
			C = 10 pF	-	190	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	6.3	ns
			C = 40 pF	-	5.1	
			C = 30 pF	-	4	
			C = 20 pF	-	2.9	
			C = 10 pF	-	1.8	
0b11[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	80	MHz
			C = 40 pF	-	100	
			C = 30 pF	-	120	
			C = 20 pF	-	166	
			C = 10 pF	-	220	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	4.4	ns
			C = 40 pF	-	3.7	
			C = 30 pF	-	2.9	
			C = 20 pF	-	2.2	
			C = 10 pF	-	1.5	

1. *The maximum frequency is defined with the following conditions: (Tr + Tf) ≤ 2/3 T and Skew ≤ 1/20 T and 45% < Duty cycle < 55%.*
2. *The fall and rise time are defined respectively between 90% and 10%, and between 10% and 90% of the output waveform.*
3. *IO compensation enabled.*

Table 58. Output timing characteristics (V_{DD}/V_{DDIOx} = 1.71 - 1.89 V, VDDIOxVRSEL = 1)

Evaluated by characterization, not tested in production unless otherwise specified.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax[1]	Maximum frequency	C = 50 pF	-	30	MHz
			C = 40 pF	-	35	

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax[1]	Maximum frequency	C = 30 pF	-	45	MHz
			C = 20 pF	-	67	
			C = 10 pF	-	110	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	11	ns
			C = 40 pF	-	9	
			C = 30 pF	-	7	
			C = 20 pF	-	5	
			C = 10 pF	-	3	
0b01	Fmax[1]	Maximum frequency	C = 50 pF	-	45	MHz
			C = 40 pF	-	55	
			C = 30 pF	-	70	
			C = 20 pF	-	100	
			C = 10 pF	-	166	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	7.4	ns
			C = 40 pF	-	6.1	
			C = 30 pF	-	4.7	
			C = 20 pF	-	3.4	
			C = 10 pF	-	2.1	
0b10[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	60	MHz
			C = 40 pF	-	75	
			C = 30 pF	-	100	
			C = 20 pF	-	133	
			C = 10 pF	-	200	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	5.7	ns
			C = 40 pF	-	4.7	
			C = 30 pF	-	3.7	
			C = 20 pF	-	2.7	
			C = 10 pF	-	1.7	
0b11[3]	Fmax[1]	Maximum frequency	C = 50 pF	-	80	MHz
			C = 40 pF	-	100	
			C = 30 pF	-	120	
			C = 20 pF	-	166	
			C = 10 pF	-	250	
	Tr/Tf[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	4.1	ns
			C = 40 pF	-	3.4	
			C = 30 pF	-	2.7	
			C = 20 pF	-	2	
			C = 10 pF	-	1.3	

1. *The maximum frequency is defined with the following conditions : (Tr + Tf) ≤ 2/3 T and Skew ≤ 1/20 T and 45% < Duty cycle < 55%.*
2. *The fall and rise time are defined respectively between 90% and 10%, and between 10% and 90% of the output waveform.*
3. *IO compensation enabled.*

Table 59. Output timing characteristics (V_{DD}/V_{DDIOx} = 1.71 - 1.89 V, VDDIOxVRSEL = 0 degraded mode)

Evaluated by characterization, not tested in production unless otherwise specified.

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b00	Fmax(1)	Maximum frequency	C 50 pF	-	10	MHz
			C = 40 pF	-	15	
			C = 30 pF	-	20	
			C = 20 pF	-	33	
			C = 10 pF	-	45	
	Tr/Tf(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	30.2	ns
			C = 40 pF	-	24.4	
			C = 30 pF	-	18.7	
			C = 20 pF	-	13	
			C = 10 pF	-	7.4	
0b01	Fmax(1)	Maximum frequency	C = 50 pF	-	15	MHz
			C = 40 pF	-	20	
			C = 30 pF	-	25	
			C = 20 pF	-	37	
			C = 10 pF	-	60	
	Tr/Tf(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	21.1	ns
			C = 40 pF	-	17.2	
			C = 30 pF	-	13.3	
			C = 20 pF	-	9.4	
			C = 10 pF	-	5.5	
0b10(3)	Fmax(1)	Maximum frequency	C = 50 pF	-	20	MHz
			C = 40 pF	-	25	
			C = 30 pF	-	30	
			C = 20 pF	-	45	
			C = 10 pF	-	75	
	Tr/Tf(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	17	ns
			C = 40 pF	-	13.9	
			C = 30 pF	-	10.8	
			C = 20 pF	-	7.8	
			C = 10 pF	-	4.5	
0b11(3)	Fmax(1)	Maximum frequency	C = 50 pF	-	30	MHz
			C = 40 pF	-	35	
			C = 30 pF	-	45	
			C = 20 pF	-	60	
			C = 10 pF	-	85	
	Tr/Tf(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF	-	11.8	ns
			C = 40 pF	-	9.8	
			C = 30 pF	-	7.9	
			C = 20 pF	-	5.8	

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
0b11(3)	Tr/Tf(2)	Output high to low level fall time and output low to high level rise time	C = 10 pF	-	3.8	ns

1. *The maximum frequency is defined with the following conditions : (Tr + Tf) ≤ 2/3 T and Skew ≤ 1/20 T and 45% < Duty cycle < 55%.*
2. *The fall and rise time are defined respectively between 90% and 10%, and between 10% and 90% of the output waveform.*
3. *IO compensation enabled.*

Table 60. GPIO advance config delay characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	0	-	0.05	ps
t_{Δ}	Unit Delay	-	-	0.25	-	

5.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see Table 55. I/O static characteristics).

Unless otherwise specified, the parameters given in Table 61 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 17. General operating conditions.

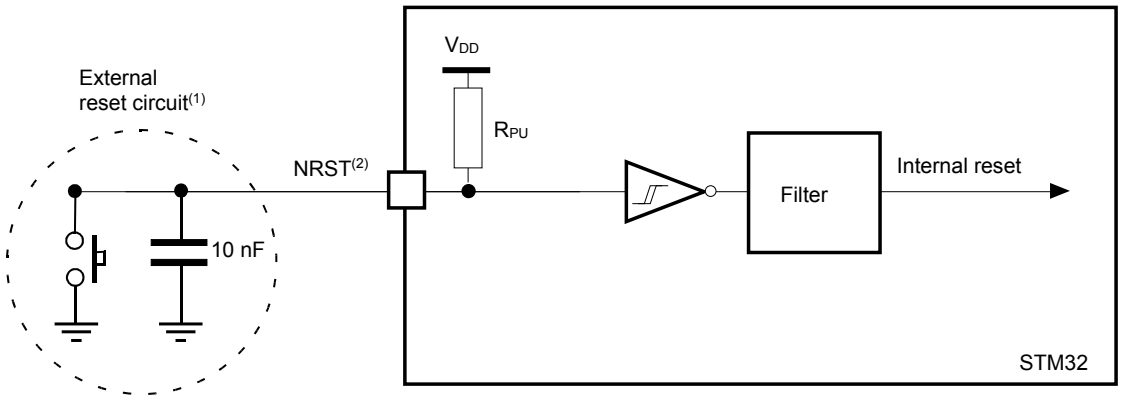
Table 61. NRST pin characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RPU(1)	Weak pull-up equivalent resistor	-	30	40	50	kΩ
tGEN	NRST minimum generated output pulse	-	17.5	-	-	µs
TFILT	NRST input filtered pulse	-	-	-	50	ns
TNFILT	NRST input not filtered pulse	-	150	-	-	ns
C_{NRST}	Capacitor on NRST pin	-	5	10	20	nF

1. *The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).*

Figure 20. Recommended NRST pin protection



1. *The reset network protects the device against parasitic resets.*
2. *The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 61. Otherwise, the reset is not taken into account by the device.*

5.3.18 DDR IOs characteristics

Refer to JEDEC standards for more details and characteristics

- DDR3L: JESD79-3F with addendum JESD79-3-1A
- DDR4: JESD79-4D
- LPDDR4: JESD209-4D

5.3.19 FMC characteristics

Unless otherwise specified, the parameters given in Table 62. Asynchronous multiplexed PSRAM/NOR read timings to Table 69. NAND flash write timings for the FMC interface are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 × VDD

Refer to Section 5.3.16: I/O port characteristics for more details on the input/output characteristics.

5.3.19.1 Asynchronous waveforms and timings

Figure 21. Asynchronous multiplexed PSRAM/NOR read waveforms through Figure 22 represent asynchronous waveforms and Table 62. Asynchronous multiplexed PSRAM/NOR read timings through Table 65 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- DataHoldTime = 0x1 (1 × $T_{fmc\_ker\_ck}$ for read operations and 2 × $T_{fmc\_ker\_ck}$ for write operations)
- ByteLaneSetup = 0x1
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all the timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period.

Table 62. Asynchronous multiplexed PSRAM/NOR read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	4 × $T_{fmc\_ker\_ck}$ - 1	4 × $T_{fmc\_ker\_ck}$ + 0.5	ns
$t_{v(NOE\_NE)}$	FMC_NEx low to FMC_NOE low	2 × $T_{fmc\_ker\_ck}$ - 1	2 × $T_{fmc\_ker\_ck}$ + 0.5	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc\_ker\_ck}$ - 1	$T_{fmc\_ker\_ck}$ + 0.5	
$t_{h(NE\_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc\_ker\_ck}$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck}$ - 1	$T_{fmc\_ker\_ck}$ + 0.5	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc\_ker\_ck}$ - 3	-	
$t_{h(A\_NOE)}$	Address hold time after FMC_NOE high	Address held until next read operation	-	
$t_{su(Data\_NE)}$	Data to FMC_NEx high setup time	$T_{fmc\_ker\_ck}$ + 14	-	

Symbol	Parameter	Min	Max	Unit
$t_{su(Data\_NOE)}$	Data to FMC_NOE high setup time	15	-	ns
$t_{h(Data\_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FMC_NOE high	0	-	

Table 63. Asynchronous multiplexed PSRAM/NOR read - NWAIT timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9 \times T_{fmc\_ker\_ck} - 1$	$9 \times T_{fmc\_ker\_ck} + 0.5$	ns
$t_{w(NOE)}$	FMC_NWE low time	$6 \times T_{fmc\_ker\_ck} - 1$	$6 \times T_{fmc\_ker\_ck} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5 \times T_{fmc\_ker\_ck} + 15$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4 \times T_{fmc\_ker\_ck} + 13$	-	

Figure 21. Asynchronous multiplexed PSRAM/NOR read waveforms

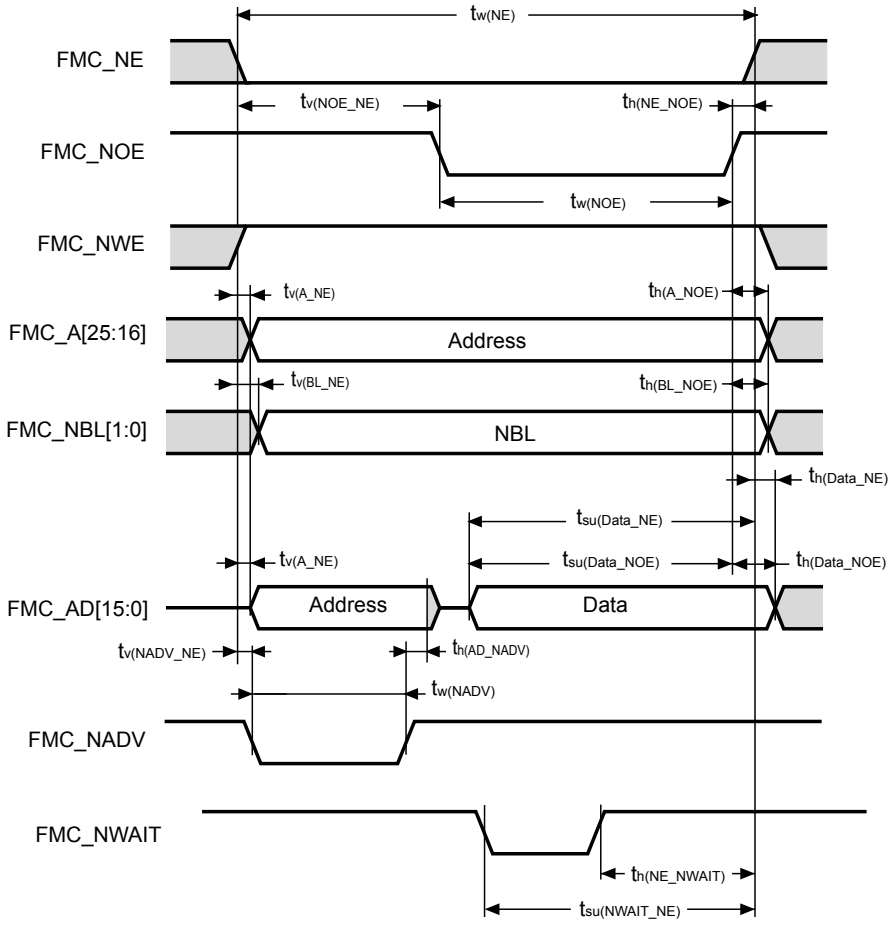


Table 64. Asynchronous multiplexed PSRAM/NOR write timings

Evaluated by characterization, not tested in production unless otherwise specified.

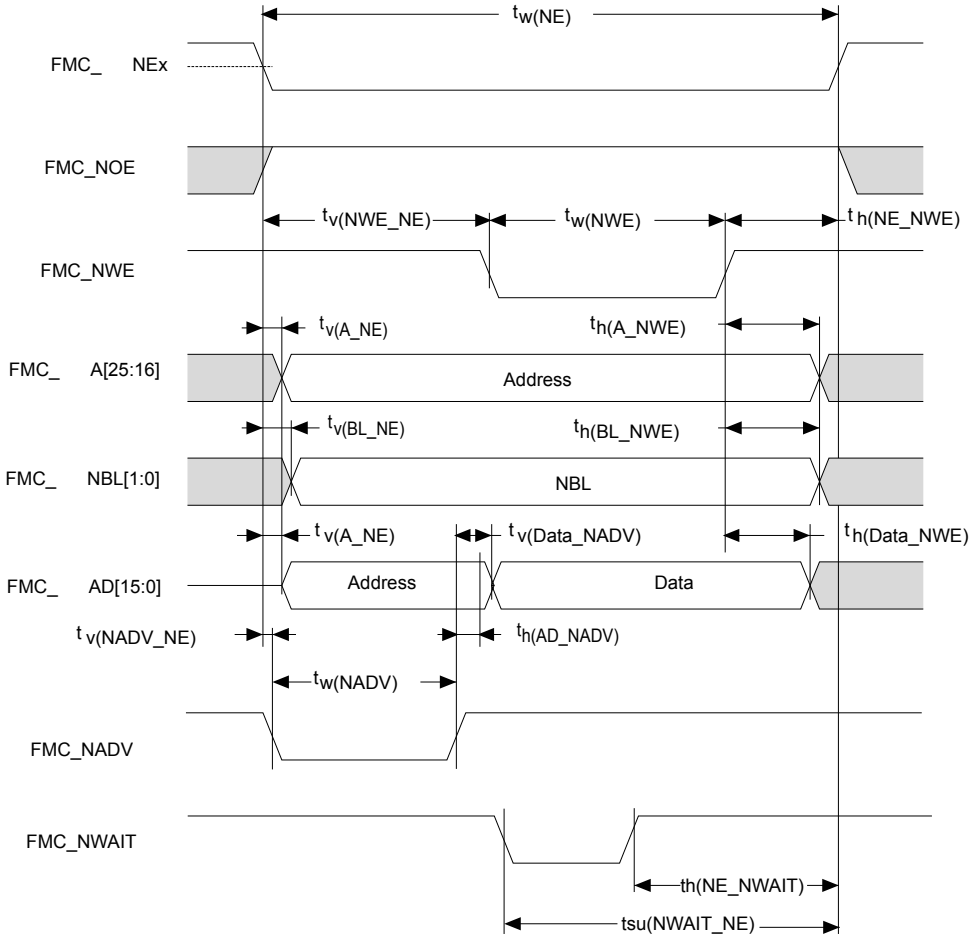
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4 \times T_{fmc\_ker\_ck} - 1$	$4 \times T_{fmc\_ker\_ck} + 1$	ns
$t_{v(NWE\_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc\_ker\_ck} - 1$	$T_{fmc\_ker\_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2 \times T_{fmc\_ker\_ck} - 0.5$	$2 \times T_{fmc\_ker\_ck} + 0.5$	
$t_{h(NE\_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc\_ker\_ck} - 0.5$	-	
$t_{v(A\_NE)}$	FMC_NEx low to FMC_A valid	-	2	
$t_{v(NADV\_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc\_ker\_ck} - 1$	$T_{fmc\_ker\_ck} + 1$	
$t_{h(AD\_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc\_ker\_ck} - 1$	-	
$t_{h(A\_NWE)}$	Address hold time after FMC_NWE high	$3 \times T_{fmc\_ker\_ck} - 1$	-	
$t_{h(BL\_NWE)}$	FMC_BL hold time after FMC_NWE high	$3 \times T_{fmc\_ker\_ck} + 1$	-	
$t_{v(BL\_NE)}$	FMC_NEx low to FMC_BL valid	-	0	
$t_{v(Data\_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc\_ker\_ck} + 1$	
$t_{h(Data\_NWE)}$	Data hold time after FMC_NWE high	$3 \times T_{fmc\_ker\_ck} - 1$	-	

Table 65. Asynchronous multiplexed PSRAM/NOR write - NWAIT timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9 \times T_{fmc\_ker\_ck} - 1$	$9 \times T_{fmc\_ker\_ck} + 0.5$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7 \times T_{fmc\_ker\_ck} - 1$	$7 \times T_{fmc\_ker\_ck} + 0.5$	
$t_{su(NWAIT\_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5 \times T_{fmc\_ker\_ck} + 15$	-	
$t_{h(NE\_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4 \times T_{fmc\_ker\_ck} + 13$	-	

Figure 22. Asynchronous multiplexed PSRAM/NOR write waveforms



5.3.19.2 *Synchronous waveforms and timings*

Figure 23. Synchronous multiplexed NOR/PSRAM read timings through Figure 24 represent synchronous waveforms and Table 66. Synchronous multiplexed NOR/PSRAM read timings through Table 67 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period, with the following FMC_CLK maximum values:

- For 1.65 V < V_{DD} < 3.6 V, FMC_CLK = 70 MHz at 20 pF

Table 66. Synchronous multiplexed NOR/PSRAM read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	R × $T_{fmc\_ker\_ck}$ -0.5(1)	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	R × $T_{fmc\_ker\_ck}$ / 2 + 1.5(1)	-	

Symbol	Parameter	Min	Max	Unit
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	ns
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16..25)	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16..25)	$R \times T_{fmc\_ker\_ck} / 2 + 0.5$(1)	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	0	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	$R \times T_{fmc\_ker\_ck} / 2 + 1$(1)	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0.5	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	3.5	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	2	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	
$t_{d(NExL-NWAIT)}$	FMC_NWAIT valid after FMC_NEx low (x = 0..2)	-	$(DATATLAT + 2.5) \times T_{fmc\_ker\_ck} \times R - 9$	

1. *Clock ratio R = (FMC_CLK period / fmc_ker_ck period).*

Figure 23. Synchronous multiplexed NOR/PSRAM read timings

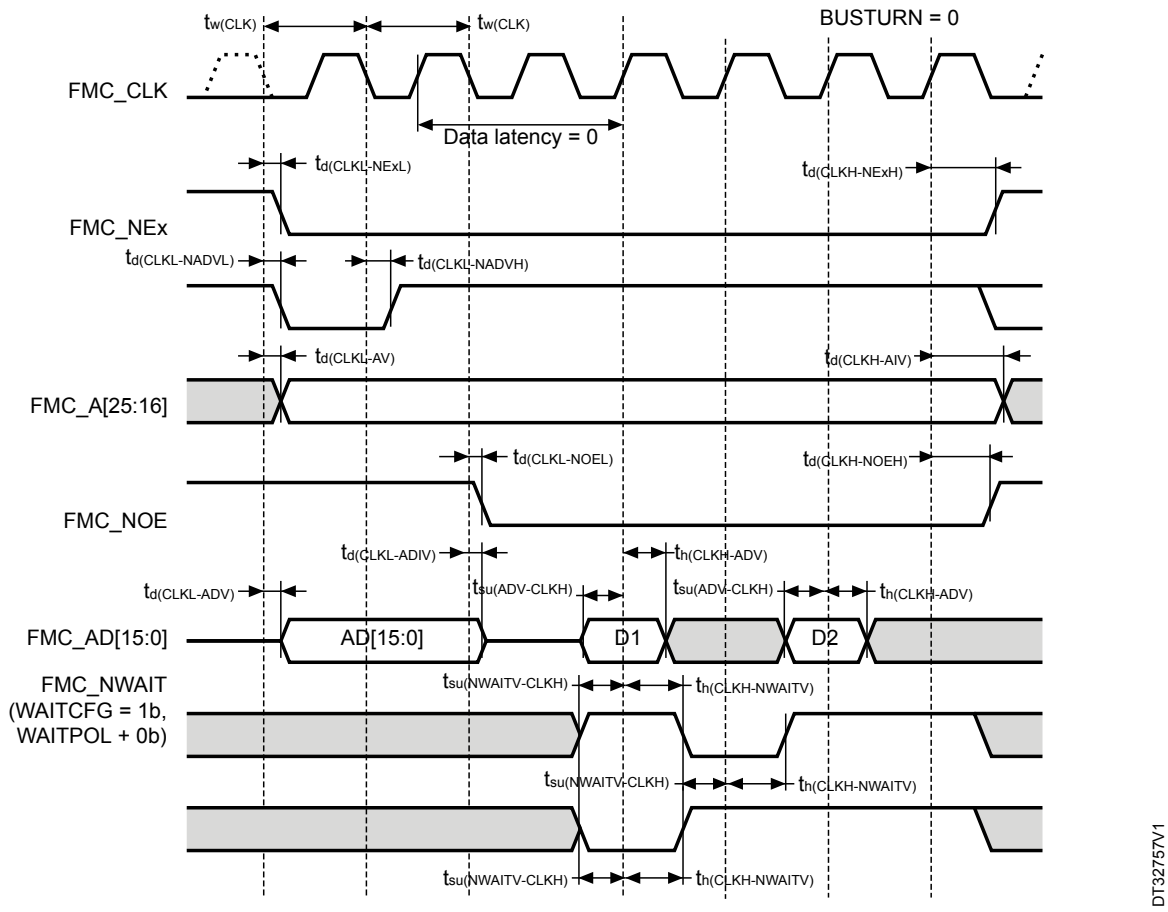


Table 67. Synchronous multiplexed PSRAM write timings

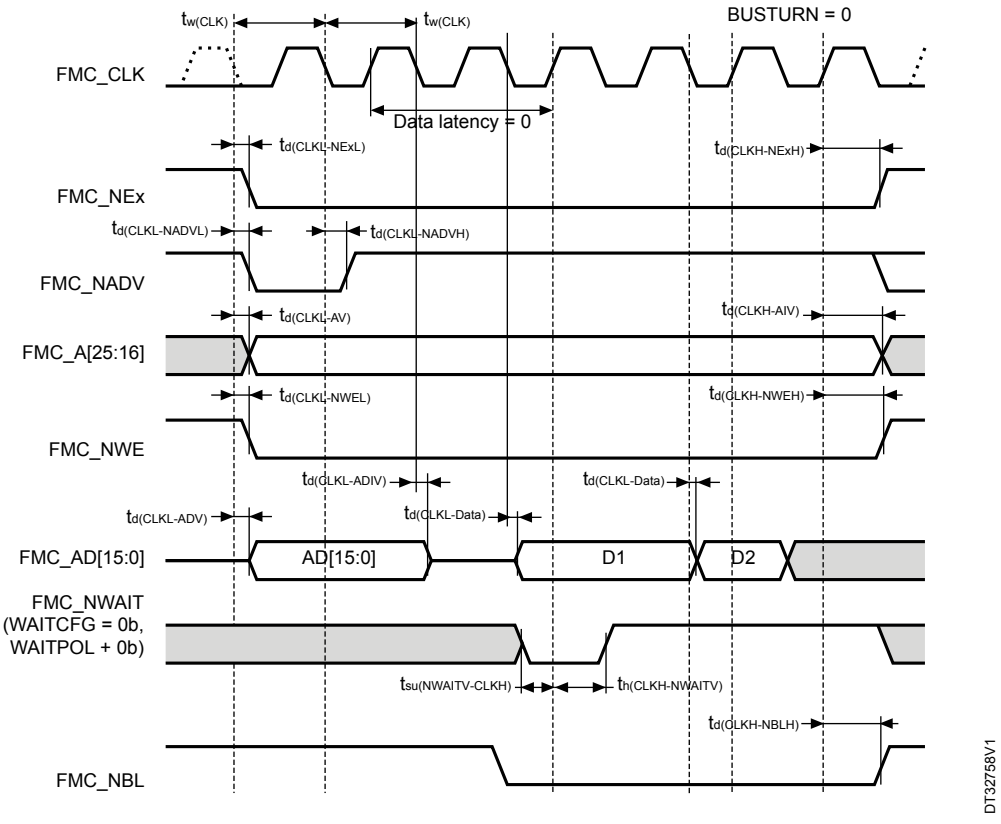
Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	$R \times T_{fmc\_ker\_ck}$-0.5(1)	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	2.5	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	$R \times T_{fmc\_ker\_ck} / 2 + 0.5$(1)	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	2.5	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	0.5	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16..25)	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16..25)	$R \times T_{fmc\_ker\_ck} / 2 + 0.5$(1)	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	1.5	

Symbol	Parameter	Min	Max	Unit
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	R × $T_{fmc\_ker\_ck}$ / 2	-	ns
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	3.5	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	0.5	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	3	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	0	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	R × $T_{fmc\_ker\_ck}$ / 2 + 2[1]	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	4	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	1	-	
$t_{d(NExL-NWAIT)}$	FMC_NWAIT valid after FMC_NEx low (x = 0..2)	-	(DATATLAT + 2.5) × $T_{fmc\_ker\_ck}$ × R - 9	

1. *Clock ratio R = (FMC_CLK period / fmc_ker_ck period).*

Figure 24. Synchronous multiplexed PSRAM write timings



5.3.19.3 *NAND controller waveforms and timings*

Figure 25 and Figure 26 represent synchronous waveforms, and Table 68 and Table 69 provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- FMC_SetupTime = 0x01
- FMC_WaitSetupTime = 0x03
- FMC_HoldSetupTime = 0x02
- FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- C_L = 30-pF

In all timing tables, the $T_{fmc\_ker\_ck}$ is the fmc_ker_ck clock period.

Table 68. NAND flash read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4 \times T_{fmc\_ker\_ck} - 0.5$	$4 \times T_{fmc\_ker\_ck} + 0.5$	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	12.5	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$2 \times T_{fmc\_ker\_ck} + 1.5$	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3 \times T_{fmc\_ker\_ck} - 1$	-	

Figure 25. NAND controller waveforms for read access

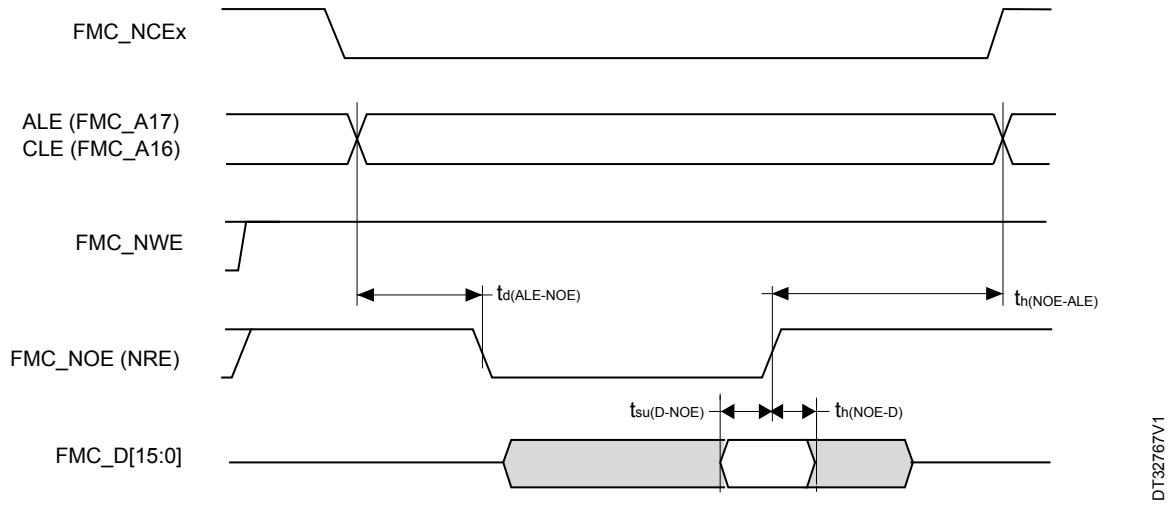
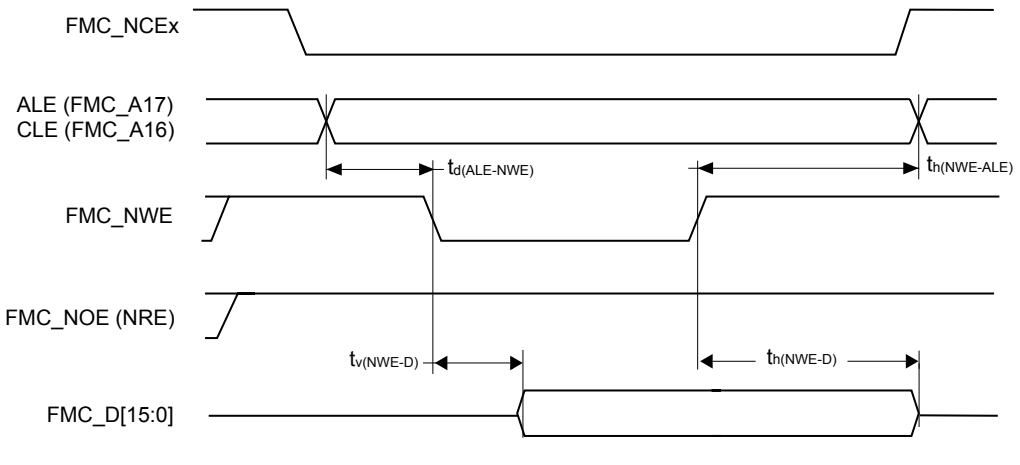


Table 69. NAND flash write timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4 \times T_{fmc\_ker\_ck} - 1$	$4 \times T_{fmc\_ker\_ck} + 1$	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$5 \times T_{fmc\_ker\_ck} - 1$	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$4 \times T_{fmc\_ker\_ck} - 1$	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$2 \times T_{fmc\_ker\_ck} + 1.5$	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$3 \times T_{fmc\_ker\_ck} - 1$	-	

Figure 26. NAND controller waveforms for write access



5.3.20 OCTOSPI interface characteristics

Unless otherwise specified, the parameters given in Table 70 , Table 71 and Table 72 for OCTOSPI are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- IO compensation cell activated
- VDDIOxVRSEL = 1 for $V_{DDIOx} < 2.7$ V

Refer to Section 5.3.16: I/O port characteristics for more details on the input/output alternate function characteristics.

Table 70. OCTOSPI characteristics in SDR mode

Evaluated by characterization, not tested in production unless otherwise specified.
Values in the table applies to octal and quad SPI mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	Clock frequency	$3\ V < V_{DDIOx} < 3.6\ V$, $C_L = 20$ pF	-	-	133	MHz
		$2.7\ V < V_{DDIOx} < 3.6\ V$, $C_L = 20$ pF	-	-	110	
		$1.71\ V < V_{DDIOx} < 1.89\ V$, $C_L = 20$ pF	-	-	133	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CLKH)}$	Clock high and low time - Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}$ / 2	-	$t_{(CLK)}$/2 +1	ns
$t_{w(CLKL)}$			$t_{(CLK)}$/2 - 1	-	$t_{(CLK)}$/2	
$t_{w(CLKH)}$	Clock high and low time - Odd division	PRESCALER[7:0] = n = 2,4,6,8	(n/2) × $t_{(CLK)}$ / (n+1)	-	(n/2) × $t_{(CLK)}$ / (n+1) + 1	
$t_{w(CLKL)}$			(n/2+1) × $t_{(CLK)}$ / (n+1) - 1	-	(n/2+1) × $t_{(CLK)}$ / (n+1)	
$t_{s(IN)}$	Data input setup time	-	3	-	-	
$t_{h(IN)}$	Data input hold time	-	1.5	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	0.5	1	
$t_{h(OUT)}$	Data output hold time	-	0	-	0	

Figure 27. OCTOSPI timing diagram - SDR mode

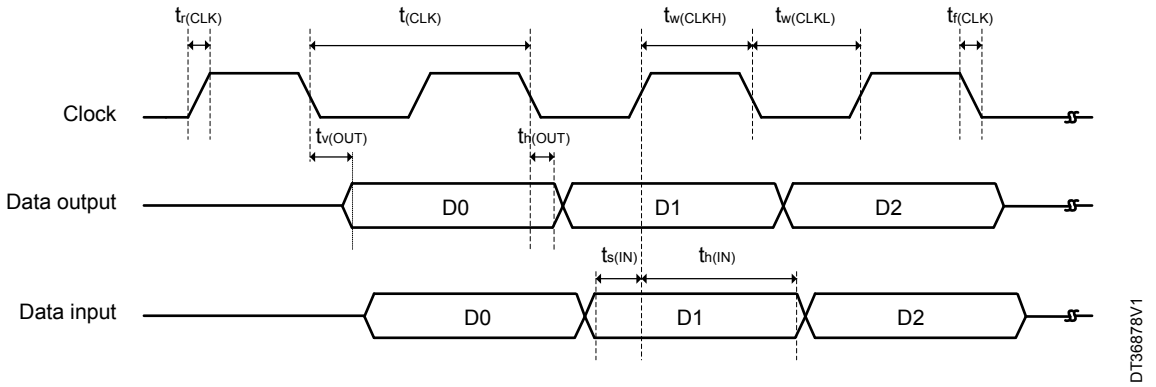


Table 71. OCTOSPI characteristics in DTR mode (without DQS)

Evaluated by characterization, not tested in production unless otherwise specified.
Values in the table applies to octal and quad SPI mode.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	Clock frequency	2.7 V < V_{DDIOx} < 3.6 V, C_L = 20 pF	-	-	100	MHz
		1.71 V < V_{DDIOx} < 1.98 V, C_L = 20 pF	-	-	100	
$t_{w(CLKH)}$	Clock high and low time - Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}$ / 2	-	$t_{(CLK)}$ / 2 + 1	ns
$t_{w(CLKL)}$			$t_{(CLK)}$/ 2 - 1	-	$t_{(CLK)}$ / 2	
$t_{w(CLKH)}$	Clock high and low time - Odd division	PRESCALER[7:0] = n = 2,4,6,8	(n/2) × $t_{(CLK)}$ / (n+1)	-	(n/2) × $t_{(CLK)}$ / (n+1) + 1	
$t_{w(CLKL)}$			(n/2+1) × $t_{(CLK)}$ / (n+1) - 1	-	(n/2+1) × $t_{(CLK)}$ / (n+1)	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	-	2.5	-	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	-	1.5	-	-	ns
$t_{vr(OUT)}$, $t_{vf(OUT)}$(1)	Data output valid time	-	-	1 + $t_{(CLK)}$ / 4	1.5 + $t_{(CLK)}$ / 4	
			-	1(1)	1(1)	
$t_{hr(OUT)}$, $t_{hf(OUT)}$(1)	Data output hold time	-	$t_{(CLK)}$ / 4 - 0.5	-	-	
			0(1)	-	-	

1. *When PRESCALER = 0 the DLL must be used for TX delay.*

Figure 28. OCTOSPI timing diagram - DTR mode

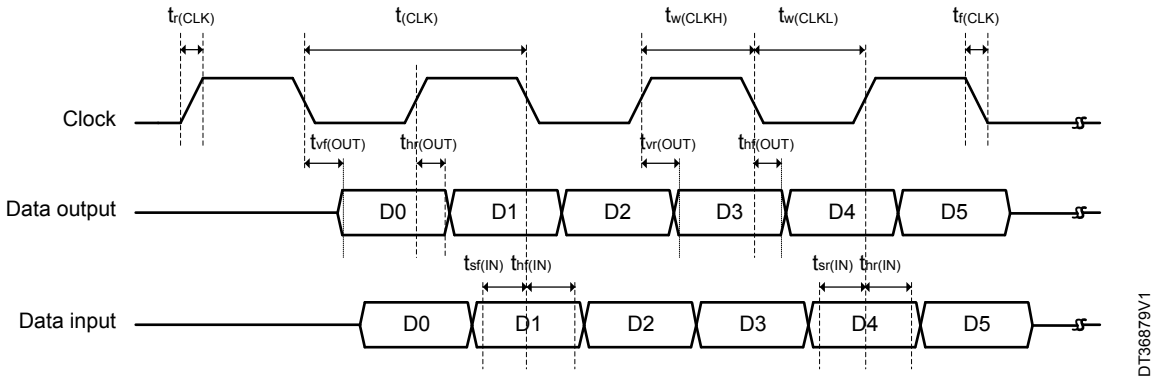


Table 72. OCTOSPI characteristics in DTR mode (with DQS or HyperBus)

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{(CLK)}$	Clock frequency	2.7 < V_{DDIOx} < 3.6, C_L = 20 pF	-	-	133	MHz
		1.71 < V_{DDIOx} < 1.89, C_L = 20 pF	-	-	133	
$t_{w(CLKH)}$	Clock high and low time - Even division	PRESCALER[7:0] = n = 0,1,3,5	$t_{(CLK)}$ / 2	-	$t_{(CLK)}$ / 2 + 1	ns
$t_{w(CLKL)}$			$t_{(CLK)}$ / 2 - 1	-	$t_{(CLK)}$ / 2	
$t_{w(CLKH)}$	Clock high and low time - Odd division	PRESCALER[7:0] = n = 2,4,6,8	(n/2) × $t_{(CLK)}$ / (n+1)	-	(n/2) × $t_{(CLK)}$ / (n+1) + 1	
$t_{w(CLKL)}$			(n/2+1) × $t_{(CLK)}$ / (n+1) - 1	-	(n/2+1) × $t_{(CLK)}$ / (n+1)	
$t_{w(CS)}$	Chip select high time	-	3 × $t_{(CLK)}$	-	-	
$t_{v(CK)}$	CS to Clock valid time	-	-	-	$t_{(CLK)}$ + 1	
$t_{h(CK)}$	Clock to CS high hold time	-	3.5×$t_{(CLK)}$	-	-	
$V_{ODr(CK)}$	CK,CK# crossing level on CK rising edge	V_{DDIOx} = 1.8 V	1157	-	1389	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{ODf(CK)}$	CK,CK# crossing level on CK falling edge	V_{DDIOx} = 1.8 V	1087	-	1312	ns
$t_{sr(DQ)}$, $t_{sf(DQ)}$	Data input setup time	$F_{(CLK)}$ > 50 MHz(1)	1.5 - $t_{(CLK)}$ / 4	-	-	
		$F_{(CLK)}$ < 50 MHz(2)	-1	-	-	
$t_{hrDQN)}$, $t_{hf(DQ)}$	Data input hold time	$F_{(CLK)}$ > 50 MHz(1)	1.5 + $t_{(CLK)}$ / 4	-	-	
		$F_{(CLK)}$ < 50 MHz(2)	3	-	-	
$t_{v(DS)}$	Data strobe input valid time	-	0	-	-	
$t_{h(DS)}$	Data strobe input hold time	-	0	-	-	
$t_{v(RWDS)}$	Data strobe output valid time	-	-	-	3 × $t_{(CLK)}$	
$t_{vr(OUT)}$, $t_{vf(OUT)}$(3)	Data output valid time	-	-	1 + $t_{(CLK)}$ / 4	1.5 + $t_{(CLK)}$ / 4	
			-	1	1.5	
$t_{hr(OUT)}$, $t_{hf(OUT)}$(3)	Data output hold time	-	$t_{(CLK)}$ / 4 - 0.5	-	-	
			0	-	-	

1. *DLL enabled in lock mode (SYSCFG_DLYBOSxCR.EN = 1) with 25% delay (SYSCFG_DLYBOSxCR.RX_TAP_SEL[5:0] = 0x8).*
2. *DLL enabled in bypass mode (SYSCFG_DLYBOSxCR.BYP_EN = 1) with typical settings (SYSCFG_DLYBOSxCR.RX_TAP_SEL[5:0] = 0x2 and SYSCFG_DLYBOSxCR.BYP_CMD[4:0] = 0x18).*
3. *When PRESCALER = 0 the DLL must be used for TX delay.*

Figure 29. OCTOSPI HyperBus clock

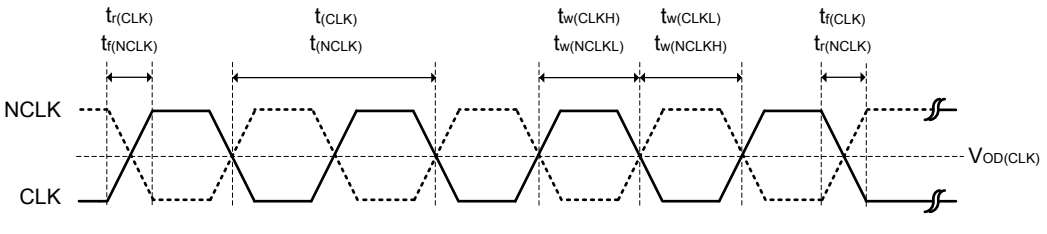


Figure 30. OCTOSPI HyperBus read

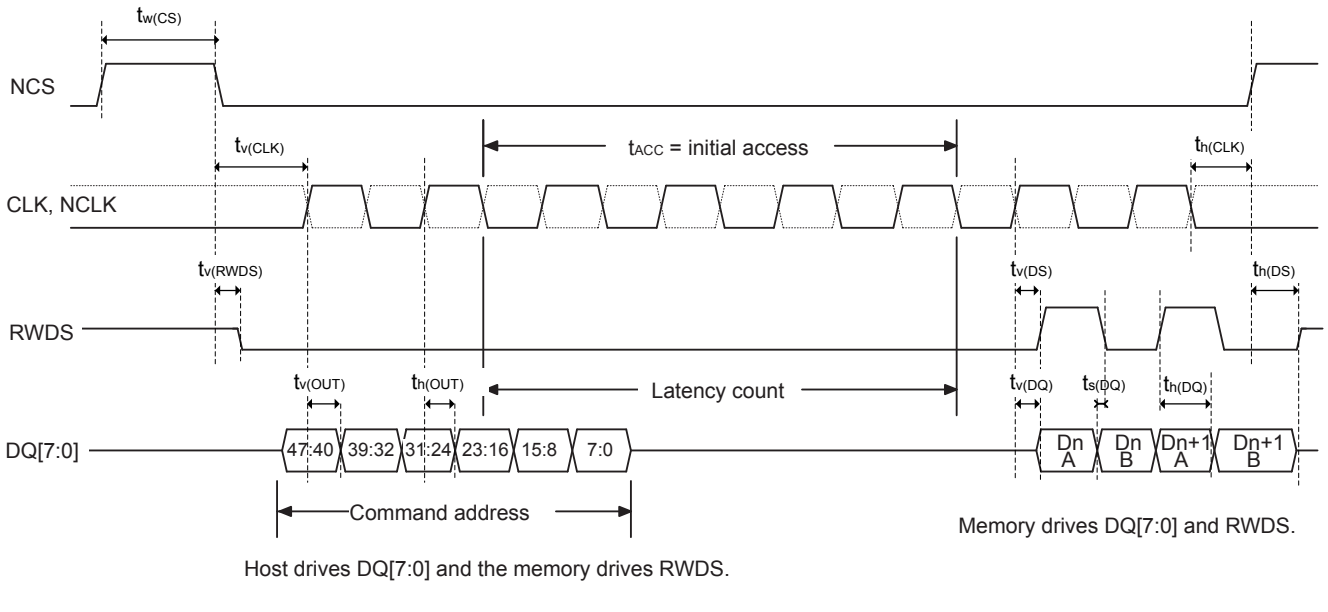


Figure 31. OCTOSPI HyperBus read with double latency

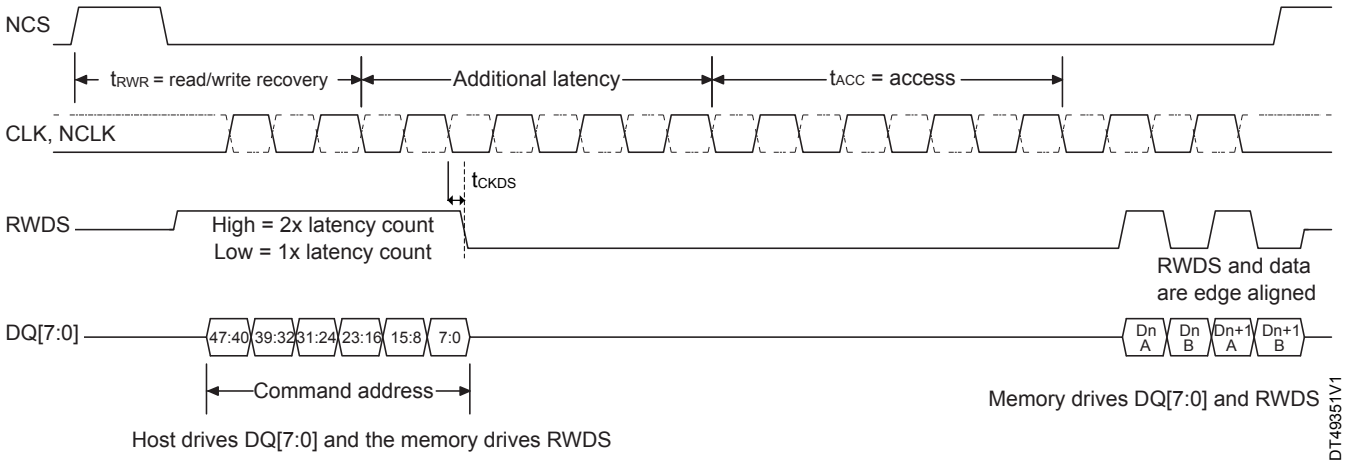
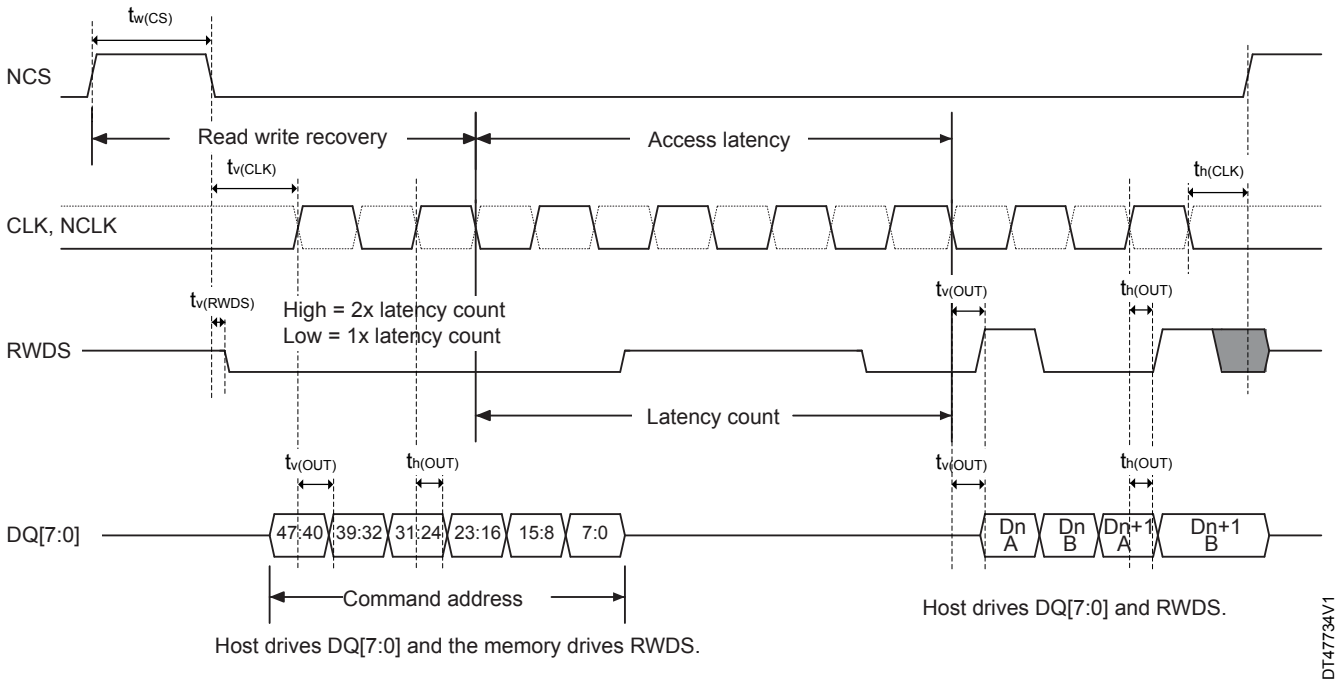


Figure 32. **OCTOSPI HyperBus write**



5.3.21 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in Table 73 for the delay block are derived from tests performed under the ambient temperature and V_{DD} supply voltage summarized in Table 17. General operating conditions.

Table 73. **DLYB characteristics**

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	Bypass mode	80	120	200	ps
t_{Δ}	Unit delay	Bypass mode	38	45	55	ps
		Lock mode	-	T / 32(1)	-	ps
			-7	-	+5	%

1. *T is the period of the DLL clock.*

5.3.22 12-bit ADC characteristics

Unless otherwise specified, the parameters given in Table 74. ADC characteristics are derived from tests performed under the ambient temperature, frequency and V_{DDA} supply voltage conditions summarized in Table 17. General operating conditions.

Table 74. **ADC characteristics**

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{ADC}	ADC adc_ker_ck clock frequency	-	0.7	-	70	MHz
f_s	Sampling rate	resolution = 12 bits	0.0467	-	4.666	MSps
		resolution = 10 bits	0.0538	-	5.384	MSps
		resolution = 8 bits	0.07	-	7	MSps

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_s	Sampling rate	resolution = 6 bits	0.0875	-	8.75	MSps
tc(1)	Conversion cycle	resolution = 12 bits	-	13.5	-	1 / f_{ADC}
		resolution = 10 bits	-	11.5	-	
		resolution = 8 bits	-	8.5	-	
		resolution = 6 bits	-	6.5	-	
f_{TRIG}	External trigger frequency	f_{ADC} = 70 MHz, Resolution = 12 bits	-	-	3.888	MHz
			18	-	-	1 / f_{ADC}
V_{AIN}(1)	Conversion voltage range(2)	Single ended	0	-	V_{REF+}	V
		Differential	-V_{REF+}	-	V_{REF+}	
V_{CMIV}(1)	Common mode input voltage	Differential	-	V_{REF+} / 2	-	V
C_{ADC}	Internal sample and hold capacitor	-	-	2.56	-	pF
t_{STAB}	ADC power-up time	DEEPPWD from 1 to 0	-	5	-	µs
t_{EN}	ADC enable time	ADEN from 0 to 1	-	5	-	1 / f_{ADC}
t_{LATR}(1)	Trigger conversion latency regular and injected channels without conversion abort	CKMODE = 0	2.5	-	3.5	1 / f_{ADC}
		CKMODE = 1	-	3	-	
$t_{LATRINJ}$(1)	Trigger conversion latency regular injected channels aborting a regular conversion	CKMODE = 0	3.5	-	4.5	1 / f_{ADC}
		CKMODE = 1	-	4	-	
t_S(1)	Sampling time	-	1.5	-	1499.5	1 / f_{ADC}
$I_{ADC(VDDA18ADC)}$	ADC supply current on $V_{DDA18ADC}$	f_s = 4.666 Msps, resolution = 12 bits	-	355	-	µA
		f_s = 5.384 Msps, resolution = 10 bits	-	330	-	
		Power down, ADEN = 0	-	2.6	-	
		Deep power down, ADEN = 0, DEEPPWD = 1	-	2.3	-	

1. *Specified by design, not tested in production.*
2. *All analog inputs must be between V_{SSA} and $V_{DDA18ADC}$. When offset calibration is used, the result of the conversion could be clipped few percent below V_{REF+}. Refer to reference manual for details.*

Table 75. ADC accuracy

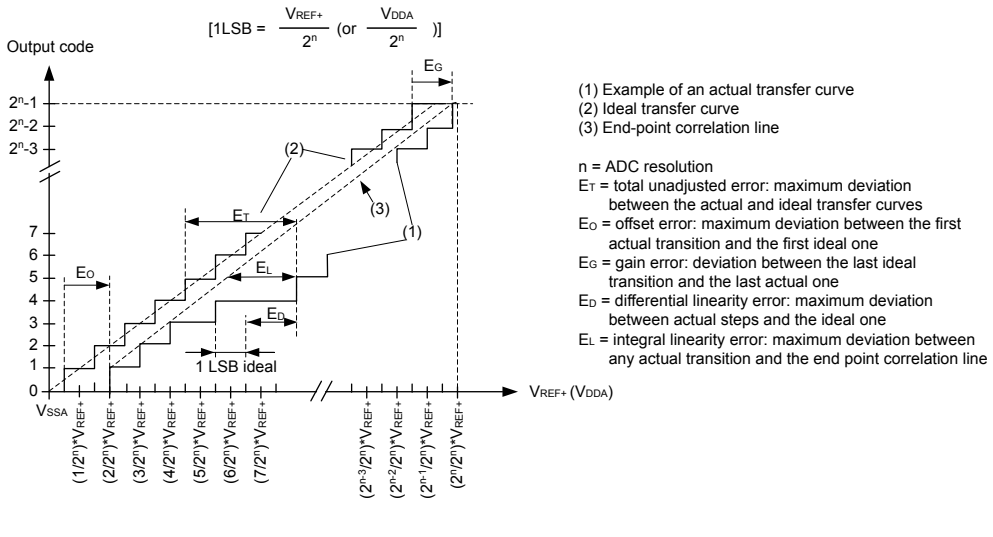
Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ET	Total unadjusted error (TUE)	Single ended with dedicated ANA input	-	4.6	14	±LSB
		Differential with dedicated ANA input	-	4.4	11	
		Single ended with general purpose I/O (GPIO) input	-	5.4	19	
		Differential with general purpose I/O (GPIO) input	-	7	20	
ED	Differential linearity error (DNL)	Single ended with dedicated ANA input	-	0	2	±LSB
		Differential with dedicated ANA input	-	0	2	
		Single ended with general purpose I/O (GPIO) input	-	0	2	
		Differential with general purpose I/O (GPIO) input	-	0	2	
EL	Integral linearity error (INL)	Single ended with dedicated ANA input	-	0	4	±LSB
		Differential with dedicated ANA input	-	0	4	
		Single ended with general purpose I/O (GPIO) input	-	0	8	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
EL	Integral linearity error (INL)	Differential with general purpose I/O (GPIO) input	-	0	10	±LSB
ENOB	Effective number of bits	Single ended with dedicated ANA input	-	9.8	-	Bits
		Differential with dedicated ANA input	-	10.5	-	
		Single ended with general purpose I/O (GPIO) input	-	9.6	-	
		Differential with general purpose I/O (GPIO) input	-	10.5	-	
SINAD	Signal-to-noise and distortion ratio(1)	Single ended with dedicated ANA input	-	60.5	-	dB
		Differential with dedicated ANA input	-	66.5	-	
		Single ended with general purpose I/O (GPIO) input	-	60	-	
		Differential with general purpose I/O (GPIO) input	-	65	-	
SNR	Signal-to-noise ratio	Single ended with dedicated ANA input	-	61	-	dB
		Differential with dedicated ANA input	-	66.5	-	
		Single ended with general purpose I/O (GPIO) input	-	60	-	
		Differential with general purpose I/O (GPIO) input	-	65.5	-	
THD	Total harmonic distortion	Single ended with dedicated ANA input	-	-77	-	dB
		Differential with dedicated ANA input	-	-79.5	-	
		Single ended with general purpose I/O (GPIO) input	-	-72.5	-	
		Differential with general purpose I/O (GPIO) input	-	-73	-	
EG	Gain error	Versus V_{REF+} value with dedicated ANA input	-1	-	+1	%FullScale
		Versus V_{REF+} value with general purpose I/O (GPIO) input	-1	-	+1	
EO	Offset error	Without calibration with ANA input	-1	-	+1	%FullScale
		After calibration with ANA input	-2	-	+2	LSB
		Without calibration with general purpose I/O (GPIO) input	-1	-	+1	%FullScale
		After calibration with general purpose I/O (GPIO) input	-2	-	+2	LSB

1. *Value measured with a -0.5 dBFS input signal and then extrapolated to full scale.*

Figure 33. ADC accuracy characteristics



1. *Refer to Table 76 for the values of R_{AIN}, R_{ADC} and C_{ADC}.*
2. *$C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to Table 55. I/O static characteristics). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} must be reduced.*
3. *Refer to Table 55. I/O static characteristics for value of I_{lkg}.*
4. *Refer to Figure 11. Power supply scheme.*

Table 76. Minimum sampling time versus RAIN

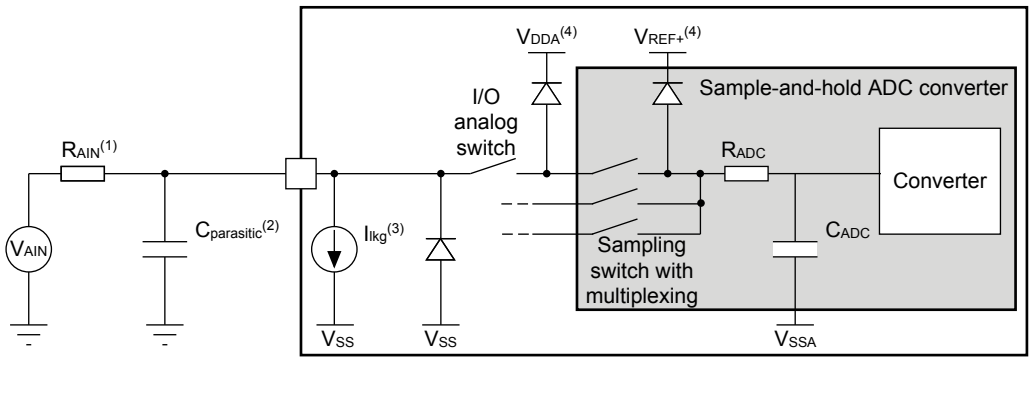
Specified by design, not tested in production.

Symbol	Parameter	Conditions (Resolution / R_{AIN} in ohms)		Min	Typ	Max	Unit
t_{s_min}	Minimum sampling time	12 bits	47	32	-	-	ns
			68	33	-	-	
			100	34	-	-	
			150	36	-	-	
			220	38	-	-	
			330	42	-	-	
			470	47	-	-	
			680	55	-	-	
			1000(1)	70	-	-	
t_{s_min}	Minimum sampling time	10 bits	47	23	-	-	ns
			68	24	-	-	
			100	25	-	-	
			150	26	-	-	
			220	28	-	-	
			330	30	-	-	
			470	33	-	-	
			680	38	-	-	
			1000	45	-	-	
			1500	55	-	-	
			2200	71	-	-	
			3300	97	-	-	
			4700	133	-	-	
			6800(1)	238	-	-	
t_{s_min}	Minimum sampling time	8 bits	47	17	-	-	ns
			68	17	-	-	
			100	18	-	-	
			150	19	-	-	
			220	20	-	-	
			330	22	-	-	
			470	25	-	-	
			680	28	-	-	
			1000	34	-	-	
			1500	42	-	-	

Symbol	Parameter	Conditions (Resolution / R_{AIN} in ohms)		Min	Typ	Max	Unit
t_{s_min}	Minimum sampling time	8 bits	2200	53	-	-	ns
			3300	70	-	-	
			4700	94	-	-	
			6800	128	-	-	
			10000	183	-	-	
			15000	277	-	-	
			22000(1)	435	-	-	

1. *Maximum external input impedance value authorized for the given Resolution.*

Figure 34. Typical connection diagram using the ADC with TT pins featuring analog switch function



5.3.22.1 *General PCB design guidelines*

PCB design guidelines are provided in AN6055 "Getting started with STM32MP21x MPUs hardware development" available from the ST website www.st.com.

5.3.23 Voltage reference buffer (VREFBUF) characteristics

Table 77. VREFBUF characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DDA18ADC}$	Analog supply voltage	-	VRS = 000	1.62	1.8	1.89(1)	V
			VRS = 001	1.75	1.8	1.89(1)	
V_{REFBUF_OUT}	Voltage Reference Buffer Output	At 30 °C, at I_{LOAD} = 10 µA, $V_{DDA18ADC}$ = 1.8 V	VRS = 000	1.203	1.21	1.216	
			VRS = 001	1.491	1.5	1.506	
TRIM	Trim step resolution	-		-	±0.05	±0.1	%
C_L	Load Capacitor	-		0.5	1.1	1.5	µF
esr	Equivalent Serial Resistor of C_L	-		-	-	1	Ω
I_{LOAD}	External DC load current	All ADCs ON		-	-	0.8	mA
		All ADCs OFF		-	-	2	
I_{LINE_REG}	Line regulation	1.62 V ≤ $V_{DDA18ADC}$ ≤ 1.89 V		-	7500	11000	ppm/V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{LOAD_REG}	Load regulation	100 µA ≤ I_{LOAD} ≤ 800 µA		-	4700	6000	ppm/mA
T_{coeff}	Temperature coefficient	-40 °C < T_J < +30 °C		89	-	+305	ppm/°C
		+30 °C < T_J < +125 °C		-15	-	68	
A_{coeff}	Long term stability	1000 hours, T_J = 125 °C		-2000	-	+2000	ppm
PSRR	Power supply rejection	DC		48	76	-	dB
		100 kHz		51	60	-	
t_{START}	Start-up time	-		-	260	388	µs
I_{INRUSH}	Control of max. DC current drive on V_{REFBUF_OUT} during start-up phase (t_{START})			-	-	10	mA
$I_{VDDA18ADC(VREFBUF)}$	VREFBUF supply current $V_{DDA18ADC}$ (excluding internal and external load)	ENVR = 1	I_{LOAD} = 0.8 mA DC	-	9	21	µA
			Peak during 2 × ADC conversion	-	48	60	
		ENVR = 0		-	3	6.5	µA

1. *Static condition. 1.98 V allowed during transients.*

5.3.24 Digital Temperature Sensor (DTS) characteristics

Table 78. DTS characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}	Operating frequency	-	4	-	8	MHz
Res	Resolution	-	8	10	12	Bits
Step	Step size	For respectively 8, 10 and 12 bits resolution	0.86	0.22	0.06	°C
t_{conv}	Conversion time	For respectively 8, 10 and 12 bits resolution	512	2048	8192	1 / f_{DTS}
t_{pwrup}	Power up time	-	-	-	256	
T_A	Accuracy	From -20 to +125 °C	-	-	3(1)	°C
		From -40° C to -20 °C	-	-	6	
G	G constant	Refer to reference manual for the formula	59.7			°C
H	H constant	Refer to reference manual for the formula	204.4			°C
J	J constant	Refer to reference manual for the formula	-0.16			°C / MHz
Cal5	Cal5 constant	Refer to reference manual for the formula	4094			-
TS_{loc}	Sensor location	TS0 sensor	Inside padring(2)			-
		TS1 sensor	Inside device logic(2)			-
$I_{DTS(VDDA18AON)}$	DTS supply current on $V_{DDA18AON}$	f_{DTS} = 8 MHz, continuous measurements, single sensor	-	120	160	µA
		At 1 measurement/s	-	-	1	
		f_{DTS} clock stopped	-	-	1	
$I_{DTS(VDDCORE)}$	DTS supply current on V_{DDCORE}	f_{DTS} = 8 MHz	-	-	15	µA

1. *Guaranteed by test in production.*
2. *Temperature in padring sensor (side of the silicon die) is usually slightly lower than device logic sensor as most heat is generated inside device logic.*

5.3.25 V_{BAT}, V_{DDCPU}, V_{DDCORE} ADC measurement characteristics

Table 79. V_{BAT}, V_{DDCPU}, V_{DDCORE} ADC measurement characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	-	130	-	kΩ
Q	Ratio on V_{BAT} measurement	-	-	4	-	-
E_r	Error on Q	-	-1	-	+1	%
t_{S_VBAT}(1)	ADC sampling time when reading the V_{BAT}	-	34	-	-	ns
t_{S_VDDCPU}(1)	ADC sampling time when reading the V_{DDCPU}	-	34	-	-	ns
$t_{S\_VDDCORE}$(1)	ADC sampling time when reading the V_{DDCORE}	-	34	-	-	ns

1. *Specified by design, not tested in production.*

5.3.26 Temperature and V_{BAT} monitoring characteristic for tamper detection

Table 80. TEMP and V_{BAT} Monitoring characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TEMPH	High T_J temperature monitoring	-	110	-	125	° C
TEMPL	Low T_J temperature monitoring	-	-40	-	-30	
V08CAPH	High V_{08CAP} supply monitoring(1)	-	0.88	-	1	V
V08CAPL	Low V_{08CAP} supply monitoring(1)	-	0.6	-	0.72	-
V08CAP_filter	V_{08CAP} supply monitoring glitch filter(1)	-	-	-	1	µs

1. *V08CAP is an internal regulator supplied by V_{SW}. V_{SW} is equal to V_{DD} when present or V_{BAT} otherwise.*

5.3.27 Voltage monitoring characteristics

Table 81. Voltage monitoring characteristics (V_{DDCORE}, V_{DDCPU}, PVD_IN, $V_{DDA18ADC}$, $V_{DDIO1/2/3}$, $V_{DD33USB}$)

Evaluated by characterization, not tested in production unless otherwise specified.

Parameter	Conditions		Min	Typ	Max	Unit
V_{DDCORE} monitoring						
Threshold on rising edge	To set VCOREH bit (overvoltage)		0.88(1)	-	-	V
Threshold on falling edge	To set VCOREL bit (undervoltage)		0.72	-	0.78(1)	
Hysteresis on monitoring	To clear VCOREL or VCOREH bit		-	20	-	mV
Supply current on $V_{DDA18AON}$	VCOREMONEN = 1		-	0.75	-	µA
V_{DDCPU} monitoring						
Threshold on rising edge	To set VCPUH bit (overvoltage)		0.99(1)	-	-	V
Threshold on falling edge	To set VCPUL bit (undervoltage)	VCPULLS = 0	0.72	-	0.78(1)	
		VCPULLS = 1	0.81	-	0.87	
Hysteresis on monitoring	To clear VCPUL or VCPUH bit		-	20	-	mV
Supply current on $V_{DDA18AON}$	VCPUMONEN = 1		-	0.75	-	µA

Parameter	Conditions		Min	Typ	Max	Unit
PVD_IN monitoring						
Threshold on rising edge	-		-	0.815	-	V
Hysteresis on monitoring	-		-	30	-	mV
Supply current on $V_{DDA18AON}$	PVDEN = 1		-	0.75	-	µA
$V_{DDA18ADC}$ monitoring						
Threshold on rising edge	-		-	-	1.55(1)	V
Hysteresis on monitoring	-		-	40	-	mV
Supply current on $V_{DDA18AON}$	AVMEN = 1		-	0.75	-	µA
Supply current on $V_{DDA18ADC}$	AVMEN = 1		-	1	-	µA
V_{DDIO1} monitoring						
Threshold on rising edge	-		-	-	1.55(1)	V
Hysteresis on monitoring	-		-	40	-	mV
Supply current on $V_{DDA18AON}$	VDDIO1VMEN = 1		-	0.75	-	µA
Supply current on V_{DDIO1}	Always ON	VDDIO1 = 1.8 V	-	0.5	-	µA
		VDDIO1 = 3.3 V	-	1	-	
V_{DDIO2} monitoring						
Threshold on rising edge	-		-	-	1.55(1)	V
Hysteresis on monitoring	-		-	40	-	mV
Supply current on $V_{DDA18AON}$	VDDIO2VMEN = 1		-	0.75	-	µA
Supply current on V_{DDIO2}	Always ON	VDDIO2 = 1.8 V	-	0.5	-	µA
		VDDIO2 = 3.3 V	-	1	-	
V_{DDIO3} monitoring						
Threshold on rising edge	-		-	-	1.55(1)	V
Hysteresis on monitoring	-		-	40	-	mV
Supply current on $V_{DDA18AON}$	VDDIO3VMEN = 1		-	0.75	-	µA
Supply current on V_{DDIO3}	Always ON	VDDIO3 = 1.8 V	-	0.5	-	µA
		VDDIO3 = 3.3 V	-	1	-	
$V_{DD33USB}$ monitoring						
Threshold on rising edge	-		-	-	1.55(1)	V
Hysteresis on monitoring	-		-	40	-	mV
Supply current on $V_{DDA18AON}$	USB33VMEN = 1		-	0.75	-	µA
Supply current on $V_{DD33USB}$	Always ON		-	1	-	µA

1. *Guaranteed by test in production.*

5.3.28 Compensation cell characteristics

Table 82. Compensation cell characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{COMPCELL}$	$V_{DDA18AON}$ current consumption during code calculation	Using a 16 MHz clock (HSI / 8)	-	250	-	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Tready	Time needed to have the first code calculation after enabling	Using a 16 MHz clock (HSI / 8)	-	96	-	µs
Tmeasure	Time needed to update the code		-	832	-	

5.3.29 Multi-function digital filter (MDF) characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell activated
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 83. MDF characteristics

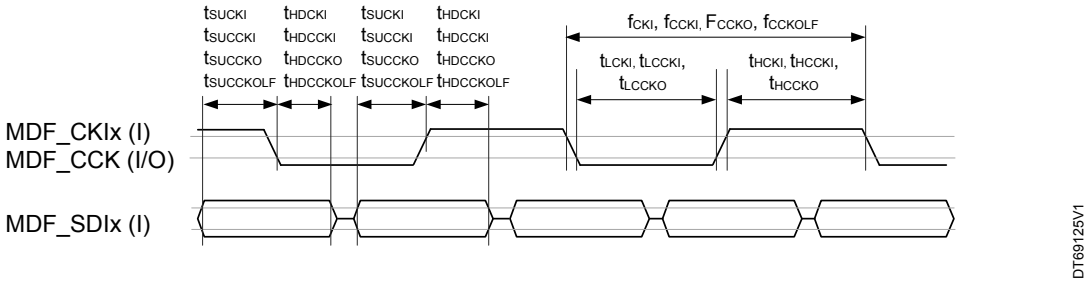
Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CKI}	Input clock frequency via MDF_CKIx pin, in SLAVE SPI mode	-	-	-	25	MHz
f_{CCKI}	Input clock frequency via MDF_CCK[1:0] pin, in SLAVE SPI mode	-	-	-	25	
f_{CCKO}	Output clock frequency in MASTER SPI mode	-	-	-	25	
f_{CCKOLF}	Output clock frequency in LF_MASTER SPI mode	-	-	-	5	
f_{SYMB}	Input symbol rate in Manchester mode	-	-	-	20	
t_{HCKI} t_{LCKI}	MDF_CKIx input clock high and low time	In SLAVE SPI mode	2 × $T_{mdf\_proc\_ck}$(1)	-	-	ns
t_{HCCKI} t_{LCCKI}	MDF_CCK[1:0] input clock high and low time	In SLAVE SPI mode	2 × $T_{mdf\_proc\_ck}$(1)	-	-	
t_{HCCKO} t_{LCCKO}	MDF_CCK[1:0] output clock high and low time	In MASTER SPI mode	2 × $T_{mdf\_proc\_ck}$(1)	-	-	
$t_{HCCKOLF}$ $t_{LCCKOLF}$	MDF_CCK[1:0] output clock high and low time	In LF_MASTER SPI mode	$T_{mdf\_proc\_ck}$(1)	-	-	
t_{SUCKI}	Data setup time with respect to MDF_CKIx input	In SLAVE SPI mode, measured on rising and falling edge	7.5	-	-	
t_{HDCKI}	Data hold time with respect to MDF_CKIx input		0.5	-	-	
t_{SUCCKI}	Data setup time with respect to MDF_CCK[1:0] input	In SLAVE SPI mode: MDF_CCK[1:0] configured in input, measured on rising and falling edge	8.5	-	-	
t_{HDCCKI}	Data hold time with respect to MDF_CCK[1:0] input		0.5	-	-	
t_{SUCCKO}	Data setup time with respect to MDF_CCK[1:0] output	In MASTER SPI mode: MDF_CCK[1:0] configured in output, measured on rising and falling edge	8.5	-	-	
t_{HDCCKO}	Data hold time with respect to MDF_CCK[1:0] output		0.5	-	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SUCCKOLF}$	Data setup time with respect to MDF_CCK[1:0] output	In LF_MASTER SPI mode, MDF_CCK[1:0] configured in output, measured on rising and falling edge	14.5	-	-	ns
$t_{HDCCKOLF}$	Data hold time with respect to MDF_CCK[1:0] output		0.5	-	-	

1. *Tmdf_proc_ck is the period of the MDF processing clock.*

Figure 35. MDF timing diagram



5.3.30 Camera interface (DCMI) characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

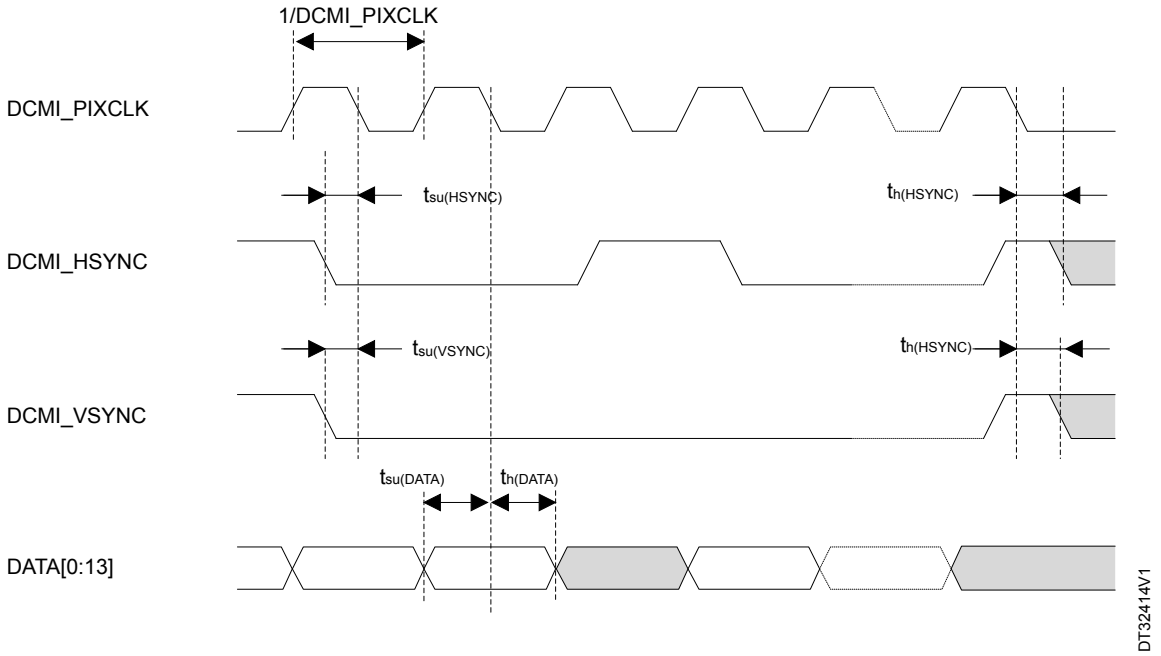
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load C_L = 30 pF
- Measurement points done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell activated
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 84. DCMI characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
clock_ratio	Frequency ratio DCMI_PIXCLK / f_{HCLK}	-	-	0.4	-
DCMI_PIXCLK	Pixel clock input	-	-	80	MHz
D_{PIXEL}	Pixel clock input duty cycle	30	-	70	%
$t_{su(DATA)}$	Data input setup time	3	-	-	ns
$t_{h(DATA)}$	Data hold time	2	-	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMI_HSYNC and DCMI_VSYNC input setup times	3	-	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMI_HSYNC and DCMI_VSYNC input hold times	2	-	-	

Figure 36. **DCMI timing diagram**



5.3.31 Camera interface (DCMIPP) characteristics

Unless otherwise specified, the parameters given in Table 85 for DCMIPP are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Section 5.3.1: General operating conditions, with the following configuration:

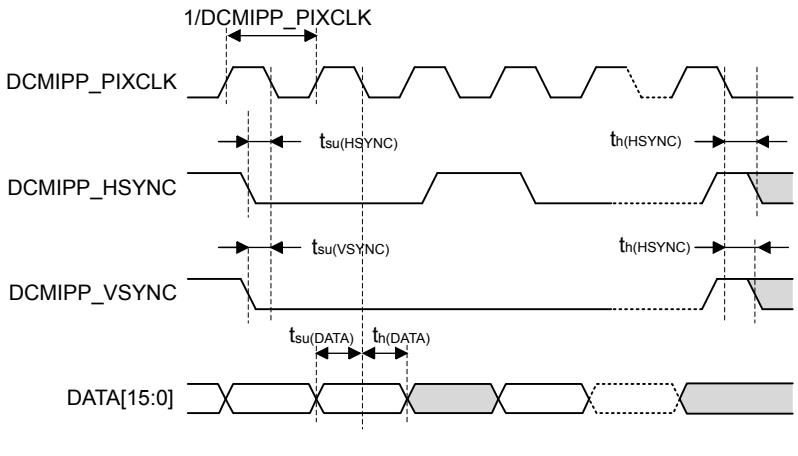
- DCMIPP_PIXCLK polarity: falling
- DCMIPP_VSYNC and DCMIPP_HSYNC polarity: high
- Advanced I/O configuration:
  - DCMIPP clock: RET = 0, INVCLK = 0, DE = 0, DLYPATH = 0
  - Other DCMIPP signals: RET = 1, INVCLK = 1, DE = 0, DLYPATH = 0
- Data formats: 16 bits
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell activated
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 85. **DCMIPP characteristics**

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DCMIPP_PIXCLK	Pixel clock input	-	-	-	120	MHz
DPixel	Pixel clock input duty cycle	-	30	-	70	%
$t_{su(DATA)}$	Data input setup time	-	2	-	-	ns
$t_{h(DATA)}$	Data input hold time	-	4	-	-	
$t_{su(HSYNC)}$ $t_{su(VSYNC)}$	DCMIPP_HSYNC / DCMIPP_VSYNC input setup time	-	2	-	-	
$t_{h(HSYNC)}$ $t_{h(VSYNC)}$	DCMIPP_HSYNC / DCMIPP_VSYNC input hold time	-	4	-	-	

Figure 37. **DCMIPP timing diagram**



5.3.32 Parallel interface (PSSI) characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- PSSI_PDCK polarity: falling
- PSSI_RDY and PSSI_DE polarity: low
- Bus width: 16 lines
- Data width: 32 bits
- Capacitive load C_L = 30 pF
- Measurement points done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell activated
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 86. **PSSI transmit characteristics**

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
clock_ratio	Frequency ratio DCMI_PDCK/f_{HCLK}	-	-	-	0.4	-
PSSI_PDCK	PSSI clock input	-	-	-	74(1)	MHz
D_{PIXEL}	PSSI clock input duty cycle	-	30	-	70	%
$t_{OV(DATA)}$	Data output valid time	-	-	-	13.5	ns
$t_{OH(DATA)}$	Data output hold time	-	5.5	-	-	
$t_{OV(DE)}$	DE output valid time		-	-	10	
$t_{OH(DE)}$	DE output hold time		6.5	-	-	
$t_{SU(RDY)}$	RDY input setup time	-	0	-	-	
$t_{H(RDY)}$	RDY input hold time		0	-	-	

1. *This maximal frequency does not consider receiver setup and hold timings.*

Figure 38. PSSI transmit timing diagram

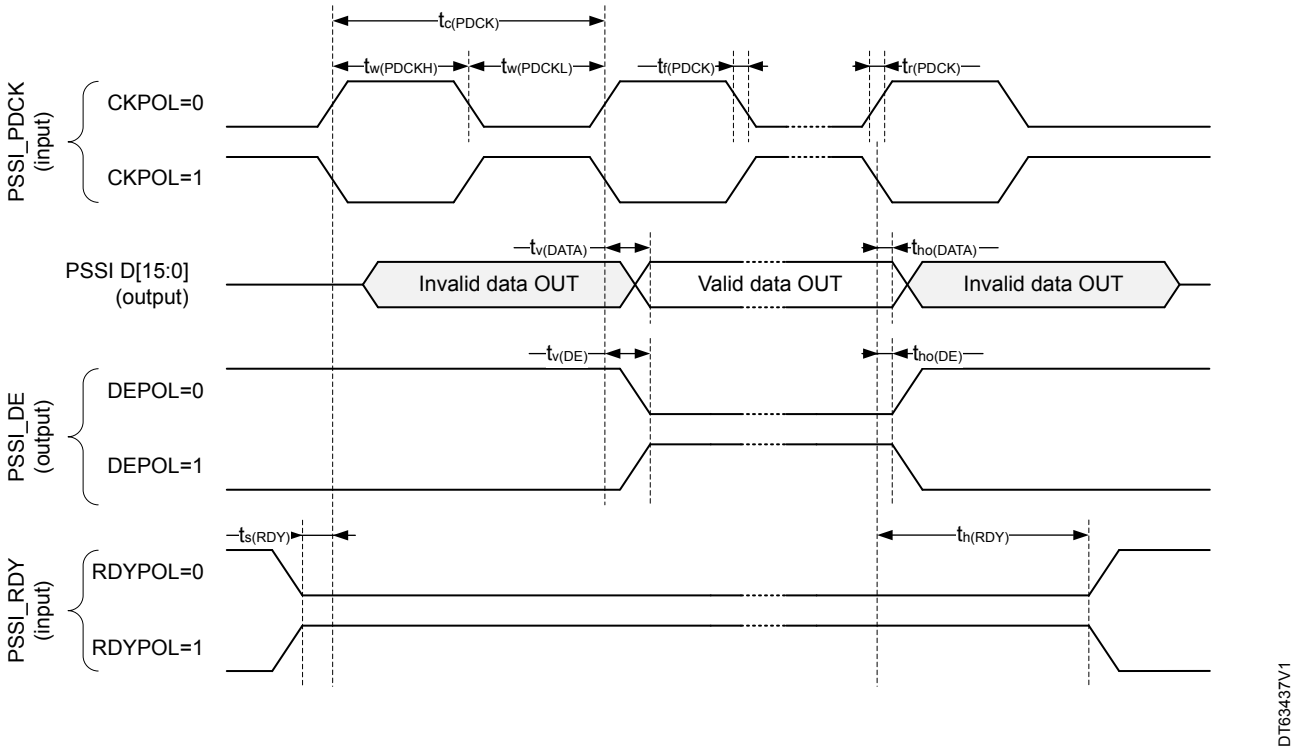
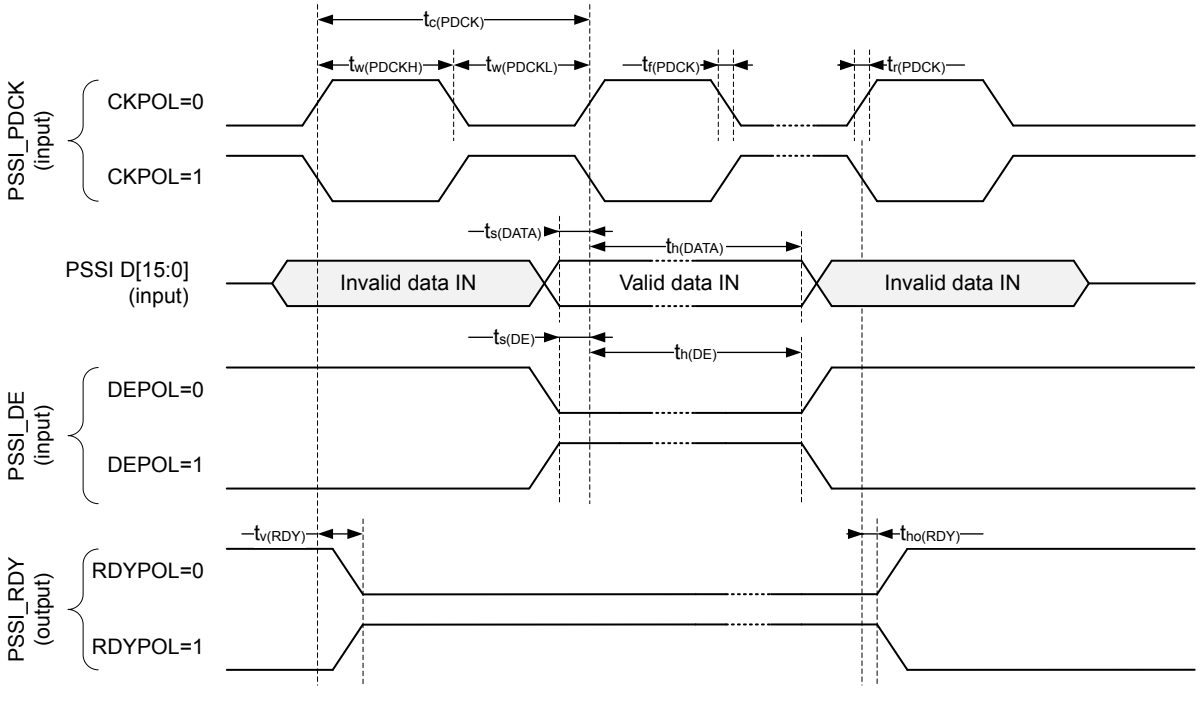


Table 87. PSSI receive characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
clock_ratio	Frequency ratio DCMI_PDCK/f_{HCLK}	-	-	-	0.4	-
PSSI_PDCK	PSSI clock input	-	-	-	80	MHz
D_{PIXEL}	PSSI clock input duty cycle	-	30	-	70	%
$t_{SU(DATA)}$	Data input setup time	-	3.5	-	-	ns
$t_{H(DATA)}$	Data input hold time	-	2.5	-	-	
$t_{SU(DE)}$	DE input setup time	-	1.5	-	-	
$t_{H(DE)}$	DE input hold time	-	2.5	-	-	
$t_{OV(RDY)}$	RDY output valid time	-	-	-	11.5	
$t_{OH(RDY)}$	RDY output hold time	-	8	-	-	

Figure 39. **PSSI receive timing diagram**



5.3.33 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in Table 88. LTDC characteristicsTable 88 for the LTDC interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- LCD_CLK polarity: low (signals change on CLK rising edge)
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to:
  - LTDC Clock: OSPEEDRy[1:0] = 11
  - Other LTDC signals: OSPEEDRy[1:0] = 01
- Advanced I/O configurations:
  - LTDC Clock: RET = 0, INVCLK = 0, DE = 0, DLYPATH = 0
  - Other LTDC signals: RET = 1, INVCLK = 0, DE = 0, DLYPATH = 0
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 88. **LTDC characteristics**

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CLK}	LTDC clock output frequency	C = 20 pF	-	-	148.5	MHz
		C = 30 pF	-	-	120	
D_{CLK}	LTDC clock output duty cycle	-	45	-	55	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CLKH)}$, $t_{w(CLKL)}$	Clock high time, low time	-	$t_{w(CLK)}$ / 2 - 0.5	-	$t_{w(CLK)}$ / 2 + 0.5	ns
$t_{v(DATA)}$	Data output valid time	-	-	-	4	
$t_{h(DATA)}$	Data output hold time	-	1	-	-	
$t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$	HSYNC/VSYNC/DE output valid time	-	-	-	3.5	
$t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$	HSYNC / VSYNC / DE output hold time	-	0.5	-	-	

Figure 40. LCD-TFT horizontal timing diagram

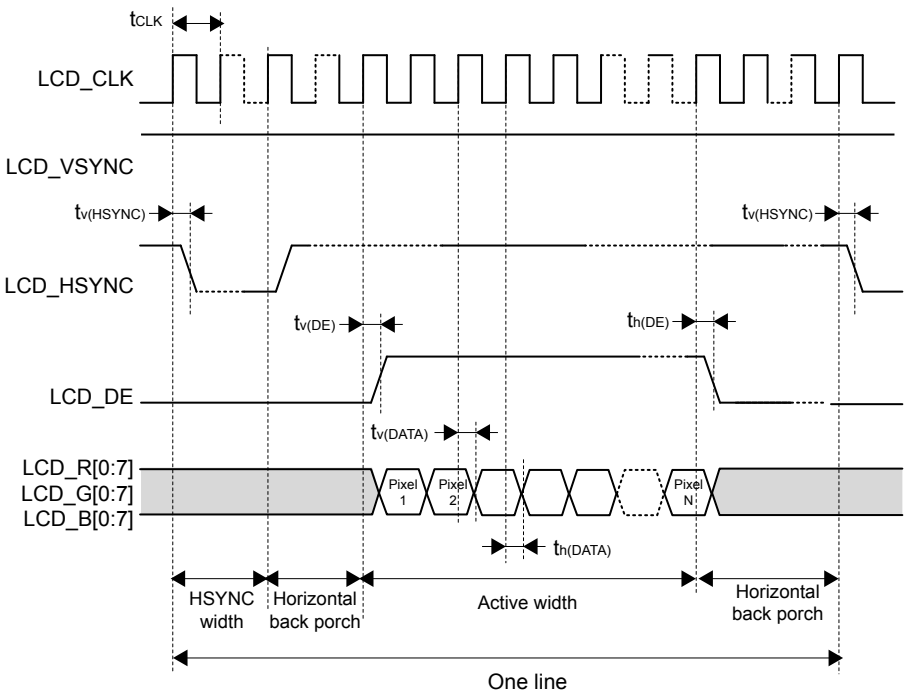
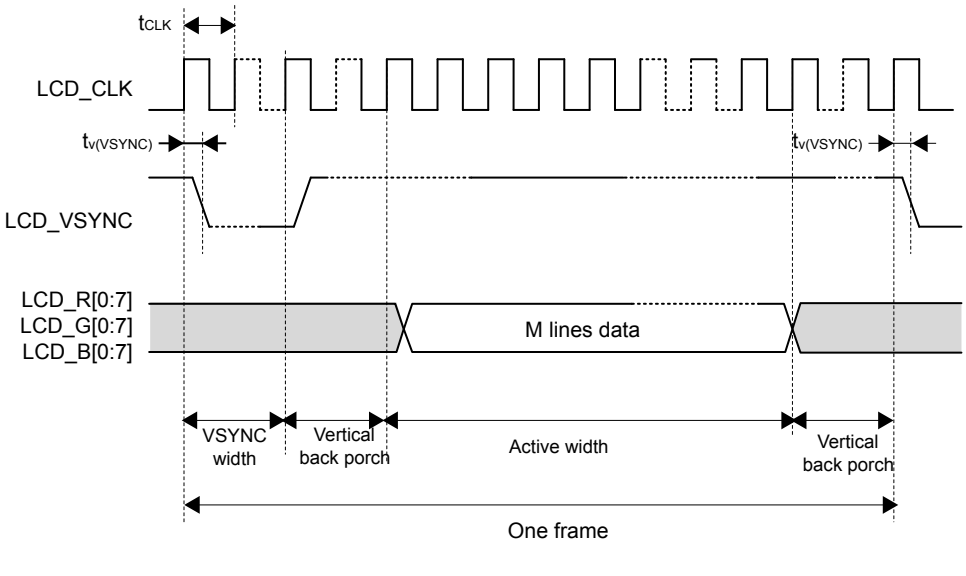


Figure 41. **LCD-TFT vertical timing diagram**



5.3.34 Timer characteristics

The parameters given in Table 89 are specified by design, not tested in production.

Refer to Section 5.3.16: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 89. **TIMx characteristics**

TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
Specified by design, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	1	-	$t_{TIMxCLK}$
$f_{TIMxCLK}$	Timer kernel clock	0	200	MHz
f_{EXT}	Timer external clock frequency on CH1 to CH4	0	$f_{TIMxCLK}$ / 2	
Res_{TIM}	Timer resolution	-	16	bit
	Timer resolution (TIM2 to TIM5)	-	32	
t_{MAX_COUNT}	Maximum possible count with 16-bit counters	-	65536	$t_{TIMxCLK}$
	Maximum possible count with 32-bit counter (TIM2 to TIM5)	-	65536 × 65536	

Table 90. **LPTIMx characteristics**

LPTIMx is used as a general term to refer to the LPTIM1 to LPTIM5 timers.
Specified by design, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{res(LPTIM)}$	Timer resolution time	1	-	$t_{LPTIMxCLK}$
$f_{LPTIMxCLK}$	Timer kernel clock	0	100	MHz
	Timer kernel clock (autonomous mode)	0	32768	Hz
f_{EXT}	Timer external clock frequency on IN1 and IN2	0	$f_{LPTIMxCLK/2}$	MHz
Res_{LPTIM}	Timer resolution	-	16	bit
t_{MAX_COUNT}	Maximum possible count	-	65536	$t_{LPTIMxCLK}$

5.3.35 Communications interfaces

5.3.35.1 *I2C interface characteristics*

The I2C interface meets the timings requirements of the I^2C-bus specification for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are specified by design, not tested in production when the I2C peripheral is properly configured (refer to product reference manual).

The SDA and SCL I/O requirements are met with the following restriction:

- The SDA and SCL I/O pins are not "true" open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

Table 91. I2C analog filter characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbols	Parameters	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes that are suppressed by the analog filter	50(1)	260(2)	ns

1. *Spikes with widths below t_{AF}(min) are filtered. At T_J = -40 °C, the guaranteed minimum is 40 ns.*
2. *Spikes with widths above t_{AF}(max) are not filtered.*

5.3.35.2 *I3C interface characteristics*

The I3C timings are in line with timings requirements of the MIPI® I3C specification v1.1, except for the one given in Table 92. This can be mitigated by increasing the corresponding SCL low duration in the I3C_TIMINGR0 register. For further details, refer to AN5879.

The I3C peripheral supports:

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

Unless otherwise specified, the parameters given in Table 92 for the I3C interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- I/O compensation cell enabled
- VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V

Table 92. I3C specific timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SU_OD}	SDA data setup time during Open-Drain mode	Controller	26	-	-	ns

Table 93. I3C pin characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$R_{PU(I3C)}$	I3C pull-up	1600	2200	2800	Ω
$R_{HK(I3C)}$	I3C high keeper (weak pull-up)	125	160	195	kΩ

5.3.35.3 *SPI interface characteristics*

Unless otherwise specified, the parameters given in Table 94 for the SPI interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when V_{DDx} ≤ 2.7 V

Refer to Section 5.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 94. SPI characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $T_{c(SCK)} = 1/f_{SCK}$	SPI clock frequency	Master mode 1.71 V < V_{DD} < 1.89 V	-	-	115	MHz
		Master mode 3.0 V < V_{DD} < 3.6 V	-	-	105	
		Slave receiver mode	-	-	100	
		Slave mode transmitter/full duplex	-	-	41.5(1)	
$t_{su(NSS)}$	NSS setup time	Slave mode	4	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	1	-	-	
$t_{w(SCKH)}$, $t_{w(SCKL)}$	SCK high and low time	Master mode	$T_{c(SCK)}$ - 1	$T_{c(SCK)}$	$T_{c(SCK)}$ + 1	
$t_{su(MI)}$	Data input setup time	Master mode	4.5	-	-	
$t_{su(SI)}$		Slave mode	3	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	1	-	-	
$t_{h(SI)}$		Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	6.5	13	13.5	
$t_{dis(SO)}$	Data output disable time	Slave mode	12.5	14.5	17.5	
$t_{v(MO)}$	Data output valid time	Master mode	-	3	3.5	
$t_{v(SO)}$		Slave mode	-	11.5	12	
$t_{h(MO)}$	Data output hold time	Master mode	2	-	-	
$t_{h(SO)}$		Slave mode	10	-	-	

1. *Maximum frequency in slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which must fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%.*

Figure 42. **SPI timing diagram - master mode**

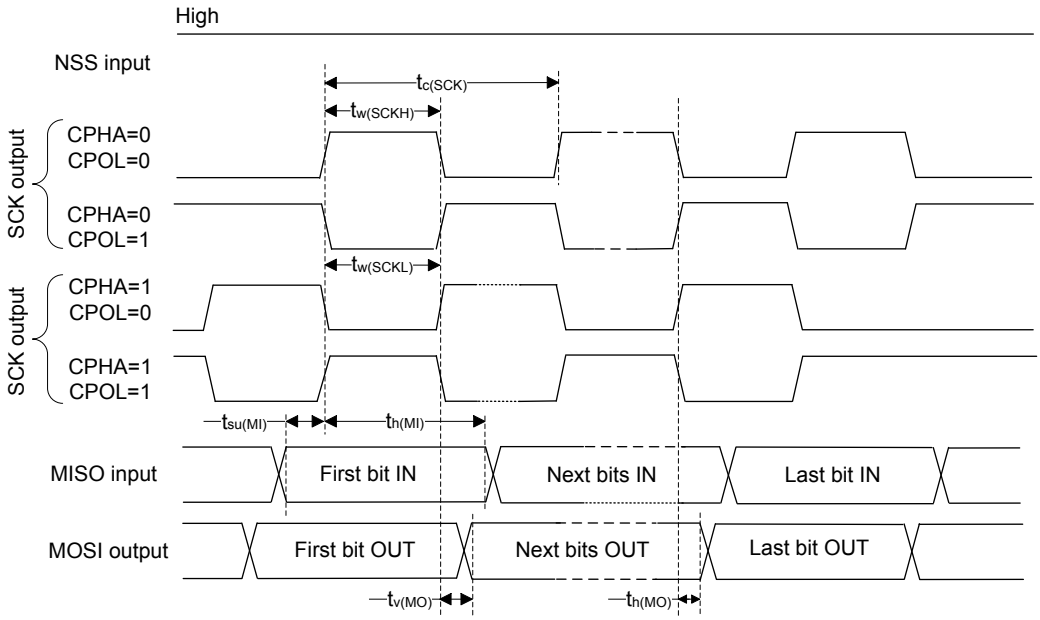


Figure 43. **SPI timing diagram - slave mode and CPHA = 0**

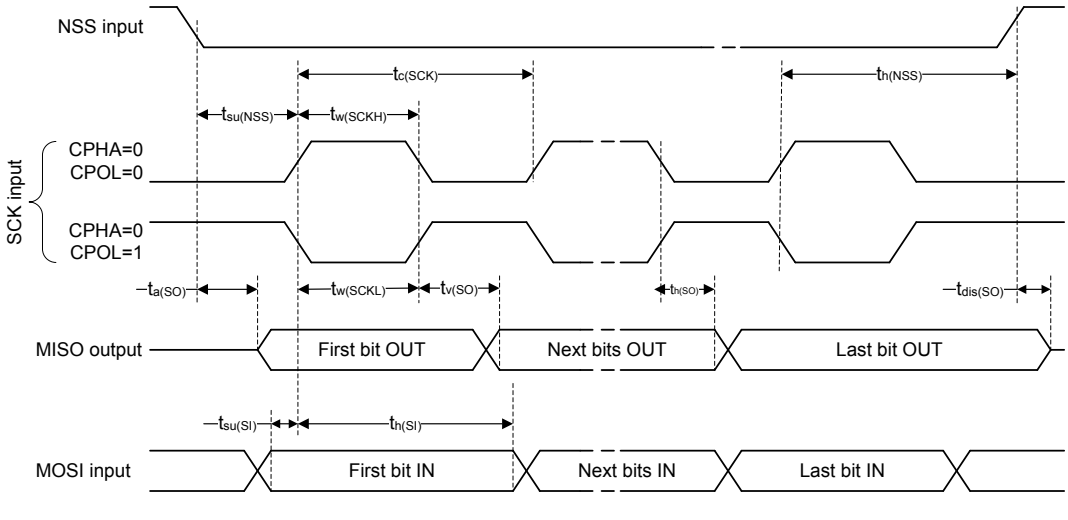
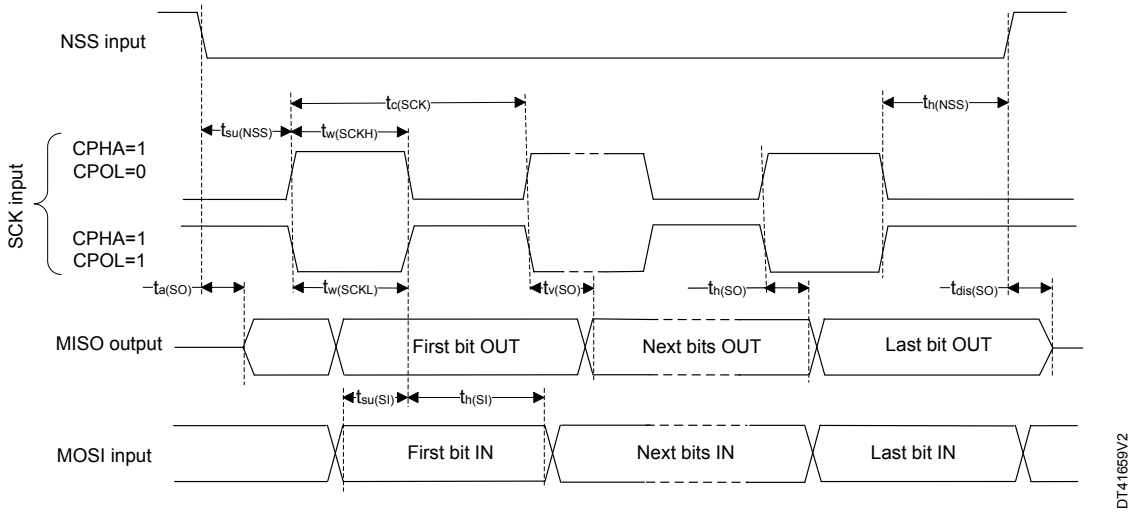


Figure 44. **SPI timing diagram - slave mode and CPHA = 1**



5.3.35.4 *I2S interface characteristics*

Unless otherwise specified, the parameters given in Table 95 for the I2S interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 01
- Capacitive load C= 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when V_{DD} ≤ 2.7 V

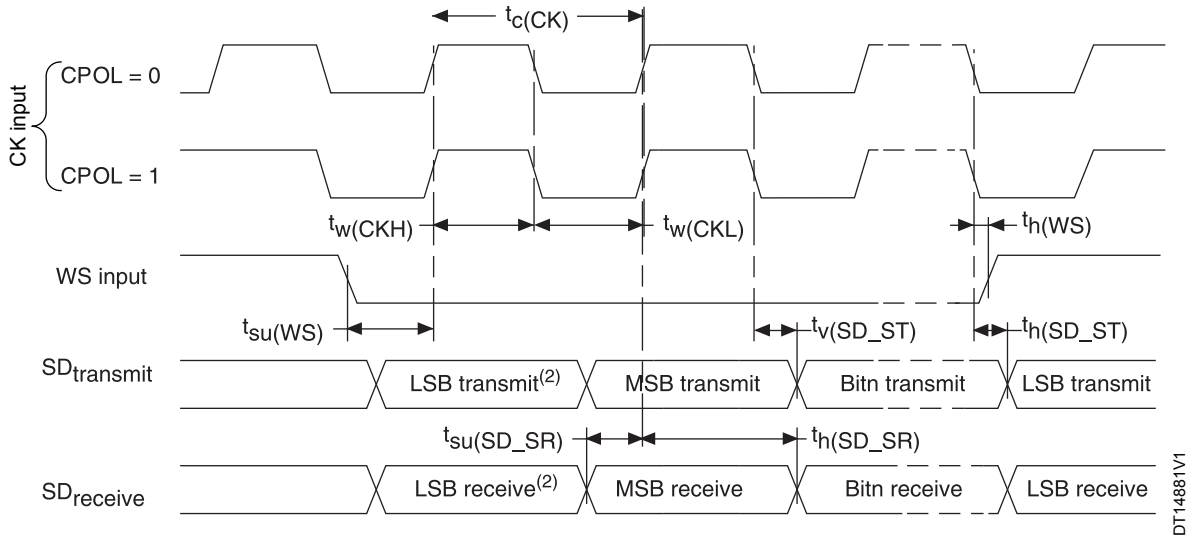
Refer to Section 5.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 95. **I2S characteristics**

Evaluated by characterization, not tested in production unless otherwise specified.

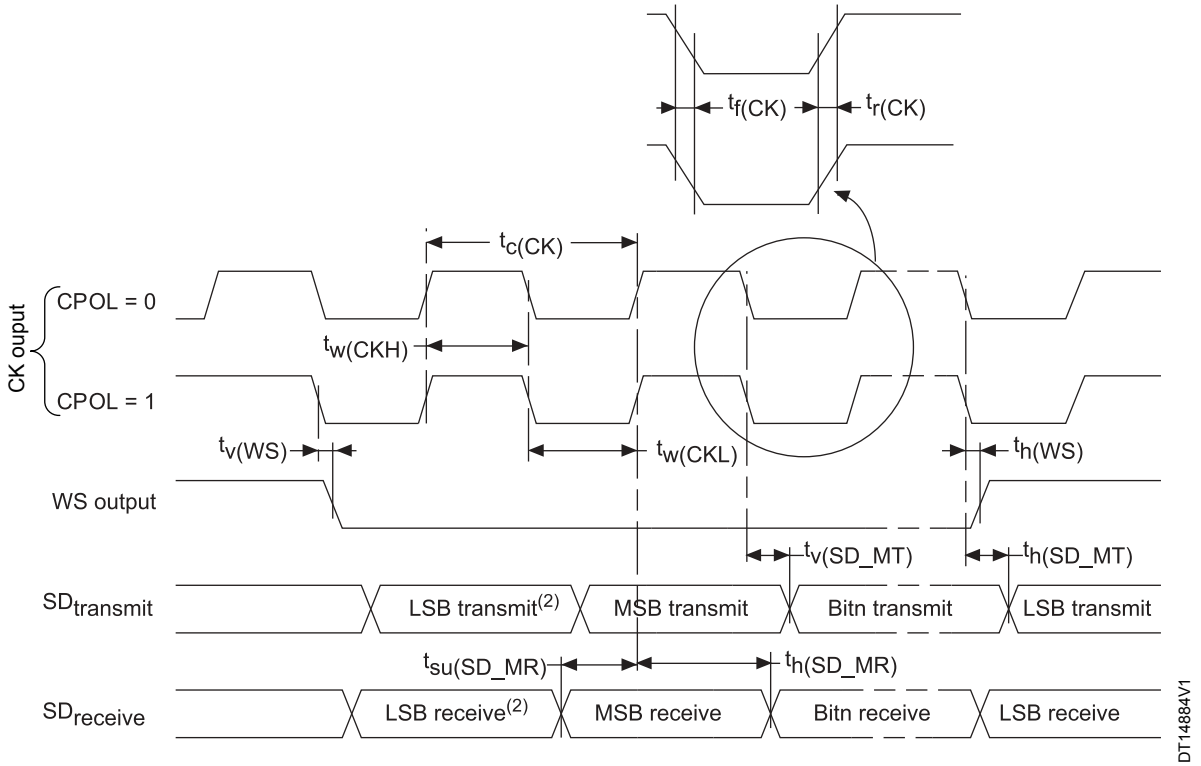
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S main clock output	-	-	50	MHz
f_{CK}	I2S clock frequency	Controller mode	-	50	MHz
		Target transmitter mode	-	23	
		Target receiver mode	-	50	
$t_{v(WS)}$	WS valid time	Controller mode	-	3.5	ns
$t_{h(WS)}$	WS hold time	Controller mode	2.5	-	
$t_{su(WS)}$	WS setup time	Target mode	3.5	-	
$t_{h(WS)}$	WS hold time	Target mode	3	-	
$t_{su(SD\_MR)}$	Data input setup time	Controller receiver	4	-	
$t_{su(SD\_SR)}$		Target receiver	3	-	
$t_{h(SD\_MR)}$	Data input hold time	Controller receiver	2.5	-	
$t_{h(SD\_SR)}$		Target receiver	1.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Target transmitter (after enable edge)	-	13	
$t_{h(SD\_ST)}$	Data output valid time	Controller transmitter (after enable edge)	8.5	-	

Figure 45. I2S target timing diagram (Philips protocol)



1. *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*

Figure 46. I2S controller timing diagram (Philips protocol)



1. *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*

5.3.35.5 *SAI interface characteristics*

Unless otherwise specified, the parameters given in Table 96 for SAI are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10

- Capacitive load C = 30 pF
- Measurement points are performed at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when V_{DDx} ≤ 2.7 V

Refer to Section 5.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (SCK, SD, WS).

Table 96. SAI characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCK}	SAI main clock output	-	-	-	50	MHz
f_{CK}	SAI bit clock frequency(1)	Master transmitter	-	-	38	MHz
		Master receiver	-	-	34	
		Slave transmitter	-	-	40	
		Slave receiver	-	-	50	
$t_{v(FS)}$	FS valid time	Master mode	-	-	13	ns
$t_{su(FS)}$	FS setup time	Slave mode	9	-	-	
$t_{h(FS)}$	FS hold time	Master mode	5.5	-	-	
		Slave mode	1	-	-	
$t_{su(SD\_A\_MR)}$	Data input setup time	Master receiver	5.5	-	-	
$t_{su(SD\_B\_SR)}$		Slave receiver	5.5	-	-	
$t_{h(SD\_A\_MR)}$	Data input hold time	Master receiver	1	-	-	
$t_{h(SD\_B\_SR)}$		Slave receiver	1	-	-	
$t_{v(SD\_B\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	-	12.5	
$t_{h(SD\_B\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8	-	-	
$t_{v(SD\_A\_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	-	12.5	
$t_{h(SD\_A\_MT)}$	Data output hold time	Master transmitter (after enable edge)	8.5	-	-	

1. *APB clock frequency must be at least twice SAI clock frequency.*

Figure 47. SAI master timing waveforms

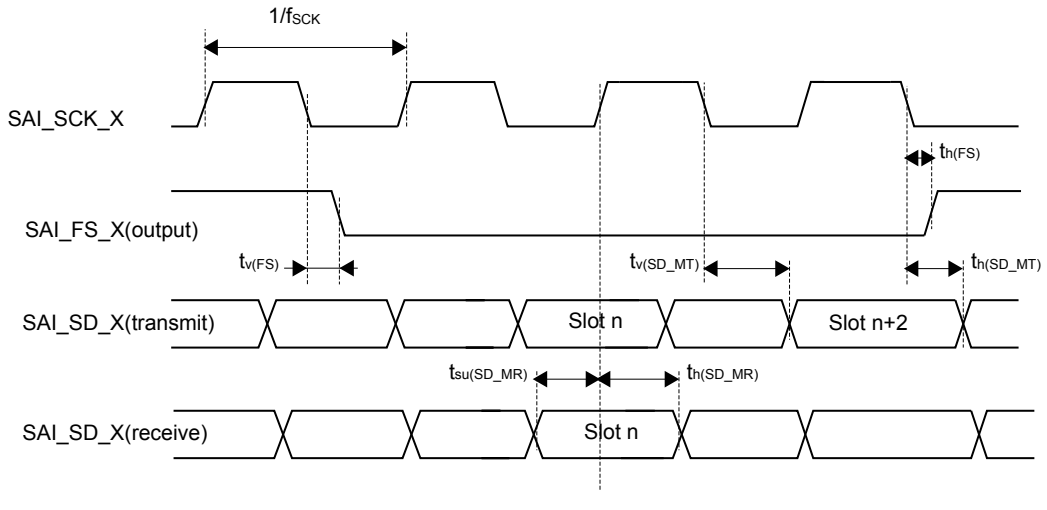
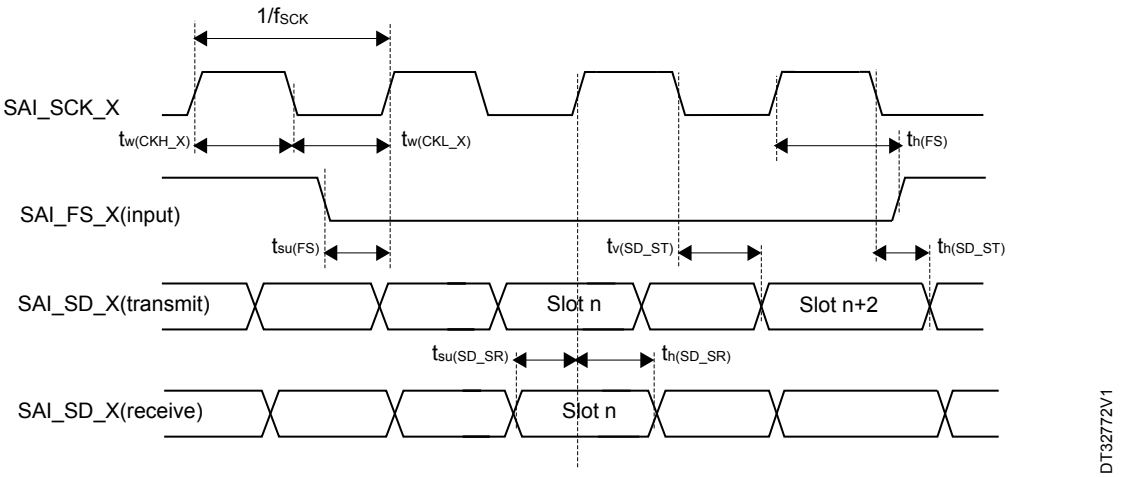


Figure 48. SAI slave timing waveforms



5.3.35.6 *SD/SDIO MMC card host interface (SDMMC) characteristics*

Unless otherwise specified, the parameters given in Table 97 for the SDIO/MMC interface are derived from tests performed under the ambient temperature, frequency and supply voltage conditions summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set as table below
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell disabled, with RAPSRC = 8 and RANSRC = 7
- VDDxVRSEL activated when V_{DDx} ≤ 2.7 V

Refer to Section 5.3.16: I/O port characteristics for more details on the input/output characteristics.

Table 97. SDMMC GPIO OSPEEDR settings for timing measurements

Voltage range (V)	Max clock frequency (MHz)	OSPEEDRy[1:0]	
		Clock	Data
1.71 - 1.89 and 2.7 - 3.6	26/25	00	00
	52/50	01	00
	DDR 52/50	01	01
	100	01	00
2.7 - 3.6	120	11	10
1.71 - 1.89	166	11	10

Table 98. SDMMC characteristics for SD-Card or SDIO usage

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	V_{DDIOx} = 2.7 V to 3.6 V	0	-	120	MHz
		V_{DDIOx} = 1.71 V to 1.89 V	0	-	166	
clock_ratio	SDMMC_CK / f_{pclk} frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 52 MHz	8.5	9.5	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in High-Speed/SDR/DDR mode(1)						
t_{ISU}	Input setup time HS	-	4	-	-	ns
t_{IH}	Input hold time HS	-	2	-	-	
t_{IDW}(2)	Input valid window (variable window)	-	4.5	-	-	
CMD, D outputs (referenced to CK) in high-speed/SDR/DDR mode(1)						
t_{OV}	Output valid time HS	-	-	7.5	8	ns
t_{OH}	Output hold time HS	-	4.5	-	-	
CMD, D inputs (referenced to CK) in default mode						
t_{ISUD}	Input setup time SD	-	4	-	-	ns
t_{IHD}	Input hold time SD	-	2	-	-	
CMD, D outputs (referenced to CK) in default mode						
t_{OVD}	Output valid default time SD	-	-	1	2	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. *SD-Card 3 V / 1.8 V support on SDMMC3 requires an external voltage translator for which timings must be considered.*
2. *The minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

Table 99. SDMMC characteristics for e•MMC usage

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	V_{DDIOx} = 2.7 V to 3.6 V	0	-	120	MHz
		V_{DDIOx} = 1.71 V to 1.89 V	0	-	166	
clock_ratio	SDMMC_CK/f_{pclk} frequency ratio	-	-	-	8/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 52 MHz	8.5	9.5	-	ns
$t_{W(CKH)}$	Clock high time		8.5	9.5	-	
CMD, D inputs (referenced to CK)						
t_{ISU}	Input setup time HS	-	2.5	-	-	ns
t_{IH}	Input hold time HS	-	2	-	-	
t_{IDW}(1)	Input valid window (variable window)	-	4	-	-	
CMD, D outputs (referenced to CK)						
t_{OV}	Output valid time HS	-	-	7.5	8	ns
t_{OH}	Output hold time HS	-	4.5	-	-	

1. *The minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

Figure 49. SD high-speed mode

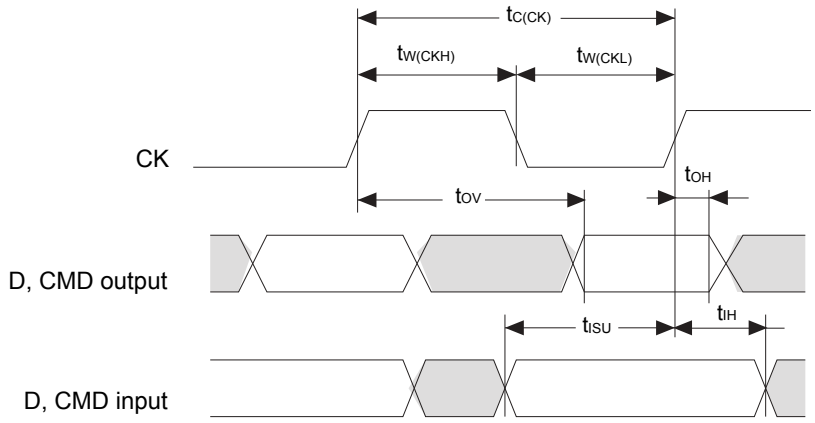


Figure 50. SD default mode

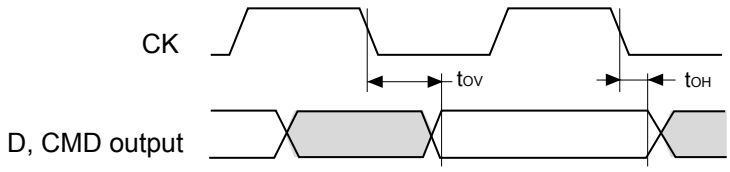
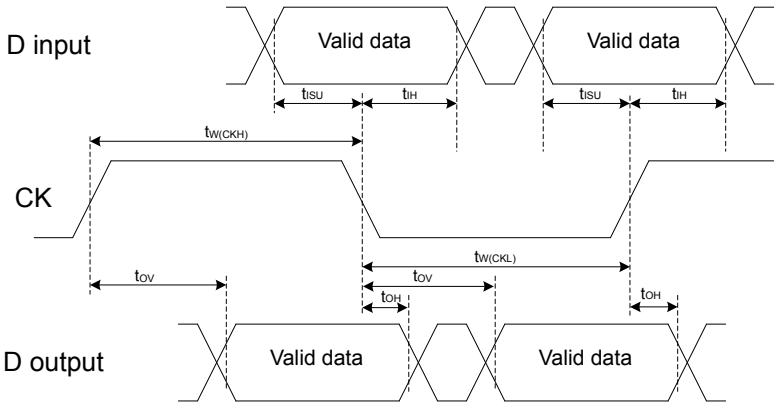


Figure 51. SDMMC DDR mode



5.3.35.7 *Ethernet (ETH) characteristics*

Unless otherwise specified, the parameters given in Table 102, Table 103, Table 104 and Table 105 for MDIO/SMA, RMII, GMII, RGMII and MII are derived from tests performed under the ambient temperature, F_{axiss_ck} frequency summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to:

Table 100. Output speed settings

Mode	OSPEEDRy[1:0]
RGMII-ID	11
RGMII	11
MII	00
RMII	00
MDIO/SMA	11

- Capacitive load C = 20 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}.
- I/O compensation cell disabled, with RAPSRC = 8 and RANSRC = 7.
- VDDxVRSEL activated when VDDx ≤ 2.7 V.

Refer to Section 5.3.16: I/O port characteristics for more details on the input/output characteristics.

Table 102 gives the list of Ethernet MAC timings for the MDIO/SMA and Figure 52 shows the corresponding timing diagram.

Table 101. GPIO advance configuration settings used for RGMII and RGMII-ID characterization

Interface	Mode	Signals	GPIOx_ADVCFGR bits				GPIOxDELAY field
			RET	INVCLK	DE	DLYPATH	DLY[3:0]
ETH1 and ETH2	RGMI	ETHx_RGMII_RX_CTL	1	0	1	0	0000
		ETHx_RGMII_RXD[3:0]	1	0	1	0	0000
		ETHx_RGMII_TX_CTL	1	0	1	0	0000
		ETHx_RGMII_TXD[3:0]	1	0	1	0	0000
ETH1 and ETH2	RGMI-ID	ETHx_RGMII_RX_CLK	0	0	0	1	1101
		ETHx_RGMII_GTX_CLK	0	0	0	1	1100
		ETHx_RGMII_RX_CTL	1	0	1	0	0000
		ETHx_RGMII_RXD[3:0]	1	0	1	0	0000
		ETHx_RGMII_TX_CTL	1	0	1	0	0000
		ETHx_RGMII_TXD[3:0]	1	0	1	0	0000

Table 102. Ethernet MAC timings for MDIO/SMA

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (2.5 MHz)	-	-	400	-	ns
$t_{d(MDIO)}$	Write data valid time	-	0	1	2	
$t_{su(MDIO)}$	Read data setup time	-	8	-	-	
$t_{h(MDIO)}$	Read data hold time	-	0	-	-	

Figure 52. Ethernet MDIO/SMA timing diagram

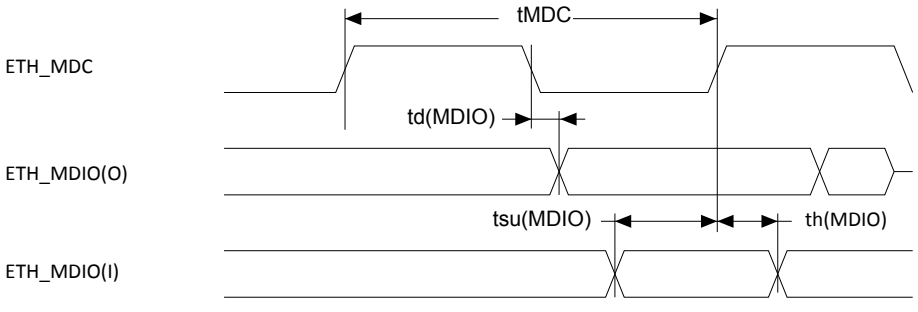


Table 103 gives the list of Ethernet MAC timings for the RMII and Figure 53 shows the corresponding timing diagram.

Table 103. Ethernet MAC timings for RMII

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	-	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	-	1	-	-	
$t_{su(CRS)}$	Carrier sense setup time	-	1	-	-	
$t_{ih(CRS)}$	Carrier sense hold time	-	1	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	-	3.5	6	8	
$t_{d(TXD)}$	Transmit data valid delay time	-	3.5	6	8	

Figure 53. Ethernet RMII timing diagram

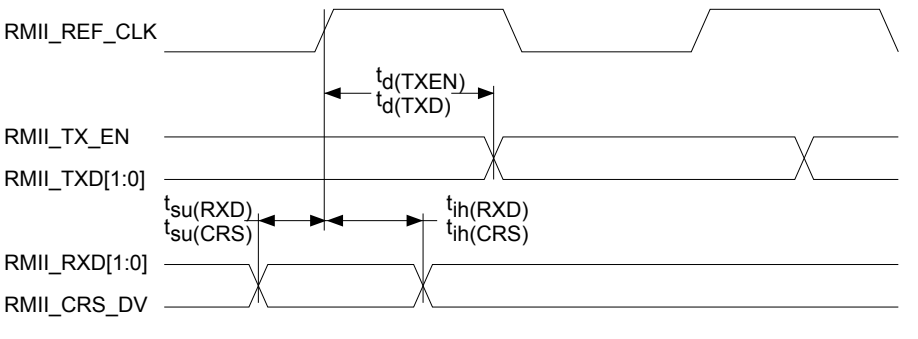


Table 104 gives the list of Ethernet MAC timings for MII and Figure 54 shows the corresponding timing diagram.

Table 104. Ethernet MAC timings for MII

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	-	2	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	-	2	-	-	
$t_{su(DV)}$	Data valid setup time	-	2	-	-	
$t_{ih(DV)}$	Data valid hold time	-	2	-	-	
$t_{su(ER)}$	Error setup time	-	2	-	-	
$t_{ih(ER)}$	Error hold time	-	2	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	-	3.5	6.5	8	
$t_{d(TXD)}$	Transmit data valid delay time	-	3.5	6.5	8	

Figure 54. Ethernet MII timing diagram

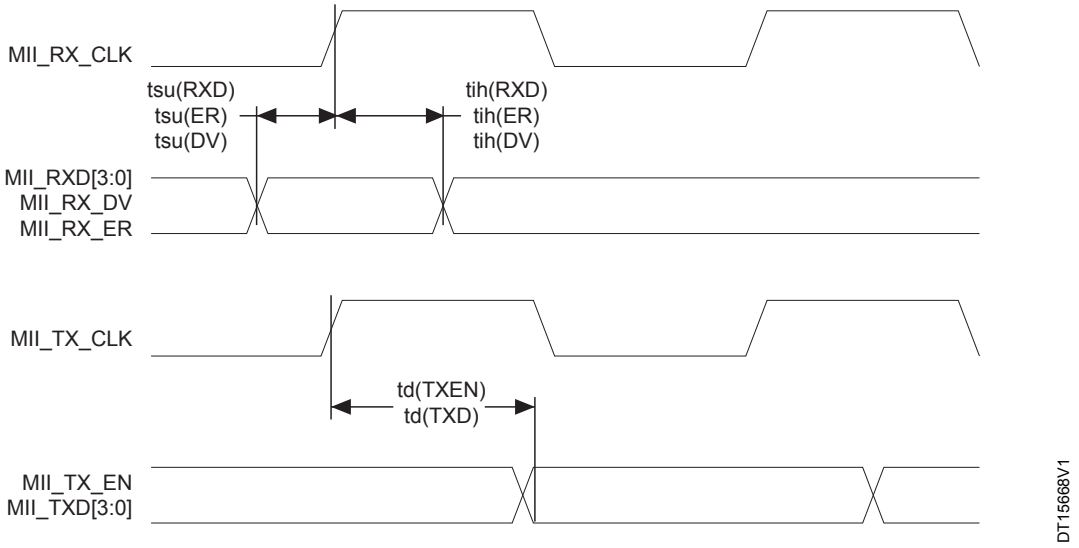


Table 105. Ethernet MAC timings for RGMII

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{cyc}	Clock cycle duration	-	7.9	8	8.1	ns
D_{CLK}	GTX_CLK duty cycle	-	45	-	55	%
$t_{su(RXD)}$	Receive data setup time	-	1(1)	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	-	1(1)	-	-	ns
$t_{su(RX\_CTL)}$	Receive control valid setup time	-	1(1)	-	-	
$t_{ih(RX\_CTL)}$	Receive control valid hold time	-	1(1)	-	-	
$t_{skew(TX\_CTL)}$	Transmit control valid delay time	-	-0.5	0.25	0.5	
$t_{skew(TXD)}$	Transmit data valid delay time	-	-0.5	0.25	0.5	

1. *Test done at 100 MHz with signal rise and fall time < 1.8 ms.*

Figure 55. Ethernet RGMII timing diagram

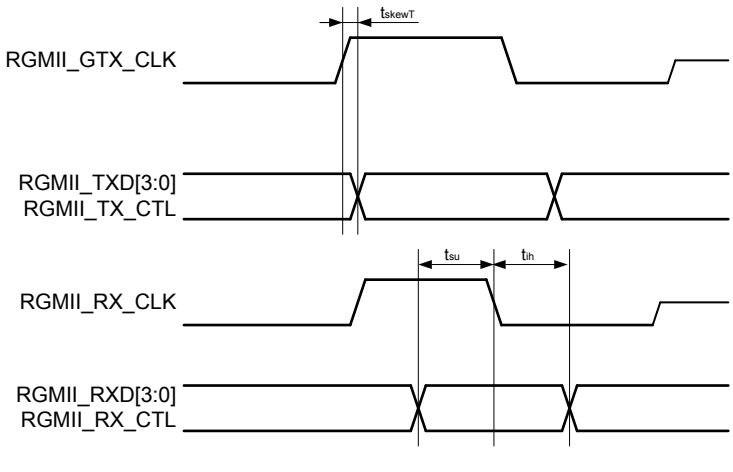


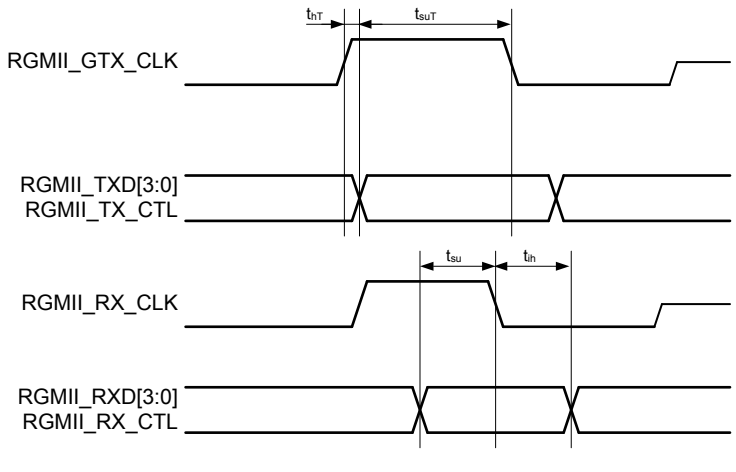
Table 106. Ethernet MAC timings for RGMII_ID

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{cyc}	Clock cycle duration	-	7	8	8	ns
D_{CLK}	GTX_CLK duty cycle	-	45	-	55	%
$t_{su(RXD)}$	Receive data setup time to RX_CLK falling edge	(1)	-1	-	-	ns
$t_{ih(RXD)}$	Receive data hold time from RX_CLK falling edge	(1)	-	-	0.5	
$t_{su(RX\_CTL)}$	Receive control valid setup time to RX_CLK falling edge	(1)	-1	-	-	
$t_{ih(RX\_CTL)}$	Receive control valid hold time from RX_CLK falling edge	(1)	-	-	0.5	
$t_{suT(TX\_CTL)}$	Transmit control valid setup time to GTX_CLK falling edge	-	1.2	-	-	
$t_{suT(TXD)}$	Transmit data valid setup time to GTX_CLK falling edge	-	1.2	-	-	
$t_{hT(TX\_CTL)}$	Transmit control valid hold time from GTX_CLK rising edge	-	1.2	-	-	
$t_{hT(TXD)}$	Transmit data valid hold time from GTX_CLK rising edge	-	1.2	-	-	

1. *Test done at 100 MHz with signal rise and fall time < 1.8 ns.*

Figure 56. Ethernet RGMII-ID timing diagram



5.3.35.8 *USART (SPI mode) interface characteristics*

Unless otherwise specified, the parameters given in Table 107 for USART are derived from tests performed under the ambient temperature, frequency, and supply voltage conditions summarized in Table 107, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- I/O compensation cell enabled
- VDDxVRSEL activated when V_{DDx} ≤ 2.7 V

Refer to Section 5.3.16: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 107. USART (SPI mode) characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	USART clock frequency	SPI master mode	-	-	$1/(8\times t_{ker})$	MHz
					16.5	
		SPI slave mode	-	-	33	
		Slave receiver mode	-	-	$1/(3\times t_{ker})$	
					44	
$t_{su(NSS)}$	NSS setup time	SPI slave mode	t_{ker} + 4(1)	-	-	ns
$t_{h(NSS)}$	NSS hold time	SPI slave mode	1	-	-	ns
$t_{w(CKH)}$, $t_{w(CKL)}$	CK high and low time	SPI master mode	1 / f_{CK} / 2 - 1	1 / f_{CK} / 2	1 / f_{CK} / 2 + 1	ns
$t_{su(RX)}$	Data input setup time	SPI master mode	13	-	-	ns
		SPI slave mode	5	-	-	
$t_{h(RX)}$	Data input hold time	SPI master mode	0	-	-	ns
		SPI slave mode	0.5	-	-	
$t_{v(TX)}$	Data output valid time	SPI slave mode	-	13.5	14	ns
		SPI master mode	-	4	4.5	
$t_{h(TX)}$	Data output hold time	SPI slave mode	7	-	-	ns
		SPI master mode	1	-	-	

1. *t_{ker} is the usart_ker_ck_pres clock period defined in the product reference manual.*

Figure 57. **USART timing diagram in SPI master mode**

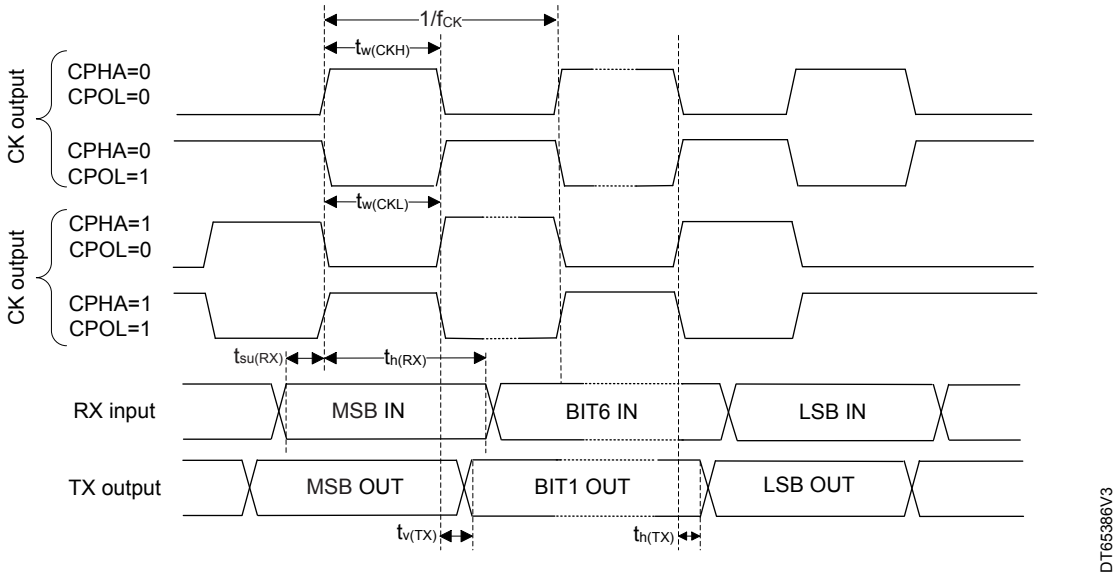
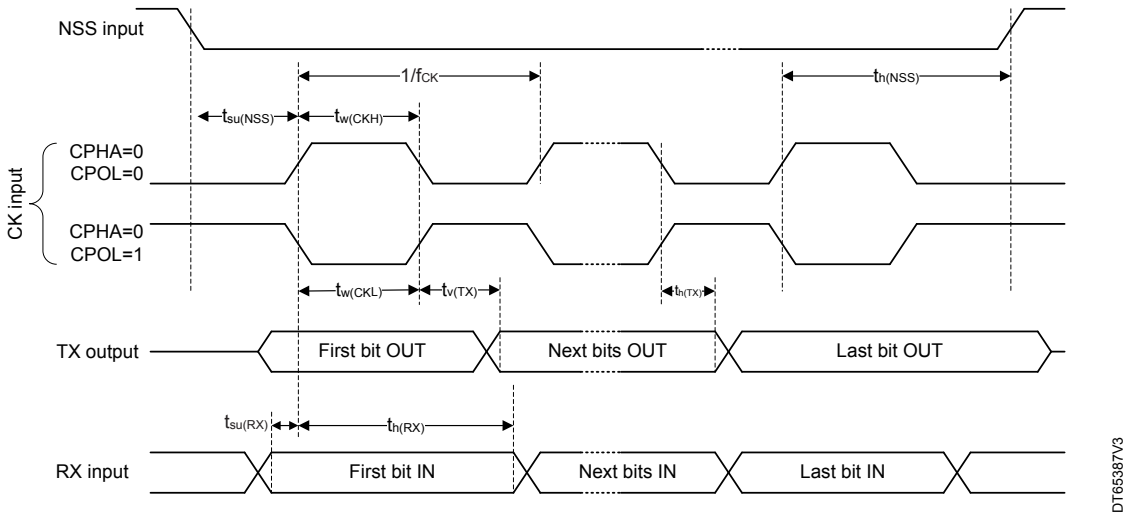


Figure 58. **USART timing diagram in SPI slave mode**



5.3.36 Embedded PHYs characteristics

5.3.36.1 DDR PHY characteristics

Table 108. **DDR PHY characteristics**

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ZQ}	External resistor on DDR_ZQ	-	237.6	240	242.4	Ω
DDR4, 1600 Mbit/s, 16-bit, 10 ACx4, 1 Rank, DBI off						
$I_{VDDCORE(DDRPHY)}$ (1)	Supply current on V_{DDCORE}	Read	-	93.5	155	mA
		Write	-	115	185	
		Idle	-	65	120	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDDCORE(DDRPHY)}$ (1)	Supply current on V_{DDCORE}	DFI_LP	-	22	68.5	mA
		Inactive	-	3.65	68.5	
		Retention(2)	OFF			
$I_{VDDA18DDR}$(1)	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention(2)	OFF			
$I_{VDDQDDR}$(1)	Supply current on V_{DDQDDR}	Read	-	235	275	mA
		Write	-	180	215	
		Idle	-	37	43	
		DFI_LP	-	1.9	3.6	
		Inactive	-	0.12	1.35	
		Retention(2)	-	0.017	1.2	
DDR3L, 1600 Mbit/s, 16-bit, 10 ACx4, 1 Rank						
$I_{VDDCORE(DDRPHY)}$ (1)	Supply current on V_{DDCORE}	Read	-	88.5	140	mA
		Write	-	110	170	
		Idle	-	62.5	110	
		DFI_LP	-	21	61	
		Inactive	-	3.6	58.5	
		Retention(2)	OFF			
$I_{VDDA18DDR}$(1)	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention(2)	OFF			
$I_{VDDQDDR}$(1)	Supply current on V_{DDQDDR}	Read	-	245	275	mA
		Write	-	270	305	
		Idle	-	39.5	44.5	
		DFI_LP	-	2.15	3.85	
		Inactive	-	0.135	1.4	
		Retention(2)	-	0.0225	1.2	
LPDDR4, 1600 Mbit/s, 16-bit, 10 ACx4, 1 Rank, DBI off						
$I_{VDDCORE(DDRPHY)}$ (1)	Supply current on V_{DDCORE}	Read	-	91	160	mA
		Write	-	110	180	
		Idle	-	59.5	115	
		DFI_LP	-	22	69	
		Inactive	-	3.65	69.5	
		Retention(2)	OFF			

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDDA18DDR}$(1)	Supply current on $V_{DDA18DDR}$	Read	-	4.3	-	mA
		Write	-	4.3	-	
		Idle	-	4.3	-	
		DFI_LP	-	4.3	-	
		Inactive	-	0.12	0.16	
		Retention(2)	OFF			
$I_{VDDQDDR}$(1)	Supply current on V_{DDQDDR}	Read	-	110	125	mA
		Write	-	285	325	
		Idle	-	48.5	56	
		DFI_LP	-	1.7	3.2	
		Inactive	-	0.11	1.25	
		Retention(2)	-	0.0185	1.1	
Low-power exit latency						
t_{EXIT}	Exit latency from DFI_LP state	-	-	2	-	DFI_CLK
	Exit latency from inactive state	DDR3L, DDR4	-	3	-	µs
		LPDDR4	-	3 + 2560 DDR_CLK	-	
	Exit latency from retention state after supplies restored	DDR3L, DDR4	-	3	-	
		LPDDR4	-	3 + 2560 DDR_CLK	-	

1. *Evaluated by characterization, not tested in production.*
2. *V_{DDCORE} OFF, $V_{DDA18DDR}$ OFF.*

5.3.36.2 CSI PHY characteristics

Table 109. CSI PHY characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{EXT}	External resistor on REXT	Connected to ground		198	200	202	Ω
$I_{VDDCORE(CSIPHY)}$(1)	Supply current on V_{DDCORE}	High-speed receive(2)	2 lanes at 1 Gbit/s	-	2.1	12	mA
			2 lanes at 1.5 Gbit/s	-	3	13	
			2 lanes at 2 Gbit/s	-	3.9	14.5	
			2 lanes at 2.5 Gbit/s	-	4.8	15.5	
		LP receive	Lane 0 at 10 Mbit/s	-	0.4	8	
		ULPS receive	ck_ker_csi2phy stopped	-	0.06	8.4	
$I_{VDDA18CSI}$(1)	Supply current on $V_{DDA18CSI}$	High-speed receive(2)	2 lanes at 1 Gbit/s	-	2.1	2.7	mA
			2 lanes at 1.5 Gbit/s	-	2.25	2.8	
			2 lanes at 2 Gbit/s	-	2.55	3.1	
			2 lanes at 2.5 Gbit/s	-	2.55	3.1	
		LP receive	Lane 0 at 10 Mbit/s	-	1.7	2.15	
		ULPS receive	ck_ker_csi2phy stopped	-	0.015	0.1	
I_{VDDCSI}(1)	Supply current on V_{DDCSI}	High-speed receive(2)	2 lanes at 1 Gbit/s	-	3.75	4.8	mA
			2 lanes at 1.5 Gbit/s	-	4.3	5.4	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{VDDCSI}[1]	Supply current on V_{DDCSI}	High-speed receive[2]	2 lanes at 2 Gbit/s	-	3.8	5.5	mA
			2 lanes at 2.5 Gbit/s	-	4.3	6	
		LP receive	Lane 0 at 10 Mbit/s	-	0.9	1.5	
		ULPS receive	ck_ker_csi2phy stopped	-	0.04	0.6	

1. *Evaluated by characterization, not tested in production.*
2. *HS mode: assume PRBS9 pattern on data lanes and 100% occupation; that is, continuous HS.*

5.3.36.3 USB2PHY characteristics

Table 110. USB high-speed PHY characteristics

Specified by design, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{TXRTUNE}$	External resistor on TXRTUNE	Connected to ground		198	200	202	Ω
$I_{VDDCORE(USB2PHY)}$[1]	Supply current on V_{DDCORE}	HS transmit, maximum transition density[2]		-	10	27	mA
		HS transmit, minimum transition density[3]		-	8.15	23.5	
		HS Idle[4]		-	9.25	23	
		FS transmit, maximum transition density[5]		-	9.2	27.5	
		LS transmit, maximum transition density[6]		-	7.85	20	
		Suspend[7]		-	0.038	6.05	
		Sleep[8]		-	2.45	13	
		Battery charging	VDATDETENB = 0, VDATSRCENB = 1[9]	-	2.4	11.5	
			VDATDETENB = 1, VDATSRCENB = 1	-	4.75	15.5	
$I_{VDDA18USB}$[1]	Supply current on $V_{DDA1V8USB}$	HS transmit, maximum transition density[2]		-	16.5	18.5	mA
		HS transmit, minimum transition density[3]		-	14.5	15.5	
		HS idle[4]		-	4.9	5.85	
		FS Transmit, maximum transition density[5]		-	4.9	5.9	
		LS Transmit, maximum transition density[6]		-	5.1	6.15	
		Suspend[7]		-	0.024	0.0945	
		Sleep[8]		-	0.031	0.0945	
		Battery charging	VDATDETENB = 0, VDATSRCENB = 1[9]	-	3.55	4.55	
			VDATDETENB = 1, VDATSRCENB = 1	-	4.3	5.4	
$I_{VDD33USB}$[1]	Supply current on $V_{DD33USB}$	HS transmit, maximum transition density[2]		-	3.05	3.2	mA
		HS transmit, minimum transition density[3]		-	2.2	2.55	
		HS idle[4]		-	2.1	2.4	
		FS transmit, maximum transition density[5]		-	12.5	16	
		LS transmit, maximum transition density[6]		-	12	16.5	
		Suspend[7]		-	0.029	0.0785	
		Sleep[8]		-	0.067	0.115	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{VDD33USB}$(1)	Supply current on $V_{DD33USB}$	Battery charging	VDATDETENB = 0, VDATSRCENB = 1(9)	-	2.1	2.4	mA
			VDATDETENB = 1, VDATSRCENB = 1	-	2.1	2.4	

1. *Evaluated by characterization, not tested in production.*
2. *Packet transmission by one transceiver operating in device mode while driving all 0's data (constant JKJK on DP/DM). Loading of 10 pF. Transfers do not include any interpacket delay.*
3. *Packet transmission by one transceiver operating in device mode while driving all 1's data (alternating 7-bit strings of J, then K on DP/DM). Loading of 10 pF. Transfers do not include any interpacket delay.*
4. *HS receive mode with no traffic on the line.*
5. *Packet transmission by one transceiver operating in device mode while driving all 0's data (constant JKJK on DP/DM). Loading of 50 pF. Transfers do not include any interpacket delay.*
6. *Packet transmission by one transceiver operating in host mode while driving all 0's data (constant JKJK on DP/DM). Loading of 600 pF. Transfers do not include any interpacket delay.*
7. *Suspend when operating in device mode with no far-side host termination on DP/DM during measurements. Measurements taken when COMMONONN (SYSCFG_USB2PHYxCR.USB2PHYxCMN) is deasserted.*
8. *Sleep mode when operating in Device mode with no far-side host termination on DP/DM during measurements.*
9. *PHY is in suspend (with clocks turned OFF), non-driving mode and operating as a portable device in the 'dead battery' condition.*

5.3.37 JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in Table 111 and Table 112 for JTAG/SWD are derived from tests performed under the ambient temperature, frequency and V_{DD} supply voltage summarized in Table 17. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x01
- Capacitive load C = 30 pF
- I/O compensation cell enabled, VDDxVRSEL activated when $V_{DDx} \leq 2.7$ V
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to Section 5.3.16: I/O port characteristics for more details on the input/output characteristics.

Table 111. JTAG dynamic characteristics

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp} $1/t_{c(TCK)}$	TCK clock frequency	(1)	-	-	45	MHz
$t_{isu(TMS)}$	TMS input setup time		2	-	-	ns
$t_{ih(TMS)}$	TMS input hold time		1	-	-	
$t_{isu(TDI)}$	TDI input setup time		3	-	-	
$t_{ih(TDI)}$	TDI input hold time		0.5	-	-	
$t_{ov\ (TDO)}$	TDO output valid time		-	9	11	
$t_{oh(TDO)}$	TDO output hold time		7	-	-	

1. *$1.65\ V < V_{DD} < 3.6\ V$.*

Figure 59. **JTAG timing diagram**

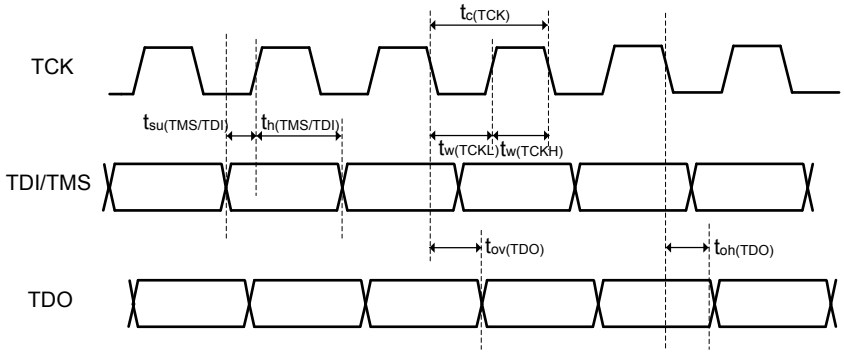


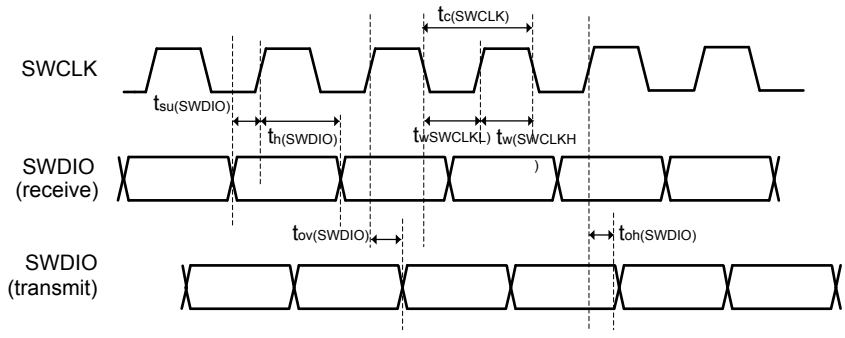
Table 112. **SWD dynamic characteristics**

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{pp} $1/t_{c(SWCLK)}$	SWCLK clock frequency	(1)	-	-	80	MHz
$t_{isu(SWDIO)}$	SWDIO input setup time		1.5	-	-	ns
$t_{ih(SWDIO)}$	SWDIO input hold time		2.5	-	-	
$t_{ov\ (SWDIO)}$	SWDIO output valid time		-	9	12.5	
$t_{oh(SWDIO)}$	SWDIO output hold time		5	-	-	

1. *1.65 V < V_{DD} < 3.6 V.*

Figure 60. **SWD timing diagram**



6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 Device marking

Refer to technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433) available on www.st.com, for the location of pin 1 / ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use.

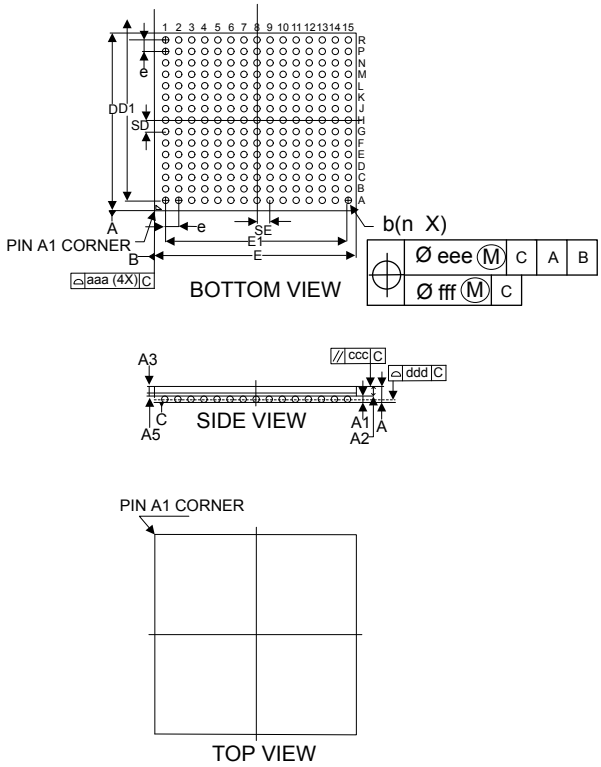
In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

6.2 VFBGA225 package information (B0P6)

This VFBGA is a 225 ball, 8 x 8 mm, 0.5 mm pitch, very fine pitch ball grid array package.

Figure 61. VFBGA225 - Outline



1. Drawing is not to scale.

Table 113. VFBGA225 - Mechanical data

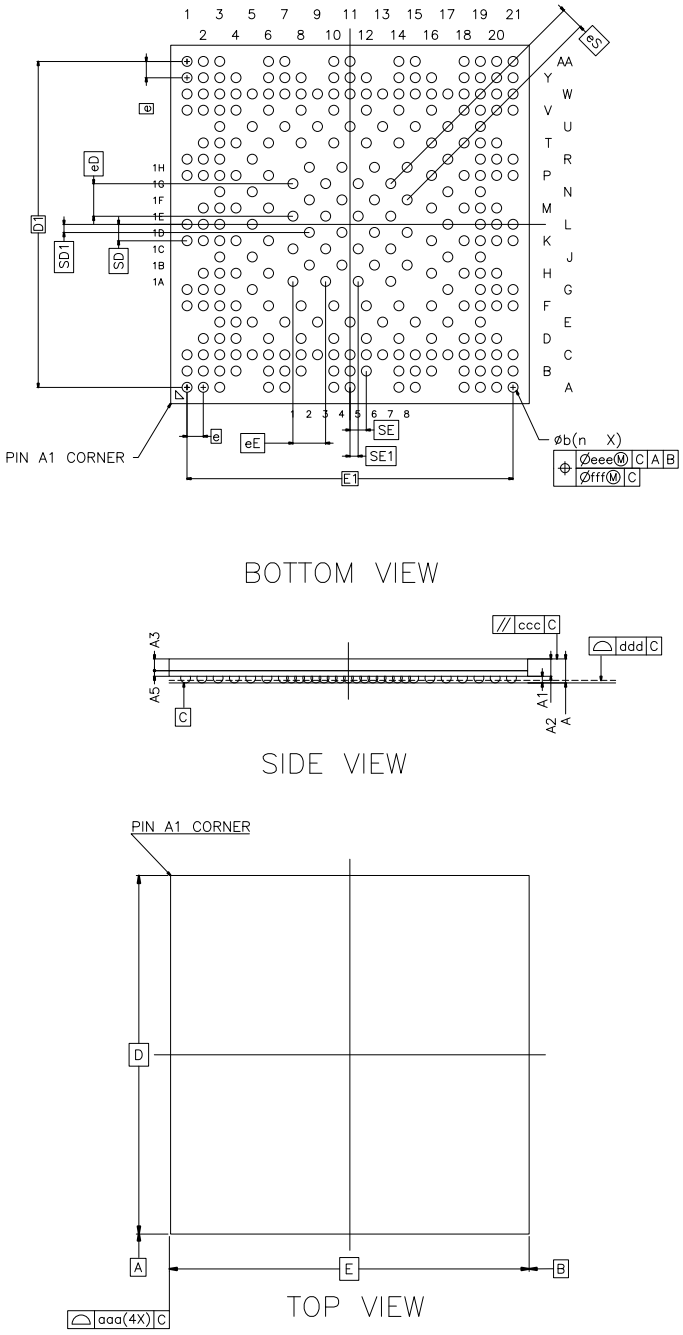
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.00	-	-	0.0394
A1[3]	0.15	-	-	0.0059	-	-
A2	-	0.70	-	-	0.0276	-
b[4]	0.26	0.31	0.36	0.0102	0.0122	0.0142
D[5]		8.00 BSC			0.3150 BSC	
D1[5]		7.00 BSC			0.2756 BSC	
E[5]		8.00 BSC			0.3150 BSC	
E1[5]		7.00 BSC			0.2756 BSC	
e[5][6]		0.50 BSC			0.0197 BSC	
N[7]			225			
SD[5][8]		0.50 BSC			0.0197 BSC	
SE[5][8]		0.50 BSC			0.0197 BSC	
aaa[9]		0.15			0.0059	
ccc[10]		0.20			0.0079	
ddd[11]		0.08			0.0031	
eee[12]		0.15			0.0059	
fff[13]		0.05			0.0020	

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *The total profile height (Dim A) is measured from the seating plane to the top of the component.*
3. *The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to Datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no linear tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.*
6. *e represents the solder balls grid pitch(es).*
7. *N represents the total number of balls.*
8. *Basic dimensions SD & SE are defining the ball matrix position with respect to datums A and B.*
9. *The profile tolerance controlling the location and orientation of the sides of the package.*
10. *The parallelism tolerance controlling the orientation of the top surface of the package with respect to the seating plane, Datum C.*
11. *The profile tolerance controlling the location of the crowns of the balls with respect to Datum C.*
12. *The tolerance of position that controls the location of the pattern of balls with respect to Datum's A and B.*
13. *The tolerance of position that controls the location of the balls within the matrix with respect to each other.*

6.3 VFBGA273 package information (B0P7)

This VFBGA is a 273 ball, 11 x 11 mm, 0.5 mm pitch, very thin fine pitch ball grid package.

Figure 62. **VFBGA273 - Outline**



Note: Drawing is not to scale.

Table 114. **VFBGA273 - Mechanical data**

Symbol	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
A [2][3]	-	-	1.00	-	-	0.0394
A1[4]	0.15	-	-	0.0059	-	-
A2	-	0.70	-	-	0.0276	-

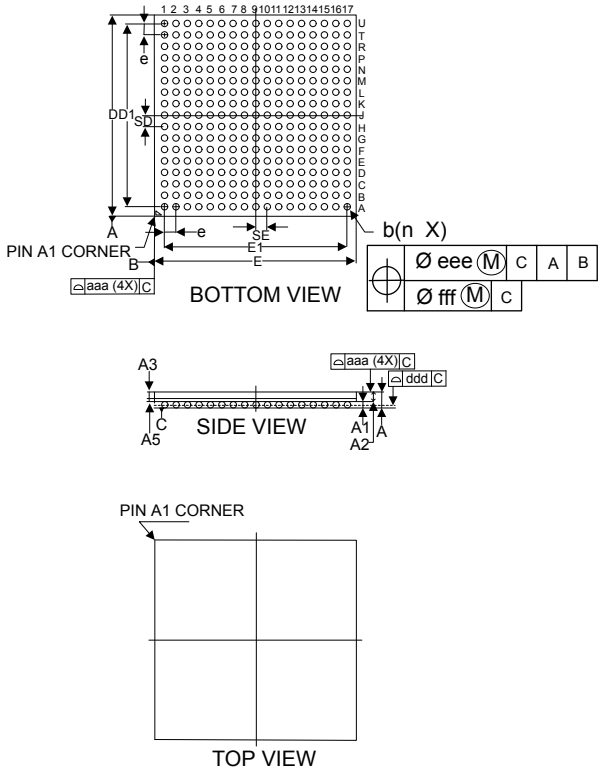
Symbol	Millimeters			Inches[1]		
	Min	Typ	Max	Min	Typ	Max
b[5]	0.26	0.31	0.36	0.0102	0.0122	0.0142
D		11.00 BSC[6]			0.4331	
D1		10.00 BSC			0.3937	
E		11.00 BSC			0.4331	
E1		10.00 BSC			0.3937	
e[7]		0.50 BSC			0.0197	
eD		1.00 BSC			0.0394	
eE		1.00 BSC			0.0394	
eS		0.71 BSC			0.0280	
N[8]		273				
SD[9]		0.50 BSC			0.0197 BSC	
SE[9]		0.50 BSC			0.0197 BSC	
SD1		0.25 BSC			0.0098 BSC	
SE1		0.25 BSC			0.0098 BSC	
aaa[10]		0.15			0.0059	
ccc[10]		0.20			0.0079	
ddd[10]		0.08			0.0031	
eee[10]		0.15			0.0059	
fff[10]		0.05			0.0020	

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *VFBGA stands for very thin fine pitch ball grid array: 0.80 mm < A ≤ 1.00 mm / Fine pitch e < 1.00 mm.*
3. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
4. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
5. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to Datum C.*
6. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no linear tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.*
7. *e represents the solder balls grid pitch(es).*
8. *N represents the total number of balls.*
9. *Basic dimensions SD & SE are defining the ball matrix position with respect to datums A and B.*
10. *Tolerance of form and position.*

6.4 TFBGA289 package information (B0NY)

This TFBGA is a 289 ball, 14x14 mm, 0.8 mm pitch, fine pitch ball grid array package.

Figure 63. TFBGA289 - Outline



B0NY_TFBGA289_ME_V1

1. Drawing is not to scale.

Table 115. **TFBGA289 - Mechanical data**

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.20	-	-	0.0472
A1[3]	0.24	-	-	0.0094	-	-
A2	-	0.70	-	-	0.0276	-
b[4]	0.38	0.43	0.48	0.0150	0.0169	0.0189
D[5]		14.00 BSC			0.5512 BSC	
D1[5]		12.80 BSC			0.5039 BSC	
E[5]		14.00 BSC			0.5512 BSC	
E1[5]		12.80 BSC			0.5039 BSC	
e[5][6]		0.80 BSC			0.0315 BSC	
N[7]			289			
SD[5][8]		0.80 BSC			0.0315 BSC	
SE[5][8]		0.80 BSC			0.0315 BSC	
aaa[9]		0.15			0.0059	
ccc[10]		0.20			0.0079	
ddd[11]		0.10			0.0039	
eee[12]		0.15			0.0059	
fff[13]		0.08			0.0031	

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *The total profile height (Dim A) is measured from the seating plane to the top of the component.*
3. *The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heat slug.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to Datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no linear tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.*
6. *e represents the solder balls grid pitch(es).*
7. *N represents the total number of balls.*
8. *Basic dimensions SD & SE are defining the ball matrix position with respect to datums A and B.*
9. *The profile tolerance controlling the location and orientation of the sides of the package.*
10. *The parallelism tolerance controlling the orientation of the top surface of the package with respect to the seating plane, Datum C.*
11. *The profile tolerance controlling the location of the crowns of the balls with respect to Datum C.*
12. *The tolerance of position that controls the location of the pattern of balls with respect to Datum's A and B.*
13. *The tolerance of position that controls the location of the balls within the matrix with respect to each other.*

6.5 VFBGA361 package information (B09U)

This VFBGA is a 361-ball, 10 x 10 mm, very thin fine pitch ball grid array package.

Figure 64. **VFBGA361 - Outline**

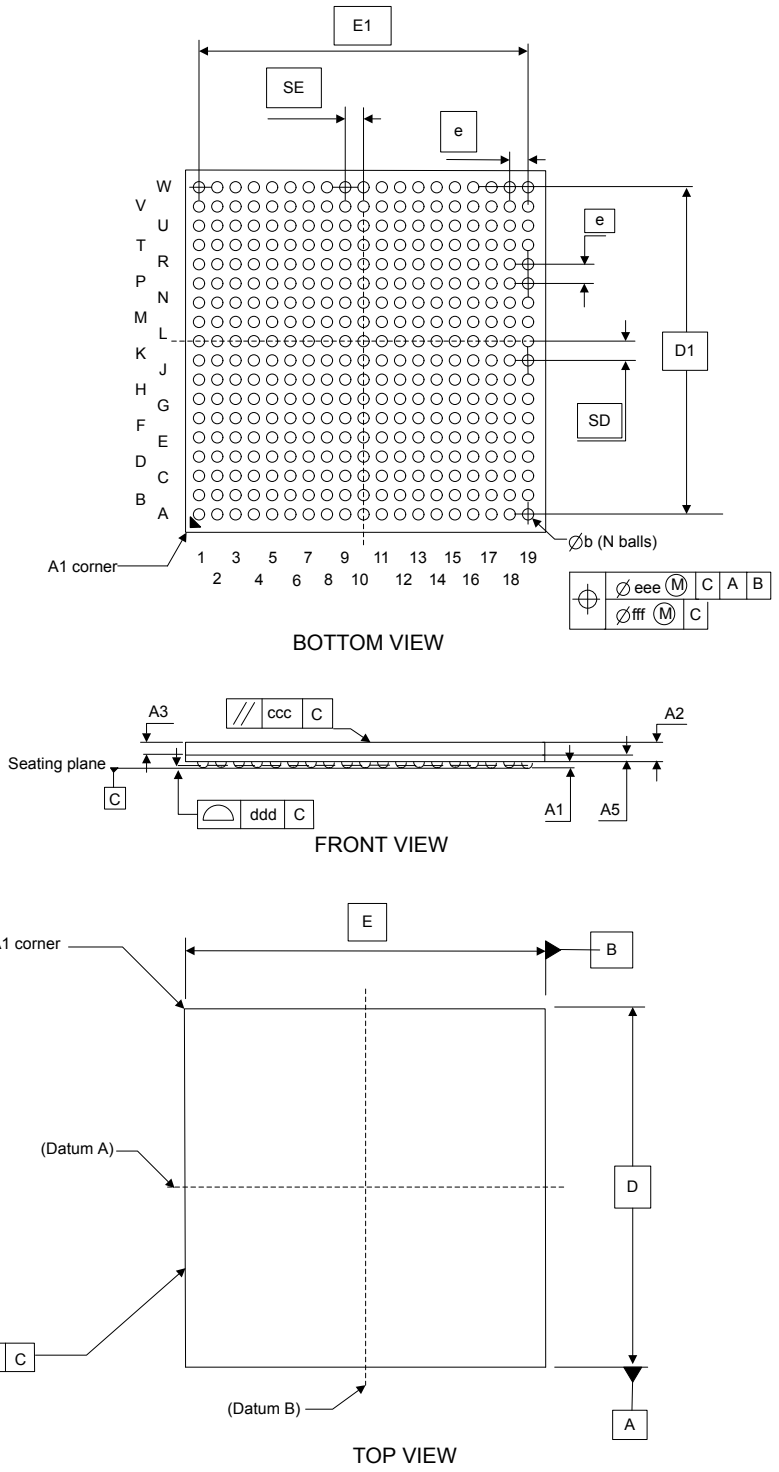


Table 116. VFBGA361 - Mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A[2]	-	-	1.00	-	-	0.0394
A1[3]	0.155	-	-	0.0061	-	-
b[4]	0.260	0.310	0.360	0.0102	0.0122	0.0142
D[5]	10.00 BSC			0.3937 BSC		
D1	9.000 BSC			0.3543 BSC		
E	10.00 BSC			0.3937 BSC		
E1	9.000 BSC			0.3543 BSC		
e[6]	0.500 BSC			0.0197 BSC		
N[7]	361					
SD[8]	0.500			0.0197		
SE[8]	0.500			0.0197		
aaa[9]	0.150			0.0059		
ccc[9]	0.200			0.0079		
ddd[9]	0.080			0.0031		
eee[9]	0.150			0.0059		
fff[9]	0.050			0.0020		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane*
3. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
4. *Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.*
5. *BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table*
6. *e(x) represents the solder ball grid pitch(es).*
7. *N represents the total number of balls on the BGA.*
8. *Basic dimensions SD(x) & SE(y) are defined with respect to datums A and B. They define the position of the centre ball(s) of the ball matrix.*
9. *Tolerance of form and position drawing.*

6.6 Package thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, can be calculated using the following equation:

$$T_J \max = T_A \max + \left(P_D \max \times \Theta_{JA}\right)$$

where:

- T_A max is the maximum ambient temperature in °C.
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W.
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max:

$$P_D \max = P_{INT} \max + P_{I/O} \max)$$

- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins:

$$P_{I/O} \max = \sum\left(V_{OL} \times I_{OL}\right) + \sum\left(\left(V_{DDIOx} - V_{OH}\right) \times I_{OH}\right)$$

considering the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

Table 117. Package thermal characteristics

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	VFBGA225 8×8 mm	27.9	°C/W
		VFBGA273 11×11 mm	25.6	
		TFBGA289 14×14 mm	23.7	
		VFBGA361 10×10 mm	25.7	
Θ_{JB}	Thermal resistance junction-board	VFBGA225 8×8 mm	12.0	
		VFBGA273 11×11 mm	12.5	
		TFBGA289 14×14 mm	13.2	
		VFBGA361 10×10 mm	12.4	
Θ_{JC}	Thermal resistance junction-top case	VFBGA225 8×8 mm	11.7	
		VFBGA273 11×11 mm	10.1	
		TFBGA289 14×14 mm	9.4	
		VFBGA361 10×10 mm	10.4	

6.6.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air) available on www.jedec.org.
- For information on thermal management, refer to application note *"Guidelines for thermal management on STM32 applications" (AN5036)* available on www.st.com.

7 Ordering information

Example: STM32 MP 215 F AM 3 ␣ T

Device family

STM32 = Arm®-based 32- or 64-bit processor

Product type

MP = MPU product

Device subfamily

211 = STM32MP211 line

213 = STM32MP213 line

215 = STM32MP215 line

Security option

C = Secure boot, cryptography hardware, 1.2 GHz CPU1

F = Secure boot, cryptography hardware, 1.5 GHz CPU1

Package and ball count

AO = VFBGA225 8x8, 225 balls pitch 0.5 mm

AN = VFBGA273 11x11, 273 balls pitch 0.5 mm

AM = TFBGA289 14x14, 289 balls pitch 0.8 mm

AL = VFBGA361 10x10, 361 balls pitch 0.5 mm

Junction temperature range

3 = -40 °C < T_J < +125 °C

Options

␣ (absent) = no options

Packing

T = Tape and reel

No character = tray or tube

Note: For a list of available options (such as speed and package) or for further information on any aspect of this device, contact your nearest ST sales office.

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Revision history

Table 118. **Document revision history**

Date	Revision	Changes
17-Oct-2025	1	Initial release.

Contents

1 **Introduction** 4
2 **Description** 5
3 **Functional overview** 11
3.1 Arm Cortex-A35 subsystem (CA35SS) 11
3.1.1 Features 11
3.1.2 Overview 11
3.2 Arm Cortex-M33 core with TrustZone and FPU (CM33) 12
3.3 Memories 12
3.3.1 External SDRAM 12
3.3.2 Embedded SRAM 12
3.4 DDR3L/DDR4/LPDDR4 controller (DDRCTRL) 13
3.5 Boot modes 13
3.6 Power supply management (PWR) 17
3.6.1 Power supply scheme 17
3.6.2 Power-supply supervisor 17
3.7 Low-power strategy 18
3.8 Resource isolation framework (RIF) 18
3.9 Reset and clock controller (RCC) 18
3.9.1 Features 19
3.9.2 Clock management 19
3.9.3 Reset sources 19
3.10 Inter-processor communication controller (IPCC1) 20
3.10.1 Main features 20
3.11 General-purpose input/outputs (GPIO) 21
3.12 Bus-interconnect matrix 21
3.13 High-performance DMA controllers (HPDMA1/2/3) 22
3.14 Extended interrupt and event controller (EXTI1/2) 23
3.15 Cyclic redundancy check calculation unit (CRC) 23
3.16 Flexible memory controller (FMC) 23
3.17 Octo-SPI memory interface (OCTOSPI1) 23
3.18 On-the-fly decoder (OTFDEC1) 24
3.19 Analog-to-digital converters (ADC1, ADC2) 24
3.20 Digital temperature sensor (DTS) 24
3.21 V_{BAT} operation 24
3.22 Voltage reference buffer (VREFBUF) 25

3.23 Multifunction digital filter (MDF1) . . . 25
3.23.1 Features . . . 25
3.24 Digital camera interface (DCMI) . . . 25
3.25 Parallel synchronous slave interface (PSSI) . . . 26
3.26 Digital camera interface with pixel processing (DCMIPP) . . . 26
3.27 Camera serial interface (CSI) . . . 27
3.28 LCD-TFT display controller (LTDC) . . . 27
3.29 True random number generator (RNG 1/2) . . . 27
3.30 Hash processor (HASH 1/2) . . . 27
3.31 Cryptographic processor (CRYP1/2) . . . 27
3.32 Secure AES (SAES) . . . 28
3.33 Public key accelerator (PKA) . . . 28
3.34 Boot and security and OTP control (BSEC) . . . 28
3.35 Timers and watchdogs . . . 28
3.35.1 Advanced-control timers (TIM1/8) . . . 29
3.35.2 General-purpose timers (TIM2/3/4/5/10/11/12/13/14/15/16/17) . . . 29
3.35.3 Basic timers (TIM6/TIM7) . . . 30
3.35.4 Low-power timer (LPTIM1/2/3/4/5) . . . 30
3.35.5 Independent watchdog (IWDG1/2/3/4) . . . 30
3.35.6 System window watchdog (WWDG1) . . . 30
3.35.7 SysTick timer . . . 30
3.35.8 Cortex-A35 generic timers (CNT) . . . 30
3.36 System timer generation (STGEN) . . . 31
3.37 Real-time clock (RTC) . . . 31
3.38 Tamper and backup registers (TAMP) . . . 31
3.39 Inter-integrated circuit interface (I2C1/2/3) . . . 32
3.40 Improved inter-integrated circuit (I3C1/2/3) . . . 32
3.41 Universal synchronous asynchronous receiver transmitter (USART1/2/3/6, UART4/5/7) . . . 33
3.42 Low-power universal asynchronous receiver transmitter (LPUART1) . . . 34
3.43 Serial peripheral interface (SPI1/2/3/4/5/6) inter-integrated sound interfaces (I2S1/2/3) . . . 35
3.44 Serial audio interfaces (SAI1/2/3/4) . . . 35
3.45 SPDIF receiver interface (SPDIFRX) . . . 35
3.46 Secure digital input/output MultiMediaCard interface (SDMMC1/2/3) . . . 35
3.47 Controller area network (FDCAN1/2) . . . 36
3.48 Universal serial bus Hi-Speed host (USBH) . . . 36
3.49 Universal serial bus 2.0 OTG high speed (OTG) . . . 36

3.50 Gigabit Ethernet MAC interface (ETH1/2) . . . 37
3.51 Debug infrastructure . . . 38
4 Pinouts/ballouts, pin description, and alternate functions . . . 39
4.1 Ballout schematics . . . 39
4.2 Ball description . . . 44
4.3 Alternate functions . . . 65
5 Electrical characteristics . . . 83
5.1 Parameter conditions . . . 83
5.1.1 Minimum and maximum values . . . 83
5.1.2 Typical values . . . 83
5.1.3 Loading capacitor . . . 83
5.1.4 Pin input voltage . . . 83
5.1.5 Power supply scheme . . . 84
5.1.6 Current consumption measurement . . . 85
5.2 Absolute maximum ratings . . . 85
5.3 Operating conditions . . . 86
5.3.1 General operating conditions . . . 86
5.3.2 Operating conditions at power-up/power-down . . . 88
5.3.3 Embedded reset and power control block characteristics . . . 89
5.3.4 Embedded reference voltage . . . 90
5.3.5 Supply current characteristics . . . 91
5.3.6 Wake-up time from low-power modes . . . 105
5.3.7 External clock source characteristics . . . 107
5.3.8 External clock source security characteristics . . . 112
5.3.9 Internal clock source characteristics . . . 112
5.3.10 PLL characteristics . . . 113
5.3.11 PLL spread spectrum clock generation (SSCG) characteristics . . . 114
5.3.12 Memory characteristics . . . 114
5.3.13 EMC characteristics . . . 115
5.3.14 Absolute maximum ratings (electrical sensitivity) . . . 116
5.3.15 I/O current injection characteristics . . . 117
5.3.16 I/O port characteristics . . . 117
5.3.17 NRST pin characteristics . . . 123
5.3.18 DDR IOs characteristics . . . 124
5.3.19 FMC characteristics . . . 124
5.3.20 OCTOSPI interface characteristics . . . 132
5.3.21 Delay block (DLYB) characteristics . . . 137

5.3.22 12-bit ADC characteristics . . . 137
5.3.23 Voltage reference buffer (VREFBUF) characteristics . . . 141
5.3.24 Digital Temperature Sensor (DTS) characteristics . . . 142
5.3.25 V_{BAT}, V_{DDCPU}, V_{DDCORE} ADC measurement characteristics . . . 143
5.3.26 Temperature and V_{BAT} monitoring characteristic for tamper detection . . . 143
5.3.27 Voltage monitoring characteristics . . . 143
5.3.28 Compensation cell characteristics . . . 144
5.3.29 Multi-function digital filter (MDF) characteristics . . . 145
5.3.30 Camera interface (DCMI) characteristics . . . 146
5.3.31 Camera interface (DCMIPP) characteristics . . . 147
5.3.32 Parallel interface (PSSI) characteristics . . . 148
5.3.33 LCD-TFT controller (LTDC) characteristics . . . 150
5.3.34 Timer characteristics . . . 152
5.3.35 Communications interfaces . . . 153
5.3.36 Embedded PHYs characteristics . . . 167
5.3.37 JTAG/SWD interface characteristics . . . 171

6 Package information . . . 173
6.1 Device marking . . . 173
6.2 VFBGA225 package information (B0P6) . . . 173
6.3 VFBGA273 package information (B0P7) . . . 174
6.4 TFBGA289 package information (B0NY) . . . 176
6.5 VFBGA361 package information (B09U) . . . 178
6.6 Package thermal characteristics . . . 181
6.6.1 Reference documents . . . 181

7 Ordering information . . . 182
Important security notice . . . 183
Revision history . . . 184
List of tables . . . 189
List of figures . . . 192

List of tables

Table 1. STM32MP21xC/F features and peripheral counts . . . 6
Table 2. STM32MP21xx differences per product lines . . . 8
Table 3. STM32MP21xx differences per packages . . . 9
Table 4. Default interfaces . . . 13
Table 5. Boot sources . . . 14
Table 6. Minimum set of default pins used during boot ROM phase . . . 14
Table 7. Timer feature comparison . . . 28
Table 8. USART/UART features . . . 34
Table 9. I/O power domains . . . 43
Table 10. Legend/abbreviations used in the ballout table . . . 44
Table 11. STM32MP21xC/F ball definitions . . . 45
Table 12. Alternate functions AF0 to AF7 . . . 65
Table 13. Alternate functions AF8 to AF15 . . . 72
Table 14. Voltage characteristics . . . 85
Table 15. Current characteristics . . . 86
Table 16. Thermal characteristics . . . 86
Table 17. General operating conditions . . . 86
Table 18. Operating conditions at power-up/power-down . . . 88
Table 19. Embedded reset and power control block characteristics . . . 89
Table 20. Embedded reference voltage characteristics . . . 90
Table 21. Embedded reference voltage calibration value . . . 90
Table 22. Current consumption (I_{DDCORE}) in Run modes . . . 92
Table 23. Current consumption (I_{DDCPU}) in Run modes . . . 95
Table 24. Current consumption (I_{DD}) in Run modes . . . 97
Table 25. Current consumption (I_{DDA18}) in Run modes . . . 98
Table 26. Current consumption ($I_{DDA18AON}$) in Run modes . . . 99
Table 27. Current consumption (I_{BAT}) in Run modes . . . 100
Table 28. Current consumption in Stop modes . . . 101
Table 29. Current consumption in LPLV-Stop modes . . . 102
Table 30. Current consumption in Standby mode . . . 103
Table 31. Current consumption in V_{BAT} mode . . . 104
Table 32. D1 (CPU1) low-power mode wake-up timings . . . 106
Table 33. D2 (CPU2) low-power mode wake-up timings . . . 106
Table 34. Wake-up time using USART/LPUART . . . 107
Table 35. High-speed external (HSE) user clock characteristics (digital bypass) . . . 107
Table 36. High-speed external (HSE) user clock characteristics (analog bypass) . . . 108
Table 37. Low-speed external (LSE) user clock characteristics (digital bypass) . . . 109
Table 38. Low-speed external (LSE) user clock characteristics (analog bypass) . . . 110
Table 39. High-speed external (HSE) oscillator characteristics . . . 110
Table 40. Low-speed external (LSE) oscillator characteristics . . . 111
Table 41. High-speed external user clock security system (HSE CSS) . . . 112
Table 42. Low-speed external user clock security system (LSE CSS) . . . 112
Table 43. HSI oscillator characteristics . . . 112
Table 44. MSI oscillator characteristics . . . 113
Table 45. LSI oscillator characteristics . . . 113
Table 46. PLL1 to PLL7 characteristics . . . 113
Table 47. PLL_USB characteristics . . . 114
Table 48. PLL2 to PLL7 SSCG parameters constraints . . . 114
Table 49. OTP characteristics . . . 115
Table 50. EMS characteristics . . . 115
Table 51. EMI characteristics for f_{HSE} = 24 MHz and F_{PLL1} = 1500 MHz . . . 116
Table 52. ESD absolute maximum ratings . . . 116

Table 53. Electrical sensitivities . . . 116
Table 54. I/O current injection susceptibility . . . 117
Table 55. I/O static characteristics . . . 117
Table 56. Output voltage characteristics for all I/Os . . . 119
Table 57. Output timing characteristics (V_{DD} = 3.0 - 3.6 V or V_{DDIOx} = 2.7 - 3.6 V, VDDIOxVRSEL = 0) . . . 119
Table 58. Output timing characteristics (V_{DD}/V_{DDIOx} = 1.71 - 1.89 V, VDDIOxVRSEL = 1) . . . 120
Table 59. Output timing characteristics (V_{DD}/V_{DDIOx} = 1.71 - 1.89 V, VDDIOxVRSEL = 0 degraded mode) . . . 122
Table 60. GPIO advance config delay characteristics . . . 123
Table 61. NRST pin characteristics . . . 123
Table 62. Asynchronous multiplexed PSRAM/NOR read timings . . . 124
Table 63. Asynchronous multiplexed PSRAM/NOR read - NWAIT timings . . . 125
Table 64. Asynchronous multiplexed PSRAM/NOR write timings . . . 126
Table 65. Asynchronous multiplexed PSRAM/NOR write - NWAIT timings . . . 126
Table 66. Synchronous multiplexed NOR/PSRAM read timings . . . 127
Table 67. Synchronous multiplexed PSRAM write timings . . . 129
Table 68. NAND flash read timings . . . 131
Table 69. NAND flash write timings . . . 132
Table 70. OCTOSPI characteristics in SDR mode . . . 132
Table 71. OCTOSPI characteristics in DTR mode (without DQS) . . . 133
Table 72. OCTOSPI characteristics in DTR mode (with DQS or HyperBus) . . . 134
Table 73. DLYB characteristics . . . 137
Table 74. ADC characteristics . . . 137
Table 75. ADC accuracy . . . 138
Table 76. Minimum sampling time versus RAIN . . . 140
Table 77. VREFBUF characteristics . . . 141
Table 78. DTS characteristics . . . 142
Table 79. V_{BAT}, V_{DDCPU}, V_{DDCORE} ADC measurement characteristics . . . 143
Table 80. TEMP and V_{BAT} Monitoring characteristics . . . 143
Table 81. Voltage monitoring characteristics (V_{DDCORE}, V_{DDCPU}, PVD_IN, $V_{DDA18ADC}$, $V_{DDIO1/2/3}$, $V_{DD33USB}$) . . . 143
Table 82. Compensation cell characteristics . . . 144
Table 83. MDF characteristics . . . 145
Table 84. DCMI characteristics . . . 146
Table 85. DCMIPP characteristics . . . 147
Table 86. PSSI transmit characteristics . . . 148
Table 87. PSSI receive characteristics . . . 149
Table 88. LTDC characteristics . . . 150
Table 89. TIMx characteristics . . . 152
Table 90. LPTIMx characteristics . . . 152
Table 91. I2C analog filter characteristics . . . 153
Table 92. I3C specific timings . . . 153
Table 93. I3C pin characteristics . . . 153
Table 94. SPI characteristics . . . 154
Table 95. I2S characteristics . . . 156
Table 96. SAI characteristics . . . 158
Table 97. SDMMC GPIO OSPEEDR settings for timing measurements . . . 159
Table 98. SDMMC characteristics for SD-Card or SDIO usage . . . 159
Table 99. SDMMC characteristics for *e*•MMC usage . . . 160
Table 100. Output speed settings . . . 162
Table 101. GPIO advance configuration settings used for RGMII and RGMII-ID characterization . . . 162
Table 102. Ethernet MAC timings for MDIO/SMA . . . 163
Table 103. Ethernet MAC timings for RMII . . . 163
Table 104. Ethernet MAC timings for MII . . . 164
Table 105. Ethernet MAC timings for RGMII . . . 164
Table 106. Ethernet MAC timings for RGMII_ID . . . 165

Table 107. USART (SPI mode) characteristics . . . 166
Table 108. DDR PHY characteristics . . . 167
Table 109. CSI PHY characteristics . . . 169
Table 110. USB high-speed PHY characteristics . . . 170
Table 111. JTAG dynamic characteristics . . . 171
Table 112. SWD dynamic characteristics . . . 172
Table 113. VFBGA225 - Mechanical data . . . 174
Table 114. VFBGA273 - Mechanical data . . . 175
Table 115. TFBGA289 - Mechanical data . . . 178
Table 116. VFBGA361 - Mechanical data . . . 180
Table 117. Package thermal characteristics . . . 181
Table 118. Document revision history . . . 184

List of figures

Figure 1. STM32MP21xC/F block diagram . . . 10
Figure 2. AXI STNoC multi-frequency network . . . 21
Figure 3. MCU multi-Layer AHB 300 MHz . . . 22
Figure 4. MCU multi-Layer AHB 150 MHz . . . 22
Figure 5. STM32MP21xC/F VFBGA225 ballout . . . 39
Figure 6. STM32MP21xC/F VFBGA273 ballout . . . 40
Figure 7. STM32MP21xC/F TFBGA289 ballout . . . 41
Figure 8. STM32MP21xC/F VFBGA361 ballout . . . 42
Figure 9. Pin loading conditions . . . 83
Figure 10. Pin input voltage . . . 83
Figure 11. Power supply scheme . . . 84
Figure 12. Current consumption measurement scheme . . . 85
Figure 13. High-speed external clock source AC timing diagram (digital bypass) . . . 108
Figure 14. High-speed external clock source AC timing diagram (analog bypass) . . . 109
Figure 15. Low-speed external clock source AC timing diagram (digital bypass) . . . 109
Figure 16. Low-speed external clock source AC timing diagram (analog bypass) . . . 110
Figure 17. Typical application with a 40 MHz crystal . . . 111
Figure 18. Typical application with a 32.768 kHz crystal . . . 112
Figure 19. V_{IL}/V_{IH} for TT I/Os . . . 118
Figure 20. Recommended NRST pin protection . . . 123
Figure 21. Asynchronous multiplexed PSRAM/NOR read waveforms . . . 125
Figure 22. Asynchronous multiplexed PSRAM/NOR write waveforms . . . 127
Figure 23. Synchronous multiplexed NOR/PSRAM read timings . . . 129
Figure 24. Synchronous multiplexed PSRAM write timings . . . 130
Figure 25. NAND controller waveforms for read access . . . 131
Figure 26. NAND controller waveforms for write access . . . 132
Figure 27. OCTOSPI timing diagram - SDR mode . . . 133
Figure 28. OCTOSPI timing diagram - DTR mode . . . 134
Figure 29. OCTOSPI HyperBus clock . . . 135
Figure 30. OCTOSPI HyperBus read . . . 136
Figure 31. OCTOSPI HyperBus read with double latency . . . 136
Figure 32. OCTOSPI HyperBus write . . . 137
Figure 33. ADC accuracy characteristics . . . 139
Figure 34. Typical connection diagram using the ADC with TT pins featuring analog switch function . . . 141
Figure 35. MDF timing diagram . . . 146
Figure 36. DCMI timing diagram . . . 147
Figure 37. DCMIPP timing diagram . . . 148
Figure 38. PSSI transmit timing diagram . . . 149
Figure 39. PSSI receive timing diagram . . . 150
Figure 40. LCD-TFT horizontal timing diagram . . . 151
Figure 41. LCD-TFT vertical timing diagram . . . 152
Figure 42. SPI timing diagram - master mode . . . 155
Figure 43. SPI timing diagram - slave mode and CPHA = 0 . . . 155
Figure 44. SPI timing diagram - slave mode and CPHA = 1 . . . 156
Figure 45. I2S target timing diagram (Philips protocol) . . . 157
Figure 46. I2S controller timing diagram (Philips protocol) . . . 157
Figure 47. SAI master timing waveforms . . . 158
Figure 48. SAI slave timing waveforms . . . 159
Figure 49. SD high-speed mode . . . 161
Figure 50. SD default mode . . . 161
Figure 51. SDMMC DDR mode . . . 161
Figure 52. Ethernet MDIO/SMA timing diagram . . . 163
Figure 53. Ethernet RMII timing diagram . . . 163

Figure 54. Ethernet MII timing diagram . . . 164
Figure 55. Ethernet RGMII timing diagram . . . 165
Figure 56. Ethernet RGMII-ID timing diagram . . . 165
Figure 57. USART timing diagram in SPI master mode . . . 167
Figure 58. USART timing diagram in SPI slave mode . . . 167
Figure 59. JTAG timing diagram . . . 172
Figure 60. SWD timing diagram . . . 172
Figure 61. VFBGA225 - Outline . . . 173
Figure 62. VFBGA273 - Outline . . . 175
Figure 63. TFBGA289 - Outline . . . 176
Figure 64. VFBGA361 - Outline . . . 179

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