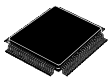
STM32H7Pxxx

Datasheet

32-bit Arm® Cortex®-M7 520 MHz MCUs, Neural-ART Accelerator, hardware signal processor, up to 2MB flash, 736 KB RAM, USB, 3× FD-CAN, 4× 12-bit ADCs, 2 DAC outputs, 2× high-res timers, 3× adv. motor control timers



LQFP100 (14 × 14 mm) pitch 0.5 mm
LQFP100 EP (14 × 14 mm) pitch 0.5 mm
LQFP128 (14 × 14 mm) pitch 0.4 mm
LQFP144 (20 × 20 mm) pitch 0.5 mm
LQFP144 EP (20 × 20 mm) pitch 0.5 mm
LQFP176 (24 × 24 mm) pitch 0.5 mm
LQFP176 EP (24 x 24 mm) pitch 0.5 mm



TFBGA100 (8 × 8 mm) pitch 0.8 mm
UFBGA176+25 (10 × 10 mm) pitch 0.65 mm

Product summary	
STM32H7P4xx	STM32H7P4VG, STM32H7P4QG, STM32H7P4ZG, STM32H7P4IG, STM32H7P4VI, STM32H7P4QI, STM32H7P4ZI, STM32H7P4II
STM32H7P5xx	STM32H7P5VG, STM32H7P5QG, STM32H7P5ZG, STM32H7P5IG, STM32H7P5VI, STM32H7P5QI, STM32H7P5ZI, STM32H7P5II

Prerelease product(s)

Features

Includes ST state-of-the-art patented technology.

Cores

- 32-bit Arm® Cortex®-M7 core with DP-FPU and L1 cache:
  32 Kbytes of data and 32 Kbytes of instruction cache allowing to fill one cache line in a single access from the 128-bit embedded flash memory, frequency up to 520 MHz, MPU, 2773 CoreMark® (5.33 CoreMark®/MHz), and DSP instructions

Neural processing unit (NPU)

- ST Neural-ART Accelerator, frequency up to 520 MHz, 85 Gops
- Specialized hardware units for DNN (deep-neural network) inference functions
- Flexible dedicated stream processing engine

Signal processing unit (HSP)

- Hardware signal processor (HSP) enabling matrix, vector and digital signal processing operation
- 32-bit floating point support
- Matrix / vector algebra, (i)FFT transform, filtering & convolution, math operators

Mathematical acceleration

- CORDIC for trigonometric functions acceleration
- FMAC: Filter mathematical accelerator

Memories

- Up to 2 Mbytes dual bank flash memory plus 1 Kbyte of OTP memory
- 736 Kbytes of on-chip RAM: 192 Kbytes of ITCM SRAM + 128 Kbytes of DTCM SRAM for time critical routines, 416 Kbytes of user SRAM, and 4 Kbytes of SRAM in backup domain
- Octo-SPI memory interface with support for serial PSRAM/NOR, hyper RAM/ flash frame formats, running up to 100 MHz in SRD mode and DTR mode
- Flexible external memory controller with up to 16-bit data bus:
  - SRAM, PSRAM, NOR flash memory clocked up to 100 MHz in synchronous mode
  - SDRAM/LPSDR SDRAM
  - 8/16-bit NAND flash memories
- CRC calculation unit

Security

- ROP, PC-ROP, active tamper, secure firmware upgrade support, secure access mode
- HASH (MD5, SHA-1, SHA-2), HMAC

- 1x 32-bit, NIST SP 800-90B compliant, true random generator

Reset and power management

- 1.71 to 3.6 V application supply and I/Os
- POR, PDR, PVD and BOR
- Integrated high efficiency SMPS step-down converter or LDO regulator
- Voltage scaling in Run and Stop mode
- Backup regulator (~0.9 V)
- Low-power modes: Sleep, Stop and Standby
- V_{BAT} battery operating mode with charging capability
- CPU power state monitoring pins

Low-power consumption

- Stop: down to TBD µA with full RAM retention
- Standby: TBD µA (backup SRAM Off, RTC/LSE On)
- V_{BAT}: TBD µA (RTC and LSE On)

Clock management

- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- External oscillators: 4-50 MHz HSE, 32.768 kHz LSE
- 3× PLLs (1 for the system clock, 2 for kernel clocks) with fractional mode

General-purpose inputs/outputs

- Up to 134 I/O ports with interrupt capability
- Fast I/Os capable of up to 133 MHz
- Up to 132 5-V-tolerant I/Os

Interconnect matrix

- 64-bit high bandwidth AXI interconnect with programmable priority
- 32-bit AHB matrix
- Independent peripheral buses (6 × AHB, 3 × APB)

2 DMA controllers to offload the CPU

- High-performance direct memory access controller (HPDMA) on AXI interconnect
- General purpose direct memory access controller (GPDMA) on AHB interconnect

Up to 20 communication peripherals

- 3× I^2C FM+ interfaces (SMBus/PMBus)
- 1× I3C
- 5× USART + 5× UART (ISO7816 interface, LIN, IrDA, modem control) and 1× LPUART
- 6× SPI, including 3 with full-duplex I2S audio class accuracy
- 1× SD/SDIO/MMC interfaces (up to 100 MHz)
- 3× CAN-FD controllers
- 1× USB OTG full speed interfaces

Analog peripherals

- 4× 12-bit ADCs, up to 5 MSPS and 44 channels
- 1× internal voltage reference (1.8 – 2.9 V)
- 1× analog and 1x digital temperature sensors

Prerelease product(s)

- 1× 12-bit dual-channel DAC with output buffers + 3× 12-bit dual-channel fast DAC for internal use
- 8× fast comparators with window mode
- 1× CIC decimation filter for PDM digital microphone

Up to 27 timers and 2 watchdogs

- 2× high resolution timers for precise PWM control (up to 520 MHz)
- 4× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input (up to 520 MHz)
- 3× 16-bit advanced motor control timers (up to 520 MHz)
- 9× 16-bit general-purpose timers (up to 520 MHz)
- 2× 16-bit general-purpose timers (up to 520 MHz)
- 5× 16-bit low-power timers (up to 100 MHz)
- 2× watchdogs (independent and window)
- 1× SysTick timer
- RTC with sub-second accuracy and hardware calendar

Debug mode

- SWD and JTAG interfaces
- 4 KB embedded trace buffer

96-bit unique ID

All packages are ECOPACK2 compliant

Prerelease product(s)

1 Introduction

This document provides information on STM32H7Pxxx devices, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging and ordering information.

For information on the Arm® Cortex®- M7 core, refer to the Cortex®- M7 Technical Reference Manual, available from the www.arm.com website.

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arm

Prerelease product(s)

2 Description

STM32H7Pxxx devices are based on the high-performance Arm® Cortex®-M7 32-bit RISC core operating at up to 520 MHz. The Cortex®-M7 core features a floating-point unit (FPU) which supports Arm® double-precision (IEEE 754 compliant) and single-precision data-processing instructions and data types. STM32H7Pxxx devices support a full set of DSP instructions and a memory protection unit (MPU) to enhance application security.

In addition to the CPU, all devices include a high-performance signal processing (HSP) unit capable of accelerating and off loading mathematical and signal processing tasks. Specific part numbers incorporate STMicroelectronics Neural-ART Accelerator.

STM32H7Pxxx devices incorporate high-speed embedded memories with a dual-bank flash memory of 2 Mbytes, 736 Kbytes of RAM (including 320 Kbytes of TCM RAM, 416 Kbytes of user SRAM and 4 Kbytes of backup SRAM), as well as an extensive range of enhanced I/Os and peripherals connected to three APB buses, five AHB buses, a 32-bit multilayer AHB bus matrix, and a 64-bit AXI interconnect for internal and external memory access.

All the devices offer four ADCs, eight DACs, of which six dedicated to internal voltage comparators, eight fast voltage comparators, a filter for a digital microphone, a low-power RTC, four 32-bit timers, nine general-purpose 16-bit timers, three PWM 16-bit timers for motor control, two basic timers, five low-power timers, a true random number generator (RNG) and a HASH accelerator.

All devices also feature the following communication interfaces:

- Standard interfaces
  - Three I2Cs and one I3C
  - Five USARTs, five UARTs, and one LPUART
  - Six SPIs, three with I2S in full-duplex mode. To achieve audio class accuracy, the I2S peripherals can be clocked via an external clock to allow synchronization.
  - One SDMMC interface
  - A USB OTG full-speed
  - Three FDCAN interfaces
- Advanced interfaces including
  - A flexible memory control (FMC) interface
  - An octo-SPI memory interface

Refer to Table 1 for the list of peripherals available on each part number.

STM32H7Pxxx devices operate in the -40 to +125°C ambient temperature range from a 1.71 to 3.6 V power supply. The supply voltage must stay above 1.71 V which is the embedded power voltage detector threshold. The device embeds an integrated voltage regulator to supply the core, or a high efficiency SMPS depending on the part number.

A comprehensive set of power-saving modes allows the design of low-power applications.

The CPU and domain states can be directly monitored on some GPIOs configured as alternate functions. STM32H7Pxxx devices are offered in several packages ranging from 100 to 176 pins/balls.

These features make the STM32H7Pxxx microcontrollers suitable for a wide range of applications:

- Industrial applications: PLC, inverters, circuit breakers

Table 1. STM32H7Pxxx features and peripheral counts

Features		STM32H7PxVIT6Q	STM32H7PxVIH6Q	STM32H7PxVIZ3Q	STM32H7PxQIT6Q	STM32H7PxZIT6Q	STM32H7PxZIZ3Q	STM32H7PxIIT6Q	STM32H7PxIIZ3Q	STM32H7PxIIK6Q	STM32H7PxVGT6	STM32H7PxVIT6	STM32H7PxVGH6	STM32H7PxVIH6	STM32H7PxQGT6	STM32H7PxQIT6	STM32H7PxZGT6	STM32H7PxZIT6	STM32H7PxIGT6	STM32H7PxIIT6	STM32H7PxIGK6	STM32H7PxIIK6
Neural-ART Accelerator (NPU)		Yes[1]																				
Flash size in Mbyte		2									1	2	1	2	1	2	1	2	1	2	1	2
SRAM in Kbyte	On AXI	320																				
	On AHB	96																				

Prerelease product(s)

Features		STM32H7PxVIT6Q	STM32H7PxVIH6Q	STM32H7PxVIZ3Q	STM32H7PxQIT6Q	STM32H7PxZIT6Q	STM32H7PxZIZ3Q	STM32H7PxIIT6Q	STM32H7PxIIZ3Q	STM32H7PxIIK6Q	STM32H7PxVGT6	STM32H7PxVIT6	STM32H7PxVGH6	STM32H7PxVIH6	STM32H7PxQGT6	STM32H7PxQIT6	STM32H7PxZGT6	STM32H7PxZIT6	STM32H7PxIGT6	STM32H7PxIIT6	STM32H7PxIGK6	STM32H7PxIIK6
TCM SRAM in Kbyte	ITCM	192																				
	DTCM	128																				
Backup SRAM in Kbytes		4																				
GPIO	PA	16																				
	PB	16																				
	PC	16																				
	PD	8	10	11	16						11	13	16									
	PE	9		10	14	15	16				9		14		15		16					
	PF	4		6	13	16					4		13		16							
	PG	0		1	3	6	12	16			0		6		9		16					
	PH	2				4	7	16			2				4		16					
	PI	1					2	3			1						6					
	Total GPIOs	72	74	79	97	106	117	131			75	77	100		109		134					
FMC	8-bit display	Yes																				
	Multiplexed NOR/PSRAM	Yes																				
	NOR flash / PSRAM 16-bit	No				Yes					No				Yes							
	16-bit NAND	Yes																				
	16-bit SDRAM	No				Yes					No				Yes							
XSPI		Yes																				
SDMMC	SDIO 4 bits internal transceiver	Yes																				
	SDIO 4 bits external transceiver	Yes																				
	eMMC internal transceiver	Yes																				
	eMMC external transceiver	Yes																				
USB OTG-FS		Yes																				
UCPD		Yes																				
HRTIM	Number of instances	2																				
	Number of channels HRTIM1/ HRTIM2	12/5	12/7	12/9	12/10	12/12					12/5	12/7	12/10		12/12							
TIMERS	Advanced control	3																				

Prerelease product(s)

Features		STM32H7PxVIT6Q	STM32H7PxVIH6Q	STM32H7PxVIZ3Q	STM32H7PxQIT6Q	STM32H7PxZIT6Q	STM32H7PxZIZ3Q	STM32H7PxIIT6Q	STM32H7PxIIZ3Q	STM32H7PxIIK6Q	STM32H7PxVGT6	STM32H7PxVIT6	STM32H7PxVGH6	STM32H7PxVIH6	STM32H7PxQGT6	STM32H7PxQIT6	STM32H7PxZGT6	STM32H7PxZIT6	STM32H7PxIGT6	STM32H7PxIIT6	STM32H7PxIGK6	STM32H7PxIIK6
TIMERS	General purpose (32 bits)	4																				
	Lite	9																				
	Basic	2																				
	Low-power	5																				
Watchdog	Window/ independent	1/1																				
Real time clock (RTC)		1																				
ADC	Number of instances	4																				
	Number of channels ADC1/ADC2/ ADC3/ADC4	15/16/11/11				16/18/17/18					15/16/13/14				16/18/17/18							
	Number of channels (Fast/Slow)	33(17/16)		35(18/17)		44(20/24)					36(18/18)				44(20/24)							
DAC	Total/buffered	8/2																				
	Dedicated VREFDAC+/ VREFDAC- pin	No/No				Yes/Yes					No/No				Yes/Yes							
COMP		8																				
SPI		6																				
I2C		3																				
I3C		1																				
USART/UART/LPUART		5/5/1																				
FDCAN		3																				
ADF		1																				
WKUP		7						8			7								8			
TAMP	Pins (IN/OUT)	6(4/4)						7(5/5)			6(4/4)								7(5/5)			
RNG		1																				
HASH		1																				
HSP		1																				
FMAC		1																				
CORDIC		1																				
Debug	Serial wire/ JTAG	Yes/Yes																				
	DBTRGI input trigger	No			Yes						No				Yes							
	DBTRGO output trigger	No				Yes					No				Yes							

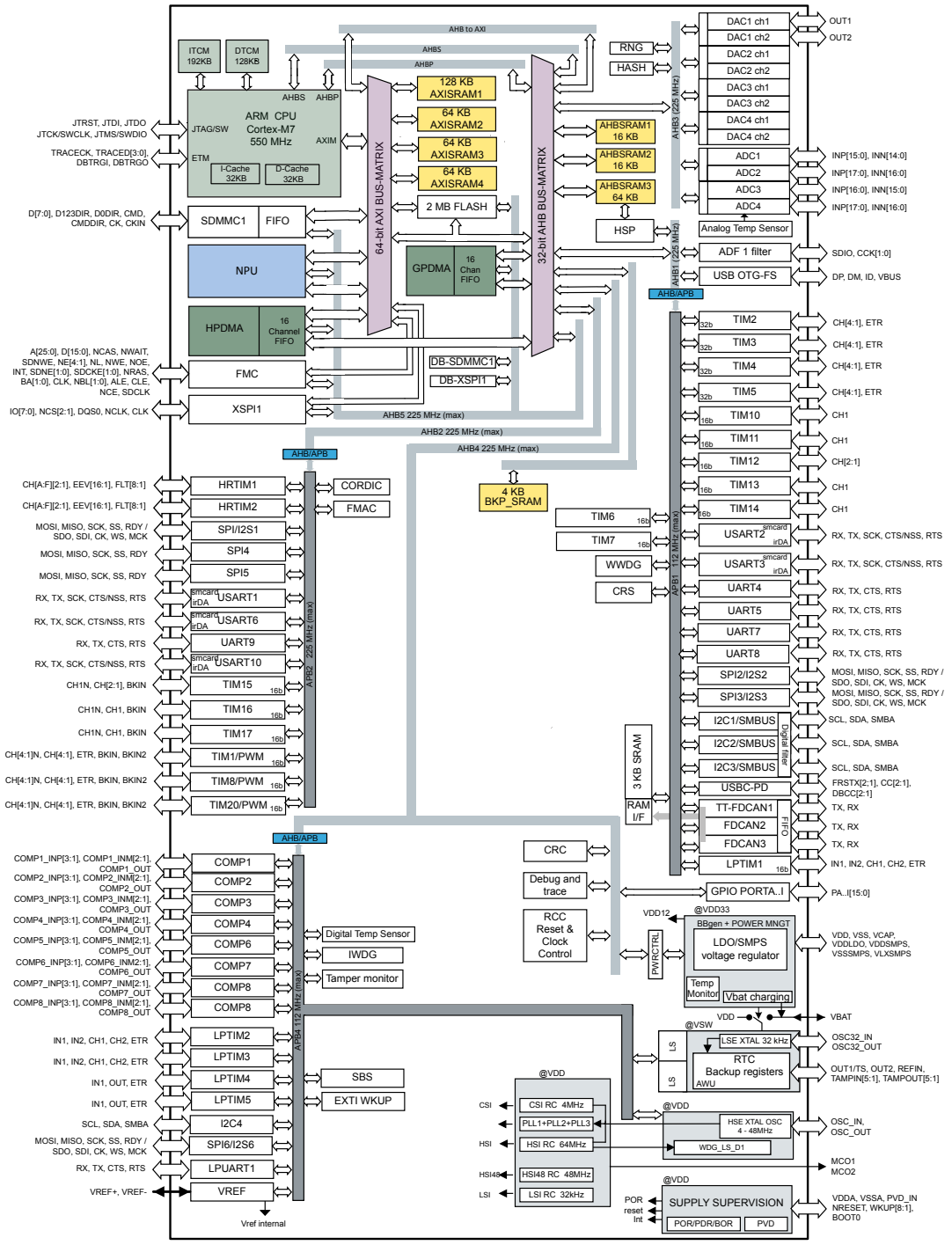
Prerelease product(s)

Features		STM32H7PxVIT6Q	STM32H7PxVIH6Q	STM32H7PxVIZ3Q	STM32H7PxQIT6Q	STM32H7PxZIT6Q	STM32H7PxZIZ3Q	STM32H7PxIIT6Q	STM32H7PxIIZ3Q	STM32H7PxIIK6Q	STM32H7PxVGT6	STM32H7PxVIT6	STM32H7PxVGH6	STM32H7PxVIH6	STM32H7PxQGT6	STM32H7PxQIT6	STM32H7PxZGT6	STM32H7PxZIT6	STM32H7PxIGT6	STM32H7PxIIT6	STM32H7PxIGK6	STM32H7PxIIK6
Debug	DBTRGIO input/output trigger	No	Yes																			
	Trace port width (bits)	4																				
Integrated SMPS		Yes									No											
Integrated LDO		No									Yes											
Exposed pad (VSS)		No		Yes	No		Yes	No	Yes	No												
Packages		LQFP100	TFBGA100	LQFP100-EP	LQFP128	LQFP144	LQFP144-EP	LQFP176	LQFP176-EP	UFBGA176	LQFP100	TFBGA100	LQFP128	LQFP144	LQFP176	UFBGA176						

1. STM32H7P5xx devices include the NPU, STM32H7P4xx devices do not.

Prerelease product(s)

Figure 1. **STM32H7Pxxx block diagram**



Prerelease product(s)

3 Functional overview

3.1 Arm® Cortex®-M7 with FPU

The Arm®Cortex®-M7 with double-precision FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and optimized power consumption, while delivering outstanding computational performance and low interrupt latency.

TheCortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard architecture with L1 caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI4 interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The following memory interfaces are supported:

- Separate Instruction and Data buses (Harvard Architecture) to optimize CPU latency
- Tightly Coupled Memory (TCM) interface designed for fast and deterministic SRAM accesses
- AXI Bus interface to optimize Burst transfers
- Dedicated low-latency AHB-Lite peripheral bus (AHBP) to connect to peripherals.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It also supports single and double precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

Refer to Figure 1 for the general block diagram of the STM32H7B3xI family.

Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.

3.2 Memory protection unit (MPU)

The memory protection unit (MPU) manages the CPU access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows defining up to 16 protected regions that can in turn be divided into up to eight independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

3.3 Memories

3.3.1 Embedded flash memory

The STM32H7Pxxx devices embed 1 or 2 Mbytes of dual-bank nonvolatile flash memory that can be used for storing programs and data.

The flash memory is composed of 128-bit words that can be used for storing code and data constants. Each word has an additional 9-bit ECC field for error detection and correction. The flash memory can be programmed by word and erased by sector. The dual-bank architecture means that one bank can be read while the other bank is being erased or programmed.

The flash memory is organized as follows:

- 2 × 512 Kbytes / 1 Mbyte of user flash memory, divided into 8 Kbyte sectors
- 2 × 64 Kbytes of system flash memory from which the device can boot
- 1 Kbyte of OTP (one-time programmable) memory containing option bytes for user configuration

Prerelease product(s)

3.3.2 Security

The STM32H7Pxxx supports nonvolatile code and data security management including:

- 128-bit password-based debug reopening with RAM and flash automatic erase
- Temporal isolation based on application HDPL (hidden data protection level)
- Securable user flash area per bank
- Unique boot entry enforcement on a closed device
- 32 × 128-bit nonvolatile option byte keys
- Sector group write-protection per bank, protecting up to 32 groups of four sectors (32 Kbyte) per bank

3.3.3 Embedded SRAM

All devices feature:

- 320 Kbytes of SRAM mapped on the AXI bus matrix:
  - AXISRAM1: 128 Kbyte
  - AXISRAM2: 64 Kbyte
  - AXISRAM3: 64 Kbyte
  - AXISRAM4: 64 Kbyte
- 96 Kbytes of AHB-RAM mapped on the AHB bus matrix:
  - AHBSRAM1: 16 Kbyte
  - AHBSRAM2: 16 Kbyte
  - AHBSRAM3: 64 Kbyte
- 4 Kbytes of backup SRAM
  The content of this area is protected against possible unwanted write accesses and is retained in Standby or V_{BAT} mode.
- Tightly coupled memory (ITCM and DTCM):
  - 192 Kbytes of tightly coupled instruction SRAM (ITCM)
- This RAM is connected to a dedicated 64-bit interface. It can be used for deterministic or critical real-time code execution.
  - 2 × 64 Kbytes of tightly coupled data SRAM (DTCM)
- This RAM is connected on two dedicated 32-bit interfaces. It can be used for critical real-time data, such as stack/heap memory. The DTCM SRAMs can be accessed in parallel thanks to the Cortex®-M7 dual issue capability.

3.4 Boot modes

At startup, the boot memory space is selected by the BOOT0 pin and NVSTATE option bits.

If NVSTATE is OPEN:

- If BOOT0 = 0: boot from user flash memory at address 0x8000 0000
- If BOOT0 = 1: boot from bootloader

If NVSTATE is CLOSED:

- Boot from RSS in system flash memory at address 0x1FF0 0080

The bootloader is in nonuser system flash memory. It is used to program the user flash memory through a serial interface (USART, I2C/I3C, SPI, USB, FDCAN). Refer to *STM32 microcontroller system memory boot mode* application note (AN2606) for details.

3.5 Power supply management

STM32H7P MCUs require at least one power supply to operate fully. The user must select either an LDO or an SMPS, depending on the package and part number (see Table 2). Additional power supplies or voltage references are necessary for specific use cases.

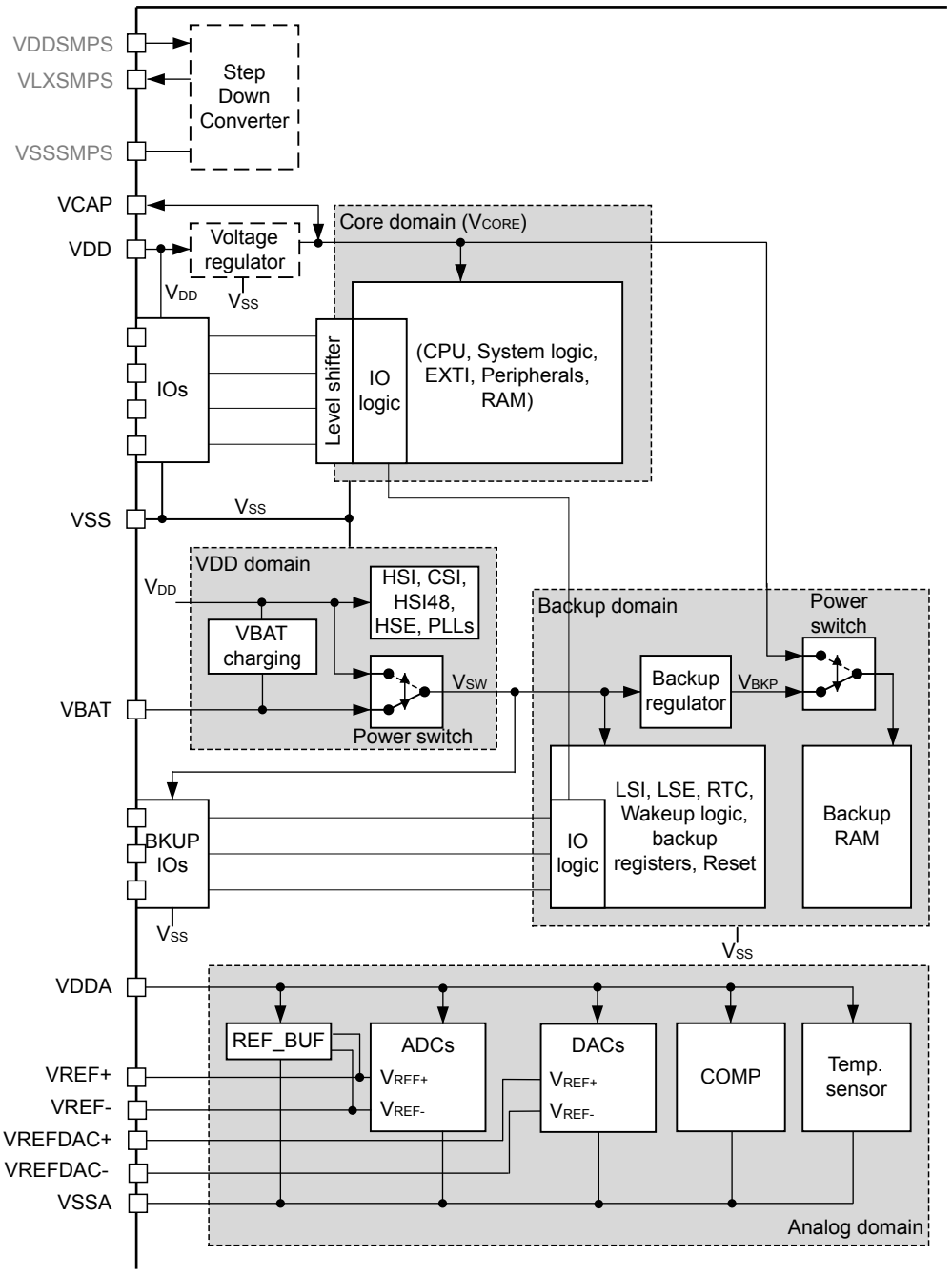
Prerelease product(s)

Table 2. Package versus supply

-	STM32H7PxVIT6Q	STM32H7PxVIH6Q	STM32H7PxVIZ3Q	STM32H7PxQIT6Q	STM32H7PxZIT6Q	STM32H7PxZIZ3Q	STM32H7PxIIT6Q	STM32H7PxIIZ3Q	STM32H7PxIIK6Q	STM32H7PxVGT6	STM32H7PxVIT6	STM32H7PxVGH6	STM32H7PxVIH6	STM32H7PxQGT6	STM32H7PxQIT6	STM32H7PxZGT6	STM32H7PxZIT6	STM32H7PxIGT6	STM32H7PxIIT6	STM32H7PxIGK6	STM32H7PxIIK6
Integrated SMPS	Yes									No											
Integrated LDO	No									Yes											
Exposed pad (VSS)	No		Yes		No		Yes		No		No										
Packages	LQFP100	TFBGA100	LQFP100-EP	LQFP128	LQFP144	LQFP144-EP	LQFP176	LQFP176-EP	UFBGA176	LQFP100	TFBGA100			LQFP128		LQFP144		LQFP176		UFBGA176	

Prerelease product(s)

Figure 2. Power supply versus power domain



Note: VDDSMPS, VLXSMPS and VSSSMPS are only available on the STM32H7PxVIT6Q, STM32H7PxVIH6Q, STM32H7PxVIZ3Q, STM32H7PxQIT6Q, STM32H7PxZIT6Q, STM32H7PxZIZ3Q, STM32H7PxIIT6Q and STM32H7PxIIZ3Q.

The internal STM32H7P system is supplied through different power domains: core domain, V_{DD} domain, backup domain, and analog domain. Figure 2 illustrates the power supply layout in relation to the power domains.

Table 3 lists the pin names, signal types, and descriptions for supply input and output signals connected to the package pins or balls.

Prerelease product(s)

Table 3. PWR input and output signals connected to package pins/balls

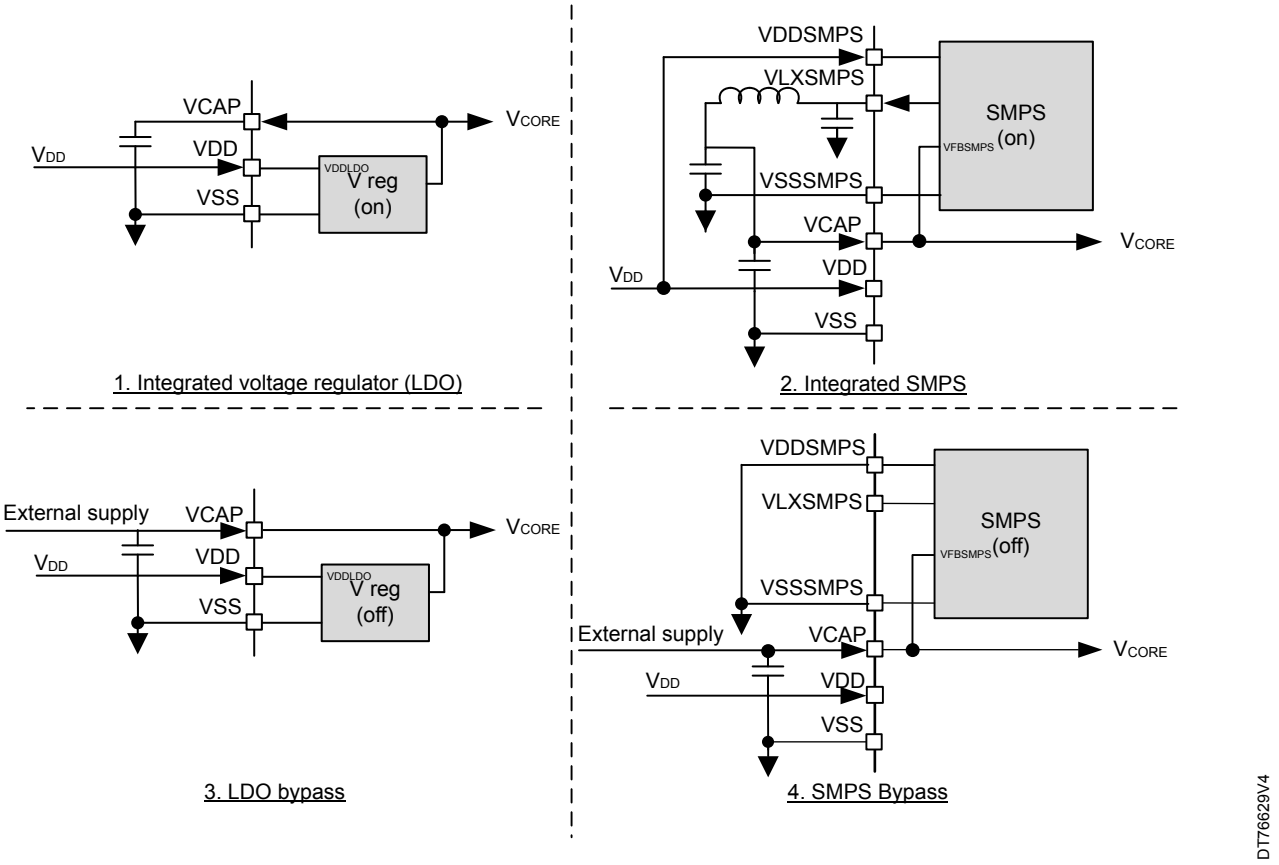
Power supply	Signal type	Description
V_{DD}	Supply input	Main I/O and V_{DD} domain supply input.
V_{SS}	Supply input	Main ground.
V_{DDA}	Supply input	External analog power supply for analog peripherals.
V_{SSA}	Supply input	Separate isolated ground for analog peripherals.
V_{BAT}	Supply input/output	Backup battery supply: • Optional external supply for the backup domain when V_{DD} is not present. • It can also be used to charge the external battery.
V_{DDSMPS}	Supply input	Supply for switch-mode power supply (SMPS) step-down converter.
V_{LXSMPS}	Supply output	SMPS step-down converter output.
V_{SSSMPS}	Supply input	Ground for SMPS step-down converter.
V_{CAP}	Supply input	Digital core supply input pin: For the SMPS package, it is supplied by the embedded SMPS or from an external source. For the LDO package, it is used to attach the bulk output capacitor of the internal LDO or an external source in bypass mode. Refer to Figure 3. System supply configurations for the different possible configurations.
V_{REF+}	Supply input/output	Reference voltage for ADCs: It can be generated from the internal V_{REFBUF} or provided by an external source.
V_{REF-}	Supply input	Ground reference for ADCs.
$V_{REFDAC+}$	Supply input/output	Reference voltage for DACs: It can be provided by an external source or by V_{REF+} when the internal V_{REFBUF} is activated.
$V_{REFDAC-}$	Supply input	Ground reference for DACs.

There are four possible supply configurations illustrated in Figure 3, depending on the selected part number:

- **Integrated voltage regulator** is used (a low-cost solution in terms of external components).
- **Integrated SMPS step-down converter** is used (a high-efficiency solution).
- **External supply source** is used (the integrated voltage regulator or integrated SMPS step-down converter is bypassed).

Prerelease product(s)

Figure 3. System supply configurations



3.5.1 Power supply scheme

- V_{DD} = 1.71 to 3.6 V: external power supply for digital I/Os, provided externally through VDD pins. It also supplies power to the integrated voltage regulator and V_{SW} (backup) domain.
- V_{DDA}= 1.62 to 3.6 V: external analog power supplies for ADC, DAC, COMP, voltage reference, reset blocks, oscillators, and PLL.
- V_{BAT} = 1.2 to 3.6 V: power supply for the V_{SW} domain when V_{DD} is not present.
- V_{CAP}: core power domain (V_{CORE}) supply. The voltage level can be varied according to the operating frequency and power mode. V_{CAP} can be supplied by the integrated voltage regulator or SMPS, depending on the package option, or by an external supply.
- V_{DDSMPS} = 1.71 to 3.6 V: integrated step-down converter input typically connected to V_{DD}.
- V_{LXSMPS}: integrated step-down converter output to external inductor.

Note: For I/O speed optimization at low V_{DD} supply, refer to Section 3.8: General-purpose input/outputs (GPIOs).

The features available on the device depend on the package (refer to Table 1. STM32H7Pxxx features and peripheral counts).

3.5.2 Power supply supervisor

The STM32H7Pxxx devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a brownout reset (BOR) circuitry:

Prerelease product(s)

- Power-on reset (POR)
  The POR supervisor monitors the V_{DD} power supply and compares it to a fixed threshold. The devices remain in reset mode when V_{DD} is below this threshold.
- Power-down reset (PDR)
  The PDR supervisor monitors the V_{DD} power supply. A reset is generated when V_{DD} drops below a fixed threshold.
- Brownout reset (BOR)
  The BOR supervisor monitors the V_{DD} power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when V_{DD} drops below this threshold.
- Programmable voltage detector (PVD)
  The PVD monitors the V_{DD} power supply by comparing it with a threshold selected from a set of predefined values.
  It can also monitor the voltage level of the PVD_IN pin by comparing it with an internal V_{REFINT} voltage reference level.
- Analog voltage detector (AVD)
  The AVD monitors the V_{DDA} power supply by comparing it with a threshold selected from a set of predefined values.
- V_{BAT} threshold
  The V_{BAT} battery voltage level can be monitored by comparing it with two threshold levels.
- Temperature threshold
  A dedicated temperature sensor monitors the junction temperature and compares it with two threshold levels.

3.5.3 Voltage regulator (option)

The integrated voltage regulator supplies the V_{CORE} domain. The output voltage can be set to one of five levels according to the application needs:

- Run mode (VOS0 to VOS2)
  - VOS0: high performance
  - VOS1: medium performance and consumption
  - VOS2: low-power consumption
- Stop mode (SVOSL, SVOSH)
  - SVOSH: low frequency clock can be maintained for some peripherals (UART, SPI, I^2C, LPTIM)
  - SVOSL: wake-up from Stop mode is possible through GPIO or asynchronous interrupt.

3.5.4 SMPS step-down converter (option)

The built-in SMPS step-down converter is a highly power-efficient DC-DC nonlinear switching regulator that provides lower power consumption than a low-drop-out voltage regulator (LDO).

The step-down converter is used to supply the V_{CORE} domain

- The SMPS step-down converter operating modes follow the device system operating modes (Run, Stop, Standby).
- The SMPS step-down converter output voltage is set according to the VOS and SVOS bits (voltage scaling)

An external power supply can be used to supply the V_{CORE} domain. In this case, the integrated SMPS step-down converter does not start up. It is up to the user to ensure that the VCORE power-on constraints are respected, and the voltage is correctly set according to the selected operating mode.

3.6 Low-power modes

There are several ways to reduce power consumption on STM32H7Pxxx:

- Decrease dynamic power consumption by slowing down the system clocks even in Run mode and by individually clock gating the peripherals that are not used.
- Save power consumption when the CPU is idle, by selecting among the available low-power modes according to the user application needs. This allows achieving the best compromise between short startup time, low-power consumption, as well as available wake-up sources.

Prerelease product(s)

The devices feature four low-power modes:

- Sleep mode (CPU clock stopped)
- Stop mode (all clocks stopped, with the exception of certain peripheral clocks such as I2C, I3C, UART, RTC, low-power timer, that can optionally be maintained active)
- Standby mode (V_{CORE} domain powered down)
- Battery backup mode (V_{BAT} domain only, supplied by an external battery)

Sleep and Stop low-power modes are entered by the MCU when executing the WFI (wait for interrupt) or WFE (wait for event) instructions, or when the SLEEPONEXIT bit of the Cortex®-M7 core is set after returning from an interrupt service routine.

The system can enter Stop or Standby when all EXTI wakeup sources are cleared.

Some GPIO pins can be used to monitor CPU low-power states:

Table 4. Overview of low-power mode monitoring pins

Power state monitoring pins	Description
PWR_CSLEEP	CPU clock OFF
PWR_CSTOP	CPU domain in low-power mode

3.7 Reset and clock controller (RCC)

The RCC manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and can be configured to apply clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable of working with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baud rate.

3.7.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, two internal oscillators with fast startup time and three PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock (1% accuracy)
  - 48 MHz RC oscillator
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - 4-50 MHz HSE clock
  - 32.768 kHz LSE clock

The RCC provides three PLLs: one for system clock, two for peripheral clocks.

The system starts on the HSI clock. The user application can then select the clock configuration.

A high precision can be achieved for the 48 MHz clock by using the embedded clock recovery system (CRS). It uses the OTG_FS_SOF (USB start of frame) signal, the LSE, or an external signal (CRS_SYNC) to fine-tune the oscillator frequency on-the-fly.

3.7.2 System reset sources

The power-on reset initializes all registers, while the system reset reinitializes the system except for:

- The debug
- Part of the RCC
- The power controller status registers
- The backup power domain

A system reset is generated in the following cases:

Prerelease product(s)

- Power-on reset (pwr_por_rst)
- Brownout reset
- Low level on NRST pin (external reset)
- Window watchdog
- Independent watchdog
- Software reset
- Low-power mode security reset
- Exit from Standby

3.8 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as:

- Output (push-pull or open-drain, with or without pull-up or pull-down)
- Input (floating, with or without pull-up or pull-down)
- Peripheral alternate function

Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption, and electromagnetic emission.

After reset, all GPIOs are in analog mode to reduce power consumption.

The I/O configuration can be locked if needed by following a specific sequence to avoid spurious writing to the I/Os registers.

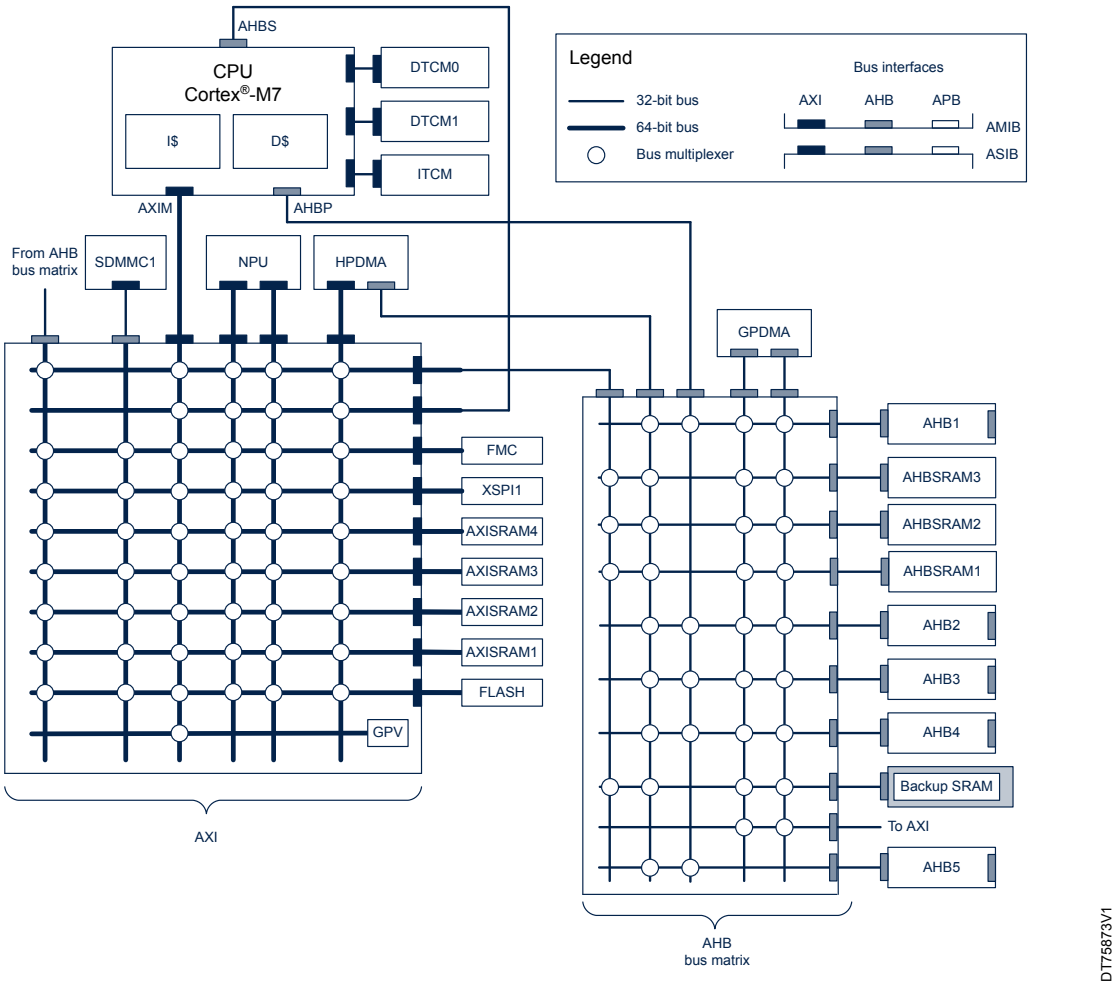
To maximize the performance, the I/O high-speed feature, HSLV, can be activated at low device supply voltage (V_{DD} < 2.7 V). This is needed to achieve the performance required for peripherals such as the SDMMC, FMC, and XSPI.

3.9 Bus-interconnect matrix

The devices feature an AXI bus matrix, an AHB bus matrix, and bus bridges that allow bus masters to interconnect with memory and peripherals (see Figure 4).

Prerelease product(s)

Figure 4. **STM32H7Pxxx bus matrix**



3.10 DMA controllers

The devices feature two DMA instances to perform background transfers between memories and/or peripherals and thereby offload the CPU.

- A high-performance direct memory access (HPDMA) controller
  The HPDMA has two bus master ports, one connected to the AXI matrix and one to the AHB matrix. This prioritizes bulk data transfers between AXI memories (AXISRAM, embedded flash, external flash/SRAM) and the CPU tightly coupled memories (ITCM, DTCM). It can manage up to 16 channels. Four channels have a 64-byte FIFO and support 2D addressing. The remaining channels have a 16-byte FIFO and support fixed increment addressing.
- A general-purpose direct memory access (GPDMA) controller
  The GPDMA has two bus leader ports, both connected to the AHB matrix. This is intended for peripheral-to-memory and memory to peripheral data transfers. It can manage up to 16 channels. Four channels have a 32-byte FIFO and support 2D addressing. The remaining channels have an 8-byte FIFO and support fixed increment addressing.

Both DMA controllers receive the same DMA requests and trigger signals from peripherals.

3.11 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller which can manage 16 priority levels and handle up to 184 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

Prerelease product(s)

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.12 Extended interrupt and event controller (EXTI)

The EXTI controller performs interrupt and event management. In addition, it can wake up the processor, power domains and/or SRD domain from Stop mode.

The EXTI handles up to 78 independent event/interrupt lines split into 34 configurable events and 44 direct events.

Configurable events have dedicated pending flags, active edge selection, and software trigger capable. Direct events provide interrupts or events from peripherals having a status flag.

3.13 Neural-ART Accelerator (NPU)

Neural-ART Accelerator is a branded family of design-time parametric and runtime reconfigurable neural processing unit (NPU) cores. These cores are specifically designed to accelerate (in area-constrained embedded and IoT devices) the inference execution of a wide range of quantized convolutional neural network (CNN) models.

The NPU implemented in the STM32H7Pxxx is configured with the following functional units:

- Stream switch - connects output stream link ports to input stream link ports
- Convolutional accelerator - implements clusters of multiply-accumulate (MAC) engines supporting fixed-point acceleration of the 3×3 convolutions. It can be configured as 16- or 8-bit MACs
- Pooling unit - 2D windowed (MxN) min, max, average pooling, as well as global max, min, or average pooling
- Activation unit - compute ReLU-like activations such as plain, parametric, and thresholded ReLUs. There is also a generic function evaluator using a second-degree piece-wise polynomial approximation ($y = ax^2 + bx + c$ or $y = (ax + b) \times x + c$)
- 2 scalar arithmetic units: $x \times y$; MIN(x,y); MAX(x,y); logical AND, OR, NOT; bitwise AND, OR, XOR, NOT; comparison operations like =, <, ≥, >; ABS(x); SIGN(x), CLIP(x)
- Six stream engines with embedded encryption/decryption
- Dual 64-bit AXI interface
- Epoch controller
- Debug controller

The Neural-ART Accelerator is configured using the ST Edge AI tool suite.

3.14 Hardware signal processor (HSP)

The hardware signal processor (HSP) is a signal coprocessor engine. The HSP is built around a dedicated high-performance signal processor engine (SPE) working in 32-bit floating-point or 8-bit integer data. The HSP embeds a library of more than 70 built-in standard functions, optimized for signal processing operations such as: FFT, DCT, filtering.

In addition, the HSP also embeds functions dedicated to neural network, working on 8-bit integer. The most commonly used operations are supported such as 2D convolution, depth-wise convolution, point-wise convolution. HSP is supported by the STM32 CubeAI software, allowing implementation of complete neural networks.

The HSP can be used as an accelerator leveraging significantly the computing possibilities of the circuit. The HSP can also work autonomously thanks to its sequencer. The sequencer allows the application to record at any time a sequence of operations and execute this sequence when a specific event is activated. The application can record up to 37 sequences, making the HSP more than just an accelerator.

The HSP has a dedicated SRAM, which is available for use by the system when the HSP is not used.

Prerelease product(s)

3.15 Filter math accelerator (FMAC)

The filter math accelerator unit performs 16-bit fixed-point arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit, together with address generation logic which allows it to index vector elements held in local memory.

The unit includes support for circular buffers on input and output, which allows digital filters to be implemented. Both finite and infinite impulse response filters can be realized.

The unit allows frequent or lengthy filtering operations to be offloaded from the CPU, freeing up the processor for other tasks. In many cases it can accelerate such calculations compared to a software implementation, resulting in a speed-up of time critical tasks.

- 16 × 16-bit multiplier
- 24 + 2-bit accumulator with addition and subtraction
- 16-bit input and output data
- 256 × 16-bit local memory
- Up to three areas can be defined in memory for data buffers (two inputs, one output), defined by programmable base address pointers and associated size registers
- Input and output buffers can be circular
- Filter functions: FIR, IIR (direct form 1)
- Vector functions: dot product, convolution, correlation
- AHB slave interface
- DMA read and write data channels

3.16 CORDIC coprocessor (CORDIC)

The CORDIC coprocessor provides hardware acceleration of mathematical functions (mainly trigonometric ones) commonly used in motor control, metering, signal processing, and many other applications.

It speeds up the calculation of these functions compared to a software implementation, making possible the use of a lower operating frequency, or freeing up processor cycles to perform other tasks.

- 24-bit CORDIC rotation engine
- Circular and Hyperbolic modes
- Rotation and Vectoring modes
- Functions: sine, cosine, sinh, cosh, atan, atan2, atanh, modulus, square root, natural logarithm
- Programmable precision
- Low latency AHB slave interface
- Results can be read as soon as ready, without polling or interrupt
- DMA read and write channels
- Multiple register read/write by DMA

3.17 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to obtain a CRC code using a programmable polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.18 Flexible memory controller (FMC)

The FMC controller main features are the following:

Prerelease product(s)

- Interface with static-memory mapped devices including:
  - Static random-access memory (SRAM)
  - NOR flash memory/OneNAND flash memory
  - PSRAM (four memory banks)
  - NAND flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-bit data bus width
- Independent chip select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by 2.

3.19 Extended-SPI memory interface (XSPI)

The XSPI is a specialized communication interface targeting single, dual, quad, or octal SPI memories.

It supports single/dual/quad/octal SPI formats.

Multiplex of single/dual/quad/octal SPI over the same bus can be achieved using the integrated I/O manager. The XSPI can operate in any of the three following modes:

- Indirect mode: all the operations are performed using the XSPI registers
- Status-polling mode: the external memory status register is periodically read and an interrupt can be generated in case of flag setting
- Memory-mapped mode: the external memory is memory mapped and it is seen by the system as if it was an internal memory supporting both read and write operations.

The XSPI supports two frame formats supported by most external serial memories such as serial PSRAMs, serial NOR flash memories, HyperRAM™ and HyperFlash™ memories:

- The classical frame format with the command, address, alternate byte, dummy cycles, and data phase
- The HyperBus™ frame format

3.20 Analog-to-digital converters (ADC)

The STM32H7Pxxx devices embed four analog-to-digital converters, whose resolution can be configured to 12, 10, 8 or 6 bits. Each ADC shares up to 18 external channels, performing conversions in single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller, allowing automatic transfer of ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM3, TIM4, TIM6, TIM8, TIM9, TIM15, TIM20 and LPTIM1 timers, as well as the high-resolution timers HRTIM1/2.

3.21 Analog temperature sensor

The STM32H7Pxxx embeds an analog temperature sensor that generates a voltage (V_{TS}) that varies linearly with the temperature. This temperature sensor is internally connected to ADC1_IN16. The conversion range is between 1.7 V and 3.6 V. It can measure the device junction temperature ranging from -40 to +125°C.

The temperature sensor has good linearity, but it has to be calibrated to obtain a good overall accuracy of the temperature measurement. As the temperature sensor offset varies from device to device due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

Prerelease product(s)

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, which is accessible in read-only mode.

3.22 Digital temperature sensor (DTS)

The STM32H7Pxxx embeds a sensor that converts the temperature into a square wave whose frequency is proportional to the temperature. The PCLK or the LSE clock can be used as reference clock for the measurements. A formula given in the product reference manual (RM0455) allows the temperature to be calculated according to the measured frequency stored in the DTS_DR register.

3.23 V_{BAT} operation

The V_{BAT} power domain contains the RTC, the backup registers, and the backup SRAM.

To optimize battery duration, this power domain is supplied by V_{DD} when available or by the voltage applied on VBAT pin (when V_{DD} supply is not present). V_{BAT} power is switched when the PDR detects that V_{DD} dropped below the PDR level.

The voltage on the VBAT pin can be provided by an external battery, a supercapacitor or directly by V_{DD}. In the latter case, V_{BAT} mode is not functional.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC, the backup registers, and the backup SRAM.

The devices embed an internal V_{BAT} battery charging circuitry that can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from V_{BAT}, the external interrupts and RTC alarm/events do not wake it from V_{BAT} mode.

3.24 Digital-to-analog converters (DAC)

The devices feature one dual-channel buffered DAC (DAC1) and three dual-channel unbuffered DACs (DAC2-4). Each dual-channel DAC contains two digital-to-analog converters.

The two buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. They can also be used to generate reference voltages for the embedded comparators (COMP1-6).

The six unbuffered DAC channels are only connected to the embedded comparators (COMP1-8).

The following features are supported by all DAC channels:

- 8-bit or 12-bit monotonic output
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual channel pairs support independent or simultaneous conversions
- DMA capability for each channel including underrun error detection
- External triggers for conversion
- External voltage reference input V_{REF+} or internal V_{REFBUF} reference

The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

3.25 Voltage reference buffer (VREFBUF)

The built-in voltage reference buffer can be used as voltage reference for ADCs and DACs, as well as voltage reference for external components through the VREF+ pin.

Five different voltages are supported (refer to the reference manual for details).

3.26 Ultralow-power comparators (COMP)

The STM32H7Pxxx devices embed eight rail-to-rail comparators. They feature programmable reference voltage (internal or external), hysteresis, and speed (low speed for low-power) as well as selectable output polarity.

The reference voltage can be one of the following:

Prerelease product(s)

- An external I/O
- A DAC output channel
- An internal reference voltage or submultiple (1/4, 1/2, 3/4)

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers, and be combined into a window comparator.

3.27 Audio digital filter (ADF)

The audio digital filter (ADF) is a high-performance module dedicated to the connection of external sigma-delta (ΣΔ) modulators. The ADF implements a single interface and filter.

3.28 True random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit. The RNG is a true random number generator that provides full entropy outputs to the application as 32-bit samples. It is composed of a live entropy source (analog) and an internal conditioning component.

3.29 Cryptographic acceleration (HASH)

The devices embed a cryptographic processor that supports the advanced cryptographic algorithms usually required to ensure authentication and data integrity:

- Universal HASH
  - SHA-1 and SHA-2 (secure HASH algorithms)
  - MD5
  - HMAC

3.30 Timers and watchdogs

The devices include three advanced-control timers, 13 general-purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

All timer counters can be frozen in Debug mode.

Table 5 compares the features of the advanced-control, general-purpose, basic, and low-power timers.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary outputs
High resolution	HRTIM1/2	16-bit	Up, Down, Up/ down	1, 2, 4	Yes	12	6
Advanced-control	TIM1/8/20	16-bit	Up, Down, Up/ down	Any integer between 1 and 65536	Yes	7	4
General purpose	TIM2/3/4/5	32-bit	Up, Down, Up/ down	Any integer between 1 and 65536	Yes	4	No
	TIM9/12	16-bit	Up	Any integer between 1 and 65536	No	2	No
	TIM10/11/13/14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TIM15	16-bit	Up, Down, Up/ down	Any integer between 1 and 65536	Yes	2	1
	TIM16/17	16-bit	Up, Down, Up/ down	Any integer between 1 and 65536	Yes	1	1
Basic	TIM6/7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Prerelease product(s)

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Comple-mentary outputs
Low-power timer	LPTIM1/2/3	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	2	No
	LPTIM4/5/6	16-bit	Up	1, 2, 4, 8, 16, 32, 64, 128	No	0	No

3.30.1 High-resolution timer (HRTIM1/2)

The high-resolution timer (HRTIM) is a versatile digital signal generator that provides multiple types of control signals, including duty cycle, frequency, or phase modulation. These signals can also be externally constrained, for example, by current limits or zero-crossing detection.

HRTIM consists of seven timers: one master and six slaves. It offers twelve high-resolution outputs (channels CHA1/CHA2 to CHF1/CHF2), which can be coupled as complementary pairs with deadtime insertion. The timer features eight fault inputs for protection and sixteen inputs to handle external events, such as current limitation, zero voltage, or zero current switching. Each fault and external event input can connect to peripherals, such as on-chip comparators.

The HRTIM timer kernel operates at up to 520 MHz, providing a resolution down to 1.9 ns for both outputs and capture inputs. This resolution is available in all operating modes, including variable duty cycle, variable frequency, variable phase, and constant ON/OFF time. The slave timers can be synchronized and combined to control large multi-switch or multi-level converters (up to 24 channels), or operate independently to manage multiple single or dual-switch converters.

Waveforms are defined by a combination of user-defined timings and external events, such as analog or digital feedback signals. HRTIM includes options for blanking and filtering spurious events or faults. It offers multiple features to offload the CPU, including DMA requests, burst mode controller, push-pull, auto-delayed and topology-specific protection schemes. HRTIM supports a wide variety of topologies, including LLC, totem pole PFC, buck or boost converters, in voltage or current mode. It is also suitable for controlling multi-level topologies, including a dedicated protection mode for NPC inverters.

HRTIM is designed for digital power applications, including lighting and welding, digital power supplies for telecom and data centers, single or three-phase PFC, three-phase UPS, solar applications (MPPT and grid-tied inverters), and energy storage systems.

In debug mode, HRTIM counters can be frozen, and the PWM outputs enter a safe state.

3.30.2 Advanced-control timers (TIM1, TIM8, TIM20)

The advanced-control timers (TIM1, TIM8, TIM20) can be seen as three-phase PWM generators multiplexed on six channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their seven independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timers can work together with the general-purpose timers via the timer link feature for synchronization or event chaining.

The advanced-control timers support independent DMA request generation.

3.30.3 General-purpose timers

There are 13 general-purpose timers embedded in the STM32H7Pxxx devices (see Table 5. Timer feature comparison for differences). All general purpose and advanced control timers share the same clock which operates at the CPU frequency, allowing synchronized operation.

Prerelease product(s)

- **TIM2, TIM3, TIM4, and TIM5**
  The devices include four full-featured general-purpose timers: TIM2, TIM3, TIM4, and TIM5. These timers are based on a 32-bit auto reload up/down counter and a 16-bit prescaler. All timers feature four independent channels for input capture/output compare, PWM, or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.
  TIM2, TIM3, TIM4, and TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers (TIM1, TIM8, TIM20) via the timer link feature for synchronization or event chaining.
  Any of these general-purpose timers can be used to generate PWM outputs.
  TIM2, TIM3, TIM4, and TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from one to four hall-effect sensors.
- **TIM9, TIM10, TIM11, IM12, TIM13, TIM14, TIM15, TIM16, and TIM17**
  These timers are based on a 16-bit auto reload upcounter and a 16-bit prescaler. TIM10, TIM11, TIM13, TIM14, TIM16, and TIM17 feature one independent channel, whereas TIM9, TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or one-pulse mode output. TIM15, TIM16, and TIM17 also feature complementary outputs with dead time insertion.

3.30.4 Basic timers (TIM6, TIM7)

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

3.30.5 Low-power timers (LPTIM1-6)

The low-power timers feature an independent clock and can operate in Stop mode if they are clocked by LSE, LSI, or an external clock. The low-power timers can wake up the devices from Stop mode.

The low-power timers support the following features:

- 16-bit up counter with 16-bit auto reload register
- 16-bit compare register
- Input capture (LPTIM1-3)
- Configurable output: pulse, PWM
- Continuous/one-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
  - Internal clock source: LSE, LSI, HSI, or APB clock
  - External clock source over LPTIM input (working even with no internal clock source running, used by the pulse counter application)
- Programmable digital glitch filter
- Encoder mode (LPTIM1-3)

3.30.6 Independent watchdog

The independent watchdog is based on a 12-bit down counter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.30.7 Window watchdog

The window watchdog is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.30.8 SysTick timer

This timer is intended for real-time operating systems, but can also be used as a standard down counter. It features:

Prerelease product(s)

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.31 Real-time clock (RTC)

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Two programmable alarms
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to V_{BAT} mode.
- 17-bit auto reload wake-up timer (WUT) for periodic events with programmable resolution and period

The RTC is supplied through a switch that takes power either from the V_{DD} supply when present or from the VBAT pin.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in V_{BAT} mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in V_{BAT} mode, but is functional in all low-power modes.

All RTC events (alarm, wake-up timer, timestamp, or tamper) can generate an interrupt and wake up the device from the low-power modes.

3.32 Tamper and backup registers (TAMP)

The TAMP main features are the following:

- 32 backup registers:
  - The backup registers (TAMP_BKPxR) are implemented in the RTC domain that remains powered-on by V_{BAT} when the V_{DD} power is switched off.
- Five external tamper detection events
  - Each external event can be configured to be active or passive
  - External passive tampers with configurable filter and internal pull-up
- Fifteen internal tamper events
- Any tamper detection can generate an RTC timestamp event
- Any tamper detection can erase the RTC backup registers, the backup SRAM, and the AXISRAM1
- Monotonic counter

3.33 Inter-integrated circuit interface (I2C)

The STM32H7Pxxx embeds three I2C interfaces.

The I2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration, and timing. The I2C peripheral supports:

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- I²C-bus rev 3 specification compatibility:
  - Target and controller modes, multicontroller capability
  - Standard mode (Sm), with a bit rate up to 100 Kbit/s
  - Fast mode (Fm), with a bit rate up to 400 Kbit/s
  - Fast mode plus (Fm+), with a bit rate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit target addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System management bus (SMBus) specification rev 3.3 compatibility:
  - Hardware PEC (packet error checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - Host and device support
  - SMBus alert
  - Timeout and idle condition detection
- Power system management protocol (PMBus™) specification rev 1.3 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wake-up from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

3.34 Improved inter-integrated circuit interface (I3C)

The I3C interface handles communication between this device and others, such as sensors and host processor, connected on an I³C bus.

The I3C SDR-only peripheral implements all the features required by the MIPI I³C specification v1.1.

It can control all I3C bus-specific sequencing, protocol, arbitration, and timing, and can act as controller, or as target.

When acting as a controller, the I3C peripheral improves the features of the I2C interface preserving some backward compatibility: it allows an I²C target to operate on an I³C bus in legacy I²C fast mode (Fm) or legacy I²C fast mode plus (Fm+), provided that the latter does not perform clock stretching.

The I3C peripheral can be used with DMA, to off-load the CPU.

The I3C peripheral supports:

- MIPI I³C specification v1.1 as:
  - I3C SDR-only primary controller
  - I3C SDR-only secondary controller
  - I3C SDR-only target
    - I3C SCL bus clock frequency up to 12.5 MHz
    - Queued data transfers:
      - Transmit FIFO (TX-FIFO) for data bytes/words to be transmitted on the I3C bus
      - Receive FIFO (RX-FIFO) for received data bytes/words on the I3C bus
      - For each FIFO, an optional DMA mode with a dedicated DMA channel
        - Queued control/status transfers, when controller:
          - Control FIFO (C-FIFO) for control words to be sent on the I3C bus
          - Optional status FIFO (S-FIFO) for status words as received on the I3C bus
          - For each FIFO, an optional DMA mode with a dedicated DMA channel
        - Messages:
          - Legacy I²C read/write messages to legacy I²C targets in Fm/Fm+
          - I3C SDR read/write private messages
          - I3C SDR broadcast CCC messages
          - I3C SDR read/write direct CCC messages

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3.35 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32H7Pxxx devices have five embedded universal synchronous receiver transmitters (USART1, USART2, USART3, USART6, and USART10) and five universal asynchronous receiver transmitters (UART4, UART5, UART7, UART8, and UART9). Refer to the table below for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS-485 driver enable. They are able to communicate at speeds of up to 10 Mbit/s.

USART1, USART2, USART3, USART6, and USART10 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

The USARTs embed a transmit FIFO (TXFIFO) and a receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

All USARTs have a clock domain independent from the CPU clock, allowing the USARTx to wake up the MCU from Stop mode. The wake-up from Stop modes are programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

All USART interfaces can be served by the DMA controller.

Table 6. USART features

X = supported.

USART modes/features	USART1/2/3/6/10	UART4/5/7/8/9
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode (Master/Slave)	X	-
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	X
LIN mode	X	X
Dual clock domain and wake-up from Low power mode	X	X
Receiver timeout interrupt	X	X
Modbus communication	X	X
Auto baud rate detection	X	X
Driver enable	X	X
USART data length	7, 8 and 9 bits	
Tx/Rx FIFO	X	X
Tx/Rx FIFO size	16	

3.36 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-power UART (LPUART1). The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUART embeds a transmit FIFO (TXFIFO) and a receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

The LPUART has a clock domain independent from the CPU clock and can wake up the system from Stop mode. The wake-up from Stop mode is programmable and can be done on:

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- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baud rate.

LPUART interface can be served by the DMA controller.

3.37 Serial peripheral interfaces (SPI) / integrated interchip sound interfaces (I2S)

The devices feature up to six SPIs (SPI1/I2S1, SPI2/I2S2, SPI3/I2S3, and SPI4, SPI5, SPI6) that allow communicating up to 125 Mbit/s in master and slave modes, in half-duplex, full-duplex, and simplex modes. The 3-bit prescaler gives eight master mode frequencies and the frame is configurable from 4 to 32 bits for SPI1/I2S1, SPI2/I2S2, SPI3/I2S3, from 4 to 16 bits for the others. All SPI interfaces support NSS pulse mode, TI mode, hardware CRC calculation, and 16× 8-bit embedded Rx and Tx FIFOs (SPI1/I2S1, SPI2/I2S2, SPI3/I2S3) or 8× 8-bit embedded Rx and Tx FIFOs (SPI4, SPI5, SPI6/I2S6), all with DMA capability.

Three standard I2S interfaces (multiplexed with SPI1, SPI2, SPI3) are available. They can be operated in master or slave mode, in simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When one or all I2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/codec at 256 times the sampling frequency. All I2S interfaces support 16x 8-bit embedded Rx and Tx FIFOs with DMA capability.

3.38 SD/SDIO/MMC card host interface (SDMMC)

The SD/SDIO, embedded MultiMediaCard (*e*•MMC) host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards and *e*•MMC devices.

The SDMMC features include the following:

- Compliance with Embedded MultiMediaCard System Specification Version 5.1. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit. (HS200 SDMMC_CK speed limited to maximum allowed I/O speed)(HS400 is not supported).
- Full compatibility with previous versions of MultiMediaCards (backward compatibility).
- Full compliance with SD memory card specifications version 6.0. (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode, and UHS-II mode not supported).
- Full compliance with SDIO card specification version 4.0. Card support for two different databus modes: 1-bit (default) and 4-bit (SDR104 SDMMC_CK speed limited to maximum allowed I/O speed, SPI mode and UHS-II mode not supported).
- Data transfer up to 208 Mbyte/s for the 8-bit mode (depending on maximum allowed I/O speed).
- Data and command output enable signals to control external bidirectional drivers.
- IDMA linked list support

The MultiMediaCard/SD bus connects cards to the host.

The current version of the SDMMC supports only one SD/SDIO/*e*•MMC card at any one time and a stack of *e*•MMC.

3.39 Controller area network (FDCAN1, FDCAN2, FDCAN3)

The controller area network (CAN) subsystem consists of three CAN modules, a shared message RAM, and a configuration block. Refer to the memory map for the base address of each of these parts. The modules (FDCAN) are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0. A 0.8-Kbyte message RAM per FDCAN instance is used for filtering, transmitting event FIFOs, and receiving and transmitting FIFOs.

3.40 USB on-the-go full-speed (OTG_FS)

The USB OTG is a dual-role device (DRD) controller that supports both device and host functions and is fully compliant with the On-The-Go supplement to the USB 2.0 specification. It can also be configured as a host-only or device-only controller, fully compliant with the USB 2.0 specification.

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OTG_FS supports 12 Mbps (full speed) in host configuration and device configuration, as well as 1.5 Mbps (low speed) in host configuration only.

The main features are:

- On-chip full-speed PHY interface
- Integrated support for A-B device identification (ID line)
- It allows the host to turn V_{BUS} off to conserve battery power in OTG applications
- It supports OTG monitoring of V_{BUS} levels with internal comparators
- It supports dynamic host-peripheral switch of role
- Software configurable as USB On-The-Go full-speed dual role device
- It supports FS SOF and LS keep-alives with SOF pulse PAD connectivity, SOF pulse internal connection to timer (TIMx), configurable framing period, and configurable end of frame interrupt
- It includes power-saving features such as system stop during USB suspend, switch-off of clock domains internal to the digital core, PHY, and DFIFO power management.
- It features a dedicated RAM of 1.25 Kbyte with advanced FIFO control:
  - Configurable partitioning of RAM space into different FIFOs for flexible and efficient use of RAM
  - Each FIFO can hold multiple packets
  - Dynamic memory allocation
  - Configurable FIFO sizes that are not powers of 2 to allow the use of contiguous memory locations
- It ensures max USB bandwidth for up to one frame (1 ms) without system intervention.
- It supports charging port detection as described in Battery Charging Specification Revision 1.2

3.41 Debug infrastructure

The devices offer a comprehensive set of debug and trace features to support software development and system integration.

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Single-wire trace port
- Parallel trace port
- Arm®CoreSight™ debug and trace components

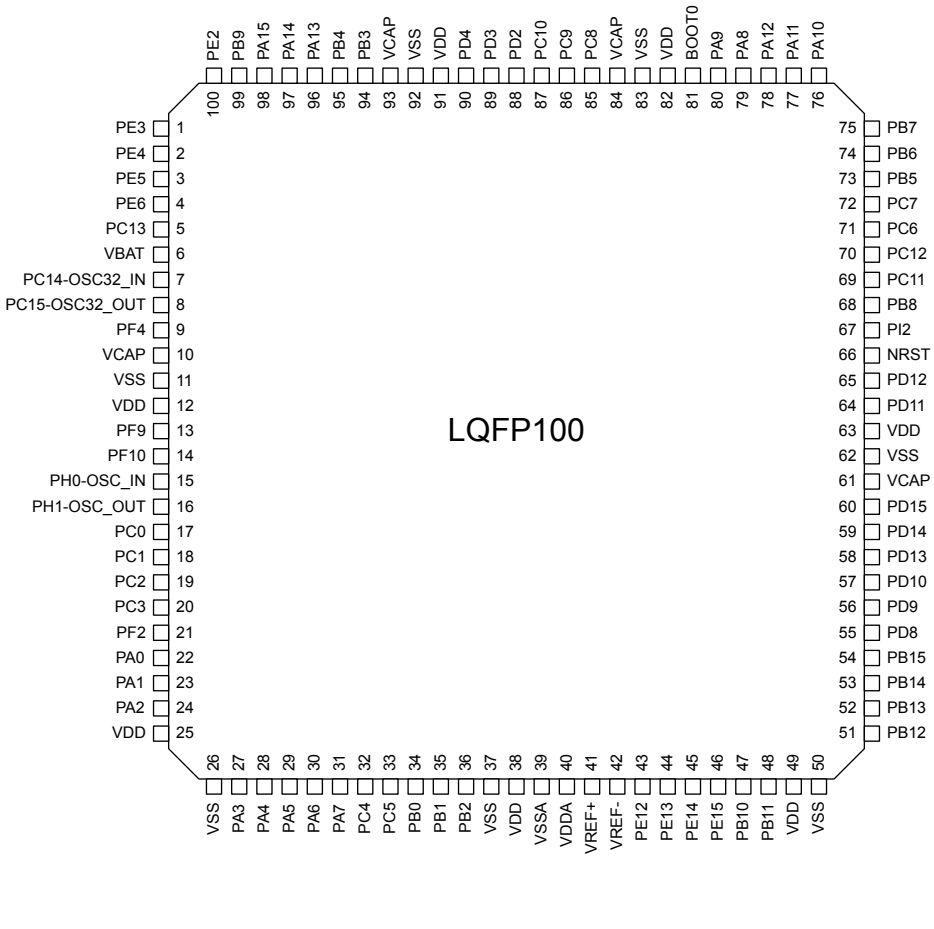
The debug can be controlled via a JTAG/Serial-wire debug access port, using industry-standard debugging tools. The trace port performs data capture for logging and analysis.

Prerelease product(s)

4 Pinouts/ballouts, pin description, and alternate functions

4.1 Pinout/ballout schematics

Figure 5. STM32H7Pxxx LQFP100 pinout

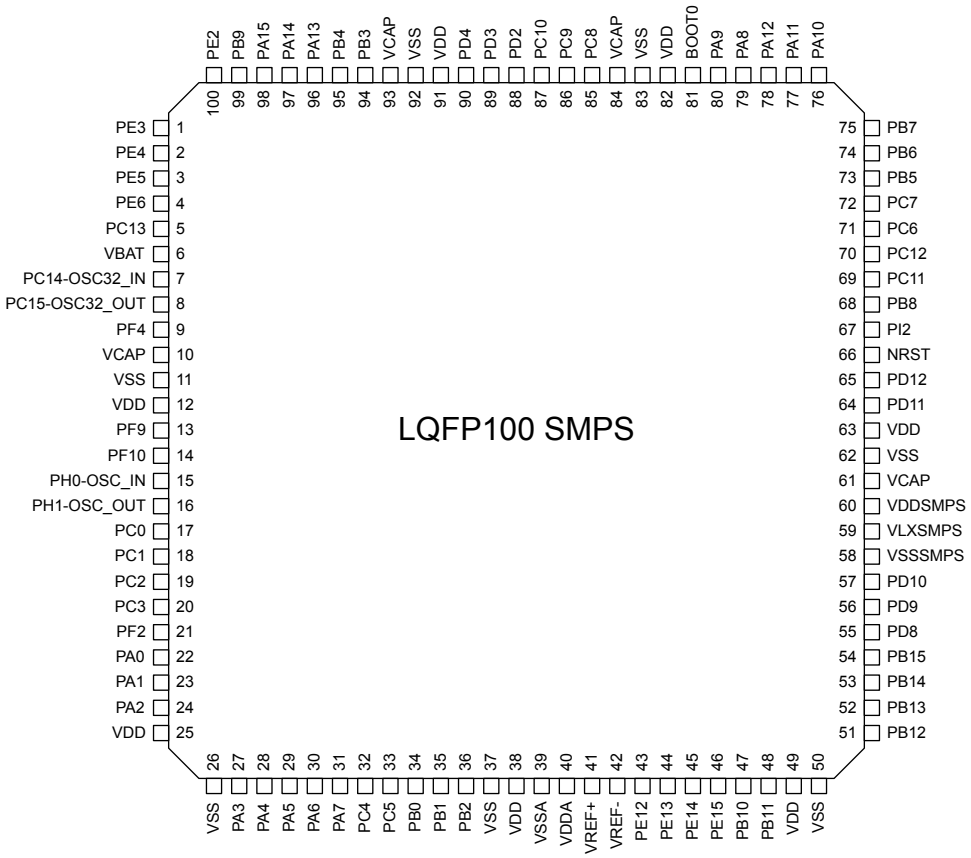


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1. *The above figure shows the package top view.*

Prerelease product(s)

Figure 6. STM32H7Pxxx LQFP100 SMPS pinout

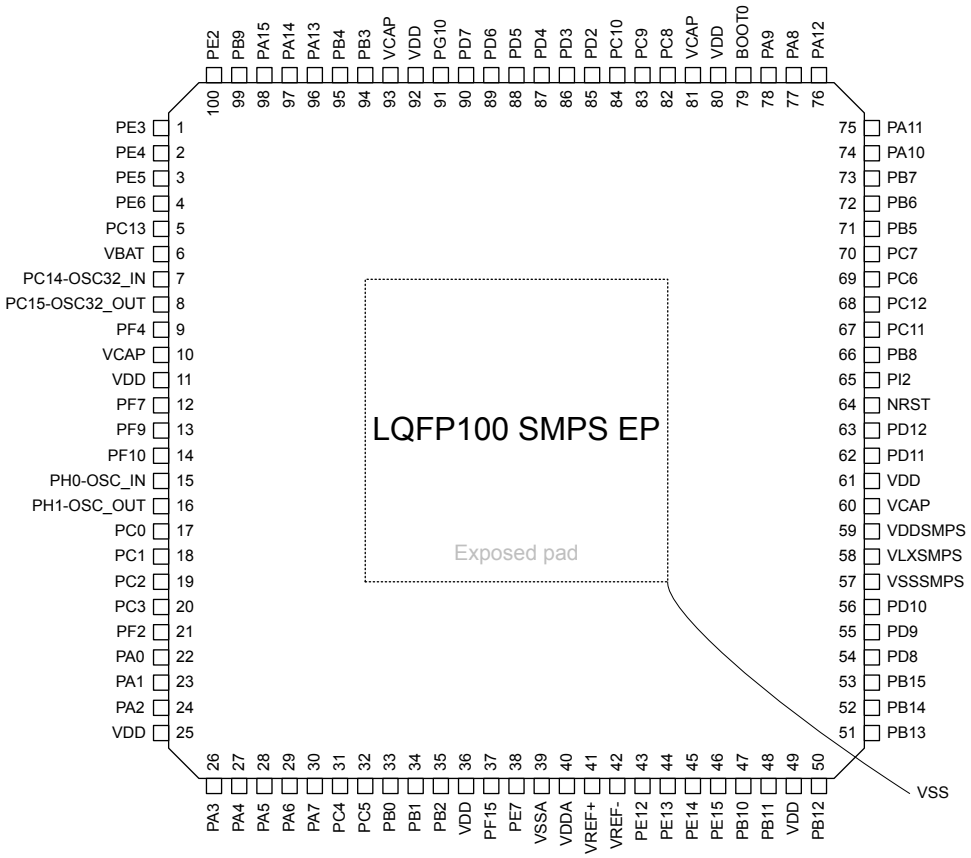


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1. *The above figure shows the package top view.*

Prerelease product(s)

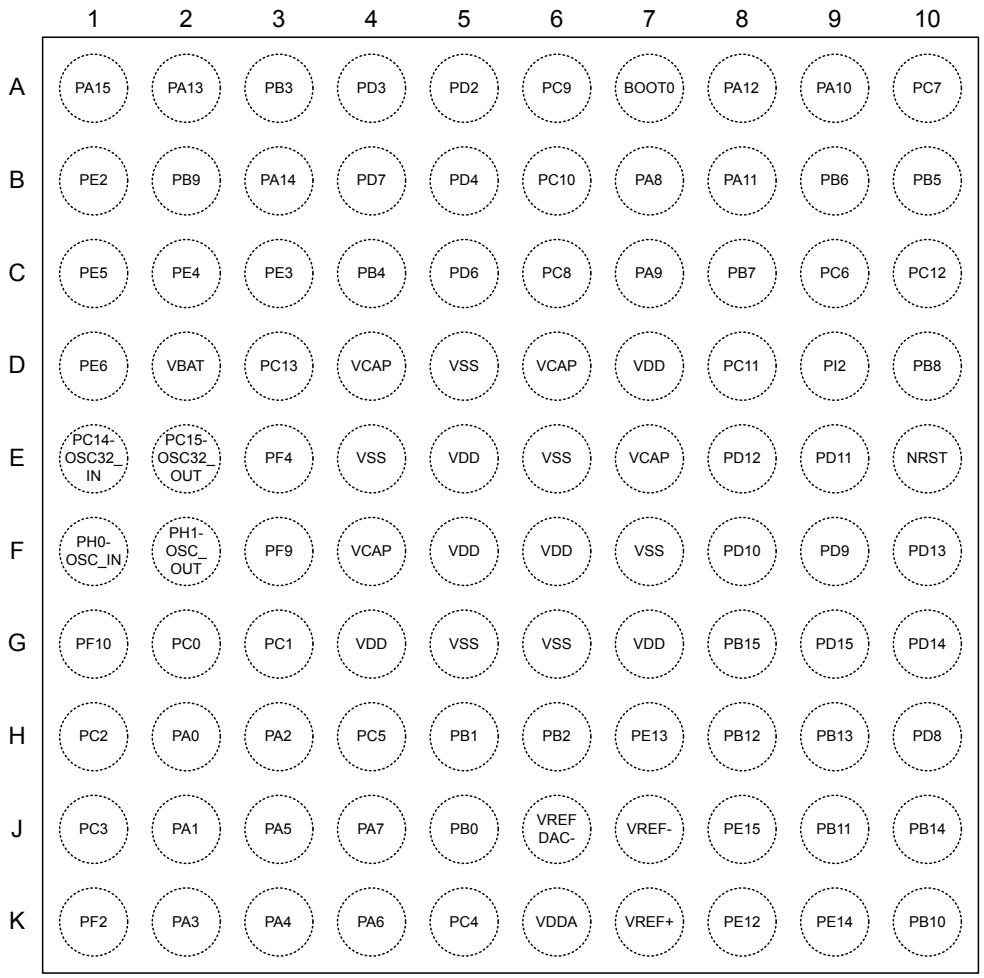
Figure 7. **STM32H7Pxxx LQFP100 SMPS EP pinout**



1. *The above figure shows the package top view.*

Prerelease product(s)

Figure 8. STM32H7Pxxx TFBGA100 ballout

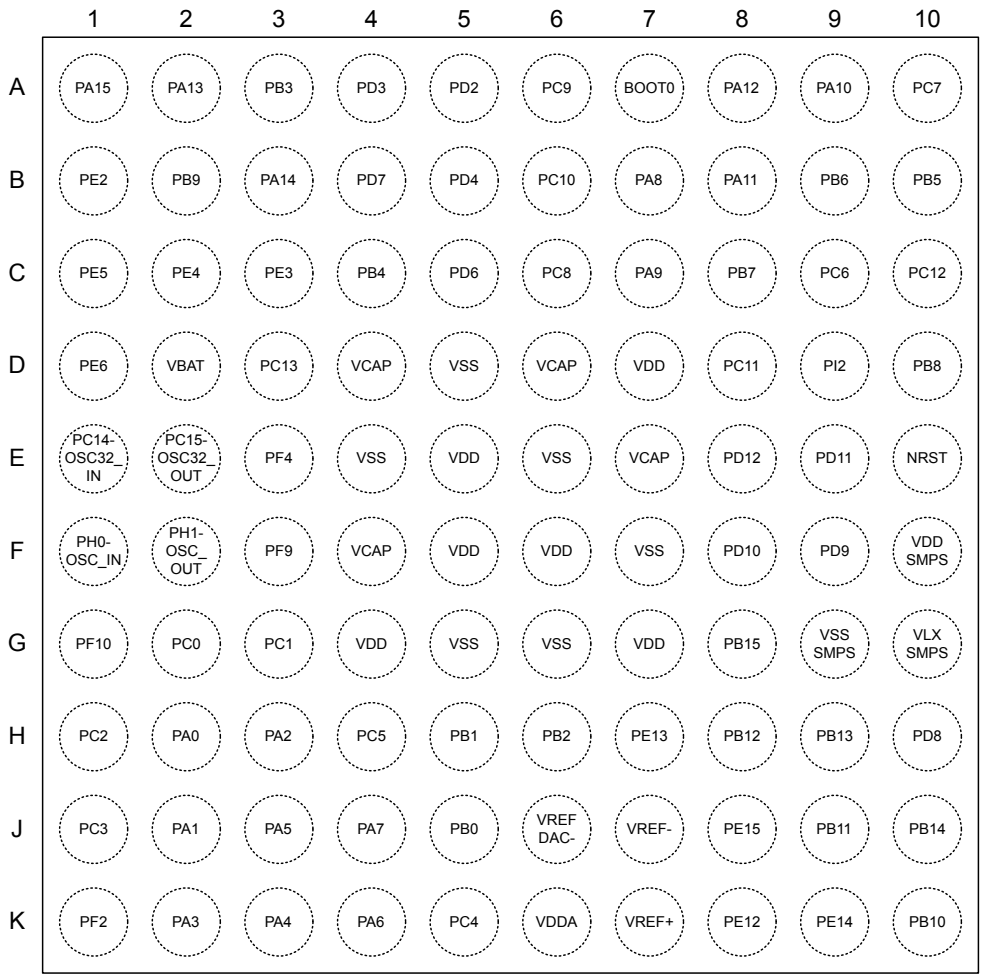


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1. *The above figure shows the package top view.*

Prerelease product(s)

Figure 9. **STM32H7Pxxx TFBGA100 SMPS ballout**

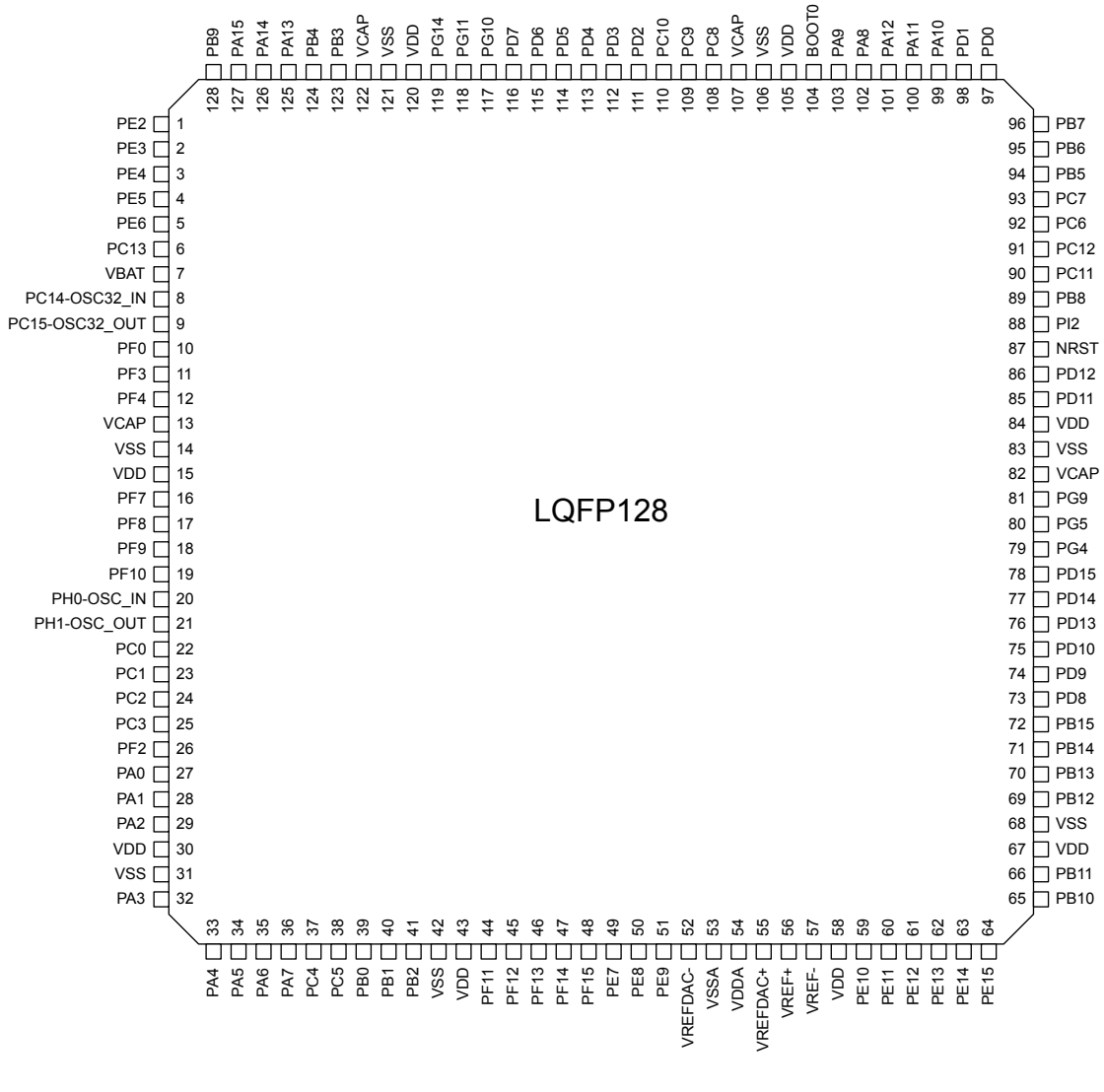


DT76673V1

1. *The above figure shows the package top view.*

Prerelease product(s)

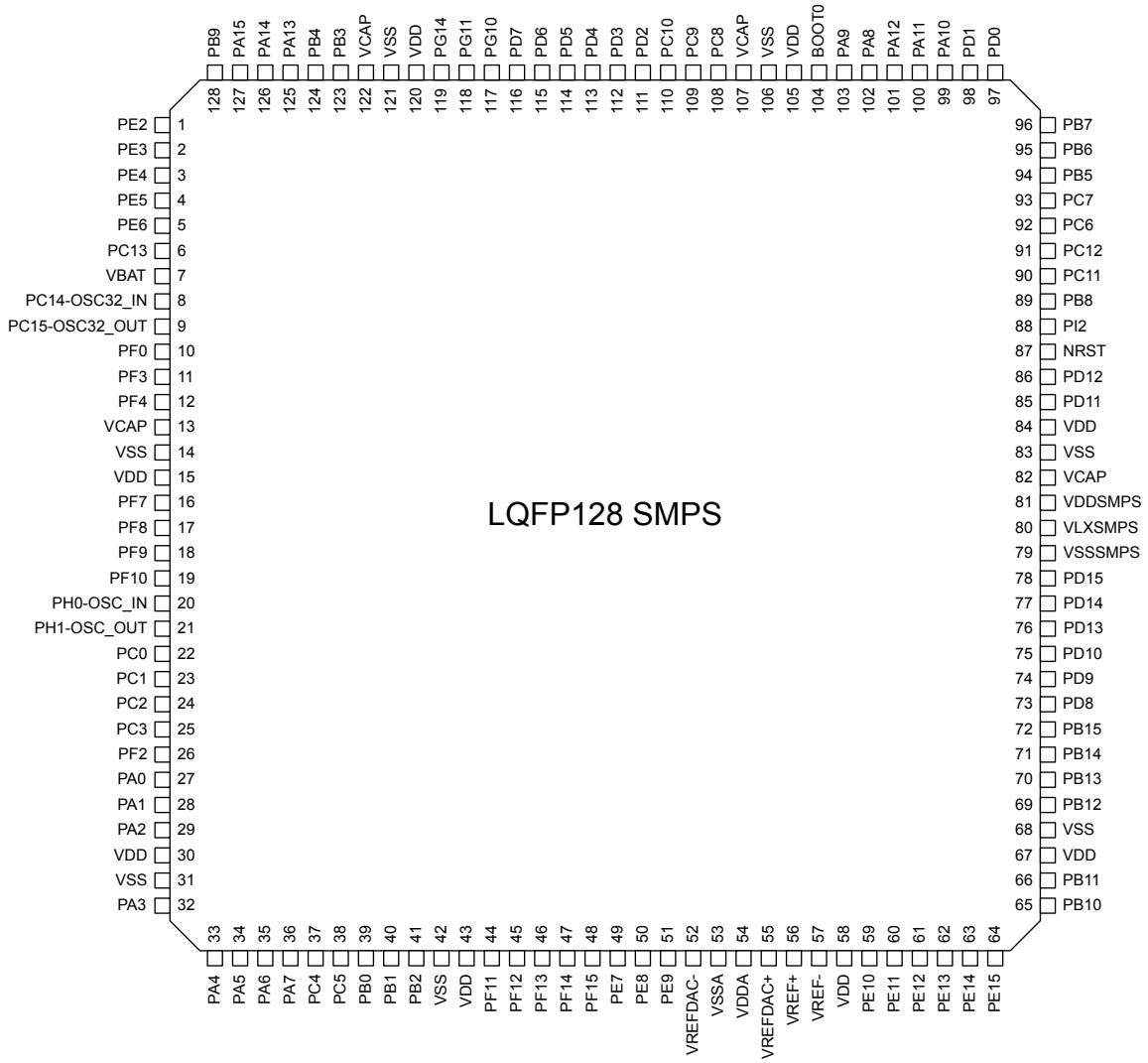
Figure 10. **STM32H7Pxxx LQFP128 pinout**



1. *The above figure shows the package top view.*

Prerelease product(s)

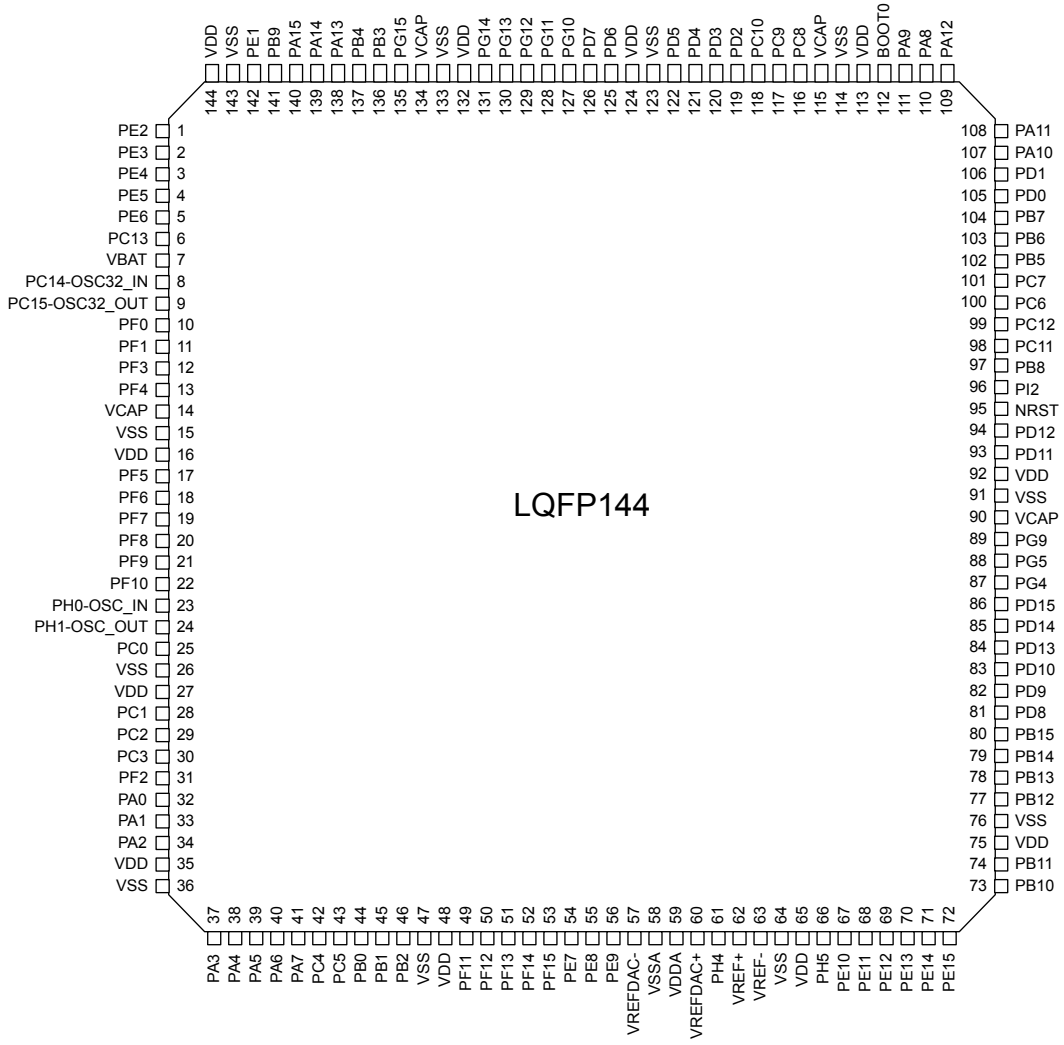
Figure 11. **STM32H7Pxxx LQFP128 SMPS pinout**



1. *The above figure shows the package top view.*

Prerelease product(s)

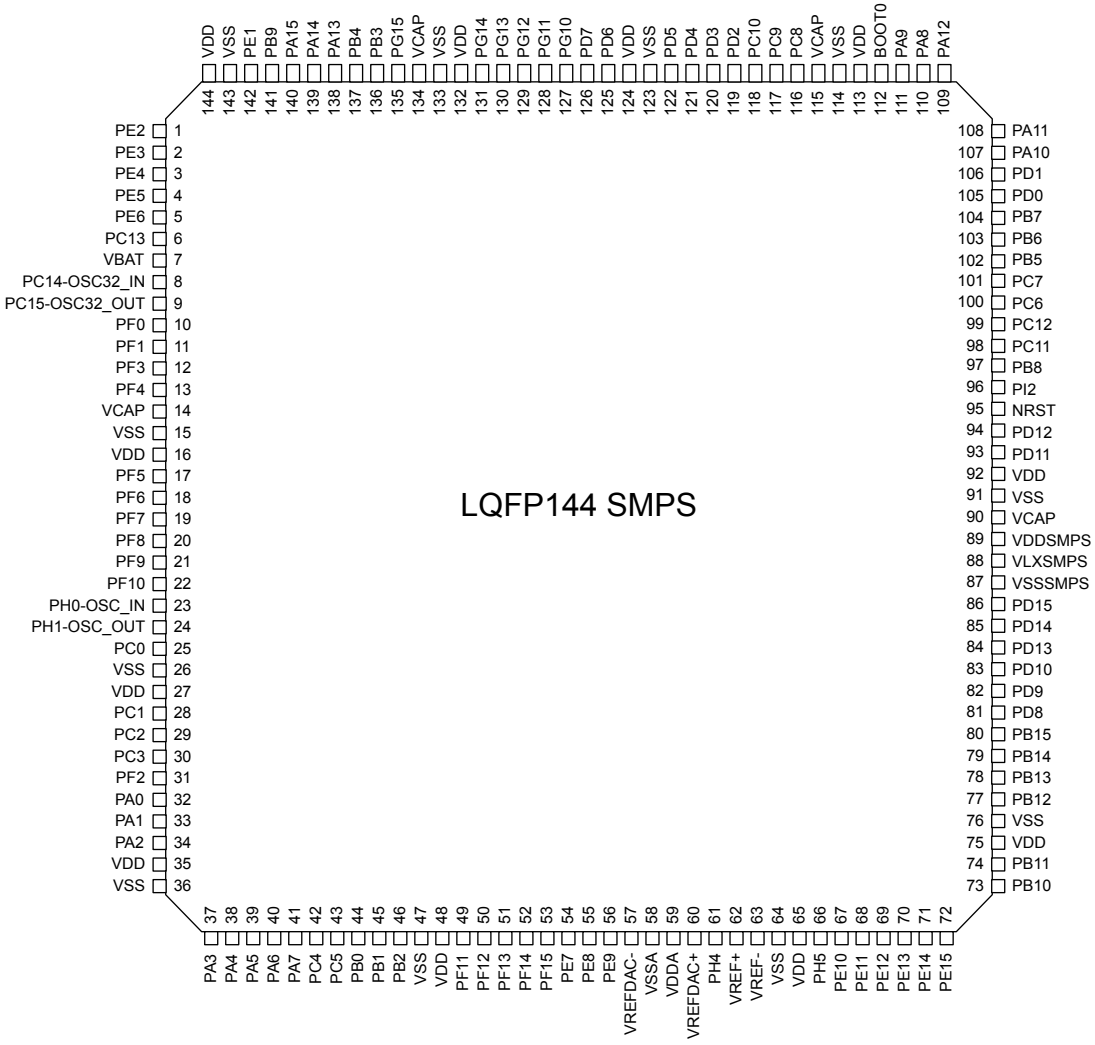
Figure 12. STM32H7Pxxx LQFP144 pinout



1. *The above figure shows the package top view.*

Prerelease product(s)

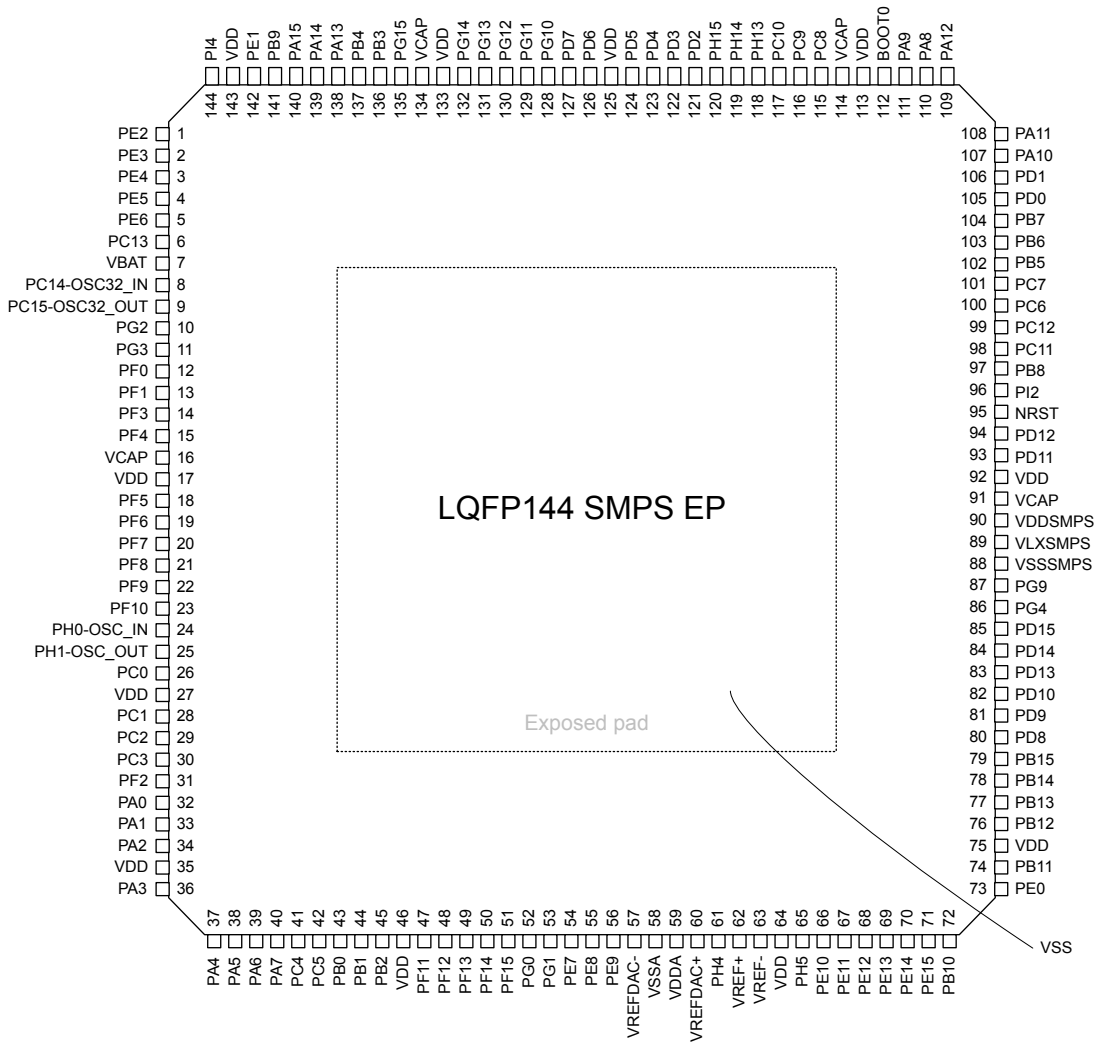
Figure 13. STM32H7Pxxx LQFP144 SMPS pinout



1. *The above figure shows the package top view.*

Prerelease product(s)

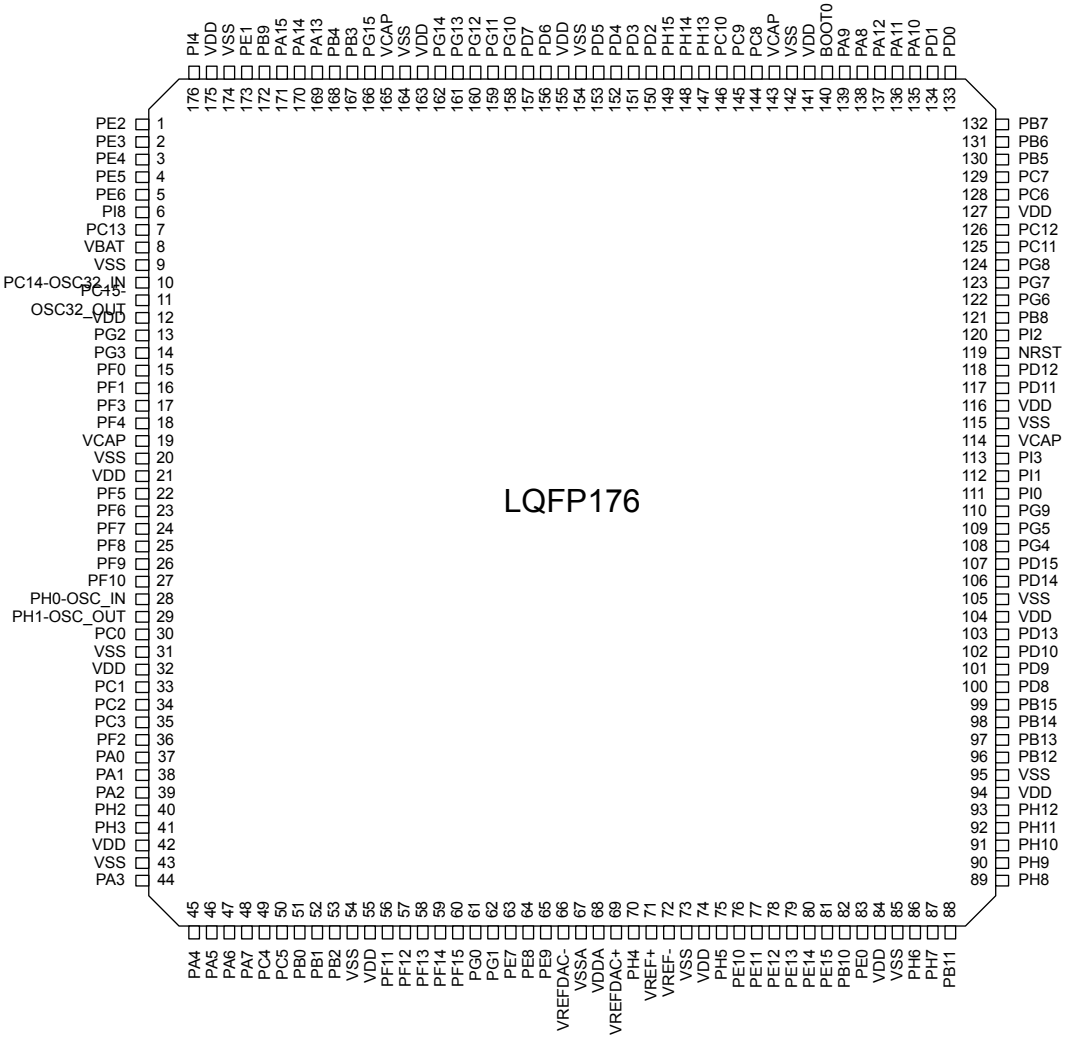
Figure 14. STM32H7Pxxx LQFP144 SMPS EP pinout



1. *The above figure shows the package top view.*

Prerelease product(s)

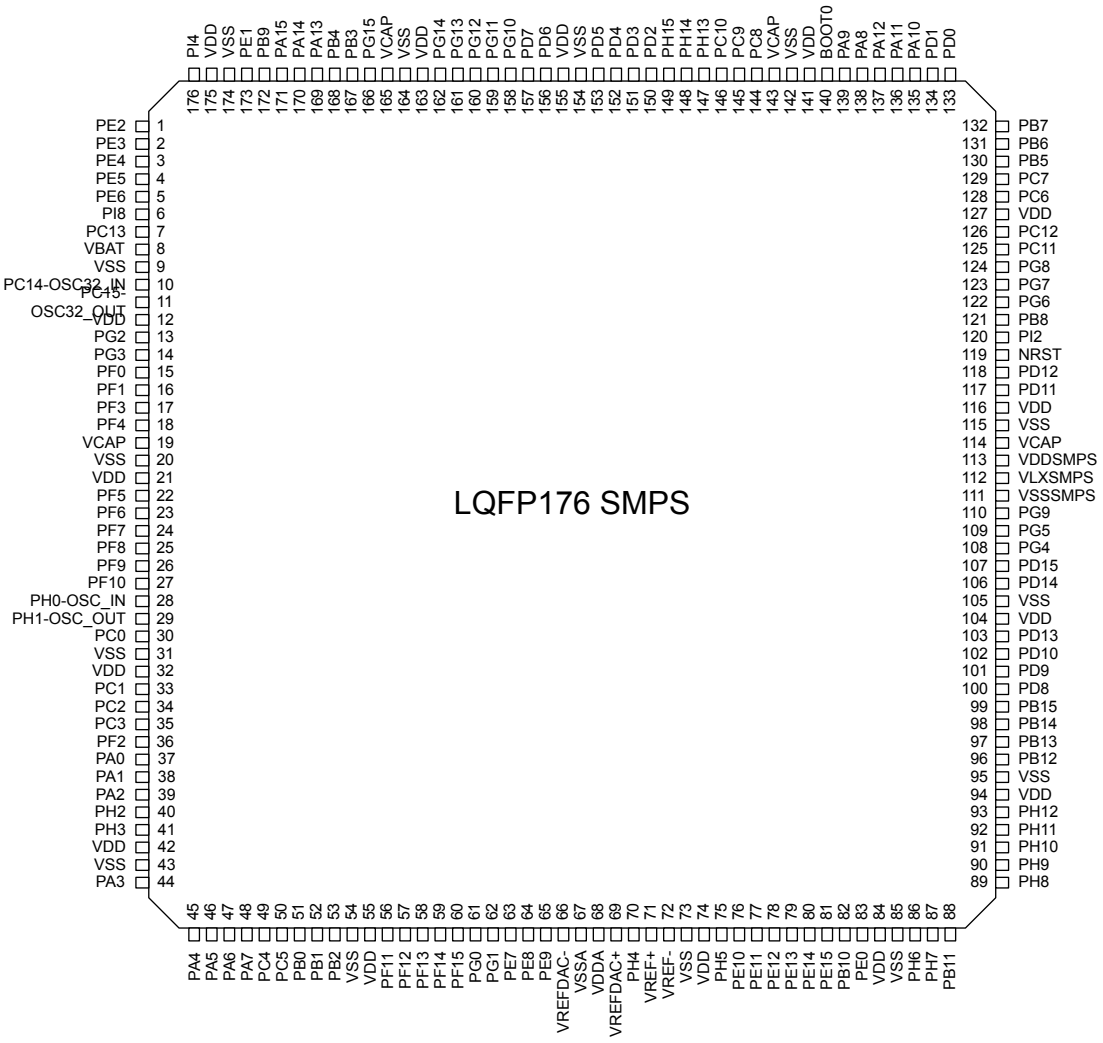
Figure 15. STM32H7Pxxx LQFP176 pinout



1. *The above figure shows the package top view.*

Prerelease product(s)

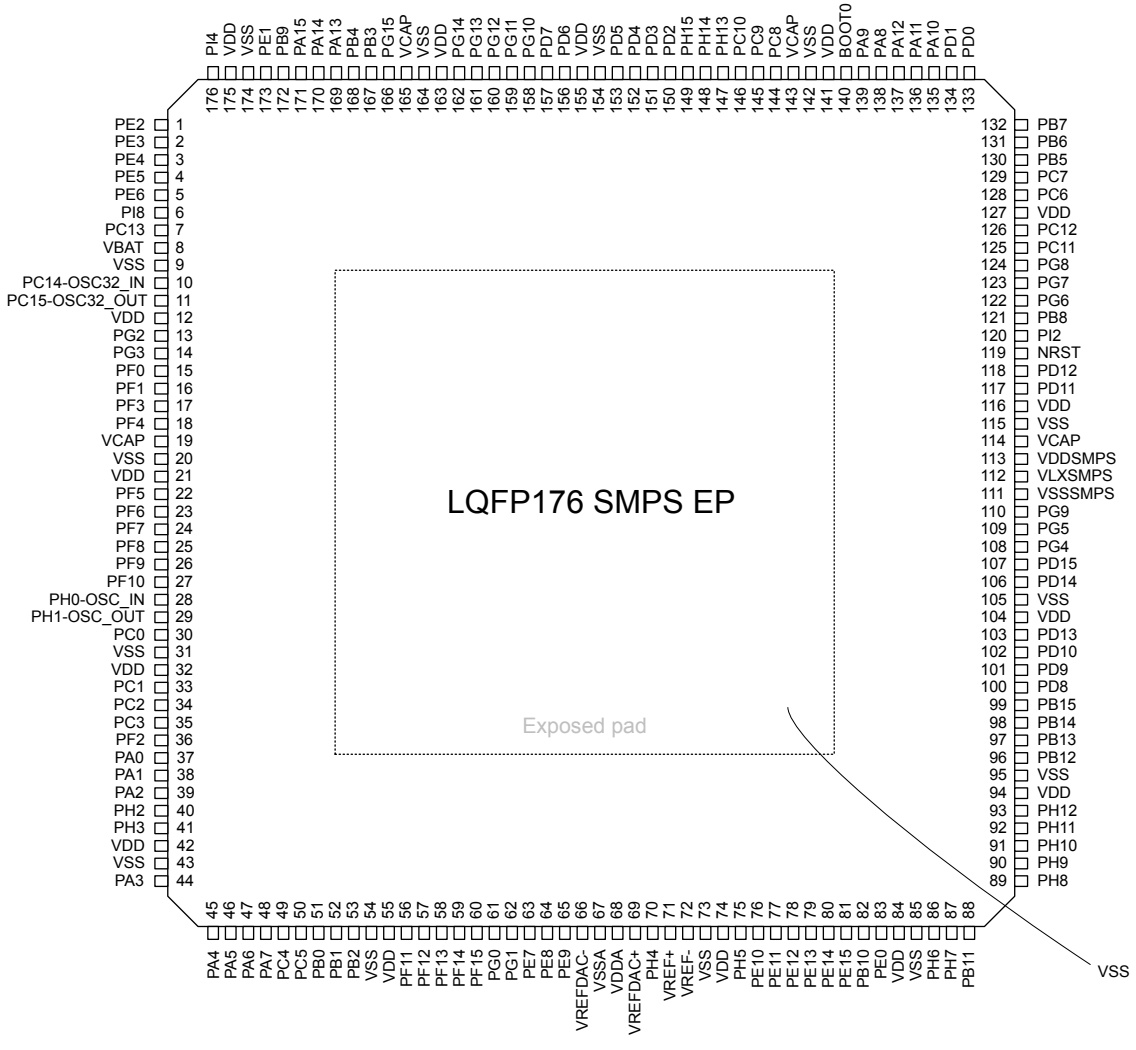
Figure 16. STM32H7Pxxx LQFP176 SMPS pinout



1. The above figure shows the package top view.

Prerelease product(s)

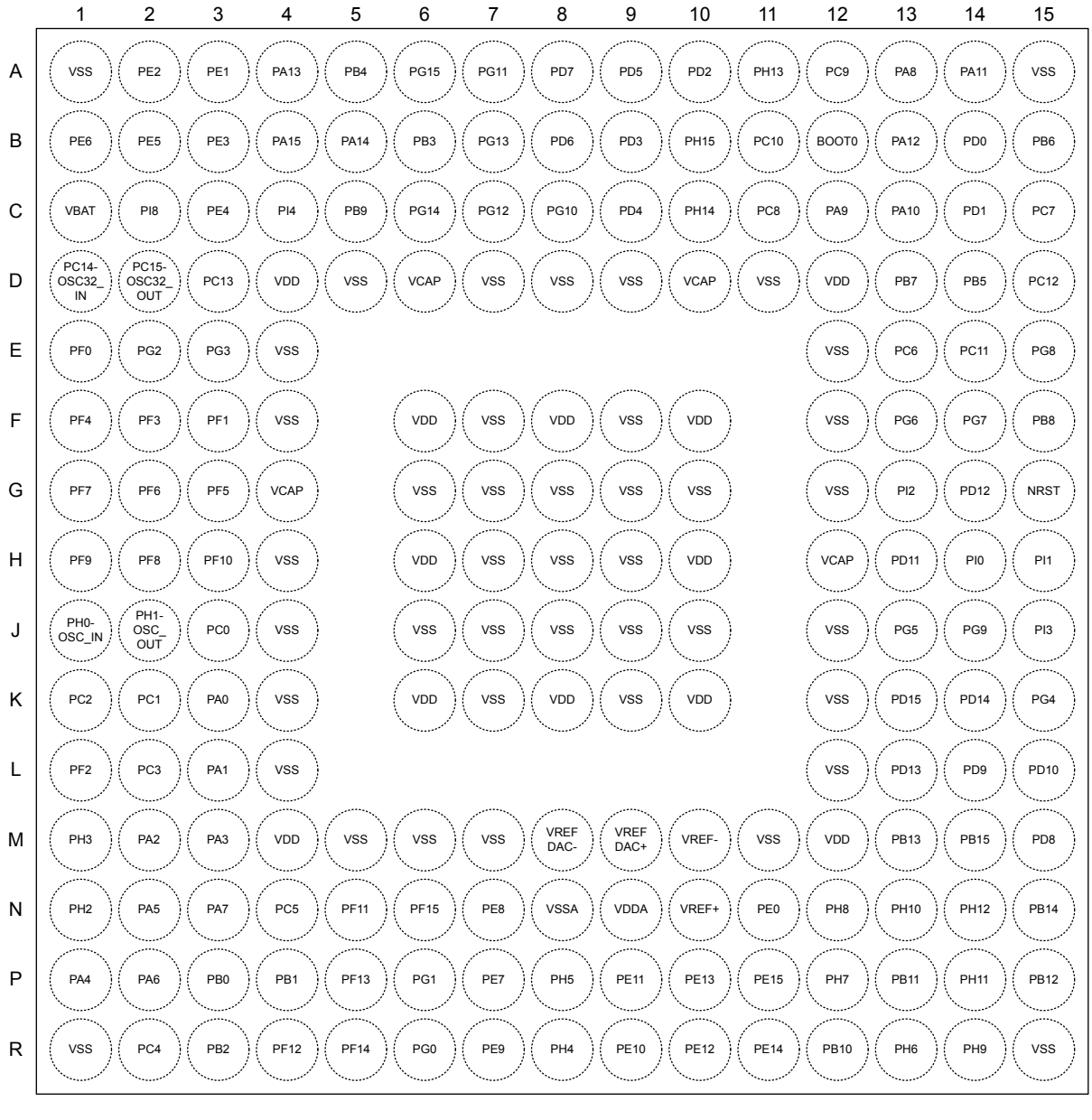
Figure 17. STM32H7Pxxx LQFP176 SMPS EP pinout



1. *The above figure shows the package top view.*

Prerelease product(s)

Figure 18. **STM32H7Pxxx UFBGA176+25 ballout**

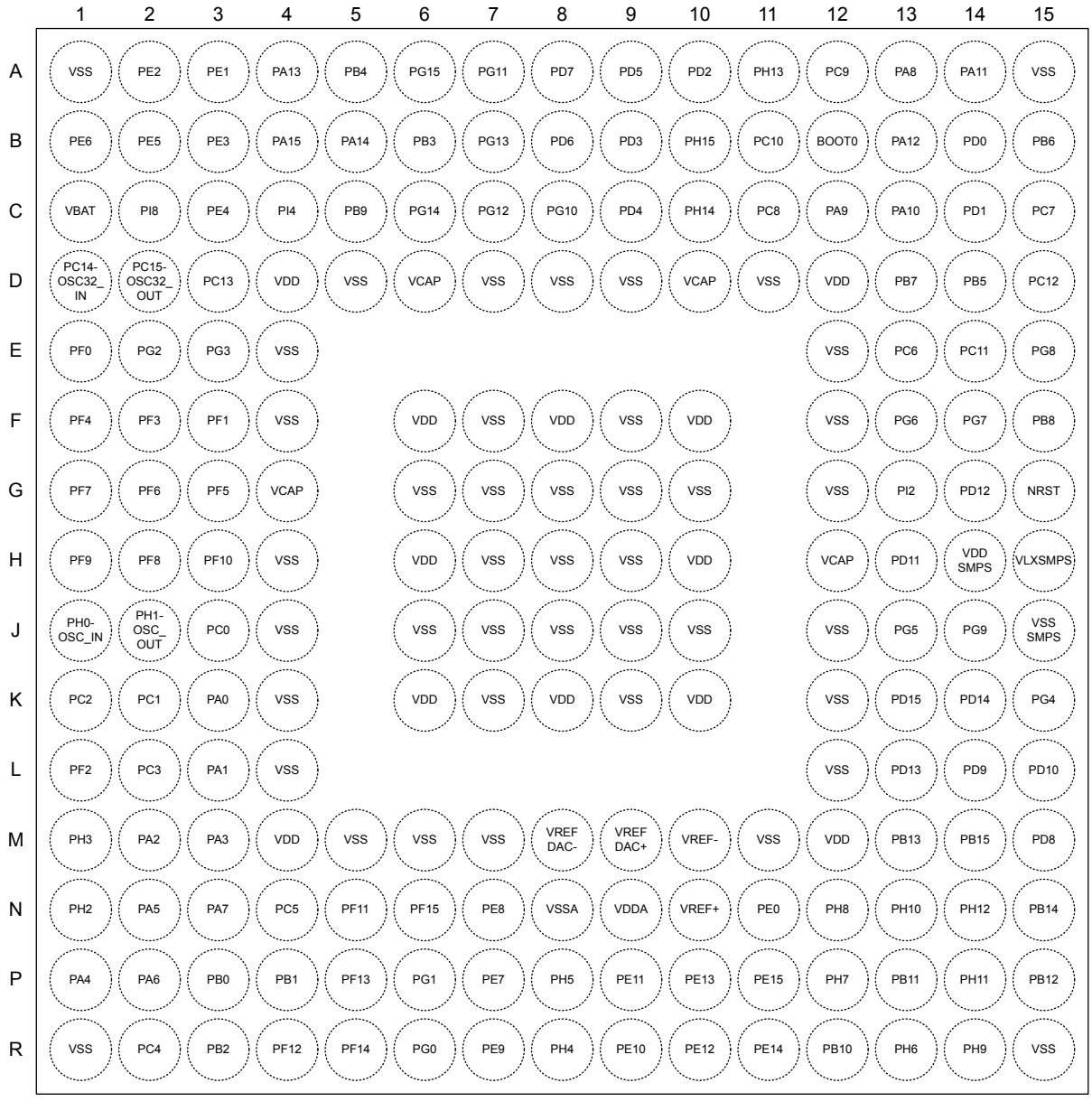


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1. *The above figure shows the package top view.*

Prerelease product(s)

Figure 19. **STM32H7Pxxx UFBGA176+25 SMPS ballout**



DT76675V1

1. *The above figure shows the package top view.*

Prerelease product(s)

4.2 Pin/ball description

Table 7. Legend/abbreviations used in the pinout/ballout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin/ball name.	
Pin type		I	Input-only pin
		I/O	Input/output pin
		O	Output-only pin
		S	Supply pin
I/O structure		FT	5 V-tolerent I/O
		TT	3.6 V-tolerant I/O
		TTa	3.6 V-tolerant I/O with internal clamping to V_{DDA}
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
		Options for TT and FT I/Os(1)	
		_a	I/O with analog switch function supplied by V_{DDA}
		_b	I/O with SMBUS 3.3 capability
		_c	USB Type-C power delivery capable I/O
		_d	USB Type-C power delivery dead battery function I/O
		_f	I2C Fm+ capable I/O
		_h	High-speed low-voltage I/O
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset.	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. *The related I/O structures in the table below are a concatenation of various options. Examples: FT_at, FT_f, FT_c, TT_a.*

Note: Alternate functions listed in following tables may be absent in some devices or packages (see Section 2 for details).

Table 8. **STM32H7Pxxx pin/ball definitions**

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
100	100	100	B1	B1	1	1	1	1	1	1	1	1	A2	A2	PE2	I/O	FT_fh	-	TRACECLK, LPTIM1_IN2, TIM3_CH1, TIM8_CH4N, HSP1_SNP0, I2C2_SCL, USART10_CK, SPI4_SCK, UART8_TX, TIM20_CH1, HRTIM2_FLT5, TIM1_CH3, FMC_A23, LPTIM4_ETR, SDMMC1_CK, EVENTOUT	-
1	1	1	C3	C3	2	2	2	2	2	2	2	2	B3	B3	PE3	I/O	FT_fh	-	TRACED0, HRTIM1_EEV8, TIM3_CH2, HRTIM2_EEV13, HSP1_SNP1, I2C2_SDA, SPI4_NSS, TIM20_CH2, I2C1_SDA, USART6_CTS/ USART6_NSS, TIM1_CH1, FMC_A19, LPTIM4_OUT, SDMMC1_D0, EVENTOUT	TAMP_OUT5
2	2	2	C2	C2	3	3	3	3	3	3	3	3	C3	C3	PE4	I/O	FT_fhb	-	TRACED1, TIM3_CH3, HRTIM2_EEV14, I2C3_SDA(boot), SPI1_NSS/I2S1_WS, USART10_CTS/ USART10_NSS, SPI4_NSS, TIM20_CH1N, I2C1_SMBA, HSP1_SNP2,	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
																			I2C2_SMBA, FMC_A20, SDMMC1_D1, EVENTOUT	
3	3	3	C1	C1	4	4	4	4	4	4	4	4	B2	B2	PE5	I/O	FT_fhb	-	TRACED2, I3C1_SCL, TIM3_CH4, HRTIM2_EEV12, I2C3_SCL(boot), I2C2_SCL, USART10_RTS, SPI4_MISO, TIM20_CH2N, HSP1_SNP3, LPTIM4_IN1, FMC_A21, HRTIM2_FLT7, SDMMC1_D2, EVENTOUT	-
4	4	4	D1	D1	5	5	5	5	5	5	5	5	B1	B1	PE6	I/O	FT_fhb	-	TRACED3, I3C1_SDA, TIM4_CH3, HRTIM2_EEV16, HSP1_SNP4, I2C2_SDA, TIM20_CH3N, SPI4_MOSI, I2C3_SMBA, I2C1_SCL, USART6_RTS, FMC_A22, SDMMC1_D3, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	6	6	6	C2	C2	PI8	I/O	FT_h	(1)	LPTIM2_IN2, UART8_RX, HRTIM2_EEV7, EVENTOUT	WKUP3, TAMP_IN2/ TAMP_OUT1

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
5	5	5	D3	D3	6	6	6	6	6	7	7	7	D3	D3	PC13	I/O	FT	(2)	TIM1_BKIN, LPUART1_TX, TIM8_BKIN, SPI2_NSS/I2S2_WS, TIM17_BKIN, UART4_TX, FDCAN1_RX, HRTIM1_EEV14, HRTIM2_EEV4, EVENTOUT	RTC_OUT1/ RTC_TS, WKUP4, TAMP_IN1/ TAMP_OUT2
6	6	6	D2	D2	7	7	7	7	7	8	8	8	C1	C1	VBAT	S	-	-	-	-
-	-	-	E4	E4	-	-	-	-	-	9	9	9	A15	A15	VSS	S	-	-	-	-
7	7	7	E1	E1	8	8	8	8	8	10	10	10	D1	D1	PC14-OSC32_IN(OSC32_IN)	I/O	FT	(3)	TIM16_BKIN, TIM1_BKIN, LPUART1_RX, LPTIM1_IN1, USART2_RX, UART4_RX, UART5_RX(boot), HRTIM1_FLT7, HRTIM2_EEV2, EVENTOUT	OSC32_IN
8	8	8	E2	E2	9	9	9	9	9	11	11	11	D2	D2	PC15-OSC32_OUT(OSC32_OUT)	I/O	FT	(3)	TIM15_BKIN, LPUART1_TX, TIM8_BKIN, LPTIM1_IN2, USART2_TX, UART4_TX, UART5_TX(boot), HRTIM1_FLT8, HRTIM2_FLT8, EVENTOUT	OSC32_OUT
-	-	-	E5	E5	-	-	-	-	-	12	12	12	D12	D12	VDD	S	-	-	-	-
-	-	-	E6	E6	-	-	-	-	-	-	-	-	D5	D5	VSS	S	-	-	-	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	-	-	-	-	10	13	13	13	E2	E2	PG2	I/O	FT_h	-	HRTIM2_FLT1, UART4_RX, FDCAN1_RX, EVENTOUT	-
-	-	-	-	-	-	-	-	-	11	14	14	14	E3	E3	PG3	I/O	FT_h	-	HRTIM2_EEV9, UART4_TX, LPTIM1_CH1, FDCAN1_TX, EVENTOUT	-
-	-	-	-	-	10	10	10	10	12	15	15	15	E1	E1	PF0	I/O	FT_h	-	HRTIM1_SCIN, HRTIM2_EEV9, SPI2_MISO/I2S2_SDI, USART1_TX, HRTIM1_EEV4, FMC_A4, EVENTOUT	-
-	-	-	-	-	-	-	11	11	13	16	16	16	F3	F3	PF1	I/O	FT_h	-	TIM16_CH1, HRTIM2_FLT3, SPI5_RDY, USART1_RX, HRTIM1_EEV8, FMC_SDNWE, EVENTOUT	-
-	-	-	-	-	11	11	12	12	14	17	17	17	F2	F2	PF3	I/O	FT_h	-	HRTIM1_EEV1, HRTIM2_FLT2, SPI2_SCK/I2S2_CK, SPI3_NSS/I2S3_WS, USART2_TX, TIM20_CH4, FMC_A3, EVENTOUT	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
9	9	9	E3	E3	12	12	13	13	15	18	18	18	F1	F1	PF4	I/O	FT_h	-	HRTIM1_EEV2, HRTIM2_FLT4, HSP1_SNP5, SPI2_MOSI/ I2S2_SDO, USART2_RX, TIM20_CH1N, LPTIM3_CH2, FMC_D11/FMC_AD11, COMP1_OUT, TIM10_CH1, EVENTOUT	-
10	10	10	F4	F4	13	13	14	14	16	19	19	19	G4	G4	VCAP	S	-	-	-	-
11	11	-	F7	F7	14	14	15	15	-	20	20	20	D7	D7	VSS	S	-	-	-	-
-	-	-	F5	-	-	-	-	-	-	-	-	-	F6	-	VDD	S	-	-	-	-
12	12	11	G4	F5	15	15	16	16	17	21	21	21	F10	F6	VDD	S	-	-	-	-
-	-	-	-	-	-	-	17	17	18	22	22	22	G3	G3	PF5	I/O	FT_h	-	HRTIM2_EEV9, SPI5_RDY, TIM20_CH2N, FMC_NCAS, HRTIM2_SCOUT, EVENTOUT	-
-	-	-	-	-	-	-	18	18	19	23	23	23	G2	G2	PF6	I/O	FT_h	-	TIM5_ETR, HRTIM2_EEV2, TIM5_CH1, SPI5_NSS, USART3_RTS, TIM4_CH4, UART7_RX, EVENTOUT	-

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	12	-	-	16	16	19	19	20	24	24	24	G1	G1	PF7	I/O	FT_ha	-	TRACED3, HRTIM2_EEV8, TIM4_CH3, TIM5_CH2, SPI5_SCK, SPI3_SCK/I2S3_CK, UART7_TX, TIM20_BKIN, FMC_A10, EVENTOUT	COMP3_INP3
-	-	-	-	-	17	17	20	20	21	25	25	25	H2	H2	PF8	I/O	FT_ha	-	TRACECLK, HRTIM2_EEV6, TIM4_CH2, TIM5_CH3, SPI5_MISO, SPI3_MISO/I2S3_SDI, UART7_RTS, TIM20_BKIN2, EVENTOUT	COMP1_INP3
13	13	13	F3	F3	18	18	21	21	22	26	26	26	H1	H1	PF9	I/O	FT_ha	-	HRTIM2_EEV4, TIM4_CH1, TIM15_CH1, TIM5_CH4, SPI5_MOSI, USART6_RX, SPI2_SCK/I2S2_CK, UART4_RX, TIM20_BKIN, LPTIM3_IN1, FMC_D9/FMC_AD9, HRTIM2_SCIN, SDMMC1_CMD, EVENTOUT	COMP2_INP3

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
14	14	14	G1	G1	19	19	22	22	23	27	27	27	H3	H3	PF10	I/O	FT_h	-	HRTIM1_SCOUT, HRTIM2_EEV3, TIM15_CH2, SPI2_NSS/I2S2_WS, USART6_TX, UART7_CTS, TIM20_BKIN2, USART10_TX, LPTIM3_IN2, FMC_D10/FMC_AD10, EVENTOUT	-
15	15	15	F1	F1	20	20	23	23	24	28	28	28	J1	J1	PH0-OSC_IN(PH0)	I/O	FT_ha	-	HRTIM1_EEV7, TIM1_CH3N, TIM8_CH3, TIM5_CH1, SPI2_SCK/I2S2_CK, USART1_TX, XSPI1_DQS0, HRTIM2_FLT1, TIM13_CH1, EVENTOUT	ADC1_INP10, ADC1_INN9, OSC_IN
16	16	16	F2	F2	21	21	24	24	25	29	29	29	J2	J2	PH1-OSC_OUT(PH1)	I/O	FT_ha	-	HRTIM1_EEV11, TIM1_ETR, TIM8_CH4, SPI2_SCK/I2S2_CK, USART1_RX, XSPI1_NCS2, HRTIM1_FLT1, TIM10_CH1, EVENTOUT	ADC2_INP10, ADC2_INN9, OSC_OUT
17	17	17	G2	G2	22	22	25	25	26	30	30	30	J3	J3	PC0	I/O	FT_ha	-	AUDIOCLK, HRTIM1_EEV8, HRTIM2_EEV8, XSPI1_IO1, TIM11_CH1, LPTIM1_CH1, TIM1_CH1, SPI2_RDY, LPUART1_RX, USART6_CK, USART10_CTS/	ADC1_INP6, ADC1_INN5, ADC2_INP6, ADC2_INN5, COMP3_INM2, WKUP7

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
																			USART10_NSS, SDMMC1_D4, COMP7_OUT, ADF1_CCK0, EVENTOUT	
-	-	-	G6	G6	-	-	26	26	-	31	31	31	D9	D9	VSS	S	-	-	-	-
-	-	-	G7	F6	-	-	27	27	27	32	32	32	H6	F8	VDD	S	-	-	-	-
18	18	18	G3	G3	23	23	28	28	28	33	33	33	K2	K2	PC1	I/O	FT_ha	-	TRACED0, HRTIM1_EEV5, HRTIM2_EEV5, XSPI1_IO2, TIM14_CH1, SPI2_MOSI/ I2S2_SDO, USART10_RX, USART1_RTS, LPUART1_TX, TIM1_CH2, LPTIM3_CH1, SDMMC1_D5, HSP1_SNP0, ADF1_CCK1, EVENTOUT	ADC1_INP7, ADC1_INN6, ADC2_INP7, ADC2_INN6, COMP3_INP2, WKUP6
19	19	19	H1	H1	24	24	29	29	29	34	34	34	K1	K1	PC2	I/O	FT_ha	-	PWR_CSTOP, TIM1_CH3, TIM2_ETR, SPI2_MOSI/ I2S2_SDO, UART9_CTS, TIM20_CH2, HRTIM2_FLT7, SDMMC1_D6, FMC_NWAIT, ADF1_SDI0, COMP3_OUT, EVENTOUT	ADC1_INP8, ADC1_INN7, ADC2_INP8, ADC2_INN7

Pin number																	
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
20	20	20	J1	J1	25	25	30	30	30	35	35	35	L2	L2	PC3	I/O	FT_ha	-	PWR_CSLEEP, HRTIM1_EEV9, TIM1_CH4, XSPI1_IO0, HSP1_SNP1, SPI2_MISO/I2S2_SDI, SPI3_NSS/I2S3_WS, UART9_RTS, TIM20_CH2N, USART10_TX, LPTIM3_CH2, SDMMC1_D7, HRTIM2_EEV9, COMP8_OUT, EVENTOUT	ADC1_INP9, ADC1_INN8, ADC2_INP9, ADC2_INN8
21	21	21	K1	K1	26	26	31	31	31	36	36	36	L1	L1	PF2	I/O	FT_ha	-	TIM16_CH1N, HRTIM2_FLT5, XSPI1_NCLK, TIM17_CH1, SPI3_MOSI/ I2S3_SDO, TIM20_CH3, USART10_RX, TIM2_CH4, LPTIM3_CH1, FMC_D14/FMC_AD14, EVENTOUT	ADC1_INP5, ADC1_INN4
22	22	22	H2	H2	27	27	32	32	32	37	37	37	K3	K3	PA0	I/O	FT_ha	-	TRACECLK, TIM2_CH1, TIM5_CH1, XSPI1_CLK, TIM11_CH1, SPI6_NSS, SPI3_RDY, USART2_CTS/ USART2_NSS, UART4_TX(boot), HSP1_SNP2, LPTIM3_IN1, FMC_D15/FMC_AD15, COMP1_OUT,	ADC1_INP1, ADC1_INN0, ADC2_INP1, ADC2_INN0, COMP1_INM2, COMP3_INP1, WKUP1, TAMP_IN3

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
																			TIM8_BKIN, EVENTOUT	
23	23	23	J2	J2	28	28	33	33	33	38	38	38	L3	L3	PA1	I/O	FT_ha	-	RTC_REFIN, TIM2_CH2, TIM5_CH2, XSPI1_IO3, LPTIM1_IN1, USART2_RTS, UART4_RX(boot), TIM15_CH1N, USART10_CK, FMC_A5, HRTIM2_EEV10, TIM10_CH1, EVENTOUT	ADC1_INP2, ADC1_INN1, ADC2_INP2, ADC2_INN1, COMP1_INP1, TAMP_IN4
24	24	24	H3	H3	29	29	34	34	34	39	39	39	M2	M2	PA2	I/O	FT_ha	-	TIM2_CH3, TIM5_CH3, LPUART1_TX, LPTIM1_IN2, SPI6_MOSI, USART2_TX(boot), UART4_CTS, TIM15_CH1, XSPI1_NCS1, HRTIM1_EEV3, FMC_NE3, COMP2_OUT, EVENTOUT	ADC1_INP3, ADC1_INN2, COMP2_INM2, COMP3_INM1, WKUP2, TAMP_OUT3
-	-	-	-	-	-	-	-	-	-	40	40	40	N1	N1	PH2	I/O	FT_f	-	LPTIM1_IN2, HRTIM2_SCOUT, I2C1_SCL, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	41	41	41	M1	M1	PH3	I/O	FT_f	-	HRTIM2_FLT8, I2C1_SDA, EVENTOUT	-
25	25	25	-	G4	30	30	35	35	35	42	42	42	H10	F10	VDD	S	-	-	-	-
26	26	-	-	-	31	31	36	36	-	43	43	43	D11	D11	VSS	S	-	-	-	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
27	27	26	K2	K2	32	32	37	37	36	44	44	44	M3	M3	PA3	I/O	FT_ha	-	TIM2_CH4, TIM5_CH4, LPUART1_RX, USART2_RX(boot), TIM15_CH2, XSPI1_DQS0, FMC_NL, HRTIM2_EEV7, EVENTOUT	ADC1_INP4, ADC1_INN3, COMP2_INP2
28	28	27	K3	K3	33	33	38	38	37	45	45	45	P1	P1	PA4	I/O	TT_ha	-	HRTIM2_EEV5, TIM3_CH4, HRTIM2_FLT3, SPI1_NSS/I2S1_WS, LPTIM2_CH1, USART2_CK, SPI6_NSS, XSPI1_NCS2, SDMMC1_CKIN, FDCAN2_RX, EVENTOUT	ADC2_INP17, ADC2_INN16, DAC1_OUT1, COMP1_INM1
29	29	28	J3	J3	34	34	39	39	38	46	46	46	N2	N2	PA5	I/O	TT_ha	-	HRTIM2_EEV10, TIM2_CH1, USART6_CTS/ USART6_NSS, TIM8_CH4, SDMMC1_CMD, ADF1_CCK0, SPI6_SCK, LPTIM1_CH2, XSPI1_NCS1, TIM9_CH1, FDCAN2_TX, UART5_RX, EVENTOUT	ADC2_INP13, ADC2_INN12, DAC1_OUT2, COMP2_INM1

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
30	30	29	K4	K4	35	35	40	40	39	47	47	47	P2	P2	PA6	I/O	FT_ha	-	TIM16_CH1, TIM3_CH1, USART6_RTS, TIM8_BKIN, SDMMC1_D0, TIM1_BKIN, ADF1_CCK1, SPI6_MISO, FDCAN1_RX(boot), TIM8_CH2, LPTIM3_IN2, HRTIM2_EEV11, COMP1_OUT, UART5_TX, EVENTOUT	ADC2_INP3, ADC2_INN2
31	31	30	J4	J4	36	36	41	41	40	48	48	48	N3	N3	PA7	I/O	FT_ha	-	TIM17_CH1, TIM3_CH2, SDMMC1_D1, TIM8_CH1N, SPI1_RDY, TIM1_CH1N, USART1_CK, ADF1_SDI0, FDCAN1_TX(boot), LPTIM3_ETR, HRTIM1_EEV10, FMC_NWE, HRTIM2_EEV4, COMP2_OUT, EVENTOUT	ADC2_INP4, ADC2_INN3, COMP2_INP1
32	32	31	K5	K5	37	37	42	42	41	49	49	49	R2	R2	PC4	I/O	FT_ha	-	HRTIM1_FLT1, TIM1_ETR, LPTIM2_ETR, USART1_TX, I2S1_MCK, TIM8_CH2, LPTIM1_CH1, FMC_D13/FMC_AD13, HRTIM2_EEV1, EVENTOUT	ADC2_INP5, ADC2_INN4

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
33	33	32	H4	H4	38	38	43	43	42	50	50	50	N4	N4	PC5	I/O	FT_ha	-	HRTIM1_EEV10, TIM15_BKIN, USART1_RX, LPTIM1_IN2, TIM1_CH4N, SPI3_NSS/I2S3_WS, TIM1_BKIN2, FMC_D12/FMC_AD12, HRTIM2_FLT1, TIM12_CH2, EVENTOUT	ADC2_INP11, ADC2_INN10
34	34	33	J5	J5	39	39	44	44	43	51	51	51	P3	P3	PB0	I/O	FT_ha	-	TIM16_BKIN, TIM1_CH4, LPTIM2_IN2, TIM8_CH2N, SPI1_SCK/I2S1_CK, TIM1_CH2N, TIM17_CH1N, SPI6_SCK, SPI3_SCK/I2S3_CK, USART6_TX, HRTIM1_FLT5, FMC_INT, SDMMC1_D2, COMP5_OUT, EVENTOUT	ADC1_INP15, ADC1_INN14, ADC3_INP12, ADC3_INN11, COMP4_INP1
35	35	34	H5	H5	40	40	45	45	44	52	52	52	P4	P4	PB1	I/O	FT_ha	-	HRTIM1_SCOUT, TIM3_CH3, LPTIM2_CH2, TIM8_CH3N, SPI1_MISO/I2S1_SDI, TIM1_CH3N, USART2_RX, SPI6_MISO, SPI3_MISO/I2S3_SDI, SDMMC1_D3, HRTIM1_EEV6, XSPI1_CLK, COMP4_OUT,	ADC1_INP12, ADC1_INN11, ADC3_INP1, ADC3_INN0, COMP1_INP2

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
																			TIM20_CH1N, EVENTOUT	
36	36	35	H6	H6	41	41	46	46	45	53	53	53	R3	R3	PB2	I/O	FT_ha	-	RTC_OUT2, SDMMC1_CK, TIM3_CH4, HRTIM1_FLT6, TIM5_CH1, SPI1_MOSI/ I2S1_SDO, TIM20_CH1, SPI6_MOSI, LPTIM1_CH1, USART6_RX, HRTIM1_SCIN, XSPI1_NCLK, HRTIM2_FLT2, COMP8_OUT, EVENTOUT	ADC2_INP12, ADC2_INN11, PVD_IN
37	37	-	-	-	42	42	47	47	-	54	54	54	E4	E4	VSS	S	-	-	-	-
38	38	36	-	G7	43	43	48	48	46	55	55	55	K6	H6	VDD	S	-	-	-	-
-	-	-	-	-	44	44	49	49	47	56	56	56	N5	N5	PF11	I/O	FT_ha	-	HRTIM2_EEV10, TIM20_ETR, HRTIM1_EEV12, FMC_A1, EVENTOUT	COMP5_INP3
-	-	-	-	-	45	45	50	50	48	57	57	57	R4	R4	PF12	I/O	FT_ha	-	LPTIM1_ETR, HRTIM2_FLT5, TIM1_CH4N, TIM20_CH1, HRTIM1_EEV13, FMC_A6, EVENTOUT	ADC2_INP16, ADC2_INN15, ADC3_INP8, ADC3_INN7, COMP6_INP3
-	-	-	-	-	46	46	51	51	49	58	58	58	P5	P5	PF13	I/O	FT_ha	-	LPTIM1_CH2, HRTIM2_SCOUT, TIM20_CH2, HRTIM1_EEV15, FMC_A7, HRTIM2_EEV1, EVENTOUT	ADC2_INP0, ADC3_INP9, ADC3_INN8

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	47	47	52	52	50	59	59	59	R5	R5	PF14	I/O	FT_ha	-	HRTIM2_SCIN, LPTIM2_CH1, TIM5_CH1, UART9_RTS, TIM20_CH3N, HRTIM1_EEV14, FMC_A8, EVENTOUT	COMP7_INP3
-	-	37	-	-	48	48	53	53	51	60	60	60	N6	N6	PF15	I/O	FT_ha	-	HRTIM2_EEV9, LPTIM2_CH2, TIM5_CH2, UART9_CTS, TIM20_CH4, HRTIM1_EEV16, FMC_A9, HRTIM2_SCOUT, EVENTOUT	ADC1_INP0
-	-	-	-	-	-	-	-	-	-	-	-	-	K8	H10	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	E12	E12	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	52	61	61	61	R6	R6	PG0	I/O	FT_h	-	HRTIM2_EEV3, LPTIM2_IN1, FDCAN3_RX, TIM20_CH1N, EVENTOUT	-
-	-	-	-	-	-	-	-	-	53	62	62	62	P6	P6	PG1	I/O	FT_h	-	LPTIM2_IN2, SPI2_MOSI/ I2S2_SDO, FDCAN3_TX, TIM20_CH2N, HRTIM1_FLT5, HRTIM2_FLT1, EVENTOUT	-
-	-	38	-	-	49	49	54	54	54	63	63	63	P7	P7	PE7	I/O	FT_ha	-	TIM1_ETR, UART7_RX, HRTIM2_FLT7, HRTIM1_EEV4, FMC_SDCKE0, EVENTOUT	ADC3_INP13, ADC3_INN12, COMP4_INP2

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	50	50	55	55	55	64	64	64	N7	N7	PE8	I/O	FT_ha	-	TIM5_CH3, TIM1_CH1N, TIM20_CH4N, UART7_TX, FDCAN1_RX, HRTIM2_FLT8, HRTIM1_EEV10, FMC_SDNE0, EVENTOUT	ADC4_INP6, ADC4_INN5, COMP4_INM1
-	-	-	-	-	51	51	56	56	56	65	65	65	R7	R7	PE9	I/O	FT_ha	-	TIM5_ETR, TIM1_CH1, UART7_RTS, FDCAN1_TX, HRTIM1_FLT3, FMC_A2, EVENTOUT	ADC4_INP17, ADC4_INN16
-	-	-	J6	J6	52	52	57	57	57	66	66	66	M8	M8	VREFDAC-	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	N8	N8	VSSA	S	-	-	-	-
39	39	39	-	-	53	53	58	58	58	67	67	67	-	-	VSSA	S	-	-	-	-
40	40	40	K6	K6	54	54	59	59	59	68	68	68	N9	N9	VDDA	S	-	-	-	-
-	-	-	-	-	55	55	60	60	60	69	69	69	M9	M9	VREFDAC+	S	-	-	-	-
-	-	-	-	-	-	-	61	61	61	70	70	70	R8	R8	PH4	I/O	FT_h	-	HRTIM2_FLT6, SPI6_RDY, FMC_A14/ FMC_BA0, EVENTOUT	-
41	41	41	K7	K7	56	56	62	62	62	71	71	71	N10	N10	VREF+	S	-	-	-	-
42	42	42	J7	J7	57	57	63	63	63	72	72	72	M10	M10	VREF-	S	-	-	-	-
-	-	-	-	-	-	-	64	64	-	73	73	73	F4	F4	VSS	S	-	-	-	-
-	-	-	-	-	58	58	65	65	64	74	74	74	K10	K6	VDD	S	-	-	-	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	-	-	66	66	65	75	75	75	P8	P8	PH5	I/O	FT_ha	-	HRTIM1_SCOUT, TIM17_CH1, TIM20_CH2N, SPI6_RDY, FMC_A15/ FMC_BA1, EVENTOUT	COMP8_INP3
-	-	-	-	-	59	59	67	67	66	76	76	76	R9	R9	PE10	I/O	FT_ha	-	HRTIM2_FLT3, TIM1_CH2N, UART7_CTS, HRTIM1_FLT7, FMC_NRAS, EVENTOUT	ADC3_INP14, ADC3_INN13, ADC4_INP14, ADC4_INN13, COMP8_INM2
-	-	-	-	-	60	60	68	68	67	77	77	77	P9	P9	PE11	I/O	FT_ha	-	HRTIM2_FLT4, TIM1_CH2, HRTIM1_FLT8, FDCAN2_TX, EVENTOUT	ADC4_INP15, ADC4_INN14
43	43	43	K8	K8	61	61	69	69	68	78	78	78	R10	R10	PE12	I/O	FT_ha	-	HRTIM2_FLT5, TIM1_CH3N, USART6_CK, LPTIM3_ETR, FMC_D8/FMC_AD8, FDCAN2_RX, EVENTOUT	ADC3_INP16, ADC3_INN15, ADC4_INP16, ADC4_INN15, COMP8_INM1
44	44	44	H7	H7	62	62	70	70	69	79	79	79	P10	P10	PE13	I/O	FT_ha	-	HRTIM2_FLT6, TIM1_CH3, USART6_RX, SPI4_MISO, TIM20_BKIN2, UART5_RTS, HRTIM1_FLT6, FMC_D0/FMC_AD0, EVENTOUT	ADC3_INP3, ADC3_INN2, COMP4_INP3

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
45	45	45	K9	K9	63	63	71	71	70	80	80	80	R11	R11	PE14	I/O	FT_ha	-	HRTIM2_EEV3, TIM1_CH4, USART6_TX, TIM1_BKIN2, SPI4_MOSI, UART5_CTS, HRTIM1_EEV3, FMC_D1/FMC_AD1, EVENTOUT	ADC3_INP4, ADC3_INN3, ADC4_INP1, ADC4_INN0, COMP5_INP2
46	46	46	J8	J8	64	64	72	72	71	81	81	81	P11	P11	PE15	I/O	FT_ha	-	HRTIM2_EEV2, TIM1_BKIN, TIM1_CH4N, USART3_RX, SPI4_SCK, HRTIM1_FLT2, FMC_D2/FMC_AD2, EVENTOUT	ADC3_INP2, ADC3_INN1, ADC4_INP2, ADC4_INN1, COMP6_INP2, COMP8_INP1
47	47	47	K10	K10	65	65	73	73	72	82	82	82	R12	R12	PB10	I/O	FT_ha	-	HRTIM1_FLT3, TIM2_CH3, HSP1_SNP3, LPTIM2_IN1, USART3_TX, LPUART1_RX, TIM1_BKIN, FMC_CLK, HRTIM2_EEV9, CRS_SYNC, EVENTOUT	ADC3_INP0, ADC4_INP9, ADC4_INN8, COMP5_INM1
-	-	-	-	-	-	-	-	-	73	83	83	83	N11	N11	PE0	I/O	FT_h	-	TIM16_CH1, LPTIM2_CH2, USART1_TX, LPTIM2_ETR, SPI3_RDY, TIM20_CH4N, TIM20_ETR, HRTIM1_FLT2, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	84	84	84	M4	K8	VDD	S	-	-	-	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	-	-	-	-	-	85	85	85	F7	F7	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	86	86	86	R13	R13	PH6	I/O	FT_h	-	HRTIM1_EEV2, I2C2_SMBA, SPI5_SCK, USART1_RX, LPTIM1_ETR, HRTIM2_FLT2, FDCAN2_RX, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	87	87	87	P12	P12	PH7	I/O	FT_fh	-	HRTIM1_EEV7, I2C3_SCL, SPI5_MISO, HRTIM2_FLT3, FDCAN2_TX, EVENTOUT	-
48	48	48	J9	J9	66	66	74	74	74	88	88	88	P13	P13	PB11	I/O	FT_ha	-	HRTIM1_FLT4, TIM1_CH3N, LPTIM2_ETR, HSP1_SNP4, SPI2_RDY, USART3_RX, LPUART1_TX, SPI4_NSS, TIM2_CH4, TIM9_CH1, FMC_NBL1, HRTIM2_EEV8, EVENTOUT	ADC1_INP14, ADC1_INN13, ADC2_INP14, ADC2_INN13, COMP6_INP1
-	-	-	-	-	-	-	-	-	-	89	89	89	N12	N12	PH8	I/O	FT_fh	-	I2C3_SDA, SPI5_MOSI, HRTIM1_FLT6, TIM10_CH1, EVENTOUT	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	-	-	-	-	-	90	90	90	R14	R14	PH9	I/O	FT_h	-	TIM11_CH1, SPI5_NSS, FDCAN3_RX, I2C3_SMBA, HRTIM1_EEV4, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	91	91	91	N13	N13	PH10	I/O	FT_h	-	SPI5_RDY, FDCAN3_TX, HSP1_SNP0, HRTIM1_EEV6, HRTIM2_FLT5, TIM12_CH1, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	92	92	92	P14	P14	PH11	I/O	FT_fh	-	HRTIM2_EEV11, I3C1_SCL, I2C2_SCL, HSP1_SNP1, TIM13_CH1, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	93	93	93	N14	N14	PH12	I/O	FT_fh	-	HRTIM2_EEV15, I3C1_SDA, I2C2_SDA, HSP1_SNP2, TIM9_CH1, EVENTOUT	-
49	49	49	-	-	67	67	75	75	75	94	94	94	M12	K10	VDD	S	-	-	-	-
50	50	-	-	-	68	68	76	76	-	95	95	95	F9	F9	VSS	S	-	-	-	-
51	51	50	H8	H8	69	69	77	77	76	96	96	96	P15	P15	PB12	I/O	FT_ha	-	HRTIM1_FLT2, TIM5_CH4, TIM8_BKIN2, TIM14_CH1, SPI2_NSS/I2S2_WS, USART3_CK, LPUART1_RTS, TIM1_BKIN, UCPD1_FRSTX1, TIM9_CH2, FMC_D3/ FMC_AD3, FDCAN1_RX,	ADC1_INP11, ADC1_INN10, ADC4_INP3, ADC4_INN2, COMP7_INM2, COMP8_INP2

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
																			UART5_RX, EVENTOUT	
52	52	51	H9	H9	70	70	78	78	77	97	97	97	M13	M13	PB13	I/O	FT_ha	-	HRTIM1_FLT6, TIM1_CH1, LPTIM2_CH1, TIM14_CH1, SPI2_SCK/I2S2_CK, USART3_CTS/ USART3_NSS, LPUART1_CTS, LPTIM1_ETR, TIM8_CH4, HRTIM2_FLT7, FMC_D4/FMC_AD4, FDCAN1_TX, UART5_TX, EVENTOUT	ADC3_INP5, ADC3_INN4, ADC4_INP8, ADC4_INN7, COMP5_INP1
53	53	52	J10	J10	71	71	79	79	78	98	98	98	N15	N15	PB14	I/O	FT_ha	-	MCO2, TIM15_CH1, TIM1_CH2, HRTIM2_EEV6, USART1_TX, SPI2_MISO/I2S2_SDI, USART3_RTS, UART4_RTS, LPTIM1_CH2, TIM8_CH4N, HRTIM1_EEV1, FMC_NOE, COMP4_OUT, EVENTOUT	ADC1_INP13, ADC1_INN12, ADC4_INP4, ADC4_INN3, COMP7_INP1
54	54	53	G8	G8	72	72	80	80	79	99	99	99	M14	M14	PB15	I/O	FT_ha	-	MCO2, TIM15_CH2, TIM15_CH1N, USART1_RX, SPI2_MOSI/ I2S2_SDO, TIM1_CH3, UART9_TX, UART4_CTS, UART5_RX, HSP1_SNP5,	ADC2_INP15, ADC2_INN14, ADC4_INP5, ADC4_INN4, COMP4_INM2, COMP6_INM2

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
																			HRTIM1_EEV2, FMC_NWE, HRTIM2_FLT4, COMP3_OUT, EVENTOUT	
55	55	54	H10	H10	73	73	81	81	80	100	100	100	M15	M15	PD8	I/O	FT_ha	-	HRTIM1_EEV4, TIM4_ETR, HRTIM2_FLT1, SPI5_SCK, USART3_TX, TIM20_ETR, FMC_D5/FMC_AD5, CRS_SYNC, EVENTOUT	ADC3_INP6, ADC3_INN5, ADC4_INP12, ADC4_INN11
56	56	55	F9	F9	74	74	82	82	81	101	101	101	L14	L14	PD9	I/O	FT_ha	-	HRTIM1_EEV6, HRTIM2_EEV1, SPI5_MISO, USART3_RX, TIM20_CH3N, TIM9_CH2, FMC_D6/FMC_AD6, EVENTOUT	ADC3_INP15, ADC3_INN14, ADC4_INP13, ADC4_INN12
57	57	56	F8	F8	75	75	83	83	82	102	102	102	L15	L15	PD10	I/O	FT_ha	-	HRTIM1_SCOUT, HRTIM2_EEV5, LPTIM2_CH2, SPI5_MOSI, USART3_CK, TIM20_CH3, HRTIM1_EEV9, FMC_D7/FMC_AD7, EVENTOUT	ADC3_INP7, ADC3_INN6, ADC4_INP7, ADC4_INN6, COMP6_INM1

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
58	-	-	F10	-	76	76	84	84	83	103	103	103	L13	L13	PD13	I/O	FT_ha	-	LPTIM1_CH1, TIM4_CH2, LPTIM2_CH1, SPI5_NSS, SPI4_RDY, SPI3_RDY, XSPI1_IO6, HRTIM1_FLT1, HRTIM2_FLT1, EVENTOUT	ADC3_INP10, ADC3_INN9, ADC4_INP10, ADC4_INN9, COMP5_INM2
-	-	-	-	-	-	-	-	-	-	104	104	104	-	M4	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	105	105	105	F12	F12	VSS	S	-	-	-	-
59	-	-	G10	-	77	77	85	85	84	106	106	106	K14	K14	PD14	I/O	FT_ha	-	HRTIM1_EEV11, TIM4_CH3, XSPI1_IO5, UART8_CTS, FMC_SDCKE1, HRTIM2_EEV6, EVENTOUT	ADC3_INP11, ADC3_INN10, ADC4_INP11, ADC4_INN10, COMP7_INP2
60	-	-	G9	-	78	78	86	86	85	107	107	107	K13	K13	PD15	I/O	FT_ha	-	TIM1_CH1, TIM4_CH4, XSPI1_IO4, TIM16_BKIN, SPI2_NSS/I2S2_WS, UART8_RTS, TIM1_BKIN, HRTIM1_FLT4, FMC_SDNE1, HRTIM2_EEV7, EVENTOUT	ADC4_INP0, COMP7_INM1
-	-	-	-	-	79	-	87	-	86	108	108	108	K15	K15	PG4	I/O	FT_h	-	HRTIM1_EEV2, SPI1_MISO/I2S1_SDI, TIM5_CH1, SPI5_NSS, TIM20_BKIN2, HRTIM2_FLT5, EVENTOUT	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	80	-	88	-	-	109	109	109	J13	J13	PG5	I/O	FT_h	-	HRTIM1_EEV7, SPI1_MOSI/ I2S1_SDO, TIM5_CH3, SPI5_RDY, LPUART1_CTS, TIM20_ETR, HRTIM2_FLT6, EVENTOUT	-
-	-	-	-	-	81	-	89	-	87	110	110	110	J14	J14	PG9	I/O	FT_h	-	HRTIM1_FLT1, SPI1_SCK/I2S1_CK, TIM5_CH4, SPI3_SCK/I2S3_CK, UART9_RX, HRTIM2_FLT7, TIM15_CH1N, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	111	-	-	H14	-	PI0	I/O	FT_h	-	SPI2_NSS/I2S2_WS, UART8_RX, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	112	-	-	H15	-	PI1	I/O	FT_h	-	SPI2_SCK/I2S2_CK, UART8_TX, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	113	-	-	J15	-	PI3	I/O	FT_h	-	UART8_CTS, FDCAN1_RX, EVENTOUT	-
-	58	57	-	G9	-	79	-	87	88	-	111	111	-	J15	VSSSMPS	S	-	-	-	-
-	59	58	-	G10	-	80	-	88	89	-	112	112	-	H15	VLXSMPS	S	-	-	-	-
-	60	59	-	F10	-	81	-	89	90	-	113	113	-	H14	VDDSMPS	S	-	-	-	-
61	61	60	E7	E7	82	82	90	90	91	114	114	114	H12	H12	VCAP	S	-	-	-	-
62	62	-	-	-	83	83	91	91	-	115	115	115	G8	G6	VSS	S	-	-	-	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	-	-	-	-	-	-	-	-	G10	G8	VSS	S	-	-	-	-
63	63	61	-	-	84	84	92	92	92	116	116	116	-	M12	VDD	S	-	-	-	-
64	64	62	E9	E9	85	85	93	93	93	117	117	117	H13	H13	PD11	I/O	FT_h	-	TIM5_ETR, TIM4_CH2, LPTIM2_IN2, LPTIM5_IN1, SPI5_NSS, TIM8_ETR, USART3_CTS/ USART3_NSS, UART4_RX, USART10_TX, HRTIM1_CHE1, FMC_A16/FMC_CLE, ADF1_CCK0, UART7_RX, EVENTOUT	-
65	65	63	E8	E8	86	86	94	94	94	118	118	118	G14	G14	PD12	I/O	FT_h	-	TIM4_CH3, LPTIM2_IN1, SPI5_RDY, USART3_RTS, UART4_TX, LPTIM1_IN1, USART10_RX, HRTIM1_CHE2, FMC_A17/FMC_ALE, ADF1_CCK1, UART7_TX, EVENTOUT	-
66	66	64	E10	E10	87	87	95	95	95	119	119	119	G15	G15	NRST	I/O	RST	-	-	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
67	67	65	D9	D9	88	88	96	96	96	120	120	120	G13	G13	PI2	I/O	FT_fh	-	TIM15_BKIN, SPI1_MOSI/ I2S1_SDO, SDMMC1_D123DIR, I2C2_SCL, I3C1_SCL(boot), SDMMC1_D7, USART2_TX, UART8_RX, TIM20_CH4, TIM8_BKIN2, USART10_CK, HRTIM1_CHD1, ADF1_SDI0, COMP5_OUT, EVENTOUT	-
68	68	66	D10	D10	89	89	97	97	97	121	121	121	F15	F15	PB8	I/O	FT_fh	(4)	SDMMC1_D5, SPI1_SCK/I2S1_CK, I2C2_SDA, I3C1_SDA(boot), TIM20_CH4N, USART3_RX, UART8_TX, TIM20_BKIN, TIM8_ETR, USART10_CTS/ USART10_NSS, HRTIM1_CHD2, COMP7_OUT, SDMMC1_CDIR, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	122	122	122	F13	F13	PG6	I/O	FT_h	-	HRTIM2_EEV1, SPI1_RDY, I2C3_SMBA, LPUART1_RTS, TIM20_BKIN, UCPD1_FRSTX1, COMP6_OUT, EVENTOUT	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	-	-	-	-	-	-	-	-	G12	G9	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	123	123	123	F14	F14	PG7	I/O	FT_h	-	HRTIM2_EEV5, LPUART1_TX, UCPD1_FRSTX2, COMP8_OUT, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	H4	G10	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	124	124	124	E15	E15	PG8	I/O	FT_h	-	HRTIM2_EEV13, SPI6_NSS, UART9_RTS, LPUART1_RX, EVENTOUT	-
69	69	67	D8	D8	90	90	98	98	98	125	125	125	E14	E14	PC11	I/O	FT_fh	-	TRACED1, HRTIM1_CHC1, TIM4_CH1, LPUART1_CTS, TIM8_CH2N, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, UCPD1_FRSTX2, TIM1_ETR, HRTIM2_EEV4, XSPI1_IO7, TIM12_CH1, EVENTOUT	-
70	70	68	C10	C10	91	91	99	99	99	126	126	126	D15	D15	PC12	I/O	FT_fh	-	TRACED3, HRTIM1_CHC2, TIM5_CH2, LPUART1_RTS, I2C2_SDA, XSPI1_IO6, SPI3_MOSI/ I2S3_SDO, USART3_CK, SPI6_SCK, TIM8_CH3N,	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
																			FMC_A18, HRTIM2_EEV15, TIM13_CH1, EVENTOUT	
-	-	-	-	-	-	-	-	-	-	-	-	-	H7	G12	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	127	127	127	-	-	VDD	S	-	-	-	-
71	71	69	C9	C9	92	92	100	100	100	128	128	128	E13	E13	PC6	I/O	FT_h	-	HRTIM1_EEV10, TIM3_CH1, TIM8_BKIN, TIM8_CH1, SDMMC1_D6, SDMMC1_D0DIR, I2S2_MCK, UART9_TX, XSPI1_IO5, USART10_RTS, HRTIM1_CHF1, HRTIM2_EEV14, LPTIM5_OUT, COMP6_OUT, EVENTOUT	-
72	72	70	A10	A10	93	93	101	101	101	129	129	129	C15	C15	PC7	I/O	FT_fh	-	TRACED2, HRTIM1_FLT5, TIM3_CH2, I2C3_SCL, TIM8_CH3, XSPI1_IO4, USART3_RTS, UART9_RX, I2S3_MCK, HRTIM1_CHF2, HRTIM2_EEV13, COMP5_OUT, EVENTOUT	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
73	73	71	B10	B10	94	94	102	102	102	130	130	130	D14	D14	PB5	I/O	FT_fdh	-	TIM16_CH1, TIM4_CH3, TIM8_CH2N, USART6_CK, I2S2_MCK, USART3_CTS/ USART3_NSS, I2C3_SDA, I2C1_SCL(boot), TIM8_CH1N, LPTIM5_ETR, HRTIM1_CHA1, COMP4_OUT, CRS_SYNC, EVENTOUT	UCPD1_DBCC2
74	74	72	B9	B9	95	95	103	103	103	131	131	131	B15	B15	PB6	I/O	FT_fdh	-	TIM1_BKIN2, TIM4_CH4, I2C1_SDA(boot), TIM8_CH2, USART2_TX, UART4_CTS, SPI3_SCK/I2S3_CK, SDMMC1_D4, HRTIM2_FLT2, HRTIM1_CHA2, COMP7_OUT, TIM12_CH1, EVENTOUT	UCPD1_DBCC1
75	75	73	C8	C8	96	96	104	104	104	132	132	132	D13	D13	PB7	I/O	FT_h	-	HRTIM1_CHB1, TIM2_CH1, TIM8_CH1, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, FDCAN3_TX, TIM1_BKIN, TIM2_ETR, FMC_A24, HRTIM2_FLT3, COMP1_OUT,	OTG_FS_VBUS

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
																			TIM12_CH2, EVENTOUT	
-	-	-	-	-	97	97	105	105	105	133	133	133	B14	B14	PD0	I/O	FT_fh	-	HRTIM1_EEV5, I2C2_SMBA, XSPI1_DQS0, I2C3_SCL, SPI1_MOSI/ I2S1_SDO, UART4_RX, FDCAN1_RX, I3C1_SCL, FMC_A25, TIM8_CH4N, EVENTOUT	-
-	-	-	-	-	98	98	106	106	106	134	134	134	C14	C14	PD1	I/O	FT_fh	-	HRTIM1_EEV8, SPI1_MISO/I2S1_SDI, XSPI1_NCS2, I2C3_SDA, UART4_TX, FDCAN1_TX, TIM8_CH4, I3C1_SDA, TIM8_BKIN2, EVENTOUT	-
76	76	74	A9	A9	99	99	107	107	107	135	135	135	C13	C13	PA10	I/O	FT_h	-	TIM17_BKIN, TIM2_CH1, LPUART1_TX, TIM8_CH1N, FMC_NBL0, TIM1_CH3, USART1_RX, UART4_RX, UCPD1_FRSTX2, TIM8_BKIN, TIM1_CH3N, HRTIM1_CHB2, FDCAN2_TX, COMP6_OUT, EVENTOUT	OTG_FS_ID

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
77	77	75	B8	B8	100	100	108	108	108	136	136	136	A14	A14	PA11	I/O	FT_h	-	TIM1_CH4N, TIM1_BKIN2, SPI2_MISO/I2S2_SDI, TIM1_CH1N, USART1_CTS/ USART1_NSS, UART4_RX, FDCAN1_RX, HRTIM2_EEV11, LPTIM4_OUT, HRTIM1_FLT1, FDCAN2_RX, TIM13_CH1, EVENTOUT	OTG_FS_DM(boot)
78	78	76	A8	A8	101	101	109	109	109	137	137	137	B13	B13	PA12	I/O	FT_h	-	MCO1, TIM16_CH1N, HRTIM2_EEV12, SPI2_MOSI/ I2S2_SDO, TIM1_CH2N, USART1_RTS, UART4_TX, FDCAN1_TX, UART7_TX, HRTIM1_EEV7, ADF1_SDI0, COMP2_OUT, EVENTOUT	OTG_FS_DP(boot)
79	79	77	B7	B7	102	102	110	110	110	138	138	138	A13	A13	PA8	I/O	FT_c	-	TIM1_ETR, TIM4_ETR, LPUART1_RX, USART1_CK, I2C2_SMBA, FDCAN3_RX, USART2_RX, UART9_RX, TIM15_BKIN, SPI1_RDY, TIM1_CH3N, HRTIM1_EEV4, UART7_RX,	UCPD1_CC1

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
																			ADF1_CCK0, EVENTOUT	
80	80	78	C7	C7	103	103	111	111	111	139	139	139	C12	C12	PA9	I/O	FT_c	-	TIM16_BKIN, TIM2_ETR, LPUART1_TX, TIM8_ETR, TIM2_CH3, LPTIM2_IN2, USART1_TX, UART4_RTS, LPTIM4_ETR, HRTIM1_FLT3, HRTIM1_EEV9, UART7_TX, ADF1_CCK1, EVENTOUT	UCPD1_CC2
81	81	79	A7	A7	104	104	112	112	112	140	140	140	B12	B12	BOOT0	I	B	-	-	BOOT0
82	82	80	-	-	105	105	113	113	113	141	141	141	-	-	VDD	S	-	-	-	-
83	83	-	-	-	106	106	114	114	-	142	142	142	H8	H4	VSS	S	-	-	-	-
84	84	81	D6	D6	107	107	115	115	114	143	143	143	D10	D10	VCAP	S	-	-	-	-
85	85	82	C6	C6	108	108	116	116	115	144	144	144	C11	C11	PC8	I/O	FT_fh	-	HRTIM2_CHA1, TIM3_CH3, I3C1_SCL, TIM8_CH3, TIM20_CH3, SPI4_SCK, I2C3_SCL, UCPD1_FRSTX2, HRTIM1_EEV15, FMC_NE2/FMC_NCE, TIM10_CH1, EVENTOUT	-

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
86	86	83	A6	A6	109	109	117	117	116	145	145	145	A12	A12	PC9	I/O	FT_fh	-	HRTIM2_CHA2, TIM3_CH2, I3C1_SDA, TIM8_CH4, TIM8_BKIN2, UART9_TX, I2C3_SDA, SPI4_MISO, HRTIM1_EEV16, FMC_NE4, EVENTOUT	-
87	87	84	B6	B6	110	110	118	118	117	146	146	146	B11	B11	PC10	I/O	FT_h	-	DBTRGIO, HRTIM1_EEV1, I2C2_SMBA, TIM8_CH1N, I2C3_SMBA, SPI1_RDY, TIM20_CH4N, USART3_TX, UART4_TX, SPI4_RDY, TIM1_BKIN, HRTIM2_FLT8, FMC_NE1/FMC_NCE, UCPD1_FRSTX1, COMP8_OUT, EVENTOUT	-
-	-	-	-	-	-	-	-	-	118	147	147	147	A11	A11	PH13	I/O	FT_h	-	HRTIM2_EEV10, LPTIM1_IN2, UART8_RX, UART4_TX, FDCAN1_TX, HSP1_SNP3, EVENTOUT	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	-	-	-	-	119	148	148	148	C10	C10	PH14	I/O	FT_h	-	HRTIM2_FLT4, SPI2_MISO/I2S2_SDI, SPI3_MOSI/ I2S3_SDO, UART4_RX, FDCAN1_RX, HSP1_SNP4, EVENTOUT	-
-	-	-	-	-	-	-	-	-	120	149	149	149	B10	B10	PH15	I/O	FT_h	-	HRTIM2_EEV4, SPI2_MOSI/ I2S2_SDO, SPI3_MISO/I2S3_SDI, SPI6_RDY, HSP1_SNP5, EVENTOUT	-
-	-	-	-	-	-	-	-	-	-	-	-	-	J4	H8	VSS	S	-	-	-	-
88	88	85	A5	A5	111	111	119	119	121	150	150	150	A10	A10	PD2	I/O	FT_h	-	TRACED2, HRTIM2_CHB1, TIM3_ETR, XSPI1_CLK, TIM8_BKIN, SPI1_SCK/I2S1_CK, SPI4_MOSI, TIM20_ETR, UART5_RX, HRTIM1_EEV12, LPTIM5_OUT, EVENTOUT	WKUP8
89	89	86	A4	A4	112	112	120	120	122	151	151	151	B9	B9	PD3	I/O	FT_h	-	HRTIM2_CHB2, TIM1_CH1, XSPI1_NCLK, TIM8_BKIN2, SPI2_SCK/I2S2_CK, USART2_CTS/ USART2_NSS, UART5_TX, TIM2_CH4, HRTIM1_EEV3, EVENTOUT	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
90	90	87	B5	B5	113	113	121	121	123	152	152	152	C9	C9	PD4	I/O	FT_h	-	TIM1_CH2, TIM2_CH2, USART1_CTS/ USART1_NSS, USART2_RTS, XSPI1_IO3, SPI4_NSS, HRTIM1_FLT3, HRTIM2_CHC1, EVENTOUT	-
-	-	88	-	-	114	114	122	122	124	153	153	153	A9	A9	PD5	I/O	FT_h	-	HRTIM2_CHC2, TIM4_CH4, TIM8_ETR, SPI2_RDY, I2C1_SMBA, USART2_TX, XSPI1_IO2, TIM1_BKIN, TIM1_BKIN2, HRTIM1_EEV10, FMC_NWE, LPTIM5_ETR, EVENTOUT	-
-	-	-	-	-	-	-	123	123	-	154	154	154	J6	H9	VSS	S	-	-	-	-
-	-	-	-	-	-	-	124	124	125	155	155	155	-	-	VDD	S	-	-	-	-
-	-	89	C5	C5	115	115	125	125	126	156	156	156	B8	B8	PD6	I/O	FT_fh	-	HRTIM2_CHD1, SPI1_MISO/I2S1_SDI, I3C1_SCL, I2C1_SCL, USART2_RX, XSPI1_IO1, SPI3_MISO/I2S3_SDI, TIM2_CH1, HRTIM1_FLT5, LPTIM5_IN1, EVENTOUT	-

Pin number														Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	90	B4	B4	116	116	126	126	127	157	157	157	A8	A8	PD7	I/O	FT_fh	-	HRTIM2_CHD2, SPI1_MOSI/ I2S1_SDO, I3C1_SDA, TIM2_ETR, I2C1_SDA, USART2_CK, XSPI1_IO0, FDCAN1_RX, TIM2_CH3, TIM9_CH1, EVENTOUT	-
-	-	91	-	-	117	117	127	127	128	158	158	158	C8	C8	PG10	I/O	FT_fh	-	DBTRGI, HRTIM2_CHE1, SPI1_NSS/I2S1_WS, XSPI1_NCS1, I2C2_SDA, SPI3_SCK/ I2S3_CK, LPUART1_TX, FDCAN1_TX, TIM8_CH2, TIM9_CH2, EVENTOUT	-
-	-	-	-	-	118	118	128	128	129	159	159	159	A7	A7	PG11	I/O	FT_fh	-	DBTRGO, HRTIM2_CHE2, SPI1_SCK/I2S1_CK, I2C2_SCL, SPI3_NSS/ I2S3_WS, TIM20_CH1, LPTIM1_IN2, TIM8_CH1, TIM12_CH2, ADF1_CCK0, EVENTOUT	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	-	-	129	129	130	160	160	160	C7	C7	PG12	I/O	FT_h	-	HRTIM2_CHF1, TIM15_CH1N, SPI6_MISO, UART9_RTS, LPUART1_RX, LPTIM1_IN1, TIM8_CH3N, FMC_A0, ADF1_CCK1, EVENTOUT	-
-	-	-	-	-	-	-	130	130	131	161	161	161	B7	B7	PG13	I/O	FT_fh	-	TRACED0, HRTIM2_CHF2, I3C1_SDA, I2C3_SDA, SPI6_SCK, UART9_CTS, LPTIM1_CH1, FMC_A11, COMP6_OUT, TIM12_CH2, EVENTOUT	-
-	-	-	-	-	119	119	131	131	132	162	162	162	C6	C6	PG14	I/O	FT_fh	-	TRACED1, LPTIM1_ETR, I3C1_SCL, I2C3_SCL, SPI6_MOSI, SPI3_MOSI/ I2S3_SDO, UART9_TX, TIM20_CH1N, LPTIM1_CH2, HRTIM1_FLT4, FMC_A12, HRTIM2_FLT1, ADF1_SDI0, EVENTOUT	-
91	91	92	-	-	120	120	132	132	133	163	163	163	-	-	VDD	S	-	-	-	-
92	92	-	-	-	121	121	133	133	-	164	164	164	J7	J4	VSS	S	-	-	-	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
93	93	93	D4	D4	122	122	134	134	134	165	165	165	D6	D6	VCAP	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	J9	J7	VSS	S	-	-	-	-
-	-	-	-	-	-	-	135	135	135	166	166	166	A6	A6	PG15	I/O	FT_h	-	HRTIM2_EEV10, SPI6_NSS, UART9_CTS, SPI4_RDY, FMC_A13, COMP1_OUT, EVENTOUT	-
94	94	94	A3	A3	123	123	136	136	136	167	167	167	B6	B6	PB3(JTDO/TRACESWO)	I/O	FT_fh	(5)	JTDO/TRACESWO, TIM2_CH2, TIM3_ETR, XSPI1_IO4, I2C2_SDA(boot), TIM8_CH1N, FDCAN3_RX, USART3_TX, I2C3_SDA, LPTIM4_IN1, TIM4_ETR, I3C1_SDA, HRTIM1_FLT5, UART7_RX, UART5_RTS, EVENTOUT	-
95	95	95	C4	C4	124	124	137	137	137	168	168	168	A5	A5	PB4(NJTRST)	I/O	FT_fhb	(6)	NJTRST, TIM16_CH1, TIM3_CH1, XSPI1_IO5, I2C2_SCL(boot), TIM8_CH2N, FDCAN3_TX, TIM17_BKIN, I2C3_SCL, I2C1_SMBA, TIM2_CH1, I3C1_SCL, HRTIM1_EEV15, UART7_TX, UART5_CTS, EVENTOUT	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
96	96	96	A2	A2	125	125	138	138	138	169	169	169	A4	A4	PA13(JTMS/SWDIO)	I/O	FT_fh	(7)	JTMS/SWDIO, HRTIM1_FLT7, TIM3_CH4, I2C3_SCL, SPI1_MOSI/ I2S1_SDO, SPI3_MOSI/ I2S3_SDO, SPI6_MOSI, TIM15_BKIN, OTG_FS_SOF, FDCAN2_RX, TIM8_CH3N, EVENTOUT	-
97	97	97	B3	B3	126	126	139	139	139	170	170	170	B5	B5	PA14(JTCK/SWCLK)	I/O	FT_h	(8)	JTCK/SWCLK, TIM16_CH1N, TIM4_CH1, LPUART1_CTS, SPI1_SCK/I2S1_CK, UART8_TX, TIM15_CH1, FDCAN2_TX, TIM8_CH1, EVENTOUT	-
98	98	98	A1	A1	127	127	140	140	140	171	171	171	B4	B4	PA15(JTDI)	I/O	FT_fhb	(9)	JTDI, HRTIM1_SCIN, TIM4_CH2, I3C1_SCL(boot), I2C1_SCL, XSPI1_IO6, TIM3_ETR, TIM17_CH1N, TIM3_CH3, FDCAN1_RX, TIM8_BKIN, SPI1_NSS/I2S1_WS, HRTIM1_EEV6, TIM15_BKIN, TIM2_CH1, EVENTOUT	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
99	99	99	B2	B2	128	128	141	141	141	172	172	172	C5	C5	PB9	I/O	FT_fhb		MCO1, TIM17_CH1, TIM4_CH4, I3C1_SDA(boot), I2C1_SDA, XSPI1_IO7, TIM20_CH3, SPI2_NSS/I2S2_WS, UART8_RX, TIM1_CH2, TIM8_CH3, HRTIM2_FLT6, HRTIM1_EEV5, FDCAN1_TX, COMP3_OUT, EVENTOUT	WKUP5, TAMP_IN5/ TAMP_OUT4
-	-	-	-	-	-	-	142	142	142	173	173	173	A3	A3	PE1	I/O	FT_h	-	HRTIM1_EEV8, TIM4_ETR, TIM20_CH4, TIM17_CH1, UART8_TX, LPTIM1_IN2, FMC_SDCLK, EVENTOUT	-
-	-	-	-	-	-	-	143	143	-	174	174	174	J10	J8	VSS	S	-	-	-	-
-	-	-	-	-	-	-	144	144	143	175	175	175	-	-	VDD	S	-	-	-	-
-	-	-	-	-	-	-	-	-	144	176	176	176	C4	C4	PI4	I/O	FT_h	-	UART8_RTS, EVENTOUT	-
-	-	-	D7	D7	-	-	-	-	-	-	-	-	D4	D4	VDD	S	-	-	-	-
-	-	-	D5	D5	-	-	-	-	-	-	-	-	A1	A1	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	R15	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	R1	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	M11	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	M7	VSS	S	-	-	-	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	-	-	-	-	-	-	-	-	-	M6	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	M5	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	L12	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	L4	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	K12	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	K9	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	K7	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	K4	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	J12	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	J10	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	-	J9	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	G6	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	G7	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	J8	J6	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	H9	H7	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	G9	G7	VSS	S	-	-	-	-
-	-	-	G5	G5	-	-	-	-	-	-	-	-	D8	D8	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	R15	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	R1	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	M11	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	M7	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	M6	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	M5	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	L12	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	L4	-	VSS	S	-	-	-	-

Pin number															Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
LQFP100	LQFP100 SMPS	LQFP100 SMPS EP	TFBGA100	TFBGA100 SMPS	LQFP128	LQFP128 SMPS	LQFP144	LQFP144 SMPS	LQFP144 SMPS EP	LQFP176	LQFP176 SMPS	LQFP176 SMPS EP	UFBGA176+25	UFBGA176+25 SMPS						
-	-	-	-	-	-	-	-	-	-	-	-	-	K12	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	K9	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	K7	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	K4	-	VSS	S	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-	-	-	J12	-	VSS	S	-	-	-	-
-	-	-	F6	-	-	-	-	-	-	-	-	-	F8	-	VDD	S	-	-	-	-

1. *Tamper input is supplied by VSW.*
2. *Power supply is VSW - RTC and tamper pin (input/output). PC13, PC14, PC15 can provide limited amount of current, the use of PC14, PC15 GPIOs in output mode is limited - The speed must not exceed 1MHz. These GPIOs must not be used as current sources (for example to drive a LED).*
3. *Power supply is VSW - LSE pins. PC13, PC14, PC15 can provide limited amount of current, the use of PC13, PC14, PC15 GPIOs in output mode is limited - The speed must not exceed 500kHz with a maximum load of 30 pF. Speed in input mode must not exceed 1MHz. These GPIOs must not be used as current sources (for example to drive a LED).*
4. *I3C1_SDA is not a bootloader pin on LQFP64 SMPS package.*
5. *JTDO default debug pin.*
6. *NJRST default debug pin. The internal pull-up is activated after reset.*
7. *SWDIO default debug pin. The internal pull-up is activated after reset.*
8. *SWCLK default debug pin. The internal pull-down is activated after reset.*
9. *JTDI default debug pin. The internal pull-up is activated after reset.*

4.3 Alternate functions

Table 9. Alternate functions AF0 to AF7

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	HRTIM1/2 / I3C1 / LPTIM1 / SDMMC1 / TIM1/2/5/15/16/17	HRTIM2 / I2C2 / SPI2S1 / TIM1/2/3/4/5/15	HRTIM1/2 / I2C3 / I3C1 / LPTIM2 / LPUART1 / SDMMC1 / TIM8/15 / USART6 / XSPI1	HSP1 / I2C1/2/3 / LPTIM5 / TIM2/5/8/11/14/16/17 / USART1/6	FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / I2C2 / I3C1 / LPTIM1 / SDMMC1 / SPI2S1/2 / SPI5/6 / TIM2/8 / XSPI1	FDCAN3 / I2C1 / LPTIM2 / SDMMC1 / SPI2S3 / SPI6 / TIM1/3/8/20 / USART6/10	ADF1 / SPI2S2/3 / SPI4/6 / TIM17 / UART7/8/9 / USART1/2/3
Port A	PA0	TRACECLK	TIM2_CH1	TIM5_CH1	XSPI1_CLK	TIM11_CH1	SPI6_NSS	SPI3_RDY	USART2_CTS/ USART2_NSS

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	HRTIM1/2 / I3C1 / LPTIM1 / SDMMC1 / TIM1/2/5/15/16/17	HRTIM2 / I2C2 / SPI2S1 / TIM1/2/3/4/5/15	HRTIM1/2 / I2C3 / I3C1 / LPTIM2 / LPUART1 / SDMMC1 / TIM8/15 / USART6 / XSPI1	HSP1 / I2C1/2/3 / LPTIM5 / TIM2/5/8/11/14/16/17 / USART1/6	FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / I2C2 / I3C1 / LPTIM1 / SDMMC1 / SPI2S1/2 / SPI5/6 / TIM2/8 / XSPI1	FDCAN3 / I2C1 / LPTIM2 / SDMMC1 / SPI2S3 / SPI6 / TIM1/3/8/20 / USART6/10	ADF1 / SPI2S2/3 / SPI4/6 / TIM17 / UART7/8/9 / USART1/2/3
Port A	PA1	RTC_REFIN	TIM2_CH2	TIM5_CH2	XSPI1_IO3	-	LPTIM1_IN1	-	USART2_RTS
	PA2	-	TIM2_CH3	TIM5_CH3	LPUART1_TX	-	LPTIM1_IN2	SPI6_MOSI	USART2_TX
	PA3	-	TIM2_CH4	TIM5_CH4	LPUART1_RX	-	-	-	USART2_RX
	PA4	-	HRTIM2_EEV5	TIM3_CH4	HRTIM2_FLT3	-	SPI1_NSS/I2S1_WS	LPTIM2_CH1	USART2_CK
	PA5	-	HRTIM2_EEV10	TIM2_CH1	USART6_CTS/ USART6_NSS	TIM8_CH4	SDMMC1_CMD	-	ADF1_CCK0
	PA6	-	TIM16_CH1	TIM3_CH1	USART6_RTS	TIM8_BKIN	SDMMC1_D0	TIM1_BKIN	ADF1_CCK1
	PA7	-	TIM17_CH1	TIM3_CH2	SDMMC1_D1	TIM8_CH1N	SPI1_RDY	TIM1_CH1N	USART1_CK
	PA8	-	TIM1_ETR	TIM4_ETR	LPUART1_RX	USART1_CK	I2C2_SMBA	FDCAN3_RX	USART2_RX
	PA9	-	TIM16_BKIN	TIM2_ETR	LPUART1_TX	TIM8_ETR	TIM2_CH3	LPTIM2_IN2	USART1_TX
	PA10	-	TIM17_BKIN	TIM2_CH1	LPUART1_TX	TIM8_CH1N	FMC_NBL0	TIM1_CH3	USART1_RX
	PA11	-	TIM1_CH4N	TIM1_BKIN2	-	-	SPI2_MISO/I2S2_SDI	TIM1_CH1N	USART1_CTS/ USART1_NSS
	PA12	MCO1	TIM16_CH1N	HRTIM2_EEV12	-	-	SPI2_MOSI/I2S2_SDO	TIM1_CH2N	USART1_RTS
	PA13	JTMS/SWDIO	HRTIM1_FLT7	TIM3_CH4	-	I2C3_SCL	SPI1_MOSI/I2S1_SDO	-	SPI3_MOSI/ I2S3_SDO
	PA14	JTCK/SWCLK	TIM16_CH1N	TIM4_CH1	LPUART1_CTS	-	SPI1_SCK/I2S1_CK	-	UART8_TX
	PA15	JTDI	HRTIM1_SCIN	TIM4_CH2	I3C1_SCL	I2C1_SCL	XSPI1_IO6	TIM3_ETR	TIM17_CH1N
Port B	PB0	-	TIM16_BKIN	TIM1_CH4	LPTIM2_IN2	TIM8_CH2N	SPI1_SCK/I2S1_CK	TIM1_CH2N	TIM17_CH1N
	PB1	-	HRTIM1_SCOUT	TIM3_CH3	LPTIM2_CH2	TIM8_CH3N	SPI1_MISO/I2S1_SDI	TIM1_CH3N	USART2_RX
	PB2	RTC_OUT2	SDMMC1_CK	TIM3_CH4	HRTIM1_FLT6	TIM5_CH1	SPI1_MOSI/I2S1_SDO	TIM20_CH1	-
	PB3	JTDO/ TRACESWO	TIM2_CH2	TIM3_ETR	XSPI1_IO4	I2C2_SDA	TIM8_CH1N	FDCAN3_RX	USART3_TX
	PB4	NJTRST	TIM16_CH1	TIM3_CH1	XSPI1_IO5	I2C2_SCL	TIM8_CH2N	FDCAN3_TX	TIM17_BKIN
	PB5	-	TIM16_CH1	TIM4_CH3	TIM8_CH2N	USART6_CK	I2S2_MCK	-	USART3_CTS/ USART3_NSS
	PB6	-	TIM1_BKIN2	TIM4_CH4	-	I2C1_SDA	TIM8_CH2	-	USART2_TX

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	HRTIM1/2 / I3C1 / LPTIM1 / SDMMC1 / TIM1/2/5/15/16/17	HRTIM2 / I2C2 / SPI2S1 / TIM1/2/3/4/5/15	HRTIM1/2 / I2C3 / I3C1 / LPTIM2 / LPUART1 / SDMMC1 / TIM8/15 / USART6 / XSPI1	HSP1 / I2C1/2/3 / LPTIM5 / TIM2/5/8/11/14/16/17 / USART1/6	FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / I2C2 / I3C1 / LPTIM1 / SDMMC1 / SPI2S1/2 / SPI5/6 / TIM2/8 / XSPI1	FDCAN3 / I2C1 / LPTIM2 / SDMMC1 / SPI2S3 / SPI6 / TIM1/3/8/20 / USART6/10	ADF1 / SPI2S2/3 / SPI4/6 / TIM17 / UART7/8/9 / USART1/2/3
Port B	PB7	-	HRTIM1_CHB1	TIM2_CH1	TIM8_CH1	-	SPI1_NSS/I2S1_WS	SPI3_NSS/ I2S3_WS	SPI6_NSS
	PB8	-	SDMMC1_D5	SPI1_SCK/ I2S1_CK	-	I2C2_SDA	I3C1_SDA	TIM20_CH4N	USART3_RX
	PB9	MCO1	TIM17_CH1	TIM4_CH4	I3C1_SDA	I2C1_SDA	XSPI1_IO7	TIM20_CH3	SPI2_NSS/ I2S2_WS
	PB10	-	HRTIM1_FLT3	TIM2_CH3	-	HSP1_SNP3	-	LPTIM2_IN1	USART3_TX
	PB11	-	HRTIM1_FLT4	TIM1_CH3N	LPTIM2_ETR	HSP1_SNP4	SPI2_RDY	-	USART3_RX
	PB12	-	HRTIM1_FLT2	TIM5_CH4	TIM8_BKIN2	TIM14_CH1	SPI2_NSS/I2S2_WS	-	USART3_CK
	PB13	-	HRTIM1_FLT6	TIM1_CH1	LPTIM2_CH1	TIM14_CH1	SPI2_SCK/I2S2_CK	-	USART3_CTS/ USART3_NSS
	PB14	MCO2	TIM15_CH1	TIM1_CH2	HRTIM2_EEV6	USART1_TX	SPI2_MISO/I2S2_SDI	-	USART3_RTS
	PB15	MCO2	TIM15_CH2	TIM15_CH1N	-	USART1_RX	SPI2_MOSI/I2S2_SDO	TIM1_CH3	UART9_TX
Port C	PC0	AUDIOCLK	HRTIM1_EEV8	HRTIM2_EEV8	XSPI1_IO1	TIM11_CH1	LPTIM1_CH1	TIM1_CH1	SPI2_RDY
	PC1	TRACED0	HRTIM1_EEV5	HRTIM2_EEV5	XSPI1_IO2	TIM14_CH1	SPI2_MOSI/I2S2_SDO	USART10_RX	USART1_RTS
	PC2	PWR_CSTOP	TIM1_CH3	TIM2_ETR	-	-	SPI2_MOSI/I2S2_SDO	-	UART9_CTS
	PC3	PWR_CSLEEP	HRTIM1_EEV9	TIM1_CH4	XSPI1_IO0	HSP1_SNP1	SPI2_MISO/I2S2_SDI	SPI3_NSS/ I2S3_WS	UART9_RTS
	PC4	-	HRTIM1_FLT1	TIM1_ETR	LPTIM2_ETR	USART1_TX	I2S1_MCK	TIM8_CH2	-
	PC5	-	HRTIM1_EEV10	TIM15_BKIN	-	USART1_RX	LPTIM1_IN2	TIM1_CH4N	SPI3_NSS/ I2S3_WS
	PC6	-	HRTIM1_EEV10	TIM3_CH1	TIM8_BKIN	TIM8_CH1	SDMMC1_D6	SDMMC1_D0DIR	I2S2_MCK
	PC7	TRACED2	HRTIM1_FLT5	TIM3_CH2	I2C3_SCL	TIM8_CH3	XSPI1_IO4	-	USART3_RTS
	PC8	-	HRTIM2_CHA1	TIM3_CH3	I3C1_SCL	TIM8_CH3	-	TIM20_CH3	SPI4_SCK
	PC9	-	HRTIM2_CHA2	TIM3_CH2	I3C1_SDA	TIM8_CH4	-	TIM8_BKIN2	UART9_TX
	PC10	DBTRGIO	HRTIM1_EEV1	I2C2_SMBA	TIM8_CH1N	I2C3_SMBA	SPI1_RDY	TIM20_CH4N	USART3_TX
	PC11	TRACED1	HRTIM1_CHC1	TIM4_CH1	LPUART1_CTS	TIM8_CH2N	SPI1_MISO/I2S1_SDI	SPI3_MISO/ I2S3_SDI	USART3_RX

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	HRTIM1/2 / I3C1 / LPTIM1 / SDMMC1 / TIM1/2/5/15/16/17	HRTIM2 / I2C2 / SPI2S1 / TIM1/2/3/4/5/15	HRTIM1/2 / I2C3 / I3C1 / LPTIM2 / LPUART1 / SDMMC1 / TIM8/15 / USART6 / XSPI1	HSP1 / I2C1/2/3 / LPTIM5 / TIM2/5/8/11/14/16/17 / USART1/6	FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / I2C2 / I3C1 / LPTIM1 / SDMMC1 / SPI2S1/2 / SPI5/6 / TIM2/8 / XSPI1	FDCAN3 / I2C1 / LPTIM2 / SDMMC1 / SPI2S3 / SPI6 / TIM1/3/8/20 / USART6/10	ADF1 / SPI2S2/3 / SPI4/6 / TIM17 / UART7/8/9 / USART1/2/3
Port C	PC12	TRACED3	HRTIM1_CHC2	TIM5_CH2	LPUART1_RTS	I2C2_SDA	XSPI1_IO6	SPI3_MOSI/ I2S3_SDO	USART3_CK
	PC13	-	-	TIM1_BKIN	LPUART1_TX	TIM8_BKIN	SPI2_NSS/I2S2_WS	-	TIM17_BKIN
	PC14	-	TIM16_BKIN	TIM1_BKIN	LPUART1_RX	-	LPTIM1_IN1	-	USART2_RX
	PC15	-	TIM15_BKIN	-	LPUART1_TX	TIM8_BKIN	LPTIM1_IN2	-	USART2_TX
Port D	PD0	-	HRTIM1_EEV5	I2C2_SMBA	XSPI1_DQS0	I2C3_SCL	SPI1_MOSI/I2S1_SDO	-	-
	PD1	-	HRTIM1_EEV8	SPI1_MISO/ I2S1_SDI	XSPI1_NCS2	I2C3_SDA	-	-	-
	PD2	TRACED2	HRTIM2_CHB1	TIM3_ETR	XSPI1_CLK	TIM8_BKIN	SPI1_SCK/I2S1_CK	-	SPI4_MOSI
	PD3	-	HRTIM2_CHB2	TIM1_CH1	XSPI1_NCLK	TIM8_BKIN2	SPI2_SCK/I2S2_CK	-	USART2_CTS/ USART2_NSS
	PD4	-	TIM1_CH2	TIM2_CH2	-	USART1_CTS/ USART1_NSS	-	-	USART2_RTS
	PD5	-	HRTIM2_CHC2	TIM4_CH4	-	TIM8_ETR	SPI2_RDY	I2C1_SMBA	USART2_TX
	PD6	-	HRTIM2_CHD1	SPI1_MISO/ I2S1_SDI	I3C1_SCL	-	-	I2C1_SCL	USART2_RX
	PD7	-	HRTIM2_CHD2	SPI1_MOSI/ I2S1_SDO	I3C1_SDA	TIM2_ETR	-	I2C1_SDA	USART2_CK
	PD8	-	HRTIM1_EEV4	TIM4_ETR	HRTIM2_FLT1	-	SPI5_SCK	-	USART3_TX
	PD9	-	HRTIM1_EEV6	HRTIM2_EEV1	-	-	SPI5_MISO	-	USART3_RX
	PD10	-	HRTIM1_SCOUT	HRTIM2_EEV5	LPTIM2_CH2	-	SPI5_MOSI	-	USART3_CK
	PD11	-	TIM5_ETR	TIM4_CH2	LPTIM2_IN2	LPTIM5_IN1	SPI5_NSS	TIM8_ETR	USART3_CTS/ USART3_NSS
	PD12	-	-	TIM4_CH3	LPTIM2_IN1	-	SPI5_RDY	-	USART3_RTS
	PD13	-	LPTIM1_CH1	TIM4_CH2	LPTIM2_CH1	-	SPI5_NSS	-	SPI4_RDY
	PD14	-	HRTIM1_EEV11	TIM4_CH3	XSPI1_IO5	-	-	-	-
	PD15	-	TIM1_CH1	TIM4_CH4	XSPI1_IO4	TIM16_BKIN	-	-	SPI2_NSS/ I2S2_WS
Port E	PE0	-	TIM16_CH1	-	LPTIM2_CH2	USART1_TX	-	LPTIM2_ETR	SPI3_RDY

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	HRTIM1/2 / I3C1 / LPTIM1 / SDMMC1 / TIM1/2/5/15/16/17	HRTIM2 / I2C2 / SPI2S1 / TIM1/2/3/4/5/15	HRTIM1/2 / I2C3 / I3C1 / LPTIM2 / LPUART1 / SDMMC1 / TIM8/15 / USART6 / XSPI1	HSP1 / I2C1/2/3 / LPTIM5 / TIM2/5/8/11/14/16/17 / USART1/6	FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / I2C2 / I3C1 / LPTIM1 / SDMMC1 / SPI2S1/2 / SPI5/6 / TIM2/8 / XSPI1	FDCAN3 / I2C1 / LPTIM2 / SDMMC1 / SPI2S3 / SPI6 / TIM1/3/8/20 / USART6/10	ADF1 / SPI2S2/3 / SPI4/6 / TIM17 / UART7/8/9 / USART1/2/3
Port E	PE1	-	HRTIM1_EEV8	TIM4_ETR	-	-	-	TIM20_CH4	TIM17_CH1
	PE2	TRACECLK	LPTIM1_IN2	TIM3_CH1	TIM8_CH4N	HSP1_SNP0	I2C2_SCL	USART10_CK	SPI4_SCK
	PE3	TRACED0	HRTIM1_EEV8	TIM3_CH2	HRTIM2_EEV13	HSP1_SNP1	I2C2_SDA	-	SPI4_NSS
	PE4	TRACED1	-	TIM3_CH3	HRTIM2_EEV14	I2C3_SDA	SPI1_NSS/I2S1_WS	USART10_CTS/ USART10_NSS	SPI4_NSS
	PE5	TRACED2	I3C1_SCL	TIM3_CH4	HRTIM2_EEV12	I2C3_SCL	I2C2_SCL	USART10_RTS	SPI4_MISO
	PE6	TRACED3	I3C1_SDA	TIM4_CH3	HRTIM2_EEV16	HSP1_SNP4	I2C2_SDA	TIM20_CH3N	SPI4_MOSI
	PE7	-	-	TIM1_ETR	-	-	-	-	UART7_RX
	PE8	-	TIM5_CH3	TIM1_CH1N	-	-	-	TIM20_CH4N	UART7_TX
	PE9	-	TIM5_ETR	TIM1_CH1	-	-	-	-	UART7_RTS
	PE10	-	HRTIM2_FLT3	TIM1_CH2N	-	-	-	-	UART7_CTS
	PE11	-	HRTIM2_FLT4	TIM1_CH2	-	-	-	-	-
	PE12	-	HRTIM2_FLT5	TIM1_CH3N	USART6_CK	-	-	-	-
	PE13	-	HRTIM2_FLT6	TIM1_CH3	USART6_RX	-	-	-	SPI4_MISO
	PE14	-	HRTIM2_EEV3	TIM1_CH4	USART6_TX	-	-	TIM1_BKIN2	SPI4_MOSI
	PE15	-	HRTIM2_EEV2	TIM1_BKIN	-	-	-	TIM1_CH4N	USART3_RX
Port F	PF0	-	HRTIM1_SCIN	HRTIM2_EEV9	-	-	SPI2_MISO/I2S2_SDI	-	USART1_TX
	PF1	-	TIM16_CH1	HRTIM2_FLT3	-	-	SPI5_RDY	-	USART1_RX
	PF2	-	TIM16_CH1N	HRTIM2_FLT5	XSPI1_NCLK	TIM17_CH1	-	SPI3_MOSI/ I2S3_SDO	-
	PF3	-	HRTIM1_EEV1	HRTIM2_FLT2	-	-	SPI2_SCK/I2S2_CK	SPI3_NSS/ I2S3_WS	USART2_TX
	PF4	-	HRTIM1_EEV2	HRTIM2_FLT4	-	HSP1_SNP5	SPI2_MOSI/I2S2_SDO	-	USART2_RX
	PF5	-	-	HRTIM2_EEV9	-	-	SPI5_RDY	-	-
	PF6	-	TIM5_ETR	HRTIM2_EEV2	-	TIM5_CH1	SPI5_NSS	-	USART3_RTS
	PF7	TRACED3	HRTIM2_EEV8	TIM4_CH3	-	TIM5_CH2	SPI5_SCK	SPI3_SCK/ I2S3_CK	UART7_TX

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	HRTIM1/2 / I3C1 / LPTIM1 / SDMMC1 / TIM1/2/5/15/16/17	HRTIM2 / I2C2 / SPI2S1 / TIM1/2/3/4/5/15	HRTIM1/2 / I2C3 / I3C1 / LPTIM2 / LPUART1 / SDMMC1 / TIM8/15 / USART6 / XSPI1	HSP1 / I2C1/2/3 / LPTIM5 / TIM2/5/8/11/14/16/17 / USART1/6	FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / I2C2 / I3C1 / LPTIM1 / SDMMC1 / SPI2S1/2 / SPI5/6 / TIM2/8 / XSPI1	FDCAN3 / I2C1 / LPTIM2 / SDMMC1 / SPI2S3 / SPI6 / TIM1/3/8/20 / USART6/10	ADF1 / SPI2S2/3 / SPI4/6 / TIM17 / UART7/8/9 / USART1/2/3
Port F	PF8	TRACECLK	HRTIM2_EEV6	TIM4_CH2	-	TIM5_CH3	SPI5_MISO	SPI3_MISO/ I2S3_SDI	UART7_RTS
	PF9	-	HRTIM2_EEV4	TIM4_CH1	TIM15_CH1	TIM5_CH4	SPI5_MOSI	USART6_RX	SPI2_SCK/ I2S2_CK
	PF10	-	HRTIM1_SCOUT	HRTIM2_EEV3	TIM15_CH2	-	SPI2_NSS/I2S2_WS	USART6_TX	UART7_CTS
	PF11	-	-	HRTIM2_EEV10	-	-	-	-	-
	PF12	-	LPTIM1_ETR	HRTIM2_FLT5	-	-	-	TIM1_CH4N	-
	PF13	-	LPTIM1_CH2	HRTIM2_SCOUT	-	-	-	-	-
	PF14	-	-	HRTIM2_SCIN	LPTIM2_CH1	TIM5_CH1	-	-	UART9_RTS
	PF15	-	-	HRTIM2_EEV9	LPTIM2_CH2	TIM5_CH2	-	-	UART9_CTS
Port G	PG0	-	-	HRTIM2_EEV3	LPTIM2_IN1	-	-	-	-
	PG1	-	-	-	LPTIM2_IN2	-	-	-	SPI2_MOSI/ I2S2_SDO
	PG2	-	HRTIM2_FLT1	-	-	-	-	-	-
	PG3	-	HRTIM2_EEV9	-	-	-	-	-	-
	PG4	-	HRTIM1_EEV2	SPI1_MISO/ I2S1_SDI	-	TIM5_CH1	SPI5_NSS	-	-
	PG5	-	HRTIM1_EEV7	SPI1_MOSI/ I2S1_SDO	-	TIM5_CH3	SPI5_RDY	-	-
	PG6	-	HRTIM2_EEV1	SPI1_RDY	-	I2C3_SMBA	-	-	-
	PG7	-	HRTIM2_EEV5	-	-	-	-	-	-
	PG8	-	HRTIM2_EEV13	-	-	-	SPI6_NSS	-	UART9_RTS
	PG9	-	HRTIM1_FLT1	SPI1_SCK/ I2S1_CK	-	TIM5_CH4	-	SPI3_SCK/ I2S3_CK	UART9_RX
	PG10	DBTRGI	HRTIM2_CHE1	SPI1_NSS/ I2S1_WS	XSPI1_NCS1	I2C2_SDA	-	-	SPI3_SCK/ I2S3_CK
	PG11	DBTRGO	HRTIM2_CHE2	SPI1_SCK/ I2S1_CK	-	I2C2_SCL	-	-	SPI3_NSS/ I2S3_WS
	PG12	-	HRTIM2_CHF1	TIM15_CH1N	-	-	SPI6_MISO	-	UART9_RTS

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	HRTIM1/2 / I3C1 / LPTIM1 / SDMMC1 / TIM1/2/5/15/16/17	HRTIM2 / I2C2 / SPI2S1 / TIM1/2/3/4/5/15	HRTIM1/2 / I2C3 / I3C1 / LPTIM2 / LPUART1 / SDMMC1 / TIM8/15 / USART6 / XSPI1	HSP1 / I2C1/2/3 / LPTIM5 / TIM2/5/8/11/14/16/17 / USART1/6	FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / I2C2 / I3C1 / LPTIM1 / SDMMC1 / SPI2S1/2 / SPI5/6 / TIM2/8 / XSPI1	FDCAN3 / I2C1 / LPTIM2 / SDMMC1 / SPI2S3 / SPI6 / TIM1/3/8/20 / USART6/10	ADF1 / SPI2S2/3 / SPI4/6 / TIM17 / UART7/8/9 / USART1/2/3
Port G	PG13	TRACED0	HRTIM2_CHF2	-	I3C1_SDA	I2C3_SDA	SPI6_SCK	-	UART9_CTS
	PG14	TRACED1	LPTIM1_ETR	-	I3C1_SCL	I2C3_SCL	SPI6_MOSI	SPI3_MOSI/ I2S3_SDO	UART9_TX
	PG15	-	-	HRTIM2_EEV10	-	-	SPI6_NSS	-	UART9_CTS
Port H	PH0	-	HRTIM1_EEV7	TIM1_CH3N	TIM8_CH3	TIM5_CH1	SPI2_SCK/I2S2_CK	-	USART1_TX
	PH1	-	HRTIM1_EEV11	TIM1_ETR	-	TIM8_CH4	SPI2_SCK/I2S2_CK	-	USART1_RX
	PH2	-	LPTIM1_IN2	HRTIM2_SCOUT	-	I2C1_SCL	-	-	-
	PH3	-	-	HRTIM2_FLT8	-	I2C1_SDA	-	-	-
	PH4	-	HRTIM2_FLT6	-	-	-	-	-	SPI6_RDY
	PH5	-	HRTIM1_SCOUT	-	-	TIM17_CH1	-	TIM20_CH2N	SPI6_RDY
	PH6	-	HRTIM1_EEV2	-	-	I2C2_SMBA	SPI5_SCK	-	USART1_RX
	PH7	-	HRTIM1_EEV7	-	-	I2C3_SCL	SPI5_MISO	-	-
	PH8	-	-	-	-	I2C3_SDA	SPI5_MOSI	-	-
	PH9	-	-	-	-	TIM11_CH1	SPI5_NSS	FDCAN3_RX	-
	PH10	-	-	-	-	-	SPI5_RDY	FDCAN3_TX	-
	PH11	-	-	HRTIM2_EEV11	I3C1_SCL	I2C2_SCL	-	-	-
	PH12	-	-	HRTIM2_EEV15	I3C1_SDA	I2C2_SDA	-	-	-
	PH13	-	-	HRTIM2_EEV10	-	-	LPTIM1_IN2	-	UART8_RX
	PH14	-	-	HRTIM2_FLT4	-	-	SPI2_MISO/I2S2_SDI	-	SPI3_MOSI/ I2S3_SDO
	PH15	-	-	HRTIM2_EEV4	-	-	SPI2_MOSI/I2S2_SDO	-	SPI3_MISO/ I2S3_SDI
Port I	PI0	-	-	-	-	-	SPI2_NSS/I2S2_WS	-	UART8_RX
	PI1	-	-	-	-	-	SPI2_SCK/I2S2_CK	-	UART8_TX
	PI2	-	TIM15_BKIN	SPI1_MOSI/ I2S1_SDO	SDMMC1_D123DIR	I2C2_SCL	I3C1_SCL	SDMMC1_D7	USART2_TX

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS	HRTIM1/2 / I3C1 / LPTIM1 / SDMMC1 / TIM1/2/5/15/16/17	HRTIM2 / I2C2 / SPI2S1 / TIM1/2/3/4/5/15	HRTIM1/2 / I2C3 / I3C1 / LPTIM2 / LPUART1 / SDMMC1 / TIM8/15 / USART6 / XSPI1	HSP1 / I2C1/2/3 / LPTIM5 / TIM2/5/8/11/14/16/17 / USART1/6	FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / I2C2 / I3C1 / LPTIM1 / SDMMC1 / SPI2S1/2 / SPI5/6 / TIM2/8 / XSPI1	FDCAN3 / I2C1 / LPTIM2 / SDMMC1 / SPI2S3 / SPI6 / TIM1/3/8/20 / USART6/10	ADF1 / SPI2S2/3 / SPI4/6 / TIM17 / UART7/8/9 / USART1/2/3
Port I	PI3	-	-	-	-	-	-	-	UART8_CTS
	PI4	-	-	-	-	-	-	-	UART8_RTS
	PI8	-	-	-	-	-	-	LPTIM2_IN2	UART8_RX

Table 10. Alternate functions AF8 to AF15

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ADF1 / FDCAN3 / I2C3 / LPUART1 / SPI6 / TIM3/20 / UART4/8/9 / XSPI1	FDCAN1 / I2C1 / LPTIM1/4 / SPI2S3 / SPI4 / TIM1/15/20 / UART5 / UCPD1 / USART10 / XSPI1	HRTIM2 / HSP1 / LPTIM3/4 / SDMMC1 / SPI2S1 / TIM1/2/4/8 / UART7 / UCPD1 / USART6/10 / XSPI1	FMC(NORmux) / FMC(NOR_RAM) / HRTIM1/2 / I2C2 / I3C1 / LPTIM3/4/5 / OTG_FS / SDMMC1 / SPI2S1 / TIM1/9 / USART10	FMC(NAND16) / FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / HRTIM1/2 / SDMMC1 / XSPI1	ADF1 / COMP1/4/6/7 / FDCAN1/2 / FMC(NORmux) / FMC(NOR_RAM) / HRTIM2 / HSP1 / LPTIM4/5 / SDMMC1 / TIM12/15 / UART7 / UCPD1	ADF1 / COMP2/3/5/6/8 / CRS / SDMMC1 / TIM2/8/10/12/13/15/20 / UART5/7	EVENTOUT
Port A	PA0	UART4_TX	-	HSP1_SNP2	LPTIM3_IN1	FMC_D15/FMC_AD15	COMP1_OUT	TIM8_BKIN	EVENTOUT
	PA1	UART4_RX	TIM15_CH1N	-	USART10_CK	FMC_A5	HRTIM2_EEV10	TIM10_CH1	EVENTOUT
	PA2	UART4_CTS	TIM15_CH1	XSPI1_NCS1	-	HRTIM1_EEV3	FMC_NE3	COMP2_OUT	EVENTOUT
	PA3	-	TIM15_CH2	XSPI1_DQS0	-	FMC_NL	HRTIM2_EEV7	-	EVENTOUT
	PA4	SPI6_NSS	-	XSPI1_NCS2	SDMMC1_CKIN	-	FDCAN2_RX	-	EVENTOUT
	PA5	SPI6_SCK	LPTIM1_CH2	XSPI1_NCS1	TIM9_CH1	-	FDCAN2_TX	UART5_RX	EVENTOUT
	PA6	SPI6_MISO	FDCAN1_RX	TIM8_CH2	LPTIM3_IN2	HRTIM2_EEV11	COMP1_OUT	UART5_TX	EVENTOUT
	PA7	ADF1_SDI0	FDCAN1_TX	LPTIM3_ETR	HRTIM1_EEV10	FMC_NWE	HRTIM2_EEV4	COMP2_OUT	EVENTOUT
	PA8	UART9_RX	TIM15_BKIN	SPI1_RDY	TIM1_CH3N	HRTIM1_EEV4	UART7_RX	ADF1_CCK0	EVENTOUT
	PA9	UART4_RTS	-	LPTIM4_ETR	HRTIM1_FLT3	HRTIM1_EEV9	UART7_TX	ADF1_CCK1	EVENTOUT
	PA10	UART4_RX	UCPD1_FRSTX2	TIM8_BKIN	TIM1_CH3N	HRTIM1_CHB2	FDCAN2_TX	COMP6_OUT	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ADF1 / FDCAN3 / I2C3 / LPUART1 / SPI6 / TIM3/20 / UART4/8/9 / XSPI1	FDCAN1 / I2C1 / LPTIM1/4 / SPI2S3 / SPI4 / TIM1/15/20 / UART5 / UCPD1 / USART10 / XSPI1	HRTIM2 / HSP1 / LPTIM3/4 / SDMMC1 / SPI2S1 / TIM1/2/4/8 / UART7 / UCPD1 / USART6/10 / XSPI1	FMC(NORmux) / FMC(NOR_RAM) / HRTIM1/2 / I2C2 / I3C1 / LPTIM3/4/5 / OTG_FS / SDMMC1 / SPI2S1 / TIM1/9 / USART10	FMC(NAND16) / FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / HRTIM1/2 / SDMMC1 / XSPI1	ADF1 / COMP1/4/6/7 / FDCAN1/2 / FMC(NORmux) / FMC(NOR_RAM) / HRTIM2 / HSP1 / LPTIM4/5 / SDMMC1 / TIM12/15 / UART7 / UCPD1	ADF1 / COMP2/3/5/6/8 / CRS / SDMMC1 / TIM2/8/10/12/13/15/20 / UART5/7	EVENTOUT
Port A	PA11	UART4_RX	FDCAN1_RX	HRTIM2_EEV11	LPTIM4_OUT	HRTIM1_FLT1	FDCAN2_RX	TIM13_CH1	EVENTOUT
	PA12	UART4_TX	FDCAN1_TX	UART7_TX	-	HRTIM1_EEV7	ADF1_SDI0	COMP2_OUT	EVENTOUT
	PA13	SPI6_MOSI	TIM15_BKIN	-	OTG_FS_SOF	-	FDCAN2_RX	TIM8_CH3N	EVENTOUT
	PA14	-	TIM15_CH1	-	-	-	FDCAN2_TX	TIM8_CH1	EVENTOUT
	PA15	TIM3_CH3	FDCAN1_RX	TIM8_BKIN	SPI1_NSS/ I2S1_WS	HRTIM1_EEV6	TIM15_BKIN	TIM2_CH1	EVENTOUT
Port B	PB0	SPI6_SCK	SPI3_SCK/ I2S3_CK	USART6_TX	HRTIM1_FLT5	FMC_INT	SDMMC1_D2	COMP5_OUT	EVENTOUT
	PB1	SPI6_MISO	SPI3_MISO/ I2S3_SDI	SDMMC1_D3	HRTIM1_EEV6	XSPI1_CLK	COMP4_OUT	TIM20_CH1N	EVENTOUT
	PB2	SPI6_MOSI	LPTIM1_CH1	USART6_RX	HRTIM1_SCIN	XSPI1_NCLK	HRTIM2_FLT2	COMP8_OUT	EVENTOUT
	PB3	I2C3_SDA	LPTIM4_IN1	TIM4_ETR	I3C1_SDA	HRTIM1_FLT5	UART7_RX	UART5_RTS	EVENTOUT
	PB4	I2C3_SCL	I2C1_SMBA	TIM2_CH1	I3C1_SCL	HRTIM1_EEV15	UART7_TX	UART5_CTS	EVENTOUT
	PB5	I2C3_SDA	I2C1_SCL	TIM8_CH1N	LPTIM5_ETR	HRTIM1_CHA1	COMP4_OUT	CRS_SYNC	EVENTOUT
	PB6	UART4_CTS	SPI3_SCK/ I2S3_CK	SDMMC1_D4	HRTIM2_FLT2	HRTIM1_CHA2	COMP7_OUT	TIM12_CH1	EVENTOUT
	PB7	FDCAN3_TX	TIM1_BKIN	TIM2_ETR	FMC_A24	HRTIM2_FLT3	COMP1_OUT	TIM12_CH2	EVENTOUT
	PB8	UART8_TX	TIM20_BKIN	TIM8_ETR	USART10_CTS/ USART10_NSS	HRTIM1_CHD2	COMP7_OUT	SDMMC1_CDIR	EVENTOUT
	PB9	UART8_RX	TIM1_CH2	TIM8_CH3	HRTIM2_FLT6	HRTIM1_EEV5	FDCAN1_TX	COMP3_OUT	EVENTOUT
	PB10	LPUART1_RX	TIM1_BKIN	-	-	FMC_CLK	HRTIM2_EEV9	CRS_SYNC	EVENTOUT
	PB11	LPUART1_TX	SPI4_NSS	TIM2_CH4	TIM9_CH1	FMC_NBL1	HRTIM2_EEV8	-	EVENTOUT
	PB12	LPUART1_RTS	TIM1_BKIN	UCPD1_FRSTX1	TIM9_CH2	FMC_D3/ FMC_AD3	FDCAN1_RX	UART5_RX	EVENTOUT
	PB13	LPUART1_CTS	LPTIM1_ETR	TIM8_CH4	HRTIM2_FLT7	FMC_D4/ FMC_AD4	FDCAN1_TX	UART5_TX	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ADF1 / FDCAN3 / I2C3 / LPUART1 / SPI6 / TIM3/20 / UART4/8/9 / XSPI1	FDCAN1 / I2C1 / LPTIM1/4 / SPI2S3 / SPI4 / TIM1/15/20 / UART5 / UCPD1 / USART10 / XSPI1	HRTIM2 / HSP1 / LPTIM3/4 / SDMMC1 / SPI2S1 / TIM1/2/4/8 / UART7 / UCPD1 / USART6/10 / XSPI1	FMC(NORmux) / FMC(NOR_RAM) / HRTIM1/2 / I2C2 / I3C1 / LPTIM3/4/5 / OTG_FS / SDMMC1 / SPI2S1 / TIM1/9 / USART10	FMC(NAND16) / FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / HRTIM1/2 / SDMMC1 / XSPI1	ADF1 / COMP1/4/6/7 / FDCAN1/2 / FMC(NORmux) / FMC(NOR_RAM) / HRTIM2 / HSP1 / LPTIM4/5 / SDMMC1 / TIM12/15 / UART7 / UCPD1	ADF1 / COMP2/3/5/6/8 / CRS / SDMMC1 / TIM2/8/10/12/13/15/20 / UART5/7	EVENTOUT
Port B	PB14	UART4_RTS	LPTIM1_CH2	TIM8_CH4N	HRTIM1_EEV1	FMC_NOE	COMP4_OUT	-	EVENTOUT
	PB15	UART4_CTS	UART5_RX	HSP1_SNP5	HRTIM1_EEV2	FMC_NWE	HRTIM2_FLT4	COMP3_OUT	EVENTOUT
Port C	PC0	LPUART1_RX	-	USART6_CK	USART10_CTS/ USART10_NSS	SDMMC1_D4	COMP7_OUT	ADF1_CCK0	EVENTOUT
	PC1	LPUART1_TX	TIM1_CH2	-	LPTIM3_CH1	SDMMC1_D5	HSP1_SNP0	ADF1_CCK1	EVENTOUT
	PC2	-	TIM20_CH2	HRTIM2_FLT7	SDMMC1_D6	FMC_NWAIT	ADF1_SDI0	COMP3_OUT	EVENTOUT
	PC3	TIM20_CH2N	USART10_TX	-	LPTIM3_CH2	SDMMC1_D7	HRTIM2_EEV9	COMP8_OUT	EVENTOUT
	PC4	-	LPTIM1_CH1	-	-	FMC_D13/ FMC_AD13	HRTIM2_EEV1	-	EVENTOUT
	PC5	-	TIM1_BKIN2	-	-	FMC_D12/ FMC_AD12	HRTIM2_FLT1	TIM12_CH2	EVENTOUT
	PC6	UART9_TX	XSPI1_IO5	USART10_RTS	HRTIM1_CHF1	HRTIM2_EEV14	LPTIM5_OUT	COMP6_OUT	EVENTOUT
	PC7	UART9_RX	I2S3_MCK	-	HRTIM1_CHF2	HRTIM2_EEV13	-	COMP5_OUT	EVENTOUT
	PC8	I2C3_SCL	-	UCPD1_FRSTX2	HRTIM1_EEV15	FMC_NE2/ FMC_NCE	-	TIM10_CH1	EVENTOUT
	PC9	I2C3_SDA	SPI4_MISO	-	HRTIM1_EEV16	FMC_NE4	-	-	EVENTOUT
	PC10	UART4_TX	SPI4_RDY	TIM1_BKIN	HRTIM2_FLT8	FMC_NE1/ FMC_NCE	UCPD1_FRSTX1	COMP8_OUT	EVENTOUT
	PC11	UART4_RX	UCPD1_FRSTX2	TIM1_ETR	HRTIM2_EEV4	XSPI1_IO7	-	TIM12_CH1	EVENTOUT
	PC12	SPI6_SCK	-	TIM8_CH3N	FMC_A18	HRTIM2_EEV15	-	TIM13_CH1	EVENTOUT
	PC13	UART4_TX	FDCAN1_RX	-	HRTIM1_EEV14	-	HRTIM2_EEV4	-	EVENTOUT
	PC14	UART4_RX	UART5_RX	-	HRTIM1_FLT7	-	HRTIM2_EEV2	-	EVENTOUT
	PC15	UART4_TX	UART5_TX	-	HRTIM1_FLT8	HRTIM2_FLT8	-	-	EVENTOUT
Port D	PD0	UART4_RX	FDCAN1_RX	-	I3C1_SCL	FMC_A25	-	TIM8_CH4N	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ADF1 / FDCAN3 / I2C3 / LPUART1 / SPI6 / TIM3/20 / UART4/8/9 / XSPI1	FDCAN1 / I2C1 / LPTIM1/4 / SPI2S3 / SPI4 / TIM1/15/20 / UART5 / UCPD1 / USART10 / XSPI1	HRTIM2 / HSP1 / LPTIM3/4 / SDMMC1 / SPI2S1 / TIM1/2/4/8 / UART7 / UCPD1 / USART6/10 / XSPI1	FMC(NORmux) / FMC(NOR_RAM) / HRTIM1/2 / I2C2 / I3C1 / LPTIM3/4/5 / OTG_FS / SDMMC1 / SPI2S1 / TIM1/9 / USART10	FMC(NAND16) / FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / HRTIM1/2 / SDMMC1 / XSPI1	ADF1 / COMP1/4/6/7 / FDCAN1/2 / FMC(NORmux) / FMC(NOR_RAM) / HRTIM2 / HSP1 / LPTIM4/5 / SDMMC1 / TIM12/15 / UART7 / UCPD1	ADF1 / COMP2/3/5/6/8 / CRS / SDMMC1 / TIM2/8/10/12/13/15/20 / UART5/7	EVENTOUT
Port D	PD1	UART4_TX	FDCAN1_TX	TIM8_CH4	I3C1_SDA	-	-	TIM8_BKIN2	EVENTOUT
	PD2	TIM20_ETR	UART5_RX	-	HRTIM1_EEV12	-	LPTIM5_OUT	-	EVENTOUT
	PD3	-	UART5_TX	TIM2_CH4	HRTIM1_EEV3	-	-	-	EVENTOUT
	PD4	XSPI1_IO3	SPI4_NSS	-	HRTIM1_FLT3	-	HRTIM2_CHC1	-	EVENTOUT
	PD5	XSPI1_IO2	TIM1_BKIN	TIM1_BKIN2	HRTIM1_EEV10	FMC_NWE	LPTIM5_ETR	-	EVENTOUT
	PD6	XSPI1_IO1	SPI3_MISO/ I2S3_SDI	TIM2_CH1	HRTIM1_FLT5	-	LPTIM5_IN1	-	EVENTOUT
	PD7	XSPI1_IO0	FDCAN1_RX	TIM2_CH3	TIM9_CH1	-	-	-	EVENTOUT
	PD8	-	TIM20_ETR	-	-	FMC_D5/ FMC_AD5	-	CRS_SYNC	EVENTOUT
	PD9	-	TIM20_CH3N	-	TIM9_CH2	FMC_D6/ FMC_AD6	-	-	EVENTOUT
	PD10	-	TIM20_CH3	-	HRTIM1_EEV9	FMC_D7/ FMC_AD7	-	-	EVENTOUT
	PD11	UART4_RX	-	USART10_TX	HRTIM1_CHE1	FMC_A16/ FMC_CLE	ADF1_CCK0	UART7_RX	EVENTOUT
	PD12	UART4_TX	LPTIM1_IN1	USART10_RX	HRTIM1_CHE2	FMC_A17/ FMC_ALE	ADF1_CCK1	UART7_TX	EVENTOUT
	PD13	-	SPI3_RDY	XSPI1_IO6	HRTIM1_FLT1	HRTIM2_FLT1	-	-	EVENTOUT
	PD14	UART8_CTS	-	-	-	FMC_SDCKE1	HRTIM2_EEV6	-	EVENTOUT
	PD15	UART8_RTS	TIM1_BKIN	-	HRTIM1_FLT4	FMC_SDNE1	HRTIM2_EEV7	-	EVENTOUT
Port E	PE0	TIM20_CH4N	TIM20_ETR	-	HRTIM1_FLT2	-	-	-	EVENTOUT
	PE1	UART8_TX	LPTIM1_IN2	-	-	FMC_SDCLK	-	-	EVENTOUT
	PE2	UART8_TX	TIM20_CH1	HRTIM2_FLT5	TIM1_CH3	FMC_A23	LPTIM4_ETR	SDMMC1_CK	EVENTOUT
	PE3	TIM20_CH2	I2C1_SDA	USART6_CTS/ USART6_NSS	TIM1_CH1	FMC_A19	LPTIM4_OUT	SDMMC1_D0	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ADF1 / FDCAN3 / I2C3 / LPUART1 / SPI6 / TIM3/20 / UART4/8/9 / XSPI1	FDCAN1 / I2C1 / LPTIM1/4 / SPI2S3 / SPI4 / TIM1/15/20 / UART5 / UCPD1 / USART10 / XSPI1	HRTIM2 / HSP1 / LPTIM3/4 / SDMMC1 / SPI2S1 / TIM1/2/4/8 / UART7 / UCPD1 / USART6/10 / XSPI1	FMC(NORmux) / FMC(NOR_RAM) / HRTIM1/2 / I2C2 / I3C1 / LPTIM3/4/5 / OTG_FS / SDMMC1 / SPI2S1 / TIM1/9 / USART10	FMC(NAND16) / FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / HRTIM1/2 / SDMMC1 / XSPI1	ADF1 / COMP1/4/6/7 / FDCAN1/2 / FMC(NORmux) / FMC(NOR_RAM) / HRTIM2 / HSP1 / LPTIM4/5 / SDMMC1 / TIM12/15 / UART7 / UCPD1	ADF1 / COMP2/3/5/6/8 / CRS / SDMMC1 / TIM2/8/10/12/13/15/20 / UART5/7	EVENTOUT
Port E	PE4	TIM20_CH1N	I2C1_SMBA	HSP1_SNP2	I2C2_SMBA	FMC_A20	-	SDMMC1_D1	EVENTOUT
	PE5	-	TIM20_CH2N	HSP1_SNP3	LPTIM4_IN1	FMC_A21	HRTIM2_FLT7	SDMMC1_D2	EVENTOUT
	PE6	I2C3_SMBA	I2C1_SCL	USART6_RTS	-	FMC_A22	-	SDMMC1_D3	EVENTOUT
	PE7	-	-	HRTIM2_FLT7	HRTIM1_EEV4	FMC_SDCKE0	-	-	EVENTOUT
	PE8	-	FDCAN1_RX	HRTIM2_FLT8	HRTIM1_EEV10	FMC_SDNE0	-	-	EVENTOUT
	PE9	-	FDCAN1_TX	-	HRTIM1_FLT3	FMC_A2	-	-	EVENTOUT
	PE10	-	-	-	HRTIM1_FLT7	FMC_NRAS	-	-	EVENTOUT
	PE11	-	-	-	HRTIM1_FLT8	-	FDCAN2_TX	-	EVENTOUT
	PE12	-	-	-	LPTIM3_ETR	FMC_D8/ FMC_AD8	FDCAN2_RX	-	EVENTOUT
	PE13	TIM20_BKIN2	UART5_RTS	-	HRTIM1_FLT6	FMC_D0/ FMC_AD0	-	-	EVENTOUT
	PE14	-	UART5_CTS	-	HRTIM1_EEV3	FMC_D1/ FMC_AD1	-	-	EVENTOUT
	PE15	-	SPI4_SCK	-	HRTIM1_FLT2	FMC_D2/ FMC_AD2	-	-	EVENTOUT
Port F	PF0	-	-	-	HRTIM1_EEV4	FMC_A4	-	-	EVENTOUT
	PF1	-	-	-	HRTIM1_EEV8	FMC_SDNWE	-	-	EVENTOUT
	PF2	TIM20_CH3	USART10_RX	TIM2_CH4	LPTIM3_CH1	FMC_D14/ FMC_AD14	-	-	EVENTOUT
	PF3	TIM20_CH4	-	-	-	FMC_A3	-	-	EVENTOUT
	PF4	TIM20_CH1N	-	-	LPTIM3_CH2	FMC_D11/ FMC_AD11	COMP1_OUT	TIM10_CH1	EVENTOUT
	PF5	TIM20_CH2N	-	-	-	FMC_NCAS	HRTIM2_SCOUT	-	EVENTOUT
	PF6	-	-	TIM4_CH4	-	-	UART7_RX	-	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ADF1 / FDCAN3 / I2C3 / LPUART1 / SPI6 / TIM3/20 / UART4/8/9 / XSPI1	FDCAN1 / I2C1 / LPTIM1/4 / SPI2S3 / SPI4 / TIM1/15/20 / UART5 / UCPD1 / USART10 / XSPI1	HRTIM2 / HSP1 / LPTIM3/4 / SDMMC1 / SPI2S1 / TIM1/2/4/8 / UART7 / UCPD1 / USART6/10 / XSPI1	FMC(NORmux) / FMC(NOR_RAM) / HRTIM1/2 / I2C2 / I3C1 / LPTIM3/4/5 / OTG_FS / SDMMC1 / SPI2S1 / TIM1/9 / USART10	FMC(NAND16) / FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / HRTIM1/2 / SDMMC1 / XSPI1	ADF1 / COMP1/4/6/7 / FDCAN1/2 / FMC(NORmux) / FMC(NOR_RAM) / HRTIM2 / HSP1 / LPTIM4/5 / SDMMC1 / TIM12/15 / UART7 / UCPD1	ADF1 / COMP2/3/5/6/8 / CRS / SDMMC1 / TIM2/8/10/12/13/15/20 / UART5/7	EVENTOUT
Port F	PF7	TIM20_BKIN	-	-	-	FMC_A10	-	-	EVENTOUT
	PF8	TIM20_BKIN2	-	-	-	-	-	-	EVENTOUT
	PF9	UART4_RX	TIM20_BKIN	-	LPTIM3_IN1	FMC_D9/ FMC_AD9	HRTIM2_SCIN	SDMMC1_CMD	EVENTOUT
	PF10	TIM20_BKIN2	USART10_TX	-	LPTIM3_IN2	FMC_D10/ FMC_AD10	-	-	EVENTOUT
	PF11	-	TIM20_ETR	-	HRTIM1_EEV12	FMC_A1	-	-	EVENTOUT
	PF12	-	TIM20_CH1	-	HRTIM1_EEV13	FMC_A6	-	-	EVENTOUT
	PF13	-	TIM20_CH2	-	HRTIM1_EEV15	FMC_A7	HRTIM2_EEV1	-	EVENTOUT
	PF14	-	TIM20_CH3N	-	HRTIM1_EEV14	FMC_A8	-	-	EVENTOUT
	PF15	-	TIM20_CH4	-	HRTIM1_EEV16	FMC_A9	HRTIM2_SCOUT	-	EVENTOUT
Port G	PG0	FDCAN3_RX	TIM20_CH1N	-	-	-	-	-	EVENTOUT
	PG1	FDCAN3_TX	TIM20_CH2N	-	HRTIM1_FLT5	HRTIM2_FLT1	-	-	EVENTOUT
	PG2	UART4_RX	FDCAN1_RX	-	-	-	-	-	EVENTOUT
	PG3	UART4_TX	LPTIM1_CH1	-	-	-	FDCAN1_TX	-	EVENTOUT
	PG4	TIM20_BKIN2	-	-	-	-	HRTIM2_FLT5	-	EVENTOUT
	PG5	LPUART1_CTS	TIM20_ETR	-	-	-	HRTIM2_FLT6	-	EVENTOUT
	PG6	LPUART1_RTS	TIM20_BKIN	-	-	-	UCPD1_FRSTX1	COMP6_OUT	EVENTOUT
	PG7	LPUART1_TX	-	-	-	-	UCPD1_FRSTX2	COMP8_OUT	EVENTOUT
	PG8	LPUART1_RX	-	-	-	-	-	-	EVENTOUT
	PG9	-	-	-	-	-	HRTIM2_FLT7	TIM15_CH1N	EVENTOUT
	PG10	LPUART1_TX	FDCAN1_TX	TIM8_CH2	TIM9_CH2	-	-	-	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ADF1 / FDCAN3 / I2C3 / LPUART1 / SPI6 / TIM3/20 / UART4/8/9 / XSPI1	FDCAN1 / I2C1 / LPTIM1/4 / SPI2S3 / SPI4 / TIM1/15/20 / UART5 / UCPD1 / USART10 / XSPI1	HRTIM2 / HSP1 / LPTIM3/4 / SDMMC1 / SPI2S1 / TIM1/2/4/8 / UART7 / UCPD1 / USART6/10 / XSPI1	FMC(NORmux) / FMC(NOR_RAM) / HRTIM1/2 / I2C2 / I3C1 / LPTIM3/4/5 / OTG_FS / SDMMC1 / SPI2S1 / TIM1/9 / USART10	FMC(NAND16) / FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / HRTIM1/2 / SDMMC1 / XSPI1	ADF1 / COMP1/4/6/7 / FDCAN1/2 / FMC(NORmux) / FMC(NOR_RAM) / HRTIM2 / HSP1 / LPTIM4/5 / SDMMC1 / TIM12/15 / UART7 / UCPD1	ADF1 / COMP2/3/5/6/8 / CRS / SDMMC1 / TIM2/8/10/12/13/15/20 / UART5/7	EVENTOUT
Port G	PG11	TIM20_CH1	LPTIM1_IN2	TIM8_CH1	-	-	TIM12_CH2	ADF1_CCK0	EVENTOUT
	PG12	LPUART1_RX	LPTIM1_IN1	TIM8_CH3N	-	FMC_A0	-	ADF1_CCK1	EVENTOUT
	PG13	-	LPTIM1_CH1	-	-	FMC_A11	COMP6_OUT	TIM12_CH2	EVENTOUT
	PG14	TIM20_CH1N	LPTIM1_CH2	-	HRTIM1_FLT4	FMC_A12	HRTIM2_FLT1	ADF1_SDI0	EVENTOUT
	PG15	-	SPI4_RDY	-	-	FMC_A13	COMP1_OUT	-	EVENTOUT
Port H	PH0	XSPI1_DQS0	-	-	-	-	HRTIM2_FLT1	TIM13_CH1	EVENTOUT
	PH1	XSPI1_NCS2	-	-	-	HRTIM1_FLT1	-	TIM10_CH1	EVENTOUT
	PH2	-	-	-	-	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	EVENTOUT
	PH4	-	-	-	-	FMC_A14/ FMC_BA0	-	-	EVENTOUT
	PH5	-	-	-	-	FMC_A15/ FMC_BA1	-	-	EVENTOUT
	PH6	-	LPTIM1_ETR	-	-	HRTIM2_FLT2	FDCAN2_RX	-	EVENTOUT
	PH7	-	-	-	-	HRTIM2_FLT3	FDCAN2_TX	-	EVENTOUT
	PH8	-	-	-	HRTIM1_FLT6	-	-	TIM10_CH1	EVENTOUT
	PH9	I2C3_SMBA	-	-	HRTIM1_EEV4	-	-	-	EVENTOUT
	PH10	-	-	HSP1_SNP0	HRTIM1_EEV6	HRTIM2_FLT5	-	TIM12_CH1	EVENTOUT
	PH11	-	-	HSP1_SNP1	-	-	-	TIM13_CH1	EVENTOUT
	PH12	-	-	HSP1_SNP2	TIM9_CH1	-	-	-	EVENTOUT
	PH13	UART4_TX	FDCAN1_TX	HSP1_SNP3	-	-	-	-	EVENTOUT
	PH14	UART4_RX	FDCAN1_RX	HSP1_SNP4	-	-	-	-	EVENTOUT
	PH15	SPI6_RDY	-	HSP1_SNP5	-	-	-	-	EVENTOUT

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		ADF1 / FDCAN3 / I2C3 / LPUART1 / SPI6 / TIM3/20 / UART4/8/9 / XSPI1	FDCAN1 / I2C1 / LPTIM1/4 / SPI2S3 / SPI4 / TIM1/15/20 / UART5 / UCPD1 / USART10 / XSPI1	HRTIM2 / HSP1 / LPTIM3/4 / SDMMC1 / SPI2S1 / TIM1/2/4/8 / UART7 / UCPD1 / USART6/10 / XSPI1	FMC(NORmux) / FMC(NOR_RAM) / HRTIM1/2 / I2C2 / I3C1 / LPTIM3/4/5 / OTG_FS / SDMMC1 / SPI2S1 / TIM1/9 / USART10	FMC(NAND16) / FMC(NORmux) / FMC(NOR_RAM) / FMC(SDRAM_16bit) / HRTIM1/2 / SDMMC1 / XSPI1	ADF1 / COMP1/4/6/7 / FDCAN1/2 / FMC(NORmux) / FMC(NOR_RAM) / HRTIM2 / HSP1 / LPTIM4/5 / SDMMC1 / TIM12/15 / UART7 / UCPD1	ADF1 / COMP2/3/5/6/8 / CRS / SDMMC1 / TIM2/8/10/12/13/15/20 / UART5/7	EVENTOUT
Port I	PI0	-	-	-	-	-	-	-	EVENTOUT
	PI1	-	-	-	-	-	-	-	EVENTOUT
	PI2	UART8_RX	TIM20_CH4	TIM8_BKIN2	USART10_CK	HRTIM1_CHD1	ADF1_SDI0	COMP5_OUT	EVENTOUT
	PI3	-	FDCAN1_RX	-	-	-	-	-	EVENTOUT
	PI4	-	-	-	-	-	-	-	EVENTOUT
	PI8	-	-	-	-	-	HRTIM2_EEV7	-	EVENTOUT

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100 % of the devices with an junction temperature at T_J = 25 °C and T_J = T_{Jmax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_J = 25°C, V_{DD} = V_{DDA} = 3.3 V (for the 2.7 ≤ V_{DD} ≤ 3.6 V range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range and supply voltage range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 20.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 21.

Figure 20. Pin loading conditions

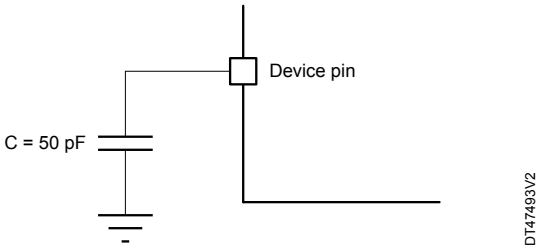
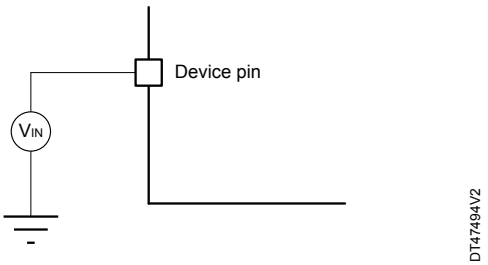


Figure 21. Pin input voltage

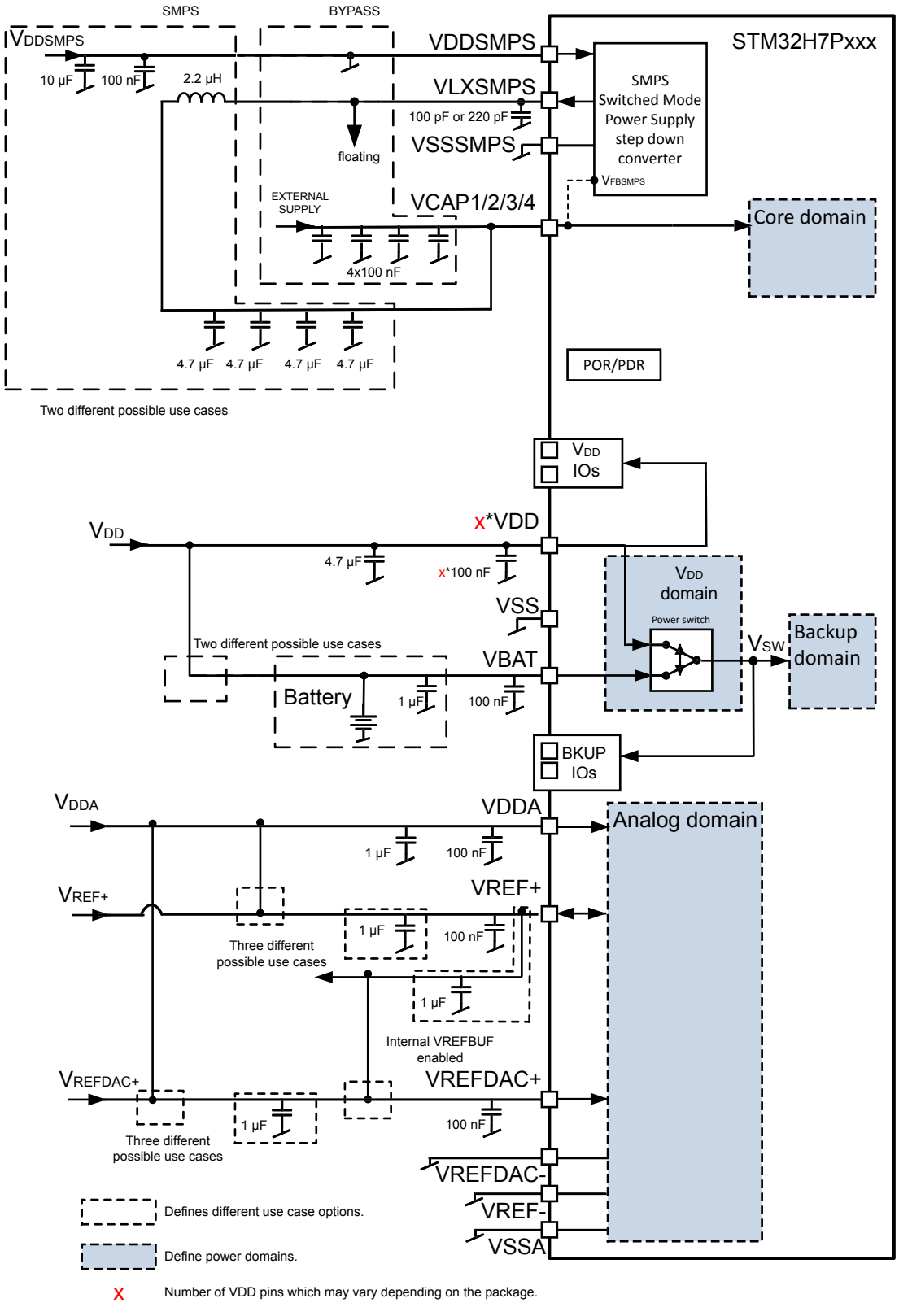


5.1.6 Power supply scheme

Each power supply pair (such as V_{DD}/V_{SS} or V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown in the following figures. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the proper functionality of the device.

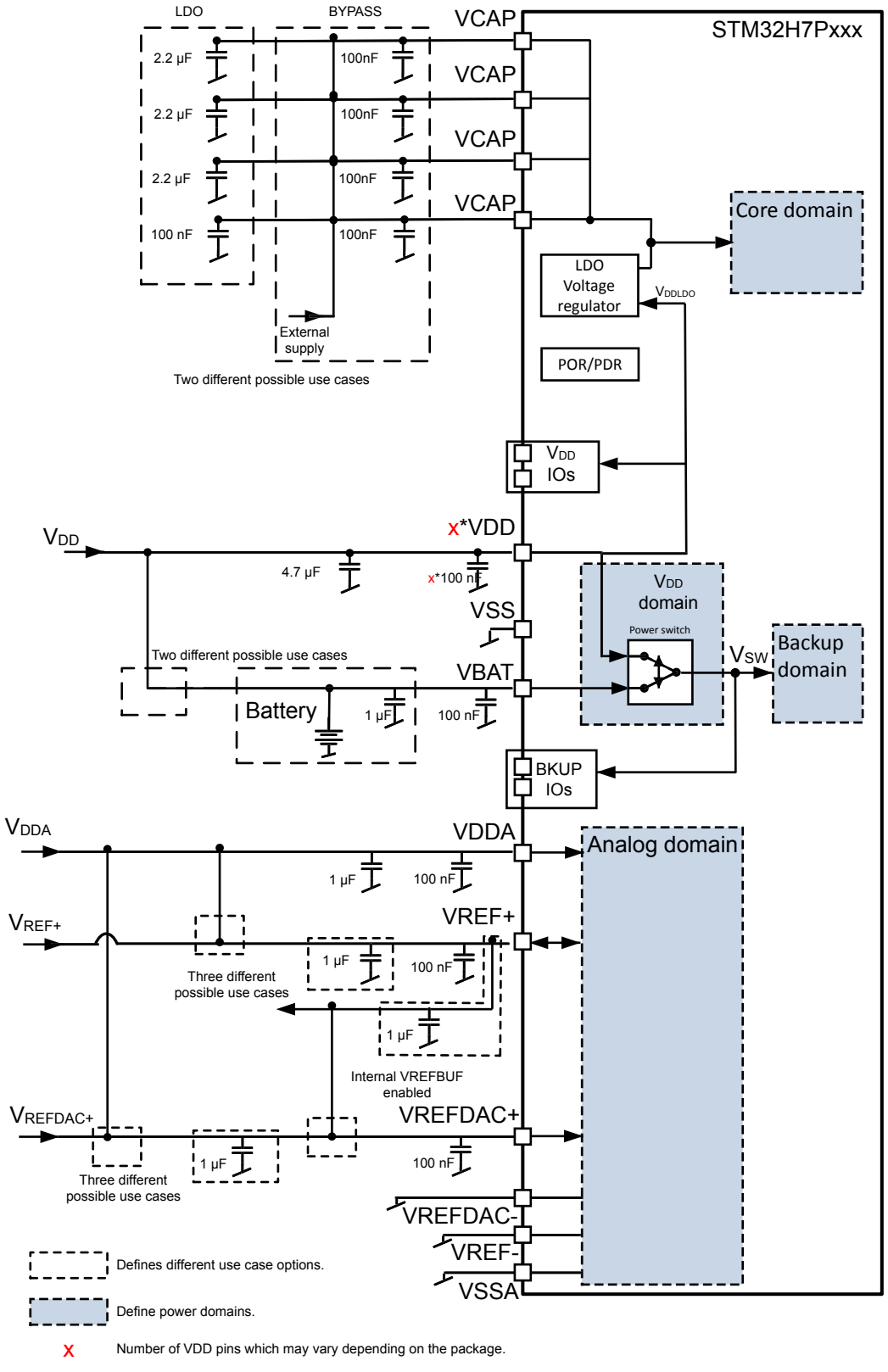
Prerelease product(s)

Figure 22. **STM32H7Pxxx power supply scheme (with SMPS)**



Prerelease product(s)

Figure 23. **STM32H7Pxxx power supply scheme (with LDO)**



Depending on the selected part number, the core domain is supplied by either an integrated low-dropout voltage regulator (LDO) (see Figure 23), or a switched-mode power supply (SMPS) (see Figure 22).

Prerelease product(s)

The SMPS output on V_{LXSMPS} connects to the core domain supply pins (VCAP) through a filter composed of a 2.2 µH series inductor and a ~20 µF parallel capacitor. Use four 4.7 µF capacitors, placed as close as possible to each VCAP pin.

The LDO output connects internally to the core domain. Decoupling capacitors—three 2.2 µF and one 100 nF—must be placed as close as possible to the VCAP pins.

The integrated voltage regulator (LDO or SMPS) can be bypassed and replaced with an external supply connected to the VCAP pins. In this case, use four 100 nF decoupling capacitors, placed as close as possible to each VCAP pin.

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 11. Voltage characteristics, Table 12. Current characteristics, and Table 13. Thermal characteristics may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 11. Voltage characteristics

All main power (VDD, VDDSMPS, VDDA, VREF+, and VREFDAC+) and ground (VSS, VSSA, VREF+, and VREFDAC+) pins must always be connected to the external power supply, in the permitted range.

Symbol	Ratings	Min	Max	Unit
V_{DDx} - V_{SS}	External main supply voltage (including V_{DD}, V_{DDSMPS}, V_{DDA}, $V_{REFDAC+}$, and V_{REF+})	-0.3	4.0	V
V_{CAP}	External V_{CORE} supply voltage (bypass mode operation)	V_{SS} - 0.3	min (V_{DD}, V_{DDA}, 1.40 V)	V
V_{IN}(1)	Input voltage on FT_xxx pins except FT_c pins	V_{SS} -0.3	min (min(V_{DD}, V_{DDA}) + 4.0, 6.0 V) (2)(3)	V
	Input voltage on TT_xx pins	V_{SS} -0.3	4.0	V
	Input voltage on BOOT0 pin	V_{SS} -0.3	min (min(V_{DD}, V_{DDA}) + 4.0, 6.0 V) (2)(3)	
	Input voltage on FT_c pins	V_{SS} -0.3	5.5	
	Input voltage on FT_fb pins	V_{SS} -0.3	5.5	
	Input voltage on COMP inputs	V_{SSA} -0.3	V_{DDA} + 0.3	
	Input voltage on any other pins	V_{SS}-0.3	4.0	
V_{AIN}	Input voltage on ADC inputs	V_{SSA}-0.3	min (V_{DDA}, V_{REF+}) + 0.3V	
V_{REF+}-V_{DDA}	Allowed voltage difference for V_{REF+} > V_{DDA} or $V_{REFDAC+,}$ > V_{DDA}	-	0.4	
$\|\Delta V_{DDx}\|$	Variations between different V_{DDX} power pins of the same domain	-	50.0	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins	-	50.0	

1. *V_{IN} maximum must always be respected. Refer to Table 12. Current characteristics for the maximum allowed injected current values.*
2. *This formula must be applied on power supplies related to the I/O structure described by the pin definition table.*
3. *To sustain a voltage higher than 4 V the internal pull-up/pull-down resistors must be disabled. Internal analog switch must also be disabled.*

Prerelease product(s)

Table 12. Current characteristics

Symbol	Ratings	Max	Unit
ΣIV_{DD}	Total current into sum of all V_{DD} power lines (source)(1)	620.0	mA
ΣIV_{SS}	Total current out of sum of all V_{SS} ground lines (sink)(1)	620.0	
IV_{DD}	Maximum current into each V_{DD} power pin (source)(1)	100.0	
IV_{SS}	Maximum current out of each V_{SS} ground pin (sink)(1)	100.0	
I_{IO}	Output current sunk by any I/O and control pin	20.0	
$\Sigma I_{(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	140.0	
	Total output current sourced by sum of all I/Os and control pins(2)	140.0	
$I_{INJ(PIN)}$(3)(4)	Injected current on FT_xx, TT_xx, RST pins	-5/0	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/Os and control pins)(5)	±25	

1. *All main power (V_{DD}, V_{DDSMPS}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.*
2. *This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.*
3. *Positive injection (when $V_{IN} > V_{DD}$) is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.*
4. *A negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to Table 11. Voltage characteristics for the minimum allowed input voltage values.*
5. *When several inputs are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the negative injected currents (instantaneous values).*

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	140(1)	°C

1. *In VOS2 voltage range. Refer to Table 14. General operating conditions for the maximum junction temperature for each voltage range.*

5.3 Operating conditions

5.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{DD}	Standard operating voltage	-	1.62(1)	-	3.6	V
V_{DDSMPS}	Supply voltage for the internal SMPS step-down converter	-	V_{DD}			V
V_{DDA}	Analog supply voltage	COMP used	2.50	-	3.6	V
		DAC used	1.62	-		
		ADC used	1.62	-		
		VREFBUF used	2.50	-		
		ADC, DAC, COMP, VREFBUF not used	0	-		

Prerelease product(s)

Symbol	Parameter	Operating conditions	Min	Typ	Max	Unit
V_{BAT}	Backup domain operating voltage	-	1.2	-	3.6	V
VIN	I/O Input voltage	All I/O except FT_c and TT_xx	−0.3	-	MIN(MIN(V_{DD}, V_{DDA}) + 3.6 V, 5.5 V)(2)(3)	V
		FT_c I/O	−0.3	-	5.0	
		TT_xx I/O	−0.3	-	V_{DD} + 0.3	
V_{CORE}	Internal regulator ON (LDO or SMPS)	VOS0(4)	1.25	1.30	1.35	V
		VOS1	1.15	1.20	1.25	
		VOS2	1.05	1.10	1.15	
		SVOSH	-	1.00	-	
		SVOSL	-	0.74	-	
	Bypass: external V_{CORE} voltage must be supplied from external regulator on VCAP pins	VOS0(4)	1.32	1.35	1.40	
		VOS1	1.17	1.20	1.26	
		VOS2	1.07	1.10	1.15	
		SVOSH	1.00	-	1.15	
f_{ACLK}, f_{HCLK}	AXI, AHB, APB2 clock frequency	VOS0(4)	-	-	275	MHz
		VOS1	-	-	200	
		VOS2	-	-	150	
f_{PCLKx} (x = 1, 2, 3)	APB1, APB4 clock frequency	VOS0(4)	-	-	137.5	MHz
		VOS1	-	-	100	
		VOS2	-	-	75	
T_A	Ambient temperature	-	–40	-	125(5)	°C
T_J	Junction temperature	VOS0	-40	-	105	°C
		VOS1	-40	-	125	
		VOS2	–40	-	140	

1. *When RESET is released, functionality is guaranteed down to the maximum PDR voltage.*
2. *Apply this formula to power supplies associated with the IO structure described in the pin definition table.*
3. *For operation with a voltage higher than Min (V_{DD}, V_{DDA}) + 0.3 V, disable the internal pull-up and pull-down resistors.*
4. *In VOS0 mode the maximum T_J is 105°C.*
5. *Absolute maximum. The maximum ambient temperature can be calculated from the power dissipation and the package thermal characteristics. See Table 13. Thermal characteristics. Ensure that T_J does not exceed the maximum value for the selected VOS.*

Table 15. Maximum allowed clock frequencies

Symbol(1)(2)	Parameter	VOS0	VOS1	VOS2	Unit
f_{CPU_MAX}	CPU (ECC off)	520	435	350	MHz
	CPU (ECC on)	465	370	300	
f_{ACLK}	AXI	$f_{CPU_MAX}/2$			
f_{HCLK}	AHB	$f_{CPU_MAX}/2$			
f_{PCLK2}	APB2	$f_{CPU_MAX}/2$			
f_{PCLK}	APB1, APB4	$f_{CPU_MAX}/4$			
f_{JTCK}	JTAG/SWD	40			

Prerelease product(s)

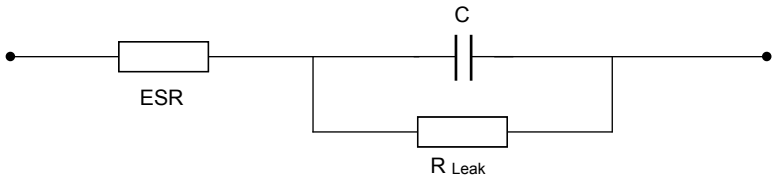
Symbol[1][2]	Parameter	VOS0	VOS1	VOS2	Unit
$f_{npu_ker_ck}$	NPU	f_{CPU_MAX}			MHz
$f_{hsp_ker_ck}$	HSP	$f_{CPU_MAX}/2$			
$f_{fmc_ker_ck}$	FMC	$f_{CPU_MAX}/2$			
$f_{xspi_ker_ck}$	XSPI1	$f_{CPU_MAX}/2$			
$f_{sdmmc_ker_ck}$	SDMMC1	200			
$f_{adf_ker_ck}$	ADF	$f_{CPU_MAX}/2$			
$f_{fdcan_ker_ck}$	FDCAN	125			
$f_{i2c_ker_ck}$	I2C1-3	$f_{CPU_MAX}/4$			
$f_{i3c_ker_ck}$	I3C1	$f_{CPU_MAX}/4$			
$f_{lptim_ker_ck}$	LPTIM1-5	$f_{CPU_MAX}/4$			
$f_{tim_ker_ck}$	TIM2-7, TIM10-14	f_{CPU_MAX}			
$f_{tim_ker_ck}$	TIM1, TIM8, TIM9, TIM15-17, TIM20	f_{CPU_MAX}			
$f_{tim_ker_ck}$	HRTIM1-2	f_{CPU_MAX}			
$f_{hsi48_ker_ck}$	RNG	48			
$f_{spi_ker_ck}$	SPI1-6	$f_{CPU_MAX}/2$			
$f_{lpuart_ker_ck}$	LPUART1	$f_{CPU_MAX}/4$			
$f_{usart_ker_ck}$	USART1/2/3/6/10	$f_{CPU_MAX}/4$			
$f_{uart_ker_ck}$	UART4/5/7/8/9	$f_{CPU_MAX}/4$			
$f_{usbfs_ker_clk}$	OTG-FS	48			
$f_{ucpd_ker_clk}$	UCPD	25			
$f_{adc_ker_ck}$	ADC1/2/3/4	80			
$f_{dac_ker_clk}$	DAC1/2	f_{CPU_MAX}			
$f_{rtc_ker_ck}$	RTC	1			
$f_{rtc_ker_ck}$	TAMPER	4			

1. *Specified by design. Not tested in production.*
2. *The maximum kernel clock frequency is limited by the maximum peripheral clock frequency. Refer to the electrical characteristics of each peripheral.*

5.3.2 VCAP external capacitor

The stabilization for the embedded LDO regulator is achieved by connecting an external capacitor C_{EXT} (whose value is specified in Table 16. Characteristics of LDO regulator external components) to the VCAPx (one or two pins, depending upon the package). Three external capacitors must be connected to VCAP pins.

Figure 24. External capacitor C_{EXT} equivalent circuit



Prerelease product(s)

Table 16. Characteristics of LDO regulator external components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{EXT}	Capacitance of external capacitor on each VCAP pin	LDO mode	-	2.2(1)	-	µF
	Capacitance of external capacitor on each VCAP pin	Bypass mode	-	100	-	nF
	ESR of external capacitor	2.4 MHz	-	-	100	mΩ

1. *Tolerance: -20% to +20% under all conditions.*

5.3.3 SMPS step-down converter

The devices embed a high power efficiency SMPS step-down converter requiring external components.

Table 17. Characteristics of SMPS step-down converter external components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{in}	Capacitance of external capacitor on VDDSMPS	-	-	10(1)	-	µF
	ESR of external capacitor	2.4 MHz	-	-	10	mΩ
C_{filt}	Capacitance of external capacitor on VLXSMPS pin	-	-	220	-	pF
C_{OUT}	Capacitance of external capacitor on each VCAP pin	-	-	4.7(1)	-	µF
	ESR of external capacitor	2.4 MHz	-	-	20	mΩ
L	Inductance of external Inductor on VLXSMPS pin	-	-	2.2(1)	-	µH
	Serial DC resistance	-	-	-	150	mΩ
I_{SAT}	DC current at which the inductance drops 30% from the value without current	-	1	-	-	A
I_{RMS}	Average current for which the temperature of the inductor is raised 40 °C by the DC current	-	1	-	-	A

1. *Tolerance: -50% to +30% under all conditions.*

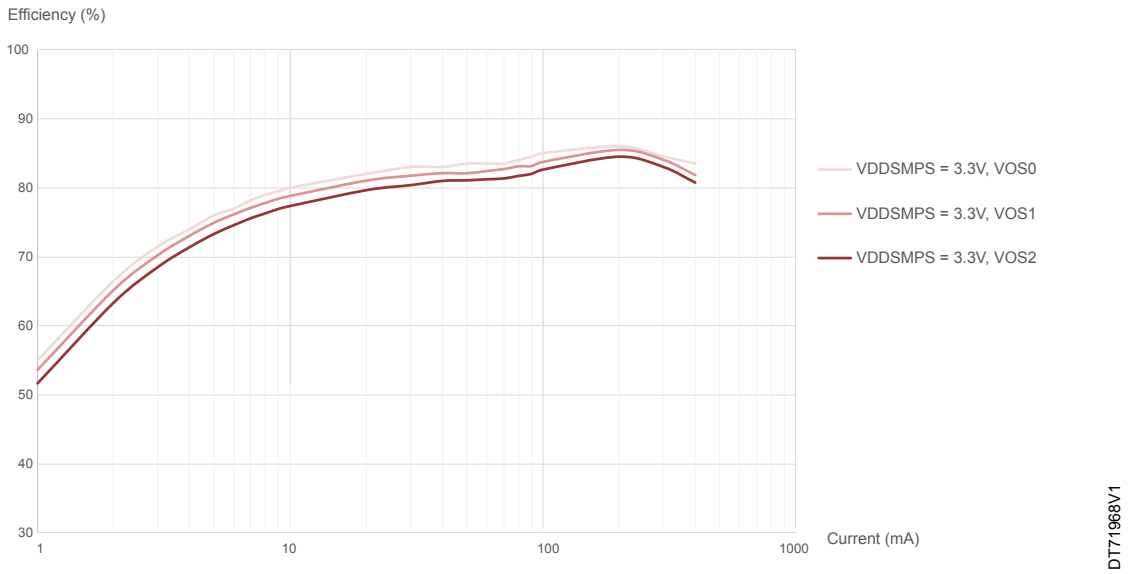
The SMPS current consumption can be determined using the following formula based on the maximum LDO current consumption provided in Section 5.3.7: Supply current characteristics:

$I_{DDSMPS} = I_{DDLDO} \times V_{CORE} / (V_{DD} \times \text{efficiency})$

I_{DDLDO} is the current in LDO configuration given in the following tables, V_{CORE} is the digital core supply (VCAP), and efficiency is defined in the following curves.

Prerelease product(s)

Figure 25. **SMPS efficiency versus load current in Run, Sleep, and Stop mode, T_J = 30°C**



Note: Stop mode is equivalent to VOS2 mode.

5.3.4 Operating conditions at power-up/down

Subject to general operating conditions for T_A.

Table 18. **Operating conditions at power-up/down (regulator ON)**

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	µs/V
	V_{DD} fall time rate	10		
t_{VDDA}	V_{DDA} rise time rate	0		
	V_{DDA} fall time rate	10		

5.3.5 Embedded reset and power control block characteristics

The parameters given in Table 19 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Section 5.3.1: General operating conditions.

Table 19. **Embedded reset and power control block characteristics**

Evaluated by characterization and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{RSTTEMPO}$(1)	Reset delay after POR released	V_{DD} rising	-	377	550	µs
$V_{POR/PDR}$	Power-on/power-down reset threshold (BOR_LEV = 0)	Rising edge	1.62	1.67	1.71	V
		Falling edge	1.58	1.62	1.68	
V_{BOR1}	Brown-out reset threshold 1 (BOR_LEV = 1)	Rising edge	2.04	2.10	2.15	V
		Falling edge	1.95	2.00	2.06	
V_{BOR2}	Brown-out reset threshold 2 (BOR_LEV = 2)	Rising edge	2.34	2.41	2.47	V
		Falling edge	2.25	2.31	2.37	
V_{BOR3}	Brown-out reset threshold 3 (BOR_LEV = 3)	Rising edge	2.63	2.70	2.78	V

Prerelease product(s)

Prerelease product(s)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOR3}	Brown-out reset threshold 3 (BOR_LEV = 3)	Falling edge	2.54	2.61	2.68	V
V_{PVD0}	Programmable voltage detector threshold 0	Rising edge	1.90	1.96	2.01	V
		Falling edge	1.81	1.86	1.91	
V_{PVD1}	Programmable voltage detector threshold 1	Rising edge	2.05	2.10	2.16	V
		Falling edge	1.96	2.01	2.06	
V_{PVD2}	Programmable voltage detector threshold 2	Rising edge	2.19	2.26	2.32	V
		Falling edge	2.10	2.15	2.21	
V_{PVD3}	Programmable voltage detector threshold 3	Rising edge	2.35	2.41	2.47	V
		Falling edge	2.25	2.31	2.37	
V_{PVD4}	Programmable voltage detector threshold 4	Rising edge	2.49	2.56	2.62	V
		Falling edge	2.39	2.45	2.51	
V_{PVD5}	Programmable voltage detector threshold 5	Rising edge	2.64	2.71	2.78	V
		Falling edge	2.55	2.61	2.68	
V_{PVD6}	Programmable voltage detector threshold 6	Rising edge	2.78	2.86	2.94	V
		Falling edge	2.69	2.76	2.83	
$V_{hyst_POR_PDR}$	Hysteresis for power-on/power-down reset	Hysteresis in Run mode	-	43	-	mV
$V_{hyst_BOR_PVD}$	Hysteresis voltage of BOR	Hysteresis in Run mode	-	100	-	mV
I_{DD_PVD}(1)	PVD consumption from V_{DD}	-	-	-	0.63	µA
$I_{DD_POR_PDR}$	POR and PDR consumption from V_{DD}	-	0.8	-	1.2	
V_{AVD0}	V_{DDA} voltage monitor 0 threshold	Rising edge	1.66	1.71	1.76	V
		Falling edge	1.56	1.61	1.66	
V_{AVD1}	V_{DDA} voltage monitor 1 threshold	Rising edge	2.06	2.12	2.19	
		Falling edge	1.96	2.02	2.08	
V_{AVD2}	V_{DDA} voltage monitor 2 threshold	Rising edge	2.42	2.50	2.58	
		Falling edge	2.35	2.42	2.49	
V_{AVD3}	V_{DDA} voltage monitor 3 threshold	Rising edge	2.74	2.83	2.91	
		Falling edge	2.64	2.72	2.80	
V_{hyst_AVD}	Hysteresis of V_{DDA} voltage detector	-	-	100.00	-	mV
I_{DD_AVD} (1)	Analog voltage detector consumption from V_{DD} (AVD)	-	-	-	0.25	µA
$I_{DD_AVD_A}$(1)	Analog voltage detector consumption from V_{DDA} (resistor bridge)	-	-	-	0.25	µA

1. *Specified by design. Not tested in production.*

5.3.6 Embedded reference voltage

The parameters given in Table 20 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 5.3.1.

Table 20. Embedded reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}(1)	Internal reference voltages	−40°C < T_J < 140°C	1.18	1.216	1.255	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{S_vrefint}$ (2)(3)	ADC sampling time when reading the internal reference voltage	-	4.3	-	-	µs
t_{S_vbat} (3)	V_{BAT} sampling time when reading the internal reference voltage	-	9	-	-	
$t_{start_vrefint}$ (3)	Start time of reference voltage buffer when ADC is enable	-	-	-	4.4	
I_{refbuf} (3)	Reference buffer consumption for ADC	V_{DD} = 3.3 V	9	13.5	23	µA
ΔV_{REFINT}(3)	Internal reference voltage spread over the temperature range	−40°C < T_J < 140°C	-	5	15	mV
T_{coeff}	Average temperature coefficient	Average temperature coefficient	-	20	70	ppm/°C
$V_{DDcoeff}$	Average voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	10	1370	ppm/V
V_{REFINT_DIV1} (3)	1/4 reference voltage	-	-	25	-	% V_{REFINT}
V_{REFINT_DIV2} (3)	1/2 reference voltage	-	-	50	-	
V_{REFINT_DIV3} (3)	3/4 reference voltage	-	-	75	-	

1. *V_{REFINT} does not take into account package and soldering effects.*
2. *The shortest sampling time for the application can be determined by multiple iterations.*
3. *Specified by design. Not tested in production.*

Table 21. Internal reference voltage calibration value

Symbol	Parameter	Memory address
V_{REFINT_CAL}	Raw data acquired at 30°C, V_{DDA} = 3.3 V	0x08FF F810 - 0x08FF F811

5.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The flash memory access time is adjusted with the minimum wait-state number, depending on the f_{HCLK} frequency (refer to the tables “FLASH recommended number of wait states and programming delay” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU frequency and the APB clock frequency is AHB frequency.

The parameters given in the following tables are derived from tests performed under supply voltage conditions summarized in Section 5.3.1, and, unless otherwise specified, at ambient temperature.

The maximum current consumption is given for LDO regulator ON.

Prerelease product(s)

Table 22. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 2-way instruction cache ON, PREFETCH ON

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Typ SMPS	Max(1)(2)				Unit
							T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 140°C	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled	VOS0	280	TBD	TBD	TBD	TBD	TBD	TBD	mA
				240	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS1	240	TBD	TBD	TBD	TBD	TBD	TBD	
				200	TBD	TBD	TBD	TBD	TBD	TBD	
				170	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS2	170	TBD	TBD	TBD	TBD	TBD	TBD	
				100	TBD	TBD	TBD	TBD	TBD	TBD	
		All peripherals enabled	VOS0	280	TBD	TBD	TBD	TBD	TBD	TBD	
				240	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS1	240	TBD	TBD	TBD	TBD	TBD	TBD	
				200	TBD	TBD	TBD	TBD	TBD	TBD	
				170	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS2	170	TBD	TBD	TBD	TBD	TBD	TBD	
				100	TBD	TBD	TBD	TBD	TBD	TBD	

1. *The maximum values are given for LDO regulator ON. Refer to Section 5.3.3 for the SMPS maximum current consumption.*
2. *Evaluated by characterization. Not tested in production.*

Table 23. Typical and maximum current consumption in Run mode, code with data processing running from flash memory, 1-way instruction cache ON, PREFETCH ON

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Typ SMPS	Max(1)(2)				Unit
							T_J = 25°C	T_J = 85°C	T_J = 105°C	T_J = 140°C	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled	VOS0	280	TBD	TBD	TBD	TBD	TBD	TBD	mA
				240	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS1	240	TBD	TBD	TBD	TBD	TBD	TBD	
				200	TBD	TBD	TBD	TBD	TBD	TBD	
				170	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS2	170	TBD	TBD	TBD	TBD	TBD	TBD	
				100	TBD	TBD	TBD	TBD	TBD	TBD	

1. *The maximum values are given for LDO regulator ON. Refer to Section 5.3.3 for the SMPS maximum current consumption.*
2. *Evaluated by characterization. Not tested in production.*

Table 24. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 1-way

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Typ SMPS	Max(1)(2)				Unit
							T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 140 °C	
I_{DD} (Run)	Supply current in Run mode	All peripherals disabled	VOS0	280	TBD	TBD	TBD	TBD	TBD	TBD	mA
				240	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS1	240	TBD	TBD	TBD	TBD	TBD	TBD	

Prerelease product(s)

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Typ SMPS	Max(1)(2)				Unit
							T_J = 25 °C	T_J = 85 °C	T_J = 105 °C	T_J = 140 °C	
I_{DD} (Run)	Supply current in Run mode	All peripherals disabled	VOS1	200	TBD	TBD	TBD	TBD	TBD	TBD	mA
				170	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS2	170	TBD	TBD	TBD	TBD	TBD	TBD	
				100	TBD	TBD	TBD	TBD	TBD	TBD	

1. *The maximum values are given for LDO regulator ON. Refer to Section 5.3.3 for the SMPS maximum current consumption.*
2. *Evaluated by characterization. Not tested in production.*

Table 25. Typical and maximum current consumption in Run mode, code with data processing running from SRAM with cache 2-way

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Typ SMPS	Max(1)(2)				Unit
							T_J = 25° C	T_J = 85° C	T_J = 105 °C	T_J = 140° C	
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled	VOS0	280	TBD	TBD	TBD	TBD	TBD	TBD	mA
				240	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS1	240	TBD	TBD	TBD	TBD	TBD	TBD	
				200	TBD	TBD	TBD	TBD	TBD	TBD	
				170	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS2	170	TBD	TBD	TBD	TBD	TBD	TBD	
				100	TBD	TBD	TBD	TBD	TBD	TBD	

1. *The maximum values are given for LDO regulator ON. Refer to Section 5.3.3 for the SMPS maximum current consumption.*
2. *Evaluated by characterization. Not tested in production.*

Table 26. Typical consumption in Run mode with CoreMark running from flash memory and SRAM

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Typ SMPS	Unit	Typ LDO	Typ SMPS	Unit
		Peripheral	Code							
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, instruction cache 2-way, prefetch ON	FLASH	280	TBD	TBD	mA	TBD	TBD	µA/MHz
				240	TBD	TBD		TBD	TBD	
				200	TBD	TBD		TBD	TBD	
				170	TBD	TBD		TBD	TBD	
				100	TBD	TBD		TBD	TBD	
		All peripherals disabled, instruction cache 1-way, prefetch ON	FLASH	280	TBD	TBD		TBD	TBD	
				240	TBD	TBD		TBD	TBD	
				170	TBD	TBD		TBD	TBD	
				100	TBD	TBD		TBD	TBD	
		All peripherals disabled, instruction cache 2-way	SRAM	280	TBD	TBD		TBD	TBD	
				240	TBD	TBD		TBD	TBD	
				200	TBD	TBD		TBD	TBD	
				170	TBD	TBD		TBD	TBD	
				100	TBD	TBD		TBD	TBD	

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Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Typ SMPS	Unit	Typ LDO	Typ SMPS	Unit
		Peripheral	Code							
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, instruction cache 1-way	SRAM	280	TBD	TBD	mA	TBD	TBD	µA/MHz
				240	TBD	TBD		TBD	TBD	
				170	TBD	TBD		TBD	TBD	
				100	TBD	TBD		TBD	TBD	

Table 27. Typical consumption in Run mode with SecureMark running from flash memory and SRAM

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Typ SMPS	Unit	Typ LDO	Typ SMPS	Unit
		Peripheral	Code							
$I_{DD(Run)}$	Supply current in Run mode	All peripherals disabled, instruction cache 2-way, prefetch ON	FLASH	280	TBD	TBD	mA	TBD	TBD	µA/MHz
				240	TBD	TBD		TBD	TBD	
				170	TBD	TBD		TBD	TBD	
				100	TBD	TBD		TBD	TBD	
		All peripherals disabled, instruction cache 1-way, prefetch ON	FLASH	280	TBD	TBD		TBD	TBD	
				240	TBD	TBD		TBD	TBD	
				170	TBD	TBD		TBD	TBD	
				100	TBD	TBD		TBD	TBD	

Table 28. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions		f_{HCLK} (MHz)	Typ LDO	Typ SMPS	Max(1)(2)				Unit
							T_J = 25°C	T_J = 85°C	T_J = 105 °C	T_J = 140°C	
$I_{DD(sleep)}$	Supply current in sleep mode	All peripherals disabled	VOS0	280	TBD	TBD	TBD	TBD	TBD	TBD	mA
				240	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS1	200	TBD	TBD	TBD	TBD	TBD	TBD	
				170	TBD	TBD	TBD	TBD	TBD	TBD	
			VOS2	170	TBD	TBD	TBD	TBD	TBD	TBD	
				100	TBD	TBD	TBD	TBD	TBD	TBD	

1. *The maximum values are given for LDO regulator ON. Refer to Section 5.3.3 for the SMPS maximum current consumption.*
2. *Evaluated by characterization. Not tested in production.*

Table 29. Typical and maximum current consumption in Stop mode

Symbol	Parameter	Conditions	Typ LDO	Typ SMPS	Max(1)(2)				Unit
					T_J = 25°C	T_J = 85°C	T_J = 105 °C	T_J = 140°C	
$I_{DD(stop)}$	Supply current in Stop	Flash memory in low power mode, SRAMs ON	TBD	TBD	TBD	TBD	TBD	TBD	mA
		Flash memory in normal mode, SRAMs ON	TBD	TBD	TBD	TBD	TBD	TBD	

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Symbol	Parameter	Conditions	Typ LDO	Typ SMPS	Max(1)(2)				Unit
					T_J = 25°C	T_J = 85°C	T_J = 105 °C	T_J = 140°C	
$I_{DD(stop)}$	Supply current in Stop	Flash memory in low power mode, SRAMs OFF except SRAM2 16 Kbytes ON	TBD	TBD	TBD	TBD	TBD	TBD	mA
		Flash memory in low power mode, SRAMs OFF except SRAM2 ON	TBD	TBD	TBD	TBD	TBD	TBD	

1. *The maximum values are given for LDO regulator ON. Refer to Section 5.3.3 for the SMPS maximum current consumption.*
2. *Evaluated by characterization - Not tested in production.*

Table 30. Typical and maximum current consumption in Standby mode

Symbol	Parameter	Conditions	Typ(1)		Max(1)				Unit
		RTC and LSE	3 V	3.3 V	T_J = 25°C	T_J = 85°C	T_J = 105 °C	T_J = 140°C	
$I_{DD(standby)}$	Supply current in standby mode, IWDG OFF	OFF	TBD	TBD	TBD	TBD	TBD	TBD	µA
		ON	TBD	TBD	TBD	TBD	TBD	TBD	

1. *Evaluated by characterization. Not tested in production.*
2. *LSE is in medium-low drive mode.*

I/O system current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in Table 51.

To estimate the current consumption for the output pins, consider also external pull-downs or loads.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this current consumption can be avoided by configuring the I/Os in analog mode. This is notably the case of ADC input pins, to be configured as analog inputs.

Caution: *Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done by using pull-up/down resistors, or by configuring the pins in output mode.*

In addition to the internal peripheral current consumption, the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin where:

- I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load
- V_{DDx} is the MCU supply voltage
- f_{SW} is the I/O switching frequency
- C_L is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$
- The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

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- At startup, all I/O pins are in analog input configuration
- All peripherals are disabled unless otherwise mentioned
- The I/O compensation cell is enabled
- f_{HCLK} is the CPU clock, $f_{PCLK} = f_{rcc_cpu_ck}$, and $f_{HCLK} = f_{rcc_cpu_ck}$.

The given value is calculated by measuring the difference of current consumption:

- With all peripherals clocked off
- With only one peripheral clocked on
- $f_{rcc_cpu_ck}$ = 260 MHz (VOS0), $f_{rcc_cpu_ck}$ = 217 MHz (VOS1), $f_{rcc_cpu_ck}$ = 175 MHz (VOS2)
- Ambient operating temperature is 25°C and V_{DD} = 3.3 V

Table 31. Peripheral current consumption in Sleep mode

Bus	Peripheral	IDD (typ)			Unit
		VOS0	VOS1	VOS2	
AHB1	AHB1	-	-	-	µA/MHz
	ADF	-	-	-	
	OTG-FS	-	-	-	
	HSP	-	-	-	
	GPDMA	-	-	-	
AHB3	AHB3	-	-	-	µA/MHz
	DAC1	-	-	-	
	DAC2	-	-	-	
	DAC3	-	-	-	
	DAC4	-	-	-	
	DAC5	-	-	-	
	DAC6	-	-	-	
	DAC7	-	-	-	
	DAC8	-	-	-	
	ADC12	-	-	-	
	ADC3-4	-	-	-	
	RNG	-	-	-	
	HASH	-	-	-	
AHB2	AHB2	-	-	-	µA/MHz
	FMAC	-	-	-	
	CORDIC	-	-	-	
AHB4	AHB4	-	-	-	µA/MHz
	CRC	-	-	-	
	PWR	-	-	-	
	GPIOI	-	-	-	
	GPIOH	-	-	-	
	GPIOG	-	-	-	
	GPIOF	-	-	-	
	GPIOE	-	-	-	
	GPIOD	-	-	-	

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Bus	Peripheral	IDD (typ)			Unit
		VOS0	VOS1	VOS2	
AHB4	GPIOC	-	-	-	µA/MHz
	GPIOB	-	-	-	
	GPIOA	-	-	-	
AHB5	SDMMC1	-	-	-	µA/MHz
	HPDMA	-	-	-	
	NPU	-	-	-	
	FMC	-	-	-	
	XSPI1	-	-	-	
	FLASH	-	-	-	
	DB-SDMMC1	-	-	-	
	DB-XSPI1	-	-	-	
APB1	APB1	-	-	-	µA/MHz
	FDCAN1	-	-	-	
	FDCAN2	-	-	-	
	CRS	-	-	-	
	I2C2	-	-	-	
	I2C3	-	-	-	
	I2C1	-	-	-	
	UART5	-	-	-	
	UART4	-	-	-	
	UART7	-	-	-	
	UART8	-	-	-	
	USART3	-	-	-	
	USART2	-	-	-	
	SPI3	-	-	-	
	SPI2	-	-	-	
	WWDG1	-	-	-	
	TIM14	-	-	-	
	TIM13	-	-	-	
	TIM12	-	-	-	
	TIM11	-	-	-	
	TIM10	-	-	-	
	TIM7	-	-	-	
	TIM6	-	-	-	
	TIM5	-	-	-	
	TIM4	-	-	-	
	TIM3	-	-	-	
	TIM2	-	-	-	
	UCPD1	-	-	-	
	I3C1	-	-	-	

Prerelease product(s)

Bus	Peripheral	IDD (typ)			Unit
		VOS0	VOS1	VOS2	
APB2	APB2	-	-	-	µA/MHz
	HRTIM2	-	-	-	
	HRTIM1	-	-	-	
	TIM20	-	-	-	
	TIM17	-	-	-	
	TIM16	-	-	-	
	TIM15	-	-	-	
	USART10	-	-	-	
	UART9	-	-	-	
	USART6	-	-	-	
	USART1	-	-	-	
	TIM9	-	-	-	
	TIM8	-	-	-	
	SPI5	-	-	-	
	SPI4	-	-	-	
	SPI1	-	-	-	
	TIM1	-	-	-	
APB4	APB4	-	-	-	µA/MHz
	VREFBUF	-	-	-	
	LPTIM5	-	-	-	
	LPTIM4	-	-	-	
	LPTIM3	-	-	-	
	LPTIM2	-	-	-	
	COMP1	-	-	-	
	COMP2	-	-	-	
	COMP3	-	-	-	
	COMP4	-	-	-	
	COMP5	-	-	-	
	COMP6	-	-	-	
	COMP7	-	-	-	
	COMP8	-	-	-	
	SPI6	-	-	-	
	I2C3	-	-	-	
	LPUART1	-	-	-	
	RTC	-	-	-	
	SBS	-	-	-	

Wake-up time from low-power modes

The times given in Table 32 are measured starting from the wake-up event trigger up to the first instruction executed by the CPU:

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- For Stop or Sleep modes: the wake-up event is WFE.
- WKUP (PA0) pin is used to wake-up from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and V_{DD} = 3.3 V.

Table 32. Low-power mode wake-up timings

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wake-up time from Sleep mode	Instruction cache enabled	15	16	CPU clock cycles
		Instruction cache disabled	15	16	
t_{WUSTOP}	Wake-up time from Stop mode	HSI 64 MHz, flash memory in normal mode	24.1	TBD	µs
		HSI 64 MHz, flash memory in low-power mode	27.6	TBD	
t_{WUSTBY}	Wake-up time from Standby mode	VCAP capacitors discharged	372.5	TBD	

5.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal must respect the Table 33. High-speed external user clock characteristics in addition to Table 51. I/O static characteristics.

Table 33. High-speed external user clock characteristics

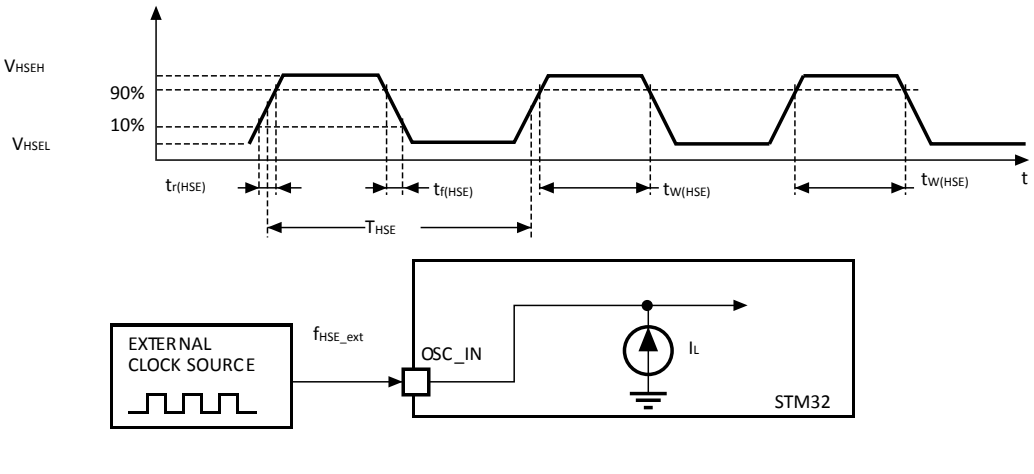
Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	External digital/analog clock	4	25	50	MHz
V_{HSEH}	Digital OSC_IN input high level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{HSEL}	Digital OSC_IN input low level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{w(HSEH)}$ / $t_{w(HSEL)}$ (1)	Digital OSC_IN input high or low time	External digital clock	7	-	-	ns
$V_{isw(HSEH)}$ (2) (V_{HSEH} -V_{HSEL})	Analog low-swing OSC_IN peak-to-peak amplitude	External analog low swing clock	0.2	-	2/3 V_{DD}	V
$DuCy_{HSE}$	Analog low-swing OSC_IN duty cycle		45	50	55	%
$t_{r(HSE)}$ / $t_{f(HSE)}$	Analog low-swing OSC_IN rise and fall times	External analog low swing clock, 10% to 90%	0.05 / f_{HSE_ext}	-	0.3 / f_{HSE_ext}	ns

1. *The rise and fall times for a digital input signal are not specified, but the V_{HSEH} and V_{HSEL} conditions must be fulfilled.*
2. *The DC component of the signal must ensure that the signal peaks are located between V_{DD} and V_{SS}.*

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Figure 26. **High-speed external clock source AC timing diagram**



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal must respect the Table 34. Low-speed external user clock characteristics in addition to Table 51. I/O static characteristics.

Table 34. **Low-speed external user clock characteristics**

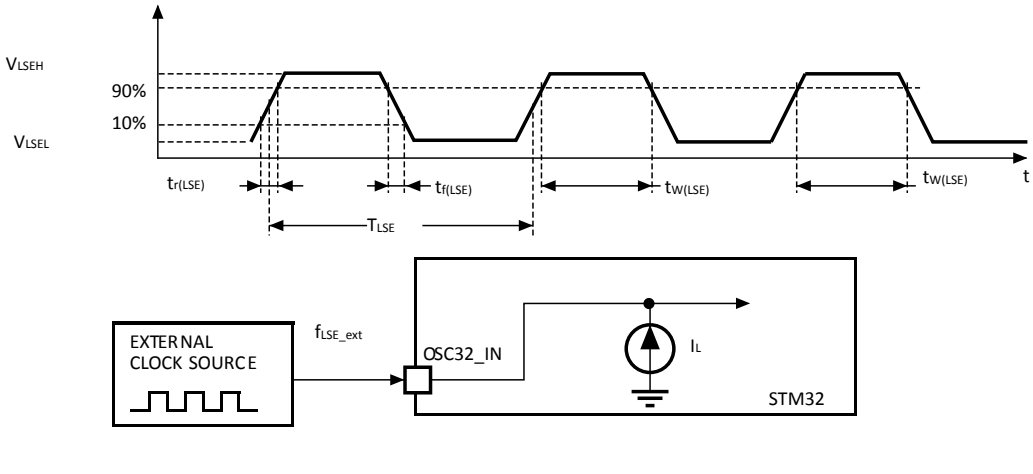
Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	External digital clock	-	32.768	1000	kHz
V_{LSEH}	Digital OSC32_IN input high level voltage	External digital clock	0.7 V_{DD}	-	V_{DD}	V
V_{LSEL}	Digital OSC32_IN input low level voltage		V_{SS}	-	0.3 V_{DD}	
$t_{w(LSEH)}/t_{w(LSEL)}$	Digital OSC_IN input high or low time	External digital clock	250	-	-	ns

Note: For information on selecting the crystal, refer to AN2867 “Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs” available from www.st.com.

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Figure 27. **Low-speed external clock source AC timing diagram**



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 50 MHz crystal/ceramic resonator oscillator.

All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 35. 4-50 MHz HSE oscillator characteristics. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 35. **4-50 MHz HSE oscillator characteristics**

Evaluated by characterization. Not tested in production.

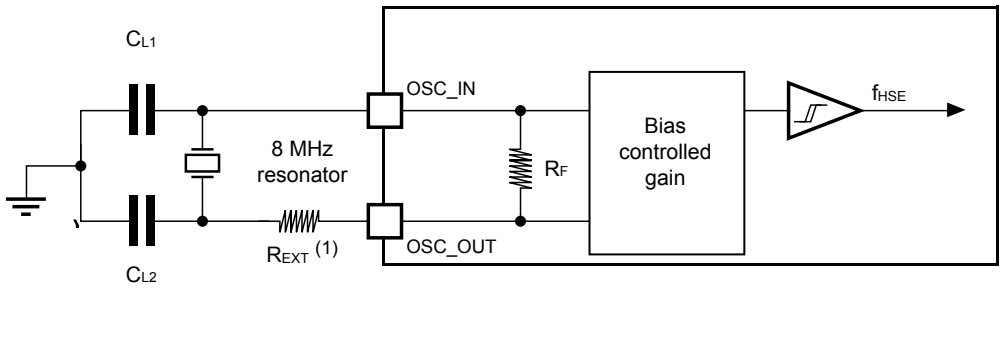
Symbol	Parameter	Operating conditions (1)	Min	Typ	Max	Unit
F	Oscillator frequency	-	4	-	50	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(2)	-	-	10	mA
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 4 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 20 Ω, CL = 10 pF at 16 MHz	-	0.55	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 32 MHz	-	0.67	-	
		V_{DD} = 3 V, Rm = 20 Ω, C_L = 10 pF at 48 MHz	-	1.17	-	
$Gm_{critmax}$	Maximum critical crystal gm	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. *Resonator characteristics given by the crystal/ceramic resonator manufacturer.*
2. *This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.*
3. *$t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.*

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Note: For information on selecting the crystal, refer to AN2867 "Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs", available from www.st.com.

Figure 28. Typical application with an 8 MHz crystal



1. *R_{EXT} value depends on the crystal characteristics.*

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph is based on design simulation results obtained with typical external components specified in Table 36. LSE oscillator characteristics (f_{LSE} = 32.768 kHz). In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 36. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Specified by design. Not tested in production.

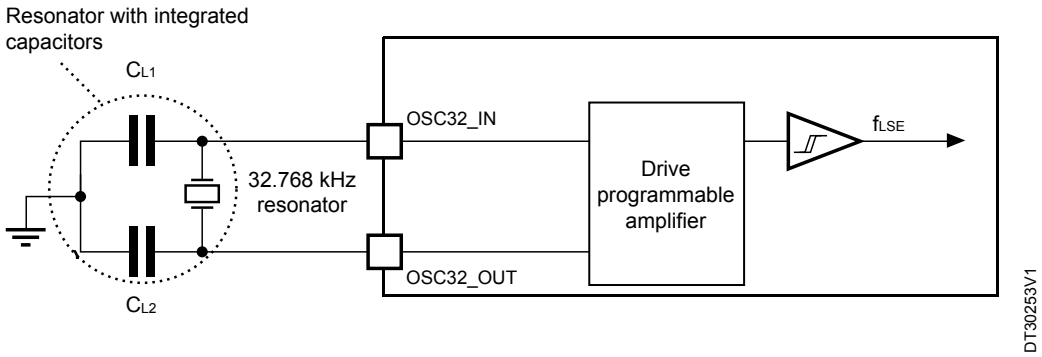
Symbol	Parameter	Conditions (1)	Min	Typ	Max	Unit
F	Oscillator frequency	-	-	32.768	-	kHz
I_{DD}	LSE current consumption	LSEDRV[1:0] = 01 Medium low drive capability	-	333	-	nA
		LSEDRV[1:0] = 10 Medium high drive capability	-	462	-	
		LSEDRV[1:0] = 11 High drive capability	-	747	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	µA/V
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$ (2)	Startup time	V_{DD} is stabilized	-	2	-	s

1. *Refer to the note and caution paragraphs below the table, and to AN2867 "Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs".*
2. *$t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to when a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and can vary significantly with the crystal manufacturer*

Note: For information on selecting the crystal, refer to AN2867 "Guidelines for oscillator design on STM8AF/AL/S and STM32 MCUs/MPUs", available from www.st.com.

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Figure 29. **Typical application with a 32.768 kHz crystal**



Note: An external resistor is not required between OSC32_IN and OSC32_OUT, and it is forbidden to add one.

5.3.9 Internal clock source characteristics

The parameters given in Table 37. HSI48 oscillator characteristics to Table 40. LSI oscillator characteristics are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Section 5.3.1.

48 MHz high-speed internal RC oscillator (HSI48)

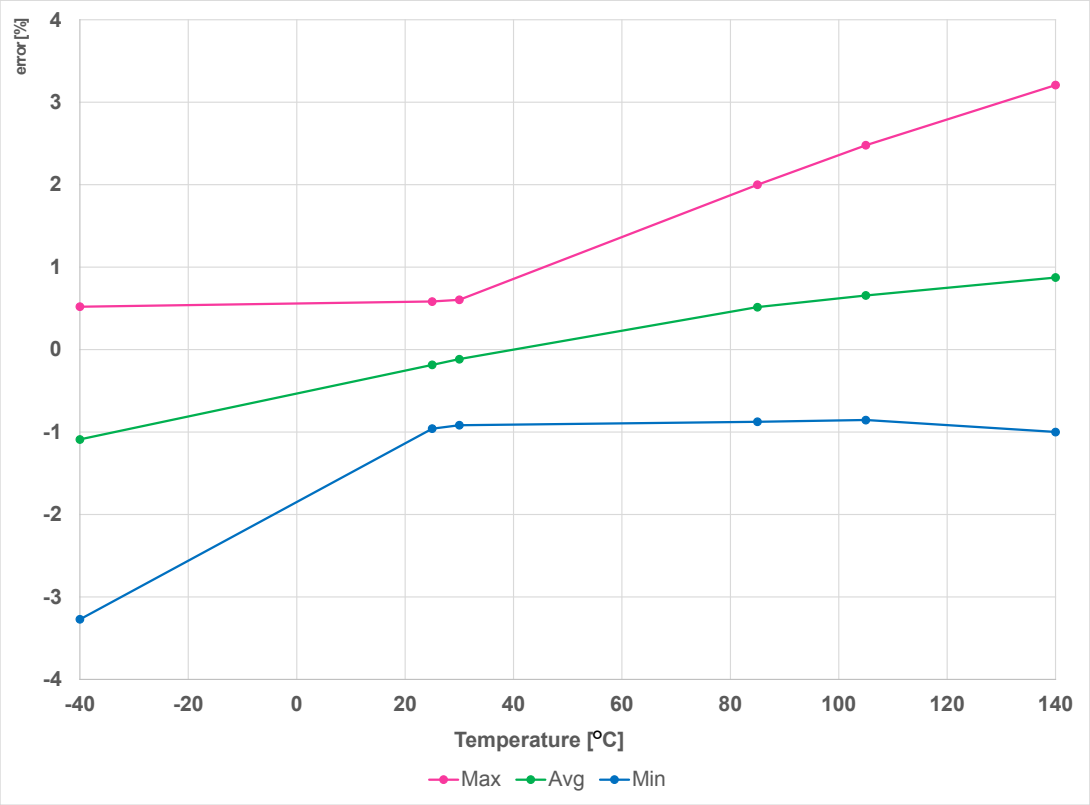
Table 37. **HSI48 oscillator characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 frequency	V_{DD} = 3.3 V, T_J = 30°C	47.5(1)	48	48.5(1)	MHz
TRIM(2)	User trimming step	-	-	0.175	-	%
USER TRIM COVERAGE(3)	User trimming coverage	±32 steps	±4.79	±5.60	-	
$DuCy_{(HSI48)}$(2)	Duty cycle	-	45	-	55	%
ACC_{HSI48_REL}(3)(4)	Accuracy of the HSI48 oscillator over temperature (reference is 30 °C)	T_J = -40 to 125°C	-4.5	-	3.5	%
		T_J = -40 to 140°C	-4.5	-	4.0	
$\Delta_{VDD(HSI48)}$(2)(4)	HSI48 oscillator frequency drift with V_{DD}(5)	V_{DD} = 3.0 to 3.6 V	-	0.025	0.05	%
		V_{DD} = 1.62 to 3.6 V	-	0.05	0.1	
$t_{su(HSI48)}$(2)	HSI48 oscillator start-up time	-	-	2.1	4.0	µs
$I_{DD(HSI48)}$(2)	HSI48 oscillator power consumption	-	-	350	400	µA
N_T jitter(2)	Next transition jitter Accumulated jitter on 28 cycles(6)	-	-	±0.15	-	ns
P_T jitter(2)	Paired transition jitter accumulated jitter on 56 cycles(6)	-	-	±0.25	-	

1. *Calibrated during manufacturing tests.*
2. *Specified by design. Not tested in production.*
3. *Evaluated by characterization. Not tested in production.*
4. *$\Delta f_{HSI} = ACC_{HSI48_REL} + \Delta V_{DD(HSI48)}$*
5. *These values are obtained by using the formula: (Freq(3.6 V) - Freq(3.0 V)) / Freq(3.0 V) or (Freq(3.6 V) - Freq(1.62 V)) / Freq(1.62 V).*
6. *Jitter measurements are performed without clock sources activated in parallel.*

Prerelease product(s)

Figure 30. **HSI48 frequency versus temperature**



64 MHz high-speed internal RC oscillator (HSI)

Table 38. **HSI oscillator characteristics**

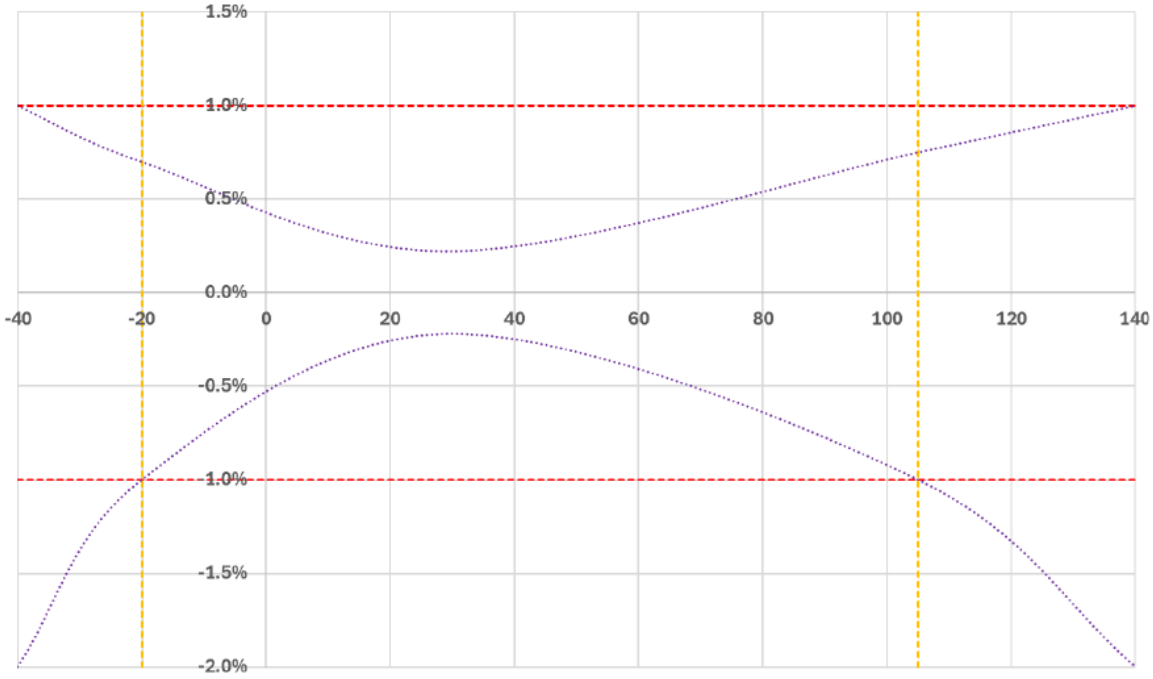
Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	V_{DD} = 3.3 V, T_J = 30°C	63.7(1)	64.0	64.3(1)	MHz
TRIM	User trimming step	Trimming is not a multiple of 32	-	0.24	0.32	%
		Trimming is 128, 256, and 384	-5.2	-1.8	-	
		Trimming is 64, 192, 320, and 488	-1.4	-0.8	-	
		Other trimmings are multiples of 32 (not including multiples of 64 and 128)	-0.6	-0.25	-	
DuCy(HSI)	Duty cycle	-	45	-	55	%
Δ_{VDD}(HSI)	HSI oscillator frequency drift over V_{DD} (reference: 3.3 V)	V_{DD} = 1.62 to 3.6 V	-0.12	-	0.03	%
Δ_{TEMP}(HSI)	HSI oscillator frequency drift over temperature (reference is 64 MHz)	T_J= -20 to 105°C	-1(2)	-	1(2)	
		T_J= -40°C to $T_J$max	-2(2)	-	1(2)	
t_{su}(HSI)	HSI oscillator start-up time	-	-	1.4	2.0	µs
t_{stab}(HSI)	HSI oscillator stabilization time	At 1% of target frequency	-	4	8	µs
I_{DD}(HSI)	HSI oscillator power consumption	-	-	300	400	µA

1. *Specified by test in production.*
2. *Specified by characterization.*

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Figure 31. **HSI frequency versus temperature (TBD)**



4 MHz low-power internal RC oscillator (CSI)

Table 39. **CSI oscillator characteristics**

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	CSI frequency	V_{DD} = 3.3 V, T_J = 30°C	3.96(1)	4	4.04(1)	MHz
TRIM	CSI Trimming step	Trimming is not a multiple of 16	-	0.40	0.75	%
		Trimming is a multiple of 32	-4.75	-2.75	0.75	
		Other trimming values	-0.43	0	0.75	
$DuCy_{(CSI)}$	Duty Cycle	-	45	-	55	%
$\Delta_{VDD\ (CSI)}$	CSI oscillator frequency drift over V_{DD}	V_{DD} = 1.62 V to 3.6 V	-0.06	-	0.06	%
$\Delta_{TEMP\ (CSI)}$	CSI oscillator frequency drift over temperature	T_J = 0 to 85°C	-3.7(2)	-	4.5(2)	%
		T_J = -40 to 140°C	-11(2)	-	7.5(2)	
$t_{su\ (CSI)}$	CSI oscillator start-up time	-	-	1	2	µs
$t_{stab\ (CSI)}$	CSI oscillator stabilization time	to reach 3% of target frequency	-	-	4	cycles
$I_{DD\ (CSI)}$	CSI oscillator power consumption	-	-	23	30	µA

1. *Specified by test in production.*
2. *Specified by characterization.*

Low-speed internal (LSI) RC oscillator

Table 40. **LSI oscillator characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	V_{DD} = 3.3 V, T_J = 25°C	31.4(1)	32	32.6(1)	kHz

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	T_J = -40 to 110°C, V_{DD} = 1.62 to 3.6 V	29.76(2)	-	33.6(2)	kHz
		T_J = -40 to 140°C, V_{DD} = 1.62 to 3.6 V	29.4(2)	-	33.6(2)	
$t_{su(LSI)}$(3)	LSI oscillator start-up time	-	-	80	130	µs
$t_{stab(LSI)}$(3)	LSI oscillator stabilization time (5% of final value)	-	-	120	170	
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	-	130	280	nA

1. *Calibrated during manufacturing tests.*
2. *Evaluated by characterization. Not tested in production.*
3. *Specified by design. Not tested in production.*

5.3.10 PLL characteristics

The parameters given in Table 41. PLL characteristics (high VCO frequency range) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in Section 5.3.1.

Table 41. PLL characteristics (high VCO frequency range)

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		2	-	16	MHz
	PLL input clock duty cycle	-		10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R, S, T	VOS0		1.5	-	520(1)	MHz
		VOS1		1.5	-	435(1)	
		VOS2		1.5	-	350(1)	
f_{VCO_OUT}	PLL VCO output	-		384	-	1672(2)	MHz
t_{LOCK}	PLL lock time	Normal mode		15	50	150(2)	µs
		Sigma-delta mode (f_{PLL_IN} ≥ 8 MHz)		25	60	120(2)	
Jitter	Cycle-to-cycle jitter multiplier output clock P, Q, R, S, T	f_{VCO_OUT} = 384 MHz		-	35	-	±ps
		f_{VCO_OUT} = 1672 MHz		-	15	-	
	Period jitter multiplier output clock P, Q, R, S, T	f_{VCO_OUT} = 384 MHz		-	32	-	%
		f_{VCO_OUT} = 1672 MHz		-	10	-	
	Long term jitter multiplier output clock P, Q, R, S, T	Normal mode (F_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 384 MHz		-	±0.18	-	
		Normal mode (F_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 384 MHz		-	±0.5	-	
		Sigma-delta mode (f_{PLL_IN} = 2 MHz), f_{VCO_OUT} = 560 MHz		-	TBD	-	
		Sigma-delta mode (f_{PLL_IN} = 16 MHz), f_{VCO_OUT} = 560 MHz		-	TBD	-	
$I_{DD(PLL)}$	PLL power consumption	f_{VCO_OUT} freq = 384 MHz	V_{DD}	-	390	548	µA
			V_{CORE}	-	590	3800	
		f_{VCO_OUT} = 1672 MHz	V_{DD}	-	1000	1100	
			V_{CORE}	-	3500	9020	

1. *This value must not exceed the maximum frequency because of the product limitation.*
2. *Evaluated by characterization. Not tested in production.*

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Table 42. PLL characteristics (low VCO frequency range)

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock	-		1	-	2	MHz
	PLL input clock duty cycle	-		10	-	90	%
f_{PLL_OUT}	PLL multiplier output clock P, Q, R	VOS0		1.17	-	210	MHz
		VOS1		1.17	-	210	
		VOS2		1.17	-	160(1)	
f_{VCO_OUT}	PLL VCO output	-		150	-	420	
t_{LOCK}	PLL lock time	Normal mode		-	60	100(2)	µs
		Sigma-delta mode		-	TBD	TBD(2)	
Jitter	Cycle-to-cycle jitter multiplier output clock P, Q, R, S, T	f_{VCO_OUT} = 150 MHz		-	20	-	±ps
		f_{VCO_OUT} = 420 MHz		-	12	-	
	Period jitter multiplier output clock P, Q, R, S, T	f_{VCO_OUT} = 150 MHz		-	15	-	±ps
		f_{VCO_OUT} = 420 MHz		-	8	-	
	Long term jitter multiplier output clock P, Q, R, S, T	Normal mode, f_{VCO_OUT} = 150 MHz	f_{PLL_IN} = 2 MHz	-	±0.35	-	%
		Normal mode, f_{VCO_OUT} = 420 MHz		-	±0.55	-	
$I_{DD(PLL)}$	PLL power consumption on V_{DD}	f_{VCO_OUT} = 420 MHz	V_{DD}	-	200	290	µA
			V_{CORE}	-	625	4880	
		f_{VCO_OUT} = 150 MHz	V_{DD}	-	460	510	
			V_{CORE}	-	1690	6400	

1. *This value must not exceed the maximum frequency because of the product limitation.*
2. *Evaluated by characterization. Not tested in production.*

5.3.11 Memory characteristics

Flash memory

The characteristics are given at T_J = -40 to 140°C unless otherwise specified.

The devices are shipped to customers with the flash memory erased.

Table 43. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
I_{DD}	Supply current	Word program(2)	-	2.5	3.6	mA
		Page erase	-	1.8	4	
		Mass erase	-	2.0	4	

1. *Specified by design. Not tested in production.*
2. *Data are evaluated with a write of 50% of the programmed bits equal to 0.*

Table 44. Flash memory programming

Data are valid for program memory and high-cycling data memory.

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	128 bits (user area)	-	20	22	µs

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Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
t_{prog}	Word programming time	16 bits (OTP area)	-	20	22	µs
t_{ERASE}	Sector (8 Kbytes) erase time	-	-	2	2.2	ms
t_{ME}	Single bank erase time	-	-	256	282	ms
t_{BE}	Dual bank mass erase time	-	-	512	563	ms
V_{prog}	Programming voltage	-	1.8	-	3.6	V

1. *Specified by design. Not tested in production.*

Table 45. Flash memory endurance and data retention

Evaluated by characterization and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Unit
N_{PEND}	Endurance program memory	T_J = -40 to +140°C	10	kcycles
t_{PRET}	Program memory, data retention	1 kcycle at T_A = 85°C	30	Years
		10 kcycles at T_A = 55°C	20	

5.3.12 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed (toggling two LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD),** positive and negative, is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows resuming normal operation.

The test results are given in Table 46. EMS characteristics. They are based on the EMS levels and classes defined in AN1709 “EMC design guide for STM8, STM32 and legacy MCUs”.

Table 46. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to apply on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = 25°C, LQFP176 SMPS, f_{cpu} = 550 MHz, conform to IEC 61000-4-2	2B
V_{FTB}	Fast transient voltage burst limits to apply through 100 pF on VDD and VSS pins to induce a functional disturbance		5A

As a consequence, it is recommended to add a serial resistor (1 kΩ), located as close as possible to the MCU, to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. Note that good EMC performance is highly dependent upon the user application, and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for its application.

Software recommendations

The software flow must include the management of runaway conditions such as:

Prerelease product(s)

- Corrupted program counter
- Unexpected reset
- Critical data corruption (such as control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST or on the oscillator pins for 1 s.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015 “Software techniques for improving microcontrollers EMC performance”).

Electromagnetic interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard, which specifies the test board and the pin loading.

Table 47. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				24/550 MHz	
S_{EMI}	Peak level(1)	V_{DD} = 3.6 V, T_A = 25 °C, LQFP128 SMPS conforming to IEC61967-2	0.1 to 30 MHz	43	dBµV
			30 to 130 MHz	18	
			130 MHz to 1 GHz	27	
			1 GHz to 2 GHz	27	
			EMI level	4	-

1. *Refer to the EMI radiated test chapter of application note AN1709 “EMC design guide for STM8, STM32 and legacy MCUs” available from the ST website www.st.com.*

5.3.13 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive pulse followed by a negative one) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

Table 48. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Packages	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = 25°C, conforming to ANSI/ESDA/JEDEC JS-001	Packages with SMPS	1C	TBD	V
			Packages without SMPS	2	2000	
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = 25°C, conforming to ANSI/ESDA/JEDEC JS-002	LQFP176/144/128	C2a	250	
			LQFP100		750	
			UFBGA/TFBGA		1250	

1. *Evaluated by characterization. Not tested in production.*

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

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- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with the JESD78 IC latch-up standard.

Table 49. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_J = 140 °C, conforming to JESD78	II level A

5.3.14 I/O current injection characteristics

As a general rule, avoid current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3.3 V-capable I/O pins) during the normal product operation. To give an indication of the device robustness when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the characterization.

Functional susceptibility to I/O current injection

While a simple application is executed, the device is stressed by injecting current into the I/O pins (one at the time) programmed in floating input mode, and checked for functional failures. The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits (-5 / +0 µA range) of induced leakage current on adjacent pins, or other functional failures (such as reset, oscillator frequency deviation).

The following table shows I/Os current injection susceptibility data. Negative/positive induced leakage currents are caused, respectively, by negative/positive injection.

Table 50. I/O current injection susceptibility

Evaluated by characterization. Not tested in production.

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on pins PA4, PA5, PC14, PC15	0	0	mA
	Injected current on all other pins	5	N/A	

5.3.15 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in Table 51. I/O static characteristics are derived from tests performed under the conditions summarized in Section 5.3.1: General operating conditions. All I/Os are CMOS and TTL compliant (except for BOOT0).

Note: For information on GPIO configuration, refer to AN4899 "STM32 GPIO configuration for hardware settings and low-power consumption", available on www.st.com.

Table 51. I/O static characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage except BOOT0	1.62 V < V_{DD} < 3.6 V	-	-	$0.3V_{DD}$(1)	V
	I/O input low level voltage except BOOT0		-	-	$0.4V_{DD}-0.1$(2)	
	FT_fb I/O in SMBUS 3.3 mode input low level voltage		-	-	0.8	

Prerelease product(s)

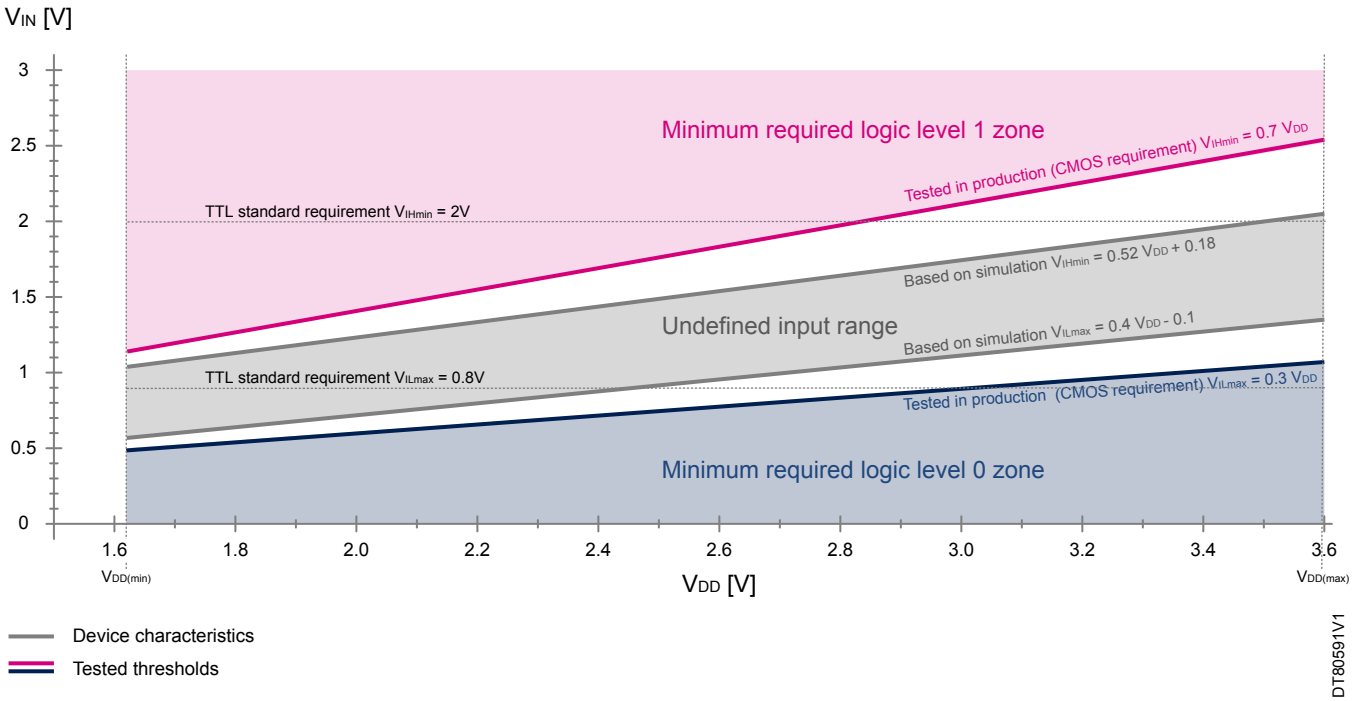
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	BOOT0 I/O input low level voltage	1.62 V < V_{DD} < 3.6 V	-	-	$0.19V_{DD}+0.1$(2)	V
V_{IH}	I/O input high level voltage except BOOT0	1.62 V<V_{DD}<3.6 V	$0.7 \times V_{DD}$(1)	-	-	V
	I/O input high level voltage except BOOT0		$0.52 \times V_{DD} + 0.18$(2)	-	-	
	FT_fb I/O in SMBUS 3.3 mode input high level voltage		1.35	-	-	
	BOOT0 I/O input high level voltage		$0.17 \times V_{DD} + 0.6$(2)	-	-	
V_{HYS}(2)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V < V_{DD} < 3.6 V	-	250	-	mV
	FT_fb I/O in SMBUS 3.3 mode input hysteresis		-	80	-	
	BOOT0 I/O input hysteresis		-	200	-	
I_{leak}(3)	FT_xx input leakage current(2)	0 < V_{IN} ≤ V_{DD}	-	-	+/-200	nA
		V_{DD} < V_{IN} ≤ (V_{DD} + 1 V)(4)	-	-	2500	
		V_{DD} < V_{IN} ≤ 5.5 V(4)	-	-	750	
	TT_xx input leakage current	0 < V_{IN} ≤ V_{DD}	-	-	+/-200	
R_{PU}	Weak pull-up equivalent resistor(5)	V_{IN} = V_{SS}	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	V_{IN} = V_{DD}	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. *Complies with CMOS requirements.*
2. *Specified by design. Not tested in production.*
3. *This parameter represents the pad leakage current of the I/O. The total pad leakage current for the product is calculated using the following formula: $I_{Total_Ileak_max}$ = 10 µA + [number of I/Os with V_{IN} applied to the pad] × I_{leak}(max).*
4. *V_{IN} must be less than V_{DD} + 3.6 V.*
5. *The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS or NMOS transistor. The contribution of the PMOS or NMOS transistor to the series resistance is minimal, approximately 10 percent.*

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in the following figure.

Prerelease product(s)

Figure 32. V_{IL}/V_{IH} for all I/Os except BOOT0



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified in Section 5.2: Absolute maximum ratings. In particular:

- The sum of the currents sourced by all the I/Os on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating $\sum I_{VDD}$ (see Table 12. Current characteristics).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating $\sum I_{VSS}$ (see Table 12. Current characteristics).

Output voltage levels

Unless otherwise specified, the parameters given in Table 52. Output voltage characteristics for all I/Os except PC13, PC14, PC15, PA8 and PA9 are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in Section 5.3.1: General operating conditions. All I/Os are CMOS and TTL compliant.

Table 52. **Output voltage characteristics for all I/Os except PC13, PC14, PC15, PA8 and PA9**

The I_{IO} current sourced or sunk by the device must always comply with the absolute maximum rating specified in Table 11. Voltage characteristics. The sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always comply with the absolute maximum ratings for ΣI_{IO}.

Symbol	Parameter	Conditions(1)	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port(2) I_{IO} = 8 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port(2) I_{IO} = -8 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	

Prerelease product(s)

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{OL}[1]	Output low level voltage	TTL port[2] I_{IO} = 8 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}[1]	Output high level voltage	TTL port[2] I_{IO} = -8 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}[1]	Output low level voltage	I_{IO} = 20 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	1.3	
V_{OH}[1]	Output high level voltage	I_{IO} = -20 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 1.3	-	
V_{OLFM+}[1]	Output low level voltage for an FTf IO pin in FM+ mode	I_{IO} = 20 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
$V_{OLSMBUS3}$[1]	Output low level voltage for an FT_b I/O pin (FT I/O with “b” option)	I_{IO} = 20 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
$V_{OHSMBUS3}$[1]	Output high level voltage for an FT_b I/O pin (FT I/O with “b” option)	I_{IO} = -20 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	TBD	-	

1. *Specified by design and not tested in production, unless otherwise specified.*
2. *TTL and CMOS outputs comply with JEDEC standards JESD36 and JESD52.*

Table 53. Output voltage characteristics for PA8 and PA9

The I_{IO} current sourced or sunk by the device must always comply with the absolute maximum rating specified in Table 11. Voltage characteristics. The sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always comply with the absolute maximum ratings for ΣI_{IO}.

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{OL}[1]	Output low level voltage	CMOS port[2] I_{IO} = 2 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}[1]	Output high level voltage	CMOS port[2] I_{IO} = -2 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	
V_{OL}[1]	Output low level voltage	TTL port[2] I_{IO} = 2 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[1]	Output high level voltage	TTL port[2] I_{IO} = -2 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}[1]	Output low level voltage	I_{IO} = 1 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[1]	Output high level voltage	I_{IO} = -1 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	

1. *Specified by design. Not tested in production.*
2. *TTL and CMOS outputs comply with JEDEC standards JESD36 and JESD52.*

Prerelease product(s)

Prerelease product(s)

Table 54. Output voltage characteristics for PC13, PC14, and PC15

The I_O current sourced or sunk by the device must always comply with the absolute maximum rating specified in Table 11. Voltage characteristics. The sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always comply with the absolute maximum ratings for ΣI_{IO}.

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{OL}	Output low level voltage	CMOS port[1] I_{IO} = 0.5 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	CMOS port[1] I_{IO} = -0.5 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	V_{DD} - 0.4	-	
V_{OL}[2]	Output low level voltage	TTL port[1] I_{IO} = 0.5 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	-	0.4	
V_{OH}[2]	Output high level voltage	TTL port[1] I_{IO} = -0.5 mA 1.62 V ≤ V_{DD} ≤ 3.6 V	2.4	-	

1. *TTL and CMOS outputs comply with JEDEC standards JESD36 and JESD52.*
2. *Specified by design. Not tested in production.*

Table 55. Output timing characteristics for all I/Os except for PA8, and PA9

Specified by design. Not tested in production.

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}[1]	Maximum frequency	C = 50 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	8	MHz
			C = 40 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	10	
			C = 30 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	12	
			C = 20 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	14	
			C = 10 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	16	
	t_r/t_f[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	18.0	ns
			C = 40 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	17.0	
			C = 30 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	15.5	
			C = 20 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	14.2	
			C = 10 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	12.2	
01	F_{max}[1]	Maximum frequency	C = 50 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	40	MHz
			C = 40 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	45	
			C = 30 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	50	
			C = 20 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	55	
			C = 10 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	60	
	t_r/t_f[2]	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	6.2	ns
			C = 40 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	5.7	
			C = 30 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	5.1	
			C = 20 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	4.5	
			C = 10 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	3.7	
10	F_{max}[1]	Maximum frequency	C = 50 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	80	MHz

Speed	Symbol	Parameter	conditions	Min	Max	Unit
10	F_{max}(1)	Maximum frequency	C = 40 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	90	MHz
			C = 30 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	100	
			C = 20 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	110	
			C = 10 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	133	
	t_r/t_f(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	3.8	ns
			C = 40 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	3.4	
			C = 30 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	2.9	
			C = 20 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	2.5	
			C = 10 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	1.9	
11	F_{max}(1)	Maximum frequency	C = 50 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	100	MHz
			C = 40 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	120	
			C = 30 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	140	
			C = 20 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	166	
			C = 10 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	200	
	t_r/t_f(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	3.3	ns
			C = 40 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	2.8	
			C = 30 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	2.3	
			C = 20 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	1.9	
			C = 10 pF, 1.62 V ≤ V_{DD} ≤ 3.6 V	-	1.4	

1. *The maximum frequency is defined under the following conditions: (t_r + t_f) ≤ 2/3 T, skew ≤ 1/20 T, and the duty cycle is between 45% and 55%.*
2. *The fall time is defined as the interval between 90% and 10% of the output waveform. The rise time is defined as the interval between 10% and 90% of the output waveform.*

Table 56. Output timing characteristics for PA8, and PA9

Specified by design. Not tested in production.

Speed	Symbol	Parameter	conditions	Min	Max	Unit
00	F_{max}(1)	Maximum frequency	C = 50 pF 1.62 V ≤ V_{DD} ≤ 3.6 V	-	2	MHz
	t_r/t_f(2)	Output high to low level fall time and output low to high level rise time	C = 50 pF 1.62 V ≤ V_{DD} ≤ 3.6 V	-	166	ns
01	F_{max}(1)	Maximum frequency	C = 30 pF 1.62 V ≤ V_{DD} ≤ 3.6 V	-	10	MHz
	t_r/t_f(2)	Output high to low level fall time and output low to high level rise time	C = 30 pF 1.62 V ≤ V_{DD} ≤ 3.6 V	-	33	ns

1. *The maximum frequency is defined under the following conditions: (t_r + t_f) ≤ 2/3 T, skew ≤ 1/20 T, and the duty cycle is between 45% and 55%.*
2. *The fall time is defined as the interval between 90% and 10% of the output waveform. The rise time is defined as the interval between 10% and 90% of the output waveform.*

5.3.16 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see Table 51. I/O static characteristics).

Prerelease product(s)

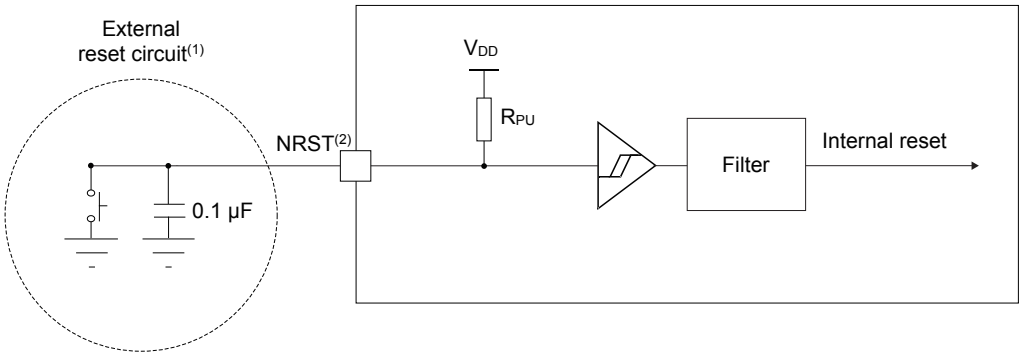
Unless otherwise specified, the parameters in Table 57. NRST pin characteristics are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in Section 5.3.1.

Table 57. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}(1)	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	1.62 V < V_{DD} < 3.6 V	-	-	50	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	1.62 V < V_{DD} < 3.6 V	350	-	-	

1. *Specified by design. Not tested in production.*
2. *The pull-up circuit is designed with a true resistor in series with a switchable PMOS transistor. The contribution of the PMOS transistor to the total series resistance must be minimal, typically on the order of 10 percent.*

Figure 33. Recommended NRST pin protection



1. *The reset network protects the device against parasitic resets.*
2. *The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 51. I/O static characteristics, otherwise the reset is not taken into account by the device.*

5.3.17 FMC characteristics

Unless otherwise specified, the parameters given in Table 58 to Table 71 for the FMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in Table 14. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 × V_{DD}
- IO compensation cell activated
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS high.

Refer to Section 5.3.15: I/O port characteristics for more details on the input/output characteristics.

5.3.17.1 Asynchronous waveforms and timings

Figure 34 through Figure 37 represent asynchronous waveforms and Table 58 through Table 65 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load C_L = 30 pF

In all the timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

Prerelease product(s)

Table 58. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings

Evaluated by characterization, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck} - 1$	$3T_{fmc_ker_ck} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	0	1.5	
$t_{w(NOE)}$	FMC_NOE low time	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck}$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	1	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$2T_{fmc_ker_ck} - 1$	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck} + 15$	-	
$t_{su(Data_NOE)}$	Data to FMC_NOEx high setup time	15	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	1.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck} + 1$	

Table 59. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings

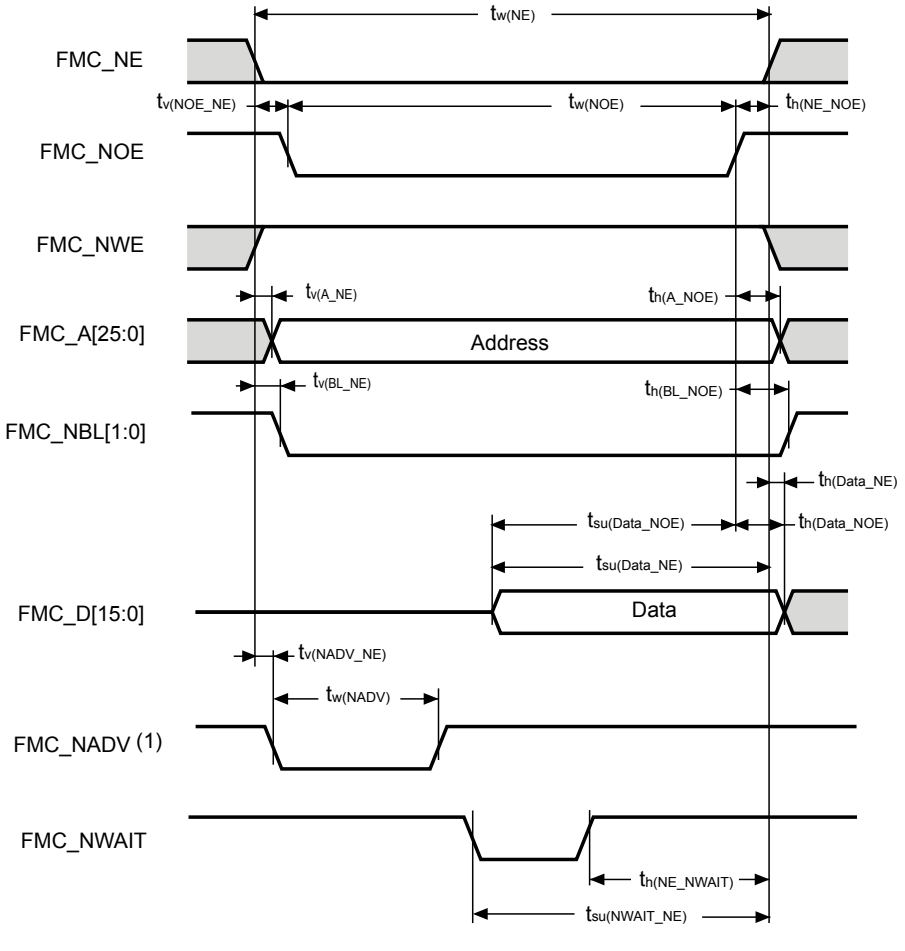
Evaluated by characterization, not tested in production unless otherwise specified.
NWAIT pulse width is equal to 1 fmc_ker_ck clock cycle.

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck} - 1$	$8T_{fmc_ker_ck} + 1$	ns
$t_{w(NOE)}$	FMC_NWE low time	$7T_{fmc_ker_ck} - 1$	$7T_{fmc_ker_ck} + 1$	
$t_{w(NWAIT)}$	FMC_NWAIT low time	$T_{fmc_ker_ck}$	-	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 16$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck} + 16$	-	

Prerelease product(s)

Prerelease product(s)

Figure 34. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. *Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.*

Table 60. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings

Evaluated by characterization, not tested in production.

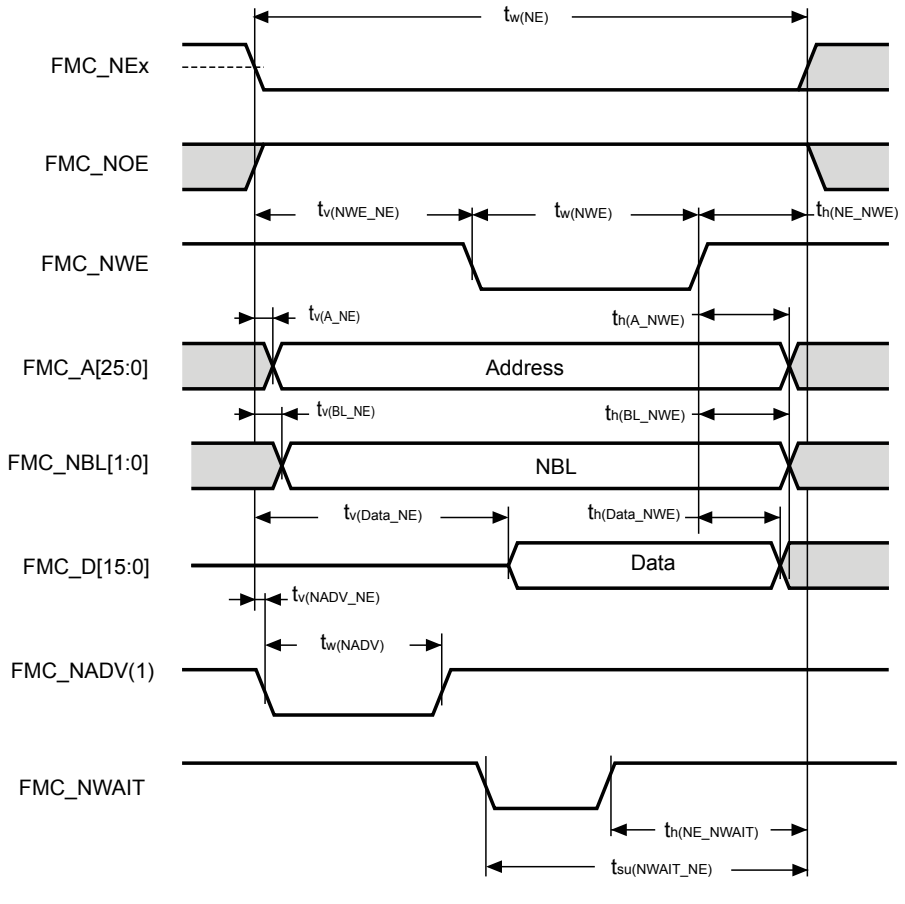
Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$3T_{fmc_ker_ck} - 1$	$3T_{fmc_ker_ck} + 1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck} + 1$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck}$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	1	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{v(Data_NE)}$	FMC_NEx low to data valid	-	$T_{fmc_ker_ck} + 1$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck} + 2$	-	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	-	0.5	
$t_{w(NADV)}$	FMC_NADV low time	-	$T_{fmc_ker_ck} + 0.5$	

Table 61. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings

Evaluated by characterization, not tested in production.
NWAIT pulse width is equal to 1 fmc_ker_ck clock cycle.

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$8T_{fmc_ker_ck} - 1$	$8T_{fmc_ker_ck} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$6T_{fmc_ker_ck} - 1$	$6T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 16$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck} + 16$	-	

Figure 35. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. *Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.*

Table 62. Asynchronous multiplexed PSRAM/NOR read timings

Evaluated by characterization, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck} - 1$	$4T_{fmc_ker_ck} + 1$	ns
$t_{v(NOE_NE)}$	FMC_NEx low to FMC_NOE low	$2T_{fmc_ker_ck} - 1$	$2T_{fmc_ker_ck} + 1$	
$t_{tw(NOE)}$	FMC_NOE low time	$T_{fmc_ker_ck} - 1$	$T_{fmc_ker_ck} + 1$	
$t_{h(NE_NOE)}$	FMC_NOE high to FMC_NE high hold time	$T_{fmc_ker_ck}$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	1.5	

Prerelease product(s)

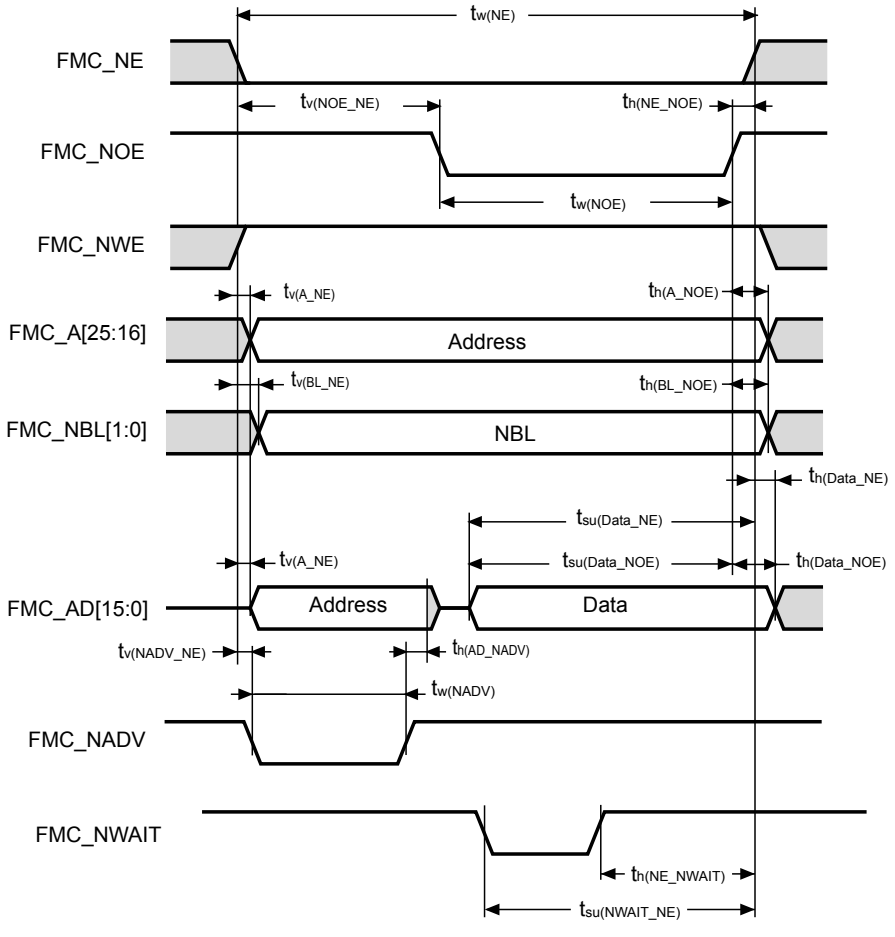
Symbol	Parameter	Min	Max	Unit
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	1.5	ns
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck}$ - 1	$T_{fmc_ker_ck}$ + 1	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck}$ - 3.5	-	
$t_{h(A_NOE)}$	Address hold time after FMC_NOE high	$2T_{fmc_ker_ck}$ - 1.5	-	
$t_{su(Data_NE)}$	Data to FMC_NEx high setup time	$T_{fmc_ker_ck}$ + 15	-	
$t_{su(Data_NOE)}$	Data to FMC_NOE high setup time	15	-	
$t_{h(Data_NE)}$	Data hold time after FMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FMC_NOE high	0	-	

Table 63. Asynchronous multiplexed PSRAM/NOR read - NWAIT timings

Evaluated by characterization, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc_ker_ck}$ - 1	$9T_{fmc_ker_ck}$ + 1	ns
$t_{w(NOE)}$	FMC_NWE low time	$6T_{fmc_ker_ck}$ - 1	$6T_{fmc_ker_ck}$ + 1	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck}$ + 16	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck}$ + 16	-	

Figure 36. Asynchronous multiplexed PSRAM/NOR read waveforms



Prerelease product(s)

Table 64. Asynchronous multiplexed PSRAM/NOR write timings

Evaluated by characterization, not tested in production .

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$4T_{fmc_ker_ck} - 1$	$4T_{fmc_ker_ck} + 1$	ns
$t_{v(NWE_NE)}$	FMC_NEx low to FMC_NWE low	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 0.5$	
$t_{w(NWE)}$	FMC_NWE low time	$2T_{fmc_ker_ck} - 0.5$	$2T_{fmc_ker_ck} + 0.5$	
$t_{h(NE_NWE)}$	FMC_NWE high to FMC_NE high hold time	$T_{fmc_ker_ck} - 1$	-	
$t_{v(A_NE)}$	FMC_NEx low to FMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FMC_NEx low to FMC_NADV low	0	0.5	
$t_{w(NADV)}$	FMC_NADV low time	$T_{fmc_ker_ck} - 0.5$	$T_{fmc_ker_ck} + 0.5$	
$t_{h(AD_NADV)}$	FMC_AD(address) valid hold time after FMC_NADV high	$T_{fmc_ker_ck} - 1.5$	-	
$t_{h(A_NWE)}$	Address hold time after FMC_NWE high	$T_{fmc_ker_ck}$	-	
$t_{h(BL_NWE)}$	FMC_BL hold time after FMC_NWE high	$T_{fmc_ker_ck} + 0.5$	-	
$t_{v(BL_NE)}$	FMC_NEx low to FMC_BL valid	-	0	
$t_{v(Data_NADV)}$	FMC_NADV high to Data valid	-	$T_{fmc_ker_ck} + 0.5$	
$t_{h(Data_NWE)}$	Data hold time after FMC_NWE high	$T_{fmc_ker_ck} + 2$	-	

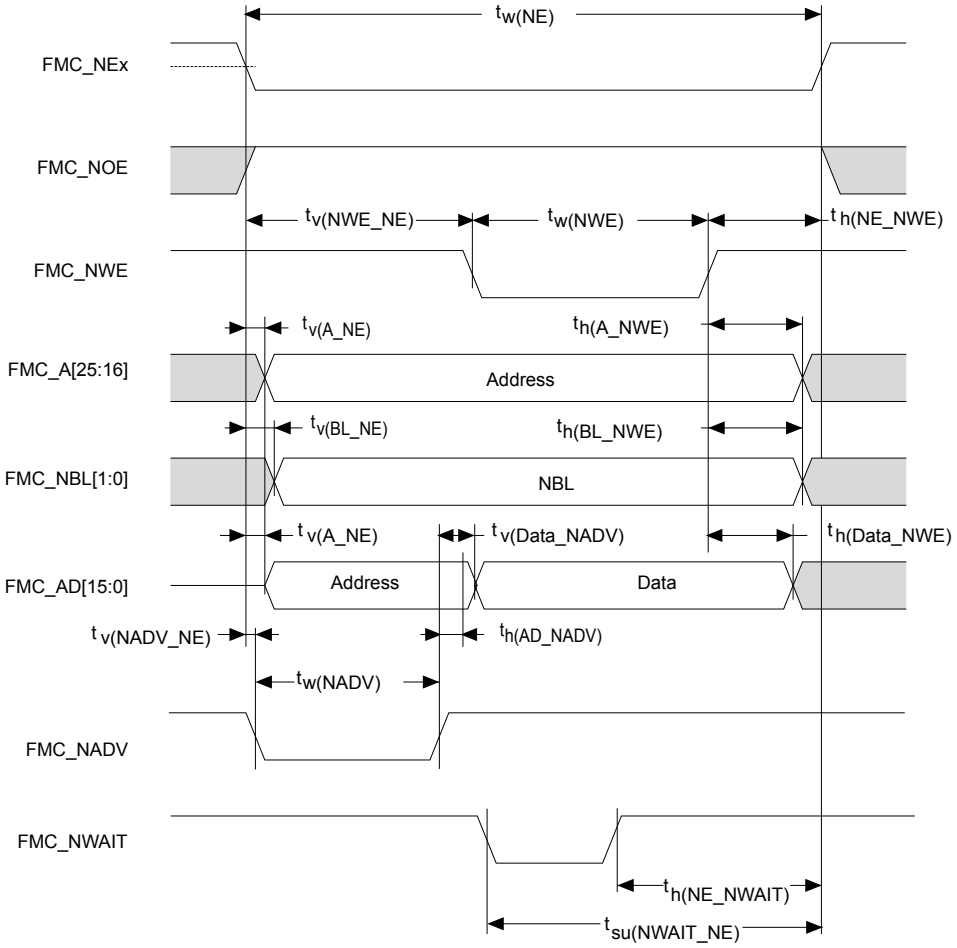
Table 65. Asynchronous multiplexed PSRAM/NOR write - NWAIT timings

Evaluated by characterization, not tested in production.
NWAIT pulse width is equal to 1 fmc_ker_ck clock cycle.

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FMC_NE low time	$9T_{fmc_ker_ck} - 1$	$9T_{fmc_ker_ck} + 1$	ns
$t_{w(NWE)}$	FMC_NWE low time	$7T_{fmc_ker_ck} - 1$	$7T_{fmc_ker_ck} + 1$	
$t_{su(NWAIT_NE)}$	FMC_NWAIT valid before FMC_NEx high	$5T_{fmc_ker_ck} + 16$	-	
$t_{h(NE_NWAIT)}$	FMC_NEx hold time after FMC_NWAIT invalid	$4T_{fmc_ker_ck} + 16$	-	

Prerelease product(s)

Figure 37. **Asynchronous multiplexed PSRAM/NOR write waveforms**



5.3.17.2 *Synchronous waveforms and timings*

Figure 38 through Figure 41 represent synchronous waveforms and Table 66 through Table 69 provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period, with the following FMC_CLK maximum values:

- For 3.0 V < V_{DD} < 3.6 V, FMC_CLK = 70 MHz at 20 pF (66 MHz when using FMC_NWAIT)
- For 1.71 V < V_{DD} < 1.89 V, FMC_CLK = 70 MHz at 20 pF (66 MHz when using FMC_NWAIT)

Table 66. **Synchronous non-multiplexed NOR/PSRAM read timings**

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	TBD	-	-	ns
$t_{(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	TBD	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	TBD	-	-	

Prerelease product(s)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	TBD	ns
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	TBD	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 0..25)	-	-	TBD	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 0..25)	TBD	-	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	-	0	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	TBD	-	-	
$t_{su(DV-CLKH)}$	FMC_D[15:0] valid data before FMC_CLK high	TBD	-	-	
$t_{h(CLKH-DV)}$	FMC_D[15:0] valid data after FMC_CLK high	TBD	-	-	
$t_{(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	TBD	-	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	TBD	-	-	
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT valid (x = 0..2)	-	-	TBD	

Figure 38. Synchronous non-multiplexed NOR/PSRAM read timings

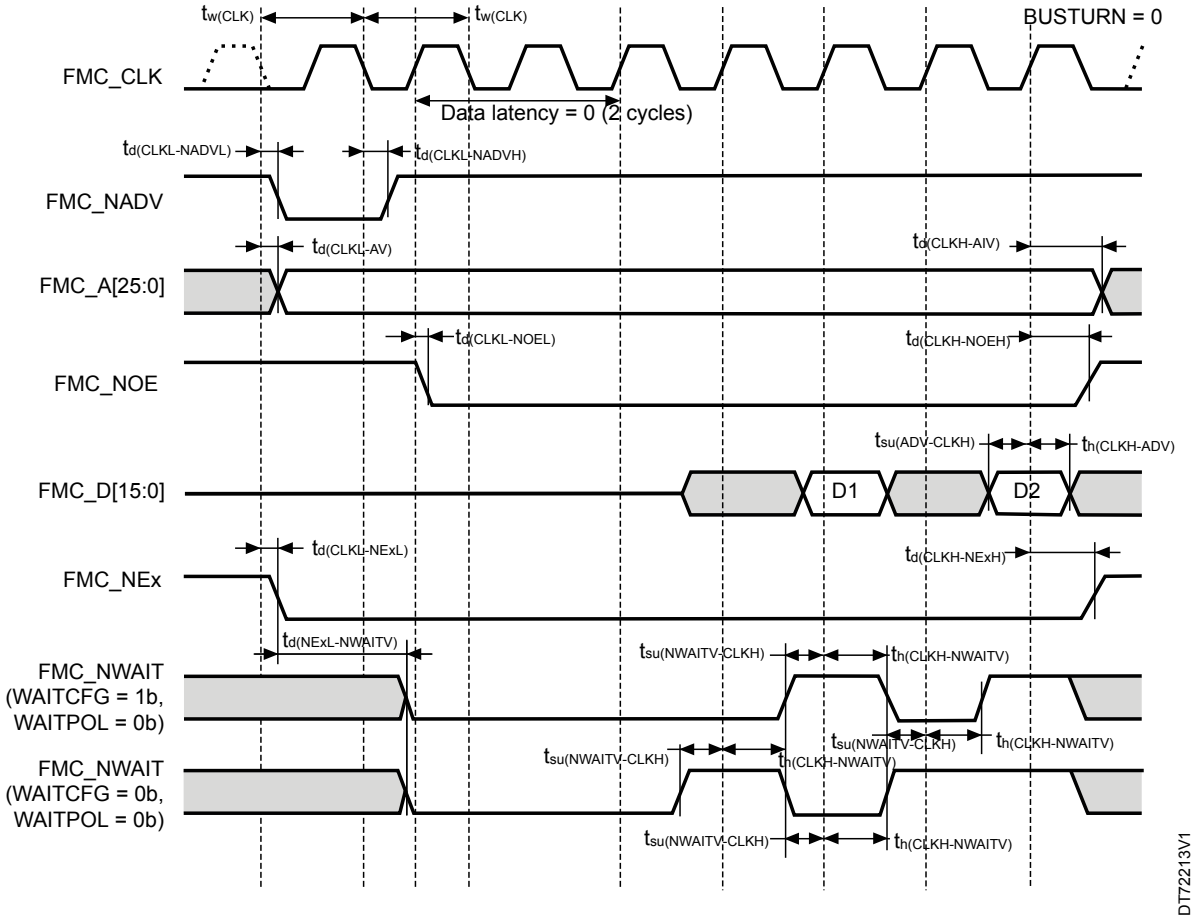


Table 67. Synchronous non-multiplexed PSRAM write timings

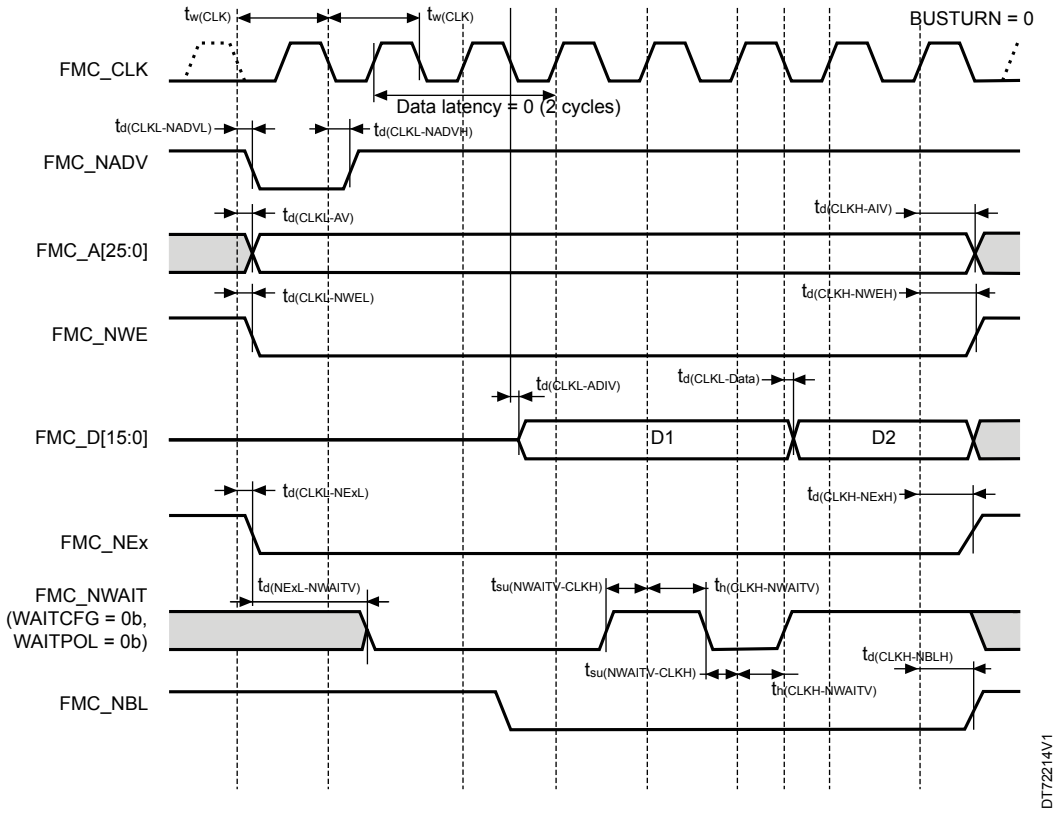
Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{(CLK)}$	FMC_CLK period	TBD	-	-	ns

Prerelease product(s)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	TBD	ns
$t_{(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	TBD	-	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	TBD	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	TBD	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 0..25)	-	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 0..25)	TBD	-	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	-	TBD	
$t_{d(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	TBD	-	-	
$t_{d(CLKL-Data)}$	FMC_D[15:0] valid data after FMC_CLK low	-	-	TBD	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	-	-	TBD	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	TBD	-	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	TBD	-	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	TBD	-	-	
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT valid (x = 0..2)	-	-	TBD	

Figure 39. Synchronous non-multiplexed PSRAM write timings



Prerelease product(s)

Table 68. Synchronous multiplexed NOR/PSRAM read timings

Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	TBD	-	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	TBD	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	TBD	-	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	TBD	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	TBD	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16..25)	-	-	0	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16..25)	TBD	-	-	
$t_{d(CLKL-NOEL)}$	FMC_CLK low to FMC_NOE low	-	-	TBD	
$t_{d(CLKH-NOEH)}$	FMC_CLK high to FMC_NOE high	TBD	-	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	-	TBD	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	TBD	-	-	
$t_{su(ADV-CLKH)}$	FMC_A/D[15:0] valid data before FMC_CLK high	TBD	-	-	
$t_{h(CLKH-ADV)}$	FMC_A/D[15:0] valid data after FMC_CLK high	TBD	-	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	TBD	-	-	
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	TBD	-	-	
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT valid (x = 0..2)	-	-	TBD	

Prerelease product(s)

Figure 40. **Synchronous multiplexed NOR/PSRAM read timings**

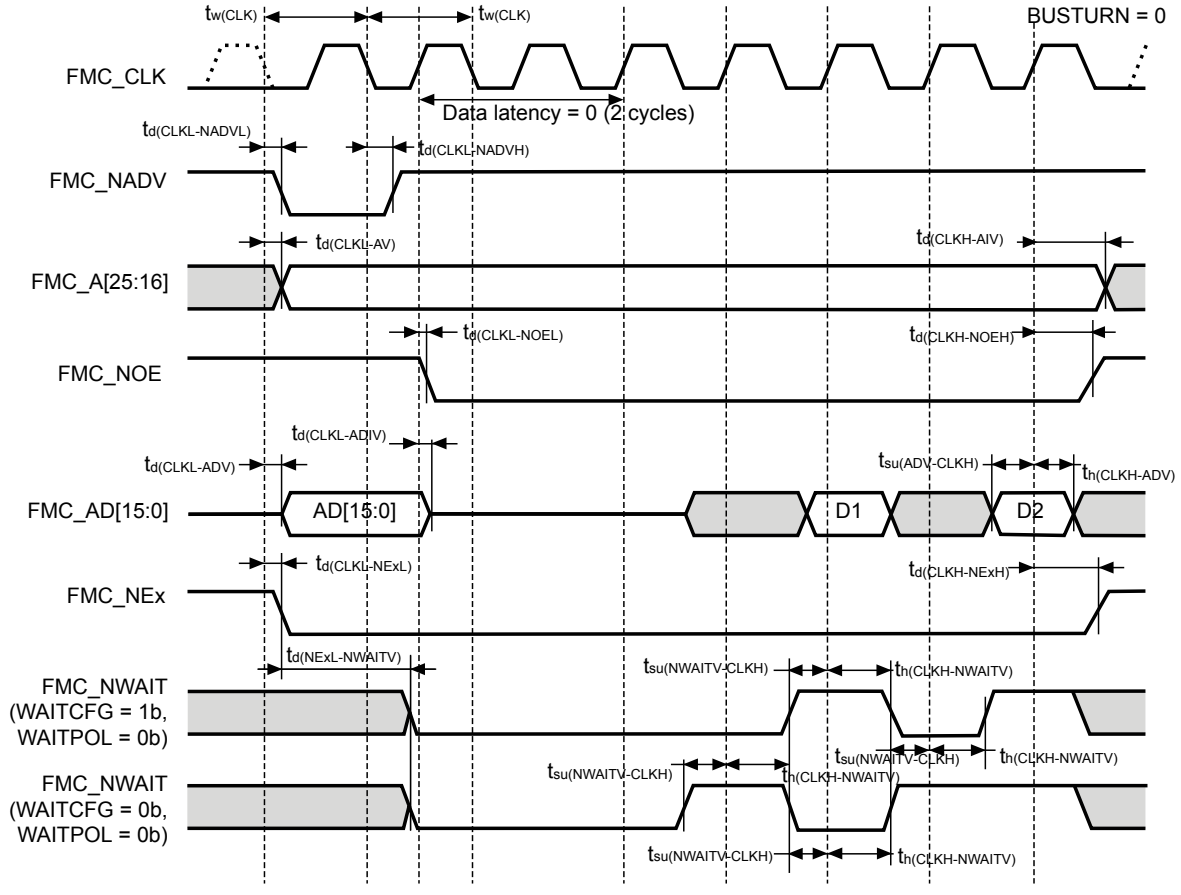


Table 69. **Synchronous multiplexed PSRAM write timings**

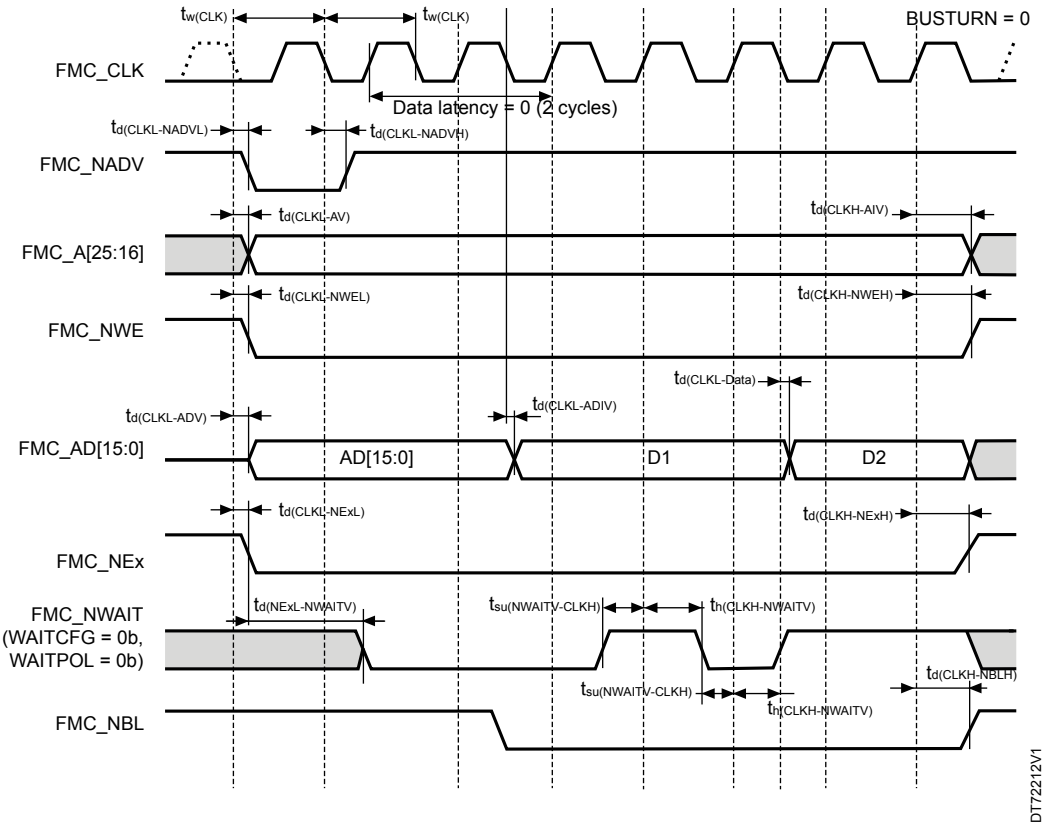
Evaluated by characterization, not tested in production unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$t_{w(CLK)}$	FMC_CLK period	TBD	-	-	ns
$t_{d(CLKL-NExL)}$	FMC_CLK low to FMC_NEx low (x = 0..2)	-	-	TBD	
$t_{d(CLKH-NExH)}$	FMC_CLK high to FMC_NEx high (x = 0..2)	TBD	-	-	
$t_{d(CLKL-NADVL)}$	FMC_CLK low to FMC_NADV low	-	-	TBD	
$t_{d(CLKL-NADVH)}$	FMC_CLK low to FMC_NADV high	TBD	-	-	
$t_{d(CLKL-AV)}$	FMC_CLK low to FMC_Ax valid (x = 16..25)	-	-	TBD	
$t_{d(CLKH-AIV)}$	FMC_CLK high to FMC_Ax invalid (x = 16..25)	TBD	-	-	
$t_{d(CLKL-NWEL)}$	FMC_CLK low to FMC_NWE low	-	-	TBD	
$t_{(CLKH-NWEH)}$	FMC_CLK high to FMC_NWE high	TBD	-	-	
$t_{d(CLKL-ADV)}$	FMC_CLK low to FMC_AD[15:0] valid	-	-	TBD	
$t_{d(CLKL-ADIV)}$	FMC_CLK low to FMC_AD[15:0] invalid	TBD	-	-	
$t_{d(CLKL-DATA)}$	FMC_A/D[15:0] valid data after FMC_CLK low	-	-	TBD	
$t_{d(CLKL-NBLL)}$	FMC_CLK low to FMC_NBL low	TBD	-	-	
$t_{d(CLKH-NBLH)}$	FMC_CLK high to FMC_NBL high	TBD	-	-	
$t_{su(NWAIT-CLKH)}$	FMC_NWAIT valid before FMC_CLK high	TBD	-	-	

Prerelease product(s)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{h(CLKH-NWAIT)}$	FMC_NWAIT valid after FMC_CLK high	TBD	-	-	ns
$t_{d(NExL-NWAITV)}$	FMC_NEx low to FMC_NWAIT valid (x = 0..2)	-	-	TBD	

Figure 41. Synchronous multiplexed PSRAM write timings



5.3.17.3 *NAND controller waveforms and timings*

Figure 42 and Figure 43 represent synchronous waveforms, and Table 70 and Table 71 provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- C_L = 30-pF

In all timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

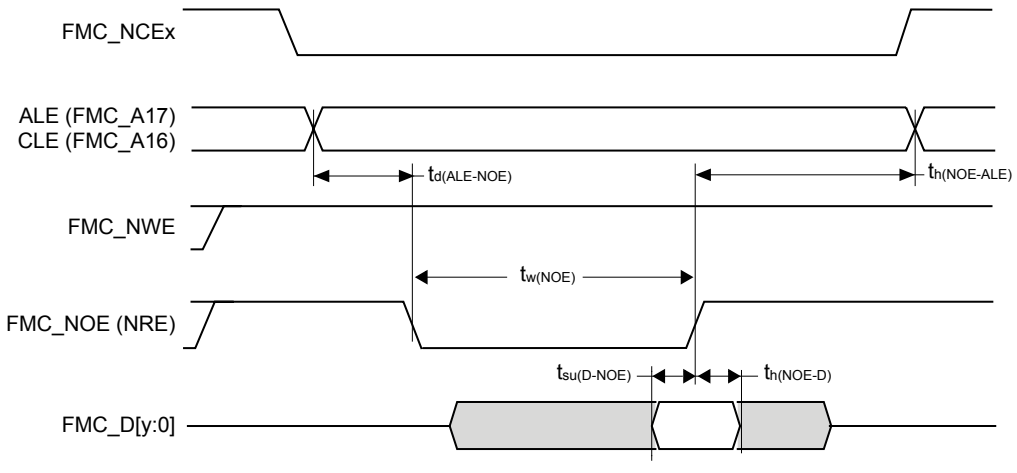
Prerelease product(s)

Table 70. NAND flash read timings

Evaluated by characterization, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{w(N0E)}$	FMC_NOE low width	$4T_{fmc_ker_ck}$ - 0.5	$4T_{fmc_ker_ck}$ + 0.5	ns
$t_{su(D-NOE)}$	FMC_D[15-0] valid data before FMC_NOE high	12.5	-	
$t_{h(NOE-D)}$	FMC_D[15-0] valid data after FMC_NOE high	0	-	
$t_{d(ALE-NOE)}$	FMC_ALE valid before FMC_NOE low	-	$3T_{fmc_ker_ck}$ + 0.5	
$t_{h(NOE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$4T_{fmc_ker_ck}$ - 1	-	

Figure 42. NAND controller waveforms for read access



1. *y = 7 or 15 depending on the NAND flash memory interface.*

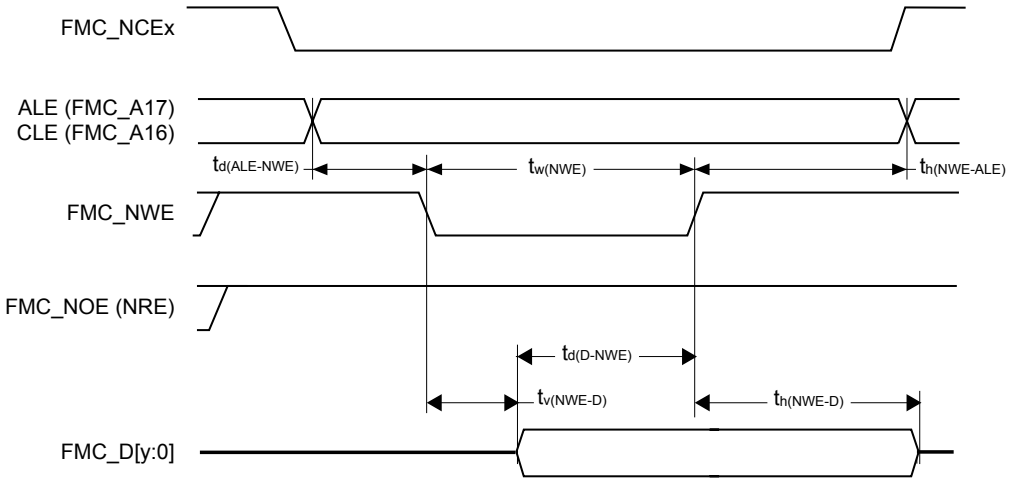
Table 71. NAND flash write timings

Evaluated by characterization, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FMC_NWE low width	$4T_{fmc_ker_ck}$ - 0.5	$4T_{fmc_ker_ck}$ + 0.5	ns
$t_{v(NWE-D)}$	FMC_NWE low to FMC_D[15-0] valid	0	-	
$t_{h(NWE-D)}$	FMC_NWE high to FMC_D[15-0] invalid	$2T_{fmc_ker_ck}$ + 1	-	
$t_{d(D-NWE)}$	FMC_D[15-0] valid before FMC_NWE high	$5T_{fmc_ker_ck}$ - 2	-	
$t_{d(ALE-NWE)}$	FMC_ALE valid before FMC_NWE low	-	$3T_{fmc_ker_ck}$ - 1	
$t_{h(NWE-ALE)}$	FMC_NWE high to FMC_ALE invalid	$2T_{fmc_ker_ck}$ + 1.5	-	

Prerelease product(s)

Figure 43. **NAND controller waveforms for write access**



1. *y = 7 or 15 depending on the NAND flash memory interface.*

5.3.17.4 *SDRAM waveforms and timings*

In all timing tables, Tfmc_ker_ck is the fmc_ker_ck clock period, with the following FMC_SDCLK maximum values:

- For 2.7 V < 3.6 V: maximum FMC_CLK = 95 MHz at 20 pF
- For 2.7 V < 3.6 V: maximum FMC_CLK = 100 MHz at 15 pF
- For 1.71 V < 1.9 V: maximum FMC_CLK = 90 MHz at 20 pF
- For 1.71 V < 1.9 V: maximum FMC_CLK = 95 MHz at 15 pF

Note: At VOS low, the performance can be degraded by up to 7% compared to VOS high.

Table 72. **SDRAM read timings**

Evaluated by characterization, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	2 $T_{fmc_ker_ck}$ - 0.5	2 $T_{fmc_ker_ck}$ + 0.5	ns
$t_{su(SDCLKH_Data)}$	Data input setup time	3	-	
$t_{h(SDCLK\ H_Data)}$	Data input hold time	1	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL-\ SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	2	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

Table 73. **LPSDR SDRAM read timings**

Evaluated by characterization, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	2 $T_{fmc_ker_ck}$ - 0.5	2 $T_{fmc_ker_ck}$ + 0.5	ns

Prerelease product(s)

Symbol	Parameter	Min	Max	Unit
$t_{su(SDCLKH_Data)}$	Data input setup time	3	-	ns
$t_{h(SDCLK\ H_Data)}$	Data input hold time	1	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	1.5	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	1.5	
$t_{h(SDCLKL-\ SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	2	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1	
$t_{h(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

Figure 44. SDRAM read access waveforms (CL = 1)

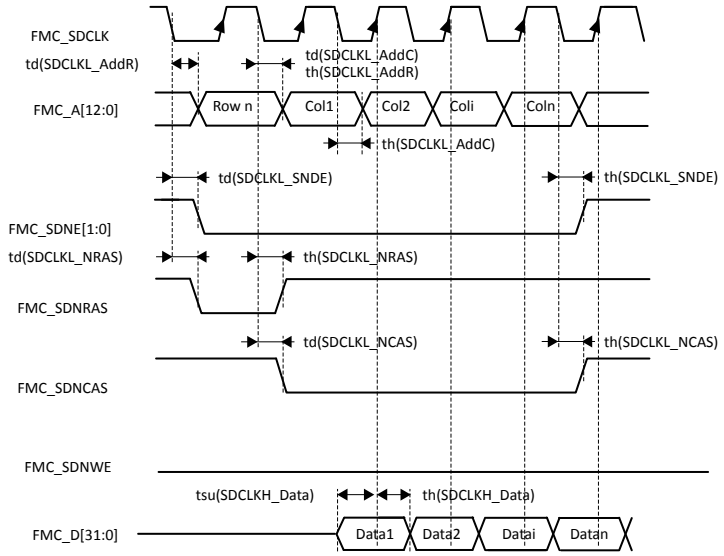


Table 74. SDRAM write timings

Evaluated by characterization, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	2 $T_{fmc_ker_ck}$ - 0.5	2 $T_{fmc_ker_ck}$ + 0.5	ns
$t_{d(SDCLKL_Data)}$	Data output valid time	-	1.5	
$t_{h(SDCLKL_Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	2	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0	-	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	1	
th(SDCLKL-SDNE)	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	

Prerelease product(s)

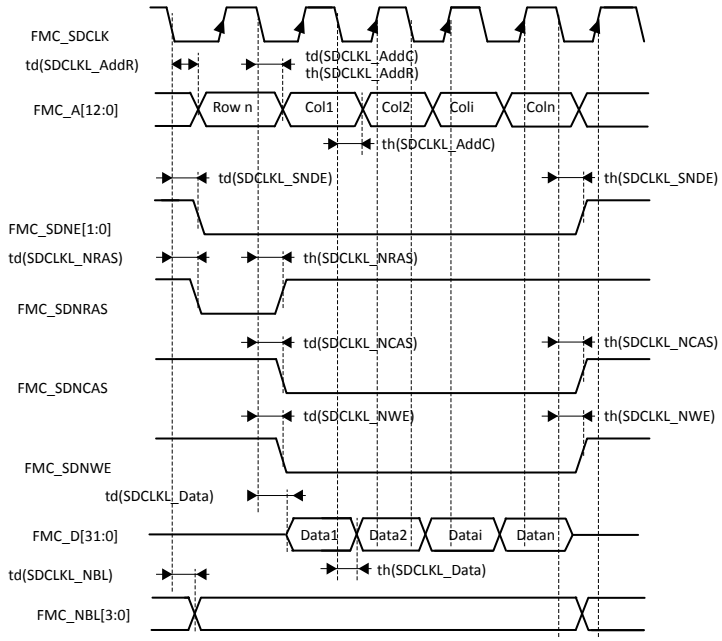
Symbol	Parameter	Min	Max	Unit
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1.5	ns
$t_{h(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

Table 75. LPSDR SDRAM Write timings

Evaluated by characterization, not tested in production.

Symbol	Parameter	Min	Max	Unit
$t_{w(SDCLK)}$	FMC_SDCLK period	2 $T_{fmc_ker_ck}$ - 0.5	2 $T_{fmc_ker_ck}$ + 0.5	ns
$t_{d(SDCLKL\ _Data)}$	Data output valid time	-	1.5	
$t_{h(SDCLKL\ _Data)}$	Data output hold time	0	-	
$t_{d(SDCLKL_Add)}$	Address valid time	-	2	
$t_{d(SDCLKL-SDNWE)}$	SDNWE valid time	-	1.5	
$t_{h(SDCLKL-SDNWE)}$	SDNWE hold time	0.5	-	
$t_{d(SDCLKL-\ SDNE)}$	Chip select valid time	-	1	
$t_{h(SDCLKL-\ SDNE)}$	Chip select hold time	0	-	
$t_{d(SDCLKL-SDNRAS)}$	SDNRAS valid time	-	1.5	
$t_{h(SDCLKL-SDNRAS)}$	SDNRAS hold time	0	-	
$t_{d(SDCLKL-SDNCAS)}$	SDNCAS valid time	-	1.5	
$t_{h(SDCLKL-SDNCAS)}$	SDNCAS hold time	0	-	

Figure 45. SDRAM write access waveforms



5.3.18 Extended interrupt and event controller input (EXTI) characteristics

The pulse on the interrupt input must have a minimal length to ensure its detection by the event controller.

Prerelease product(s)

Table 76. EXTI input characteristics

Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PLEC	Pulse length to event controller	-	20	-	-	ns

5.3.19 XSPI interface characteristics

Unless otherwise specified, the parameters given in Table 77 and Table 78 are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in Section 5.3.1: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- VOS level set to VOS0

Refer to Section 5.3.15: I/O port characteristics for more details on the input/output alternate function characteristics.

Table 77. XSPI characteristics in SDR mode

All values apply to octo-SPI and quad-SPI modes.
Evaluated by characterization. Not tested in production.
Delay block bypassed.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(CLK)}$	Clock frequency	1.71 V < V_{DD} < 3.6 V, C_L = 15 pF	-	-	100	MHz
		2.71V < V_{DD} < 3.6 V, C_L = 15 pF			130	
$t_{w(CLKH)}$	Clock high and low time, even division	PRESCALER[7:0] = n (= 0, 1, 3, 5, …, 255)	$t_{(CLK)}/2$	-	$t_{(CLK)}/2 + 1$	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2 - 1$		$t_{(CLK)}/2$	
$t_{w(CLKH)}$	Clock high and low time, odd division	PRESCALER[7:0] = n (= 2, 4, 6, …, 254)	$(n/2) \times t_{(CLK)}/(n + 1)$	-	$(n/2) \times t_{(CLK)}/(n + 1) + 1$	
$t_{w(CLKL)}$			$(n/2 + 1) \times t_{(CLK)}/(n + 1) - 1$		$(n/2 + 1) \times t_{(CLK)}/(n + 1)$	
$t_{s(IN)}$	Data input setup time	-	2.5	-	-	
$t_{h(IN)}$	Data input hold time	-	2	-	-	
$t_{v(OUT)}$	Data output valid time	-	-	0.5	1.0	
$t_{h(OUT)}$	Data output hold time	-	0	-	-	

Prerelease product(s)

Figure 46. **XSPI SDR read/write timing diagram**

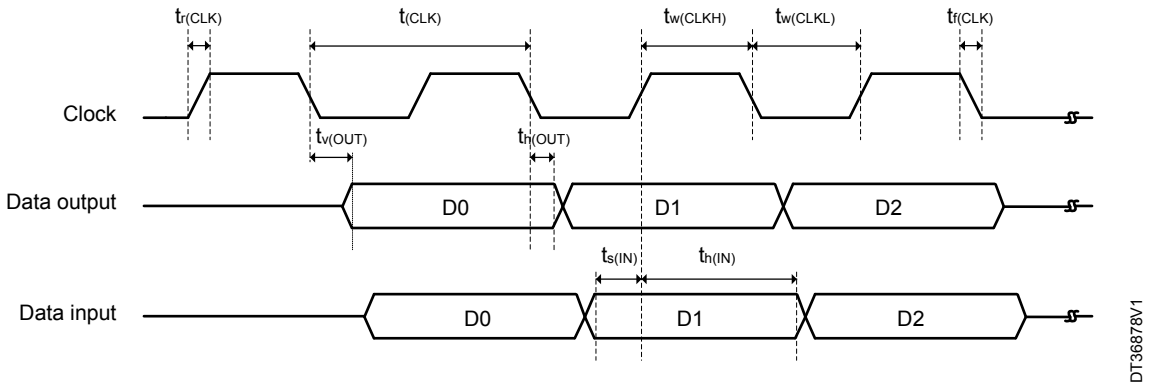


Table 78. **XSPI characteristics in DTR mode (no DQS)**

All values apply to octo-SPI and quad-SPI modes.
Evaluated by characterization. Not tested in production.
Delay block bypassed.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(CLK)}$	Clock frequency	1.71 V < V_{DD} < 3.6 V, C_L = 15 pF	-	-	100(1)	MHz
$t_{w(CLKH)}$	Clock high and low time, even division	PRESCALER[7:0] = n (= 0, 1, 3, 5, …, 255)	$t_{(CLK)}/2$	-	$t_{(CLK)}/2 + 1$	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2 - 1$		$t_{(CLK)}/2$	
$t_{w(CLKH)}$	Clock high and low time, odd division	PRESCALER[7:0] = n (= 2, 4, 6, …, 254)	$(n/2) \times t_{(CLK)}/(n + 1)$	-	$(n/2) \times t_{(CLK)}/(n + 1) + 1$	
$t_{w(CLKL)}$			$(n/2 + 1) \times t_{(CLK)}/(n + 1) -1$		$(n/2 + 1) \times t_{(CLK)}/(n + 1)$	
$t_{sr(IN)}$,$t_{sf(IN)}$	Data input setup time	-	2	-	-	
$t_{hr(IN)}$, $t_{hr(IN)}$	Data input hold time	-	2	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	DHQC = 0	-	3.5	4.5	
		DHQC = 1, PRESCALER[7:0] = 1, 2…	-	$t_{(CLK)}/4 + 0.5$	$t_{(CLK)}/4 + 1.5$	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	DHQC = 0	1	-	-	
		DHQC = 1, PRESCALER[7:0] = 1, 2…	$t_{(CLK)}/4 - 0.5$	-	-	

1. *Set DHQC to reach the specified frequency.*

Table 79. **XSPI characteristics in DTR mode (with DQS) / HyperBus**

Evaluated by characterization. Not tested in production.
Delay block activated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{(CLK)}$	Clock frequency	1.71V < V_{DD} < 3.6 V, C_L = 15 pF	-	-	111(1)(2)	MHz
$t_{w(CLKH)}$	Clock high and low time, even division	PRESCALER[7:0] = n (= 0, 1, 3, 5, …, 255)	$t_{(CLK)}/2$	-	$t_{(CLK)}/2 + 1$	ns
$t_{w(CLKL)}$			$t_{(CLK)}/2 - 1$		$t_{(CLK)}/2$	
$t_{w(CLKH)}$	Clock high and low time, odd division	PRESCALER[7:0] = n (= 2, 4, 6, …, 254)	$(n/2) \times t_{(CLK)}/(n + 1)$	-	$(n/2) \times t_{(CLK)}/(n + 1) + 1$	
$t_{w(CLKL)}$			$(n/2 + 1) \times t_{(CLK)}/(n + 1) - 1$		$(n/2 + 1)*t_{(CLK)}/(n+1)$	

Prerelease product(s)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(CLK)}$	Clock valid time	-	-	-	$t_{(CLK)}$ + 2	ns
$t_{h(CLK)}$	Clock hold time	-	$t_{(CLK)}/2$ - 1	-	-	
$V_{ODr(CLK)}$ (3)	CLK, NCLK crossing level on CLK rising edge	V_{DD} = 1.8 V	1015	-	1320	mV
$V_{ODf(CLK)}$ (3)	CLK, NCLK crossing level on CLK falling edge	V_{DD} = 1.8 V	975	-	1310	
$t_{w(CS)}$	Chip select high time	-	3 × $t_{(CLK)}$	-	-	ns
$t_{v(DQ)}$	Data input valid time	-	0	-	-	
$t_{v(DS)}$	Data strobe input valid time	-	0	-	-	
$t_{h(DS)}$	Data strobe input hold time	-	0	-	-	
$t_{v(RWDS)}$	Data strobe output valid time	-	-	-	3 × $t_{(CLK)}$	
$t_{sr(DQ)}$,$t_{sf(DQ)}$	Data input setup time	-	-0.5	-	-	
$t_{hr(DQ)}$, $t_{hr(DQ)}$	Data input hold time	-	4	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	DHQC = 0	-	3.5	4.5	
		DHQC = 1, PRESCALER[7:0] = 1, 2…	-	$t_{(CLK)}/4$ + 0.5	$t_{(CLK)}/4$ + 1.5	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	DHQC = 0	1	-	-	
		DHQC = 1, PRESCALER[7:0] = 1, 2…	$t_{(CLK)}/4$ - 0.5	-	-	

1. *Maximum frequency values are specified for a maximum RWDS-to-DQ skew of 1 ns.*
2. *Set DHQC to reach the specified frequency.*
3. *It is recommended that PD2/PD3 are aligned according to the crossing specification.*

Figure 47. XSPI timing diagram - DTR mode

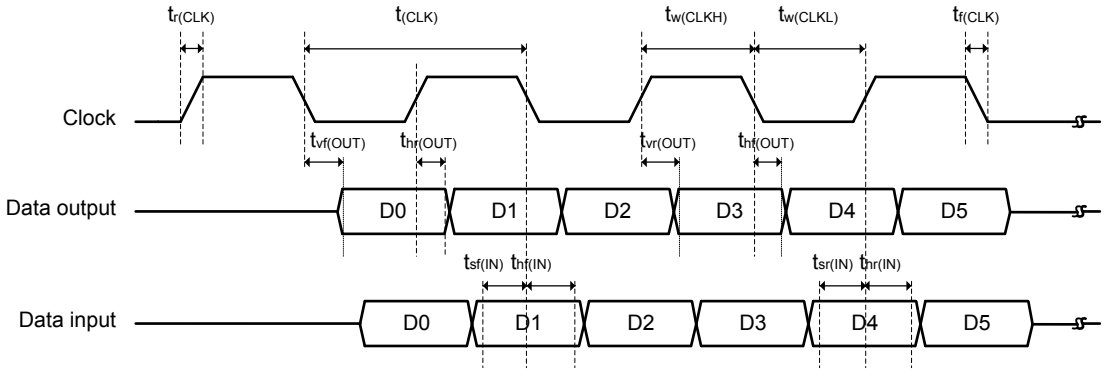
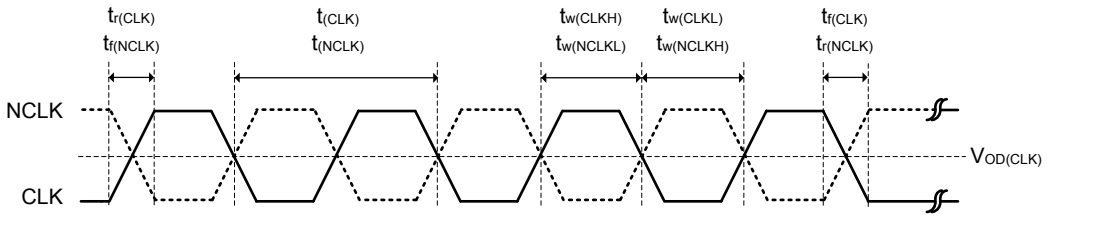


Figure 48. XSPI HyperBus clock



Prerelease product(s)

Figure 49. **XSPI HyperBus read**

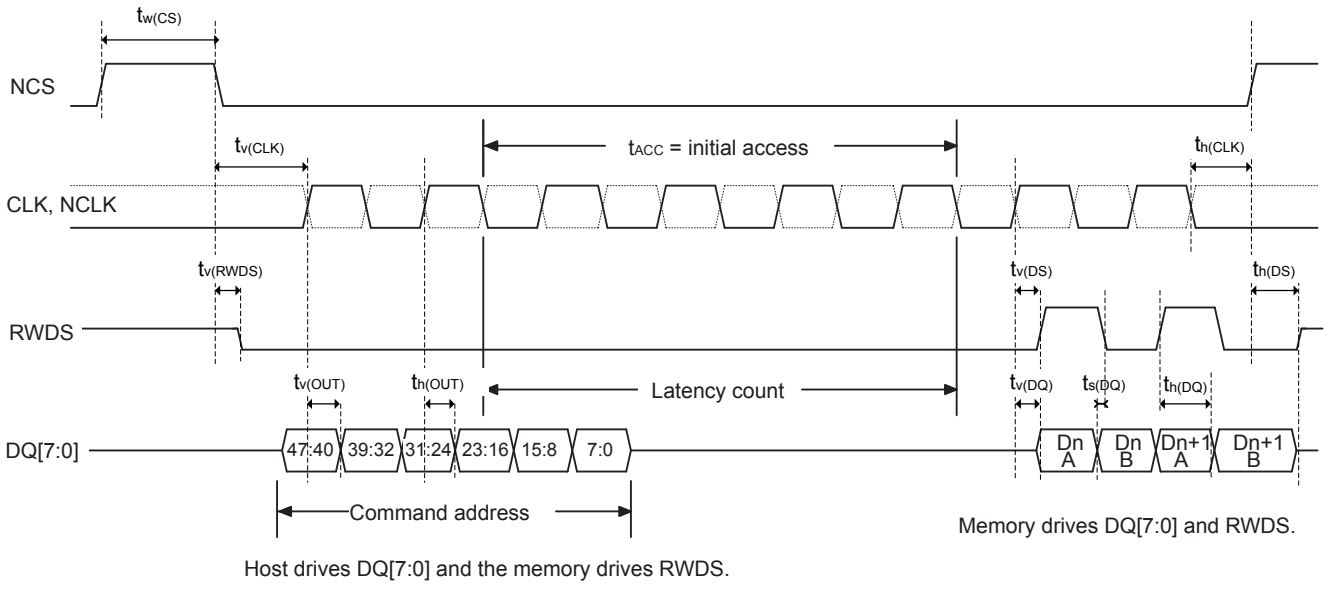
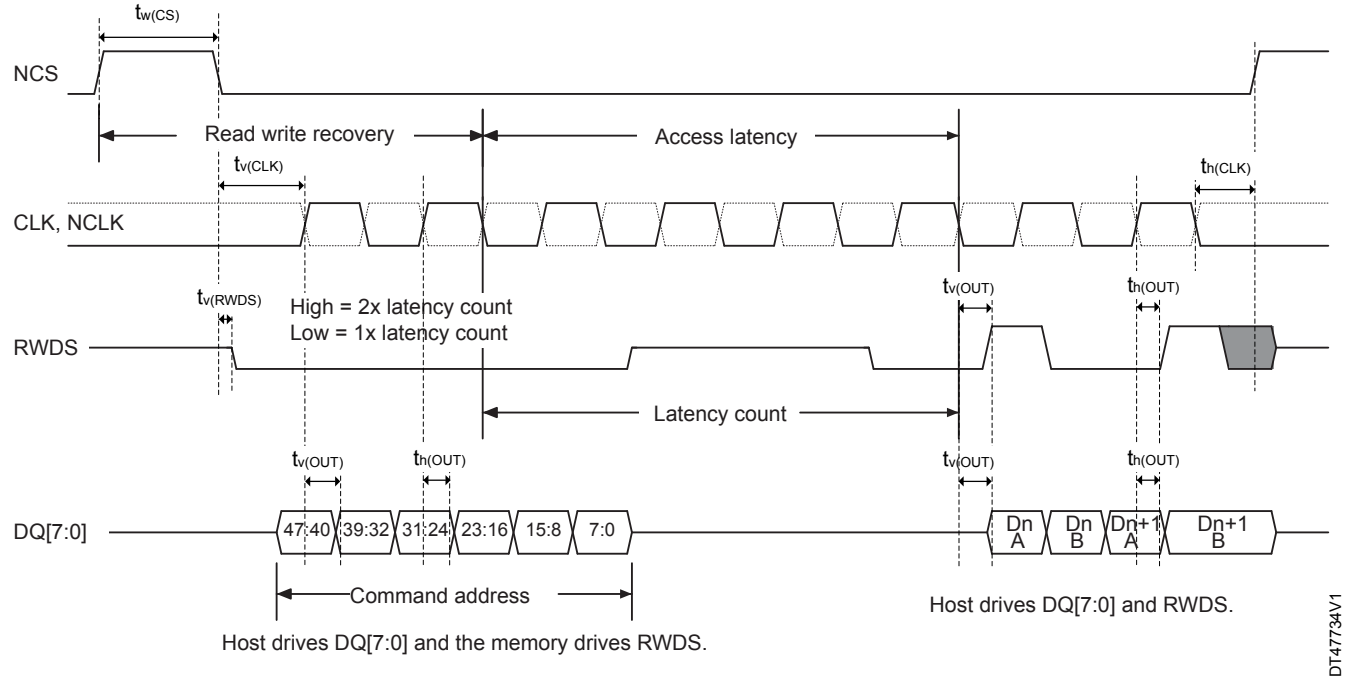


Figure 50. **XSPI HyperBus write**



5.3.20 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in Table 80. Delay block characteristics are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage summarized in Section 5.3.1: General operating conditions, with the following configuration:

Prerelease product(s)

Table 80. Delay block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{init}	Initial delay	-	1200	1440	1750	ps
t_{Δ}	Unit delay	-	42	46	48	ps

5.3.21 SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in Table 81 and Table 82 are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in Table 14. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}
- I/O Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2$ V
- VOS level set to VOS0. Refer to Section 5.3.15: I/O port characteristics for more details on the input/output characteristics.

Refer to Table 51. I/O static characteristics for more details on the input/output characteristics.

In the following tables, Tker is the period of the SDMMC kernel clock provided by the RCC (reset and clock control) unit.

Table 81. SD/eMMC characteristics (V_{DD} = 2.7 V to 3.6 V)

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	-	-	115(1)	MHz
$t_{C(CK)}$	Clock period	-	8.7	-	-	ns
$t_{W(CKL)}$	Clock low time	f_{pp} = 48 MHz	9.5	10.5	-	
$t_{W(CKH)}$	Clock high time	f_{pp} = 48 MHz	9.5	10.5	-	
CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) mode						
t_{ISU}	Input setup time HS	-	3.5	-	-	ns
t_{IHD}	Input hold time HS	-	1.5	-	-	
T_{IDW}(3)	Input valid window (variable window)	-	4.5	-	-	-
CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(2)/DDR(2) mode						
t_{OV}	Output valid time HS	-	-	(Tker / 2)	(Tker / 2) + 0.5	ns
t_{OH}	Output hold time HS	-	(Tker / 2) – 0.5	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	-	3.5	-	-	ns
t_{IHD}	Input hold time SD	-	1.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	-	-	0.5	1	ns
t_{OHD}	Output hold default time SD	-	0	-	-	

1. *With capacitive load C_L = 20 pF.*
2. *For SD 1.8 V support, an external voltage converter is needed.*
3. *Minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

Prerelease product(s)

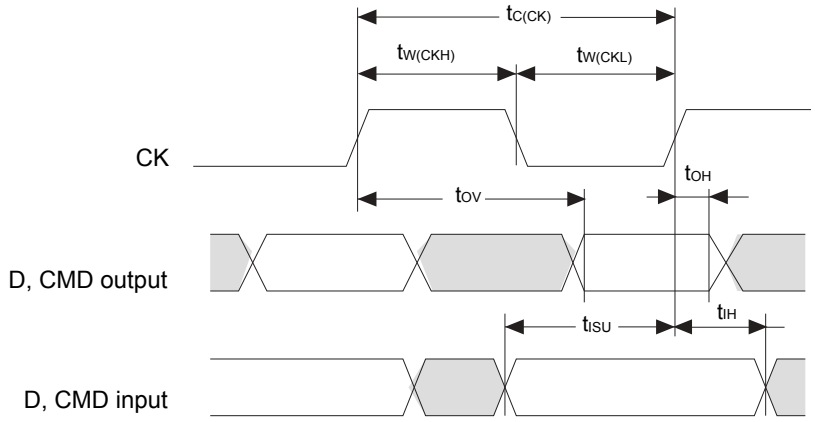
Table 82. eMMC characteristics (V_{DD} = 1.71 V to 1.9 V)

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	-	-	115(1)	MHz
$t_{C(CK)}$	Clock period	-	8.7	-	-	ns
$t_{W(CKL)}$	Clock low time	f_{pp} = 52 MHz	9.5	10.5	-	
$t_{W(CKH)}$	Clock high time	f_{pp} = 52 MHz	9.5	10.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	-	2	-	-	ns
t_{IH}	Input hold time HS	-	1.5	-	-	
t_{idw}(2)	Input valid window (variable window)	-	3	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	-	-	(Tker / 2)	(Tker / 2) + 0.5	ns
t_{OH}	Output hold time HS	-	(Tker / 2) – 0.5	-	-	

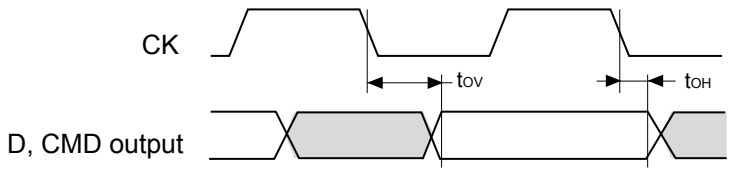
1. *With capacitive load C_L = 20 pF*
2. *Minimum window of time where the data needs to be stable for proper sampling in tuning mode.*

Figure 51. SDIO high speed mode



DT69709V1

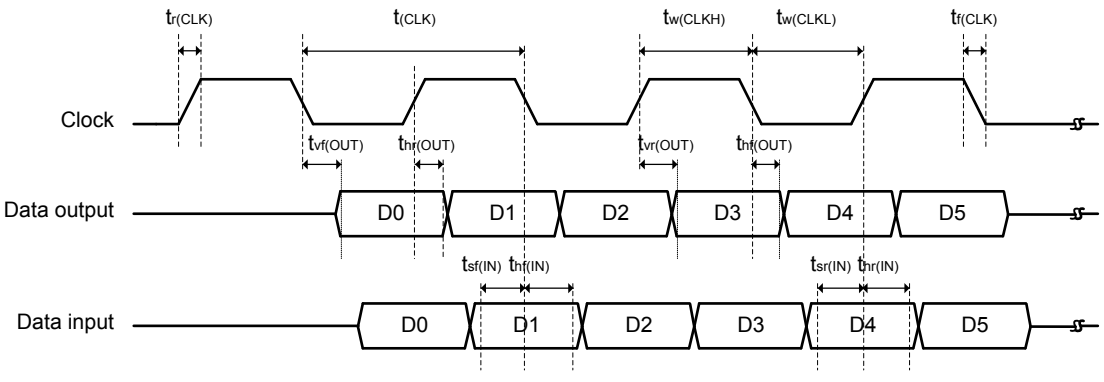
Figure 52. SD default mode



DT69710V1

Prerelease product(s)

Figure 53. **SDMMC DDR mode**



5.3.22 Analog-to-digital converter characteristics

Unless otherwise specified, the parameters given in Table 83 are derived from tests performed under the ambient temperature, f_{HCLK} frequency, and V_{DDA} supply voltage conditions summarized in Section 5.3.1: General operating conditions.

Note: It is recommended to perform an ADC calibration after each power-up.

Table 83. **12-bit ADC characteristics**

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
V_{DDA}	Analog power supply for ADC ON	-			2.5	-	3.6	V
V_{REF+}	Positive reference voltage	-			1.8	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-			V_{SSA}			
$f_{adc_ker_ck}$ (1)	ADC clock frequency	2.5 V ≤ V_{DDA} ≤ 3.6 V			1.5	-	80	MHz
f_S with RAIN = 47 Ω and C_{PCB} = 22 pF	Sampling rate for fast channels (ADCx_IN[0:5])	Resolution = 12 bits	All Modes	2.5 V ≤ V_{DDA} ≤ 3.6 V, -40°C ≤ T_J ≤ 140°C, $f_{adc_ker_ck}$ = 80 MHz, SMP = 2.5	-	5.00	-	MSPS
		Resolution = 10 bits			-	5.71	-	
		Resolution = 8 bits			-	6.67	-	
		Resolution = 6 bits			-	8.00	-	
	Sampling rate for slow channels (ADCx_IN[6:19])	Resolution = 12 bits	All modes	2.5 V ≤ V_{DDA} ≤ 3.6 V, -40°C ≤ T_J ≤ 140°C, $f_{adc_ker_ck}$ = 80 MHz, SMP = shortest possible (see Table 84. Minimum sampling time versus R_{AIN})	-	3.08	-	
		Resolution = 10 bits			-	5.00	-	
		Resolution = 8 bits			-	5.71	-	
		Resolution = 6 bits			-	8.00	-	
t_{TRIG}	External trigger period	Regular conversions	t_S + 6.5 + N		21	-	-	$1/f_{adc_ker_ck}$

Prerelease product(s)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{TRIG}	External trigger period	Injected conversions	t_S + 7.5 + N	22	-	-	$1/f_{adc_ker_ck}$
V_{AIN}	Conversion voltage range	-		0	-	V_{REF+}	V
V_{CMIV}	Common mode input voltage	Differential mode	-	V_{REF}/2 - 10%	V_{REF}/2	V_{REF}/ 2 + 10%	V
		Pseudo-differential mode	PDIFFREF=0 (reference voltage = V_{REF-})	V_{REF-}	-	V_{REF+}	V
			PDIFFREF=1 (reference voltage = V_{REF}/2)	V_{REF}/2	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	$f_{adc_ker_ck}$ = 80 MHz, t_S = 2.5, Tolerance 4 LSBs	Resolution = 12 bits, T_J = 140°C	-	-	321	-
		$f_{adc_ker_ck}$ = 80 MHz, t_S = 2.5, Tolerance 2 LSBs	Resolution = 12 bits, T_J = 125°C	-	-	220	-
			Resolution = 10 bits, T_J = 140°C	-	-	1039	-
			Resolution = 10 bits, T_J = 125°C	-	-	2100	-
			Resolution = 8 bits, T_J = 140°C	-	-	6327	-
			Resolution = 8 bits, T_J = 125°C	-	-	12000	-
			Resolution = 6 bits, T_J = 140°C	-	-	47620	-
			Resolution = 6 bits, T_J = 125°C	-	-	80000	-
C_{ADC}	Internal sample and hold capacitor	-		-	3	-	pF
$t_{ADCVREG_STUP}$	ADC LDO internal voltage regulator startup time	-		-	5	10	µs
t_{STAB}	ADC power-up time	ADC LDO internal voltage regulator already started		1	-	-	conversion cycle
t_{OFF_CAL}	Offset calibration time	-		1335			$1/f_{adc_ker_ck}$
t_{LATR}	Trigger conversion latency for regular channels without aborting the conversion	-		1	-	2	$1/f_{adc_ker_ck}$
$t_{LATRINJ}$	Trigger conversion latency for injected channels	-		2	-	3	$1/f_{adc_ker_ck}$
t_S	Sampling time	-		2.5	-	848.5	$1/f_{adc_ker_ck}$
t_{CONV}	Total conversion time (including sampling time)	N-bits resolution		t_S + 1.5 + N			$1/f_{adc_ker_ck}$

Prerelease product(s)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA_D(ADC)}$	ADC consumption on V_{DDA} and V_{REF}, Differential mode	fs = 5 MSPS	-	600	-	µA
		fs = 1 MSPS	-	190	-	
		fs = 0.1 MSPS	-	50	-	
$I_{DDA_SE(ADC)}$	ADC consumption on V_{DDA} and V_{REF} Single-ended mode	fs = 2.5 MSPS	-	500	-	
		fs = 1 MSPS	-	150	-	
		fs = 0.1 MSPS	-	50	-	
$I_{DD(ADC)}$	ADC consumption on V_{DD}	f_{ADC} = 80 MHz	-	265	-	
		f_{ADC} = 50 MHz	-	175	-	
		f_{ADC} = 25 MHz	-	90	-	
		f_{ADC} = 12,5 MHz	-	45	-	
		f_{ADC} = 6,25 MHz	-	22	-	
		f_{ADC} = 3,125 MHz	-	11	-	

1. *This frequency is the analog ADC specification, it must respect the value in Table 15. Maximum allowed clock frequencies.*
2. *For more detailed RAIN selection see Table 84. Minimum sampling time versus R_{AIN}. Maximum allowed RAIN depends from I_{leak} current for given pin (see Table 51. I/O static characteristics.*

Table 84. Minimum sampling time versus R_{AIN}

Specified by design. Not tested in production.
Tolerance for 2 LSB error. Data valid up to T_J = 140°C, with a 22 pF PCB capacitor, and V_{DDA} = 2.7 V.
Maximum allowed R_{AIN} for extra-long sampling time depends on the I_{leak} current for the given pin, causing a voltage drop across R_{AIN} (see Table 51. I/O static characteristics).

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channels(1)	Slow channels (2)
12 bits	47	3.75E-08	6.16E-08
	68	4.05E-08	6.29E-08
	100	4.59E-08	6.65E-08
	150	5.52E-08	7.23E-08
	220	6.96E-08	8.41E-08
	330	9.31E-08	1.05E-07
	470	1.24E-07	1.34E-07
	680	1.72E-07	1.79E-07
	1000	2.45E-07	2.52E-07
	1500	3.63E-07	3.67E-07
10 bits	47	3.20E-08	5.10E-08
	68	3.43E-08	5.25E-08
	100	3.82E-08	5.52E-08
	150	4.55E-08	6.06E-08
	220	5.70E-08	6.94E-08
	330	7.56E-08	8.61E-08

Prerelease product(s)

Resolution	R_{AIN} (Ω)	Minimum sampling time (s)	
		Fast channels(1)	Slow channels (2)
10 bits	470	9.96E-08	1.09E-07
	680	1.37E-07	1.45E-07
	1000	1.96E-07	2.01E-07
	1500	2.88E-07	2.91E-07
	2200	4.19E-07	4.18E-07
	3300	6.28E-07	6.23E-07
	4700	8.96E-07	8.83E-07
	6800	1.30E-06	1.27E-06
8 bits	47	2.64E-08	4.17E-08
	68	2.76E-08	4.24E-08
	100	3.02E-08	4.39E-08
	150	3.51E-08	4.66E-08
	220	4.27E-08	5.13E-08
	330	5.52E-08	6.19E-08
	470	7.17E-08	7.72E-08
	680	9.68E-08	1.00E-07
	1000	1.34E-07	1.37E-07
	1500	1.93E-07	1.94E-07
	2200	2.76E-07	2.74E-07
	3300	4.06E-07	4.01E-07
	4700	5.73E-07	5.62E-07
	6800	8.21E-07	7.99E-07
	10000	1.20E-06	1.17E-06
	15000	1.79E-06	1.74E-06
6 bits	47	2.14E-08	3.16E-08
	68	2.23E-08	3.21E-08
	100	2.40E-08	3.31E-08
	150	2.68E-08	3.52E-08
	220	3.13E-08	3.87E-08
	330	3.89E-08	4.51E-08
	470	4.88E-08	5.39E-08
	680	6.38E-08	6.79E-08
	1000	8.70E-08	8.97E-08
	1500	1.23E-07	1.24E-07
	2200	1.73E-07	1.73E-07
	3300	2.53E-07	2.49E-07
	4700	3.53E-07	3.45E-07
	6800	5.04E-07	4.90E-07
	10000	7.34E-07	7.11E-07
	15000	1.09E-06	1.05E-06

Prerelease product(s)

1. *Fast channels range from ADCx_INP0 to ADCx_INP5.*
2. *Slow channels correspond to all ADC inputs except the fast channels.*

Table 85. ADC accuracy - LDO mode

Evaluated by characterization for LQFP128 package. Not tested in production.
ADC DC accuracy values are measured after internal calibration in continuous mode.
Characterized at 1 MHz and 80 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+/-3	+/-7	LSBs
			Differential	-	+/-3	+/-6	
EO	Offset error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	-2	+0/-6	
			Differential	-	-2	+1/-5	
EG	Gain error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+3	+9	
			Differential	-	+3	+8	
ED	Differential linearity error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+/-0.75	+1.6/-1	
			Differential	-	+/-0.75	+1.7/-1	
EL	Integral linearity error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+/-2	+/-4	
			Differential	-	+/-1	+/-2.5	
ENOB	Effective number of bits	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	10	10.8	-	Bits
			Differential	11	11.5	-	
SINAD	Signal-to-noise and distortion ratio	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	62	68	-	dB
			Differential	68	71	-	
SNR	Signal-to-noise ratio	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	62	70	-	
			Differential	69	72	-	
THD	Total harmonic distortion	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-70	-75	-	
			Differential	-75	-80	-	

Table 86. ADC accuracy (ADC1) - SMPS mode

Evaluated by characterization for LQFP128 package. Not tested in production.
ADC DC accuracy values are measured after internal calibration in continuous mode.
Characterized at 1 MHz and 80 MHz.
Accuracy values are valid for all ADC pins except PD15, PD14, PD13, PD10, PD9, PD8, PB15, PB14, PB13, and PB12. For these specific pins, refer to ANXXXX.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+/-4	-	LSBs
			Differential	-	+/-4	-	
EO	Offset error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	-3	-	
			Differential	-	-3	-	
EG	Gain error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+4	-	
			Differential	-	+4	-	
ED	Differential linearity error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+/-1	-	
			Differential	-	+/-1	-	
EL	Integral linearity error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+/-2	-	
			Differential	-	+/-2	-	
ENOB	Effective number of bits	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	10.8	-	Bits

Prerelease product(s)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ENOB	Effective number of bits	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Differential	-	11.5	-	Bits
SINAD	Signal-to-noise and distortion ratio	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	68	-	dB
			Differential	-	71	-	
SNR	Signal-to-noise ratio	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	70	-	
			Differential	-	72	-	
THD	Total harmonic distortion	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	-75	-	
			Differential	-	-80	-	

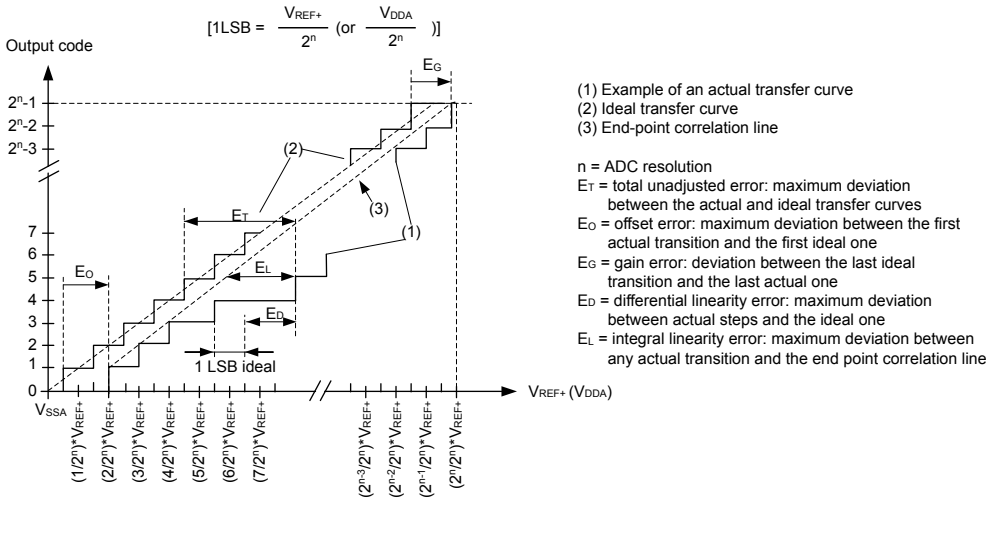
Table 87. ADC accuracy (ADC1+ADC2+ADC3+ADC4) - SMPS mode

Data evaluated by characterization for LQFP128 package. Not tested in production.
ADC DC accuracy values are measured after internal calibration in continuous mode.
Characterized at 1 MHz and 80 MHz.
Accuracy values are valid for all ADC pins except PD15, PD14, PD13, PD10, PD9, PD8, PB15, PB14, PB13, and PB12. For these specific pins, refer to ANXXXX.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ET	Total unadjusted error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+/-5	-	LSBs
			Differential	-	+/-5	-	
EO	Offset error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	-4	-	
			Differential	-	-4	-	
EG	Gain error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+/-5	-	
			Differential	-	+/-5	-	
ED	Differential linearity error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+/-1	-	
			Differential	-	+/-1	-	
EL	Integral linearity error	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	+/-2.5	-	
			Differential	-	+/-2.5	-	
ENOB	Effective number of bits	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	10.8	-	Bits
			Differential	-	11.5	-	
SINAD	Signal-to-noise and distortion ratio	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	68	-	dB
			Differential	-	71	-	
SNR	Signal-to-noise ratio	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	70	-	
			Differential	-	72	-	
THD	Total harmonic distortion	Fast and slow channels $f_{adc_ker_ck}$ = 80 MHz	Single ended	-	-70	-	
			Differential	-	-80	-	

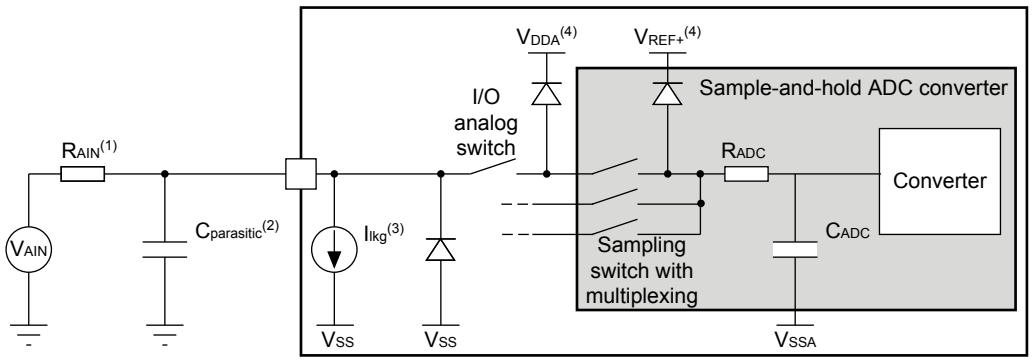
Prerelease product(s)

Figure 54. ADC accuracy characteristics



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Figure 55. Typical connection diagram when using the ADC with FT/TT pins featuring analog switch function



DT67871V3

Note:

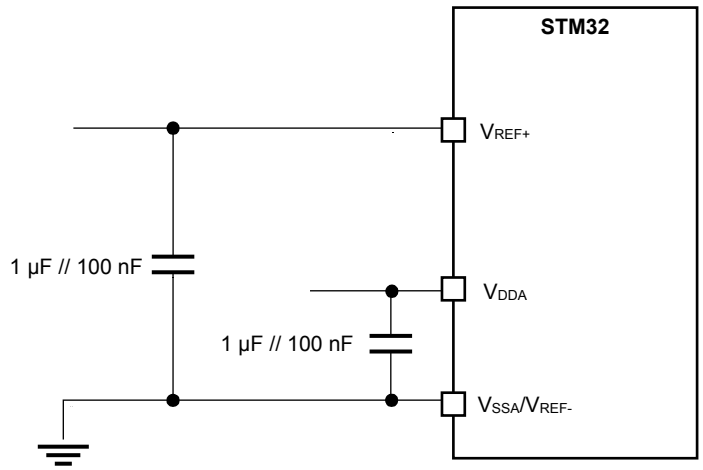
1. *Refer to Table 83. 12-bit ADC characteristics for the values of R_{AIN} and C_{ADC}.*
2. *$C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (refer to Section 5.3.15: I/O port characteristics) for the value of the pad capacitance). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{adc_ker_ck}$ should be reduced.*
3. *Refer to Section 5.3.15: I/O port characteristics for the values of I_{lkg}.*
4. *Refer to Section 5.1.6: Power supply scheme.*

General PCB design guidelines:

It is recommended to perform power supply decoupling as shown in Figure 23 or Figure 22 and Figure 56, depending on whether V_{REF+} is connected to V_{DDA} or not. The 1 µF capacitors must be ceramic (good quality), and placed as close as possible to the chip.

Prerelease product(s)

Figure 56. **Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})**



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5.3.23 DAC characteristics

Table 88. **DAC 1 characteristics**

Specified by design and not tested in production, unless otherwise specified.
Refer to Table 51. I/O static characteristics.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	3.3	3.6	V
$V_{REFDAC+}$	Positive reference voltage	-		1.62	-	V_{DDA}	
$V_{REFDAC-}$	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	Connected to V_{SSA}	5	-	-	kΩ
			Connected to V_{DDA}	25	-	-	
R_O	Output impedance	DAC output buffer OFF		9.6	11.7	13.8	
R_{BON}	Output impedance sample and hold mode, output buffer ON	DAC output buffer ON	V_{DD} = 1.62 V	-	-	1.6	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	DAC output buffer OFF	V_{DD} = 1.62 V	-	-	16.5	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		V_{SSA} + 0.2	-	V_{DDA} – 0.2	V
		DAC output buffer OFF		$V_{REFDAC-}$	-	$V_{REFDAC+}$	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value.	Normal mode DAC output buffer ON $C_L \leq$ 50pF, $R_L \geq$ 5kΩ	±0.5 LSB	-	2.05	3	µs
			±1 LSB	-	1.97	2.87	
			±2 LSB	-	1.67	2.84	
			±4 LSB	-	1.66	2.78	
			±8 LSB	-	1.65	2.7	
		Normal mode, DAC output buffer OFF, ±1LSB, C_L = 10 pF		-	1.7	2	

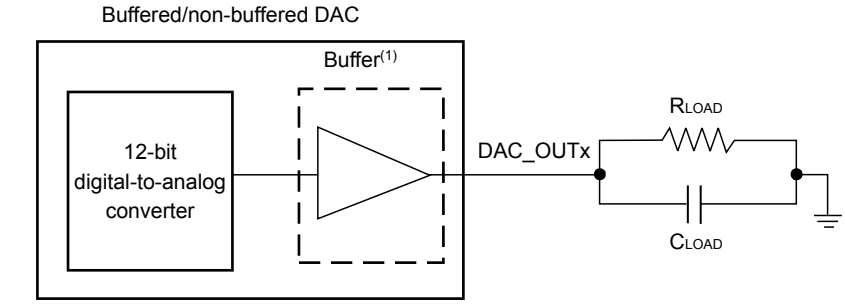
Prerelease product(s)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WAKEUP}(1)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until the ±1 LSB final value	Normal mode, DAC output buffer ON, $C_L \le 50$ pF, $R_L = 5$ kΩ		-	5	7.5	µs
		Normal mode, DAC output buffer OFF, $C_L \le 10$ pF		-	2	5.0	
PSRR	DC V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON $C_L \le 50$pF, $R_L = 5$kΩ		-	-80	-28	dB
$T_{W_to_W}$	Minimal time between two consecutive writes into the DAC_DORx register to guarantee a correct DAC_OUT for a small variation of the input code (1 LSB)	DAC_MCR:MODEx[2:0] = 000 or 001 $C_L \le 50$ pF, $R_L \ge 5$ kΩ		1	-	-	µs
		DAC_MCR: MODEx[2:0] = 010 or 011 $C_L \le 10$ pF		1.4	-	-	
t_{SAMP}	Sampling time in Sample and Hold mode. (Code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1 LSB)	DAC_OUT pin connected	DAC output buffer ON, C_{SH} = 100 nF	-	0.7	2.6	ms
			DAC output buffer OFF, C_{SH} = 100 nF	-	11.5	18.7	
		DAC_OUT pin not connected (internal connection only)	DAC output buffer OFF	-	0.3	0.6	µs
I_{leak}	Output leakage current	Sample and hold mode, DAC_OUT pin connected		-	-	-3	nA
C_{lint}	Internal sample and hold capacitor	-		1.8	2.2	2.6	pF
t_{TRIM}	Middle code offset trim time	DAC output buffer ON		50	-	-	µs
V_{offset}	Middle code offset for 1 trim code step	$V_{REFDAC+}$ = 3.6 V		-	850	-	µV
		$V_{REFDAC+}$ = .8 V		-	425	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	DAC output buffer ON	No load, middle code (0x800)	-	360	-	µA
			No load, worst code (0xF1C)	-	490	-	
		DAC output buffer OFF	No load, middle/ worst code (0x800)	-	20	-	
		Sample and hold mode, C_{SH} = 100 nF		-	360 × Ton/ (Ton+Toff)(2)	-	
I_{DDV}(DAC)	DAC consumption from $V_{REFDAC+}$	DAC output buffer ON	No load, middle code (0x800)	-	170	-	
			No load, worst code (0xF1C)	-	170	-	
		DAC output buffer OFF	No load, middle/ worst code (0x800)	-	160	-	
		Sample and Hold mode, Buffer ON, C_{SH}=100 nF (worst code)		-	170 × Ton/ (Toff+Toff)(2)	-	
		Sample and Hold mode, Buffer OFF, C_{SH}=100 nF (worst code)		-	160 × Ton/ (Toff+Toff)(2)	-	

1. *In buffered mode, the output can overshoot the final value for low input codes (starting from the minimum value).*
2. *Ton is the refresh phase duration, and Toff is the hold phase duration. For more information, see the reference manual.*

Prerelease product(s)

Figure 57. **12-bit buffered/non-buffered DAC**



(1) The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

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Table 89. **DAC 1 accuracy**

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DNL	Differential non linearity(1)	DAC output buffer ON		-2	-	2	LSB
		DAC output buffer OFF		-2	-	2	
	Monotonicity	10 bits		Guaranteed			-
INL	Integral non linearity(2)	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ		-4	-	4	LSB
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-4	-	4	
Offset	Offset error at code 0x800	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ	$V_{REFDAC+}$ = 3.6 V	-	-	±12	LSB
			$V_{REFDAC+}$ = 1.8 V	-	-	±25	
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±8	
Offset1	Offset error at code 0x001(3)	DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±5	LSB
OffsetCal	Offset error at code 0x800 after factory calibration	DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ	$V_{REFDAC+}$ = 3.6 V	-	-	±5	LSB
			$V_{REFDAC+}$ = 1.8 V	-	-	±7	
Gain	Gain error(4)	DAC output buffer ON,$C_L \le 50$ pF, $R_L \ge 5$ kΩ		-	-	±1	%
		DAC output buffer OFF, $C_L \le 50$ pF, no R_L		-	-	±1	
TUE	Total undajusted error	DAC output buffer ON $C_L \le 50$pF, $R_L \ge 5$ kΩ		-	-	±30	LSB
		DAC output buffer OFF $C_L \le 50$pF, no R_L		-	-	±12	
TUECal	Total undajusted error after calibration	DAC output buffer ON $C_L \le 50$pF, $R_L \ge 5$ kΩ		-	-	±23	LSB
SNR	Signal-to-noise ratio(5)	DAC output buffer ON $C_L \le 50$pF, $R_L \ge 5$ kΩ, 1 kHz, BW 500 kHz		-	67.8	-	dB
		DAC output buffer OFF $C_L \le 50$pF, no R_L, 1 kHz, BW 500 kHz		-	67.8	-	
THD	Total harmonic distorsion(5)	DAC output buffer ON $C_L \le 50$pF, $R_L \ge 5$kΩ, 1 kHz		-	-78, 6	-	dB
		DAC output buffer OFF $C_L \le 50$pF, no R_L, 1 kHz		-	-78, 6	-	

Prerelease product(s)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SINAD	Signal-to-noise and distorsion ratio(5)	DAC output buffer ON $C_L \le 50pF$, $R_L \ge 5\ k\Omega$, 1 kHz	-	67.5	-	dB
		DAC output buffer OFF $C_L \le 50pF$, no R_L, 1 kHz	-	67.5	-	
ENOB	Effective number of bits	DAC output buffer ON $C_L \le 50pF$, $R_L \ge 5\ k\Omega$, 1 kHz	-	10.9	-	bits
		DAC output buffer OFF $C_L \le 50pF$, no R_L, 1 kHz	-	10.9	-	

1. *Difference between two consecutive codes minus 1 LSB.*
2. *Difference between the value measured at code i and the value measured at code i on a line drawn between code 0 and the last code 4095.*
3. *Difference between the value measured at code 0x001 and the ideal value.*
4. *Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and code 0xFFF when the buffer is off, and from the code that gives 0.2.*
5. *The signal level is -0.5 dBFS with a sampling frequency of 1 MHz.*

Table 90. DAC 2-4 characteristics

Specified by design and not tested in production, unless otherwise specified.
Refer to Table 51. I/O static characteristics.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2.50	3.3	3.6	V
$V_{REFDAC+}$	Positive reference voltage	-		2.50	-	V_{DDA}	
$V_{REFDAC-}$	Negative reference voltage	-		V_{SSA}			
V_{dac_out}	Voltage on dac_out output	-		$V_{REFDAC-}$	-	$V_{REFDAC+}$	-
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value.	With one comparator on DAC output	10% - 90%	-	16	22	ns
			5% - 95%	-	21	29	
			1% - 99%	-	33	46	
			32 LSB	-	40	53	
			1 LSB	-	64	87	
		With two comparator on DAC output	10% - 90%	-	24	32	
			5% - 95%	-	32	43	
			1% - 99%	-	49	67	
			32 LSB	-	57	75	
			1 LSB	-	93	125 142	
t_{WAKEUP}	Wakeup time from off state (setting the ENx bit in the DAC control register) until the ±1 LSB final value	Normal mode, $C_L \le 10$ pF		-	1.4	3.5	µs
PSRR	V_{DDA} supply rejection ratio	-		-	-80	-60	dB
t_{SAMP}	Sampling time in sample and hold mode. (code transition between the lowest input code and the highest input code when DACOUT reaches final value ±1 LSB)	-		-	0.7	-	µs
C_{lint}	Internal sample and hold capacitor	-		1.44	1.8	2.1	pF
dV/dt (hold phase)	Voltage decay rate in sample and hold mode, during hold phase	C_{SH} = 1.8 pF, T = 55°C		-	50	-	mV/ms
V_{offset}	Middle code offset for 1 trim code step	$V_{REFDAC+}$ = 3.6 V		-	850	-	µV
		$V_{REFDAC+}$ = 1.8 V		-	425	-	
I_{DDA}(DAC)	DAC consumption from V_{DDA}	No load, middle code (0x800)		-	20	-	µA

Prerelease product(s)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDV}(DAC)	DAC consumption from $V_{REFDAC+}$	No load, middle code (0x800)	-	504	-	µA

Table 91. DAC 2-4 accuracy

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	Differential non linearity(1)	-	-2	-	2	LSB
	Monotonicity	10 bits	Guaranteed			-
INL	Integral non linearity(2)	-	-5	-	5	LSB
TUE	Total undajusted error	-	-	-	±12	LSB
DCS_d	Dynamic code spike	Spike amplitude on DAC voltage when DAC output value is decreasing	-	0	2	LSB
DCS_i	Dynamic code spike	Spike amplitude on DAC voltage when DAC output value is increasing	-	0	4	LSB

1. *Difference between the value measured at code i and the value measured at code i on a line drawn between code 0 and the last code 4095.*
2. *Difference between the value measured at code 0x001 and the ideal value.*

5.3.24 Analog temperature sensor characteristics

Table 92. Analog temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature (from V_{SENSOR} voltage)	-	-	3	°C
	V_{SENSE} linearity with temperature (from ADC counter)	-	-	3	
Avg_Slope(2)	Average slope (from V_{SENSOR} voltage))	-	2	-	mV/°C
	Average slope (from ADC counter)	-	2	-	
V30(3)	Voltage at 30°C ± 5 °C	-	0.62	-	V
t_{start_run}(1)	Startup time in Run mode (buffer startup)	-	-	25.2	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	9	-	-	
I_{sens}(1)	Sensor consumption	-	0.18	0.31	µA
$I_{sensbuf}$(1)	Sensor buffer consumption	-	3.8	6.5	

1. *Specified by design. Not tested in production.*
2. *Evaluated by characterization. Not tested in production.*
3. *Measured at V_{DDA} = 3.3 V ±10 mV. The V30 ADC conversion result is stored in the TS_CAL1 byte.*

Table 93. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	Temperature sensor raw data acquired value at 30 °C, V_{DDA} = 3.3 V	0x08FF F814 - 0x08FF F815
TS_CAL2	Temperature sensor raw data acquired value at 140 °C, V_{DDA} = 3.3 V	0x08FF F818 - 0x08FF F819

Prerelease product(s)

5.3.25 Digital temperature sensor characteristics

Table 94. Digital temperature sensor characteristics

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DTS}(1)	Output clock frequency	-	500	750	1150	kHz
T_{LC}(1)	Temperature linearity coefficient	VOS2	1660	2100	2750	Hz/°C
T_{TOTAL_ERROR}(1)	Temperature offset measurement, all VOS	T_J = -40°C to 30°C	-13	-	4	°C
		T_J = 30°C to 140°C	-7	-	2	
T_{VDD_CORE}	Additional error due to supply variation	VOS2	0	-	0	°C
		VOS0, VOS1	-1	-	1	
t_{TRIM}	Calibration time	-	-	-	2	ms
t_{WAKE_UP}	Wake-up time from off state until DTS ready bit is set	-	-	67	116	µs
I_{DDCORE_DTS}	DTS consumption on VDD_CORE	-	8.5	30	70	µA

1. *Evaluated by characterization. Not tested in production.*

5.3.26 V_{CORE} monitoring characteristics

Table 95. V_{CORE} monitoring characteristics

Specified by design. Not tested in production.

Symbol	Parameter	Min	Typ	Max	Unit
T_{S_VCORE}	ADC sampling time when reading the V_{CORE} voltage	1	-	-	µs

5.3.27 Temperature monitoring

Table 96. Temperature monitoring characteristics

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit
$TEMP_{high}$	High temperature monitoring	130	135	140	°C
$TEMP_{low}$	Low temperature monitoring	-40	-35	-30	

5.3.28 V_{REFBUF} characteristics

Table 97. V_{REFBUF} characteristics

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode V_{DDA} = 3.3 V	VRS = 000	3.135	3.3	3.6	V
			VRS = 001	2.8	-	3.6	
			VRS = 010	2.7	-	3.6	
			VRS = 011	2.7	-	3.6	
		Degraded mode(1)	VRS = 000	2.7	-	3.135	
			VRS = 001	2.7	-	2.8	
			VRS = 010	-	-	-	

Prerelease product(s)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Degraded mode(1)	VRS = 011	-	-	-	V
V_{REFBUF_OUT}	Voltage reference buffer output	Normal mode at 30°C, I_{LOAD} = 100 µA	VRS = 000		2.9000		
			VRS = 001	2,498	2.5000	2,5035(2)	
			VRS = 010	2.0460	2.0490	2.0520	
			VRS = 011	1.8010	1.8040	1.8060	
		Degraded mode(1)	VRS = 000	V_{DDA} - 150 mV	-	V_{DDA}	
			VRS = 001	V_{DDA} - 150 mV	-	V_{DDA}	
			VRS = 010	-	-	-	
			VRS = 011	-	-	-	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
C_L	Load capacitor	-	-	0.5	1	1.50	uF
esr	Equivalent serial resistor of C_L	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{LOAD} = 500 µA	-	200	-	ppm/V
			I_{load} = 4 mA	-	100	-	
I_{load_reg}	Load regulation	500 µA ≤ I_{LOAD} ≤ 4 mA	Normal Mode	-	50	-	ppm/ mA
T_{coeff}	Temperature coefficient	−40°C < T_J < +140°C	-	-	-	T_{coeff} V_{REFINT} + 100	ppm/ °C
PSRR	Power supply rejection	DC	-	-	60	-	dB
		100 kHz	-	-	40	-	
t_{START}	Start-up time	C_L = 0.5 µF	-	-	300	-	µs
		C_L = 1 µF	-	-	500	-	
		C_L = 1.5 µF	-	-	650	-	
I_{INRUSH}	Control of maximum DC current drive on V_{REFBUF_OUT} during startup phase(3)	-		-	8	-	mA
$I_{DDA(VREFBUF)}$	VREFBUF consumption from V_{DDA}	I_{LOAD} = 0 µA	-	-	15	25	µA
		I_{LOAD} = 500 µA	-	-	16	30	
		I_{LOAD} = 4 mA	-	-	32	50	

1. *In degraded mode, the voltage reference buffer cannot maintain the output voltage (V_{DDA} minus drop voltage) accurately.*
2. *Evaluated by characterization. Not tested in production.*
3. *To control the V_{REFBUF} I_{INRUSH} current during startup and scaling changes, ensure that the VDDA voltage is in the range of 2.7 V to 3.6 V.*

Prerelease product(s)

5.3.29 Comparator characteristics

Table 98. COMP characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		2.5	3.3	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	
V_{BG}(1)	Scaler input voltage	-		V_{REFINT}			
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	800	1000	
t_{START_SCALER}	Scaler startup time	-		-	140	250	µs
t_{START}	Comparator startup time to reach propagation delay specification	PWRMODE[1:0]=0(2)		-	2	5	µs
t_D(3)	Propagation delay for 200 mV step with 100 mV overdrive	50 pF load	DGLT = 0	-	14	30	ns
		PWRMODE[1:0] = 0(2)	DGLT = 1	-	20	50	
V_{offset}	Comparator offset error	Full common mode range		-2.5	-	3	mV
V_{hys}	Comparator hysteresis	HYST[2:0] = 0		-	0	-	mV
		HYST[2:0] = 1		6	10	13	
		HYST[2:0] = 2		13	20	25	
		HYST[2:0] = 3		22	30	37	
		HYST[2:0] = 4		30	40	50	
		HYST[2:0] = 5		40	50	63	
		HYST[2:0] = 6		58	73	90	
		HYST[2:0] = 7		78	95	118	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Static		-	500	680	µA
		With 50 kHz ±100 mV overdrive square signal		-	500	-	

1. *Refer to Table 20. Embedded reference voltage.*
2. *PWRMODE[1:0] > 0 is not supported on this product.*
3. *Evaluated by characterization and not tested in production.*

5.3.30 Audio digital filter (ADF) characteristics

Unless otherwise specified, the parameters given in Table 99 are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in Table 14. General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}
- IO compensation cell activated.
- HSLV activated when V_{DD} ≤ 2.7 V
- Voltage scaling range 1

Refer to Table 51. I/O static characteristics for more details on the input/output characteristics.

Prerelease product(s)

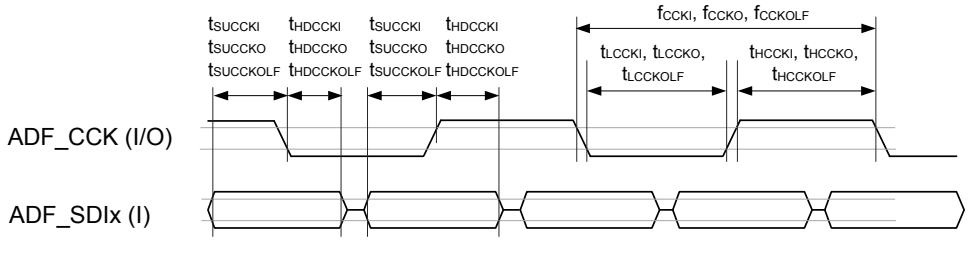
Table 99. ADF timing measurements

Evaluated by characterization, not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CCKI}	Input clock frequency via ADF_CCK[1:0] pin, in SLAVE_SPI mode	1.71 V ≤ V_{DD} ≤ 3.6 V	-	-	25	MHz
f_{CCKO}	Output clock frequency in MASTER_SPI	2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	25/10(1)	MHz
		1.71 V ≤ V_{DD} ≤ 3.6 V	-	-	25/4(1)	
f_{CCKOLF}	Output clock frequency in LF_MASTER_SPI	2.7 V ≤ V_{DD} ≤ 3.6 V	-	-	5	MHz
		1.71 V ≤ V_{DD} ≤ 3.6 V	-	-	5/4(1)	
f_{SYMB}	Input symbol rate in MANCHESTER mode	-	-	-	20	MHz
t_{HCCKI}, t_{LCCKI}	ADF_CCK[1:0] input clock high and low time	In SLAVE_SPI mode	2 × Tadf_proc_ck(2)	-	-	ns
t_{HCCKO}, t_{LCCKO}	ADF_CCK[1:0] output clock high and low time	In MASTER_SPI mode	2 × Tadf_proc_ck(2)	-	-	
$t_{HCCKOLF}$, $t_{LCCKOLF}$	ADF_CCK[1:0] output clock high and low time	In LF_MASTER_SPI mode	Tadf_proc_ck(2)	-	-	
t_{SUCCKI}	Data setup time w.r.t. ADF_CCK[1:0] input	In SLAVE_SPI mode: ADF_CCK[1:0] configured in input, measured on rising and falling edge	2	-	-	
t_{HDCCKI}	Data hold time w.r.t. ADF_CCK[1:0] input		1	-	-	
t_{SUCCKO}	Data setup time w.r.t. ADF_CCK[1:0] output	In MASTER_SPI mode: ADF_CCK[1:0] configured in output, measured on rising and falling edge	3.5/5.7(1)	-	-	
t_{HDCCKO}	Data hold time w.r.t. ADF_CCK[1:0] output		0.5	-	-	
$t_{SUCCKOLF}$	Data setup time w.r.t. ADF_CCK[1:0] output	In LF_MASTER_SPI mode: ADF_CCK[1:0] configured in output, measured on rising and falling edge	11.5/64(1)	-	-	
$t_{HDCCKOLF}$	Data hold time w.r.t. ADF_CCK[1:0] output		0	-	-	

1. *When using PA8/PA9.*
2. *Tadf_proc_ck is the period of the ADF processing clock.*

Figure 58. ADF timing diagram



5.3.31 Timer characteristics

The parameters given in Table 100 are specified by design.

Refer to Section 5.3.15: I/O port characteristics for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

IDTBL00-9179

Prerelease product(s)

Prerelease product(s)

Table 100. TIMx characteristics

TIMx is a general term in which x represents 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 15, 16, 17, or 20.

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{RES(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 520 MHz	1.92	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 520 MHz	0	260	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2, TIM3, TIM4 and TIM5)	-	16	bits
		TIM2, TIM3, TIM4 and TIM5	-	32	
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 520 MHz	1.92	126031	ns
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	TIM2, TIM3, TIM4 and TIM5	-	2^{32}	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 520 MHz	-	8.26	s
f_{ENC}	Encoder frequency on TI1 and TI2 input pins	-	0	$f_{TIMxCLK}/4$	MHz
		$f_{TIMxCLK}$ = 520 MHz	0	130	MHz
$t_{W(INDEX)}$	Index pulse width on ETR input	-	2	-	$t_{TIMxCLK}$
$t_{W(TI1,TI2)}$	Pulse width on TI1 and TI2 inputs in all encoder modes except directional clock x1	-	2	-	$t_{TIMxCLK}$
	Pulse width on TI1 and TI2 inputs in directional clock x1 mode	-	3	-	$t_{TIMxCLK}$

Table 101. IWDG min/max timeout period at 32 kHz (LSI)

The exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0] = 0x000	Max timeout RL[11:0] = 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

Table 102. WWDG min/max timeout value at 280 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.014625	0.936	ms
2	1	0.02925	1.872	
4	2	0.0585	3.744	
8	3	0.117	7.488	

5.3.32 Low-power timer characteristics

Table 103. LPTIMx characteristics

LPTIMx is a general term in which x represents 1 to 6.

Symbol	Parameter	Min	Max	Unit
$t_{RES(TIM)}$	Timer resolution time	1	-	$t_{LPTIM_KER_CK}$
$f_{LPTIM_KER_CK}$	Timer kernel clock	0	130	MHz
f_{EXT}	Timer external clock frequency on input1 and input2	0	$f_{LPTIM_KER_CK}/3$	MHz
Res_{TIM}	Timer resolution	-	16	bits
t_{MAX_COUNT}	Maximum possible count	-	65536	$t_{LPTIM_KER_CK}$

5.3.33 High resolution timer

The parameters given in Table 104 are derived from tests performed under ambient temperature and supply voltage conditions summarized in Section 5.3.1: General operating conditions.

Table 104. HRTIM characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_A	Timer ambient temperature range	f_{HRTIM} = 435 MHz	-40	-	125	°C
$t_{RES(HRTIM)}$	High resolution step size	f_{HRTIM} = 520 MHz, T_A from -40 to 105°C	-	1.92	-	ns
Res_{HRTIM}	Timer resolution	-	-	-	16	bit
t_{DTG}	Dead time generator clock period	-	0.125	-	16	t_{HRTIM}
		f_{HRTIM} = 520 MHz	1.92	-	30.8	ns
$\|t_{DTR}\|/\|t_{DTF}\|$ max	Dead time range (absolute value)	-	-	-	511	t_{DTG}
		f_{HRTIM} = 520 MHz	-	-	15723	ns
f_{CHPFRQ}	Chopper stage clock frequency	-	1/256	-	1/16	f_{HRTIM}
		f_{HRTIM} = 520 MHz	2.03	-	32.5	MHz
f_{1STPW}	Chopper first pulse length	-	16	-	256	t_{HRTIM}
		f_{HRTIM} = 520 MHz	30.8	-	492	ns

Table 105. HRTIM output response to fault protection

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
$t_{LAT(DF)}$	Digital fault response latency	Propagation delay from HRTIM_FLTx digital input to HRTIM_CHxy output pin	-	9	20	ns
$t_{W(FLT)}$	Minimum fault pulse width	-	7	-	-	
$t_{LAT(AF)}$	Analog fault response latency	Propagation delay from COMPx_INP input pin to HRTIM_CHxy output pin	-	16	31	

1. *Evaluated by characterization. Not tested in production.*

Prerelease product(s)

Table 106. HRTIM output response to external events 1 to 5 (low-latency mode)

The EEXFAST bit in the HRTIM_EECR1 register is set to enable low latency mode. This function is available on external event channels 1 to 5.

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIM_EEVx digital input to HRTIM_CHxy output pin (30pF load)	-	12	22	ns
$t_{W(EEV)}$	Minimum external event pulse width	-	7	-	-	
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from COMPx_INP input pin to HRTIM_CHxy output pin (30pF load)	-	18	22	

1. *Evaluated by characterization. Not tested in production.*

Table 107. HRTIM output response to external events 1 to 10 (synchronous mode)

The EXFAST bit in the HRTIM_EECR1 or HRTIM_EECR2 register is cleared to enable synchronous mode. External event filtering is disabled; that is, EExF[3:0] = 0000 in the HRTIM_EECR2 register.

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from HRTIM_EEVx digital input to HRTIM_CHxy output pin (30 pF load)	-	12	22	ns
$t_{W(EEV)}$	Minimum external event pulse width	-	7	-	-	
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from COMPx_INP input pin to HRTIM_CHxy output pin (30 pF load)(2)	-	18	22	
$t_{JIT(EEV)}$	External event response jitter	Jitter of the delay from HRTIM_EEVx digital input or COMPx_INP to HRTIM_CHxy output pin	-	-	1	t_{HRTIM}(3)

1. *Evaluated by characterization. Not tested in production.*
2. *This parameter is specified for f_{HRTIM} = 400 MHz.*
3. *t_{HRTIM} = 1/f_{HRTIM} with f_{HRTIM} = 400 MHz.*

Table 108. HRTIM synchronization input / output

Specified by design and not tested in production, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{W(SYNCIN)}$	Minimum pulse width on SYNCIN inputs, including HRTIM_SCIN	-	2	-	-	t_{HRTIM}
$t_{RES(ESR)}$	Response time to external synchronization request	-	-	-	3	t_{HRTIM}
$t_{W(SYNCOUT)}$	Pulse width on HRTIM_SCOUT output	-	-	16	-	t_{HRTIM}
		f_{HRTIM} = 520 MHz	-	30.8	-	ns

5.3.34 Communication interfaces

I²C interface characteristics

The I²C interface meets the timings requirements of the I²C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s
- SMBUS 2.0 specifications
- SMBUS 3.3 specifications (on FT_fhb I/O)

The I²C timings requirements are specified by design, not tested in production, when the I²C peripheral is properly configured (refer to the product reference manual).

Prerelease product(s)

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but still present. Only FT_f I/O pins support Fm+ low level output current maximum requirement. Refer to Section 5.3.15: I/O port characteristics for the I2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter, refer to Table 109. I^2C analog filter characteristics for its characteristics.

Table 109. I^2C analog filter characteristics

Evaluated by characterization. Not tested in production.
Measurement points are done at 50% V_{DD}.

Symbol	Parameter	Min	Max	Unit
t_{AF}	Maximum pulse width of spikes suppressed by analog filter	50(1)	180(2)	ns

1. *Spikes with widths less than $t_{AF(min)}$ are filtered.*
2. *Spikes with widths greater than $t_{AF(max)}$ are not filtered.*

USART interface characteristics

Unless otherwise specified, the parameters given in Table 110. USART characteristics are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Section 5.3.1, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- VOS level set to VOS0
- HSLV activated when $V_{DD} \leq 2.7$ V

Refer to Section 5.3.15: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

Table 110. USART characteristics

Evaluated by characterization. Not tested in production.

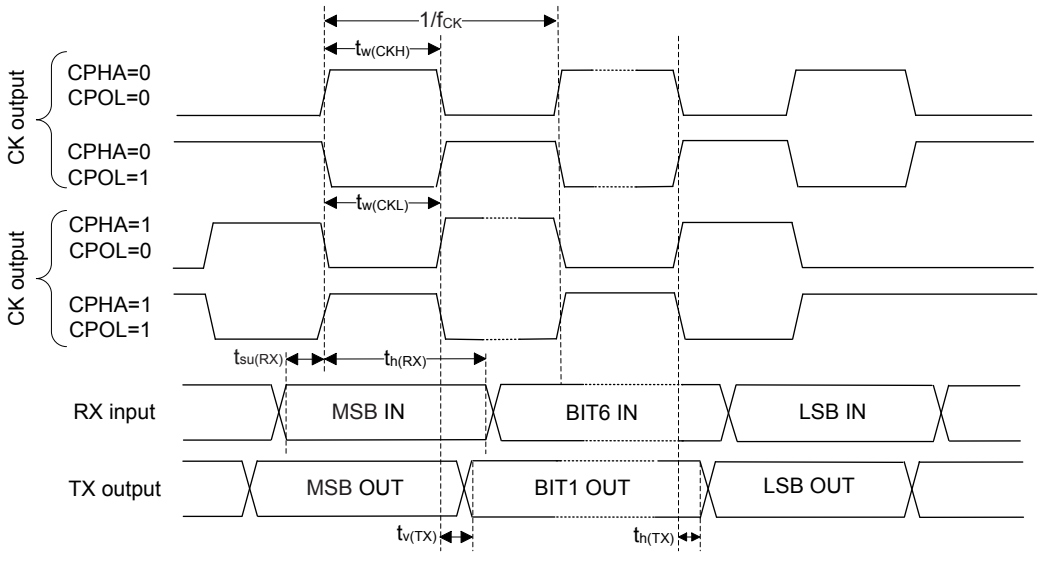
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	15.5/4(1)	MHz
		Slave receiver			41.5	
		Slave transmitter			35.5/4(1)	
T_{CK}	USART clock period	Master mode	$1000/f_{CK}$	-	-	ns
		Slave receiver	24.1			
		Slave transmitter	$1000/f_{CK}$			
$t_{su(NSS)}$	NSS setup time	Slave mode	T_{ck} + 2.5	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode	1	-	-	
$t_{w(CKH)}$ $t_{w(CKL)}$	CK high and low time	Master mode	$T_{ck}/2$ -1	$T_{ck}/2$	$T_{ck}/2$ +1	
$t_{su(RX)}$	Data input setup time	Master mode	13	-	-	
		Slave mode	4	-	-	
$t_{h(RX)}$	Data input hold time	Master mode	0	-	-	
		Slave mode	0.5	-	-	

Prerelease product(s)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(TX)}$	Data output valid time	Master mode	-	1.5	2/87(1)	ns
		Slave mode	-	12	14/115(1)	
$t_{h(TX)}$	Data output hold time	Slave mode	1	-	-	
		Master mode	9	-	-	

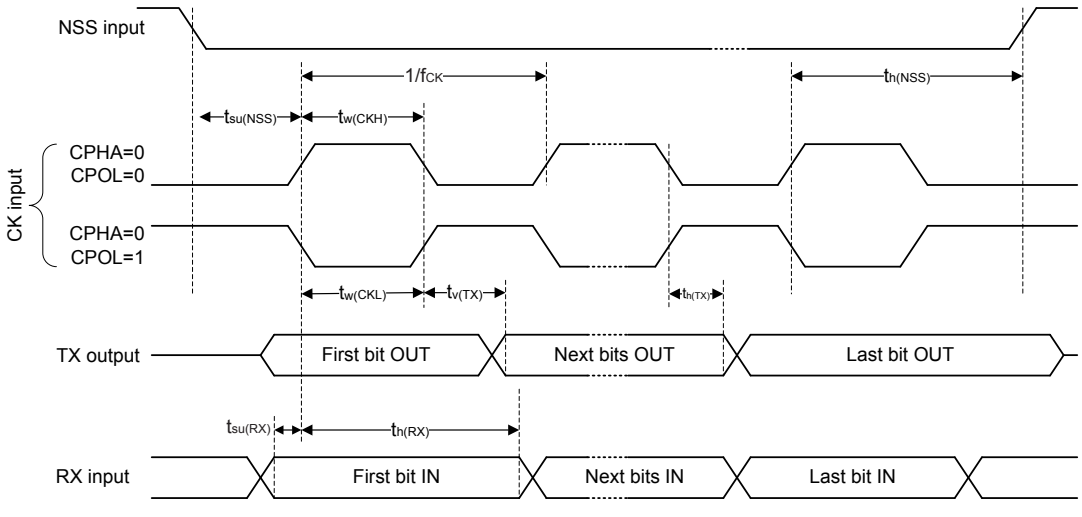
1. *When using PA9.*

Figure 59. USART timing diagram in Master mode



1. *Measurement points are done at 0.5V_{DD} and with external C_L = 30 pF.*

Figure 60. USART timing diagram in Slave mode



I3C interface characteristics

The I3C interface meets the timings requirements of the MIPI® I3C specification v1.1.
The I3C peripheral supports:

Prerelease product(s)

- I3C SDR-only as controller
- I3C SDR-only as target
- I3C SCL bus clock frequency up to 12.5 MHz

The parameters given in Table 111. I3C open-drain measured timing are obtained with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- I/O compensation cell activated
- HSLV activated when $V_{DD} \leq 2.7$ V

The timings are in line with MIPI specification, except for the ones given in Table 111. I3C open-drain measured timing and Table 112. I3C push-pull measured timing. For t_{SU_OD} this can be mitigated by increasing the corresponding SCL low duration in the I3C_TIMINGR0 register. For t_{SCO} this can be mitigated by enabling and adjusting the clock stall time both on the address ACK phase and on the data read Tbit phase in the I3C_TIMINGR2 register. This can also be mitigated by increasing the SCL low duration in the I3C_TIMINGR0 register. For further details refer to AN5879.

Table 111. I3C open-drain measured timing

Symbol	Parameter	Conditions	I3C open drain mode (specification)		Timing measurements	Unit
			Min	Max		
t_{SU_OD}	SDA data setup time in open drain mode	Controller 1.71 V < V_{DD} < 3.6 V	3	-	Tker(1) + 18	ns

1. *Tker is the period of the I3C kernel clock provided by the RCC (reset and clock control) unit.*

Table 112. I3C push-pull measured timing

Symbol	Parameter	Conditions	I3C push-pull mode (specification)		Timing measurements	Unit
			Min	Max		
t_{SCO}	Clock in to data out for target	Target 2.7 V < V_{DD} < 3.6 V	-	12	12	ns
		Target 1.71 V ≤ V_{DD} ≤ 2.7 V			30	

SPI interface characteristics

Unless otherwise specified, the parameters given in Table 113. SPI characteristics are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Section 5.3.1, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- VOS level set to VOS0
- HSLV activated when V_{DD} < 2.7 V

Refer to Section 5.3.15: I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 113. SPI characteristics

Evaluated by characterization. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	Master mode 1.71 V < V_{DD} < 3.6 V	-	-	85	MHz

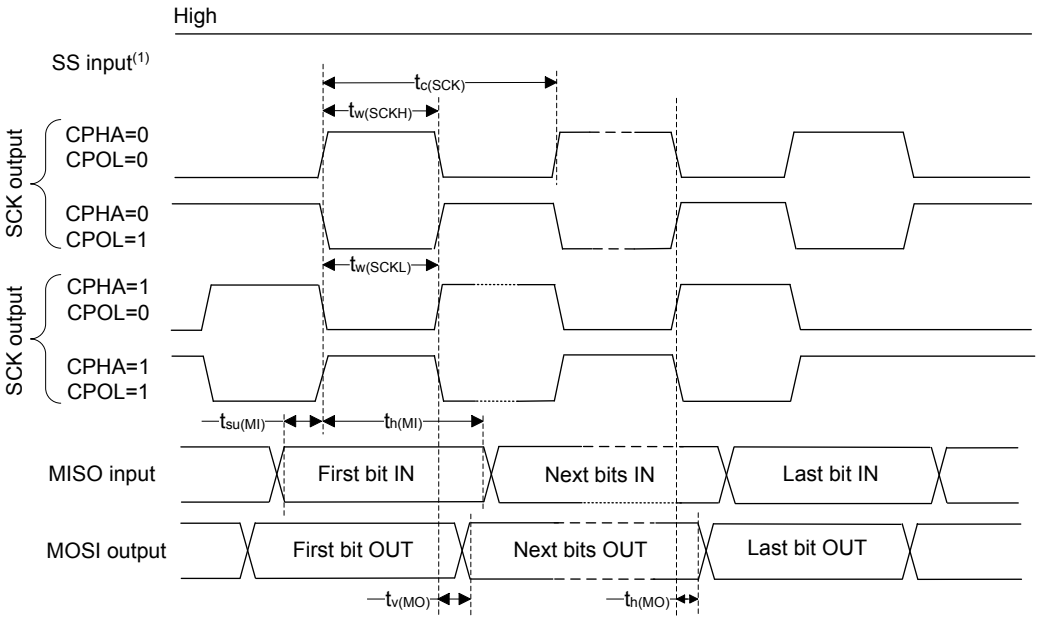
Prerelease product(s)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SPI clock frequency	SPI 1, 4, 5, 6	-	-		MHz
		Master mode 1.71 V < V_{DD} < 3.6 V SPI 2, 3			80	
		Master mode 2.7 V < V_{DD} < 3.6 V SPI 2, 3, 4, 5			130	
		Master mode 2.7 V < V_{DD} < 3.6 V SPI 1, 6			125	
		Slave receiver mode 1.71 V < V_{DD} < 3.6 V			125	
		Slave mode transmitter/full duplex 1.71 V < V_{DD} < 3.6 V			35.5	
		Slave mode transmitter/full duplex 2.7 V < V_{DD} < 3.6 V			41.5	
$t_{c(SCK)}$	SPI clock period	-	-	$1000/f_{SCK}$	-	ns
$t_{su(NSS)}$	NSS setup time	Slave mode	4/6.5(1)	-	-	
$t_{h(NSS)}$	NSS hold time	Slave mode	2/3.5(1)			
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode Prescaler = 2	$t_{c(SCK)}/2$ - 1	$t_{c(SCK)}/2$	$t_{c(SCK)}/2$ + 1	
$t_{su(MI)}$	Data input setup time	Master mode	3.5	-	-	
$t_{su(SI)}$		Slave mode	2			
$t_{h(MI)}$	Data input hold time	Master mode	0.5			
$t_{h(SI)}$		Slave mode	1.5			
$t_{a(SO)}$	Data output access time	Slave mode	9.5	12.5/14(1)	17.5/20(1)	
$t_{dis(SO)}$	Data output disable time	Slave mode	6.5	9/10.5(1)	13/15.5(1)	
$t_{v(SO)}$	Data output valid time	Slave mode 2.7 V < V_{DD} < 3.6 V	-	8.5	12	
		Slave mode 1.71 V < V_{DD} < 3.6 V		8.5	14	
$t_{v(MO)}$		Master mode 1.71 V < V_{DD} < 3.6 V		1	1.5	
$t_{h(SO)}$	Data output hold time	Slave mode	6	-	-	
$t_{h(MO)}$		Master mode	0			

1. *When using PC13.*

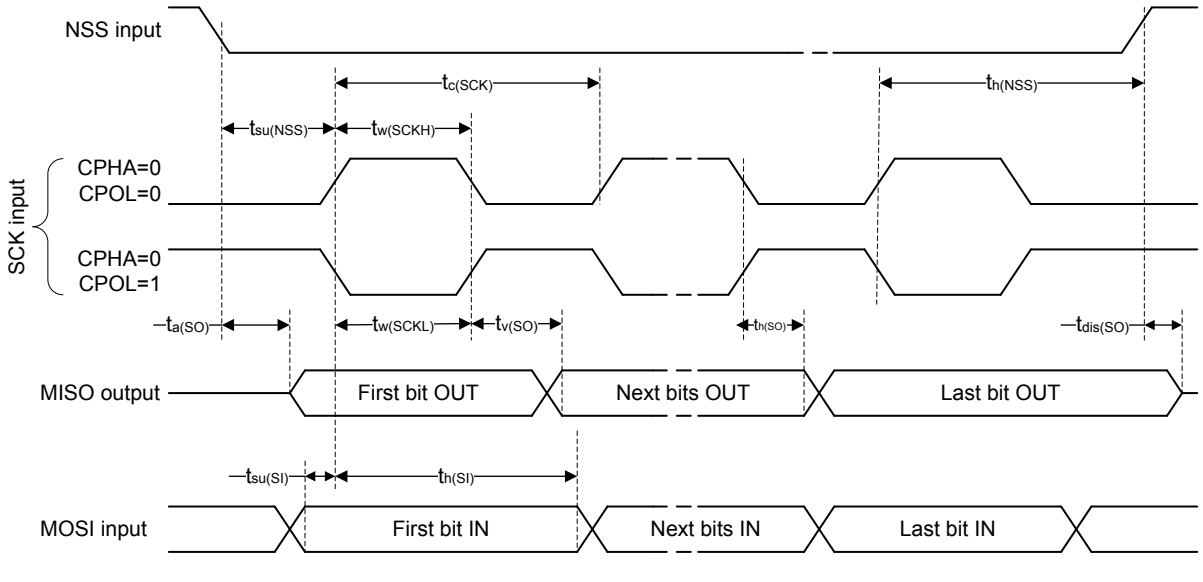
Prerelease product(s)

Figure 61. **SPI timing diagram - Master mode**



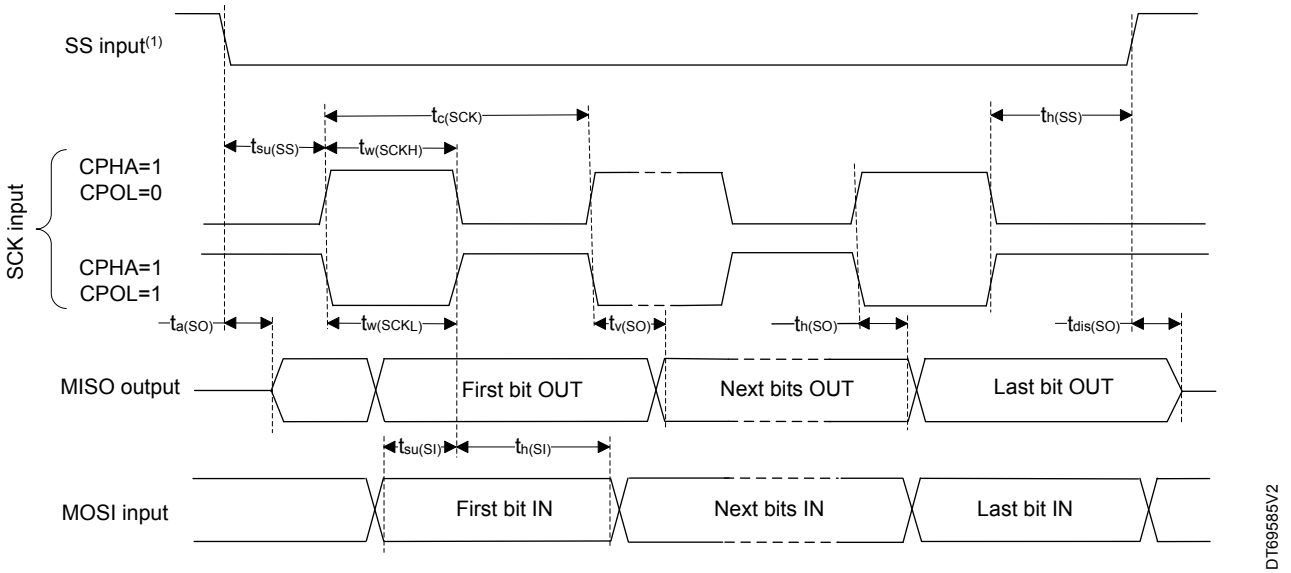
1. *The SS input can be configured to active low or active high.*

Figure 62. **SPI timing diagram - Slave mode and CPHA = 0**



Prerelease product(s)

Figure 63. **SPI timing diagram - Slave mode and CPHA = 1**



1. *The SS input can be configured to active low or active high.*

I²S interface characteristics

Unless otherwise specified, the parameters given in Table 114. I²S dynamic characteristics are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in Section 5.3.1, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L = 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}
- I/O compensation cell activated
- VOS level set to VOS0

Refer to Section 5.3.15: I/O port characteristics for more details on the input/output alternate function characteristics (CK,SD,WS).

Table 114. **I²S dynamic characteristics**

Evaluated by characterization. Not tested in production.

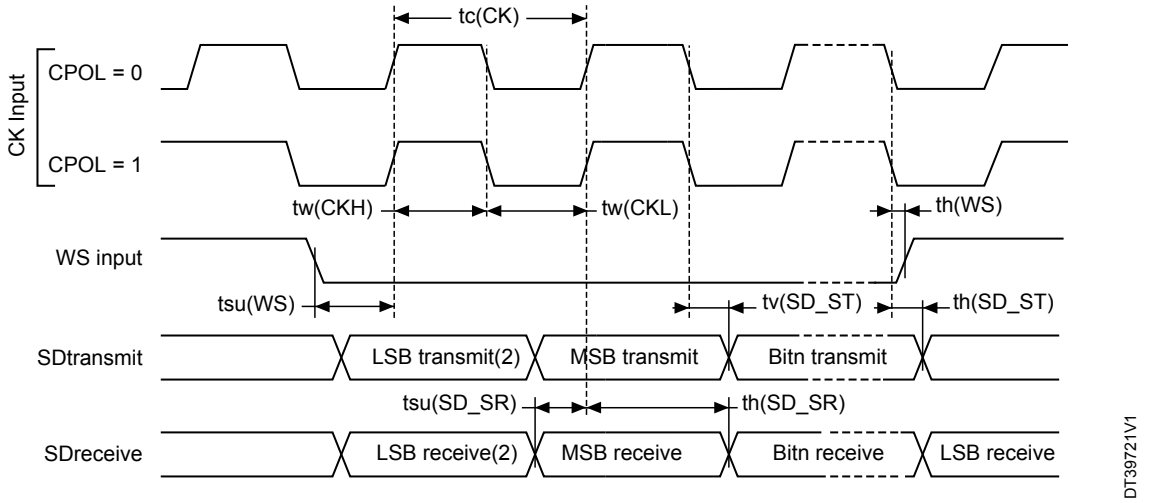
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I²S main clock output	-	-	50	MHz
f_{CK}	I²S clock frequency	Master receiver	-	50/31.5(1)	
		Master transmitter	-	50/31.5(1)	
		Slave receiver	-	50	
		Slave transmitter	-	21	
$t_{c(CK)}$	I²S clock period	Master receiver	20/31.75(1)	-	ns
		Master transmitter	20/31.75(1)	-	
		Slave receiver	20	-	
		Slave transmitter	48	-	
$t_{v(WS)}$	WS valid time	Master mode	-	2.5/9.5(1)	ns
$t_{h(WS)}$	WS hold time		0.5	-	

Prerelease product(s)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su(WS)}$	WS setup time	Slave mode	2.5	-	ns
$t_{h(WS)}$	WS hold time		2	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	3.5	-	
$t_{su(SD_SR)}$		Slave receiver	2	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	0.5	-	
$t_{h(SD_SR)}$		Slave receiver	1.5	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after CK↓)	-	14	
$t_{v(SD_MT)}$		Master transmitter (after CK↓)	-	1.5	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after CK↓)	6	-	
$t_{h(SD_MT)}$		Master transmitter (after CK↓)	0.5	-	

1. *When using PC13.*

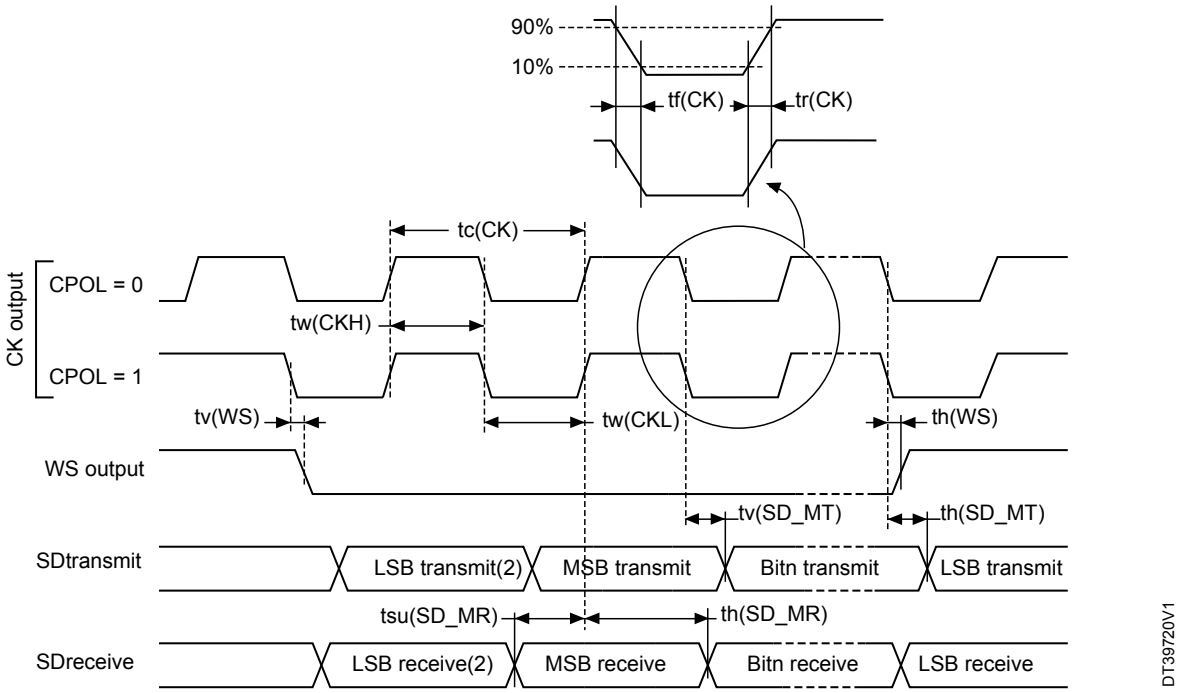
Figure 64. I²S target timing diagram (Philips protocol)(1)



1. *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*

Prerelease product(s)

Figure 65. I²S controller timing diagram (Philips protocol)(1)



1. *LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.*
2. *Refer to Section 5.3.15: I/O port characteristics for more details on the input/output alternate function characteristics (FDCANx_TX and FDCANx_RX).*

USB full speed (FS) characteristics

The USB interface is fully compliant with the USB specification version 2.0.

Table 115. USB DC electrical characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{DD}	USB full speed transceiver operating voltage	-	3.0(2)	-	3.6	V
V_{DI}(3)	Differential input sensitivity	Over VCM range	0.2	-	-	V
V_{CM}(3)	Differential input common mode range	Includes V_{DI} range	0.8	-	2.5	
V_{SE}(3)	Single ended receiver input threshold	-	0.8	-	2.0	
V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V	-	-	0.3	V
V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}(3)	Pull down resistor on PA11, PA12 (USB_DM, USB_DP)	V_{IN} = V_{DD}	14.25	-	24.8	kΩ
R_{PU}(3)	Pull-up resistor on PA12 (USB_DP)	V_{IN} = V_{SS}, during idle	0.9	1.25	1.575	
	Pull-up resistor on PA12 (USB_DP)	V_{IN} = V_{SS} during reception	1.425	2.25	3.09	

1. *All the voltages are measured from the local ground potential.*
2. *The USB full speed transceiver functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics, which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.*
3. *Specified by design. Not tested in production.*
4. *R_L is the load connected on the USB full speed drivers.*

Prerelease product(s)

Figure 66. **USB timings - definition of data signal rise and fall time**

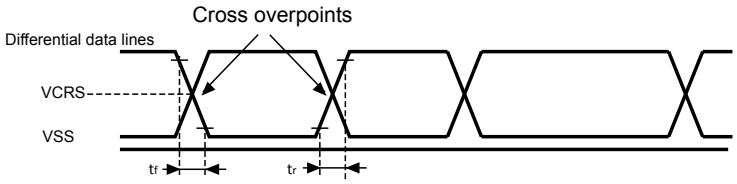


Table 116. **USB startup time**

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. *Specified by design. Not tested in production.*

Table 117. **USB electrical characteristics**

Specified by design. Not tested in production.

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_{rLS}	Rise time in LS(1)	C_L = 200 to 600 pF	75	300	ns
t_{fLS}	Fall time in LS(1)	C_L = 200 to 600 pF	75	300	ns
t_{rfmLS}	Rise/fall time matching in LS	t_r/t_f	80	125	%
t_{rFS}	Rise time in FS(1)	C_L = 50 pF	4	20	ns
t_{fFS}	Fall time in FS(1)	C_L = 50 pF	4	20	ns
t_{rfmFS}	Rise/fall time matching in FS	t_r/t_f	90	111	%
V_{CRS}	Output signal crossover voltage (LS/FS)	-	1.3	2.0	V
Z_{DRV}	Output driver impedance(2)	Driving high or low	28	44	Ω

1. *Measured from 10% to 90% of the data signal. For more detailed information, refer to USB specification - chapter 7 (version 2.0).*
2. *No external termination series resistors are required on DP (D+) and DM (D-) pins since the matching impedance is included in the embedded driver.*

Table 118. **USB BCD DC electrical characteristics**

Specified by design. Not tested in production.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DD(USBBCD)}$	Primary detection mode consumption	-	-	-	300	µA
	Secondary detection mode consumption	-	-	-	300	
R_{DAT_LKG}	Data line leakage resistance	-	300	-	-	kΩ
V_{DAT_LKG}	Data line leakage voltage	-	0.0	-	3.6	V
R_{DCP_DAT}	Dedicated charging port resistance across D+/D-	-	-	-	200	Ω
V_{LGC_HI}	Logic high	-	2.0	-	3.6	V
V_{LGC_LOW}	Logic low	-	-	-	0.8	
V_{LGC}	Logic threshold	-	0.8	-	2.0	
V_{DAT_REF}	Data detect voltage	-	0.25	-	0.4	

Prerelease product(s)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DP_SRC}	D+ source voltage	-	0.5	-	0.7	V
V_{DM_SRC}	D- source voltage	-	0.5	-	0.7	
I_{DP_SINK}	D+ sink current	-	25	-	175	µA
I_{DM_SINK}	D- sink current	-	25	-	175	

Table 119. UCPD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	UCPD operating supply voltage	Sink mode only	3.0	3.3	3.6	V
		Sink and source mode	3.135	3.3	3.465	

JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in Table 120. Dynamic JTAG characteristics and Table 121. Dynamic SWD characteristics for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and V_{DD} supply voltage summarized in Section 5.3.1: General operating conditions, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C_L= 30 pF
- Measurement points are done at CMOS levels: 0.5 V_{DD}

Refer to Section 5.3.15: I/O port characteristics for more details on the input/output characteristics:

Table 120. Dynamic JTAG characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{TCK}	T_{CK} clock frequency	-	-	-	33	MHz
$ti_{su(TMS)}$	TMS input setup time	-	2.5	-	-	ns
$ti_{h(TMS)}$	TMS input hold time	-	1.5	-	-	
$ti_{su(TDI)}$	TDI input setup time	-	1.5	-	-	
$ti_{h(TDI)}$	TDI input hold time	-	0.1	-	-	
$t_{ov(TDO)}$	TDO output valid time	-	-	11.5	15	
$t_{oh(TDO)}$	TDO output hold time	-	8	-	-	

Table 121. Dynamic SWD characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{SWCLK}	SWCLK clock frequency	-	-	-	76	MHz
$ti_{su(SWDIO)}$	SWDIO input setup time	-	2	-	-	ns
$ti_{h(SWDIO)}$	SWDIO input hold time	-	1	-	-	
$t_{ov(SWDIO)}$	SWDIO output valid time	-	-	10	13	
$t_{oh(SWDIO)}$	SWDIO output hold time	-	6	-	-	

Prerelease product(s)

Figure 67. **JTAG timing diagram**

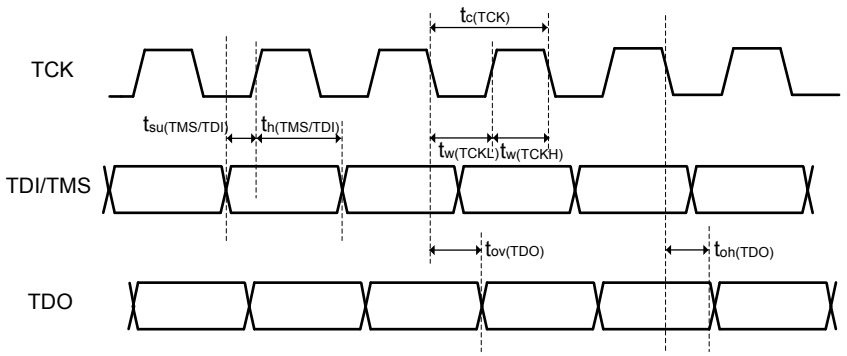
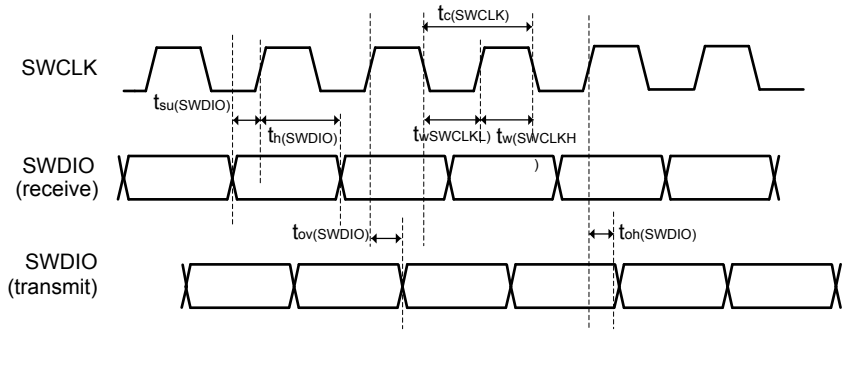


Figure 68. **SWD timing diagram**



Prerelease product(s)

6 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 Device marking

Refer to technical note "Reference device marking schematics for STM32 microcontrollers and microprocessors" (TN1433) available on www.st.com, for the location of pin 1/ball A1 as well as the location and orientation of the marking areas versus pin 1 / ball A1.

Parts marked as "ES", "E" or accompanied by an engineering sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use.

In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

A WLCSP simplified marking example (if any) is provided in the corresponding package information subsection.

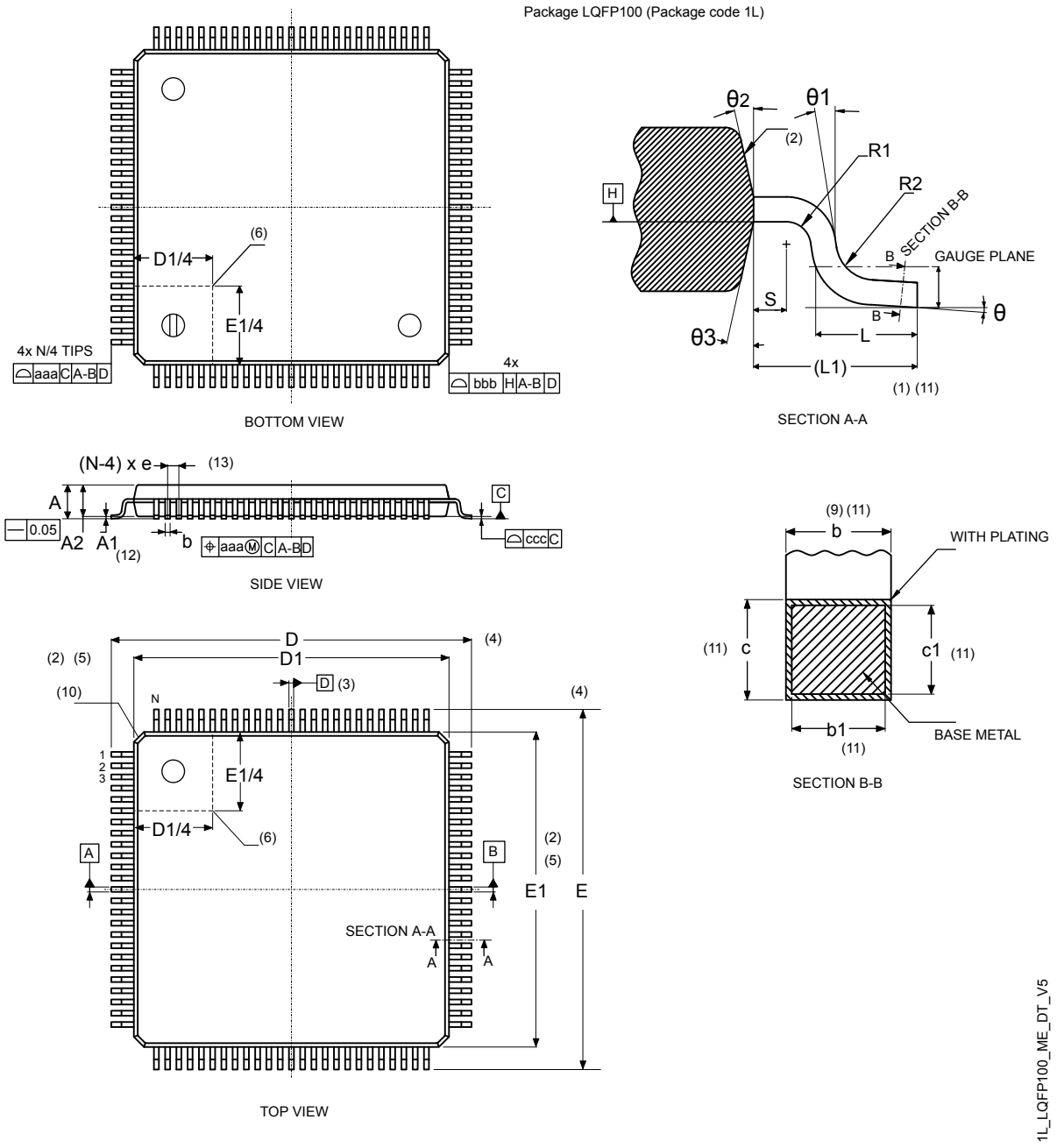
6.2 LQFP100 package information (1L)

This LQFP is a 100-pin, 14 x 14 mm, low-profile quad flat package.

Note: See list of notes in the notes section.

Prerelease product(s)

Figure 69. **LQFP100 - Outline**[15.]



Prerelease product(s)

Table 122. **LQFP100 - Mechanical data**

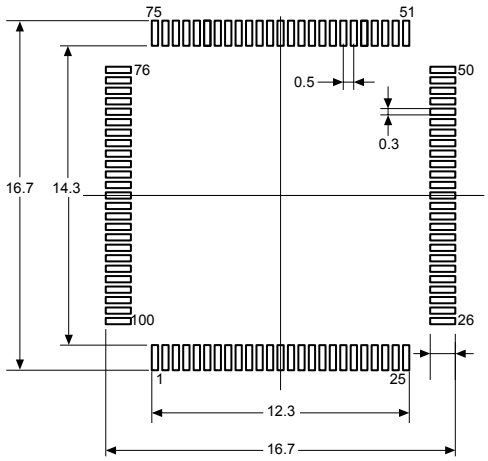
Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	1.50	1.60	-	0.0590	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	16.00 BSC			0.6299 BSC		
D1[2.][5.]	14.00 BSC			0.5512 BSC		
E[4.]	16.00 BSC			0.6299 BSC		
E1[2.][5.]	14.00 BSC			0.5512 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1[1.][11.]	-	1.00	-	-	0.0394	-
N[13.]	100					
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[1.]	0.20			0.0079		
bbb[1.]	0.20			0.0079		
ccc[1.]	0.08			0.0031		
ddd[1.]	0.08			0.0031		

Prerelease product(s)

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion is allowed inwards the leads.
9. Dimension “b” does not include a dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. The exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 70. LQFP100 - Footprint example



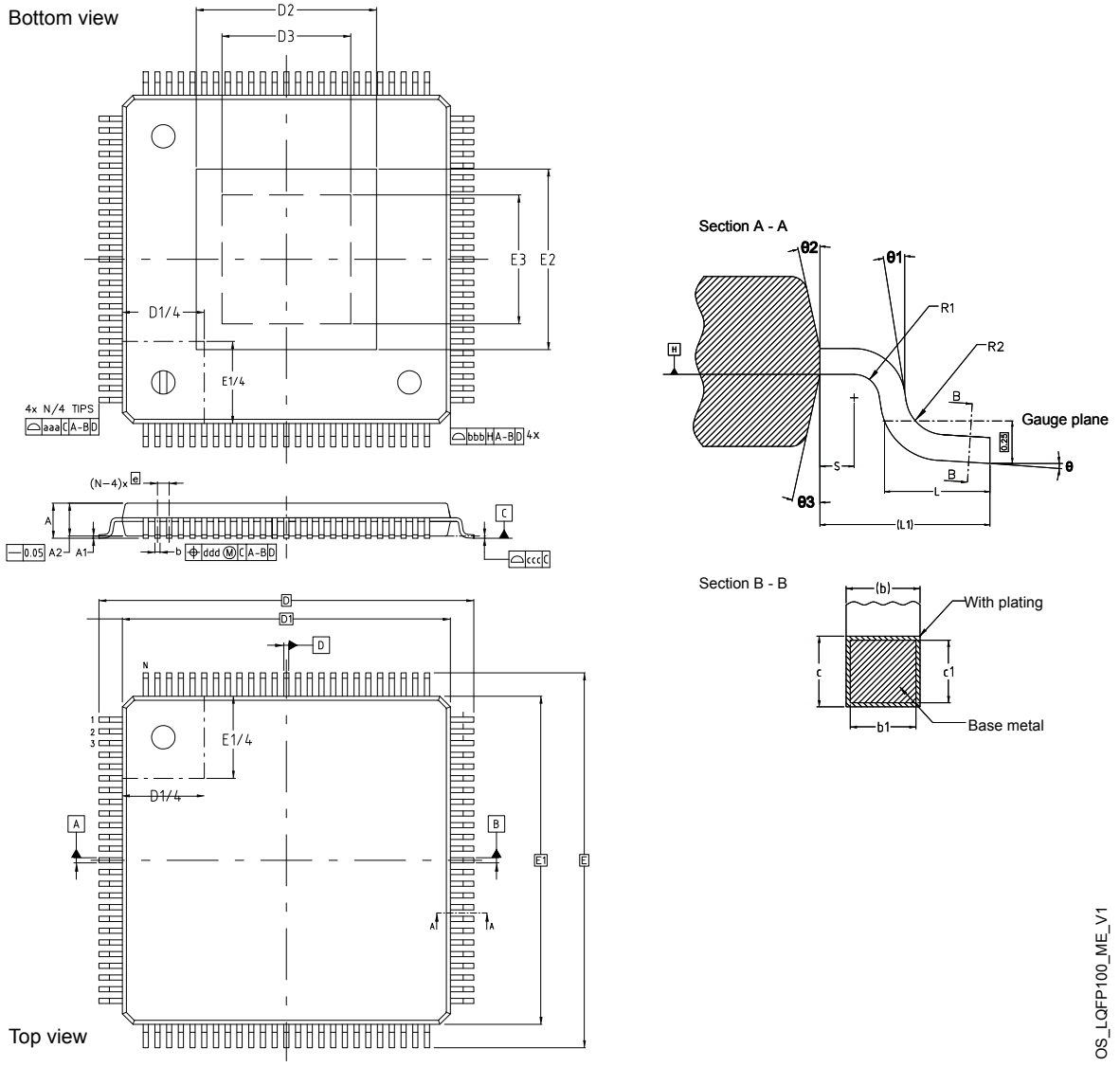
1. *Dimensions are expressed in millimeters.*

6.3 LQFP100-EP package information (OS_A)

This LQFP is a 100-pin, 14 x 14 mm, low-profile quad flat package with an exposed pad (EP) measuring 5.5 x 5.5 mm.

Prerelease product(s)

Figure 71. **LQFP100-EP - Outline**



1. *The drawing is not to scale.*

Prerelease product(s)

Prerelease product(s)

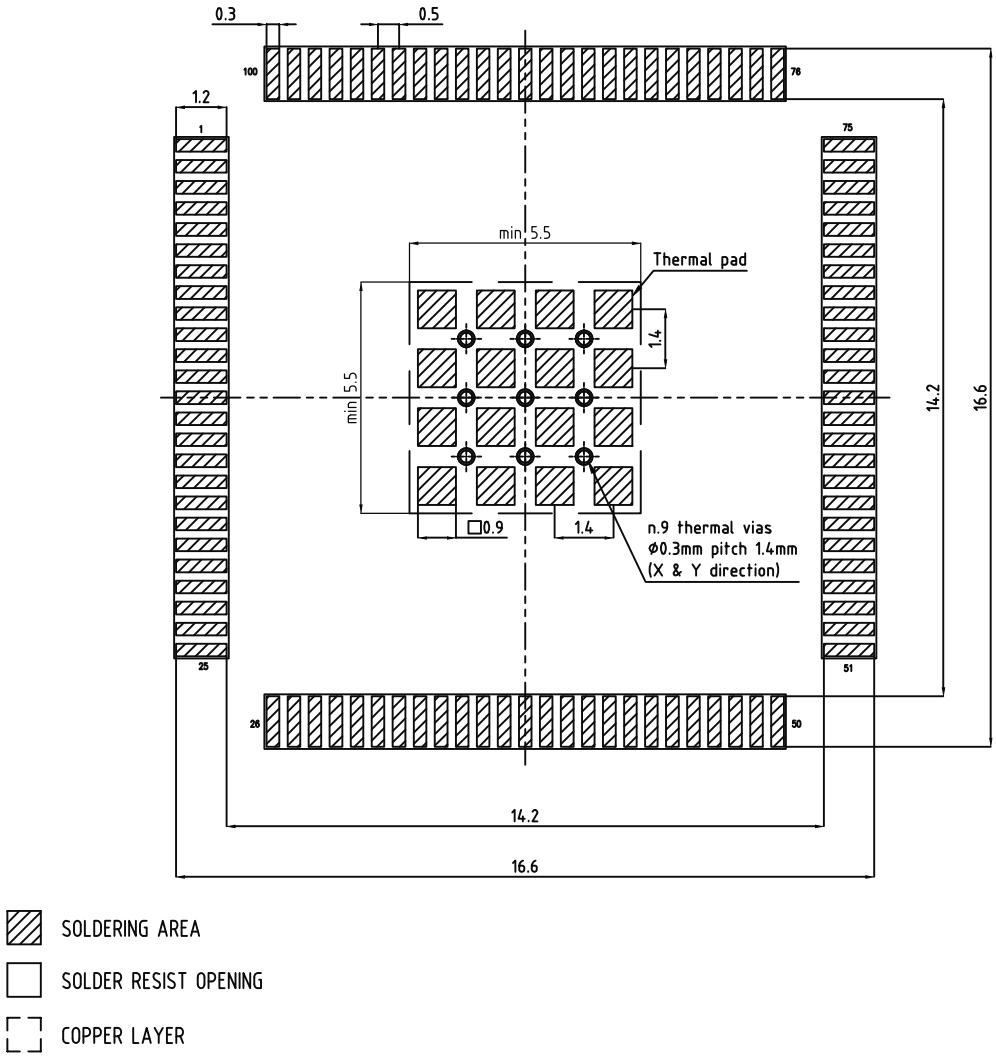
Table 123. LQFP100-EP - Mechanical data

Symbol[1]	Millimeters			Inches[2]		
	Min	Typ	Max	Min	Typ	Max
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
A[3]	-	-	1.60	-	-	0.0630
A1[4]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[5][6]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[6]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[6]	0.09	-	0.20	0.0035	-	0.0079
c1[6]	0.09	-	0.16	0.0035	-	0.0063
D[7][8]	16.00 BSC			0.6299 BSC		
D1[8][9][10]	14.00 BSC			0.5512 BSC		
D2[11]	-	-	5.55	-	-	0.2185
D3[12]	4.65	-	-	0.1831	-	-
e[8]	0.50 BSC			0.0197 BSC		
E[7][8]	16.00 BSC			0.6299 BSC		
E1[8][9][10]	14.00 BSC			0.5512 BSC		
E2[11]	-	-	5.55	-	-	0.2185
E3[12]	4.65	-	-	0.1831	-	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13]	100					
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[14]	0.20			0.0079		
bbb[14]	0.20			0.0079		
ccc[14]	0.08			0.0031		
ddd[14]	0.08			0.0031		

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *Values in inches are converted from millimeters and rounded to four decimal digits, except for the Θ values, which are provided in degrees.*
3. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
4. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
5. *Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.*
6. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
7. *To be determined at seating datum plane C.*

8. *BSC stands for basic dimensions. It corresponds to the nominal value and has no tolerance.*
9. *Top package body size may be smaller than the bottom package size by as much as 0.15 mm.*
10. *Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
11. *Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located. It includes all metal protrusions from exposed pad itself.*
12. *Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.*
13. *N represents the total number of pins on the QFP.*
14. *Tolerance of form and position.*

Figure 72. LQFP100-EP - Footprint example



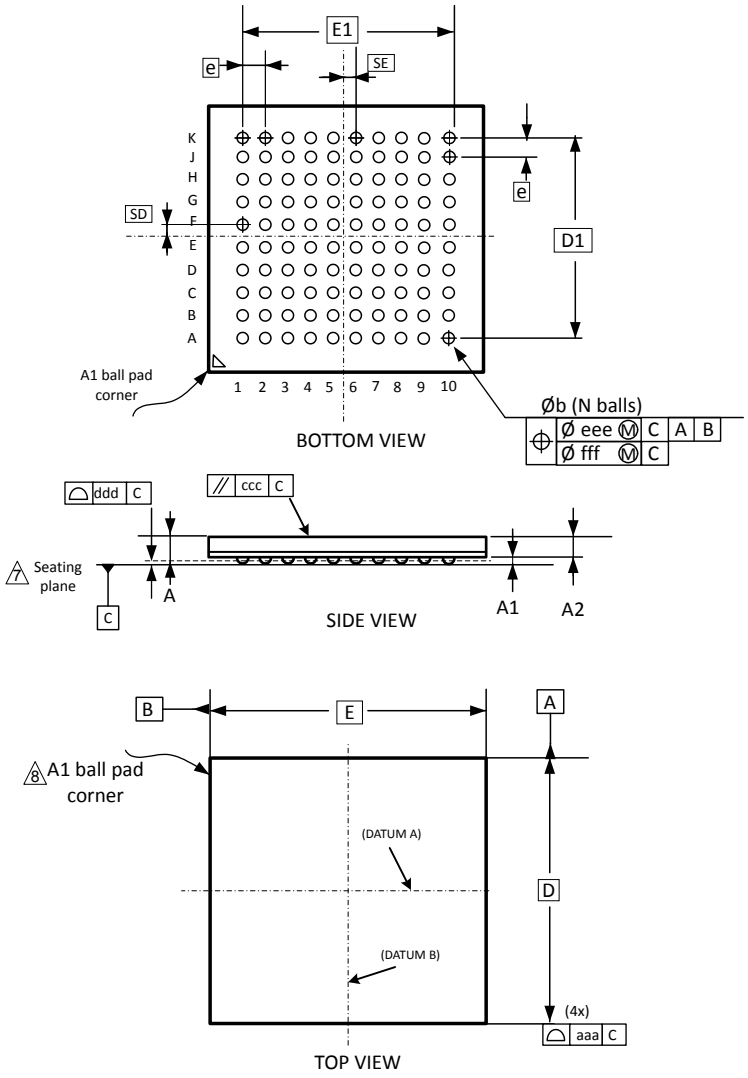
6.4 TFBGA100 package information (A08Q)

This TFBGA is a 100 ball, 8 x 8 mm, 0.8 mm pitch, thin profile fine pitch ball grid array package.

Note: See list of notes in the notes section.

Prerelease product(s)

Figure 73. **TFBGA100 - Outline**(13.)



A08Q_UFBGA100_ME_DT_V1

Prerelease product(s)

Table 124. **TFBGA100 - Mechanical data**

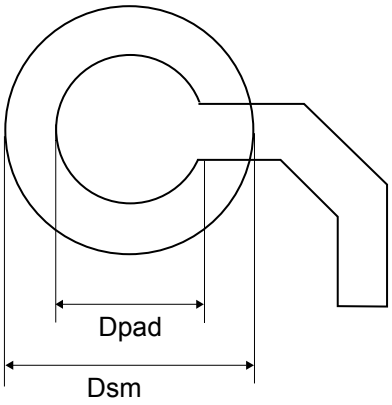
Symbol	millimeters(1.)			inches(12.)		
	Min	Typ	Max	Min	Typ	Max
A(2.)(3.)	-	-	1.20	-	-	0.0472
A1(4.)	0.15	-	-	0.0059	-	-
A2	-	0.74	-	-	0.0291	-
b(5.)	0.35	0.40	0.45	0.0138	0.0157	0.0177
D	8.00 BSC(6.)			0.3150 BSC		
D1	7.20 BSC			0.2835 BSC		
E	8.00 BSC			0.3150 BSC		
E1	7.20 BSC			0.2835 BSC		
e(9.)	0.80 BSC			0.0315 BSC		
N(10.)	100					
SD(11.)	0.40 BSC			0.0157		
SE(11.)	0.40 BSC			0.0157		
aaa	0.15			0.0059		
ccc	0.20			0.0079		
ddd	0.10			0.0039		
eee	0.15			0.0059		
fff	0.08			0.0031		

Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-2018
2. TFBGA stands for thin profile fine pitch ball grid array: 1.00 mm < A ≤ 1.20 mm / fine pitch e < 1.00 mm.
3. The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.
4. A1 is defined as the distance from the seating plane to the lowest point on the package body.
5. Dimension b is measured at the maximum diameter of the terminal (ball) in a plane parallel to primary datum C.
6. BSC stands for BASIC dimensions. It corresponds to the nominal value and has no tolerance. For tolerances refer to form and position table. On the drawing these dimensions are framed.
7. Primary datum C is defined by the plane established by the contact points of three or more solder balls that support the device when it is placed on top of a planar surface.
8. The terminal (ball) A1 corner must be identified on the top surface of the package by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug. A distinguish feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.
9. e represents the solder ball grid pitch.
10. N represents the total number of balls on the BGA.
11. Basic dimensions SD and SE are defined with respect to datums A and B. It defines the position of the centre ball(s) in the outer row or column of a fully populated matrix.
12. Values in inches are converted from mm and rounded to 4 decimal digits.
13. Drawing is not to scale.

Prerelease product(s)

Figure 74. **TFBGA100 - Footprint example**



DT_BGA_WLCSP_FT_V1

Table 125. **TFBGA100 - Example of PCB design rules (0.8 mm pitch BGA)**

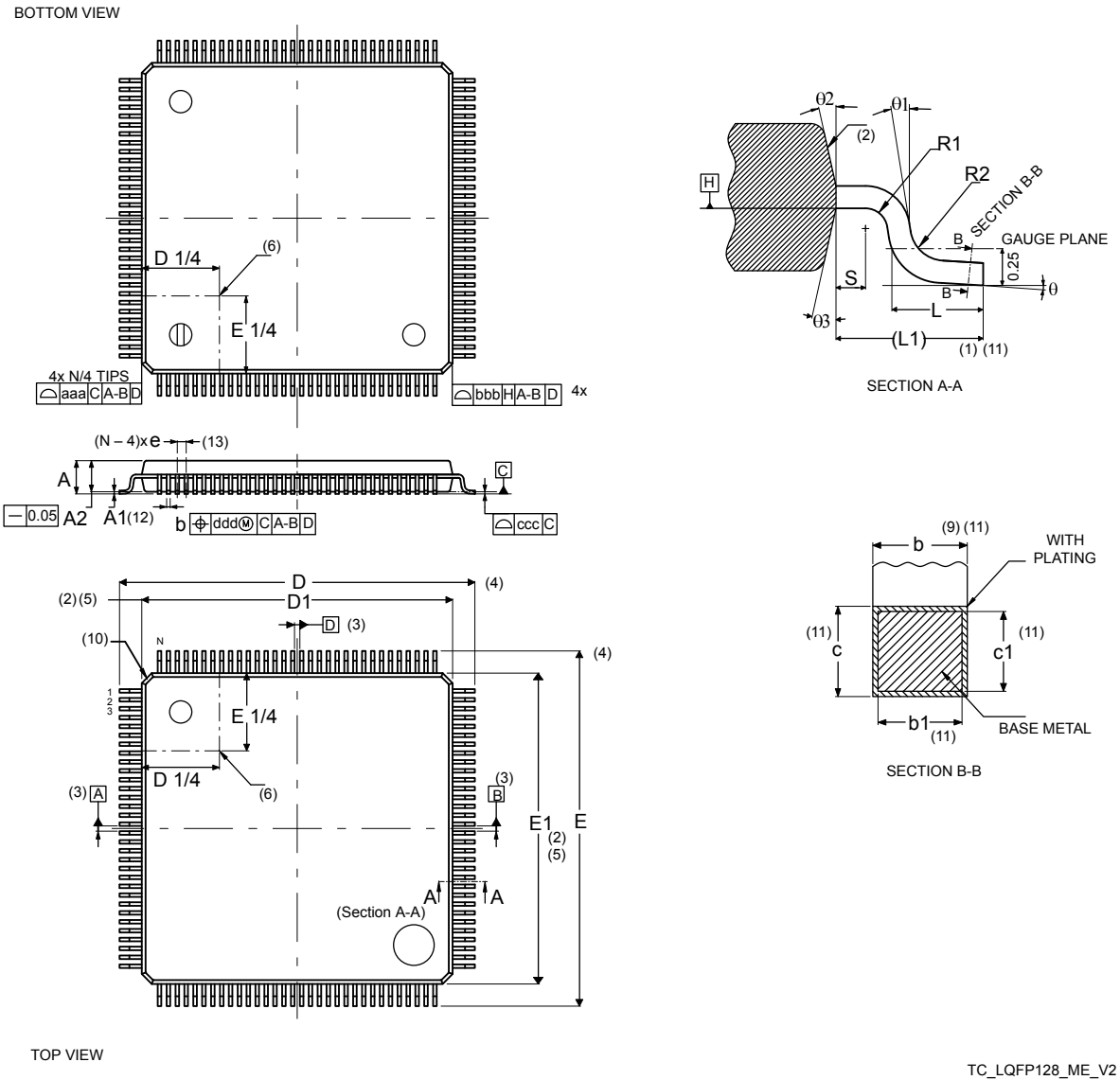
Dimension	Values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typical (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

6.5 LQFP128 package information (TC)

This LQFP128 is a 128-pin, 14 x 14 mm low-profile quad flat package.

Prerelease product(s)

Figure 75. **LQFP128 - Outline**



Note:

1. *Drawing is not to scale.*
2. *Datums A-B and D to be determined at datum plane H.*
3. *Details of pin 1 identifier are optional but must be located within the zone indicated.*
4. *No intrusion allowed inwards the leads.*

Prerelease product(s)

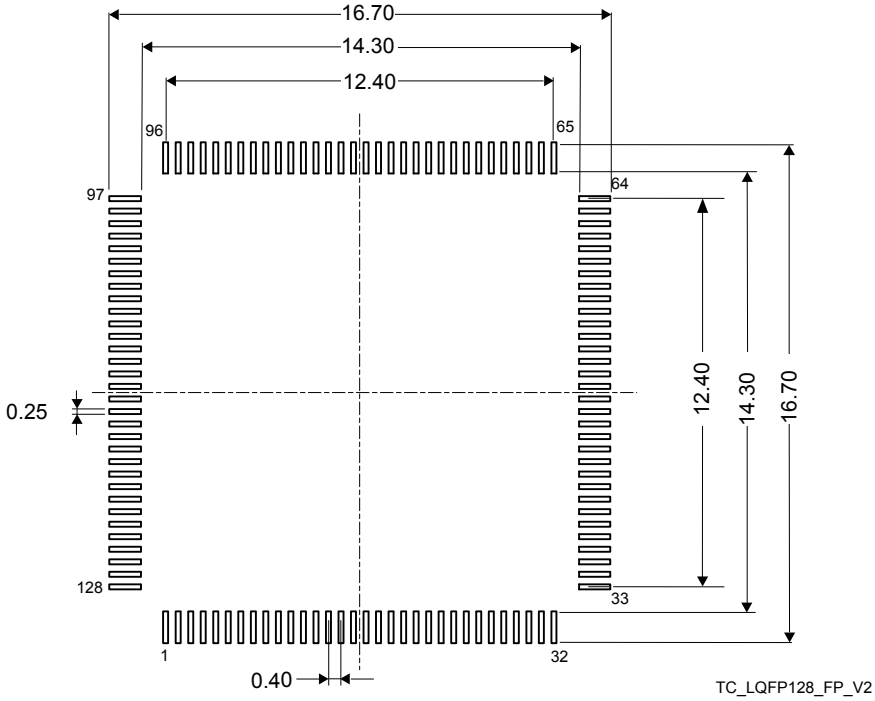
Table 126. **LQFP128 - Mechanical data**

Symbol	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.60	-	-	0.0630
A1[2]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[3][4]	0.13	0.18	0.23	0.0051	0.0071	0.0091
b1[4]	0.13	0.16	0.19	0.0051	0.0063	0.0075
c[4]	0.09	-	0.20	0.0035	-	0.0079
c1[4]	0.09	-	0.16	0.0035	-	0.0063
D[5]	16.00 BSC			0.6299 BSC		
D1[7]	14.00 BSC			0.5512 BSC		
E[5]	16.00 BSC			0.6299 BSC		
E1[6][7]	14.00 BSC			0.5512 BSC		
e	0.40 BSC			0.0157 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[8]	128					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa[9]	0.20			0.0079		
bbb[9]	0.20			0.0079		
ccc[9]	0.08			0.0031		
ddd[9]	0.07			0.0027		

1. *Values in inches are converted from mm and rounded to 4 decimal digits.*
2. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
3. *Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.*
4. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
5. *To be determined at seating datum plane C.*
6. *The Top package body size may be smaller than the bottom package size by as much as 0.15 mm.*
7. *Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.*
8. *“N” is the number of terminal positions for the specified body size.*
9. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*

Prerelease product(s)

Figure 76. **LQFP128 - Footprint example**



1. *Dimensions are expressed in millimeters.*

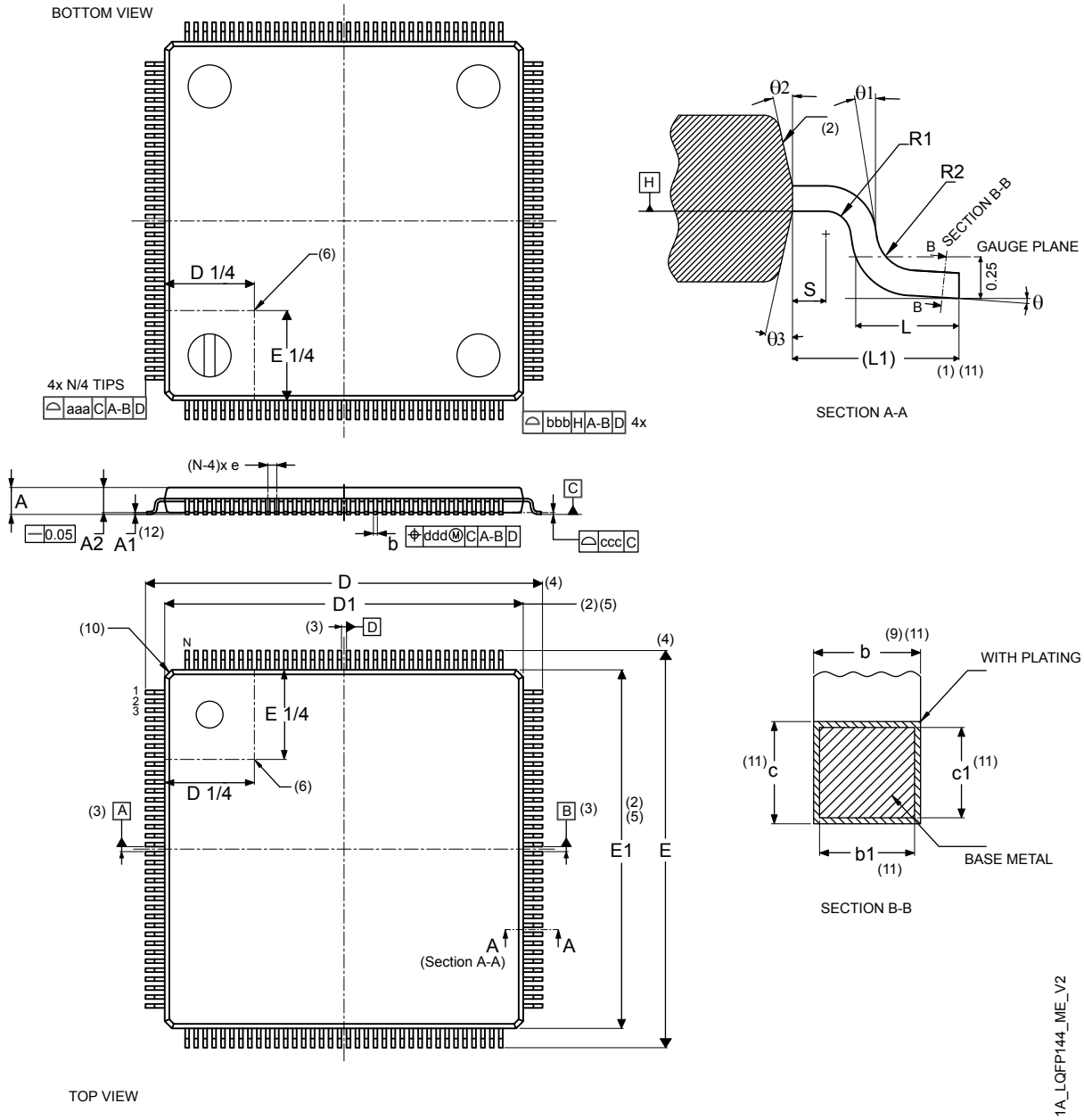
6.6 LQFP144 package information (1A)

LQFP144 is a 144-pin, 20 x 20 mm low-profile quad flat package.

Note: See list of notes in the notes section.

Prerelease product(s)

Figure 77. **LQFP144 - Outline**[15.]



Prerelease product(s)

Table 127. **LQFP144 - Mechanical data**

Symbol	Millimeters			Inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.60	-	-	0.0630
A1[12.]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[9.][11.]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[11.]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[11.]	0.09	-	0.20	0.0035	-	0.0079
c1[11.]	0.09	-	0.16	0.0035	-	0.0063
D[4.]	22.00 BSC			0.8661 BSC		
D1[2.][5.]	20.00 BSC			0.7874 BSC		
E[4.]	22.00 BSC			0.8661 BSC		
E1[2.][5.]	20.00 BSC			0.7874 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[13.]	144					
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	0.20			0.0079		
bbb	0.20			0.0079		
ccc	0.08			0.0031		
ddd	0.08			0.0031		

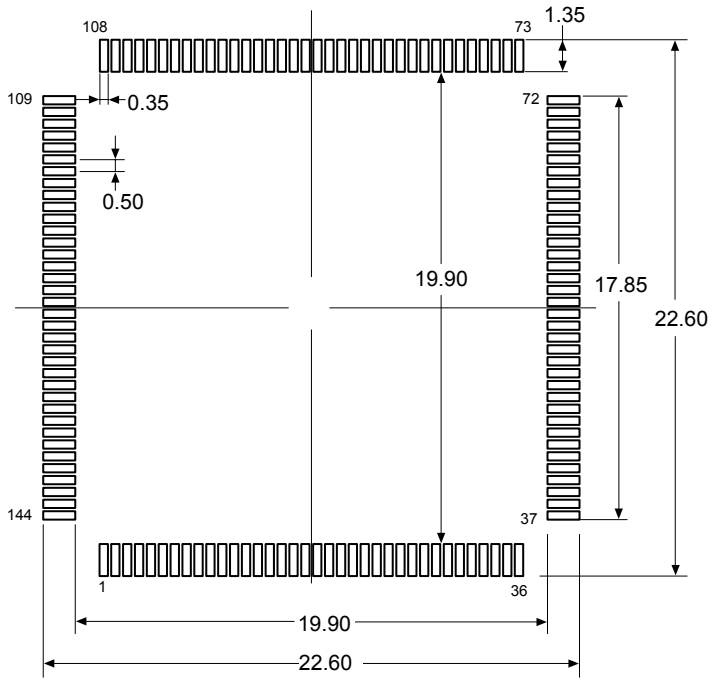
Notes:

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.

Prerelease product(s)

10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 78. LQFP144 - Footprint example



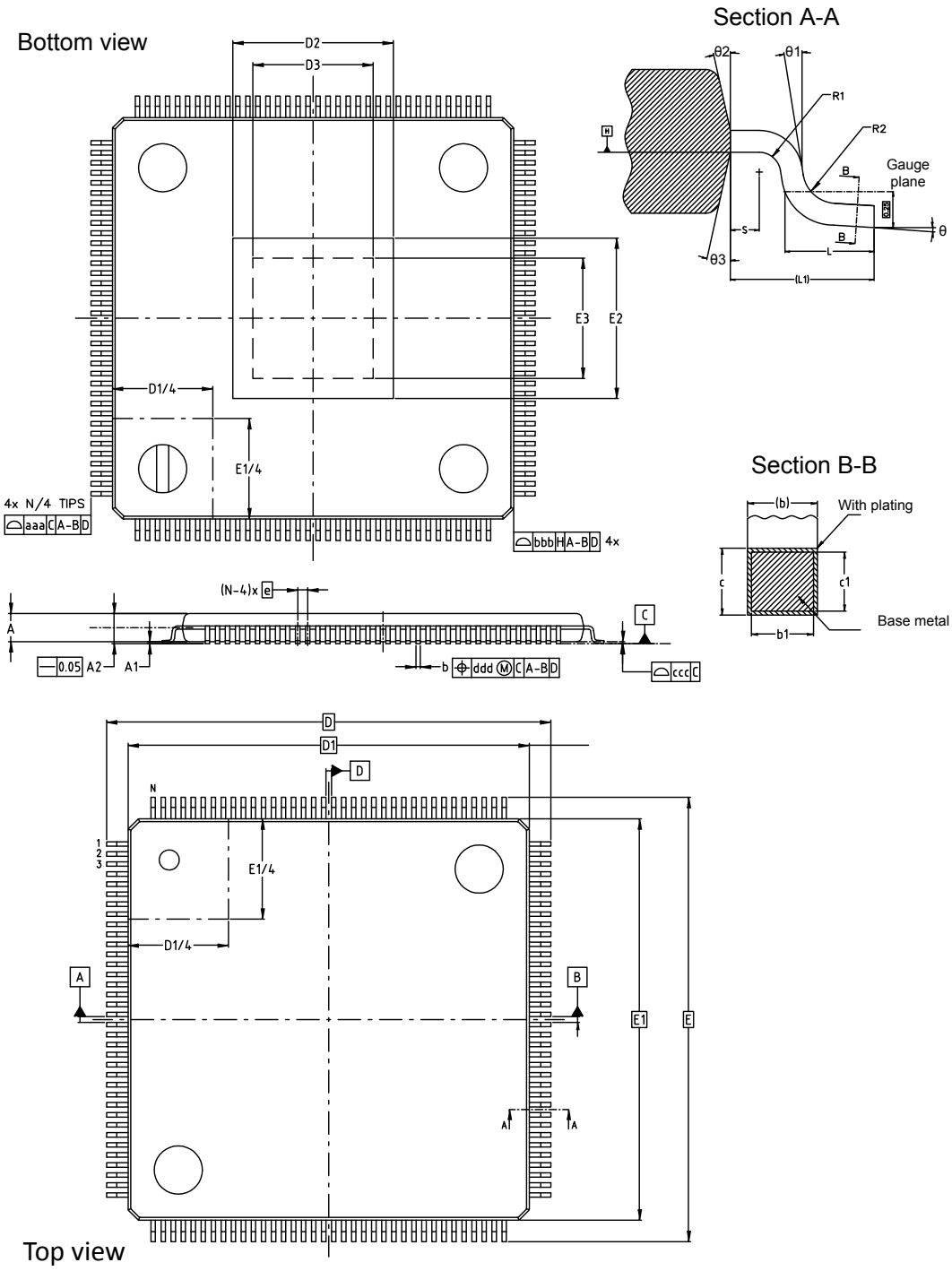
1. Dimensions are expressed in millimeters.

6.7 LQFP144-EP package information (ZO_A)

This LQFP is a 144-pin, 20 x 20 mm low-profile quad flat package with an exposed pad (EP) measuring 5.5 x 5.5 mm.

Prerelease product(s)

Figure 79. **LQFP144-EP - Outline**



Note: The drawing is not to scale.

Table 128. **LQFP144-EP - Mechanical data**

Symbol[1]	Millimeters			Inches[2]		
	Min	Nom	Max	Min	Nom	Max
A[3]	-	-	1.60	-	-	0.0630

Prerelease product(s)

Symbol[1]	Millimeters			Inches[2]		
	Min	Nom	Max	Min	Nom	Max
A1[4]	0.05	-	0.15	0.0020	-	0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[5][6]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[6]	0.17	0.20	0.23	0.0067	0.0079	0.0090
c[6]	0.09	-	0.20	0.0035	-	0.0079
c1[6]	0.09	-	0.16	0.0035	-	0.0063
D[7][8]		22.00 BSC			0.8661 BSC	
D1[8][9][10]		20.00 BSC			0.7874 BSC	
D2[11]	-	-	5.55	-	-	0.2185
D3[12]	4.65	-	-	0.1831	-	-
e[8]	-	0.50 BSC	-	-	0.0197 BSC	-
E[7][8]	-	22.00 BSC	-	-	0.8661 BSC	-
E1[8][9][10]	-	20.00 BSC	-	-	0.7874 BSC	-
E2[11]	-	-	5.55	-	-	0.2185
E3[12]	4.65	-	-	0.1831	-	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00 REF	-	-	0.0394 REF	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	-	-	0°	-	-
Θ2	10°	12°	14°	10°	12°	14°
Θ3	10°	12°	14°	10°	12°	14°

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *Values in inches are converted from millimeters and rounded to four decimal places, except for N, which represents the pin number.*
3. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
4. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
5. *Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.*
6. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
7. *To be determined at seating datum plane C.*
8. *BSC stands for basic dimensions. It corresponds to the nominal value and has no tolerance.*
9. *Top package body size may be smaller than the bottom package size by as much as 0.15 mm.*
10. *Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.*
11. *Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located. It includes all metal protrusions from exposed pad itself.*
12. *Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.*

Prerelease product(s)

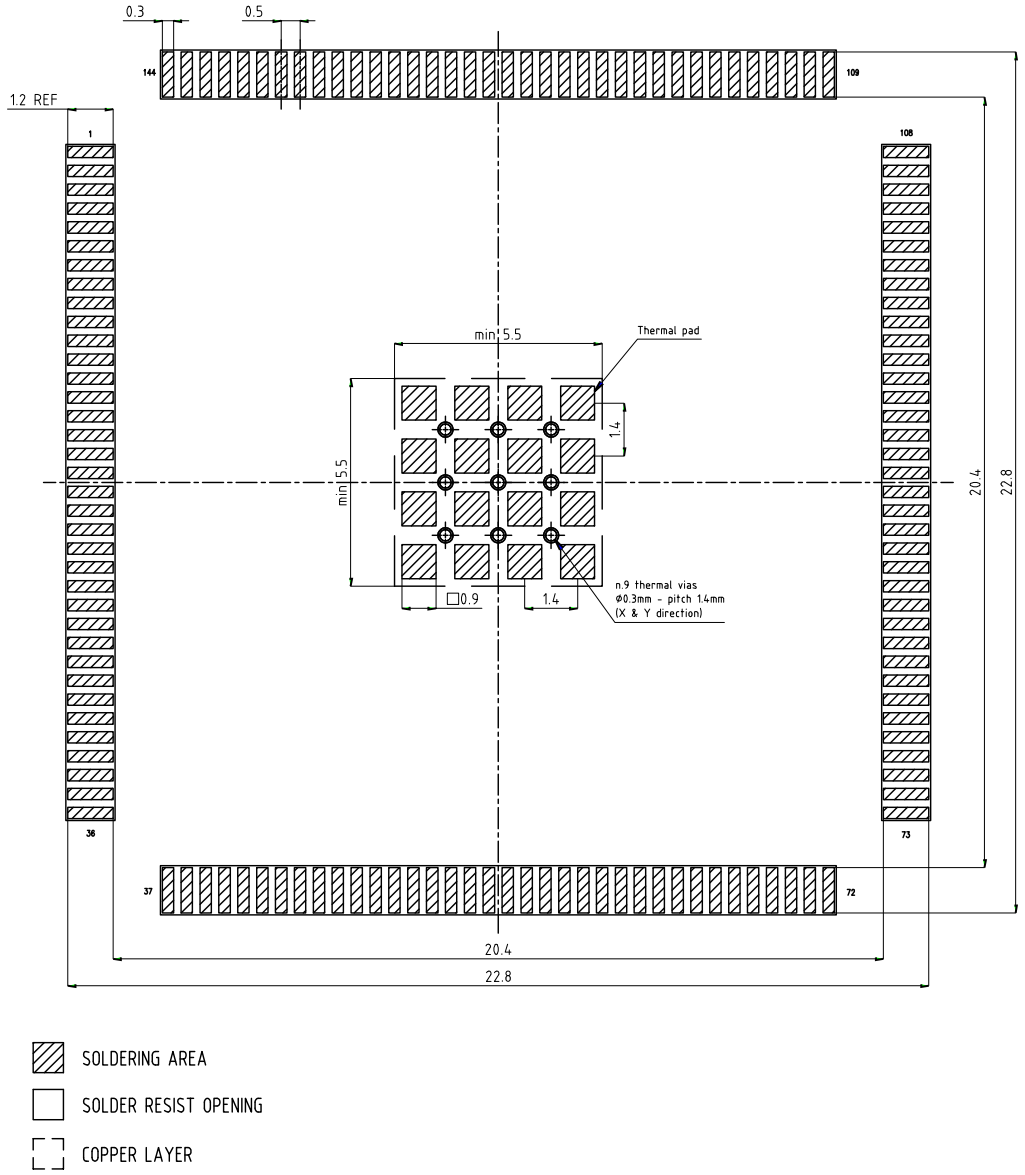
Table 129. **LQFP144-EP - Tolerance of form and position**

Symbol[1]	Millimeters			Inches[2]		
	Min	Typ	Max	Min	Typ	Max
aaa[3]		0.20			0.0079	
bbb[4]		0.20			0.0079	
ccc[5]		0.08			0.0031	
ddd[6]		0.08			0.0031	

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *Values in inches are converted from millimeters and rounded to four decimal places.*
3. *The tolerance controls the position of the terminal pattern with respect to datum A and B.*
4. *The bilateral profile tolerance controls the position of the plastic body sides.*
5. *The unilateral tolerance is located above the seating plane, where the bottom surface of all terminals must be located.*
6. *The tolerance controls the position of the terminals relative to each other. The centers of the profile zones are defined by the basic dimension e.*

Prerelease product(s)

Figure 80. **LQFP144-EP - Footprint example**



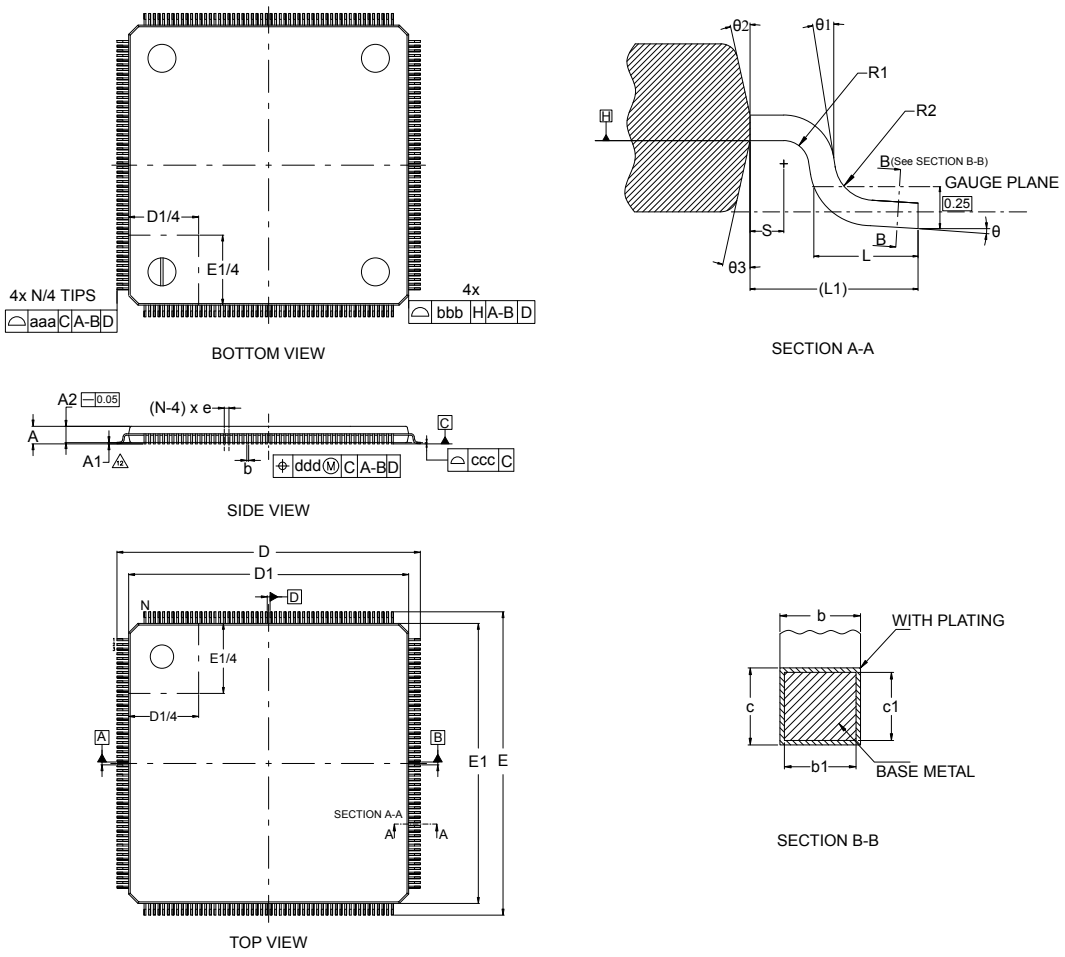
6.8 LQFP176 package information (1T)

This LQFP is a 176-pin, 24 x 24 mm, 0.5 mm pitch, low profile quad flat package.

Note: See list of notes in the notes section.

Prerelease product(s)

Figure 81. **LQFP176 - Outline**[15.]



Prerelease product(s)

Table 130. **LQFP176 - Mechanical data**

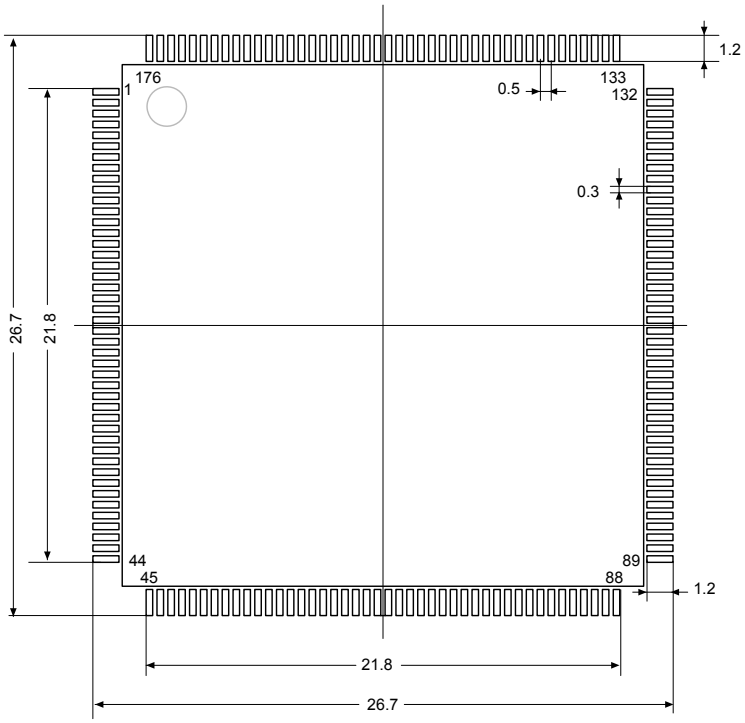
Symbol	millimeters			inches[14.]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1[12.]	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b[9.][11.]	0.170	0.220	0.270	0.0067	0.0087	0.0106
b1[11.]	0.170	0.200	0.230	0.0067	0.0079	0.0091
c[11.]	0.090	-	0.200	0.0035	-	0.0079
c1[11.]	0.090	-	0.160	0.0035	-	0.063
D[4.]	26.000			1.0236		
D1[2.][5.]	24.000			0.9449		
E[4.]	26.000			0.0197		
E1[2.][5.]	24.000			0.9449		
e	0.500			0.1970		
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1[1.][11.]	1 REF			0.0394 REF		
N[13.]	176					
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
R1	0.080	-	-	0.0031	-	-
R2	0.080	-	0.200	0.0031	-	0.0079
S	0.200	-	-	0.0079	-	-
aaa[1.]	0.200			0.0079		
bbb[1.]	0.200			0.0079		
ccc[1.]	0.080			0.0031		
ddd[1.]	0.080			0.0031		

Prerelease product(s)

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package size by as much as 0.15 mm.
3. Datums A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All dimensions are in millimeters.
8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. “N” is the number of terminal positions for the specified body size.
14. Values in inches are converted from mm and rounded to 4 decimal digits.
15. Drawing is not to scale.

Figure 82. LQFP176 - Footprint example



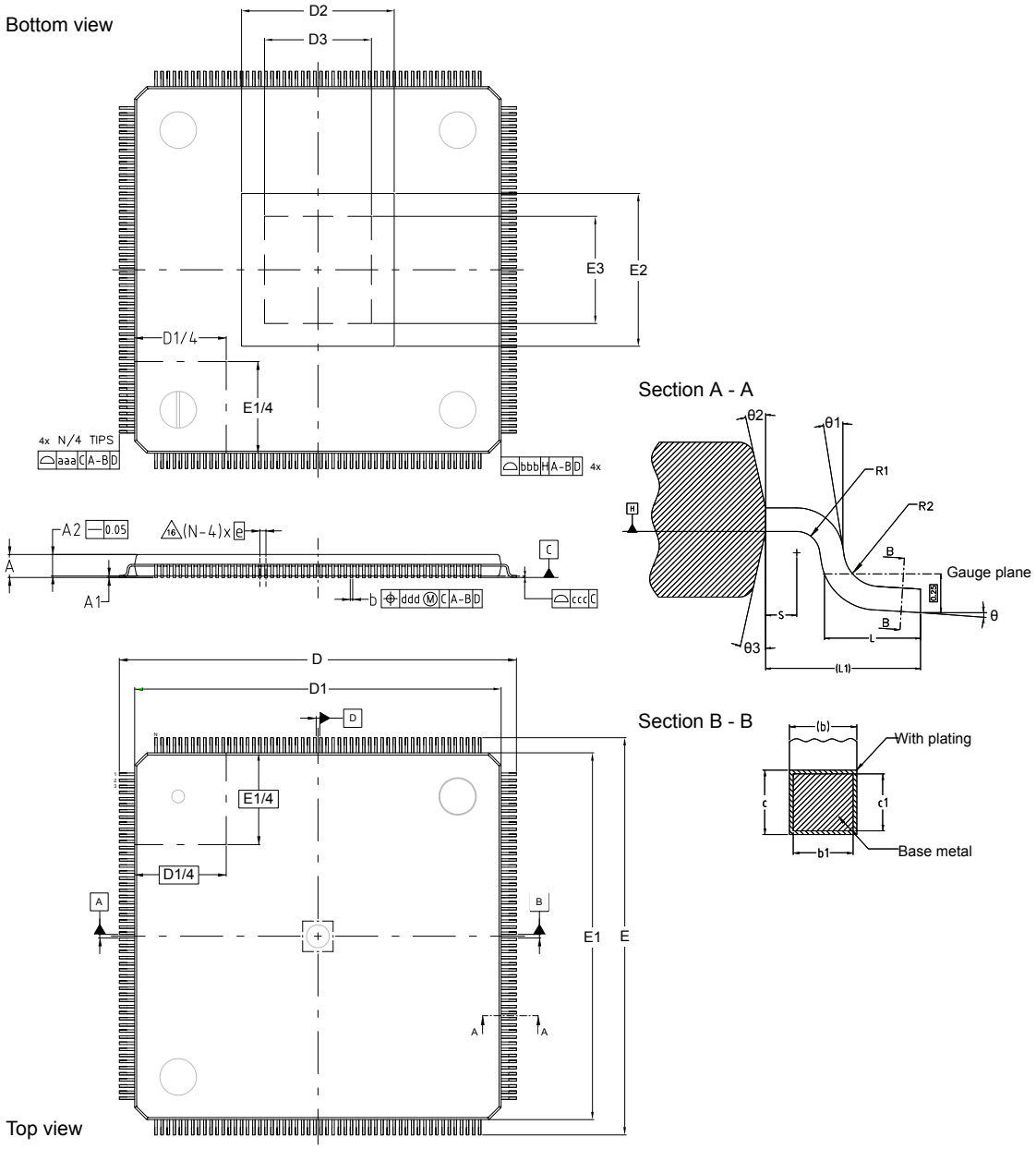
Note: Dimensions are expressed in millimeters.

6.9 LQFP176-EP package information (A0A4_A)

This LQFP is a 176-pin, 24 x 24 mm low-profile quad flat package with an exposed pad (EP) measuring 6.0 x 6.0 mm.

Prerelease product(s)

Figure 83. **LQFP176-EP - Outline**



Note: The drawing is not to scale.

Prerelease product(s)

Table 131. **LQFP176-EP - Mechanical data**

Symbol[1]	Millimeters			Inches[2]		
	Min	Typ	Max	Min	Typ	Max
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	-	-	0°	-	-
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°
A[3][4]	-	-	1.60	-	-	0.0630
A1[5]	0.05	-	0.15	0.0020	-	0.0059
A2[4]	1.35	1.40	1.45	0.0531	0.0551	0.0571
b[6][7]	0.17	0.22	0.27	0.0067	0.0087	0.0106
b1[7]	0.17	0.20	0.23	0.0067	0.0079	0.0091
c[7]	0.09	-	0.20	0.0035	-	0.0079
c1[7]	0.09	-	0.16	0.0035	-	0.0063
D[8]	26.00 BSC[9]			1.0236 BSC		
D1[10][11]	24.00 BSC			0.9449 BSC		
D2[12]	-	-	6.05	-	-	0.2382
D3[13]	5.15	-	-	0.2028	-	-
e	0.50 BSC			0.197 BSC		
E	26.00 BSC			1.0236 BSC		
E1[11]	24.00 BSC			0.9449 BSC		
E2[12]	-	-	6.05	-	-	0.2382
E3[13]	5.15	-	-	0.2028	-	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	1.00 REF			0.0394 REF		
N[14]	176					
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *Values in inches are converted from millimeters and rounded to four decimal digits. However, Θ values are provided in degrees, and N represents the number of pins.*
3. *The profile height, A, is the distance from the seating plane to the highest point on the package. It is measured perpendicular to the seating plane.*
4. *The optional exposed pad is typically aligned with the top or bottom side of the package and must not extend beyond that surface.*
5. *A1 is defined as the distance from the seating plane to the lowest point on the package body.*
6. *Dimension b does not include a dambar protrusion. The allowable dambar protrusion must not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. The dambar must not be located on the lower radius or the foot. The minimum space between the protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.*
7. *These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.*
8. *To be determined at seating datum plane C.*
9. *BSC stands for basic dimensions. It corresponds to the nominal value and has no tolerance.*
10. *The top package body size can be smaller than the bottom package size by up to 0.15 mm.*
11. *Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.*

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12. *Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located. It includes all metal protrusions from the exposed pad itself.*
13. *Dimensions D3 and E3 show the minimum solderable area, defined as the portion of the exposed pad, which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.*
14. *N represents the total number of pins.*

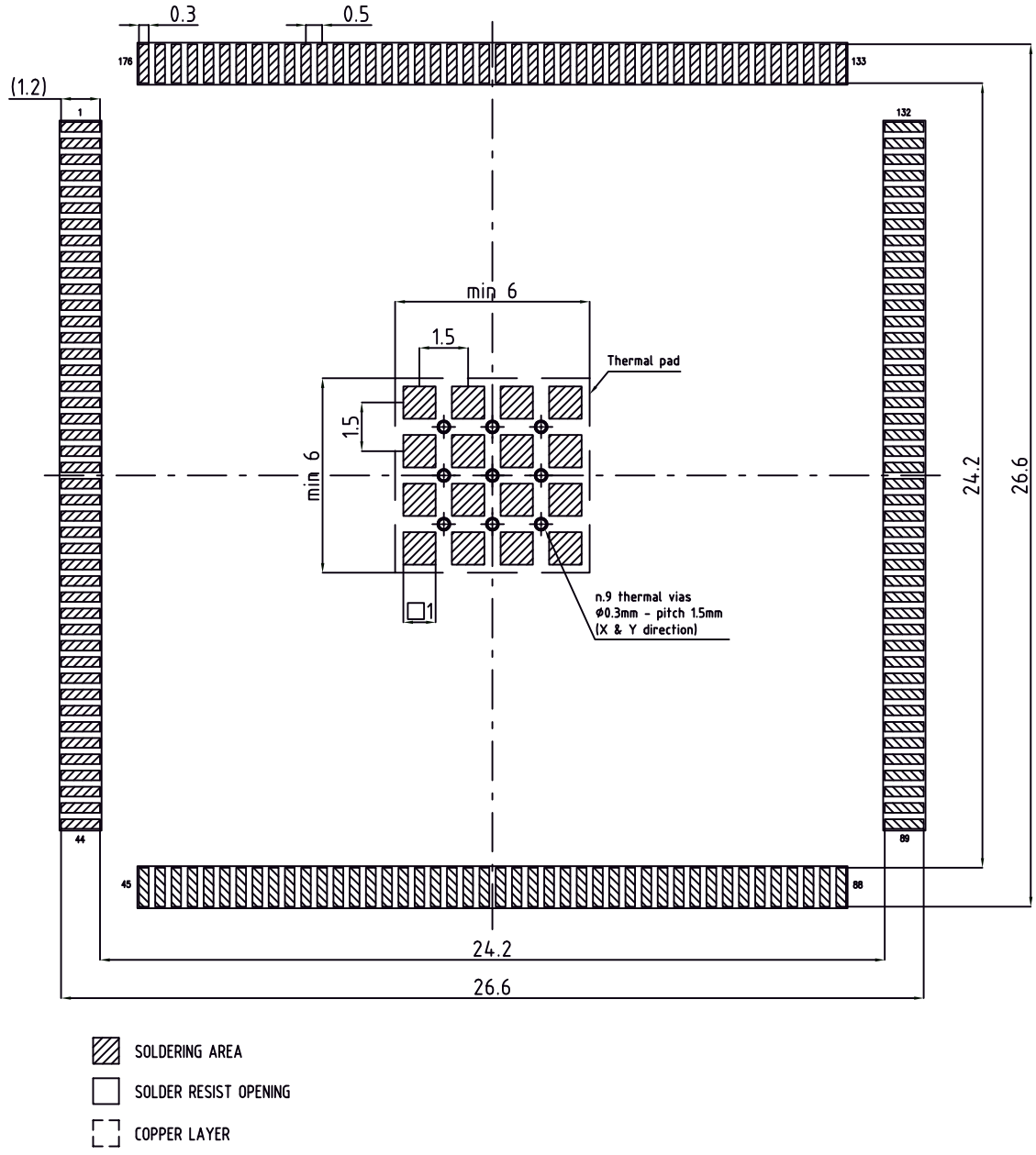
Table 132. LQFP176-EP - Tolerance of form and position

Symbol[2]	Millimeters			Inches[2]		
	Min	Typ	Max	Min	Typ	Max
aaa[3]		0.20			0.0079	
bbb[4]		0.20			0.0079	
ccc[5]		0.08			0.0031	
ddd[6]		0.08			0.0031	

1. *Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.*
2. *Values in inches are converted from millimeters and rounded to four decimal digits.*
3. *The tolerance controls the position of the terminals with respect to datums A and B. The center of the tolerance zone for each terminal is defined by basic dimension e as related to datums A and B.*
4. *The bilateral profile tolerance controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.*
5. *The unilateral tolerance above the seating plane specifies the location of the bottom surface of all terminals. It is commonly known as the coplanarity of the package terminals.*
6. *The tolerance controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension e.*

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Figure 84. **LQFP176-EP - Footnote example**

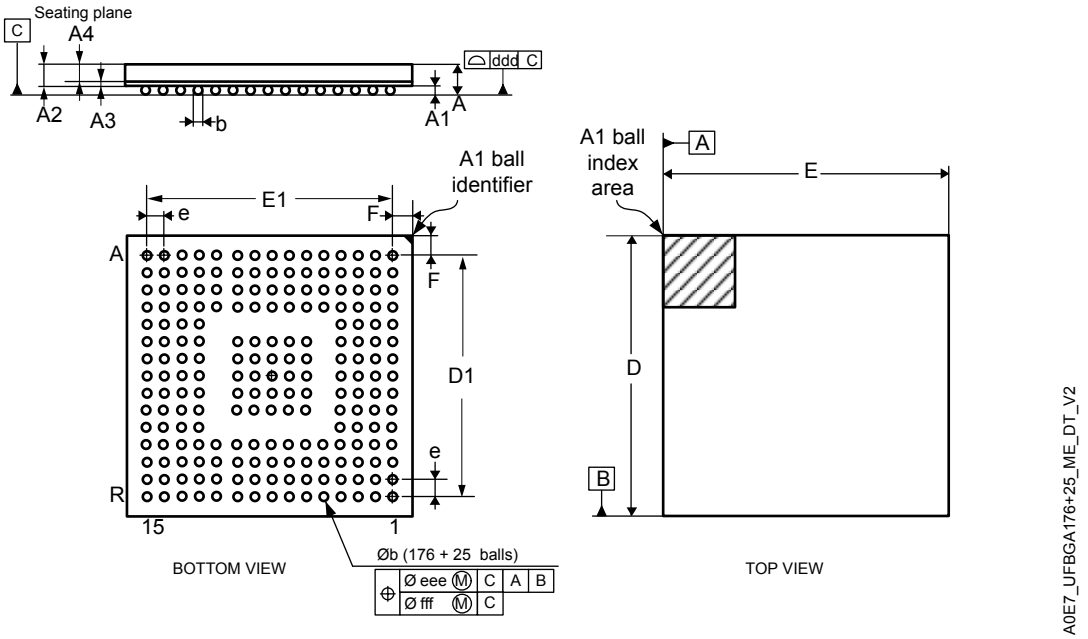


6.10 UFBGA(176+25) package information (A0E7)

This UFBGA is a 176+25 balls, 10 x 10 mm, 0.65 mm pitch, ultra thin profile fine pitch ball grid array package.

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Figure 85. **UFBGA(176+25) - Outline**



1. *Drawing is not to scale.*
2. *The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metalized markings, or other feature of package body or integral heat slug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.*

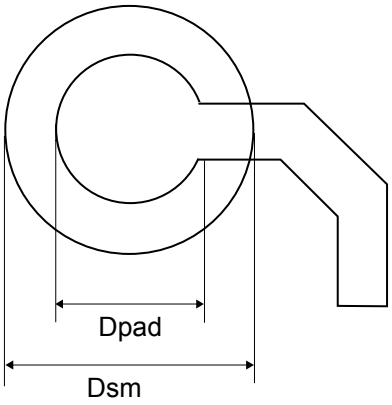
Prerelease product(s)

Table 133. **UFBGA(176+25) - Mechanical data**

Symbol	millimeters			inches (1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A(2)	-	-	0.60	-	-	0.0236
A1	0.05	0.08	0.11	0.0020	0.0031	0.0043
A2	-	0.45	-	-	0.0177	-
A3	-	0.13	-	-	0.0051	-
A4	-	0.32	-	-	0.0126	-
b	0.24	0.29	0.34	0.0094	0.0114	0.0134
D	9.85	10.00	10.15	0.3878	0.03937	0.3996
D1	-	9.10	-	-	0.3583	-
E	9.85	10.00	10.15	0.3878	0.03937	0.3996
E1	-	9.10	-	-	0.3583	-
e	-	0.65	-	-	0.0256	-
F	-	0.45	-	-	0.0177	-
ddd	-	-	0.08	-	-	0.0031
eee (3)	-	-	0.15	-	-	0.0059
fff(4)	-	-	0.05	-	-	0.0020

1. *Values in inches are converted from mm and rounded to four decimal digits.*
2. *Ultra thin profile: 0.50 < A Max \u0001 0.65 mm / Fine pitch: e < 1.00 mm. The total profile height (Dim.A) is measured from the seating plane “C” to the top of the component.*
3. *The tolerance of position that controls the location of the pattern of balls with respect to datum A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datum A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.*
4. *The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.*

Figure 86. **UFBGA(176+25) - Footprint example**



DT_BGA_WLCSP_FT_V1

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Table 134. **UFBGA(176+25) - Example of PCB design rules (0.65 mm pitch BGA)**

Dimension	Values
Pitch	0.65 mm
Dpad	0.300 mm
Dsm	0.400 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.300 mm aperture diameter
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.100 mm

6.11 Package thermal characteristics

The maximum chip-junction temperature, T_J max, in degrees Celsius, can be calculated using the following equation:

$$T_J \max = T_A \max + \left(P_D \max \times \Theta_{JA}\right)$$

where:

- T_A max is the maximum ambient temperature in °C.
- Θ_{JA} is the package junction-to-ambient thermal resistance in °C/W.
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max:

$$P_D \max = P_{INT} \max + P_{I/O} \max)$$

- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins:

$$P_{I/O} \max = \sum\left(V_{OL} \times I_{OL}\right) + \sum\left(\left(V_{DDIOx} - V_{OH}\right) \times I_{OH}\right)$$

taking into account the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high level in the application.

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Table 135. **Package thermal characteristics**

Symbol	Parameter	Package	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient	LQFP100 14×14 mm	33.8	°C/W
		LQFP100-EP 14×14 mm	22.5	
		TFBGA100 8×8 mm	34.3	
		LQFP128 14×14 mm	35.7	
		LQFP144 20×20 mm	35.2	
		LQFP144-EP 20×20 mm	21.6	
		LQFP176 24×24 mm	33.9	
		LQFP176-EP 24×24 mm	20.6	
		UFBGA176+25 10×10 mm	33.8	
Θ_{JB}	Thermal resistance junction-board	LQFP100 14×14 mm	19.6	
		LQFP100-EP 14×14 mm	10.5	
		TFBGA100 8×8 mm	20.8	
		LQFP128 14×14 mm	21.5	
		LQFP144 20×20 mm	24	
		LQFP144-EP 20×20 mm	11.6	
		LQFP176 24×24 mm	23.9	
		LQFP176-EP 24×24 mm	11.6	
		UFBGA176+25 10×10 mm	21.5	
Θ_{JC}	Thermal resistance junction-top case	LQFP100 14×14 mm	7.3	
		LQFP100-EP 14×14 mm	14.4	
		TFBGA100 8×8 mm	11.8	
		LQFP128 14×14 mm	8.1	
		LQFP144 20×20 mm	7.4	
		LQFP144-EP 20×20 mm	10.1	
		LQFP176 24×24 mm	7.1	
		LQFP176-EP 24×24 mm	11.8	
		UFBGA176+25 10×10 mm	8.2	

6.11.1 Reference documents

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air) available on www.jedec.org.
- For information on thermal management, refer to application note *"Guidelines for thermal management on STM32 applications" (AN5036)* available on www.st.com.

Prerelease product(s)

7 Ordering information

Example: STM32 H 7Px I I T 6 Q

Device family

STM32 = Arm® -based 32-bit MCUs

Product type

H = high performance

Device subfamily

7P4 = with HSP

7P5 = with Neural-ART Accelerator and HSP

Pin count

I = 176 pins

Z = 144 pins

Q = 128 pins

V = 100 pins

NVM size

I = 2048 Kbytes

G = 1024 Kbytes

Package

T = LQFP

K = UFBGA

H= TFBGA

Z= LQFP with exposed pad

Junction temperature range

3 = -40 °C < T_J < +125 °C

6 = -40 °C < T_J < +85 °C

Options

Q = SMPS

Note: For a list of available options (such as speed and package) or for further information on any aspect of this device, contact your nearest ST sales office.

Prerelease product(s)

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Prerelease product(s)

Revision history

Table 136. **Document revision history**

Date	Revision	Changes
28-Oct-2026	1	Initial release.

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