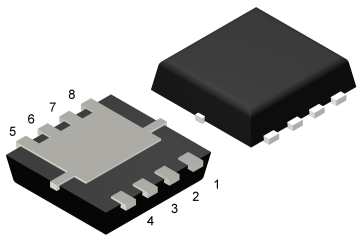
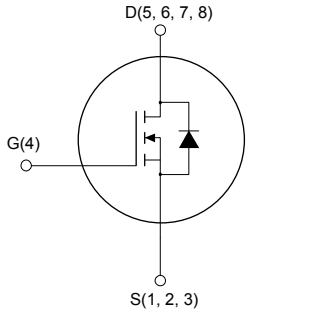
STL100N4LF8

Datasheet

N-channel logic level 40 V, 2.7 mΩ max., 103 A, STripFET F8 Power MOSFET in a PowerFLAT 3.3x3.3 package



PowerFLAT 3.3x3.3



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL100N4LF8	40	2.7 mΩ	103 A

- MSL1 grade
- 150 °C operating temperature
- 100% avalanche tested
- Low gate charge Q_g

Applications

- Industrial tools, motor drives and equipment
- Industrial motor control
- Power supplies and converters

Description

The STL100N4LF8 is a 40 V N-channel enhancement mode Power MOSFET designed in STripFET F8 technology featuring an enhanced trench gate structure.

It ensures a state-of-the-art of figure of merit for very low on-state resistance while reducing internal capacitances and gate charge for faster and more efficient switching.

Product status link
STL100N4LF8

Product summary	
Order code	STL100N4LF8
Marking	1004L
Package	PowerFLAT 3.3x3.3
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings (at T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C (2)	103	A
	Drain current (continuous) at T_C = 100 °C (2)	65	
	Drain current (continuous) at T_C = 25 °C (3)	45	
I_{DM} (1)(2)(4)	Drain current (pulsed), t_P = 10 µs	414	A
P_{TOT}	Total power dissipation at T_C = 25 °C	52	W
I_{AS}	Single pulse avalanche current (pulse width limited by maximum junction temperature)	22	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = 22 A, R_{Gmin} = 25 Ω)	98	mJ
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		°C

1. *Specified by design, not tested in production.*
2. *This is the theoretical current value only related to the silicon.*
3. *This current value is limited by package.*
4. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA} (1)	Thermal resistance, junction-to-ambient (on 2s2p FR-4 board vertical in still area)	19	°C/W
R_{thJC}	Thermal resistance, junction-to-case	2.4	°C/W

1. *Defined according to JEDEC standards (JESD51-5, -7).*

2 Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	40			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 40 V, V_{GS} = 0 V			1	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125°C(1)			100	
I_{GSS}	Gate-body leakage current	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.2		2.0	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 22 A		2.3	2.7	mΩ
		V_{GS} = 4.5 V, I_D = 22 A		3.1	3.85	
R_G(1)	Gate resistance			1.5		Ω

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}(1)	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	2070	-	pF
C_{oss}(1)	Output capacitance		-	550	-	pF
C_{rss}(1)	Reverse transfer capacitance		-	13	-	pF
Q_g(1)	Total gate charge	V_{DD} = 20 V, I_D = 20 A, V_{GS} = 0 to 4.5 V	-	13	-	nC
		V_{DD} = 20 V, I_D = 20 A, V_{GS} = 0 to 10 V	-	28	-	
Q_{gs}(1)	Gate-source charge	V_{DD} = 20 V, I_D = 20 A, V_{GS} = 0 to 4.5 V	-	6.4	-	nC
Q_{gd}(1)	Gate-drain charge		-	2.8	-	nC
$Q_{g(sync)}$(1)	Total gate charge, sync. MOSFET	V_{DS} = 0.1 V, V_{GS} = 0 to 4.5 V	-	11	-	nC
Q_{oss}(1)	Output charge	V_{DD} = 20 V, V_{GS} = 0 V	-	27	-	nC

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(1)	Turn-on delay time	V_{DD} = 20 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	8	-	ns
t_r(1)	Rise time		-	2.7	-	ns
$t_{d(off)}$(1)	Turn-off delay time		-	22	-	ns
t_f(1)	Fall time		-	4.5	-	ns

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)(2)	Forward on current (continuous)	T_C = 25 °C	-		45	A
V_{SD}	Forward on voltage	I_{SD} = 20 A, V_{GS} = 0 V	-		1	V
t_{rr} (1)	Reverse recovery time	I_D = 20 A, di/dt = 100 A/µs, V_{DD} = 32 V	-	35		ns
Q_{rr} (1)	Reverse recovery charge		-	24		nC
I_{RRM} (1)	Reverse recovery current		-	1.5		A

1. *Specified by design and evaluated by characterization, not tested in production.*
2. *This is the theoretical current value only related to the silicon.*

2.1 Electrical characteristics (curves)

Figure 1. Total power dissipation

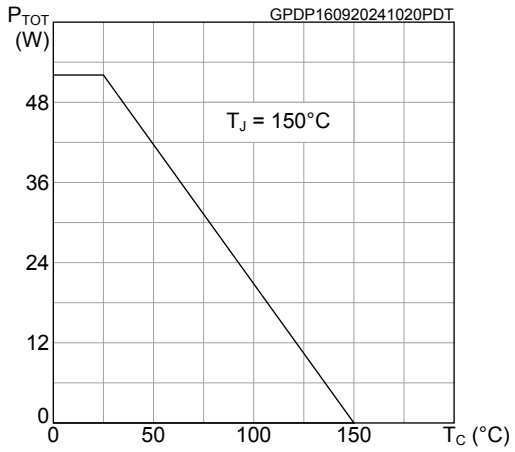


Figure 2. Drain current vs case temperature

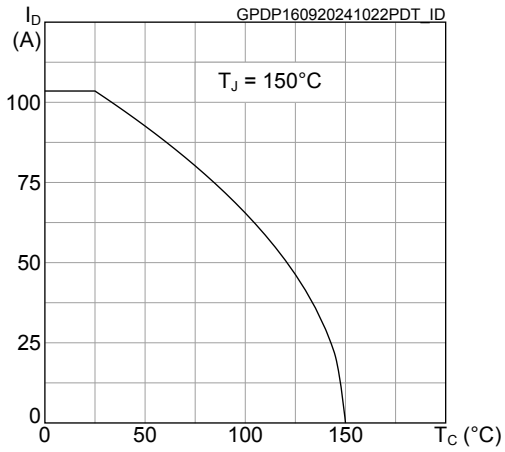


Figure 3. Typical output characteristics

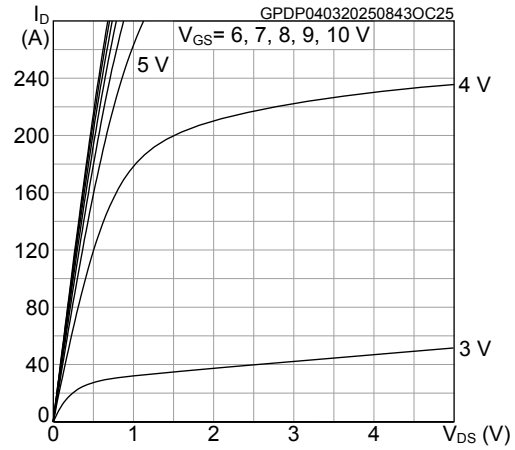


Figure 4. Typical transfer characteristics

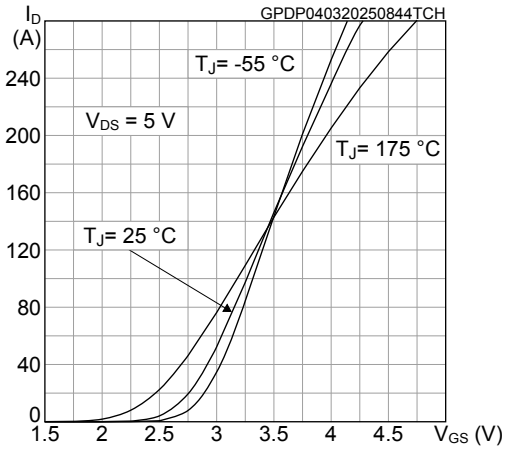


Figure 5. Safe operating area

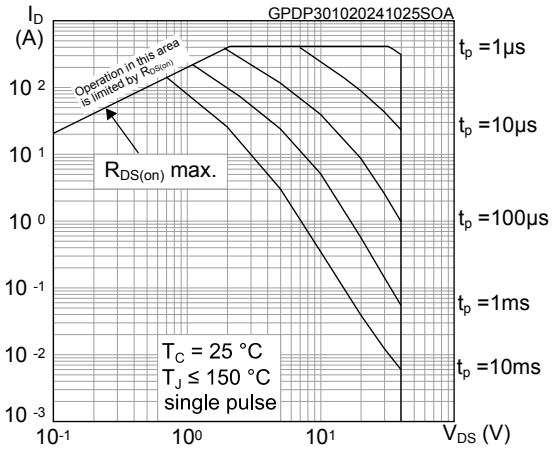


Figure 6. Normalized transient thermal impedance

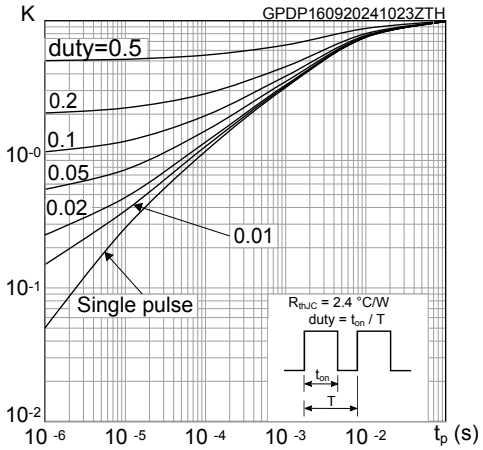


Figure 7. Typical gate charge characteristics

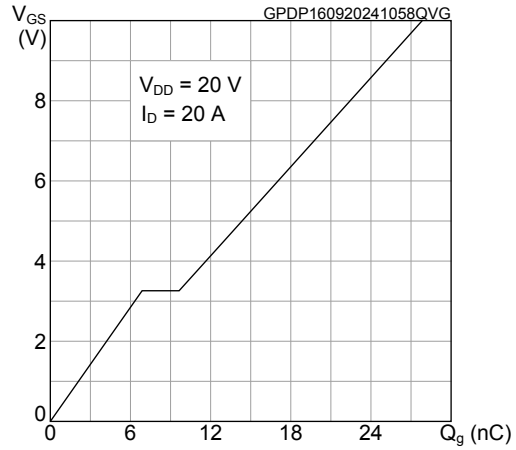


Figure 8. Typical capacitance characteristics

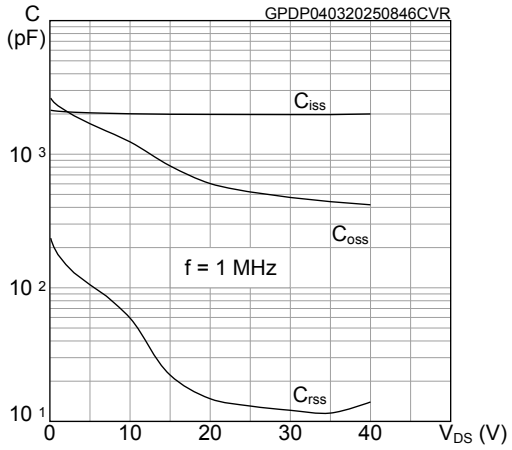


Figure 9. Avalanche characteristics

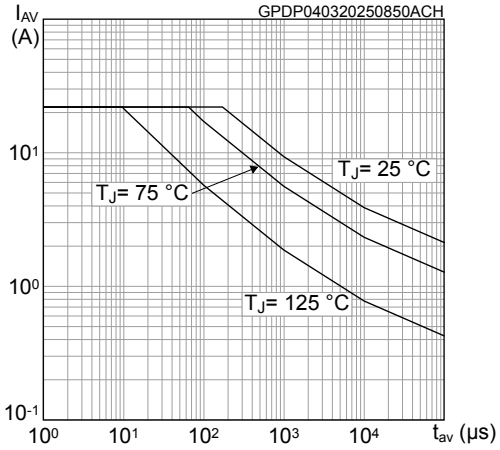


Figure 10. Avalanche energy

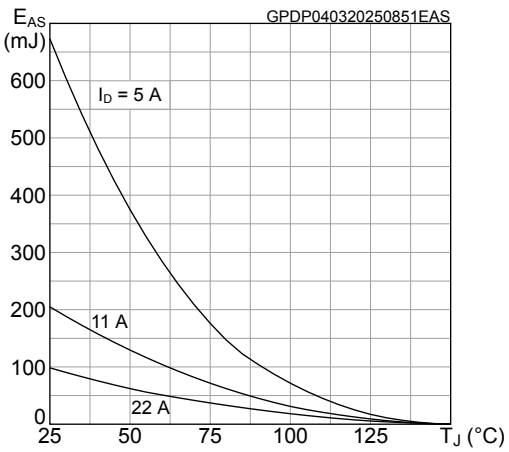


Figure 11. Typical drain-source on-resistance

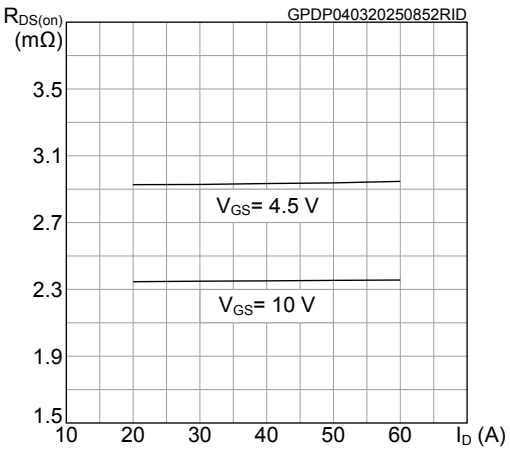


Figure 12. Typical on-resistance vs gate-source voltage

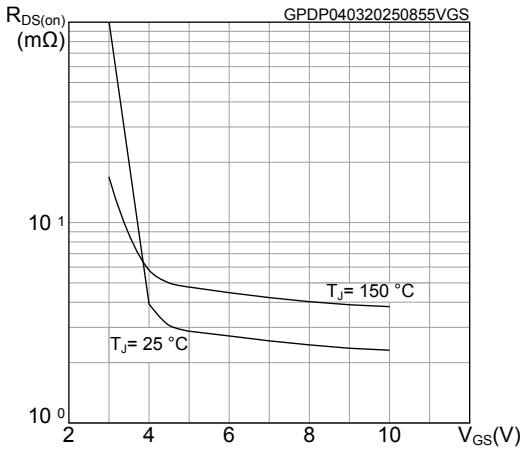


Figure 13. Normalized on-resistance vs temperature

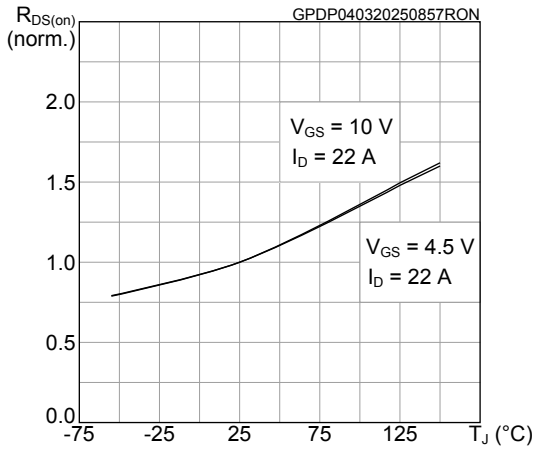


Figure 14. Normalized gate threshold voltage vs temperature

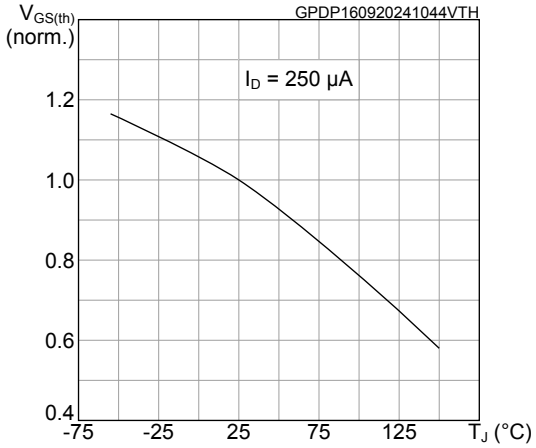


Figure 15. Typical reverse diode forward characteristics

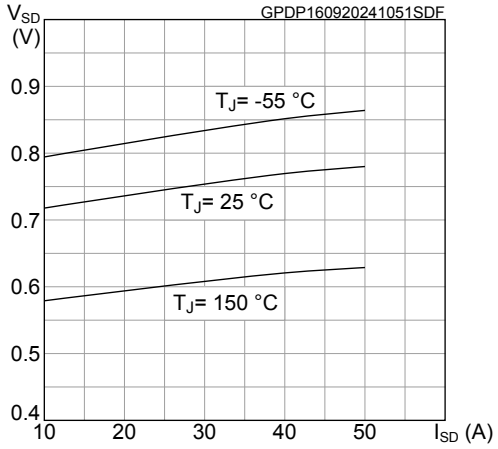
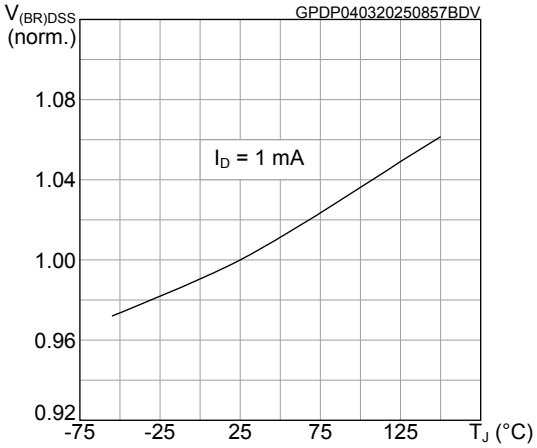


Figure 16. Normalized $V_{(BR)DSS}$ vs temperature



3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 PowerFLAT 3.3x3.3 package information

Figure 17. PowerFLAT 3.3x3.3 package outline

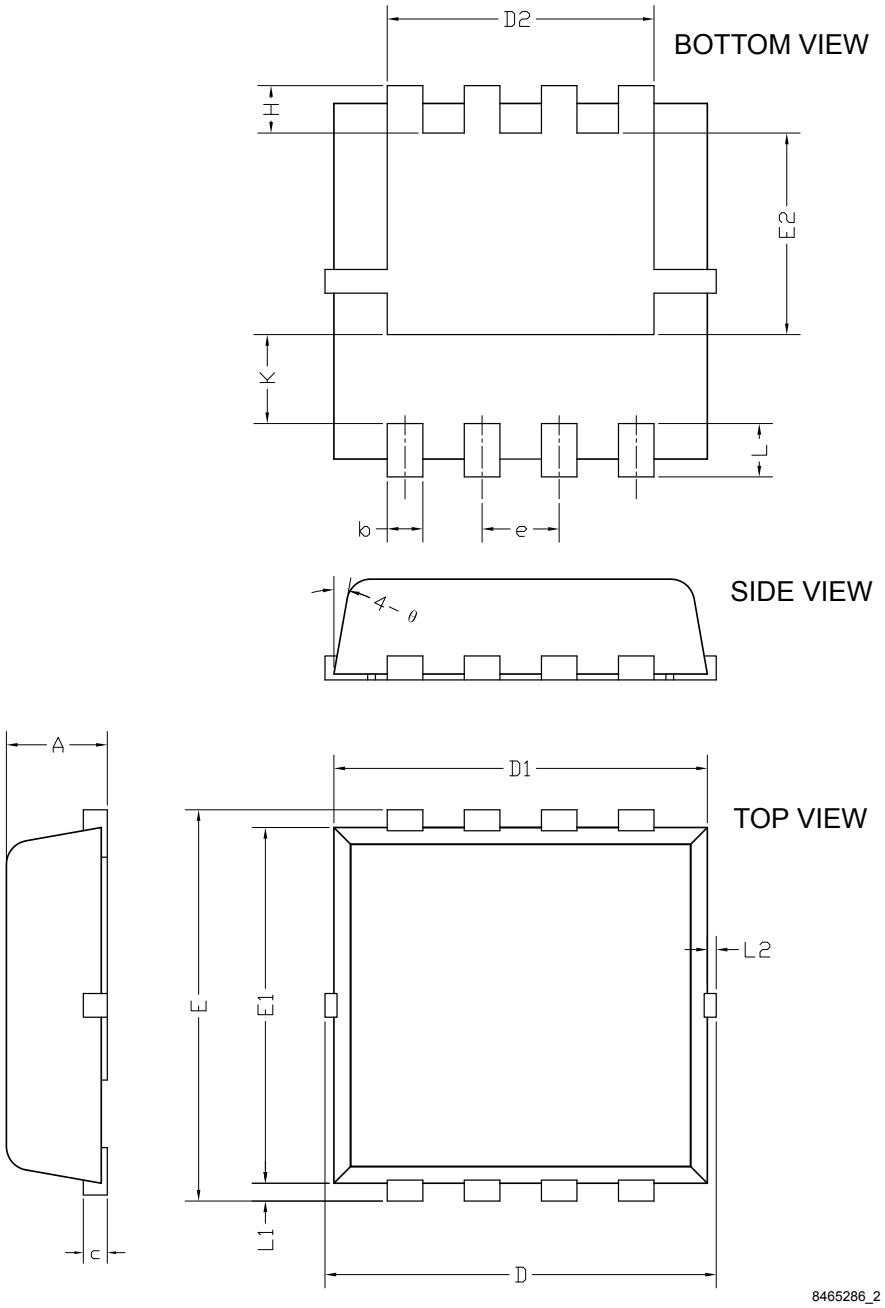
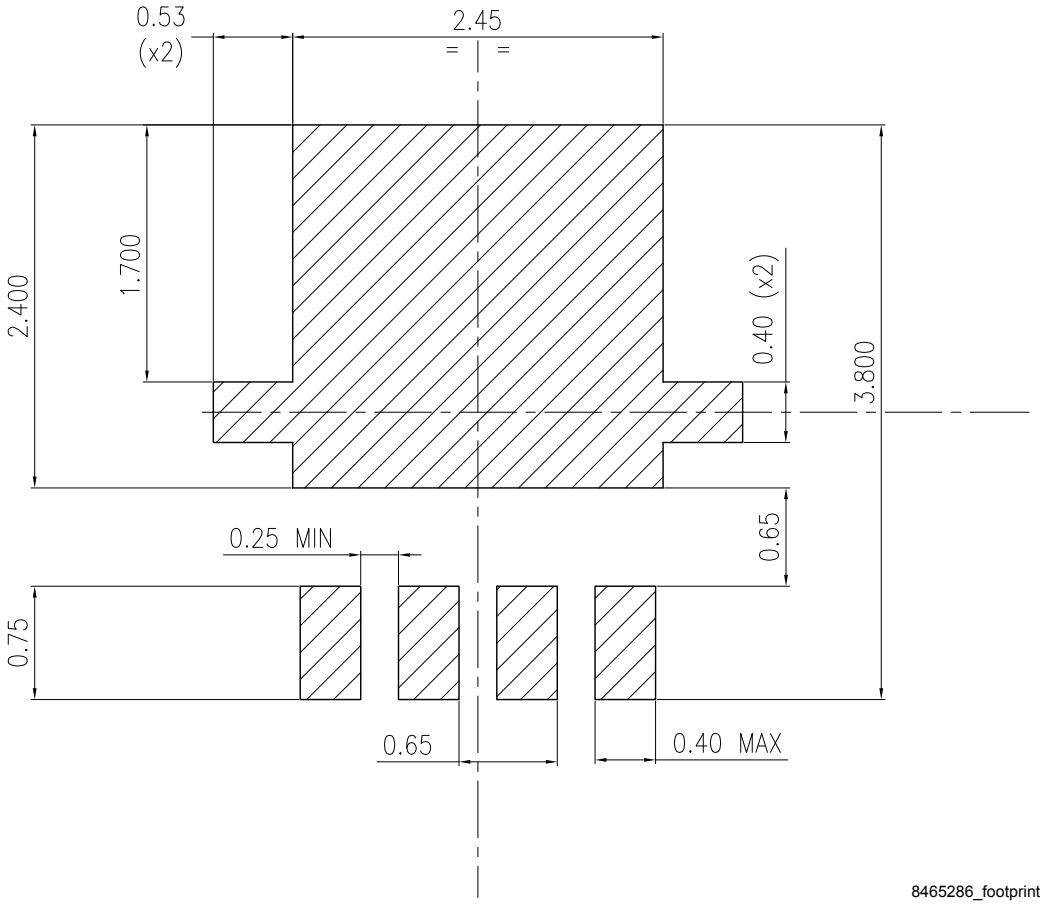


Table 7. **PowerFLAT 3.3x3.3 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.80	0.90
b	0.25	0.30	0.39
c	0.14	0.15	0.20
D	3.10	3.30	3.50
D1	3.05	3.15	3.25
D2	2.15	2.25	2.35
e	0.55	0.65	0.75
E	3.10	3.30	3.50
E1	2.90	3.00	3.10
E2	1.60	1.70	1.80
H	0.25	0.40	0.55
K	0.65	0.75	0.85
L	0.30	0.45	0.60
L1	0.05	0.15	0.25
L2			0.15
θ	8°	10°	12°

Figure 18. **PowerFLAT 3.3x3.3 recommended footprint (dimensions are in mm)**



Revision history

Table 8. **Document revision history**

Date	Revision	Changes
16-Feb-2023	1	Initial release.
20-Sep-2024	2	Modified title, *Features*, *Section Applications*, *Description* and marking on cover page. Modified *Section 1: Electrical ratings* and *Section 2: Electrical characteristics*. Updated *Section 2.1: Electrical characteristics (curves)*. Minor text changes.
05-Nov-2024	3	Updated *Figure 5. Safe operating area*.
07-Apr-2025	4	Updated *Figure 3. Typical output characteristics*, *Figure 4. Typical transfer characteristics*, *Figure 8. Typical capacitance characteristics*, *Figure 9. Avalanche characteristics*, *Figure 10. Avalanche energy*, *Figure 11. Typical drain-source on-resistance*, *Figure 12. Typical on-resistance vs gate-source voltage*, *Figure 13. Normalized on-resistance vs temperature* and *Figure 16. Normalized $V_{(BR)DSS}$ vs temperature*. Minor text changes in *Table 1. Absolute maximum ratings (at T_C = 25 °C unless otherwise specified)*.
09-Apr-2025	5	Updated Section Internal schematic on cover page.

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