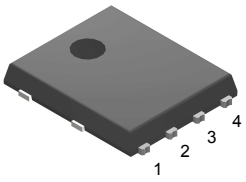
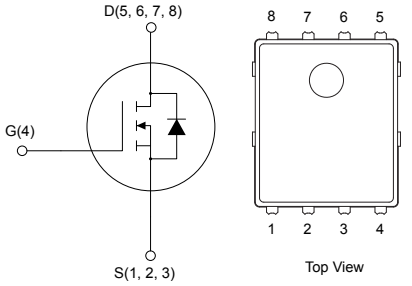
STL075N4S8AG

Datasheet

Automotive N-channel logic level 40 V, 0.75 mΩ max., 350 A Smart STripFET F8 Power MOSFET in a PowerFLAT 5x6 package



PowerFLAT 5x6



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL075N4S8AG	40 V	0.75 mΩ	350 A

- AEC-Q101 qualified
- MSL1 grade
- 175 °C operating temperature
- 100% avalanche tested
- Wettable flank package
- Extremely low $R_{DS(on)}$
- Logic level

Applications

- Power distribution

Description

The STL075N4S8AG is a 40 V N-channel enhancement mode Power MOSFET designed in Smart STripFET F8, the new dedicated STripFET F8 based technology aimed for Power distribution applications, featuring an enhanced trench gate structure.

The Smart STripFET F8 ensures an extremely low on state resistance, which makes it excellent, in combination with STi²Fuse gate drivers, for high current Power distribution units.

Product status link
STL075N4S8AG

Product summary	
Order code	STL075N4S8AG
Marking	075N4S8
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings (at T_C = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D[1]	Drain current (continuous) at T_C = 25 °C[2]	350	A
	Drain current (continuous) at T_C = 100 °C[2]	248	
	Drain current (continuous) at T_C = 25 °C[3]	120	
I_{DM}[1][2][4]	Drain current (pulsed), t_p = 10 µs	1400	A
P_{TOT}	Total power dissipation at T_C = 25 °C	167	W
I_{AS}	Single pulse avalanche current (pulse width limited by T_J max.)	60	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = 60 A, R_{Gmin} = 25 Ω)	600	mJ
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		°C

1. *Specified by design, not tested in production.*
2. *This is the theoretical current value only related to the silicon.*
3. *This current value is limited by package.*
4. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}[1]	Thermal resistance, junction-to-ambient (on 2s2p FR-4 board vertical in still area)	15.4	°C/W
R_{thJC}	Thermal resistance, junction-to-case	0.9	°C/W

1. *Defined according to JEDEC standards (JESD51-5, -7).*

2 Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	40	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 40 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125 °C(1)	-	-	100	
I_{GSS}	Gate-body leakage current	V_{GS} = 20 V, V_{DS} = 0 V	-	-	100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.2	-	2.0	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 60 A	-	0.59	0.75	mΩ
		V_{GS} = 4.5 V, I_D = 60 A	-	0.87	1.1	

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}(1)	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	7700	-	pF
C_{oss}(1)	Output capacitance		-	1570	-	pF
C_{rss}(1)	Reverse transfer capacitance		-	1520	-	pF
Q_g(1)	Total gate charge	V_{DD} = 20 V, I_D = 120 A, V_{GS} = 4.5 V	-	120	-	nC
		V_{DD} = 20 V, I_D = 120 A, V_{GS} = 10 V	-	200	-	
Q_{gs}(1)	Gate-source charge	V_{DD} = 20 V, I_D = 120 A	-	22	-	nC
Q_{gd}(1)	Gate-drain charge		-	80	-	nC

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$(1)	Turn-on delay time	V_{DD} = 20 V, I_D = 60 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	18	-	ns
t_r(1)	Rise time		-	66	-	ns
$t_{d(off)}$(1)	Turn-off delay time		-	98	-	ns
t_f(1)	Fall time		-	244	-	ns

1. *Specified by design and evaluated by characterization, not tested in production.*

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)(2)	Forward on current (continuous)	T_C = 25 °C	-	-	121	A
V_{SD}	Forward on voltage	I_{SD} = 60 A, V_{GS} = 0 V	-	-	1.1	V
t_{rr} (1)	Reverse recovery time	I_D = 60 A, di/dt = 100 A/µs, V_{DD} = 32 V	-	60	-	ns
Q_{rr} (1)	Reverse recovery charge		-	74	-	nC
I_{RRM} (1)	Reverse recovery current		-	2.5	-	A

1. *Specified by design and evaluated by characterization, not tested in production.*
2. *This is the theoretical current value only related to the silicon.*

2.1 Electrical characteristics (curves)

Figure 1. Total power dissipation

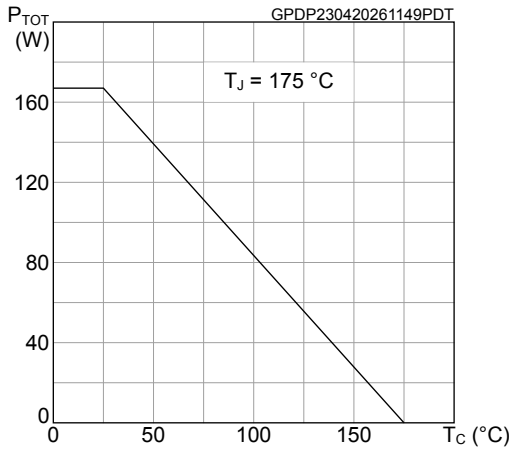


Figure 2. Drain current vs case temperature

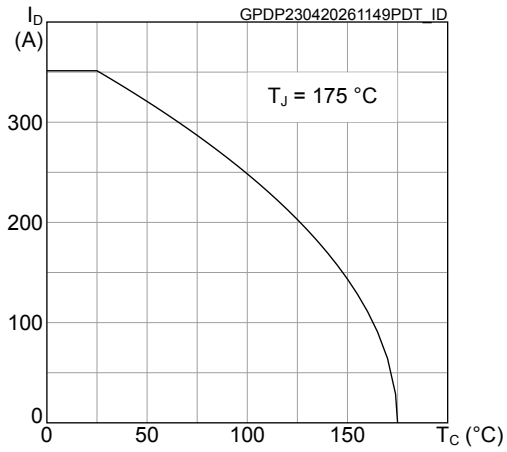


Figure 3. Typical output characteristics

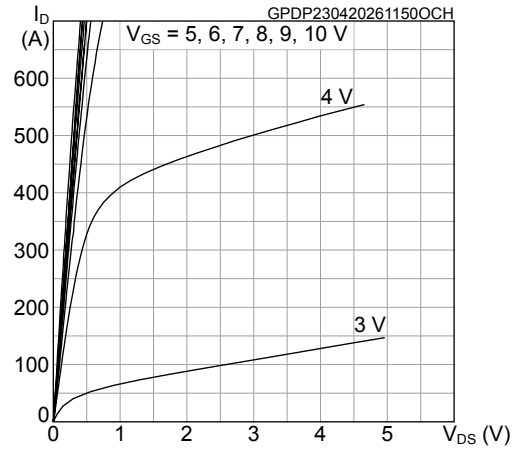


Figure 4. Typical transfer characteristics

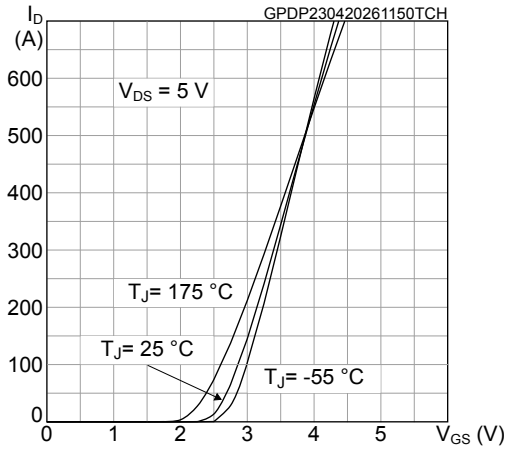


Figure 5. Safe operating area

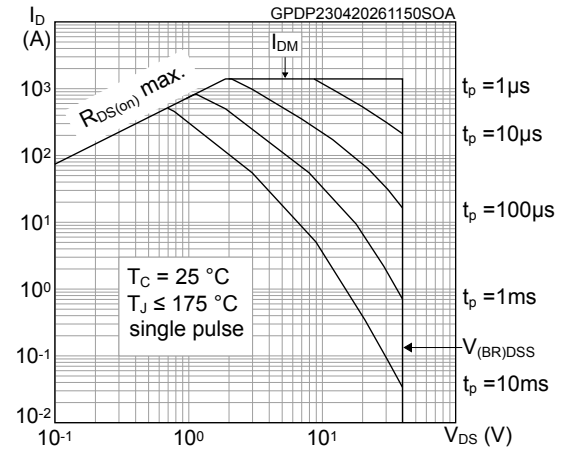


Figure 6. Normalized transient thermal impedance

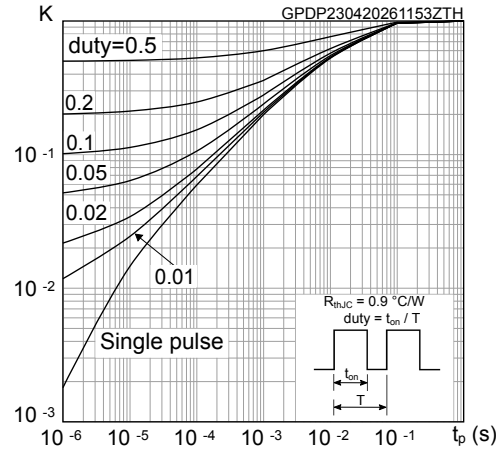


Figure 7. Typical gate charge characteristics

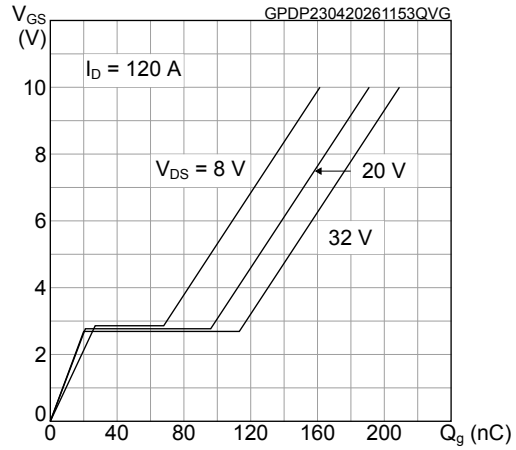


Figure 8. Typical capacitance characteristics

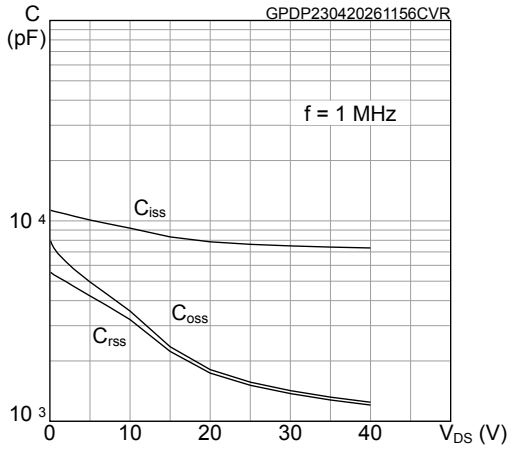


Figure 9. Avalanche characteristics

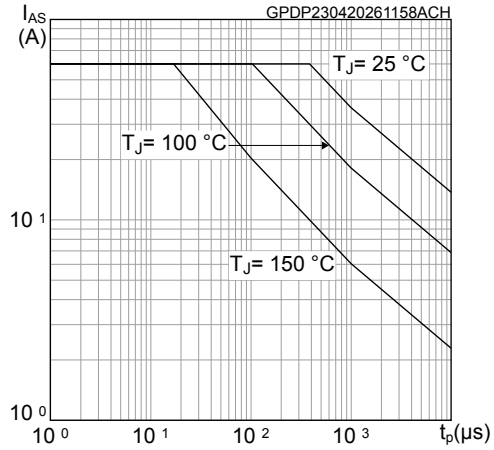


Figure 10. Avalanche energy

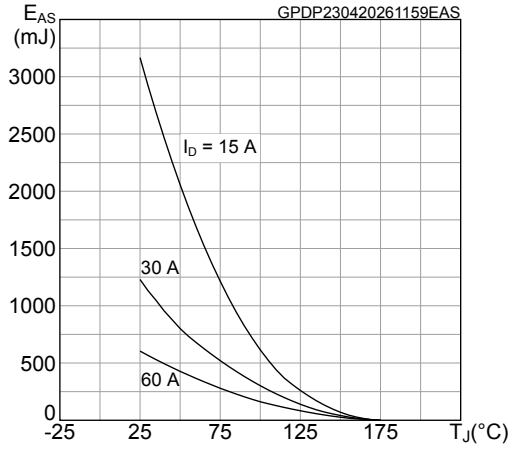


Figure 11. Typical drain-source on-resistance

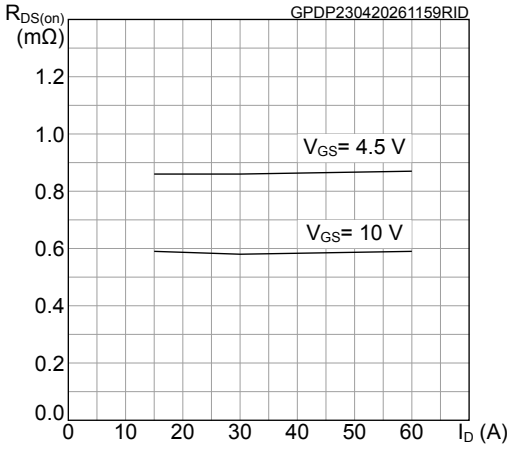


Figure 12. Typical on-resistance vs gate-source voltage

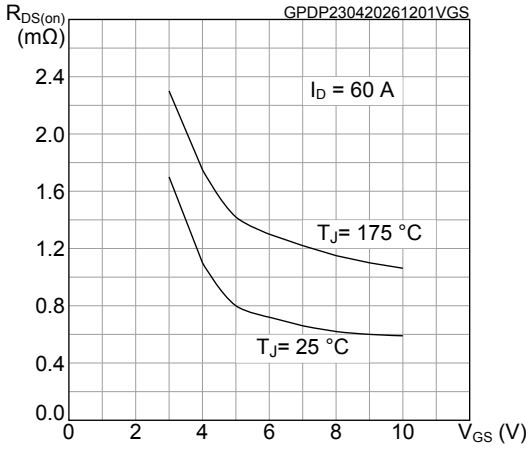


Figure 13. Normalized on-resistance vs temperature

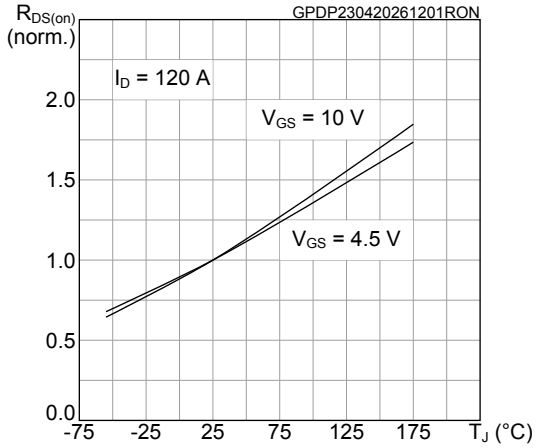


Figure 14. Normalized gate threshold voltage vs temperature

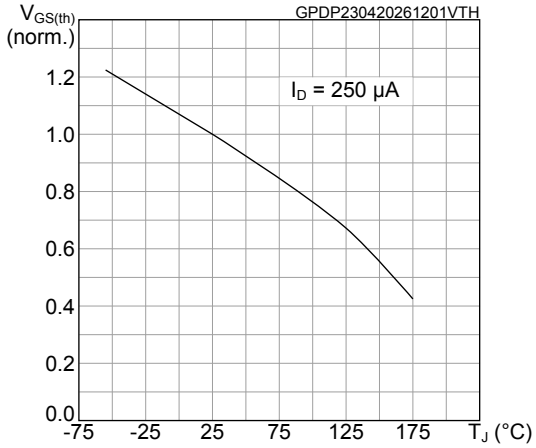


Figure 15. Typical reverse diode forward characteristics

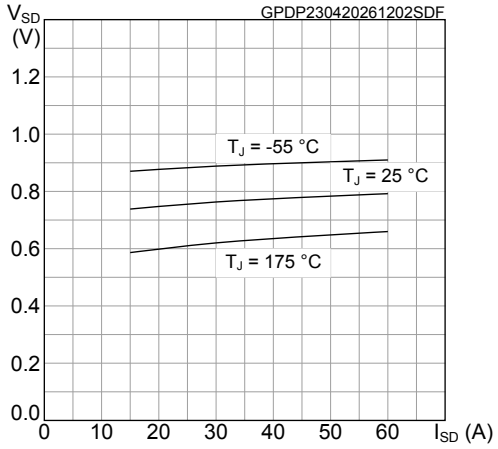
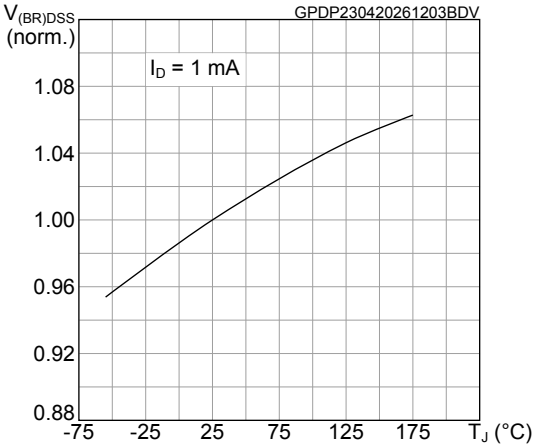


Figure 16. Normalized $V_{(BR)DSS}$ vs temperature

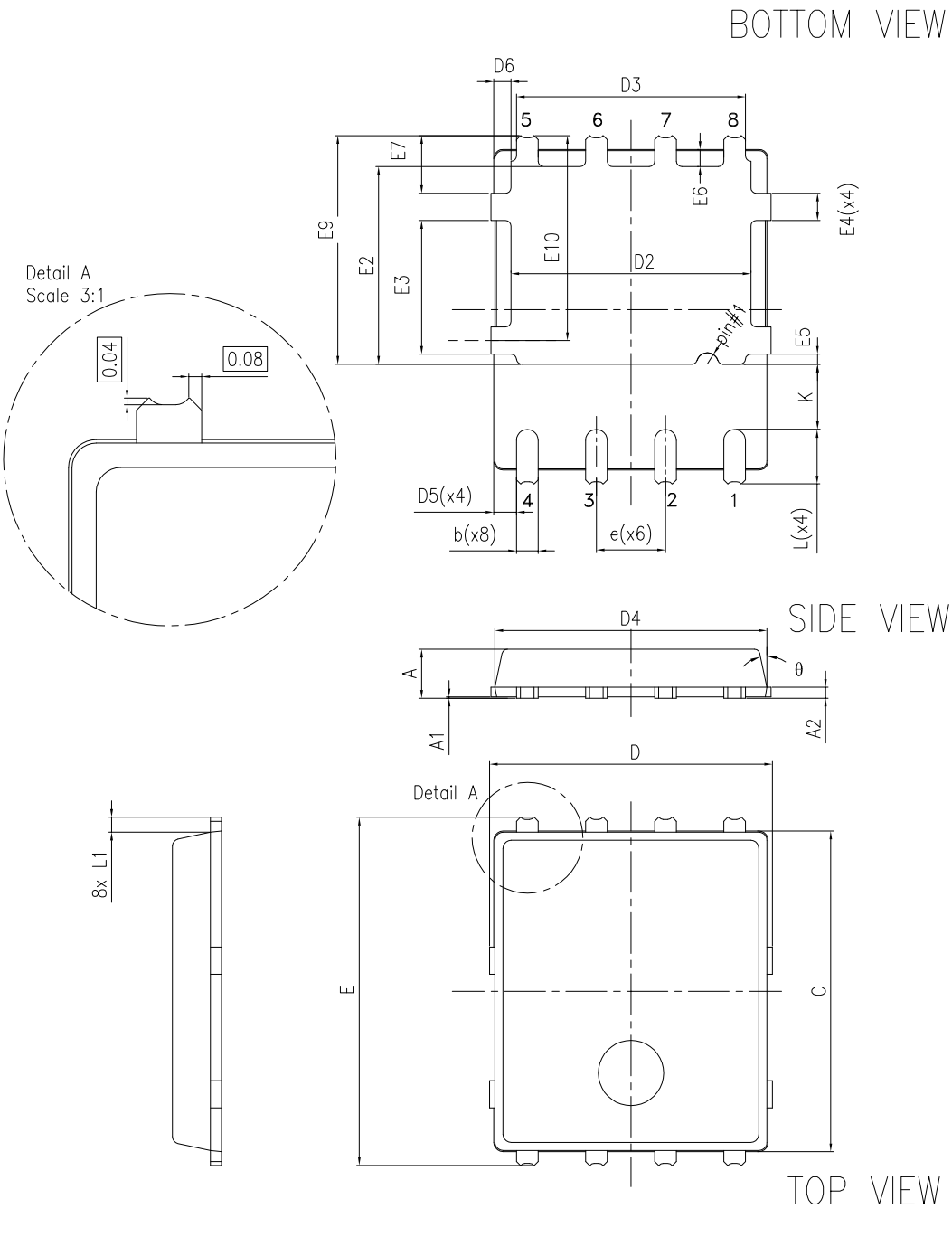


3 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 PowerFLAT 5x6 WF type C package information

Figure 17. PowerFLAT 5x6 WF type C package outline

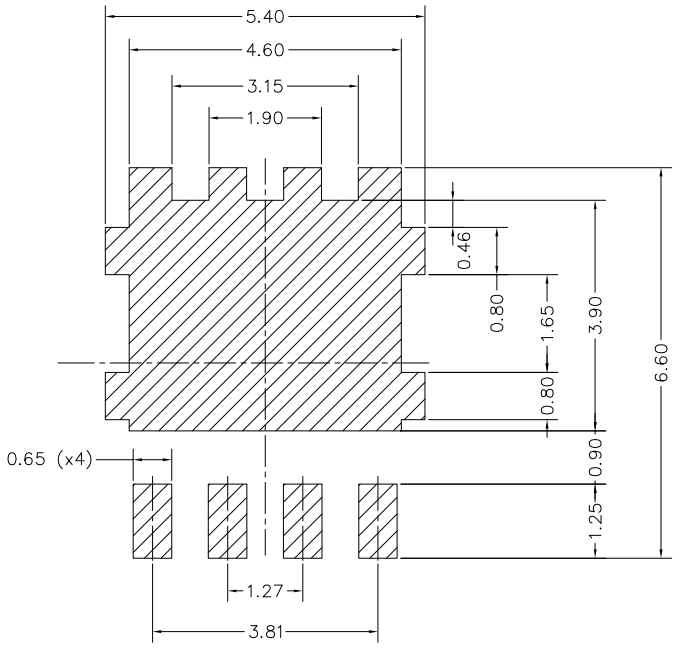


8231817_WF_typeC_r24

Table 7. **PowerFLAT 5x6 WF type C mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.00		0.05
A2	0.20	0.25	0.30
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

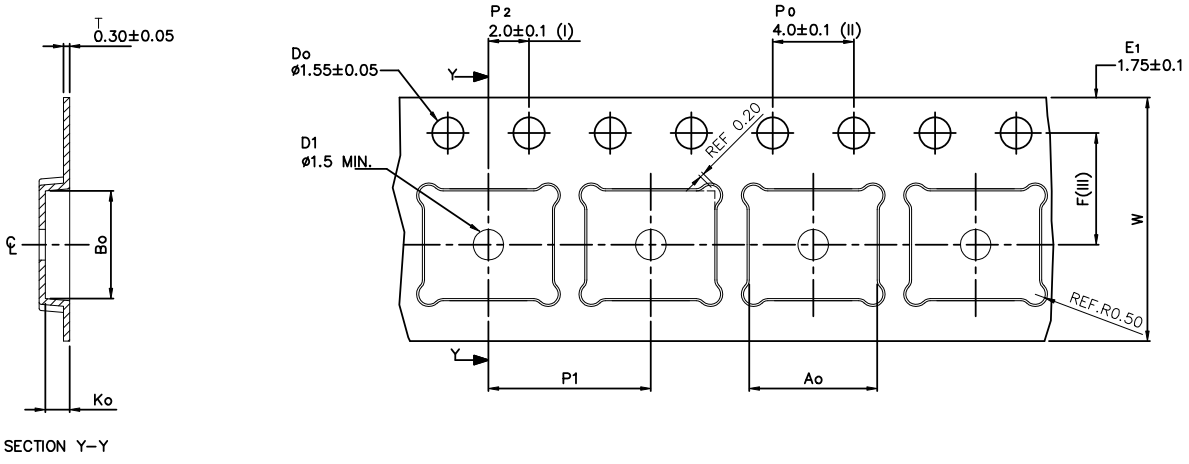
Figure 18. **PowerFLAT 5x6 recommended footprint (dimensions are in mm)**



8231817_FOOTPRINT_rev24

3.2 PowerFLAT 5x6 packing information

Figure 19. **PowerFLAT 5x6 tape (dimensions are in mm)**



Ao	6.30 +/– 0.1
Bo	5.30 +/– 0.1
Ko	1.20 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.

(II) Cumulative tolerance of 10 sprocket holes is ±0.20.

(III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs
All dimensions are in millimeters

8234350_Tape_rev_C

Figure 20. **PowerFLAT 5x6 package orientation in carrier tape**

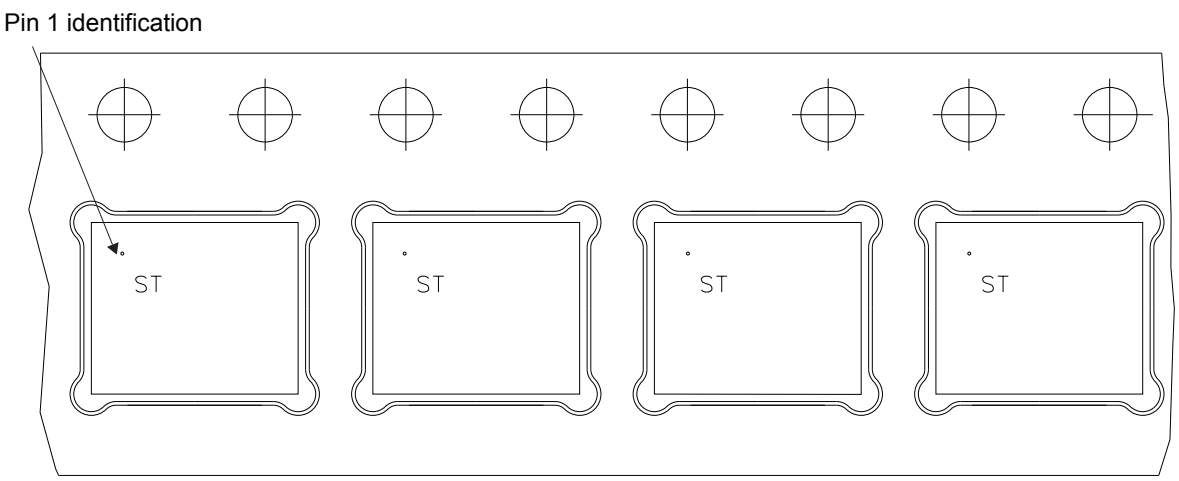
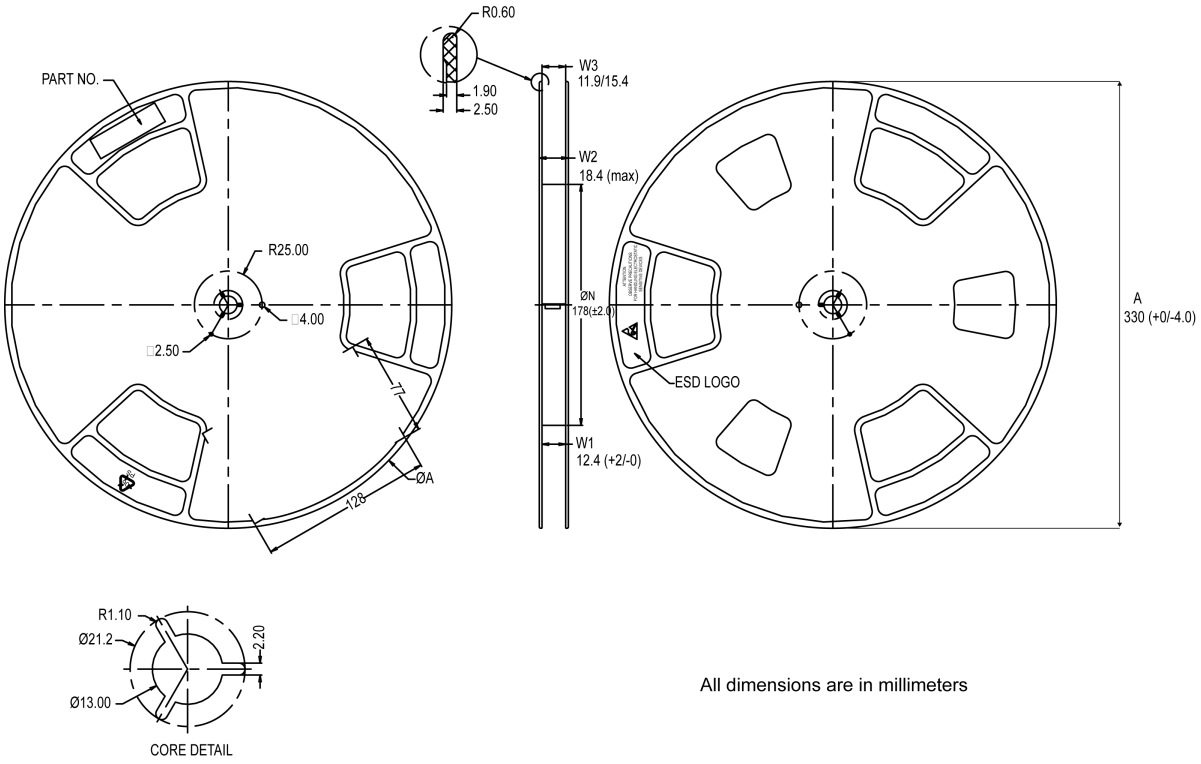


Figure 21. **PowerFLAT 5x6 reel**

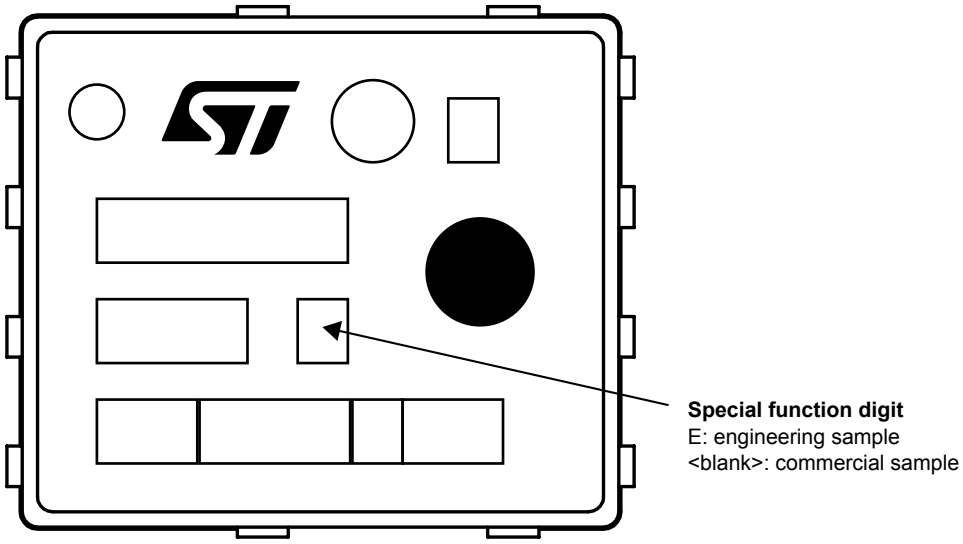


All dimensions are in millimeters

8234350_Reel_rev_C

3.3 PowerFLAT 5x6 marking information

Figure 22. **PowerFLAT 5x6 marking information**



Note: Engineering Samples: these samples can be clearly identified by a dedicated special symbol in the marking of each unit. These samples are intended to be used for electrical compatibility evaluation only; usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial Samples: fully qualified parts from ST standard production with no usage restrictions.

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
23-Apr-2026	1	First release.
11-Jun-2026	2	Updated Table 1. Absolute maximum ratings (at T_C = 25 °C unless otherwise specified). Updated Figure 5. Safe operating area. Updated Figure 6. Normalized transient thermal impedance.

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3 **Package information** 8
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