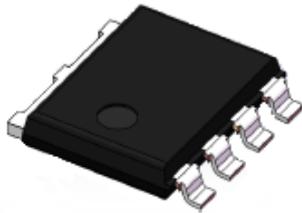
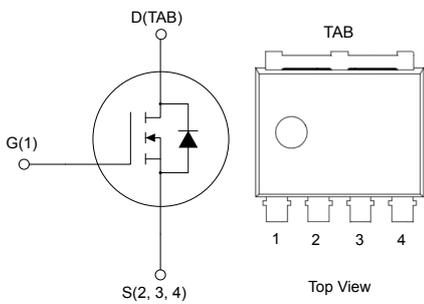


Automotive N-channel 100 V, 1.9 mΩ max., 302 A STripFET F8 Power MOSFET in a PowerLeaded 8x8 package

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STK295N10F8AG	100 V	1.9 mΩ	302 A


PowerLeaded 8x8


- AEC-Q101 qualified
- MSL1 grade
- 175 °C maximum operating junction temperature
- 100% avalanche tested
- Low gate charge Q_g

Applications

- Automotive motor control
- Body and convenience
- Chassis and safety
- Power train for ICE

Description

The **STK295N10F8AG** is a 100 V N-channel enhancement mode Power MOSFET designed in STripFET F8 technology featuring an enhanced trench gate structure. It ensures a state-of-the-art of figure of merit for very low on-state resistance while reducing internal capacitances and gate charge for faster and more efficient switching.



Product status link

[STK295N10F8AG](#)

Product summary

Order code	STK295N10F8AG
Marking⁽¹⁾	295N10F8
Package	PowerLeaded 8x8
Packing	Tape and reel

1. Engineering samples are clearly identified with a dedicated special symbol in the marking of each unit.

1 Electrical ratings

Table 1. Absolute maximum ratings (at $T_C = 25\text{ °C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}^{(2)}$	302	A
	Drain current (continuous) at $T_C = 100\text{ °C}^{(2)}$	214	
	Drain current (continuous) at $T_C = 25\text{ °C}^{(3)}$	200	
$I_{DM}^{(1)(2)(4)}$	Drain current (pulsed), $t_p = 10\text{ }\mu\text{s}$	1209	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	382	W
I_{AS}	Single pulse avalanche current (pulse width limited by T_J max.)	90	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = 90\text{ A}$, $R_G = 25\text{ }\Omega$)	394	mJ
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

1. Specified by design and evaluated by characterization, not tested in production.
2. This is the theoretical current value only related to the silicon.
3. This current value is limited by package.
4. Pulse width is limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient (on 2s2p FR-4 board vertical in still area)	14.2	°C/W
R_{thJC}	Thermal resistance, junction-to-case	0.39	°C/W

1. Defined according to JEDEC standards (JESD51-5, -7).

2 Electrical characteristics

$T_J = 25\text{ °C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	100			V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 90\text{ A}$		1.5	1.9	m Ω

1. Specified by design and evaluated by characterization, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}^{(1)}$	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	8740	-	pF
$C_{oss}^{(1)}$	Output capacitance		-	1850	-	pF
$C_{rss}^{(1)}$	Reverse transfer capacitance		-	40	-	pF
$Q_g^{(1)}$	Total gate charge	$V_{DD} = 50\text{ V}$, $I_D = 180\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$	-	130	-	nC
$Q_{gs}^{(1)}$	Gate-source charge		-	45	-	nC
$Q_{gd}^{(1)}$	Gate-drain charge		-	30	-	nC

1. Specified by design and evaluated by characterization, not tested in production.

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}^{(1)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$, $I_D = 90\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	29	-	ns
$t_r^{(1)}$	Rise time		-	19	-	ns
$t_{d(off)}^{(1)}$	Turn-off delay time		-	65	-	ns
$t_f^{(1)}$	Fall time		-	27	-	ns

1. Specified by design and evaluated by characterization, not tested in production.

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Forward on current (continuous)	$T_C = 25\text{ }^\circ\text{C}$	-		256	A
V_{SD}	Forward on voltage	$I_{SD} = 90\text{ A}, V_{GS} = 0\text{ V}$	-		1.2	V
$t_{rr}^{(1)}$	Reverse recovery time	$I_D = 90\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 80\text{ V}$	-	80		ns
$Q_{rr}^{(1)}$	Reverse recovery charge		-	160		nC
$I_{RRM}^{(1)}$	Reverse recovery current		-	4		A

1. Specified by design and evaluated by characterization, not tested in production.

2.1 Electrical characteristics (curves)

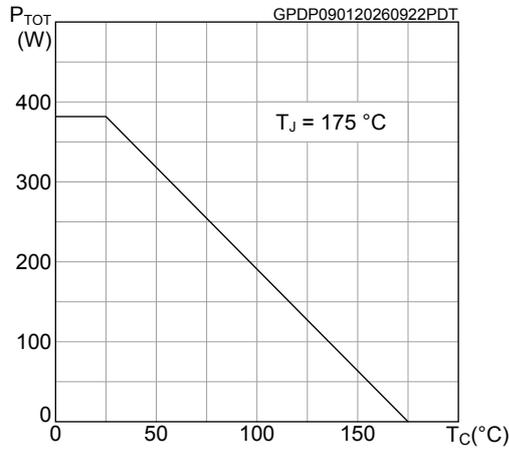
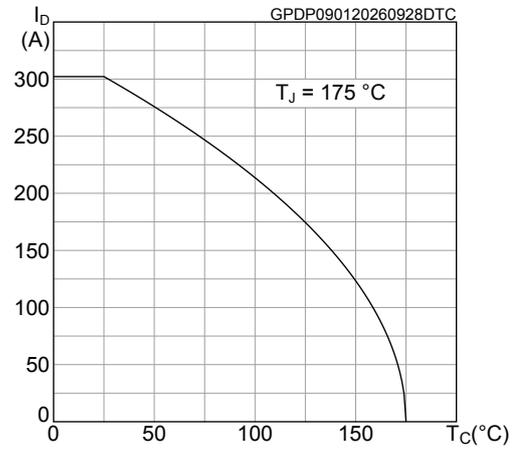
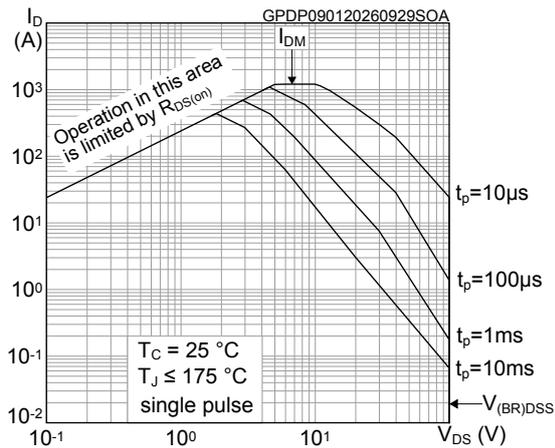
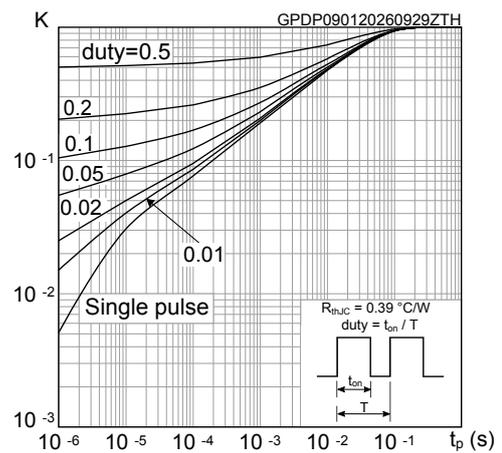
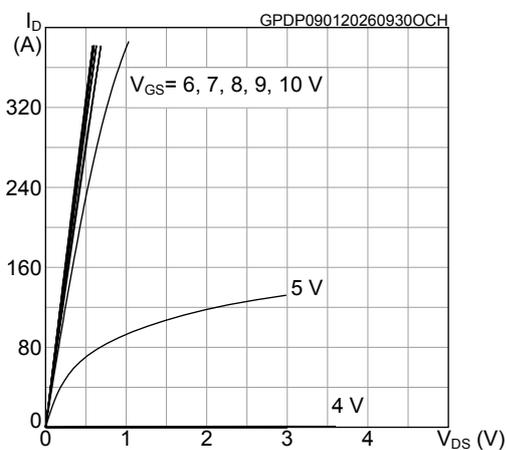
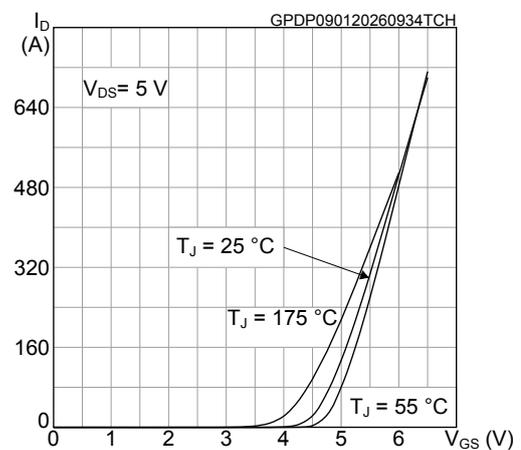
Figure 1. Total power dissipation

Figure 2. Drain current vs case temperature

Figure 3. Safe operating area

Figure 4. Normalized transient thermal impedance

Figure 5. Typical output characteristics

Figure 6. Typical transfer characteristics


Figure 7. Typical gate charge characteristics

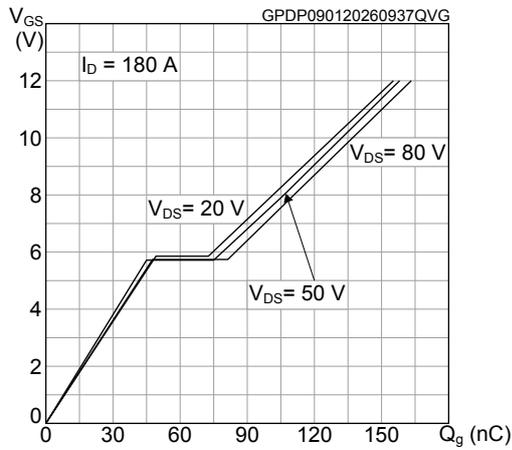


Figure 8. Typical capacitance characteristics

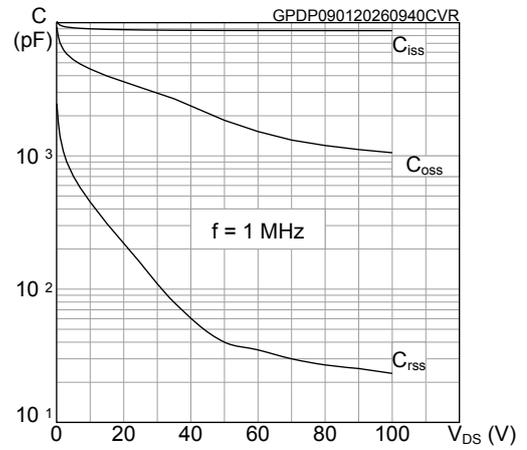


Figure 9. Avalanche characteristics

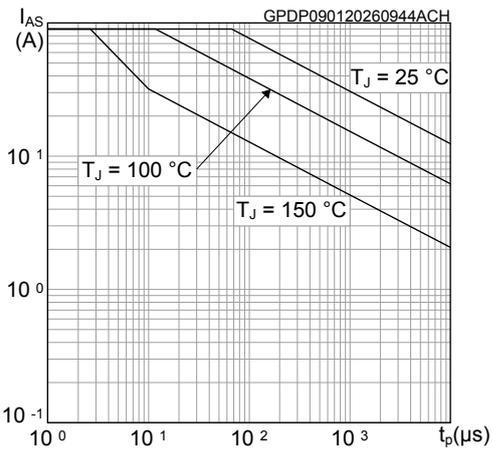


Figure 10. Avalanche energy

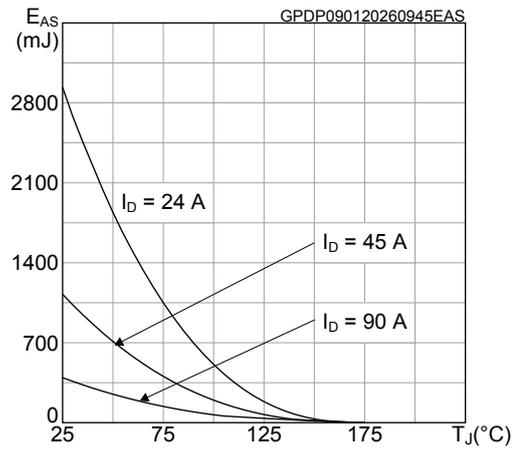


Figure 11. Typical drain-source on-resistance

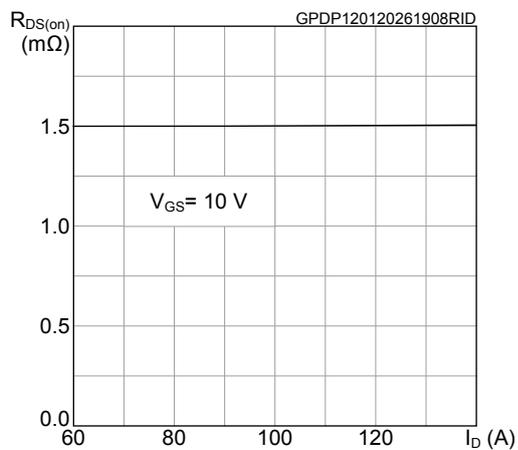


Figure 12. Typical on-resistance vs. gate-source voltage

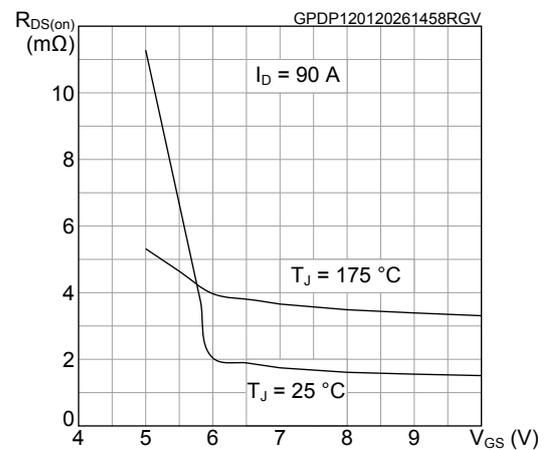


Figure 13. Normalized on-resistance vs temperature

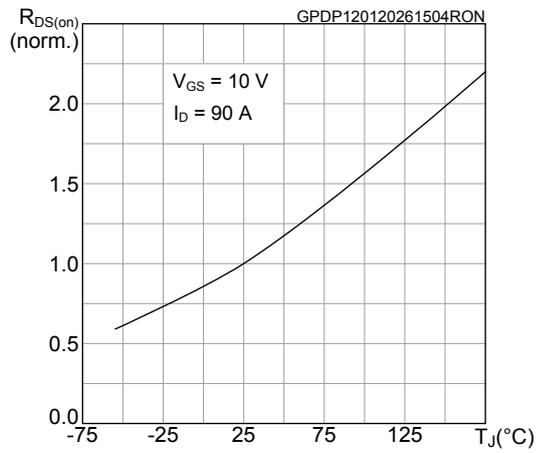


Figure 14. Normalized gate threshold voltage vs temperature

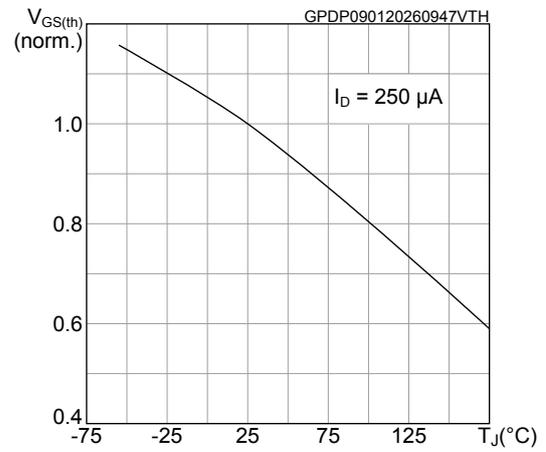


Figure 15. Typical reverse diode forward characteristics

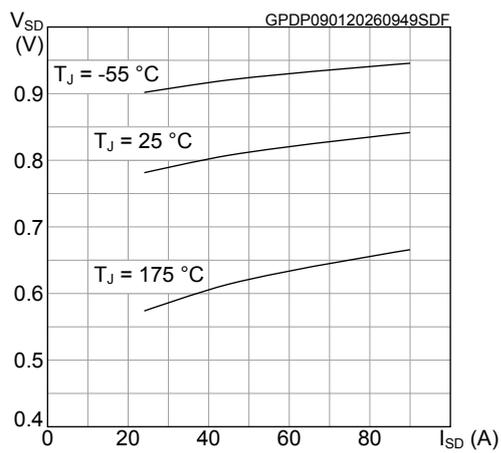
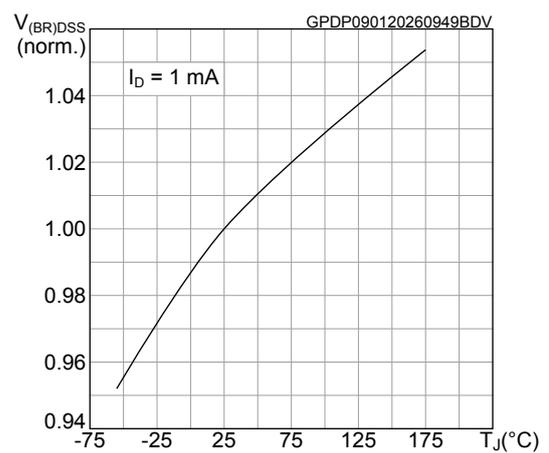


Figure 16. Normalized V_{(BR)DSS} vs temperature

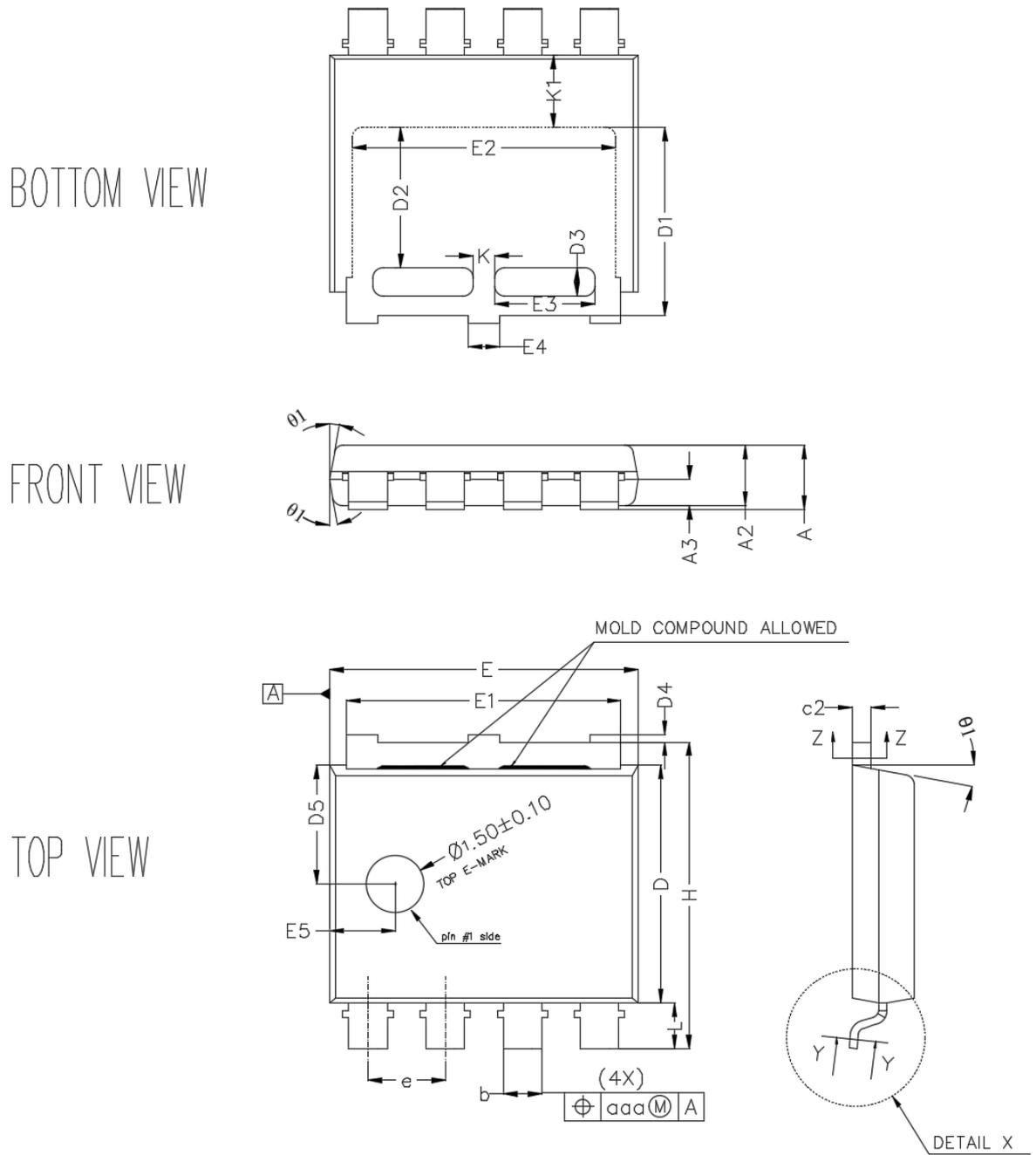


3 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 PowerLeaded 8x8 package information

Figure 17. PowerLeaded 8x8 package outline



DM00548355_Rev_5

Table 7. PowerLeaded 8x8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.85
A1	0.00	0.08	0.15
A2	1.50	1.60	1.70
A3	0.60	0.70	0.80
b	0.90	1.00	1.10
c	0.20		0.25
c1	0.19	0.20	0.21
c2	0.49		0.56
c3	0.48	0.50	0.52
D	6.10	6.20	6.30
D1	4.75	4.90	5.05
D2	3.50	3.65	3.80
D3	0.65	0.75	0.85
D4			0.20
D5	2.90	3.10	3.30
E	7.90	8.00	8.10
E1	6.95	7.10	7.25
E2	6.70	6.80	6.90
E3	2.50	2.60	2.70
E4	0.65	0.80	0.95
E5	1.50	1.70	1.90
e	1.90	2.00	2.10
H	7.85	8.00	8.15
K	0.45	0.55	0.65
K1	1.75	1.90	2.05
L	1.00	1.20	1.30
L1	0.60	0.70	0.80
L2		0.23BSC	
R		0.20REF	
aaa		0.250	
bbb		0.100	
θ	0°		8°
θ1	6°	10°	14°

Revision history

Table 8. Document revision history

Date	Revision	Changes
26-Oct-2022	1	First release.
26-Jun-2025	2	Updated <i>Features</i> , <i>Applications</i> and <i>Description</i> in cover page. Updated <i>Section 1: Electrical ratings</i> , <i>Section 2: Electrical characteristics</i> and <i>Section 3: Package information</i> .
29-Jan-2026	3	Updated <i>Table 1. Absolute maximum ratings (at $T_c = 25\text{ °C}$ unless otherwise specified)</i> . Updated <i>Section 2: Electrical characteristics</i> . Added <i>Section 2.1: Electrical characteristics (curves)</i> .
06-Mar-2026	4	Updated <i>Figure 7. Typical gate charge characteristics</i> and <i>Figure 16. Normalized $V_{(BR)DSS}$ vs temperature</i> . Updated <i>Section 3.1: PowerLeaded 8x8 package information</i> . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Package information	8
3.1	PowerLeaded 8x8 package information	9
3.1.1	PowerLeaded 8x8 package information	12
	Revision history	13

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