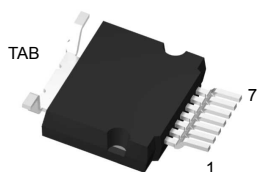
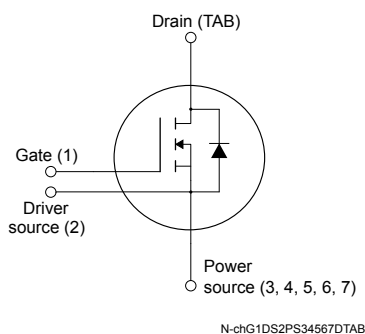


Automotive-grade N-channel 650 V, 83 mΩ typ., 26 A MDmesh DM9 Power MOSFET in an HU3PAK package



HU3PAK



Product status link

[STHU65N110DM9AG](#)

Product summary

Order code	STHU65N110DM9AG
Marking	65A110DM9
Package	HU3PAK
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STHU65N110DM9AG	650 V	110 mΩ	26 A

- AEC-Q101 qualified 
- Fast-recovery body diode
- Very low FOM (R_{DS(on)} · Q_g)
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Excellent switching performance thanks to the extra driving source pin

Applications

- DC/DC converter for EV/HEV
- On board charger (OBC)

Description

This N-channel Power MOSFET is based on the most innovative super-junction MDmesh DM9 technology, suitable for medium/high voltage MOSFETs featuring very low R_{DS(on)} per area coupled with a fast-recovery diode. The silicon-based DM9 technology benefits from a multi-drain manufacturing process which allows an enhanced device structure. The fast-recovery diode featuring very low recovery charge (Q_{rr}), time (t_{rr}) and R_{DS(on)} makes this fast-switching super-junction Power MOSFET tailored for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	26	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	16	
$I_{DM}^{(1)}$	Drain current (pulsed)	97	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	179	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	120	V/ns
$di/dt^{(2)}$	Peak diode recovery current slope	900	A/ μ s
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	120	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 13\text{ A}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.7	$^{\circ}\text{C/W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	30	$^{\circ}\text{C/W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_J max.)	5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	307	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$	-	-	5	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$	-	-	± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.5	4.0	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 13\text{ A}$	-	83	110	m Ω

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 400\text{ V}$, $f = 250\text{ kHz}$, $V_{GS} = 0\text{ V}$	-	2133	-	pF
C_{oss}	Output capacitance		-	41	-	pF
$C_{oss\text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	330	-	pF
R_g	Intrinsic gate resistance	$f = 250\text{ kHz}$, open drain	-	1.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 13\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 14. Test circuit for gate charge behavior)	-	46	-	nC
Q_{gs}	Gate-source charge		-	12	-	nC
Q_{gd}	Gate-drain charge		-	17	-	nC

1. $C_{oss\text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 13\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	15	-	ns
t_r	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	49	-	ns
t_f	Fall time		-	4	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	26	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	97	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 26\text{ A}$	-	1.1	1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 26\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 150\text{ V}$	-	130	-	ns
Q_{rr}	Reverse recovery charge		-	0.74	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	10.5	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 26\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 150\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	165	-	ns
Q_{rr}	Reverse recovery charge		-	1.3	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	14	-	A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

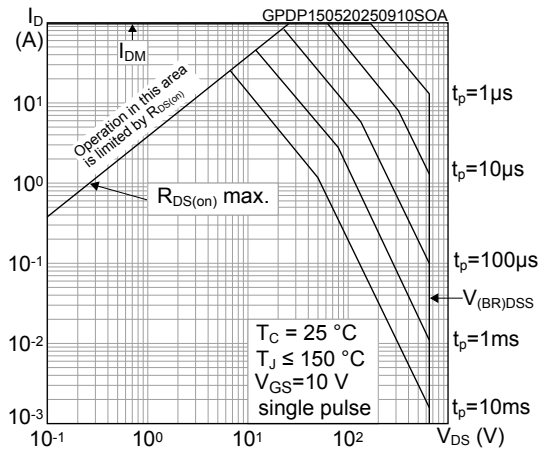
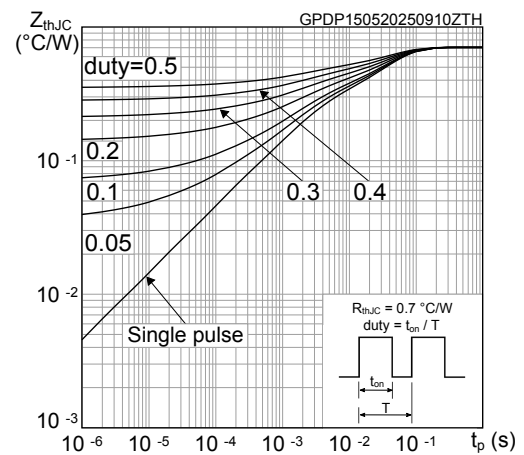
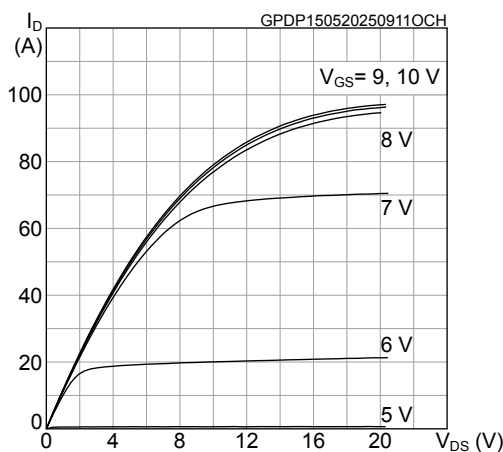
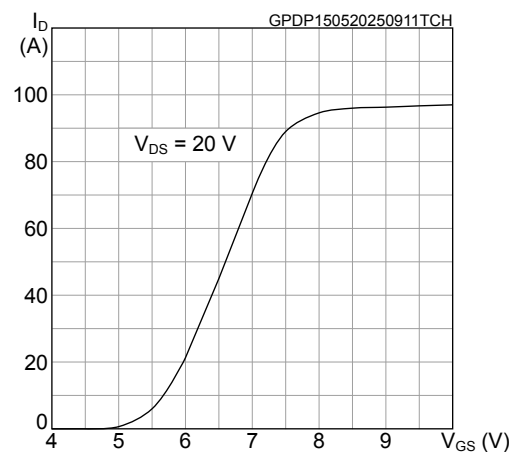
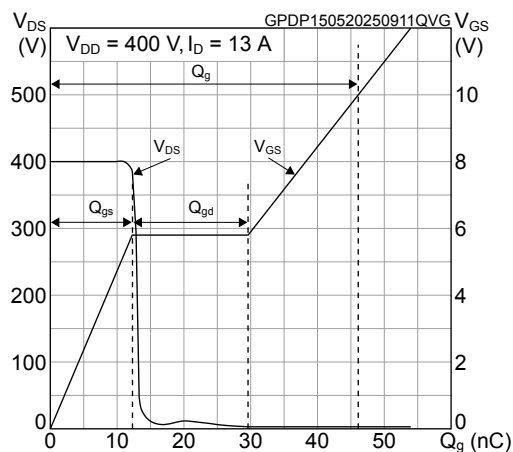
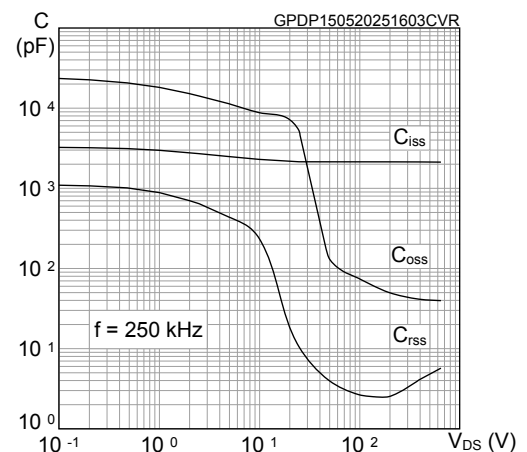
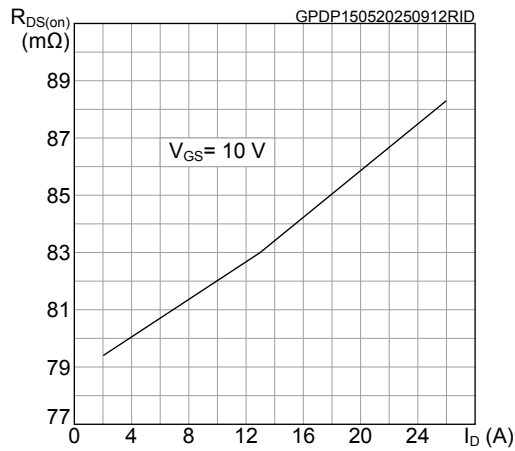
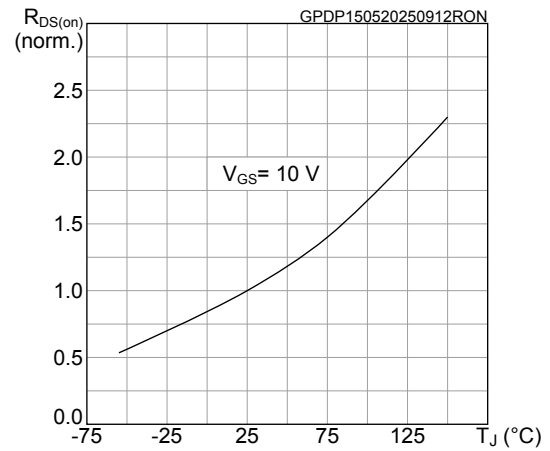
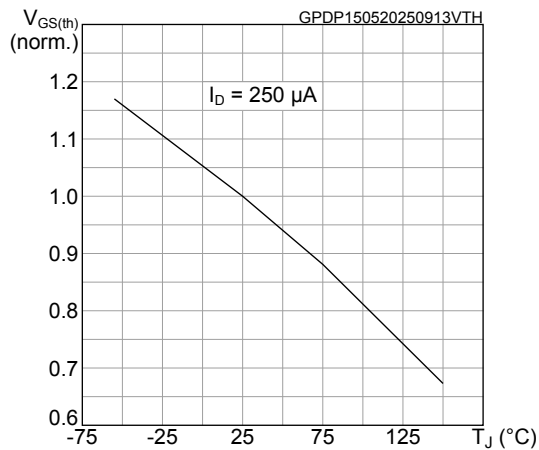
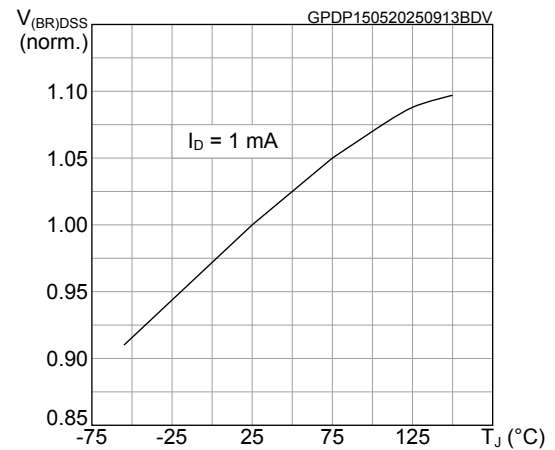
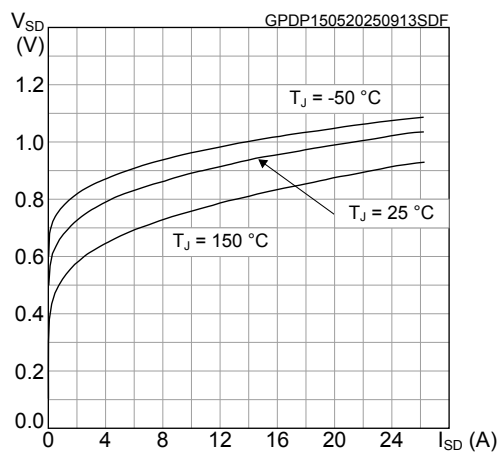
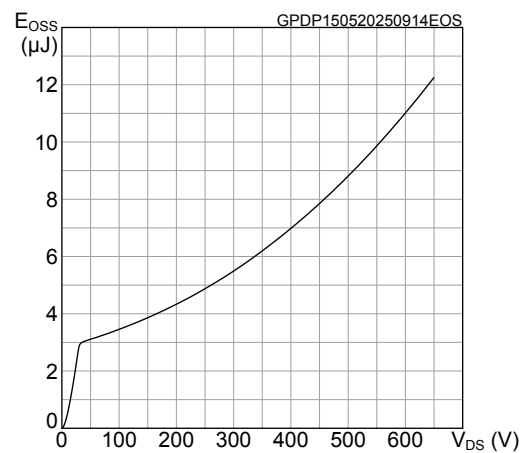
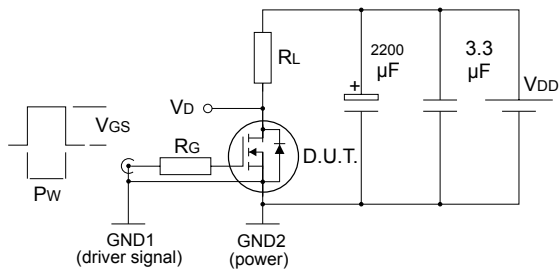
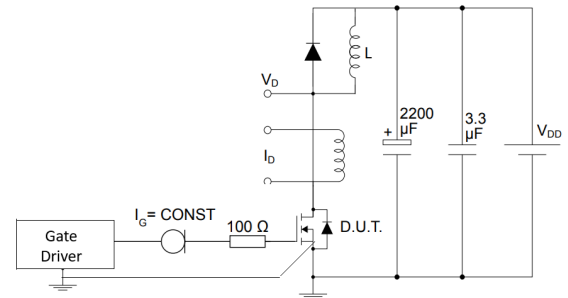
Figure 1. Safe operating area

Figure 2. Maximum transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical capacitance characteristics


Figure 7. Typical drain-source on-resistance

Figure 8. Normalized on-resistance vs temperature

Figure 9. Normalized gate threshold vs temperature

Figure 10. Normalized breakdown voltage vs temperature

Figure 11. Typical reverse diode forward characteristics

Figure 12. Typical output capacitance stored energy


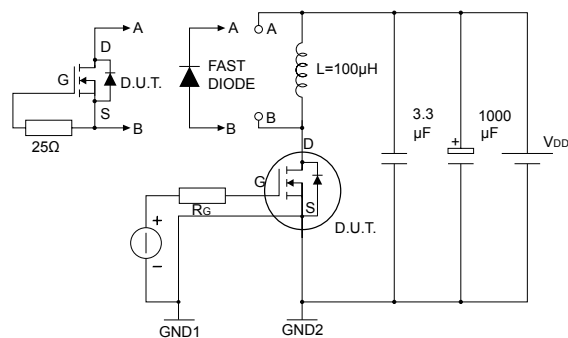
3 Test circuits

Figure 13. Switching times test circuit for resistive load


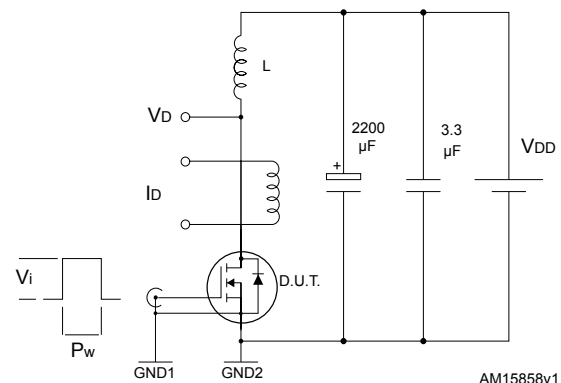
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Figure 14. Test circuit for gate charge behavior


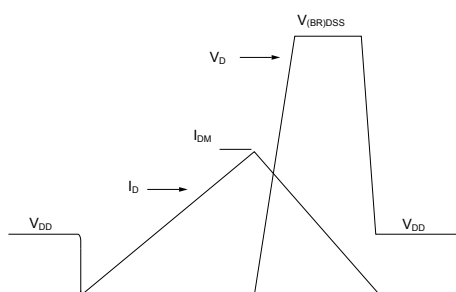
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Figure 15. Test circuit for inductive load switching and diode recovery times


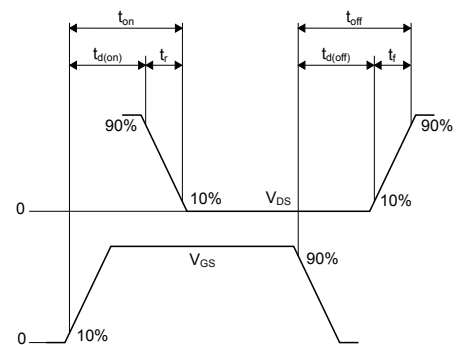
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


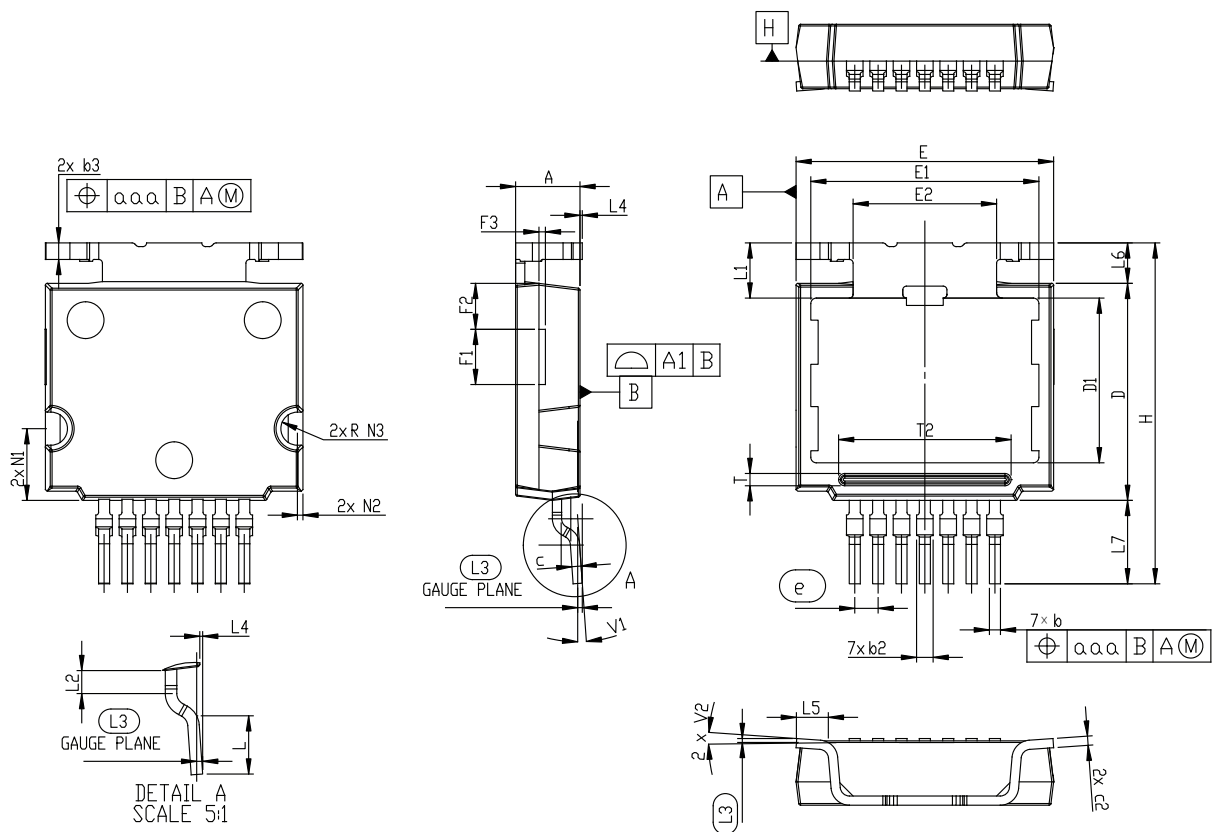
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 HU3PAK package information

Figure 19. HU3PAK package outline



DM00674007_2

Table 8. HU3PAK package mechanical data

Ref.	Dimensions		
	mm		
	Min.	Typ.	Max.
A	3.40	3.50	3.60
A1		0.05	
b	0.50	0.60	0.70
b2	0.50	0.70	1.00
b3	0.80	0.90	1.00
c	0.40	0.50	0.60
c2	0.40	0.50	0.60
D	11.70	11.80	11.90
D1	8.80	8.955	9.10
E	13.90	14.00	14.10
E1	12.30	12.40	12.50
E2	7.75	7.80	7.85
e		1.27	
H	18.00	18.58	19.00
aaa		0.10	
L	2.40	2.52	2.60
L1		3.05	
L2	0.90	1.00	1.10
L3		0.26	
L4	0.075	0.125	0.175
L5	1.83	1.93	2.03
L6	2.14	2.24	2.34
L7	4.44	4.54	4.64
F1	2.90	3.00	3.10
F2	2.40	2.50	2.60
F3	0.25	0.35	0.45
N1	3.80	3.90	4.00
N2	0.25	0.30	0.45
N3	0.80	0.90	1.00
T	0.50	0.67	0.70
T2	9.18	9.38	9.43
V1		0 °	8 °
V2		0 °	8 °

Technical drawing of a mechanical part, likely a bracket or support, showing dimensions in millimeters (mm). The drawing includes a top view and a side view.

Top View Dimensions:

- Overall width: 14.70
- Distance from left edge to centerline: 2.45
- Distance from centerline to right edge: 11.80 (calculated as 14.70 - 2.45)

Side View Dimensions:

- Overall height: 19.00
- Distance from bottom edge to the start of the vertical section: 1.50
- Width of the vertical section: 3.00
- Width of the base: 6 × 1.27 (indicating 6 holes, each 1.27 mm wide)
- Width of the base flange: 7 × 0.90 (indicating 7 holes, each 0.90 mm wide)

Figure 21. HU3PAK carrier tape outline

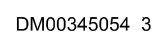
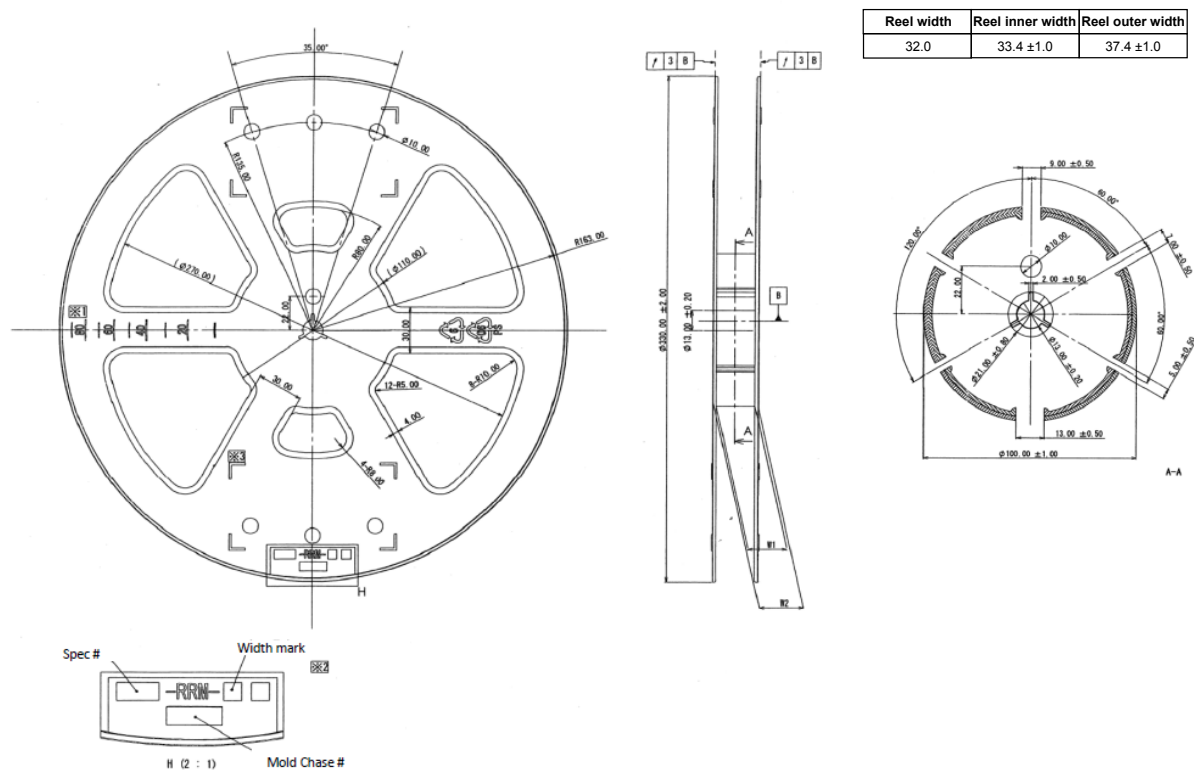


Table 9. HU3PAK tape mechanical data

Dimension	Value
	mm
A0	14.40 ±0.10
B0	19.70
D	1.50 ±0.10
E	1.75 ±0.10
F	15.65 ±0.10
I0	11.00
I1	11.60 ±0.10
I2	8.00
I3	7.00
K0	4.20
P0	4.00 ±0.10
P1	20.00 ±0.10
P2	2.00 ±0.10
T	0.40 ±0.50
W	32.00 ±0.30

Figure 22. HU3PAK reel outline (dimensions are in mm)



DM00345054_3_reel

Revision history

Table 10. Document revision history

Date	Revision	Changes
15-May-2025	1	First release.

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