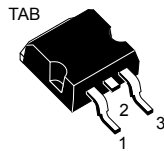
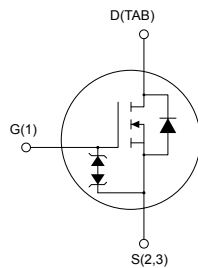


## N-channel 950 V, 1 $\Omega$ typ., 6 A MDmesh K5 Power MOSFET in an H<sup>2</sup>PAK-2 package



H<sup>2</sup>PAK-2



NCHG10TAB523TZ



### Features

| Order code  | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|-------------|----------|-------------------|-------|
| STH6N95K5-2 | 950 V    | 1.25 $\Omega$     | 6 A   |

- Ultra-low gate charge
- Very low FoM (figure of merit)
- Zener-protected
- 100% avalanche tested

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

#### Product status link

[STH6N95K5-2](#)

#### Product summary

|            |                      |
|------------|----------------------|
| Order code | STH6N95K5-2          |
| Marking    | 6N95K5               |
| Package    | H <sup>2</sup> PAK-2 |
| Packing    | Tape and reel        |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value      | Unit               |
|----------------|-------------------------------------------------------------------|------------|--------------------|
| $V_{GS}$       | Gate-source voltage                                               | $\pm 30$   | V                  |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 6          | A                  |
|                | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 3.8        |                    |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 24         | A                  |
| $P_{TOT}$      | Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$     | 110        | W                  |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 4.5        | V/ns               |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                         | 50         | V/ns               |
| $T_{stg}$      | Storage temperature range                                         | -55 to 150 | $^{\circ}\text{C}$ |
| $T_J$          | Operating junction temperature range                              |            | $^{\circ}\text{C}$ |

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 6\text{ A}$ ,  $V_{DS} \text{ (peak)} < V_{(BR)DSS}$ ,  $di/dt = 100\text{ A}/\mu\text{s}$ .
3.  $V_{DD} = 760\text{ V}$ .

**Table 2. Thermal data**

| Symbol           | Parameter                               | Value | Unit                        |
|------------------|-----------------------------------------|-------|-----------------------------|
| $R_{thJC}$       | Thermal resistance, junction-to-case    | 1.14  | $^{\circ}\text{C}/\text{W}$ |
| $R_{thJA}^{(1)}$ | Thermal resistance, junction-to-ambient | 30    | $^{\circ}\text{C}/\text{W}$ |

1. When mounted on a standard 1 inch<sup>2</sup> area of FR-4 PCB with 2-oz copper.

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                              | Value | Unit |
|----------|------------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_J$ max.)                                    | 3     | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 90    | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

**Table 4. On/off-states**

| Symbol        | Parameter                         | Test conditions                                                                                      | Min. | Typ. | Max.     | Unit          |
|---------------|-----------------------------------|------------------------------------------------------------------------------------------------------|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                                          | 950  |      |          | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 950\text{ V}$                                                      |      |      | 1        | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 950\text{ V}$ , $T_C = 125\text{ }^{\circ}\text{C}$ <sup>(1)</sup> |      |      | 50       |               |
| $I_{GSS}$     | Gate-body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$                                                   |      |      | $\pm 10$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$                                                   | 3    | 4    | 5        | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 3\text{ A}$                                                          |      | 1    | 1.25     | $\Omega$      |

1. Specified by design, not tested in production.

**Table 5. Dynamic characteristics**

| Symbol            | Parameter                              | Test conditions                                                                                     | Min. | Typ. | Max. | Unit     |
|-------------------|----------------------------------------|-----------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$         | Input capacitance                      | $V_{DS} = 100\text{ V}$ , $f = 1\text{ kHz}$ , $V_{GS} = 0\text{ V}$                                | -    | 450  | -    | pF       |
| $C_{oss}$         | Output capacitance                     |                                                                                                     | -    | 30   | -    | pF       |
| $C_{rss}$         | Reverse transfer capacitance           |                                                                                                     | -    | 1.6  | -    | pF       |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance, time-related   | $V_{DS} = 0\text{ to }760\text{ V}$ , $V_{GS} = 0\text{ V}$                                         | -    | 45   | -    | pF       |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance, energy-related |                                                                                                     | -    | 19   | -    | pF       |
| $R_g$             | Intrinsic gate resistance              | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                             | -    | 7    | -    | $\Omega$ |
| $Q_g$             | Total gate charge                      | $V_{DD} = 760\text{ V}$ , $I_D = 6\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 2) | -    | 13   | -    | nC       |
| $Q_{gs}$          | Gate-source charge                     |                                                                                                     | -    | 3    | -    | nC       |
| $Q_{gd}$          | Gate-drain charge                      |                                                                                                     | -    | 7    | -    | nC       |

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                                                     | Min. | Typ. | Max. | Unit |
|--------------|---------------------|-------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 475\text{ V}$ , $I_D = 3\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see Figure 1 and Figure 6) | -    | 12   | -    | ns   |
| $t_r$        | Rise time           |                                                                                                                                     | -    | 12   | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time |                                                                                                                                     | -    | 33   | -    | ns   |
| $t_f$        | Fall time           |                                                                                                                                     | -    | 21   | -    | ns   |

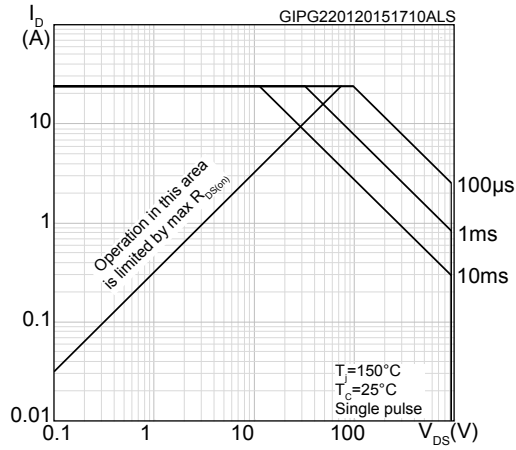
**Table 7. Source-drain diode**

| Symbol          | Parameter                     | Test conditions                                                                                                                              | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                              | -    |      | 6    | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                              | -    |      | 24   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $V_{GS} = 0\text{ V}$ , $I_{SD} = 6\text{ A}$                                                                                                | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$<br>(see Figure 3)                                        | -    | 372  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                              | -    | 4    |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                              | -    | 22   |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ ,<br>$T_J = 150\text{ }^\circ\text{C}$<br>(see Figure 3) | -    | 522  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                              | -    | 5    |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                              | -    | 20   |      | A             |

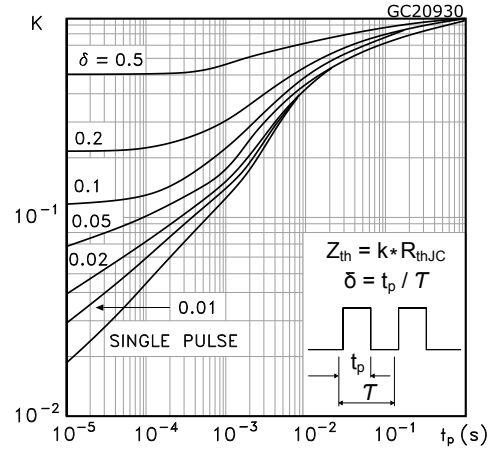
1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

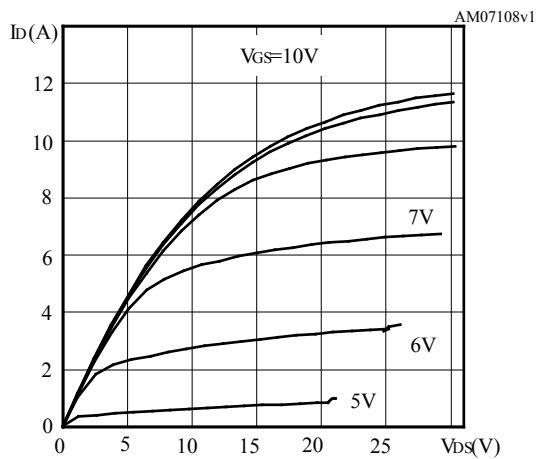
**Figure 1. Safe operating area**



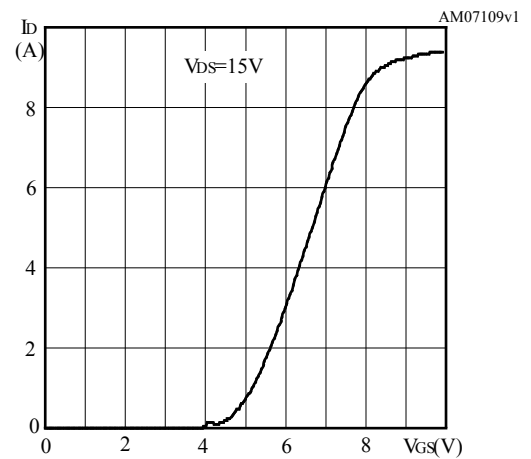
**Figure 2. Normalized transient thermal impedance**



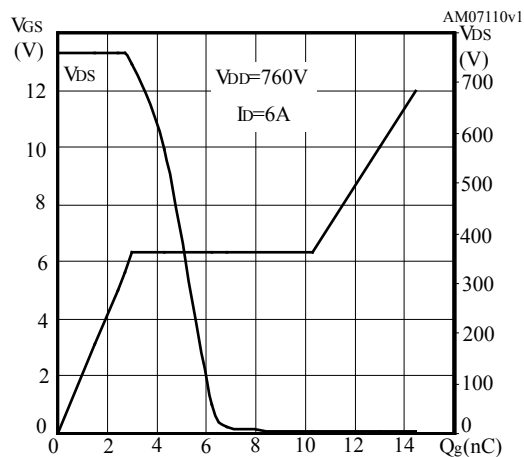
**Figure 3. Typical output characteristics**



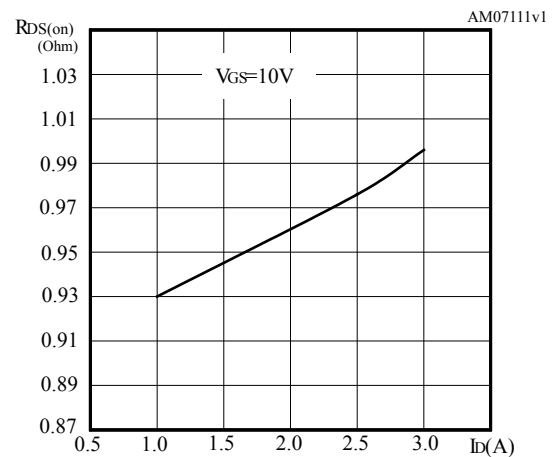
**Figure 4. Typical transfer characteristics**



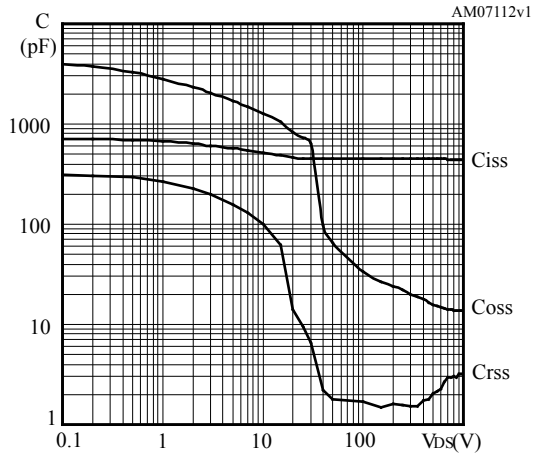
**Figure 5. Typical gate charge characteristics**



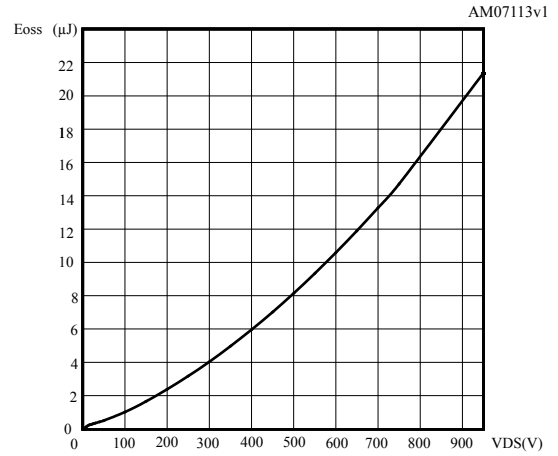
**Figure 6. Typical drain-source on-resistance**



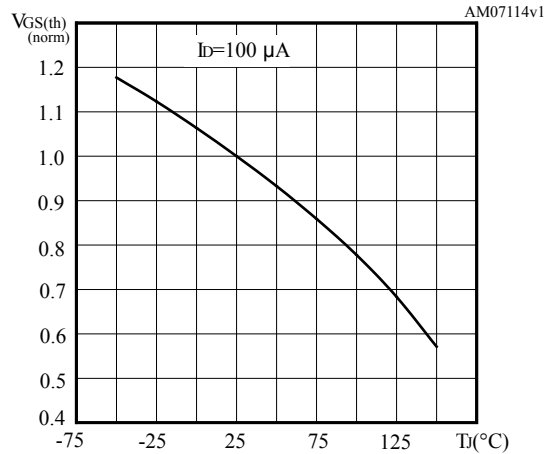
**Figure 7. Typical capacitance characteristics**



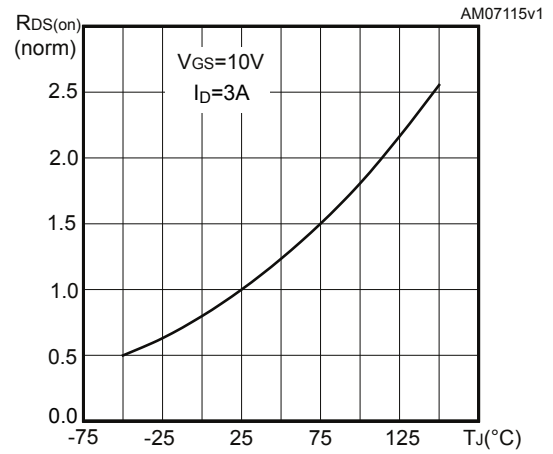
**Figure 8. Typical output capacitance stored energy**



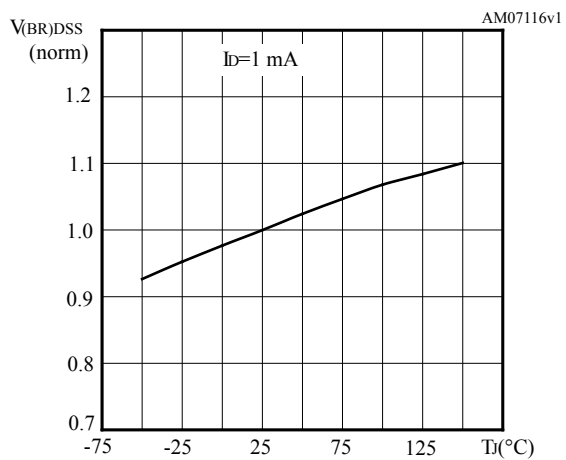
**Figure 9. Normalized gate threshold vs temperature**



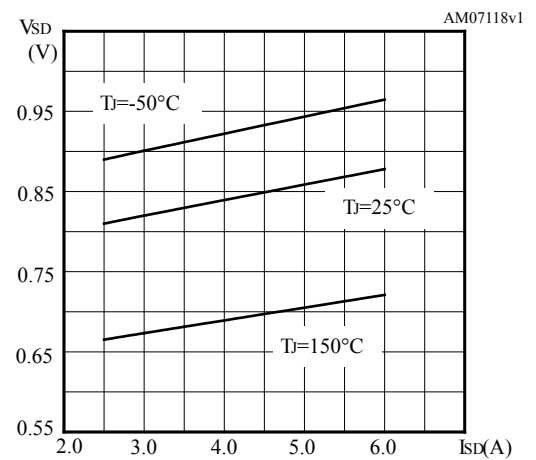
**Figure 10. Normalized on-resistance vs temperature**



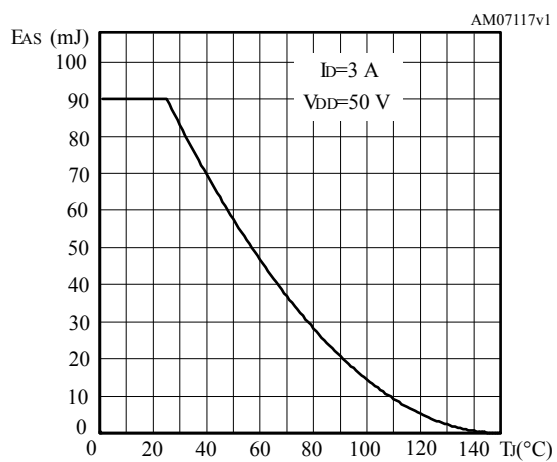
**Figure 11. Normalized breakdown voltage vs temperature**



**Figure 12. Typical reverse diode forward characteristics**



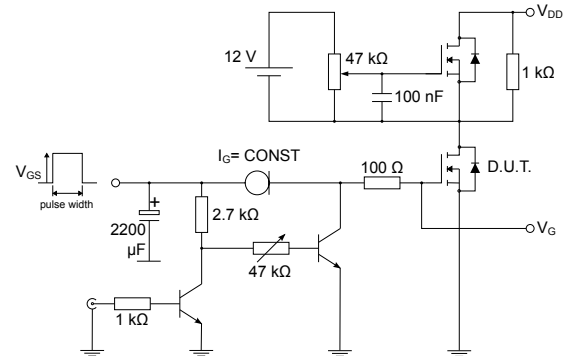
**Figure 13. Maximum avalanche energy vs temperature**



### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


AM01468v1

**Figure 15. Test circuit for gate charge behavior**


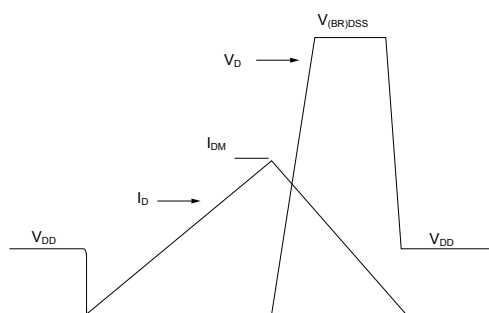
AM01469v1

**Figure 16. Test circuit for inductive load switching and diode recovery times**

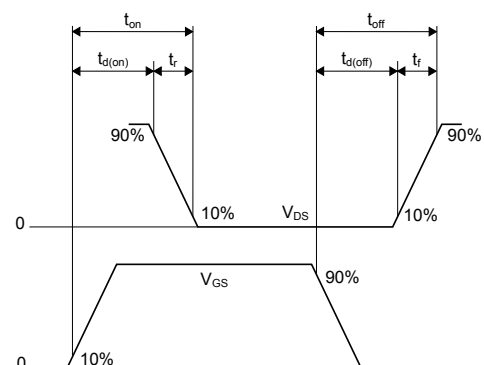

AM01470v1

**Figure 17. Unclamped inductive load test circuit**


AM01471v1

**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


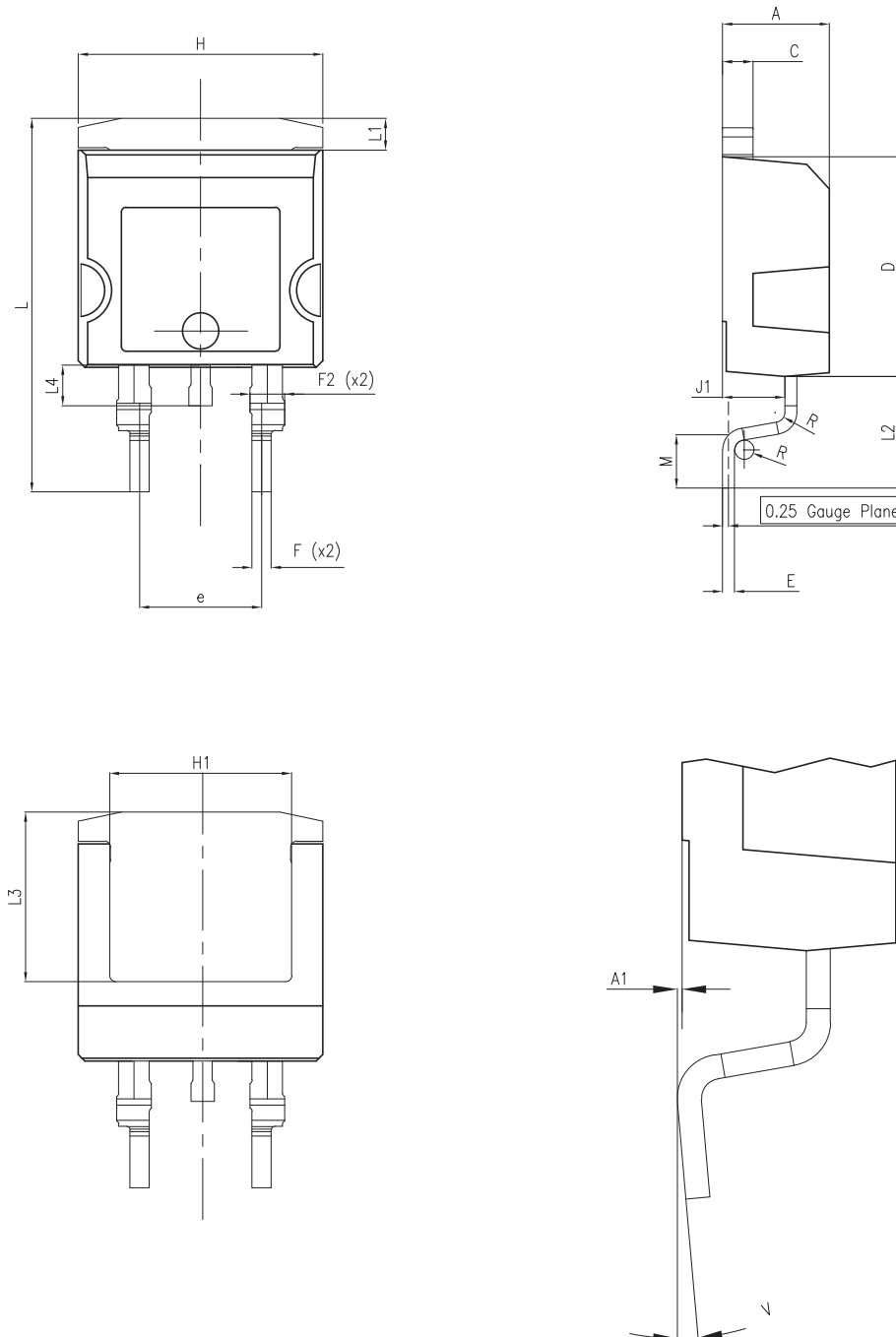
AM01473v1

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 H<sup>2</sup>PAK-2 package information

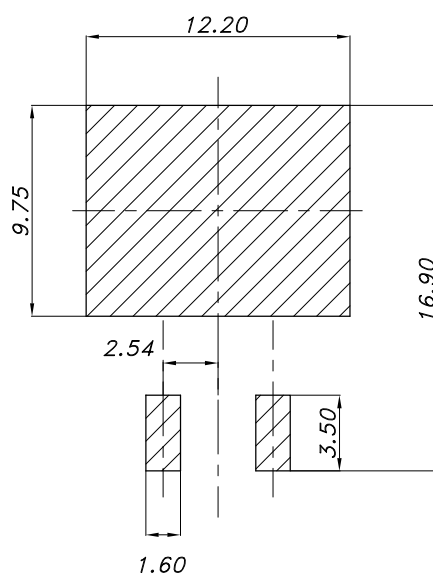
**Figure 20. H<sup>2</sup>PAK-2 package outline**



8159712\_10

**Table 8. H<sup>2</sup>PAK-2 package mechanical data**

| Dim. | mm    |      |       |
|------|-------|------|-------|
|      | Min.  | Typ. | Max.  |
| A    | 4.30  | -    | 4.70  |
| A1   | 0.03  |      | 0.20  |
| C    | 1.17  |      | 1.37  |
| D    | 8.95  |      | 9.35  |
| e    | 4.98  |      | 5.18  |
| E    | 0.50  |      | 0.90  |
| F    | 0.78  |      | 0.85  |
| F2   | 1.14  |      | 1.70  |
| H    | 10.00 |      | 10.40 |
| H1   | 7.40  |      | 7.80  |
| J1   | 2.49  |      | 2.69  |
| L    | 15.30 |      | 15.80 |
| L1   | 1.27  |      | 1.40  |
| L2   | 4.93  |      | 5.23  |
| L3   | 6.85  |      | 7.25  |
| L4   | 1.50  |      | 1.70  |
| M    | 2.60  |      | 2.90  |
| R    | 0.20  |      | 0.60  |
| V    | 0°    |      | 8°    |

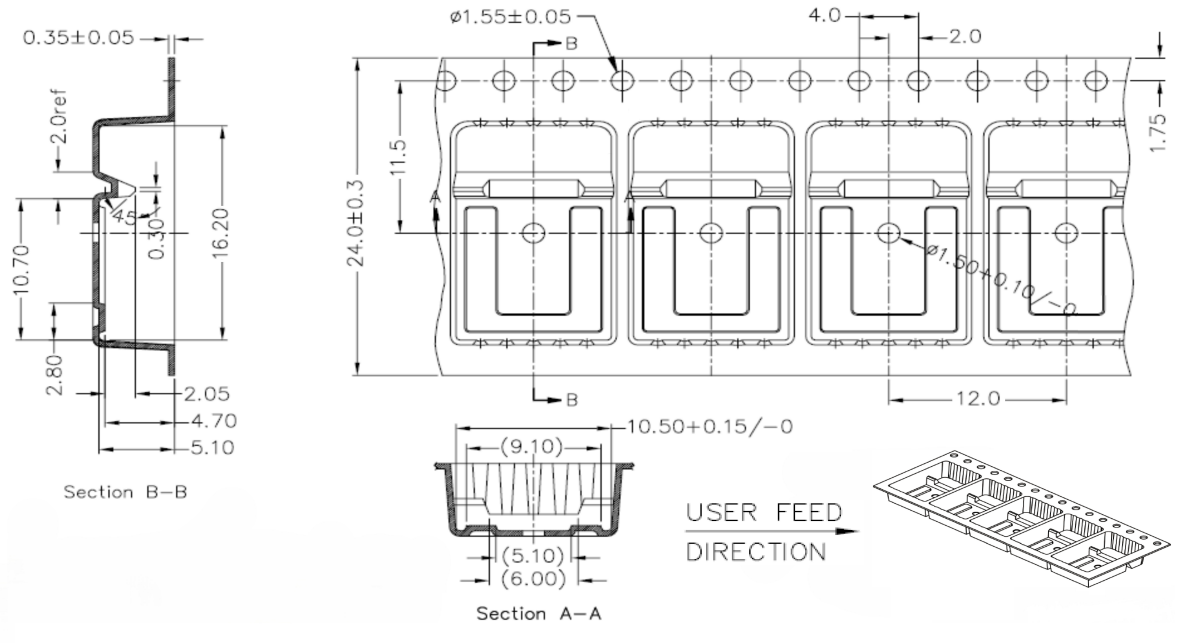
**Figure 21. H<sup>2</sup>PAK-2 recommended footprint**


8159712\_10

**Note:** Dimensions are in mm.

## 4.2 H<sup>2</sup>PAK-2 packing information

Figure 22. H<sup>2</sup>PAK-2 tape drawing (dimensions are in mm)



DM01095771\_2

## Revision history

**Table 9. Document revision history**

| Date        | Revision | Changes                                                                                           |
|-------------|----------|---------------------------------------------------------------------------------------------------|
| 23-Jan-2015 | 1        | First release.                                                                                    |
| 04-Feb-2015 | 2        | Updated <i>Section 2: "Electrical characteristics"</i>                                            |
| 12-Mar-2015 | 3        | Document status changed from preliminary to production data.                                      |
| 07-Nov-2025 | 4        | Updated <a href="#">Section 4.2: H<sup>2</sup>PAK-2 packing information</a> . Minor text changes. |

## Contents

|          |                                                |           |
|----------|------------------------------------------------|-----------|
| <b>1</b> | <b>Electrical ratings .....</b>                | <b>2</b>  |
| <b>2</b> | <b>Electrical characteristics.....</b>         | <b>3</b>  |
| 2.1      | Electrical characteristics (curves) .....      | 5         |
| <b>3</b> | <b>Test circuits .....</b>                     | <b>8</b>  |
| <b>4</b> | <b>Package information.....</b>                | <b>9</b>  |
| 4.1      | H <sup>2</sup> PAK-2 package information ..... | 9         |
| 4.2      | H <sup>2</sup> PAK-2 packing information.....  | 11        |
|          | <b>Revision history .....</b>                  | <b>12</b> |

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