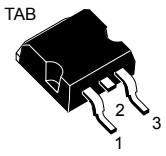
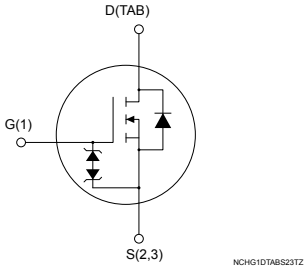
STH13N120K5-2AG

Datasheet

Automotive-grade N-channel 1200 V, 0.62 Ω typ., 12 A, MDmesh K5 Power MOSFET in an H²PAK-2 package



H²PAK-2



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STH13N120K5-2AG	1200 V	0.69 Ω	12 A	250 W

- AEC-Q101 qualified
- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status link
STH13N120K5-2AG

Product summary[1]	
Order code	STH13N120K5-2AG
Marking	13N120K5
Package	H²PAK-2
Packing	Tape and reel

1. *HTRB test was performed at 80% of $V_{(BR)DSS}$ according to AEC-Q101 rev. C. All other tests were performed according to AEC-Q101 rev. D.*

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	12	A
	Drain current (continuous) at T_C = 100 °C	7.6	A
I_{DM} (1)	Drain current (pulsed)	48	A
P_{TOT}	Total power dissipation at T_C = 25 °C	250	W
I_{AR} (2)	Maximum current during repetitive or single-pulse avalanche	4	A
E_{AS} (3)	Single-pulse avalanche energy	215	mJ
dv/dt (4)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt(5)	MOSFET dv/dt ruggedness	50	V/ns
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *Pulse width limited by T_J max.*
3. *Starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.*
4. *I_{SD} ≤ 12 A, di/dt ≤ 100 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$.*
5. *V_{DS} ≤ 960 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.5	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	30	°C/W

1. *When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1200			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1200 V			1	µA
		V_{GS} = 0 V, V_{DS} = 1200 V, T_C = 125 °C(1)			50	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		0.62	0.69	Ω

1. *Specified by design, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	1370	-	pF
C_{oss}	Output capacitance		-	110	-	pF
C_{rss}	Reverse transfer capacitance		-	0.6	-	pF
$C_{o(tr)}$(1)	Time-related equivalent capacitance	V_{GS} = 0 V, V_{DS} = 0 to 960 V	-	128	-	pF
$C_{o(er)}$(2)	Energy-related equivalent capacitance		-	42	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	3	-	Ω
Q_g	Total gate charge	V_{DD} = 960 V, I_D = 12 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	44.2	-	nC
Q_{gs}	Gate-source charge		-	7.3	-	nC
Q_{gd}	Gate-drain charge		-	30	-	nC

1. *Time-related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *Energy-related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 600 V, I_D = 6 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	23	-	ns
t_r	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off delay time		-	68.5	-	ns
t_f	Fall time		-	18.5	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM}	Source-drain current (pulsed)		-		48	A
V_{SD} (1)	Forward on voltage	I_{SD} = 12 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,	-	630		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	12.6		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	40		A
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,	-	892		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_J = 150 °C	-	15.6		µC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	35		A

1. *Pulsed: pulse duration = 300µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

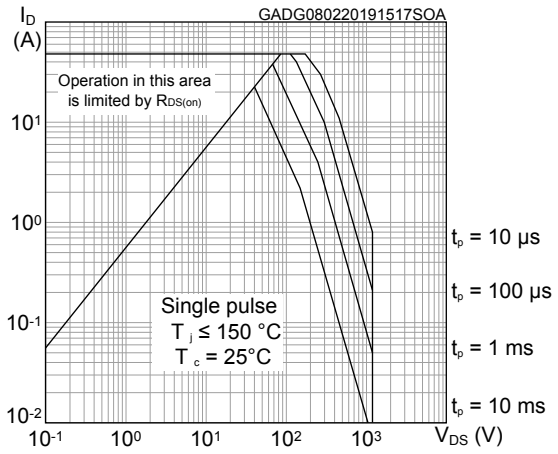


Figure 2. Normalized transient thermal impedance

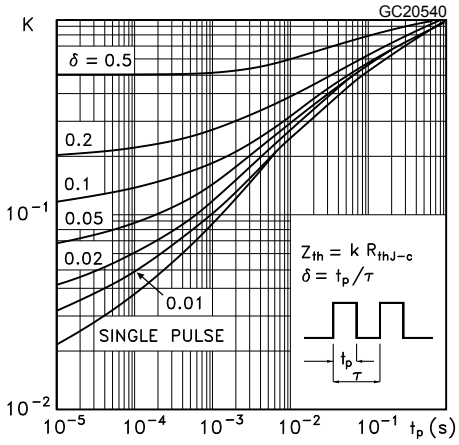


Figure 3. Typical output characteristics

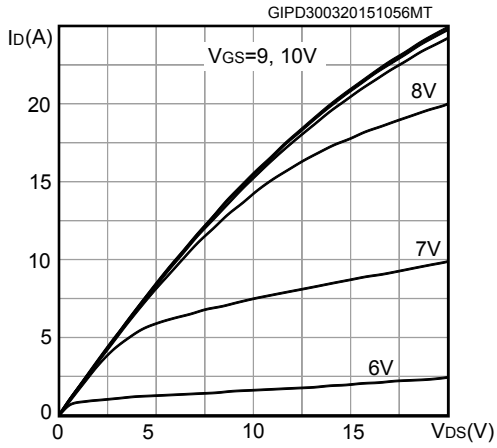


Figure 4. Typical transfer characteristics

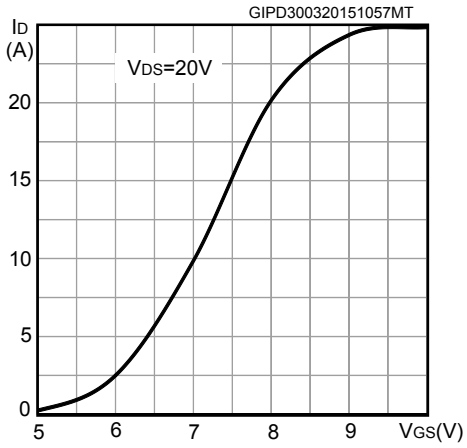


Figure 5. Typical gate charge characteristics

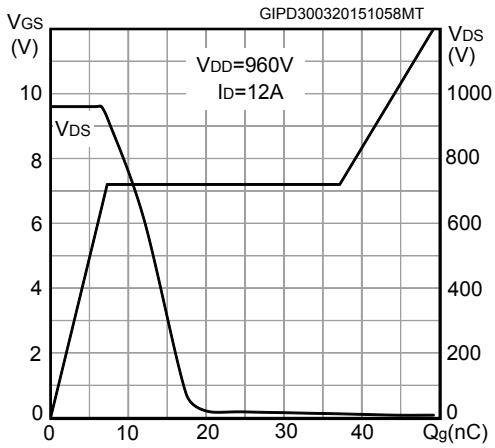


Figure 6. Typical drain-source on-resistance

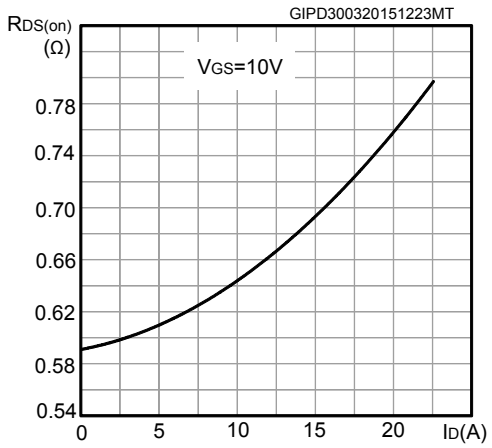


Figure 7. Typical capacitance characteristics

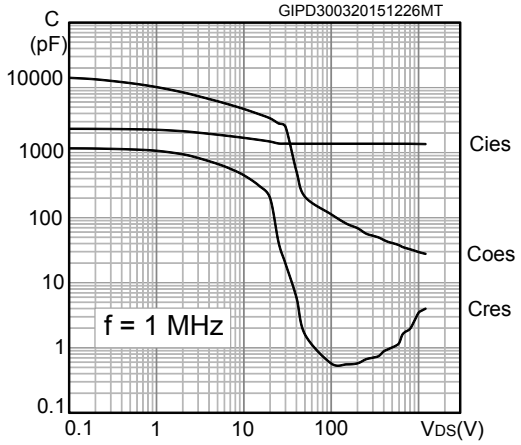


Figure 8. Typical output capacitance stored energy

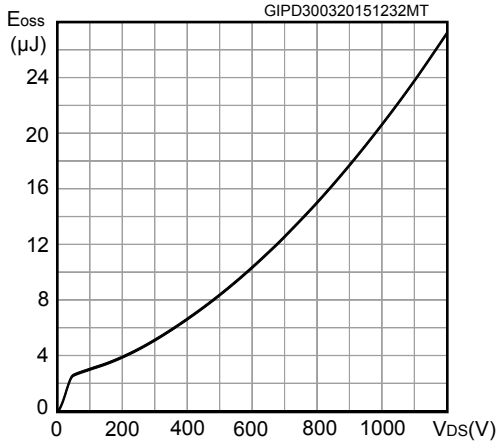


Figure 9. Normalized gate threshold vs temperature

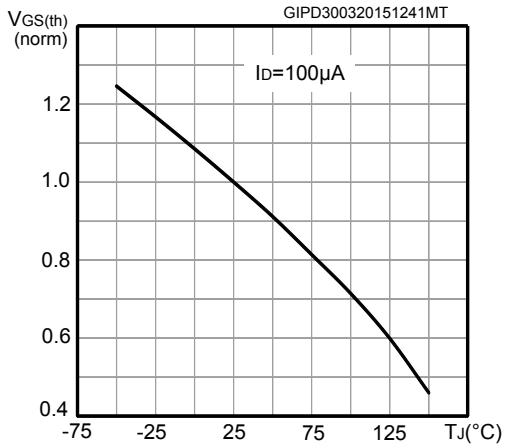


Figure 10. Normalized on-resistance vs temperature

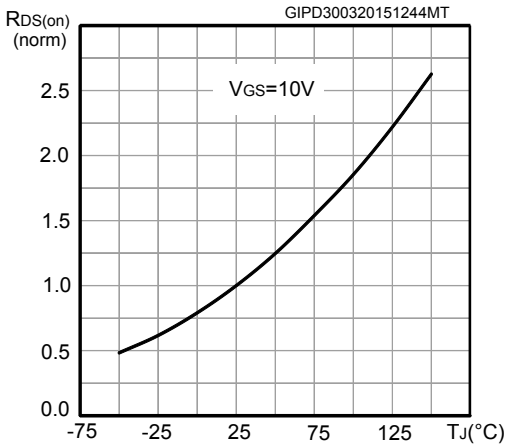


Figure 11. Normalized breakdown voltage vs temperature

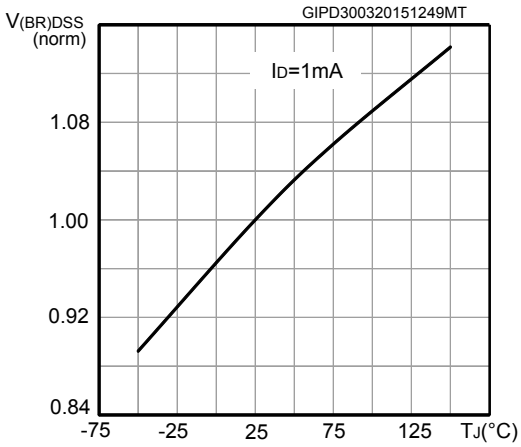


Figure 12. Typical reverse diode forward characteristics

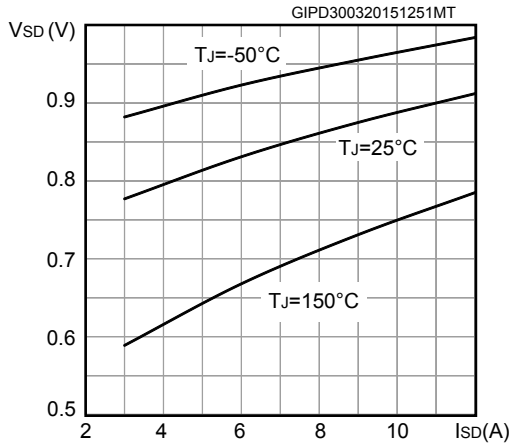
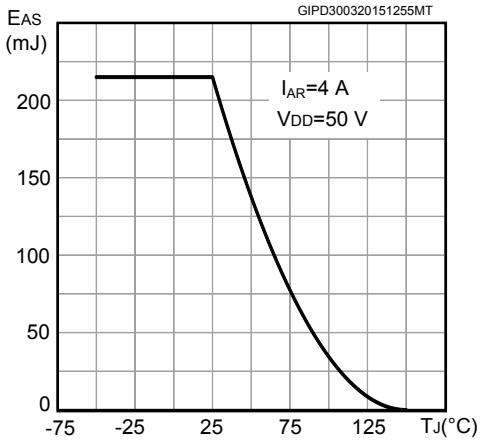


Figure 13. **Maximum avalanche energy vs temperature**



3 Test circuits

Figure 14. Test circuit for resistive load switching times

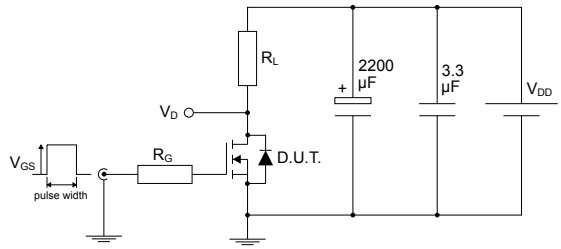


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Figure 15. Test circuit for gate charge behavior

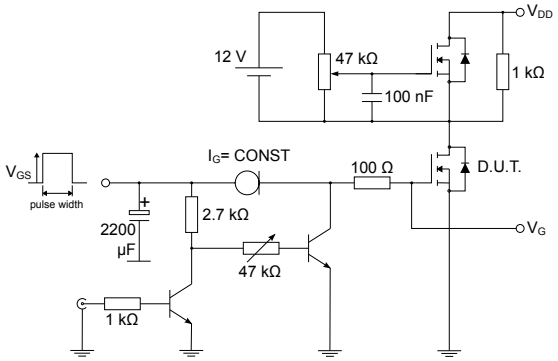

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Figure 16. Test circuit for inductive load switching and diode recovery times

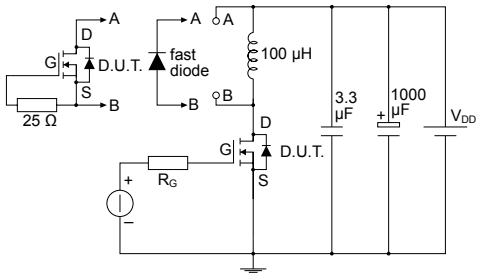

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Figure 17. Unclamped inductive load test circuit

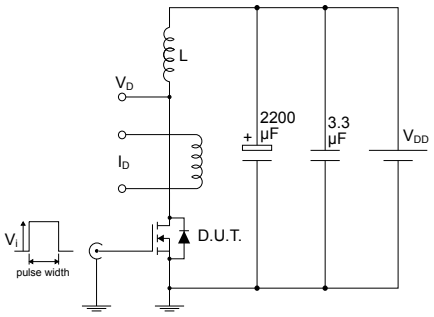

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Figure 18. Unclamped inductive waveform

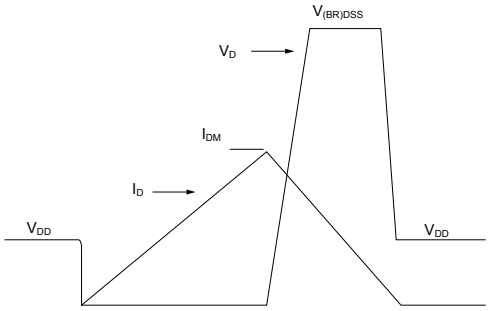

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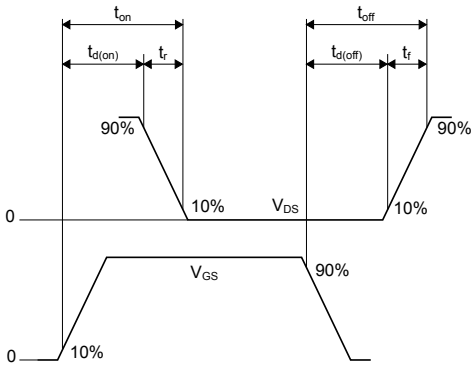
Figure 19. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-2 package information

Figure 20. H²PAK-2 package outline

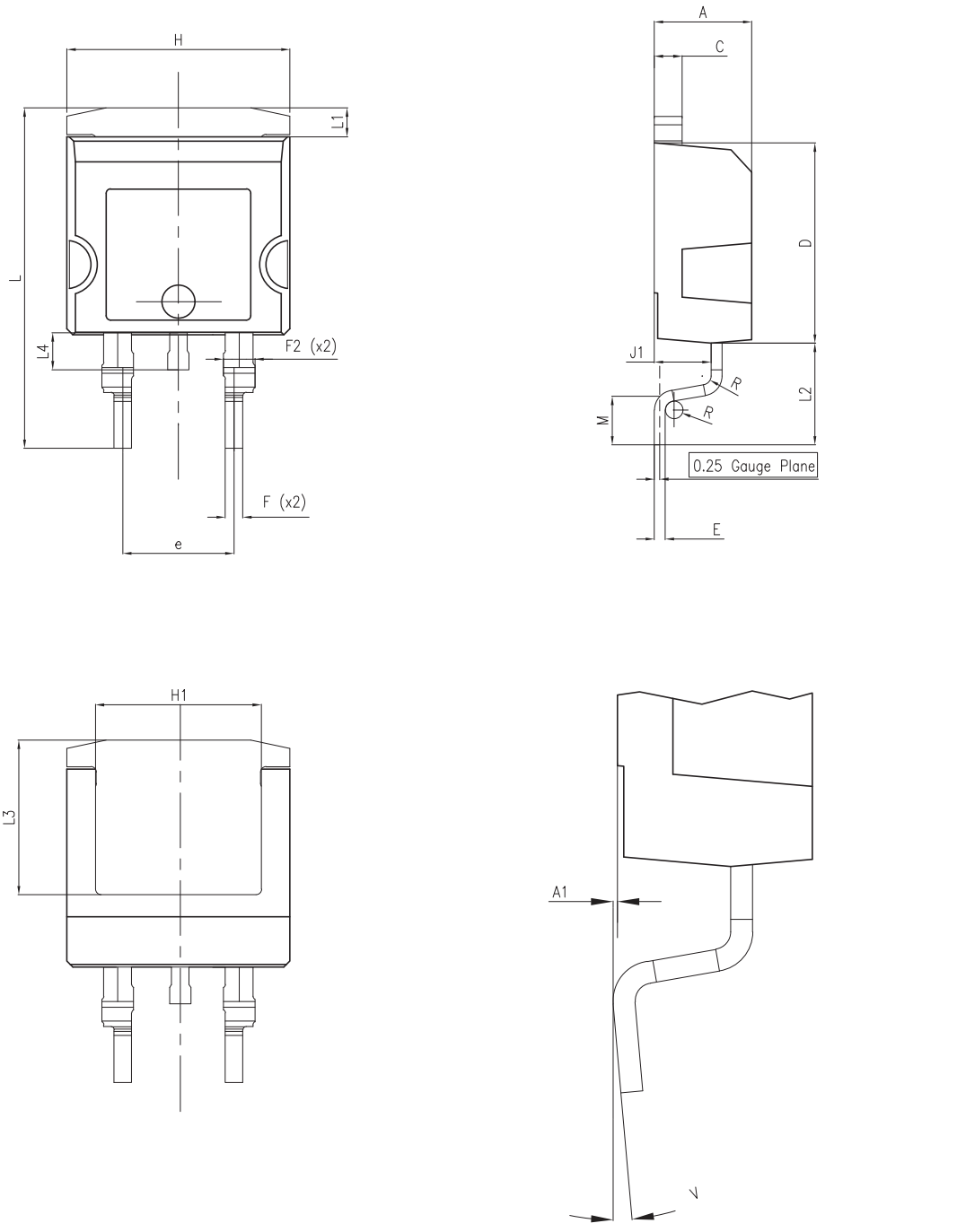
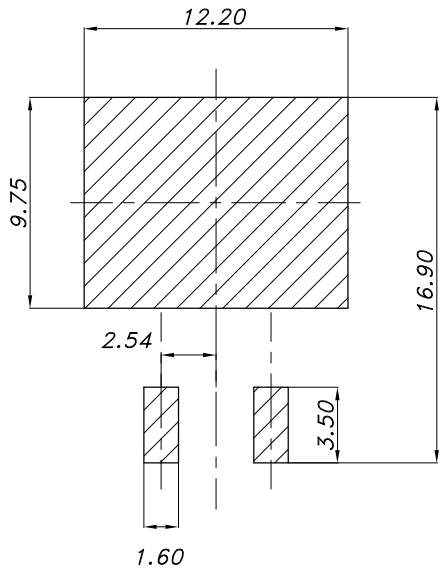


Table 7. H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30		4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40	-	7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

Figure 21. H²PAK-2 recommended footprint



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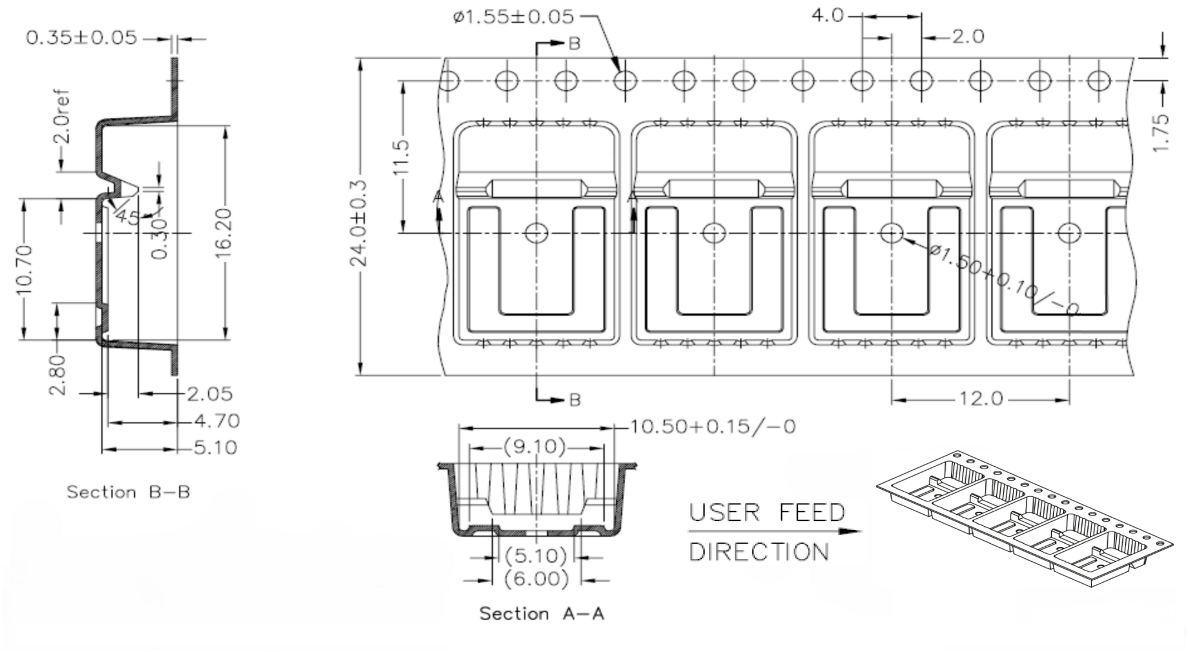
Note: Dimensions are in mm.

4.2 H²PAK-2 packing information

Figure 22. **H²PAK-2 tape drawing (dimensions are in mm)**



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Revision history

Table 8. **Document revision history**

Date	Version	Changes
14-Feb-2019	1	First release.
10-Sep-2019	2	Updated *title* and *features* in cover page. Updated *Section 1 Electrical ratings, Section 2 Electrical characteristics* and *Section 2.1 Electrical characteristics (curves)*. Minor text changes.
23-Oct-2019	3	Modified *Table 1. Absolute maximum ratings, Table 2. Thermal data, Table 3. On/off states, Table 4. Dynamic, Table 5. Switching times and Table 6. Source-drain diode.* Modified *Section 2.1 Electrical characteristics (curves)*.
11-Mar-2020	4	Updated device summary in cover page.
16-Jun-2020	5	Updated *Section 4 Package information*.
22-Aug-2025	6	Updated Section 4: Package information. Minor text changes.

Contents

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