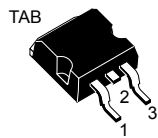
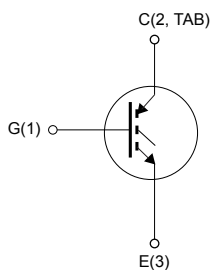


Trench gate field-stop, 650 V, 50 A, high-speed HB2 series IGBT in a D²PAK package


D²PAK


G1C2TE3



Features

- Maximum junction temperature: $T_J = 175\text{ }^{\circ}\text{C}$
- Low $V_{CE(sat)} = 1.55\text{ V (typ.) @ } I_C = 50\text{ A}$
- Minimized tail current
- Tight parameter distribution
- Low thermal resistance
- Positive $V_{CE(sat)}$ temperature coefficient

Applications

- Welding
- PFC converters - single phase input
- Solar inverters (string and central)
- Uninterruptable power supplies (UPS)
- EV charging - DC fast charging stations

Description

The newest IGBT 650 V HB2 series represents an evolution of the advanced proprietary trench gate field-stop structure. The performance of the HB2 series is optimized in terms of conduction, thanks to a better $V_{CE(sat)}$ behavior at low current values, as well as in terms of reduced switching energy. The result is a product specifically designed to maximize efficiency for a wide range of fast applications.

Product status link

[STGB50H65FB2](#)

Product summary

Order code	STGB50H65FB2
Marking	G50H65FB2
Package	D ² PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GE} = 0$ V)	650	V
I_C	Continuous collector current at $T_C = 25$ °C	86	A
	Continuous collector current at $T_C = 100$ °C	53	
I_{CP} ⁽¹⁾⁽²⁾	Pulsed collector current	150	
V_{GE}	Gate-emitter voltage	±20	V
	Transient gate-emitter voltage ($t_p \leq 10$ µs)	±30	
P_{TOT}	Total power dissipation at $T_C = 25$ °C	272	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	-55 to 175	

1. Defined by design, not subject to production test.
2. Pulse width is limited by maximum junction temperature.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case	0.55	°C/W
R_{thJA}	Thermal resistance junction-ambient	50	

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 3. Static characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	$V_{GE} = 0\text{ V}$, $I_C = 1\text{ mA}$	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}$, $I_C = 50\text{ A}$		1.55	2	V
		$V_{GE} = 15\text{ V}$, $I_C = 50\text{ A}$, $T_J = 125\text{ °C}$		1.8		
		$V_{GE} = 15\text{ V}$, $I_C = 50\text{ A}$, $T_J = 175\text{ °C}$		1.9		
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 1\text{ mA}$	5	6	7	V
I_{CES}	Collector cut-off current	$V_{GE} = 0\text{ V}$, $V_{CE} = 650\text{ V}$			25	μA
I_{GES}	Gate-emitter leakage current	$V_{CE} = 0\text{ V}$, $V_{GE} = \pm 20\text{ V}$			± 250	nA

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GE} = 0\text{ V}$	-	2928	-	pF
C_{oes}	Output capacitance		-	162	-	
C_{res}	Reverse transfer capacitance		-	78	-	
Q_g	Total gate charge	$V_{CC} = 520\text{ V}$, $I_C = 50\text{ A}$, $V_{GE} = 0\text{ to }15\text{ V}$ (see Figure 22. Gate charge test circuit)	-	151	-	nC
Q_{ge}	Gate-emitter charge		-	30	-	
Q_{gc}	Gate-collector charge		-	63	-	

Table 5. Switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 400\text{ V}$, $I_C = 50\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 4.7\text{ }\Omega$ (see Figure 21. Test circuit for inductive load switching)	-	28	-	ns
t_r	Current rise time		-	20	-	ns
$E_{on(1)}$	Turn-on switching energy		-	910	-	μJ
$t_{d(off)}$	Turn-off delay time		-	115	-	ns
t_f	Current fall time		-	40	-	ns
$E_{off(2)}$	Turn-off switching energy		-	580	-	μJ
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 400\text{ V}$, $I_C = 50\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 4.7\text{ }\Omega$, $T_J = 175\text{ °C}$ (see Figure 21. Test circuit for inductive load switching)	-	24	-	ns
t_r	Current rise time		-	17	-	ns
$E_{on(1)}$	Turn-on switching energy		-	1800	-	μJ
$t_{d(off)}$	Turn-off delay time		-	135	-	ns
t_f	Current fall time		-	90	-	ns
$E_{off(2)}$	Turn-off switching energy		-	1090	-	μJ

1. Including the reverse recovery of the external diode. The diode is the same of the co-packed STGWA50H65DFB2.
2. Including the tail of the collector current.

2.1 Electrical characteristics (curves)

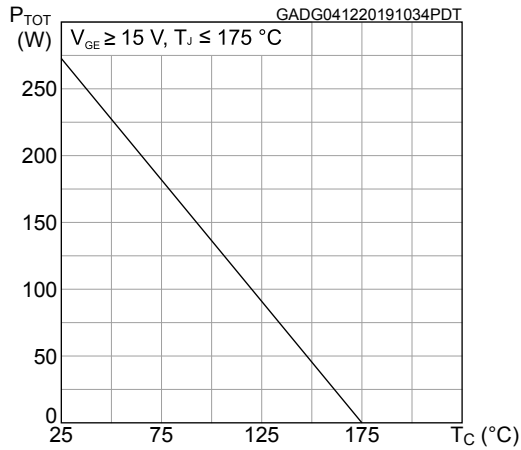
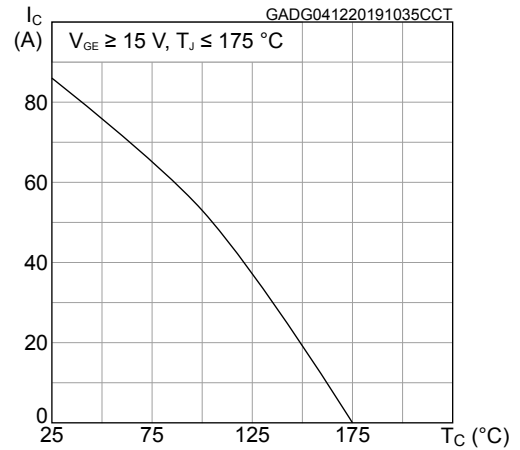
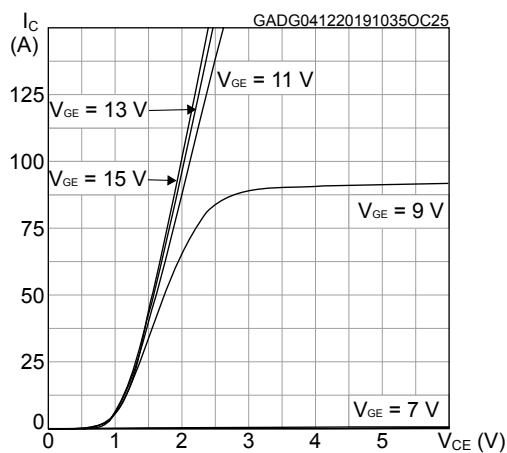
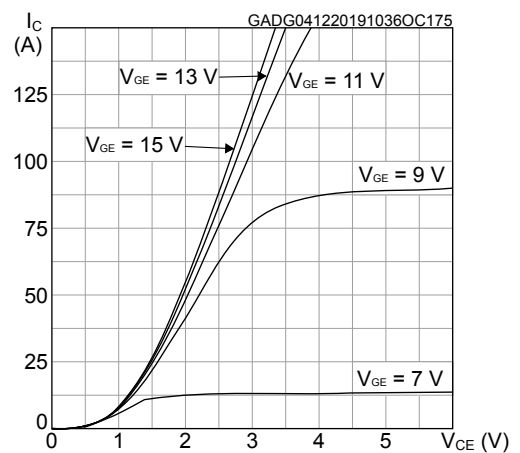
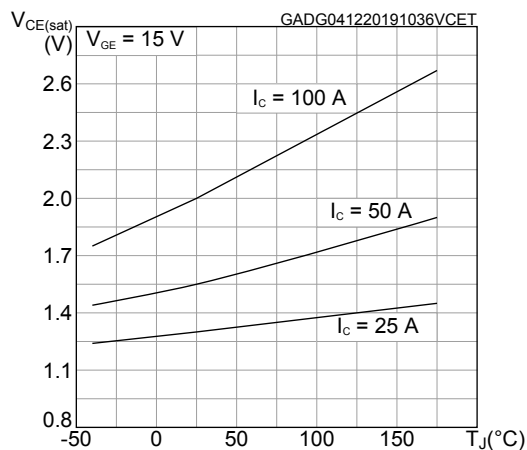
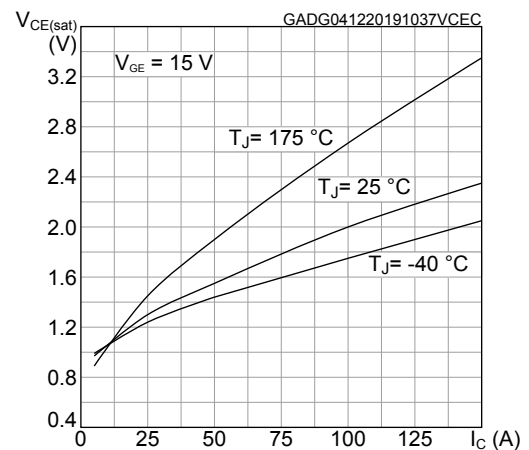
Figure 1. Power dissipation vs case temperature

Figure 2. Collector current vs case temperature

Figure 3. Output characteristics (T_J = 25 °C)

Figure 4. Output characteristics (T_J = 175 °C)

Figure 5. V_CE(sat) vs junction temperature

Figure 6. V_CE(sat) vs collector current


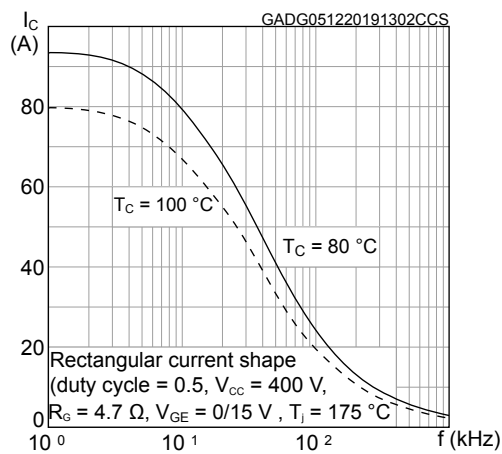
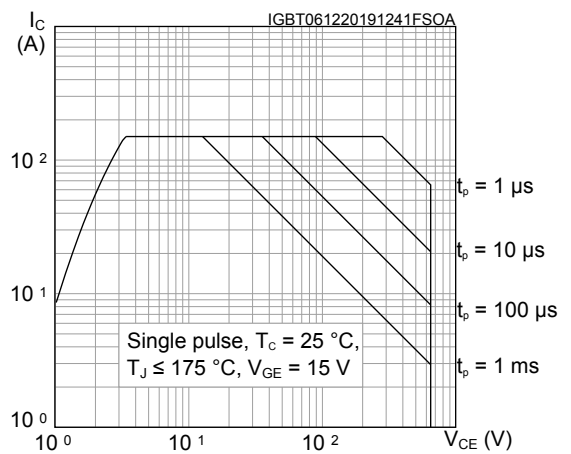
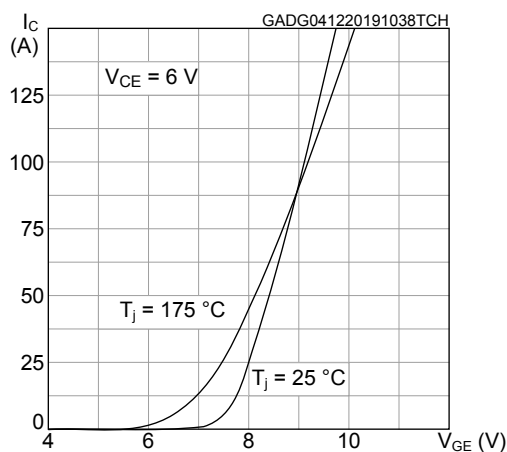
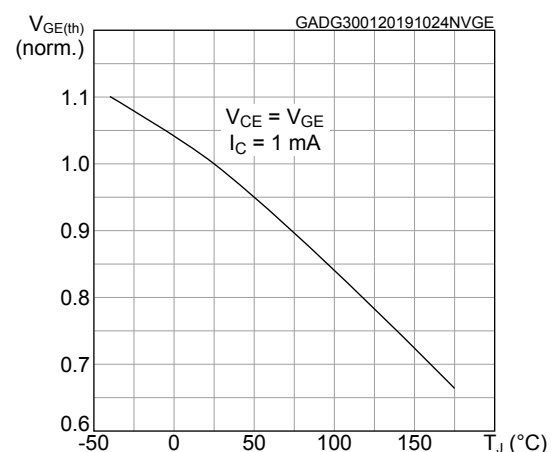
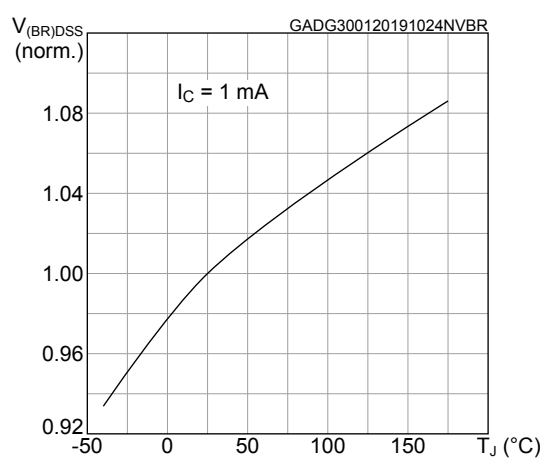
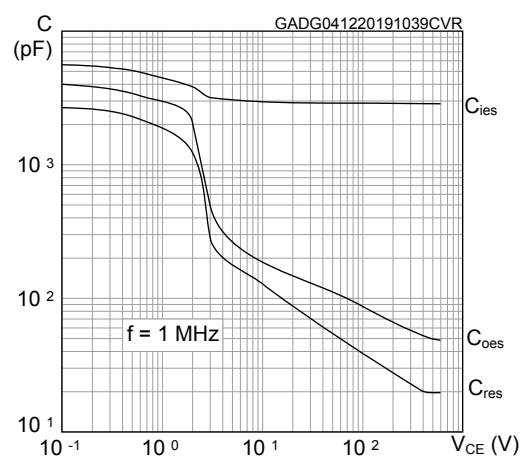
Figure 7. Collector current vs switching frequency

Figure 8. Forward bias safe operating area

Figure 9. Transfer characteristics

Figure 10. Normalized $V_{GE(th)}$ vs junction temperature

Figure 11. Normalized $V_{(BR)CES}$ vs junction temperature

Figure 12. Capacitance variations


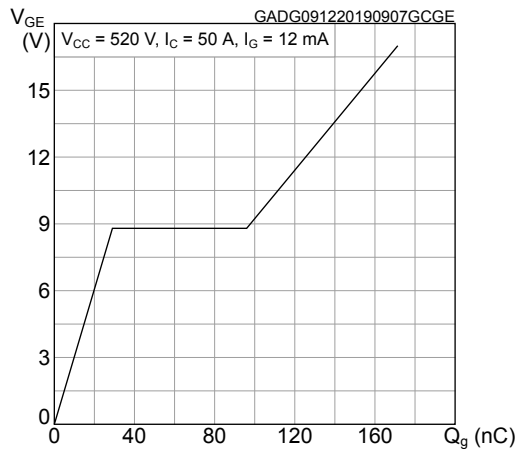
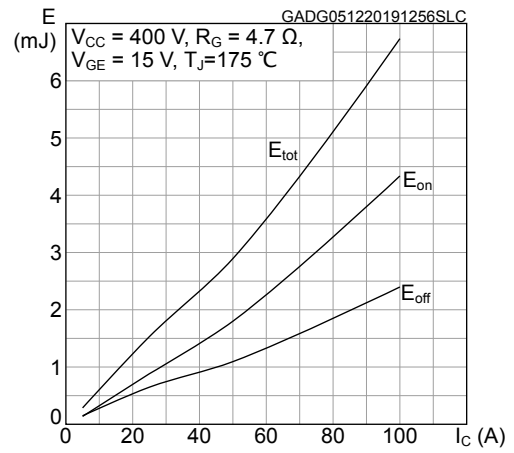
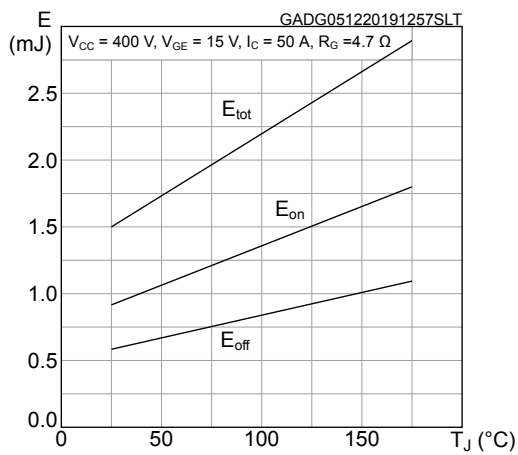
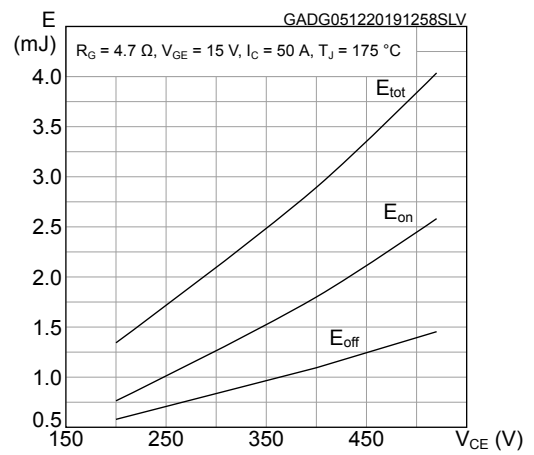
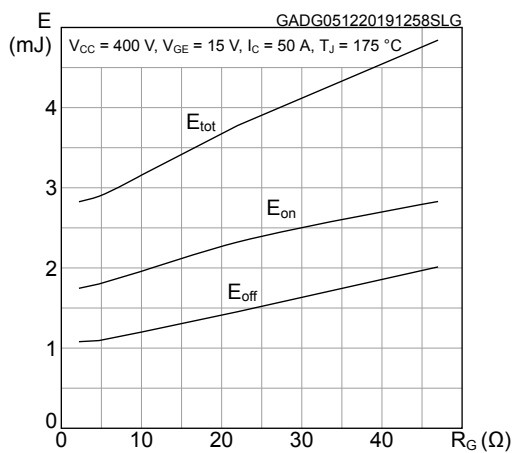
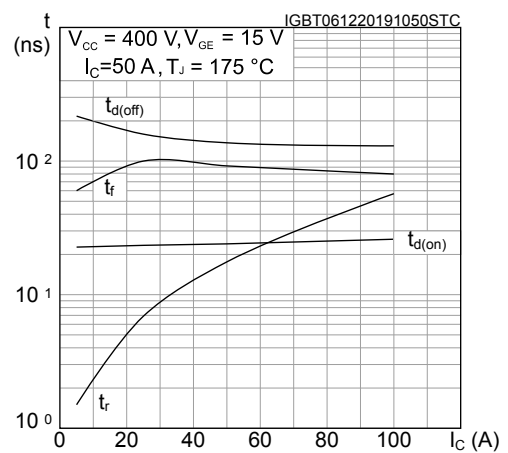
Figure 13. Gate charge vs gate-emitter voltage

Figure 14. Switching energy vs collector current

Figure 15. Switching energy vs temperature

Figure 16. Switching energy vs collector emitter voltage

Figure 17. Switching energy vs gate resistance

Figure 18. Switching times vs collector current


Figure 19. Switching times vs gate resistance

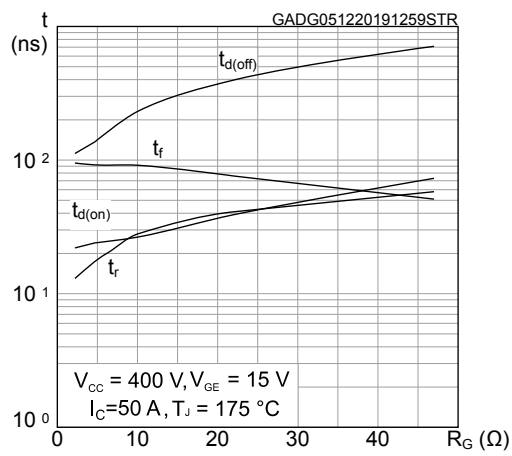
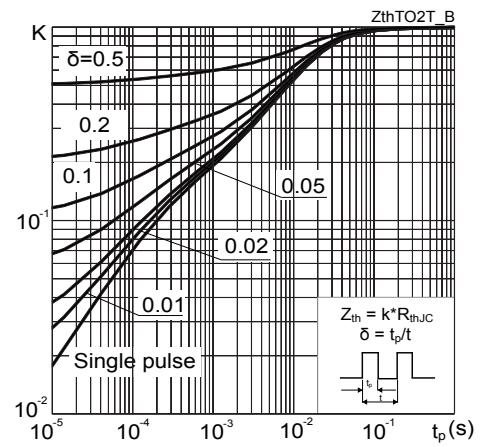
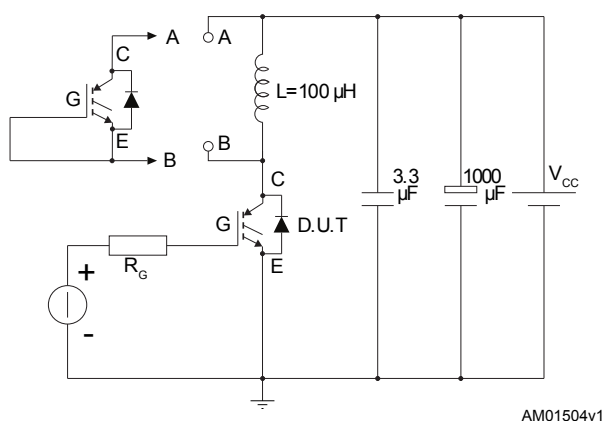
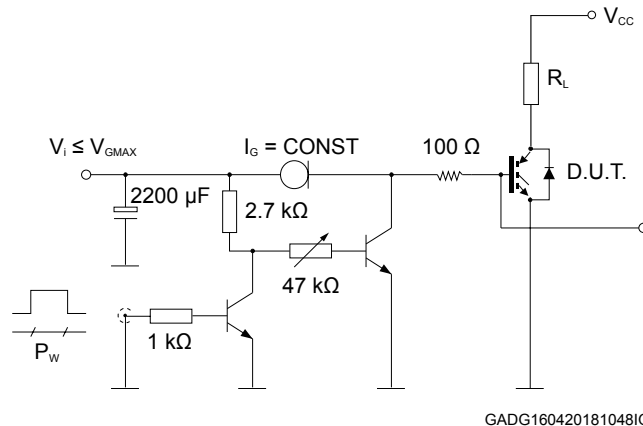
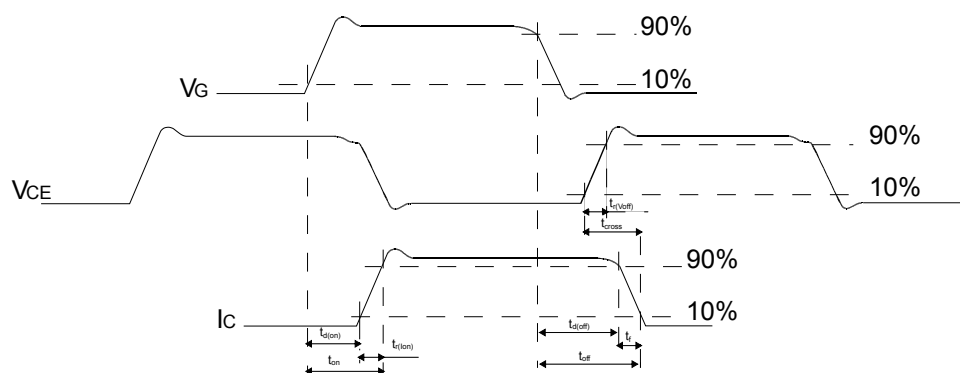


Figure 20. Thermal impedance



3 Test circuits

Figure 21. Test circuit for inductive load switching

Figure 22. Gate charge test circuit

Figure 23. Switching waveform


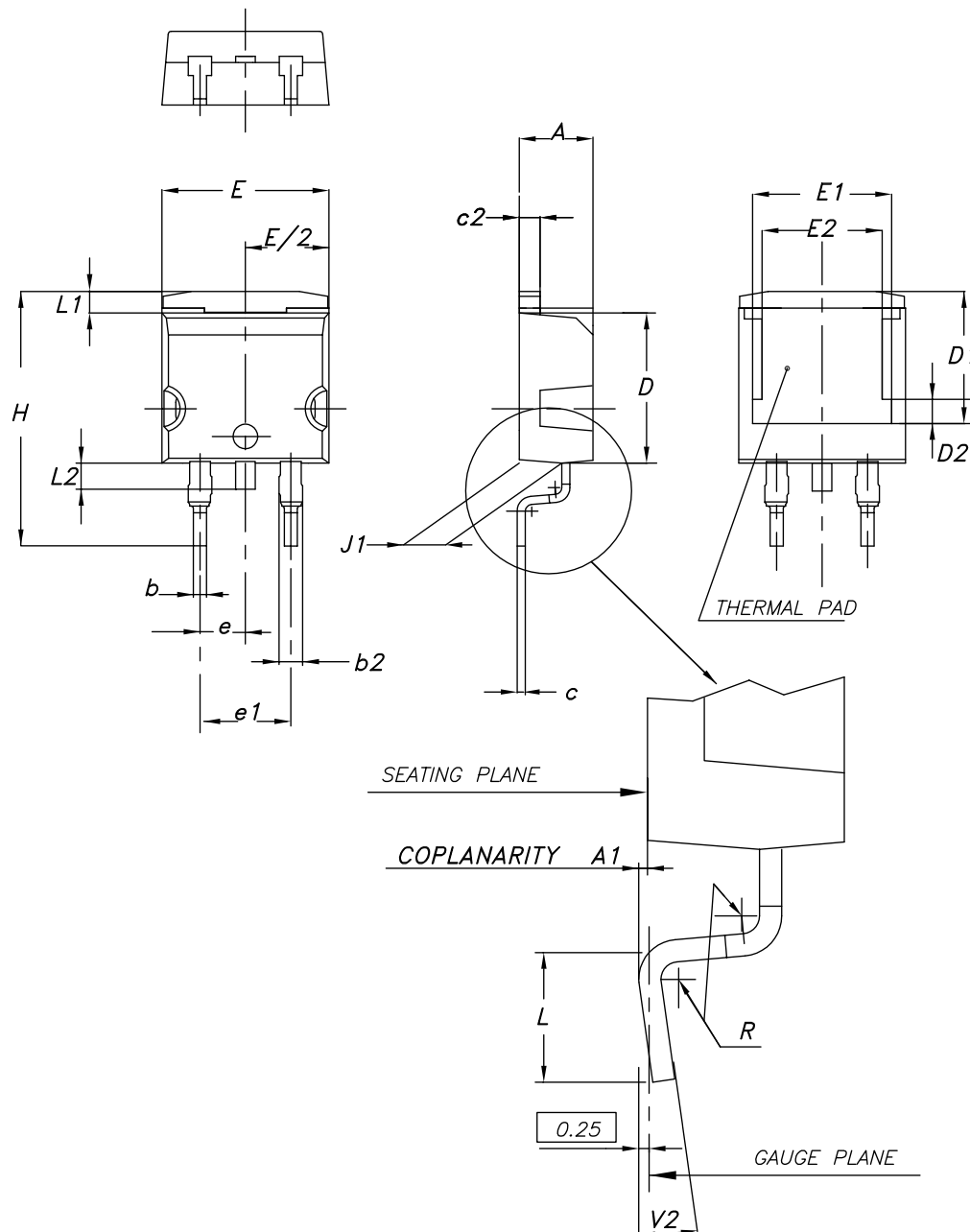
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 24. D²PAK (TO-263) type A2 package outline

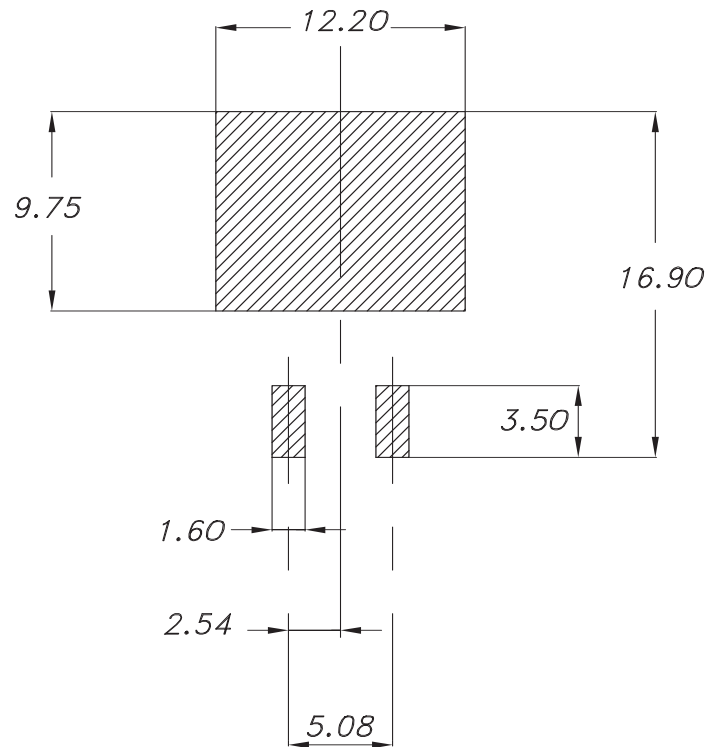


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Table 6. D²PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

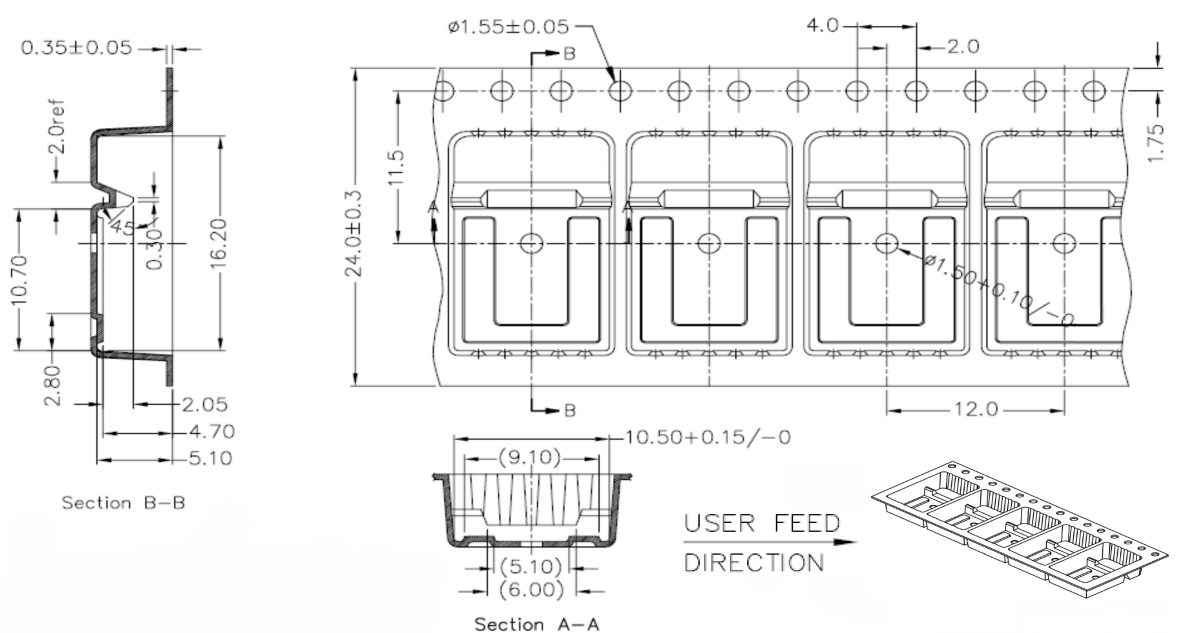
Figure 25. D²PAK (TO-263) recommended footprint (dimensions are in mm)



0079457_Rev27_footprint

4.2 D²PAK packing information

Figure 26. D²PAK tape drawing (dimensions are in mm)



DM01095771_1

Revision history

Table 7. Document revision history

Date	Revision	Changes
16-Jan-2020	1	First release.
21-May-2020	2	Updated <i>Section 4 Package information</i> .
05-May-2025	3	Updated Section 4: Package information .

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