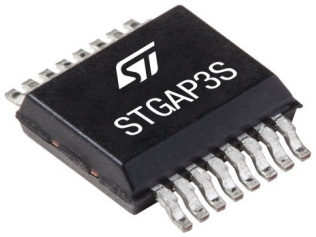
STGAP3S3IF, STGAP3S3S

Datasheet

Galvanically isolated 3 A single gate drivers with protection features



SO-16W

STGAP

Product status link
STGAP3S3IF
STGAP3S3S

Product label
SUSTAINABLE TECHNOLOGY

Features

- High voltage rail up to 1200 V
- Driver current capability: 3 A sink/source @25 °C
- ±200 V/ns Common Mode Transient Immunity (CMTI)
- 75 ns input-output propagation delay
- Internal Miller CLAMP, 3 A sink current
- Adjustable soft turn-off function option
- VDD UVLO
- VH UVLO: IGBT and SiC variants
- Desaturation protection: IGBT and SiC variants
- Gate driving voltage up to 32 V
- Negative gate driving voltage up to -10 V
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Temperature shutdown protection
- Reinforced galvanic isolation:
  - Isolation voltage V_{ISO} = 5.7 kV_{RMS} (UL 1577)
  - Transient Overvoltage V_{IOTM} = 8 kV_{PEAK} (IEC 60747-17)
  - Max. Repetitive Isolation Voltage V_{IORM} = 1.2 kV_{PEAK} (IEC 60747-17)
- Wide body SO-16W package

Applications

- Motor driver for home appliances, fans, pumps
- Industrial drives, factory automation
- 600/1200 V inverters
- Battery chargers
- Induction heating
- Welding
- UPS
- Power supply units, DC-DC converters
- Power factor correction

Description

The STGAP3S is a product family of protected single gate drivers within the STGAP platform, providing galvanic isolation between the gate driving section and the low-voltage control and interface circuits.

The product family includes different options with 3 A current capability, each of which is available with dedicated UVLO variants for SiC MOSFETs and IGBTs.

Ultrafast desaturation protection is also available with differentiated intervention thresholds and adjustable soft turn-off.

The availability of the Miller CLAMP and optional negative driving enables optimal driving performance.

1 Block diagram

Figure 1. **Block diagram - STGAP3S3IF**

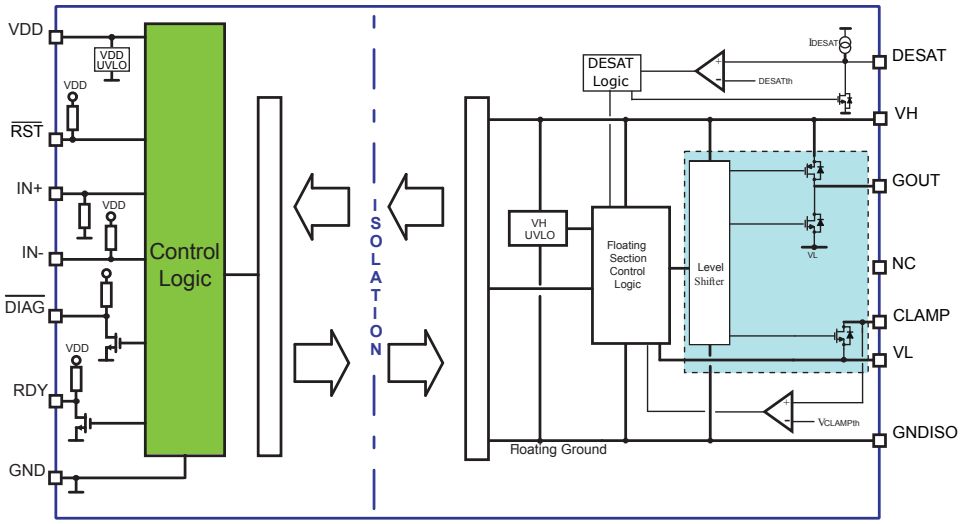
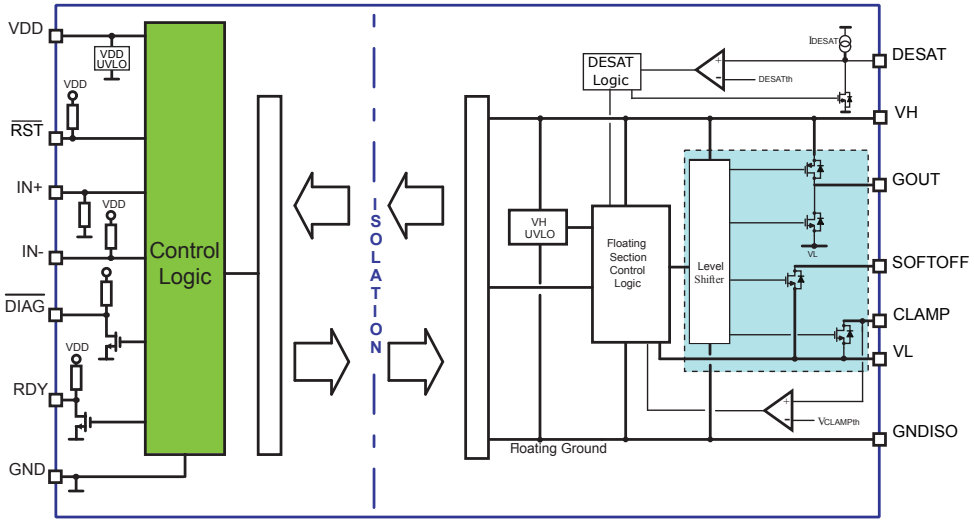


Figure 2. **Block diagram - STGAP3S3S**



2 Pin description and connection diagram

Figure 3. **Pin connection - STGAP3S3IF (top view)**

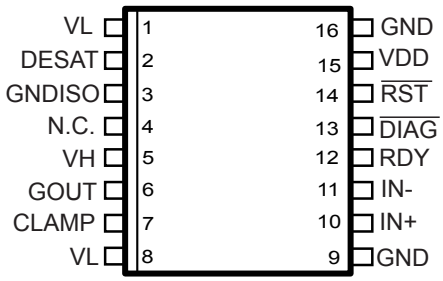


Figure 4. **Pin connection - STGAP3S3S (top view)**

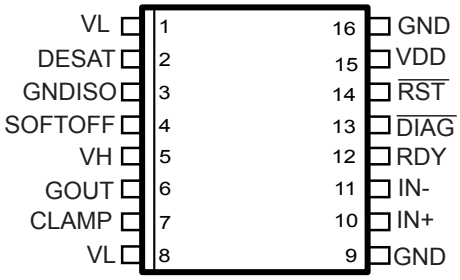


Table 1. **Pin description**

Pin STGAP3S3IF	Pin STGAP3S3S	Pin name	Type	Function
1, 8		VL	Power supply	Gate driving negative voltage supply
2		DESAT	Analog input	Desaturation protection input
3		GNDISO	Power supply	Gate driving isolated ground
-	4	SOFTOFF	Analog output	Soft turn-off
4	-	N.C.	-	Not connected.
5		VH	Power supply	Gate driving positive voltage supply
6		GOUT	Analog output	Sink/source output
7		CLAMP	Analog output	Active Miller clamp output
9, 16		GND	Power supply	Driver logic ground
10		IN+	Logic input	Driver logic input
11		IN-	Logic input	Driver logic input
12		RDY	Open drain	Diagnostic output (UVLO and overtemperature protection)
13		$\overline{\text{DIAG}}$	Open drain	Diagnostic output (Desat protection)
14		$\overline{\text{RST}}$	Logic input	Fault reset and shutdown logic input, active low
15		VDD	Power supply	Driver logic supply voltage

3 Device ratings

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	-0.3	6.0	V
V_{LOGIC}	Logic pins voltage (IN+, IN-, $\overline{RST}$) vs. GND	-0.3	6.0	V
VH	Positive supply voltage VH vs. GNDISO	-0.3	36	V
VL	Negative supply voltage VL vs. GNDISO	-15	0.3	V
V_{HL}	Differential supply voltage VH vs. VL	-0.3	36	V
V_{OUT}	Voltage on gate driver outputs (GOUT, CLAMP, SOFTOFF) vs. VL	-0.3	(+20, VH+0.3)min	V
V_{DESAT}	Voltage on DESAT vs. GNDISO	-0.3	VH + 0.3	V
V_{DIAG}	Open drain output voltage vs. GND	-0.3	6.0	V
V_{RDY}	Open drain output voltage vs. GND	-0.3	6.0	V
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C
ESD	HBM (human body model)	2		kV

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Package	Value	Unit
$R_{th(JA)}$	Thermal resistance junction-to-ambient	SO-16W	74	°C/W

3.3 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Min.	Max.	Unit
VDD	Logic supply voltage vs. GND	3.1	5.5	V
V_{LOGIC}	Logic pins (IN+, IN-, $\overline{RST}$) voltage vs. GND	0	5.5	V
$V_{SOFTOFF}$	SOFTOFF pin voltage vs. VL	0	VH	V
VH	Positive supply voltage (VH vs. GNDISO)	5	32	V
VL	Negative supply voltage (VL vs. GNDISO)	-10	0	V
V_{HL}	Differential supply voltage (VH vs. VL)	-	32	V
$V_{DESATth}$	Threshold voltage of DESAT protection vs. GND	-	VH - 2	V
F_{SW}	Maximum switching frequency (1)	-	1	MHz
T_J	Operating junction temperature	-40	125	°C
T_{amb}	Ambient temperature	-40	125	°C

1. *Actual limit depends on power dissipation and T_J.*

4 Electrical characteristics

Test conditions: T_J = 25 °C, VH = 15 V, VL = GNDISO, VDD = 5 V, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Dynamic characteristics							
t_{Don}	IN+, IN-	Input to output propagation delay ON	(1)	55	75	95	ns
t_{Doff}	IN+, IN-	Input to output propagation delay OFF	(1)	55	75	95	ns
t_{Drst}	$\overline{RST}$	Reset to output propagation delay OFF	No load	55	75	95	ns
t_r	GOUT	Rise time	(1) 20% to 80%, C_L = 3.3 nF	-	24	-	ns
t_f	GOUT	Fall time	(1) 80% to 20%, C_L = 3.3 nF	-	16	-	ns
PWD	GOUT	Pulse width distortion $\lvert t_{Don} - t_{Doff} \rvert$	t_{IN} > 100 ns	-	0	10	ns
t_{INmin}	IN+, IN-, $\overline{RST}$	Minimum propagated input pulse	C_L = 2 nF, R_{GON} = R_{GOFF} = 3.9 Ω	-	17	-	ns
CMTI (2)		Common-mode transient immunity $\lvert dV_{ISO}/dt \rvert$	V_{CM} = 1200 V, see Figure 23	200	-	-	V/ns
Supply voltage							
VDD_{on}	VDD	VDD UBLO turn-on threshold		2.85	2.95	3.05	V
VDD_{off}	VDD	VDD UVLO turn-off threshold		2.60	2.80	2.95	V
VDD_{hyst}	VDD	VDD UVLO hysteresis		120	160	180	mV
$t_{VDD-RDY}$	RDY	VDD UVLO to RDY low delay	See Figure 5	1.5	2.5	3.5	µs
$t_{VDD-GOUT}$	GOUT	VDD UVLO to GOUT low delay	See Figure 5	1.6	2.6	3.6	µs
I_{QDD}	VDD	VDD quiescent supply current	IN+ = 0	1.2	2.0	2.5	mA
			IN+ = RDY = VDD, IN- = GND	8	11	13	
VH_{on}	VH	VH UVLO turn-on threshold	STGAP3S3S	12.9	13.6	14.3	V
			STGAP3S3IF	11.3	11.9	12.5	
VH_{off}	VH	VH UVLO turn-off threshold	STGAP3S3S	12.2	12.8	13.4	V
			STGAP3S3IF	10.5	11.1	11.7	
VH_{hyst}	VH	VH UVLO hysteresis		0.6	0.8	1.0	V
t_{VH-RDY}	RDY	VH UVLO to RDY low delay	See Figure 6	10	15	20	µs
$t_{VH-GOUT}$	GOUT	VH UVLO to GOUT low delay	See Figure 6	1.5	2.5	3.5	µs
I_{QH}	VH	VH quiescent supply current	IN+ = GND	3	5	7	mA
SafeClp	GOUT	GOUT active clamp	I_{GOUT} = 0.2 A, VH floating	-	2.0	2.3	V

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Logic inputs							
V_{il}	IN+, IN-, $\overline{RST}$	Low-level logic threshold voltage		0.29·VDD	0.33·VDD	0.37·VDD	V
V_{ih}	IN+, IN-, $\overline{RST}$	High-level logic threshold voltage		0.62·VDD	0.66·VDD	0.70·VDD	V
I_{IN+h}	IN+	IN+ logic “1” input bias current	IN+ = VDD	120	150	210	µA
I_{IN+l}	IN+	IN+ logic “0” input bias current	IN+ = GND	-	-	1	µA
R_{in_pd}	IN+	Input pull-down resistors	IN+ = 5 V	23	30	42	kΩ
I_{IN-l}	IN-, $\overline{RST}$	IN-, $\overline{RST}$ logic “0” input bias current	IN-, $\overline{RST}$ = GND	40	55	70	µA
I_{IN-h}	IN-, $\overline{RST}$	IN-, $\overline{RST}$ logic “1” input bias current	IN-, $\overline{RST}$ = VDD	-	-	1	µA
R_{in_pu}	IN-, $\overline{RST}$	Input pull-up resistors	IN+ = GND	70	95	125	kΩ
t_{rst}	$\overline{RST}$	Minimum pulse width to rest $\overline{DIAG}$	(3)	240	500	800	ns
Driver buffer section							
I_{GON}	GOUT	Source short-circuit current	T_J = 25 °C	2.5	3.0	3.5	A
			-40 °C ≤ T_J ≤ 125 °C (2)	2.2	-	3.8	
V_{GON}	GOUT	GOUT output high-level voltage	I_{GON} = 100 mA	0.16	0.19	0.22	V
R_{DON}	GOUT	Source R_{DS_ON}	I_{GON} = 100 mA	1.6	1.9	2.2	Ω
I_{GOFF}	GOUT	Sink short-circuit current	T_J = 25 °C	2.5	3.0	3.5	A
			-40 °C ≤ T_J ≤ 125 °C (2)	2.2	-	4.0	
V_{GOFF}	GOUT	Sink output low-level voltage	I_{GOFF} = 100 mA	0.09	0.12	0.15	V
R_{DOFF}	GOUT	Sink R_{DS_ON}	I_{GOFF} = 100 mA	0.9	1.2	1.5	Ω
Miller clamp driver							
$V_{CLAMPth}$	CLAMP	CLAMP voltage threshold vs. VL		1.8	2.0	2.2	V
I_{CLAMP}	CLAMP	CLAMP short-circuit current	T_J = 25 °C	2.5	3.0	3.5	A
			-40 °C ≤ T_J ≤ 125 °C (2)	2.0	-	4.0	
V_{CLAMP_L}	CLAMP	CLAMP low-level output vs. VL	I_{CLAMP} = 100 mA	0.06	0.12	0.17	V
R_{CLAMP}	CLAMP	CLAMP R_{DS_ON}	I_{CLAMP} = 100 mA	0.6	1.15	1.7	Ω
t_{CLAMP}	CLAMP	Miller clamp intervention time		30	55	80	ns
Desaturation protection							
$V_{DESATth}$	DESAT	Desaturation threshold	STGAP3S3S	5.70	6.00	6.30	V
			STGAP3S3IF	8.55	9.00	9.45	
I_{DESAT}	DESAT	DESAT blanking charge current	V_{DESAT} = 0 V	0.93	1.00	1.10	mA
I_{DESoff}	DESAT	DESAT blanking discharge current	V_{DESAT} = 8 V, IN+ = GND	110	150	195	mA
$t_{DESfilter}$	DESAT	DESAT pin deglitch filter	STGAP3S3S Step on DESAT pin: 0 → ($V_{DESATth}$+ 1 V)	-	120	-	ns
			STGAP3S3IF Step on DESAT pin: 0 → ($V_{DESATth}$+ 1 V)	-	150	-	ns

Symbol	Pin	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{BLK}	DESAT	DESAT protection fixed blanking time	(3)	180	200	220	ns
t_{DESAT}	DESAT	DESAT protection intervention time	(3) Step on DESAT pin: 0 → ($V_{DESATth}$+ 1 V) Time from step to SOFTOFF / GOUT 90%, No load	80	150	220	ns
t_{DIAG}	$\overline{DIAG}$	DESAT event to $\overline{DIAG}$ low delay	(3)	-	1.8	2.5	µs
SOFTOFF (STGAP3S3S only)							
I_{STO}	SOFTOFF	Soft turn-off current on fault conditions	T_J = 25 °C	700	800	900	mA
			-40 °C ≤ T_J ≤ 125 °C (2)	550	-	1100	
$t_{SOFTOFF}$	SOFTOFF	Soft turn-off deactivation limit	(3)	4	5	6	µs
Overtemperature protection							
T_{SD}		Shutdown temperature		164	-	-	°C
T_{hys}		Temperature hysteresis		-	20	-	°C
t_{OT-RDY}		Overtemperature to RDY low delay	(2) See Figure 17	15	23	30	µs
$t_{OT-GOUT}$		Overtemperature to GOUT low delay	(2) See Figure 17	1.5	2.5	3.5	µs
Diagnostic							
I_{DIAG}	$\overline{DIAG}$	$\overline{DIAG}$ low-level sink current	V_{DIAG} = 0.4 V	20	30	40	mA
I_{RDY}	RDY	RDY low-level sink current	V_{RDY} = 0.4 V	20	30	40	mA
R_{DIAG_pu}	$\overline{DIAG}$, RDY	$\overline{DIAG}$ & RDY pull-up resistor	$\overline{DIAG}$, RDY = GND	35	55	72	kΩ

1. *See Figure 22.*
2. *Characterization data, not tested in production.*
3. *See Figure 13.*

5 Isolation

Table 6. Isolation and safety specifications

Symbol	Parameter	Test conditions	Value	Unit
General				
CLR	Clearance (Minimum external air gap)	Measured from input terminals to output terminals, shortest distance trough air	8	mm
CPG	Creepage (Minimum external tracking)	Measured from input terminals to output terminals, shortest distance path along body	8	mm
CTI	Comparative tracking index (Tracking resistance)	IEC 60112	≥ 400	V
-	Material group	According to IEC 60664-1	II	-
-	Overvoltage category per IEC 60664-1	Rated mains voltages ≤ 150 V_{RMS}	I - IV	-
		Rated mains voltages ≤ 300 V_{RMS}	I - IV	-
		Rated mains voltages ≤ 600 V_{RMS}	I - IV	-
		Rated mains voltages ≤ 1000 V_{RMS}	I - III	-
DIN EN IEC 60747-17 (VDE 0884-17)				
V_{IORM}	Maximum repetitive isolation voltage	AC voltage	1200	V_{PEAK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave)	850	V_{RMS}
		DC voltage	1200	V_{PEAK}
V_{PR}	Partial discharge test voltage	Method a, type and sample test $V_{PR} = V_{IORM} \times 1.6$, t_m = 10 s Partial discharge < 5 pC	1920	V_{PEAK}
		Method b1, 100% production test $V_{PR} = V_{IORM} \times 1.875$, t_m = 1 s Partial discharge < 5 pC	2250	V_{PEAK}
V_{IOTM}	Maximum transient isolation voltage	Method a, type and sample test t_{ini} = 60 s	8000	V_{PEAK}
$V_{IOTM,test}$	Transient isolation voltage test	Method b1, 100% production test $V_{IOTM,test} = V_{IOTM} \times 1.2$, t_{ini} = 1 s	9600	V_{PEAK}
V_{IMP}	Maximum impulse voltage	Type test; tested in air 1.2/50 µs waveform per IEC 62368-1	8000	V_{PEAK}
V_{IOSM}	Maximum surge isolation voltage	Type test; tested in oil 1.2/50 µs waveform per IEC 62368-1	12800	V_{PEAK}
R_{IO}	Isolation resistance	Type test; V_{IO} = 500 V T_{amb} = 25 °C	> 10^{12}	Ω
		Type and sample test; V_{IO} = 500 V 100 °C ≤ T_{amb} ≤ T_S = 150 °C	> 10^{11}	
		Type and sample test; V_{IO} = 500 V T_{amb} = T_S = 150 °C	> 10^{9}	
C_{IO}	Barrier capacitance, input to output	Typical value, not tested in production	1	pF

Symbol	Parameter	Test conditions	Value	Unit
UL-1577				
V_{ISO}	Isolation withstand voltage	60 s; type test	5700 / 8061	V_{RMS} / V_{PEAK}
$V_{ISO,test}$	Isolation voltage test	1 s; 100% production	6840 / 9674	V_{RMS} / V_{PEAK}

6 Functional description

The STGAP3S is a family of fully protected single gate drivers with integrated galvanic isolation that relies on state-of-the-art capacitive communication. The device is able to work with high voltage rails up to 1200 V and is offered in several variants with 3 A output current capability and dedicated UVLO and DESAT options for IGBTs and SiC MOSFETs.

The control interface side consists of two gate drive input pins (IN+, IN-), a fault reset and shutdown input pin ($\overline{\text{RST}}$), and two open drain output pins for desaturation protection ($\overline{\text{DIAG}}$) and for UVLO and overtemperature protections (RDY).

The dual inputs pins allow the selection of gate driving control signal polarity control and the implementation of HW interlocking protection to avoid cross conduction in case of controller malfunction.

The driving side consists of the gate control pin (GOUT), the desaturation protection pin (DESAT), a pin for adjustable soft turn-off protection (SOFTOFF) and a pin for the optional negative supply voltage (VL).

The ultrafast DESAT protection event is latched and a turn-off speed can be optimized by the tunable SOFTOFF function, to maximize the protection turn-off speed while avoiding excessive collector overvoltage spikes. The fault condition is notified to the control device by an open drain diagnostic pin ($\overline{\text{DIAG}}$).

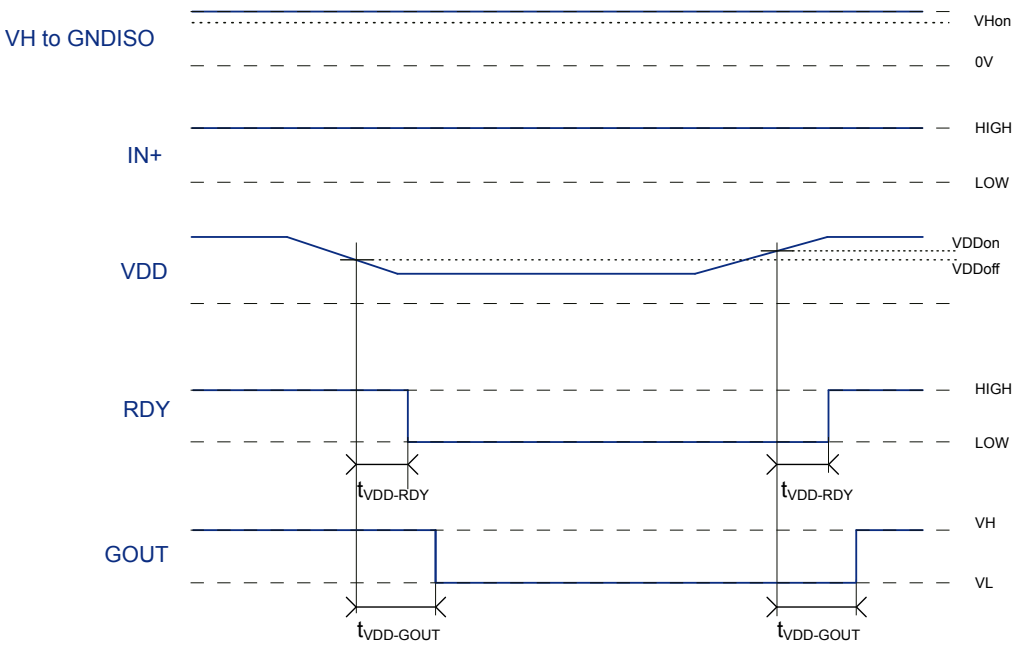
The undervoltage lock out (UVLO) feature prevents the external power switch to be actuated with insufficient gate voltage, the UVLO event is notified through a diagnostic open drain pin (RDY).

The internal Miller clamp function enables the use of fast switching speeds while preventing the unwanted induced turn-on side effect.

6.1 Power supplies and UVLO

Undervoltage lockout (UVLO) protection is available on both the control interface supply voltage VDD (see Figure 5) and on the driving side supply voltage VH (see Figure 6). A fixed hysteresis sets the turn-off threshold, thus avoiding intermittent operation.

Figure 5. UVLOD protection timings



There are two options for the UVLOH threshold:

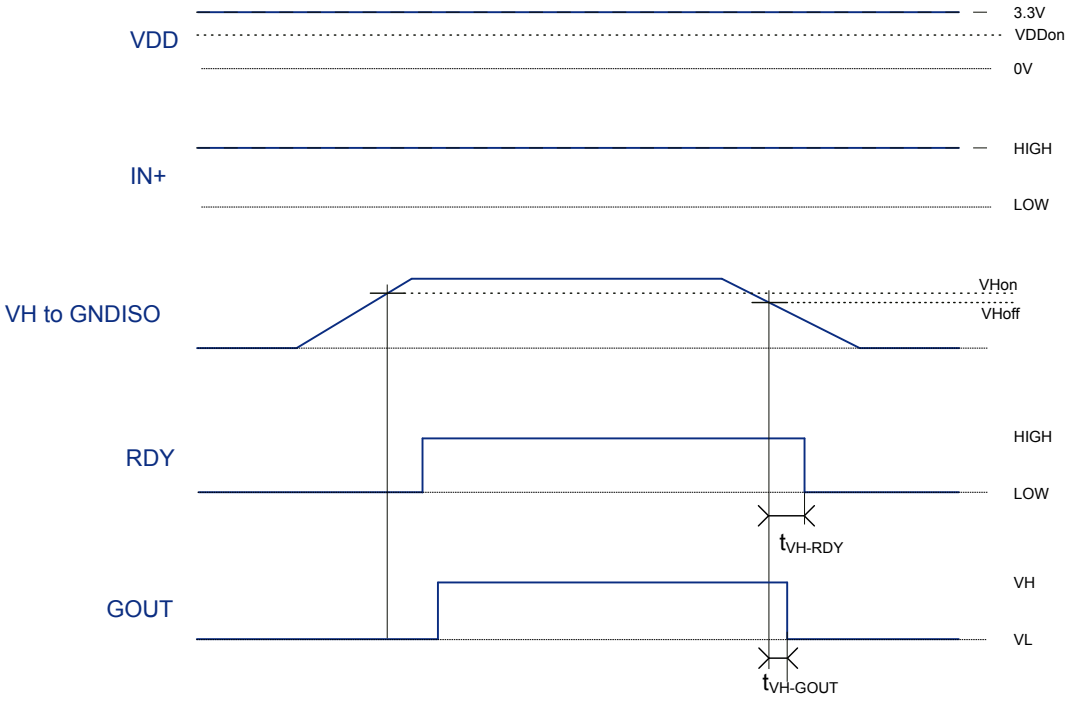
- The threshold of STGAP3S3IF suitable for driving IGBTs and Si MOSFETs.
- The threshold of STGAP3S3S suitable for driving SiC MOSFETs.

When the VH voltage falls below the VH_{off} threshold, the output buffer enters a “safe state”. When the VH voltage reaches the VH_{on} threshold, the device returns to normal operation and sets the output according to the actual input pins status.

The VDD and VH supply pins must be properly filtered with local bypass capacitors. The use of capacitors with different values in parallel provides both local storage for impulsive current supply and high-frequency filtering.

The use of low-ESR SMT ceramic capacitors is recommended because they provide the optimal filtering. A 100 nF ceramic capacitor must be placed as close as possible to each supply pin, and a second bypass capacitor with a value in the range between 1 µF and 10 µF should be placed close to it.

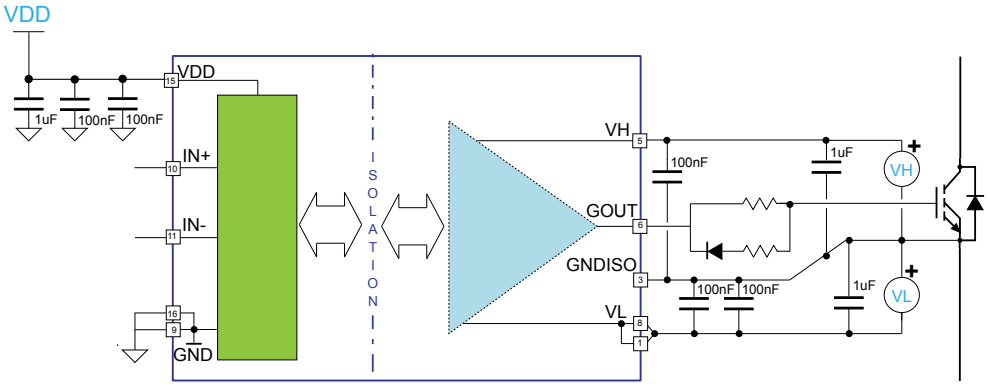
Figure 6. UVLOH protection timings



The driver allows to implement either unipolar gate driving or bipolar gate driving for the power switch.

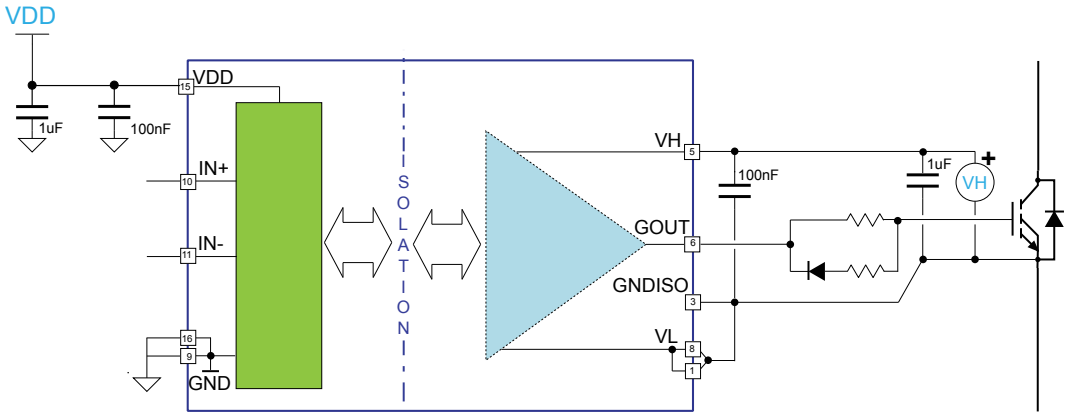
In the case of bipolar gate driving (see Figure 7), the negative supply voltage shall be connected between the GNDISO and VL pins. The use of a negative gate driving can further mitigate the risk of induced turn-on due to Miller effect in hard-switching conditions, and can also help to increase the turn-off speed of the power switch.

Figure 7. Power supply configuration for bipolar gate driving



If a unipolar gate driving is used (see Figure 8), the GNDISO and VL pins shall be connected together by means of short traces.

Figure 8. **Power supply configuration for unipolar gate driving**



6.2 Power-up, power-down, and “safe state”

There is no required power-on or power-off sequencing of the supply pins, as long as the device is operated within the maximum recommended values.

If the primary side is not supplied, or one of the driver’s protection is triggered (VDD UVLO, VH UVLO, DESAT, Overtemperature) the device enters in “safe state”.

The following conditions define the “safe state”:

- GOUT: forced to VL;
- SOFTOFF: forced to VL;
- DESAT: forced to GNDISO (internal switch on);
- CLAMP: forced to V_L.

Such conditions are maintained at power-up of the device and during the device power-down phase (VH < VH_{off} and VDD < VDD_{off}), regardless of the value of the input pins.

The device integrates a structure that clamps the driver output to a voltage not higher than SafeClp when the VH voltage is not high enough to actively turn the internal GOFF MOSFET on. If the VH positive supply pin is floating or not supplied, the GOUT pin is clamped to a voltage smaller than SafeClp.

At the power-up, the diagnostic pin RDY is forced to GND and remains in such condition until both VDD and VH rise above the relative $UVLO_{on}$ thresholds.

After power-up of both the isolated and low voltage side, the device output state depends on the input pins status.

6.3 Control inputs

The device is controlled through the following logic inputs:

- IN+ and IN-: driver inputs
- $\overline{RST}$: Active low shutdown input.

And the following logic outputs:

- $\overline{DIAG}$: desaturation event diagnostic signal (open drain)
- RDY: diagnostic power-good signal (open drain).

The device is designed to work with 5 V or 3.3 V VDD supply voltage, and in order to maximize noise margin the logic input thresholds vary according to VDD voltage. The I/Os IN-, $\overline{DIAG}$, RDY, and $\overline{RST}$ have a weak internal pull-up resistor, while IN+ has a weak internal pull-down resistor in order to force the output to switch off the external power device in case of floating inputs.

The truth table in Table 7, describes how the outputs are driven by the logics inputs.

Table 7. Truth table (applicable when device is not in UVLO or "safe state")

Input pins			Output pin
$\overline{RST}$	IN+	IN-	GOUT
L	X (1)	X (1)	LOW
H	L	L	LOW
H	H	L	**HIGH**
H	L	H	LOW
H	H	H	LOW (interlocking)

1. *Do not care.*

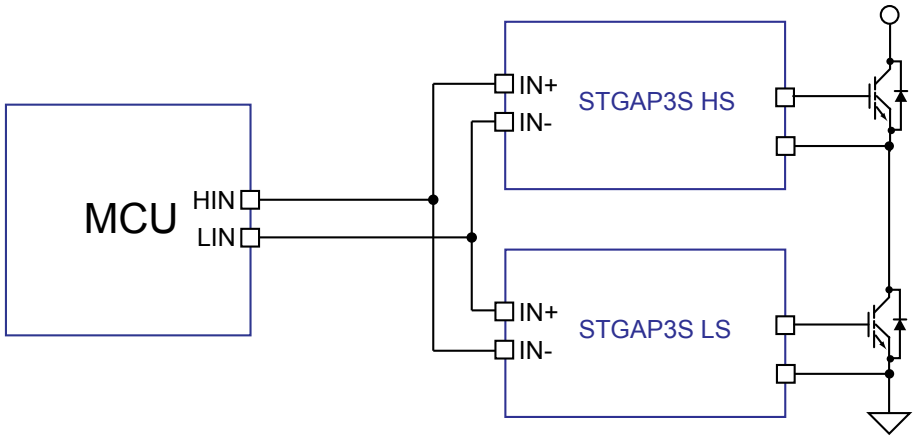
A deglitch filter is applied to device inputs ($\overline{RST}$, IN+, IN-). Each input pulse, positive or negative, shorter than t_{INmin} is neglected by internal logic. This minimum input pulse timing filters out both positive and negative pulses at the IN+, IN-, and $\overline{RST}$ pins.

6.3.1 Anti cross conduction interlocking

When single gate drivers are used in half-bridge configuration, they usually do not allow preventing cross conduction in case of wrong input signals coming from the controller device. Indeed, each driver does not have the possibility to know the status of the input signal of the other companion driver in the same leg. Thanks to the availability of two input pins with opposite polarity, the STGAP3S allows implementing a hardware interlocking that prevents cross conduction even in case of wrong input signals generated by the control unit.

This functionality can be achieved by implementing the connection shown in Figure 9.

Figure 9. Hardware cross conduction prevention in half-bridge configuration with two single gate drivers



6.4 Miller clamp function

The Miller clamp function allows the mitigation of the positive and negative gate spikes caused by Miller current during the power stage hard-switching commutations in half-bridge configurations.

When the driven power switch is in the OFF state the driver operates to avoid the induced turn-on phenomenon that may occur due to C_{GD} capacitance during the turn-on of the other switch in the same leg.

The Miller clamp MOSFET is integrated in the gate driver and its drain is connected directly to the gate of the external power switch through the CLAMP pin. The use of a small resistor (0.5 to 1 Ω) in the connection loop might help to damp ringing and oscillations.

When GOUT is HIGH the Miller clamp internal MOSFET is OFF, and the gate voltage is not monitored.

As soon as GOUT is set low the CLAMP comparator starts monitoring the gate voltage, and when it goes below the $V_{CLAMPth}$ threshold the internal N-channel clamp MOSFET is activated thus creating a low impedance path between the power switch gate and VL. Such condition is latched and maintained until GOUT is set high at the following turn-on cycle, forcing the clamp N-channel MOSFET to turn off.

Figure 10. Internal Miller CLAMP, schematic principle

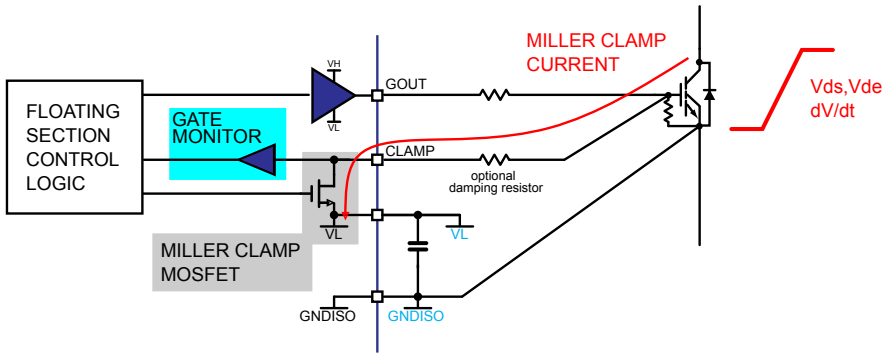
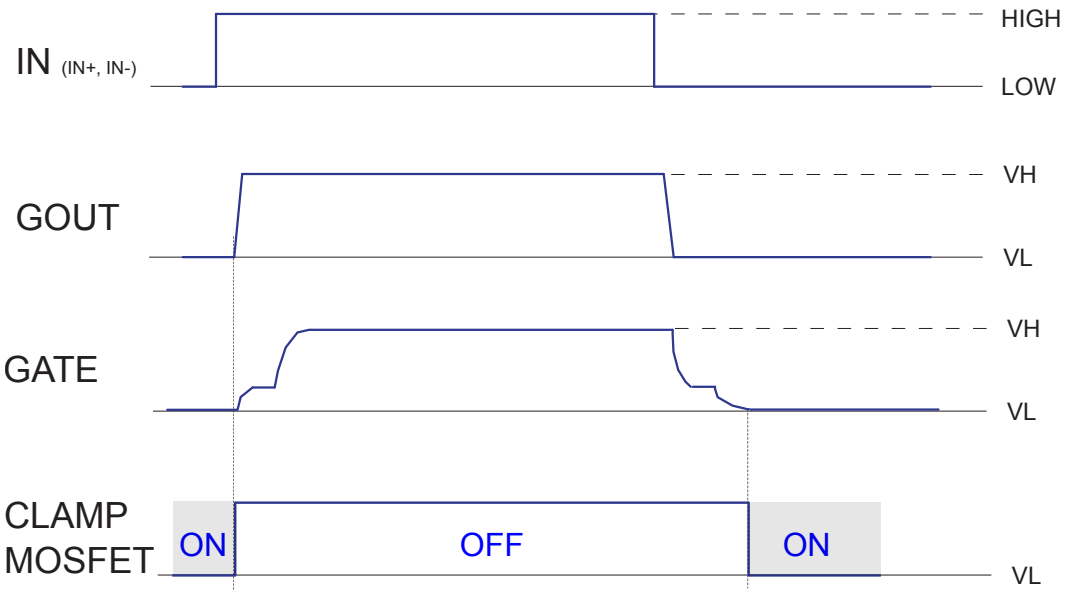


Figure 11. Internal Miller CLAMP driver, timings definition



6.5 Desaturation protection

This feature allows implementing overload and short-circuit protection for the external power switch. The DESAT pin monitors the drain/collector during the ON time, and if the protection threshold is reached, the external power switch is promptly turned off within a t_{DESAT} time. In that situation the DESAT intervention is reported to the control side and the dedicated $\overline{DIAG}$ diagnostic pin is set low to notify the controlling device within the t_{DIAG} time.

During the OFF time of the external power switch (GOUT = LOW), the internal N-channel discharge MOSFET is ON to maintain the external blanking capacitor C_{blank} connected to the DESAT pin discharged (see Figure 12 and Figure 15).

As soon as the external power switch turn-on command is received (GOUT = HIGH), a blanking time t_{blank} is applied to the DESAT protection so to provide enough time to the power switch to complete the turn-on transient. During this interval the protection is masked to avoid unwanted spurious triggering. The blanking time is composed by two contributions:

- $t_{BLK:}$ an internally generated interval of fixed duration during which the internal discharge MOSFET is ON, keeping C_{blank} discharged. The discharge MOSFET is turned OFF at the end of this interval.
- t_{BLK_Cblank}: the time that it takes for the DESAT blanking charge current I_{DESAT} to charge the external C_{blank} capacitor up to the $V_{DESATth}$ threshold.

During a regular turn-on transition the power switch completes the transient before the expiration of the blanking time, the D_{DES} diode gets forward biased, and the DESAT pin is maintained to a value lower than the $V_{DESATth}$ protection threshold.

A deglitch filter is implemented on the DESAT pin: each pulse exceeding the $V_{DESATth}$ for a time shorter than $t_{DESfilter}$ does not trigger the protection.

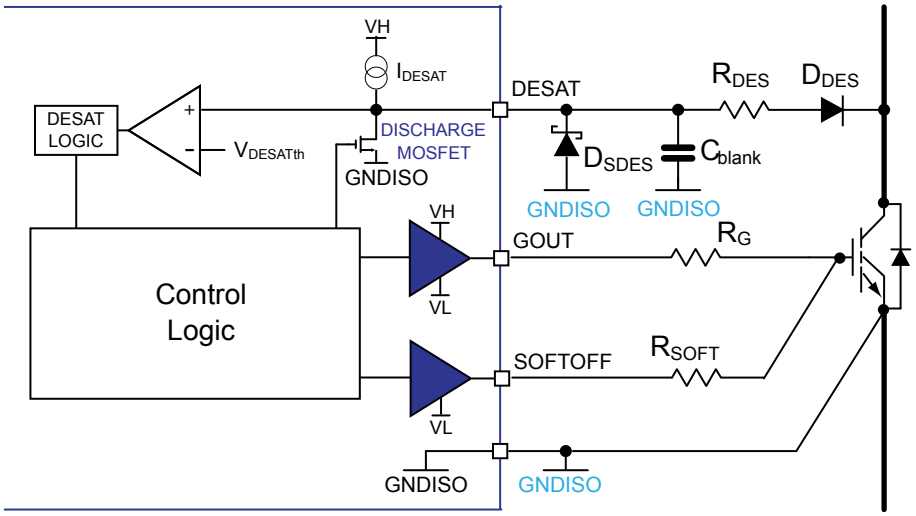
If a desaturation event occurs the V_{CE}/V_{DS} voltage increases and when the voltage at the DESAT pin reaches the desaturation threshold $V_{DESATth}$, the protection is triggered and after a t_{DESAT} time the output is turned off and the device is forced in “safe state”. The protection is latched and can only be reset by forcing the $\overline{RST}$ pin low for at least t_{rst} time.

6.5.1 Adjustable soft turn-off function (STGAP3S3S only)

The soft turn-off function is used to slow down the turn-off of the external MOSFET/IGBT when a desaturation event is triggered. This allows the reduction of the dangerous overvoltage spike on the drain/collector.

The soft turn-off function switches off the external power switch through an embedded N-channel MOSFET connected to the SOFTOFF pin. The connection of the SOFTOFF pin to the external power switch gate through a resistor is mandatory to execute the turn-off when DESAT is triggered.

Figure 12. DESAT protection connection diagram, adjustable soft turn-off

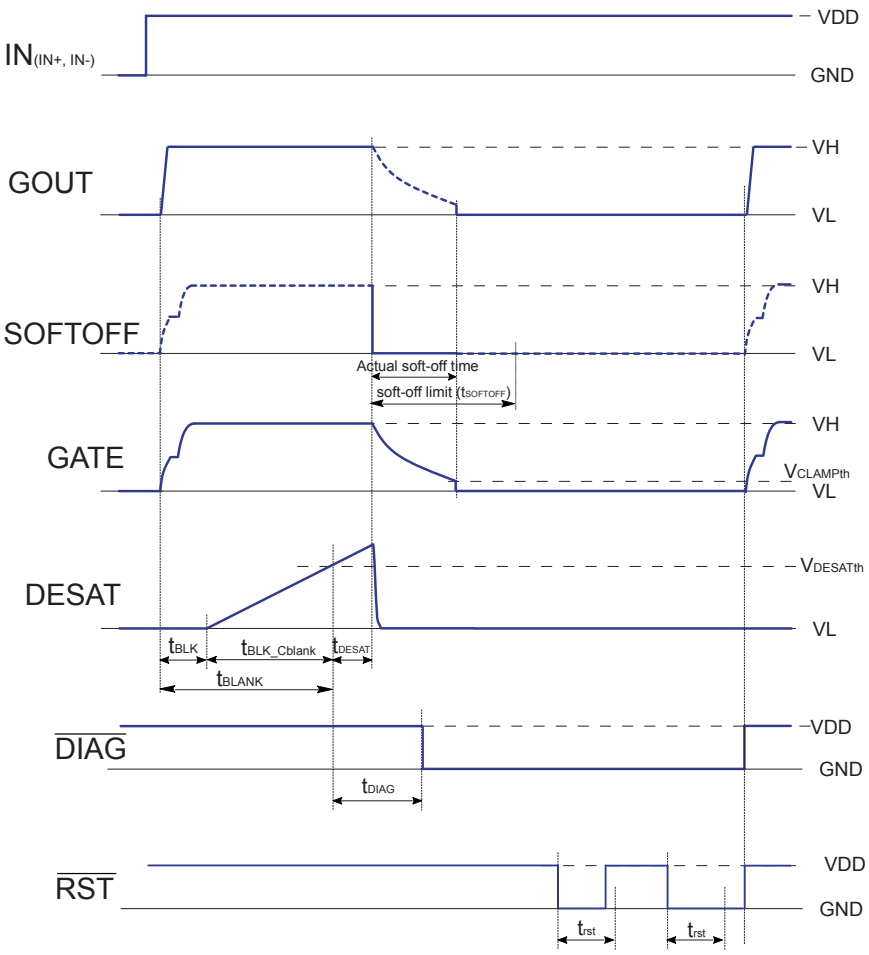


Thanks to the dedicated SOFTOFF pin, the STGAP3S offers the great advantage to fine-tune the turn-off speed in case of overload or short-circuit condition, thus allowing to find the best compromise between the reduction of the drain/collector overvoltage spike and the effective protection of the power switch from the excessive power dissipation caused by the overload. The optimal turn-off speed can be achieved by selecting the proper value of the soft turn-off external resistor.

As soon as a DESAT event is triggered, GOUT is immediately set in high impedance, the SOFTOFF internal MOSFET is turned on starting a controlled speed turn-off of the power switch.

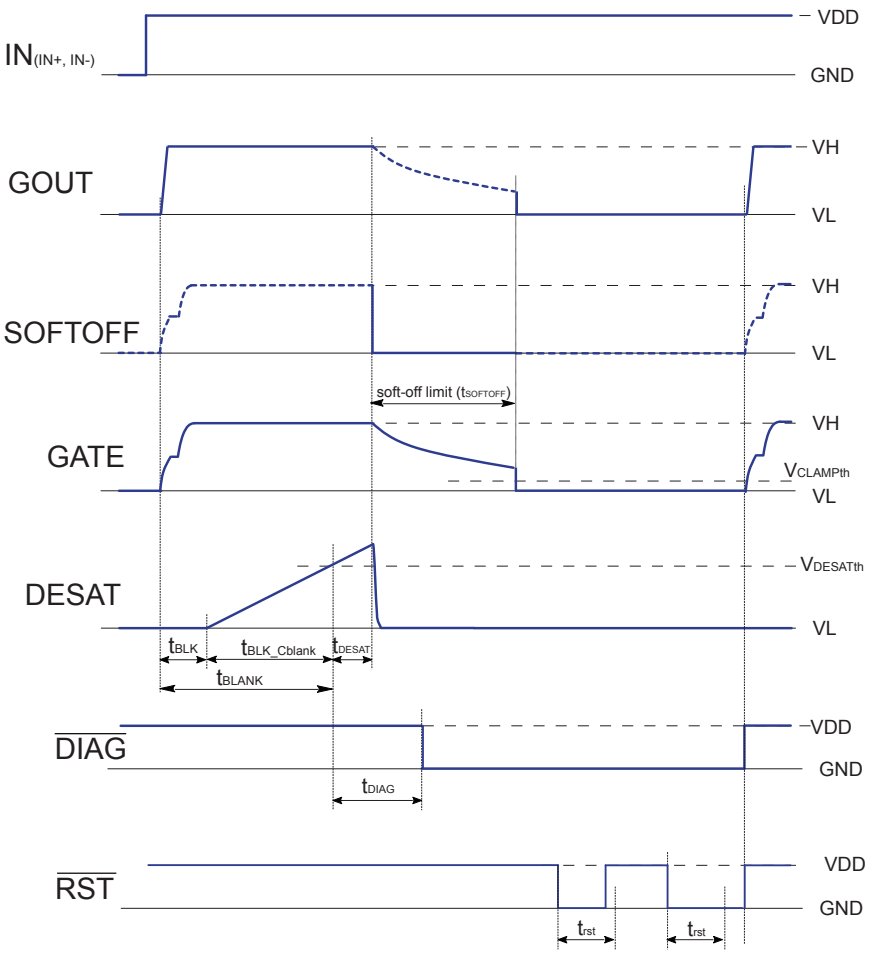
Under normal circumstances, the power switch is turned off in a relatively short time if the soft turn-off gate resistor R_{SOFT} is properly dimensioned. As soon as the gate voltage reaches the $V_{CLAMPth}$ threshold, the transient is completed, the SOFTOFF pin goes in high impedance condition and both GOUT and CLAMP pins start to actively force the gate to VL (see Figure 13).

Figure 13. DESAT protection timings, adjustable soft turn-off



The STGAP3 SOFTOFF has an internal deactivation limiting time that ends the soft turn-off phase and completes the power switch turn-off by forcing GOUT low if the gate has not reached the $V_{CLAMPth}$ threshold within a $t_{SOFTOFF}$ time from the triggering of the DESAT protection (see Figure 14).

Figure 14. DESAT protection timings, adjustable soft turn-off with deactivation time limit reached



6.5.2 Standard turn-off (STGAP3S3IF only)

Some variants in the STGAP3S3 family react to the DESAT event with a standard turn-off transient, and in that case the power switch turn-off is performed by pulling GOUT low. In these variants, the SOFTOFF pin is not present (see Figure 15 and Figure 16).

Figure 15. DESAT protection connection diagram, standard turn-off

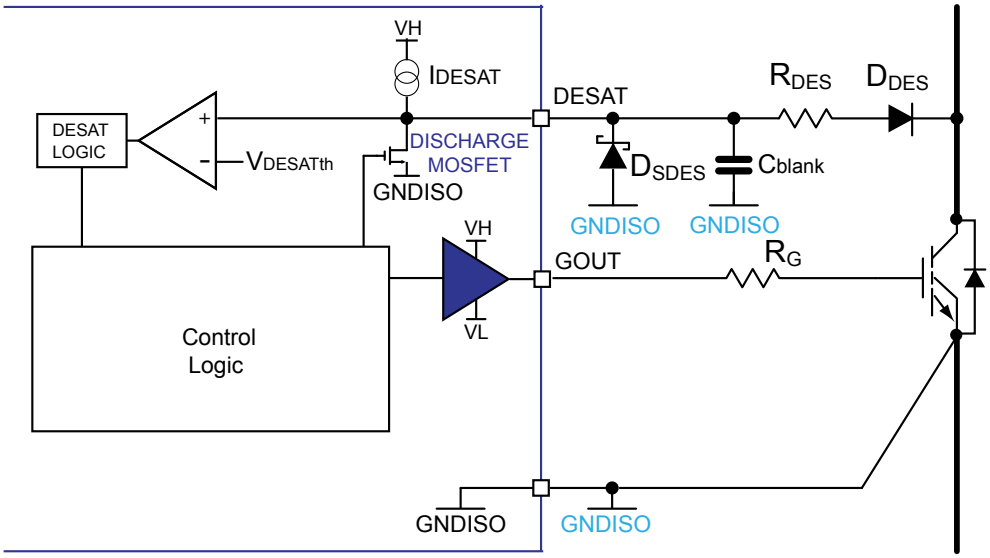
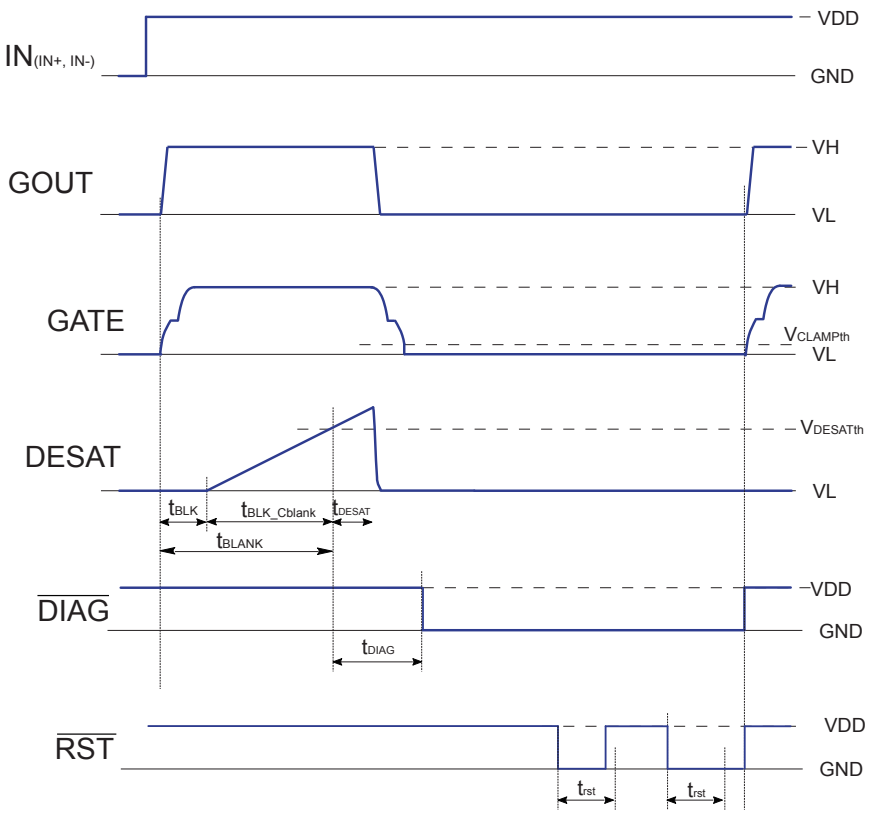


Figure 16. DESAT protection timings with standard turn-off



6.6 Watchdog

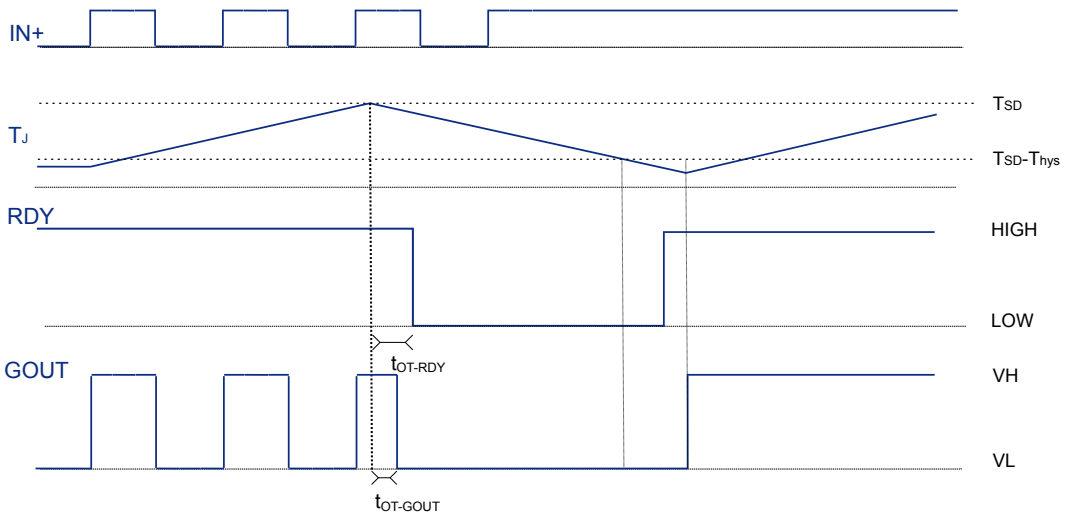
A watchdog function is implemented in the driver in order to identify when it is not able to communicate, for example because the supply voltage is not present on the control side or on the driving side.

If the control side supply is missing or in UVLO condition, the driving side immediately sets the output low and goes in “safe state”. If the driving side supply is missing, or in UVLO condition, the driver goes in “safe state” and the open drain RDY diagnostic pin is turned on after a t_{VH-RDY} time. This condition is maintained until the VH supply returns in the operative range, which establish the communication link and resumes normal operation.

6.7 Thermal shutdown protection

The device provides a thermal shutdown protection. When the junction temperature reaches the T_{SD} temperature threshold, the device is forced in “safe state”. The device operation is restored as soon as the junction temperature is lower than 'T_{SD} - T_{hys}'.

Figure 17. Overtemperature protection timings



7 Typical application diagram

Figure 18. **Typical application diagram with standard turn-off**

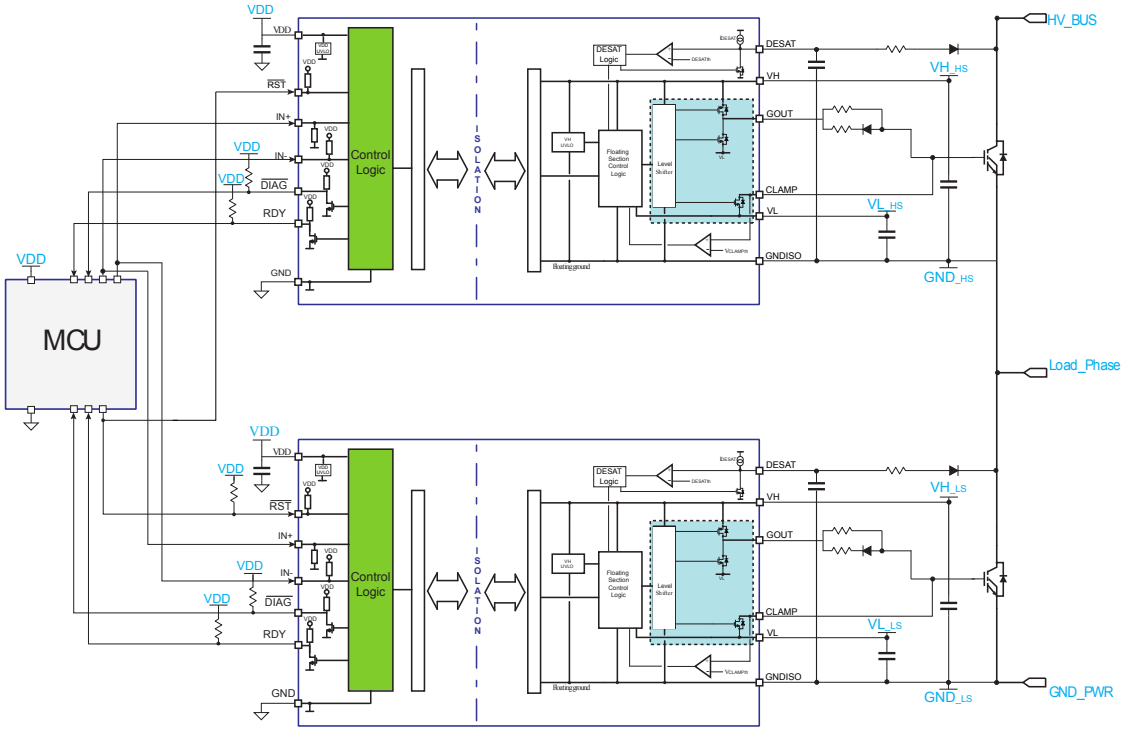
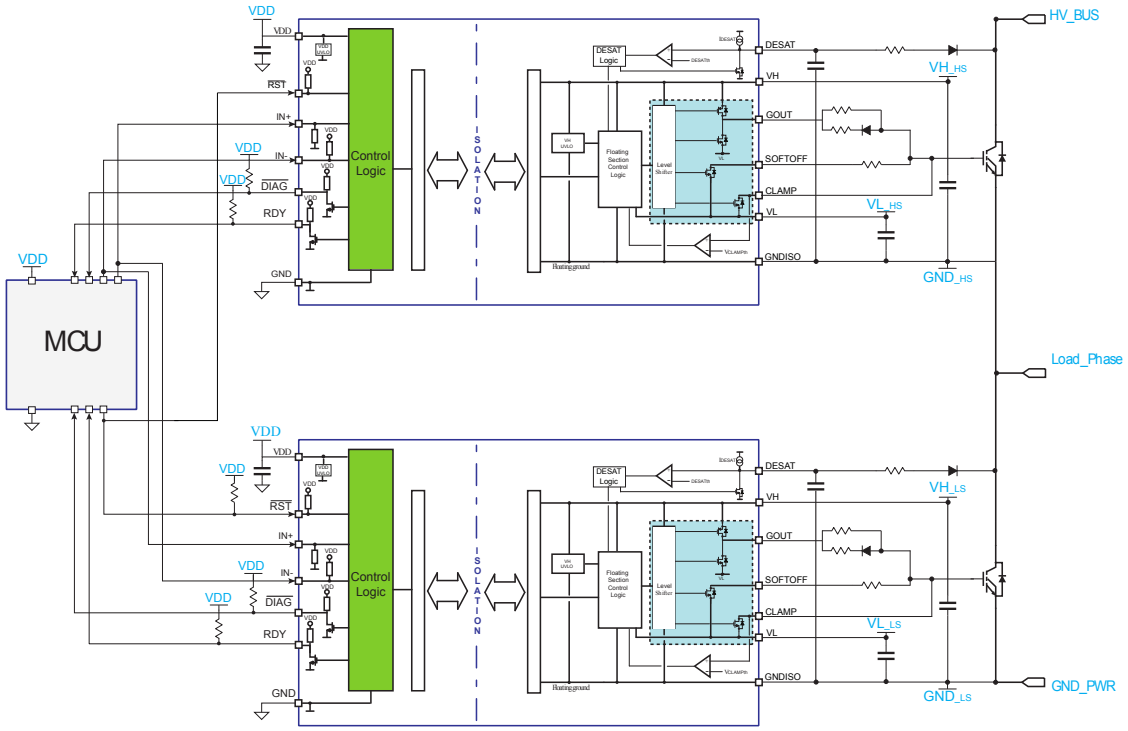


Figure 19. **Typical application diagram with SOFTOFF**



8 PCB layout

8.1 Layout guidelines and considerations

In order to optimize the PCB layout, the following considerations should be considered:

- SMT ceramic capacitors (or different types of low-ESR and low-ESL capacitors) must be placed close to each supply rail pin. In order to filter high-frequency noise and spikes, a 100 nF capacitor must be placed between VDD and GND, between VH and GNDISO, and between VL and GNDISO, as close as possible to device pins. In order to provide local storage for pulsed current, a second capacitor with a value between 1 µF and 10 µF should also be placed close to the supply pins.
- It is good practice to add filtering capacitors close to logic inputs of the device (IN+, IN-), particularly for fast switching or noisy applications.
- The power transistors must be placed as close as possible to the gate driver to minimize the gate loop area and inductance that might carry noise or cause ringing.
- To avoid degradation of the isolation between the primary and secondary side of the driver, there should not be any trace or conductive area below the driver.
- If the system has multiple layers, it is recommended to connect the VH, VL, and GNDISO pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity.

8.2 Layout example

An example of STGAP3S3 suggested PCB layout with main signals highlighted by different colors is shown in Figure 20 and Figure 21. It is recommended to follow this example for optimal positioning and connection of external components, filtering and bypass capacitors in particular.

Figure 20. Reference layout - control side (top and bottom view)

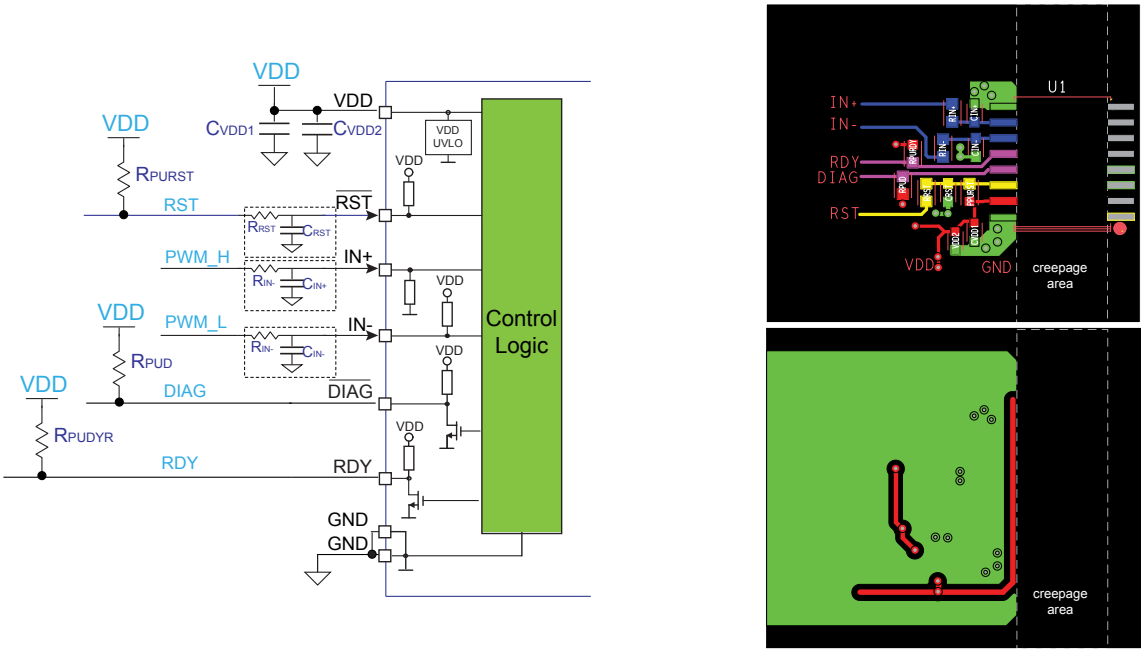
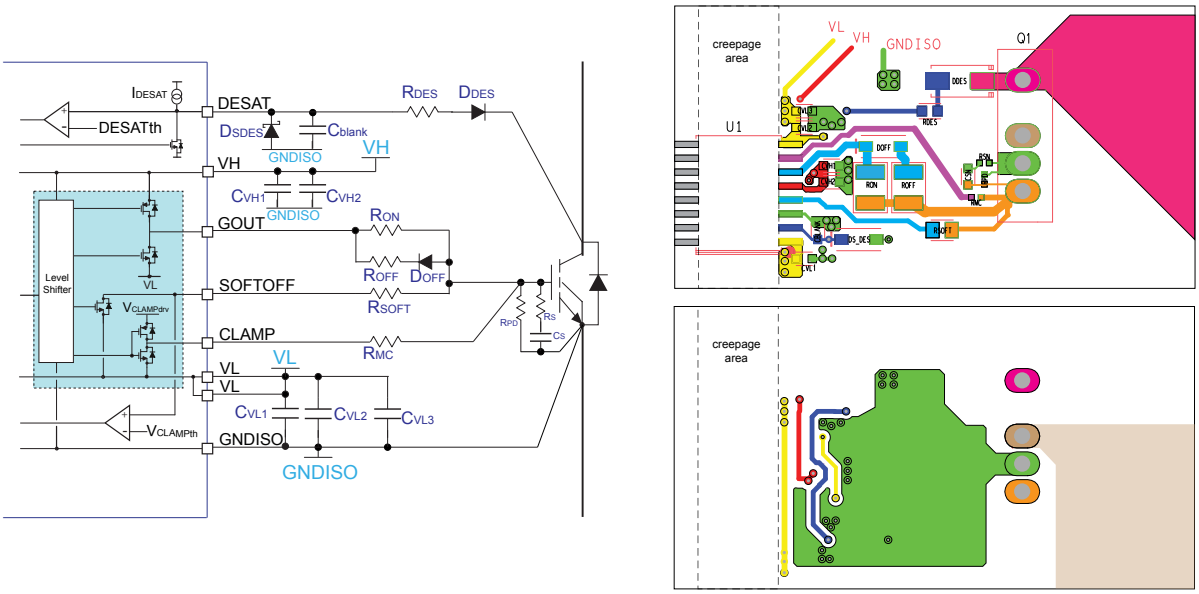


Figure 21. **Reference layout - gate driving side (top and bottom view)**



9 Unused functions

The following table lists the connections to be performed when one or more functions of the devices are unused.

Table 8. Unused functions connections

Unused functionality	Connections	Notes
Desaturation protection	• Connect DESAT to GNDISO • Leave $\overline{\text{DIAG}}$ floating • Connect SOFTOFF to VL	
Miller CLAMP	• Connect CLAMP to VL	
UVLO and thermal shutdown reporting	• Leave RDY floating	UVLO and thermal shutdown protections are always active. Leave RDY floating only if reporting of the activation of such protections to the control unit is not needed by the application.

10 Testing and characterization information

Figure 22. **Input to output timings definition**

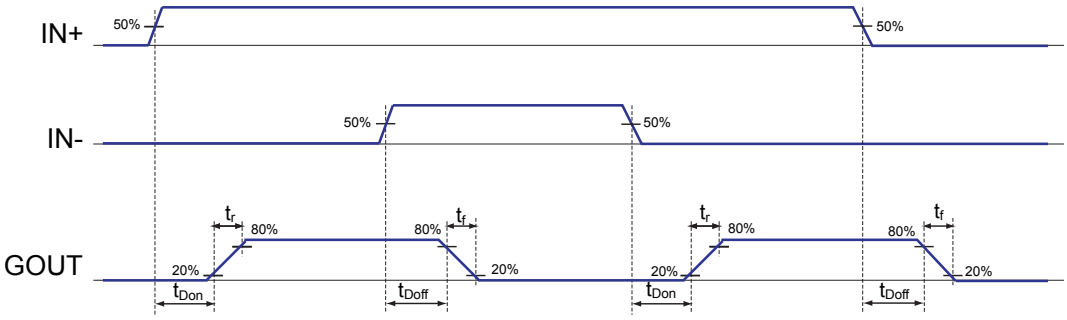
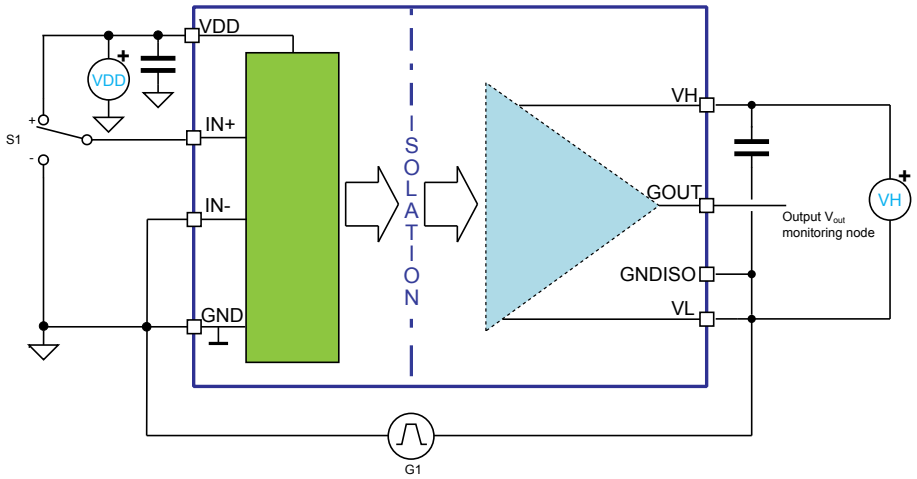


Figure 23. **CMTI test circuit**



11 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

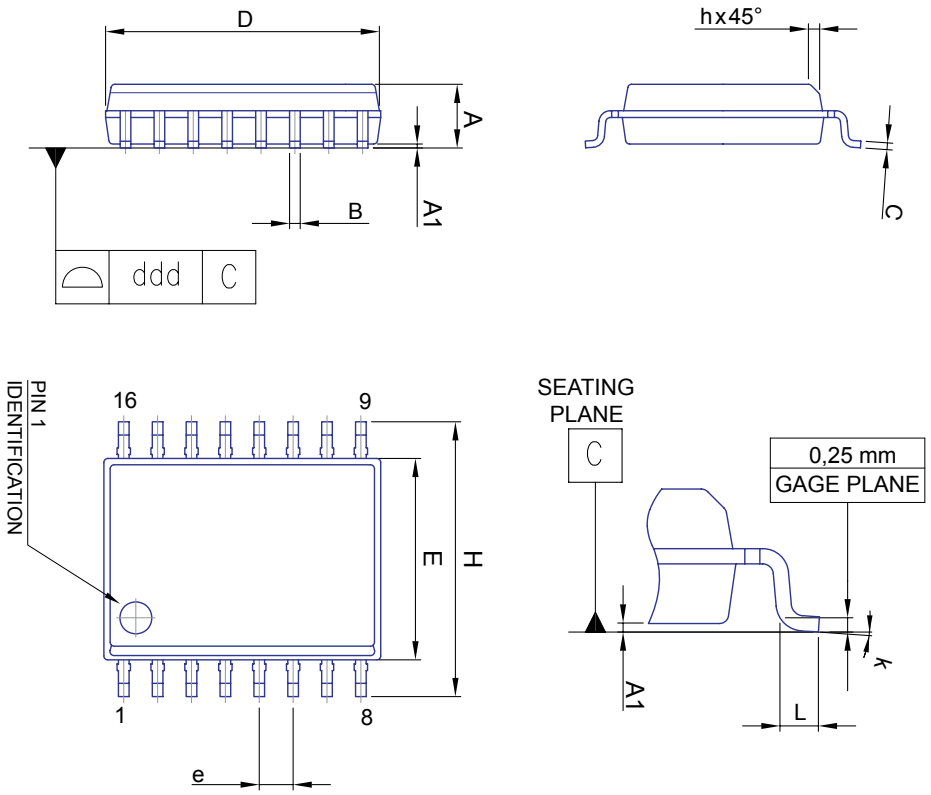
11.1 SO-16W package information

Table 9. SO-16W package dimensions

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	2.35	-	2.65
A1	0.10	-	0.30
B	0.33	-	0.51
C	0.23	-	0.32
D (1)	10.10	-	10.50
E	7.40	-	7.60
e		1.27	
H	10.00	-	10.65
h	0.25	-	0.75
L	0.40	-	1.27
k (2)	0		8
ddd		0.25	

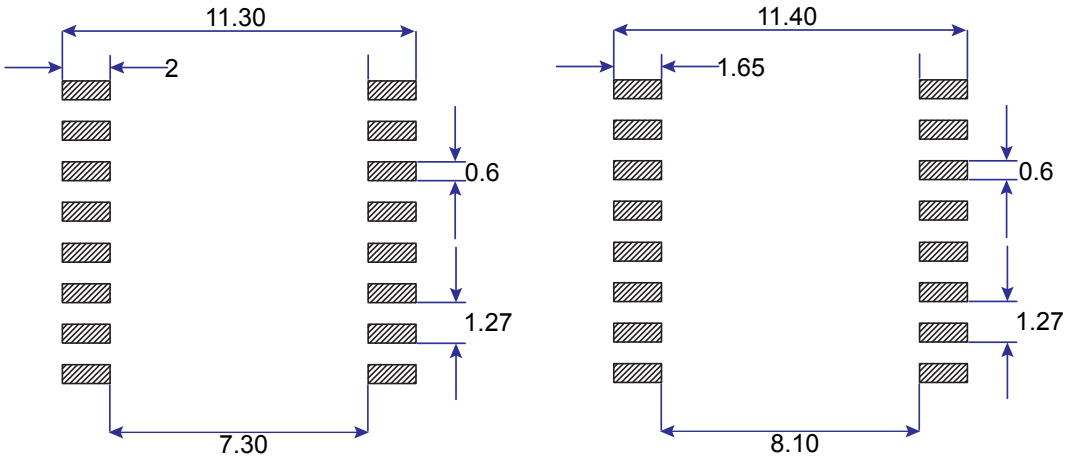
1. *Dimension “D” does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.*
2. *Degrees.*

Figure 24. **SO-16W mechanical data**



11.2 SO-16W suggested land pattern

Figure 25. **SO-16W suggested land pattern**



IPC-SM-782A
7.3 mm CLEARANCE/CREEPAGE

HV/ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

12 Ordering information

Table 10. **Device summary**

Order code	Driving stage	UVLO	DESAT threshold	SOFTOFF	Package	Package marking	Packing
STGAP3S3IF	±3 A Internal CLAMP	IGBT	9 V	No	SO-16W	GAP3S3IF	Tube
STGAP3S3IFTR	±3 A Internal CLAMP	IGBT	9 V	No	SO-16W		Tape and reel
STGAP3S3S	±3 A Internal CLAMP	SiC	6 V	Tunable	SO-16W	GAP3S3S	Tube
STGAP3S3STR	±3 A Internal CLAMP	SiC	6 V	Tunable	SO-16W		Tape and reel

Revision history

Table 11. **Document revision history**

Date	Version	Changes
16-Feb-2026	1	Initial release.

Contents

List of tables

List of figures

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.