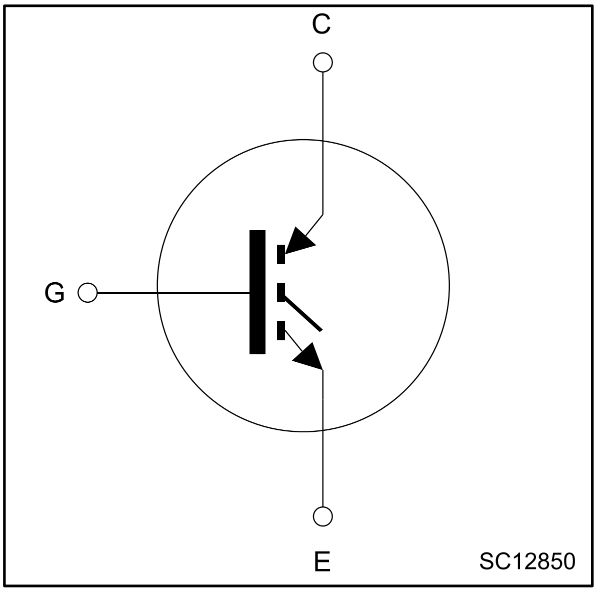
STG75M120F3D7

1200 V, 75 A trench gate field-stop M series low-loss IGBT die in D7 packing

Datasheet - production data



Features

- 10 µs of short-circuit withstand time
- Low $V_{CE(sat)}$ = 1.85 V (typ.) @ I_C = 75 A
- Positive $V_{CE(sat)}$ temperature coefficient
- Tight parameter distribution
- Maximum junction temperature: T_J = 175 °C

Applications

- Motor control
- Industrial drives
- PFC
- UPS
- Solar
- General purpose inverter

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where low-loss and short-circuit functionality are essential. Furthermore, the positive $V_{CE(sat)}$ temperature coefficient and tight parameter distribution result in safer paralleling operation.

Table 1: Device summary

Order code	V_{CE}	I_{CN}	Die size	Packing
STG75M120F3D7	1200 V	75 A	8.03 x 9.36 mm²	D7

Contents

1 Mechanical parameters

Table 2: Mechanical parameters

Symbol		Value	Unit
Die size including scribe line		8.03 x 9.36	mm²
Wafer size		200	mm
Maximum possible dice per wafer		343	dice
Die thickness		110	µm
Front side passivation		Silicone nitride	
Emitter pad size including gate pad (x2)		7.00 x 4.03	mm²
Gate pad size		1.61 x 1.01	mm²
Front side metallization	composition	AlCu	
	thickness	4.5	µm
Back side metallization	composition	Al/Ti/NiV/Ag	
	thickness	0.65	µm
Die bond		Electrically conductive glue or soft solder	
Recommended wire bonding		≤500	µm

2 Electrical ratings

2.1 Absolute maximum ratings

Table 3: Absolute maximum ratings (T_J = 25 °C unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)	1200	V
V_{GE}	Gate-emitter voltage	±20	V
I_{CN}(1)	Continuous collector current at T = 100 °C	75	A
I_{CP}(1)(2)	Pulsed collector current	225	A
t_{SC}(3)	Short -circuit withstand time V_{CC} = 600 V, V_{GE} = 15 V, $V_{CE(peak)} \leq$ 1200 V, $T_{Jstart} \leq$ 150 °C	10	µs
T_J	Operating junction temperature range	-55 to 175	°C

Notes:

(1)Nominal collector current for die packaged in ST power module solution. Current level depends on the assembly thermal properties and is limited by maximum junction temperature.

(2)Pulse width is limited by maximum junction temperature.

(3)Not tested at chip level, verified by design/characterization.

2.2 Electrical characteristics

Table 4: Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	I_C = 1 mA, V_{GE} = 0 V	1200			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 15 A			1.7	V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 1 mA	5	6	7	V
I_{CES}	Collector cut-off current	V_{GE} = 0 V, V_{CE} = 1200 V			100	µA
I_{GES}	Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = ±20 V			±500	µA

Table 5: Electrical characteristics (not tested at chip level, verified by design/characterization)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 75 A	-	1.85	2.3	V
		V_{GE} = 15 V, I_C = 75 A, T_J = 150 °C	-	2.15		V
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0 V	-	4700		pF
C_{oes}	Output capacitance		-	350		pF
C_{res}	Reverse transfer capacitance		-	190		pF
Q_g	Total gate charge	V_{CC} = 960 V, I_C = 75 A, V_{GE} = -15 to 15 V	-	350		nC
R_g	Integrated gate resistance		-	5		Ω

Table 6: Switching characteristics on inductive load

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600 V, I_C = 75 A, V_{GE} = ±15 V, R_G = 6.8 Ω	-	168	-	ns
t_r	Current rise time		-	45	-	ns
$t_{d(off)}$	Turn-off-delay time		-	229	-	ns
t_f	Current fall time		-	103	-	ns
E_{off}(1)	Turn-off switching energy		-	4.2	-	mJ
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600 V, I_C = 75 A, V_{GE} = ±15 V, R_G = 6.8 Ω, T_J = 150 °C	-	168	-	ns
t_r	Current rise time		-	49	-	ns
$t_{d(off)}$	Turn-off-delay time		-	229	-	ns
t_f	Current fall time		-	168	-	ns
E_{off}(1)	Turn-off switching energy		-	5.7	-	mJ

Notes:

(1)Including the tail of the collector current.

The aforementioned values are not tested at chip level and are strongly dependent on the package/module design and the mounting technology.

3 Die layout

Figure 1: Die drawing (dimensions are in mm)

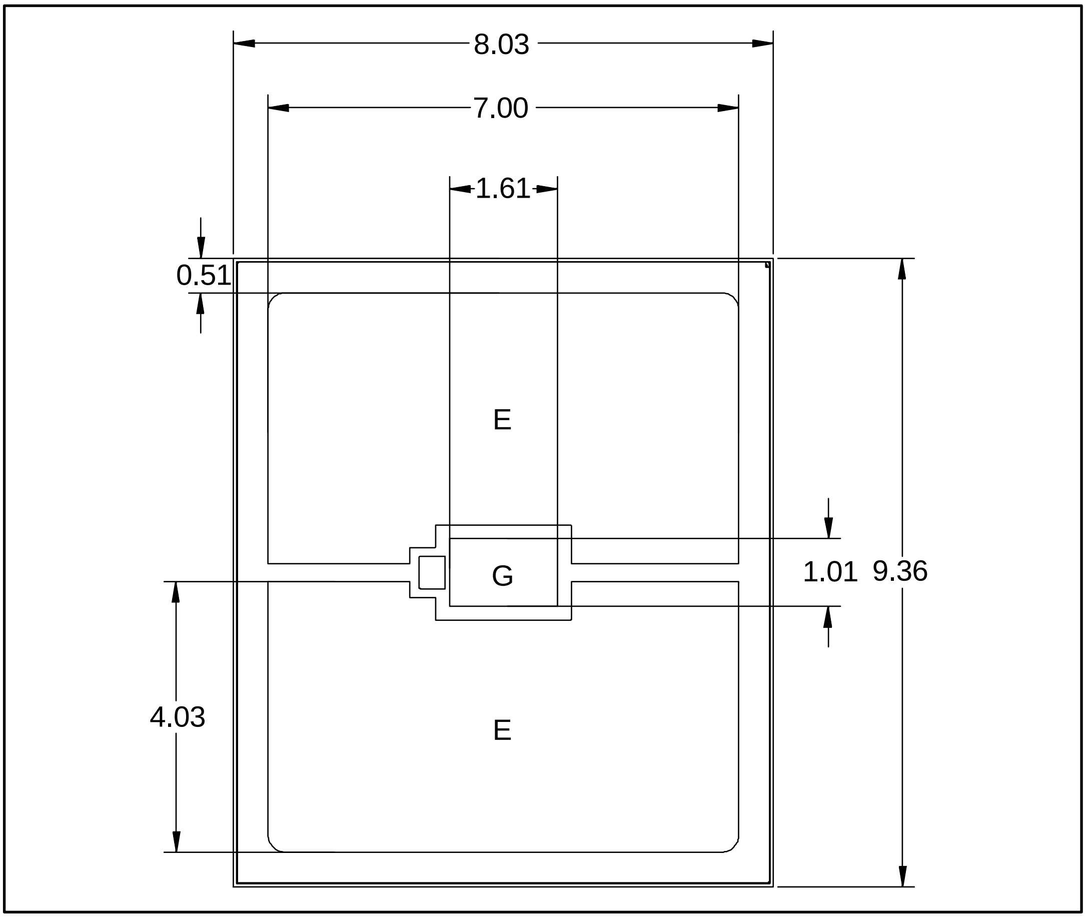
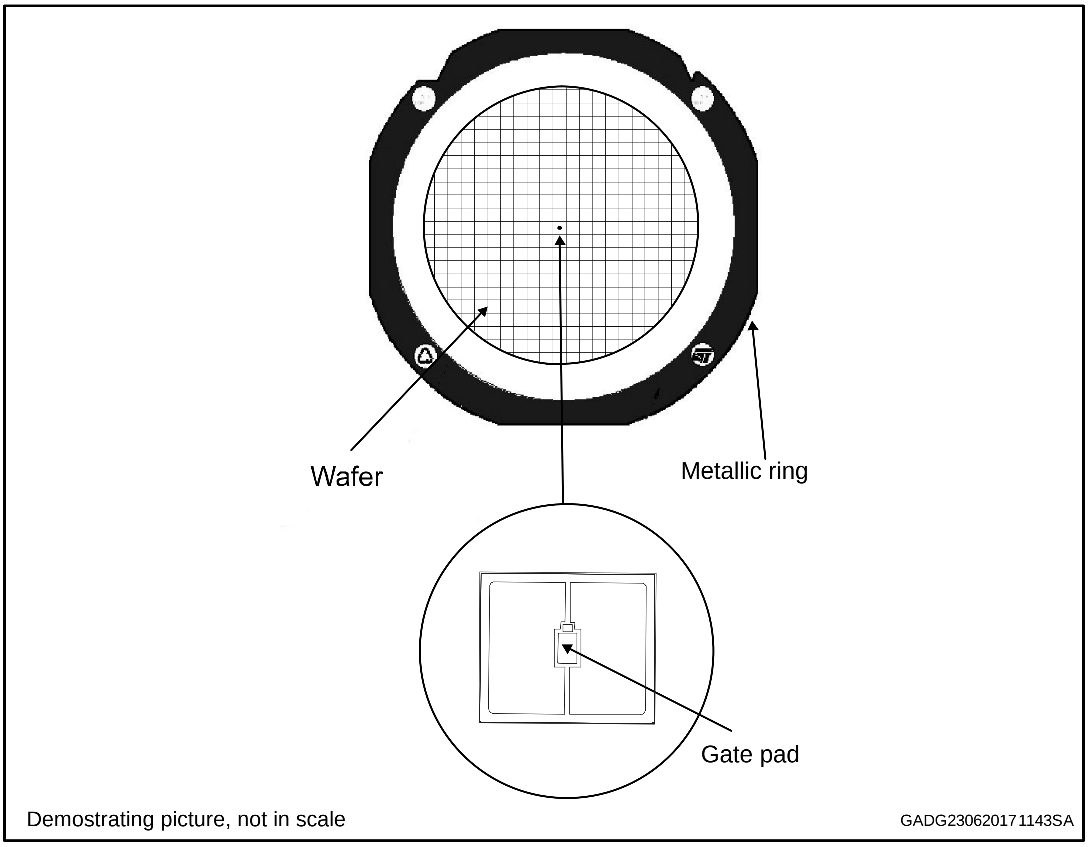


Table 7: Die delivery

Package option	Test condition	Details
D7	Wafer (8 inches) tested, inked, cut on sticky foil on 10.8" (276 mm) ring (see *Figure 3: "D7 drawing and die orientation"*)	Wafer (8 inches) is held by ring protected by two carton shells, inside a plastic envelope sealed under vacuum. Maximum number of wafers for each package is 5, weight is about 3.7 Kg.

Figure 2: D7 drawing and die orientation



4 Additional information

4.1 Additional testing and screening

For customers requiring product supplied as known good die (KGD) or requiring specific die level testing (i.e. for dynamic and switching characterization), please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

4.2 Shipping

Several shipping options are offered, consult the local ST sales office for availability:

- Die on film sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8

4.3 Handling

- Products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Products must be handled only in a class 1000 or better-designated clean room environment.
- Singular die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

4.4 Wafer/die storage

Once the packaging is opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen.

Optimum temperature for storage is 18 °C ±2 °C with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by customer.

After the customer opens the package, the customer is responsible for the products.

5 Revision history

Table 8: Document revision history

Date	Revision	Changes
23-Jun-2017	1	Initial release

IMPORTANT NOTICE – PLEASE READ CAREFULLY