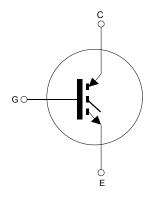


Trench gate field-stop 1200 V, 40 A low loss M series IGBT die in D7 packing



Features

- Low $V_{CE(sat)} = 1.85 \text{ V (typ.)} @ I_C = 40 \text{ A}$
- 10 µs of short-circuit withstand time
- · Minimized tail current
- · Tight parameter distribution
- Positive V_{CE(sat)} temperature coefficient

Applications

- · Industrial motor control
- Motor drives

EGCD

- · Power supplies and converters
- Solar inverters (string and central)

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where the low-loss and the short-circuit functionality is essential. Furthermore, the positive $V_{\text{CE(sat)}}$ temperature coefficient and the tight parameter distribution result in safer paralleling operation.



Product status link

STG40M120F3D7

Product summary			
Order code	STG40M120F3D7		
V _{CE}	1200 V		
I _{CN}	40 A		
Die size	6.11 x 6.80 mm		
Packing	D7		



1 Mechanical parameters

Table 1. Mechanical parameters

Symbol		Value	Unit		
Die size including scribe	e line	6.11 x 6.80	mm		
Wafer size	Wafer size		mm		
Maximum possible dice pe	er wafer	644	dice		
Die thickness		110	μm		
Front side passivation	Front side passivation				
Emitter pad size	Emitter pad size		See Die drawing (dimensions are in mm)		
Gate pad size	Gate pad size		mm		
Front side metallization	composition	AlCu			
Front side metaliization	thickness	4.5	μm		
Back side metallization	composition	Al/Ti/NiV/Ag			
Back side metallization	thickness	0.65	μm		
Die bond	Die bond		or soft solder		
Recommended wire bonding		≤500	μm		

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2 Electrical ratings

 T_J = 25 °C unless otherwise specified.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CES}	Collector-emitter voltage (V _{GE} = 0 V)	1200	V
V _{GE}	Gate-emitter voltage	±20	V
I _{CN} ⁽¹⁾	Continuous collector current at T = 100 °C	40	Α
I _{CP} ⁽¹⁾⁽²⁾	Pulsed collector current	120	Α
t _{SC} (3)	Short circuit withstand time (V_{CC} = 600 V, V_{GE} = 15 V, V_{CE} (peak) ≤ 1200 V, T_{Jstart} ≤ 150 °C)	10	μs
TJ	Operating junction temperature range	-55 to 175	°C

Nominal collector current for die packaged in ST discrete solution. Current level depends on the assembly thermal properties and is limited by maximum junction temperature.

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^{2.} Pulse width is limited by maximum junction temperature. Specified by design, not tested in production.

^{3.} Evaluated by characterization, not tested in production.



3 Electrical characteristics

Table 3. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Parameter Test conditions		Тур.	Max.	Unit
V _{(BR)CES}	Collector-emitter breakdown voltage	I _C = 1 mA, V _{GE} = 0 V	1200			V
V _{CE(sat)}	Collector-emitter saturation voltage	V _{GE} = 15 V, I _C = 15 A			1.8	V
V _{GE(th)}	Gate threshold voltage	$V_{CE} = V_{GE}$, $I_C = 2 \text{ mA}$	5	6	7	V
I _{CES}	Collector cut-off current	V _{GE} = 0 V, V _{CE} = 1200 V			25	μA
I _{GES}	Gate-emitter leakage current	V _{CE} = 0 V, V _{GE} = ±20 V			±250	nA

Table 4. Electrical characteristics (specified by design and evaluated by characterization, not tested at chip level)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
	V _{CE(sat)} Collector-emitter saturation voltage	V _{GE} = 15 V, I _C = 40 A	-	1.85	2.30	V
V _{CE(sat)}		$V_{GE} = 15 \text{ V}, I_{C} = 40 \text{ A},$ $T_{J} = 175 ^{\circ}\text{C}$	-	2.3		V
C _{ies}	Input capacitance	\/ - 25 \/ f = 4 MH=	-	2500		pF
C _{oes}	Output capacitance	$V_{CE} = 25 \text{ V, f} = 1 \text{ MHz,}$ $V_{GF} = 0 \text{ V}$	-	275		pF
C _{res}	Reverse transfer capacitance	VGE - 0 V		95		pF
Qg	Total gate charge	V _{CC} = 960 V, I _C = 40 A, V _{GF} = 0 to 15 V	-	125		nC
Q_{ge}	Gate-emitter charge		-	15		nC
Q_{gc}	Gate-collector charge	VGE 0 to 10 V		75		nC

Table 5. Switching characteristics on inductive load (specified by design and evaluated by characterization, not tested at chip level)

Symbol	Parameter	Parameter Test conditions				Unit
t _{d(on)}	Turn-on delay time		-	35	-	ns
t _r	Current rise time	V = 600 V I = 40 A	-	15	-	ns
t _{d(off)}	Turn-off-delay time	V_{CC} = 600 V, I_{C} = 40 A, V_{GF} = ±15 V, R_{G} = 10 Ω	-	140	-	ns
t _f	Current fall time	VGE - 110 V, NG - 10 12	-	135	-	ns
E _{off} (1)	Turn-off switching energy		_	2.25	-	mJ
t _{d(on)}	Turn-on delay time		-	35	-	ns
t _r	Current rise time	V _{CC} = 600 V, I _C = 40 A,	-	18	-	ns
t _{d(off)}	Turn-off-delay time	V_{GE} = ±15 V, R_{G} = 10 Ω ,	-	150	-	ns
t _f	Current fall time	T _J = 175 °C	-	240	-	ns
E _{off} (1)	Turn-off switching energy		-	3.45	-	mJ

^{1.} Including the tail of the collector current.

Note: The aforementioned values are not tested at chip level and are strongly dependent on the package/module design and the mounting technology.

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4 Die layout

0.5126 0.5126

Figure 1. Die drawing (dimensions are in mm)

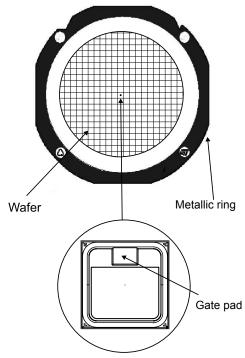
Table 6. Die delivery

Package option	Description	Details
D7	Wafer tested, inked, cut on sticky foil on 10.8" (276 mm) ring (see Figure 2. D7 drawing and die orientation)	Wafer is held by ring protected by two carton shells, inside a plastic envelope sealed under vacuum. Maximum number of wafers for each package is 5, weight is about 3.7 Kg.

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Figure 2. D7 drawing and die orientation



Demonstrating picture, not in scale

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5 Additional information

5.1 Additional testing and screening

For customers requiring product supplied as known good die (KGD) or requiring specific die level testing (that is for dynamic and switching characterization), please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

5.2 Shipping

Several shipping options are offered. Consult the local ST sales office for availability:

- Die on film-sticky foil suffix on sales type D7
- Carrier tape suffix on sales type D8

5.3 Handling

- Products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Products must be handled only in a class 1000 or better-designated clean room environment.
- Singular die is not to be handled with tweezers. A vacuum wand with a nonmetallic ESD protected tip should be used.

5.4 Wafer/die storage

Once the packaging is opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen. Optimum temperature for storage is 18 $^{\circ}$ C ± 2 $^{\circ}$ C with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by the customer. After the customer opens the package, the customer is responsible for the products.

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Revision history

Table 7. Document revision history

Date	Revision	Changes
23-Apr-2015	1	Initial release.
20-Sep-2017	2	Modified title, features and description. Modified Table 2: "Mechanical parameters", Table 3: "Absolute maximum ratings (T _J = 25 °C unless otherwise specified)", Table 4: "Static characteristics (tested on wafer unless otherwise specified)", Table 5: "Electrical characteristics (not tested at chip level, verified by design/characterization)" and Table 6: "Switching characteristics on inductive load (not tested at chip level, verified by design/characterization)". Modified Figure 1: "Die drawing (dimensions are in mm)" and Figure 2: "D7 drawing and die orientation". Minor text changes.
21-Feb-2022	3	Updated title and Device summary on cover page. Updated Section 1 Mechanical parameters. Updated Figure 1. Die drawing (dimensions are in mm) and Figure 2. D7 drawing and die orientation. Minor text changes.

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