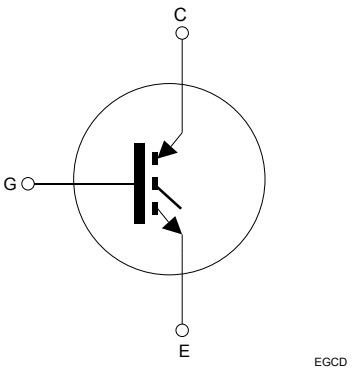
STG40M120F3D7

Datasheet

Trench gate field-stop 1200 V, 40 A low loss M series IGBT die in D7 packing



Features

- Low $V_{CE(sat)}$ = 1.85 V (typ.) @ I_C = 40 A
- 10 µs of short-circuit withstand time
- Minimized tail current
- Tight parameter distribution
- Positive $V_{CE(sat)}$ temperature coefficient

Applications

- Industrial motor control
- Motor drives
- Power supplies and converters
- Solar inverters (string and central)

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where the low-loss and the short-circuit functionality is essential. Furthermore, the positive $V_{CE(sat)}$ temperature coefficient and the tight parameter distribution result in safer paralleling operation.

Product status link
STG40M120F3D7

Product summary	
Order code	STG40M120F3D7
V_{CE}	1200 V
I_{CN}	40 A
Die size	6.11 x 6.80 mm
Packing	D7

1 Mechanical parameters

Table 1. Mechanical parameters

Symbol		Value	Unit
Die size including scribe line		6.11 x 6.80	mm
Wafer size		200	mm
Maximum possible dice per wafer		644	dice
Die thickness		110	µm
Front side passivation		Silicon nitride	
Emitter pad size		See Die drawing (dimensions are in mm)	
Gate pad size		0.819 x 1.200	mm
Front side metallization	composition	AlCu	
	thickness	4.5	µm
Back side metallization	composition	Al/Ti/NiV/Ag	
	thickness	0.65	µm
Die bond		Electrically conductive glue or soft solder	
Recommended wire bonding		≤500	µm

2 Electrical ratings

T_J = 25 °C unless otherwise specified.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)	1200	V
V_{GE}	Gate-emitter voltage	±20	V
I_{CN}(1)	Continuous collector current at T = 100 °C	40	A
I_{CP}(1)(2)	Pulsed collector current	120	A
t_{SC}(3)	Short circuit withstand time (V_{CC} = 600 V, V_{GE} = 15 V, V_{CE} (peak) ≤ 1200 V, T_{Jstart} ≤ 150 °C)	10	µs
T_J	Operating junction temperature range	-55 to 175	°C

1. *Nominal collector current for die packaged in ST discrete solution. Current level depends on the assembly thermal properties and is limited by maximum junction temperature.*
2. *Pulse width is limited by maximum junction temperature. Specified by design, not tested in production.*
3. *Evaluated by characterization, not tested in production.*

3 Electrical characteristics

Table 3. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	I_C = 1 mA, V_{GE} = 0 V	1200			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 15 A			1.8	V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 2 mA	5	6	7	V
I_{CES}	Collector cut-off current	V_{GE} = 0 V, V_{CE} = 1200 V			25	µA
I_{GES}	Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = ±20 V			±250	nA

Table 4. Electrical characteristics (specified by design and evaluated by characterization, not tested at chip level)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 40 A	-	1.85	2.30	V
		V_{GE} = 15 V, I_C = 40 A, T_J = 175 °C	-	2.3		V
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0 V	-	2500		pF
C_{oes}	Output capacitance		-	275		pF
C_{res}	Reverse transfer capacitance		-	95		pF
Q_g	Total gate charge	V_{CC} = 960 V, I_C = 40 A, V_{GE} = 0 to 15 V	-	125		nC
Q_{ge}	Gate-emitter charge		-	15		nC
Q_{gc}	Gate-collector charge		-	75		nC

Table 5. Switching characteristics on inductive load (specified by design and evaluated by characterization, not tested at chip level)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600 V, I_C = 40 A, V_{GE} = ±15 V, R_G = 10 Ω	-	35	-	ns
t_r	Current rise time		-	15	-	ns
$t_{d(off)}$	Turn-off-delay time		-	140	-	ns
t_f	Current fall time		-	135	-	ns
E_{off} (1)	Turn-off switching energy		-	2.25	-	mJ
$t_{d(on)}$	Turn-on delay time	V_{CC} = 600 V, I_C = 40 A, V_{GE} = ±15 V, R_G = 10 Ω, T_J = 175 °C	-	35	-	ns
t_r	Current rise time		-	18	-	ns
$t_{d(off)}$	Turn-off-delay time		-	150	-	ns
t_f	Current fall time		-	240	-	ns
E_{off} (1)	Turn-off switching energy		-	3.45	-	mJ

1. *Including the tail of the collector current.*

Note: The aforementioned values are not tested at chip level and are strongly dependent on the package/module design and the mounting technology.

4 Die layout

Figure 1. **Die drawing (dimensions are in mm)**

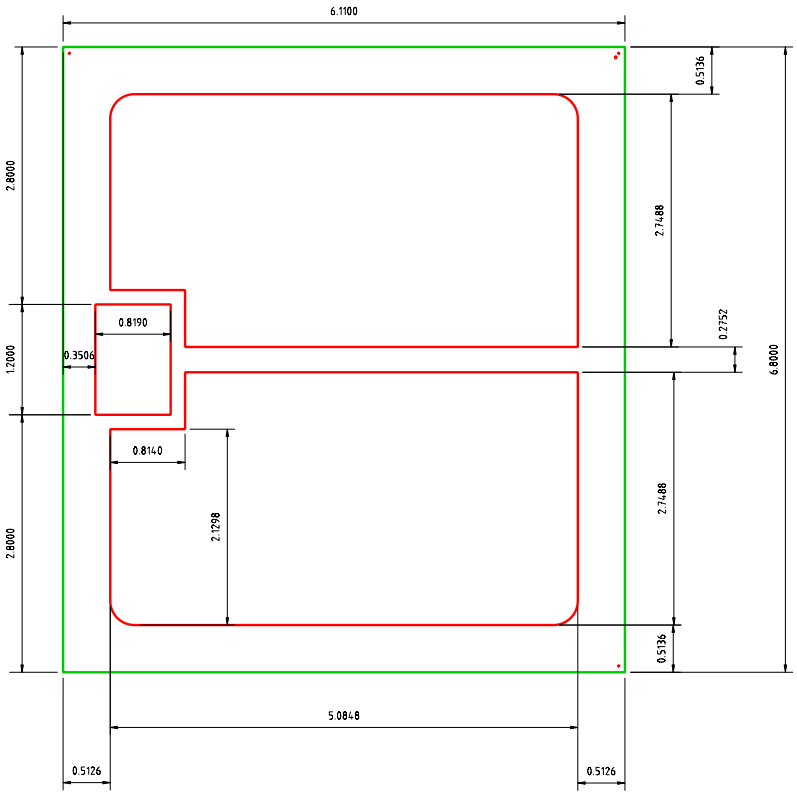
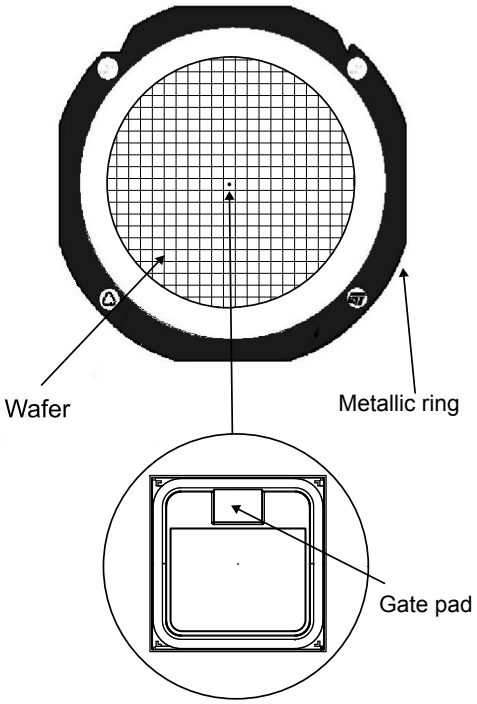


Table 6. **Die delivery**

Package option	Description	Details
D7	Wafer tested, inked, cut on sticky foil on 10.8" (276 mm) ring (see Figure 2. D7 drawing and die orientation)	Wafer is held by ring protected by two carton shells, inside a plastic envelope sealed under vacuum. Maximum number of wafers for each package is 5, weight is about 3.7 Kg.

Figure 2. D7 drawing and die orientation



Demonstrating picture, not in scale

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5 Additional information

5.1 Additional testing and screening

For customers requiring product supplied as known good die (KGD) or requiring specific die level testing (that is for dynamic and switching characterization), please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

5.2 Shipping

Several shipping options are offered. Consult the local ST sales office for availability:

- Die on film-sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8

5.3 Handling

- Products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Products must be handled only in a class 1000 or better-designated clean room environment.
- Singular die is not to be handled with tweezers. A vacuum wand with a nonmetallic ESD protected tip should be used.

5.4 Wafer/die storage

Once the packaging is opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen.

Optimum temperature for storage is 18 °C ±2 °C with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by the customer.

After the customer opens the package, the customer is responsible for the products.

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
23-Apr-2015	1	Initial release.
20-Sep-2017	2	Modified title, features and description. Modified *Table 2: "Mechanical parameters"*, *Table 3: "Absolute maximum ratings (T_J = 25 °C unless otherwise specified)"*, *Table 4: "Static characteristics (tested on wafer unless otherwise specified)"*, *Table 5: "Electrical characteristics (not tested at chip level, verified by design/characterization)"* and *Table 6: "Switching characteristics on inductive load (not tested at chip level, verified by design/characterization)"*. Modified *Figure 1: "Die drawing (dimensions are in mm)"* and *Figure 2: "D7 drawing and die orientation"*. Minor text changes.
21-Feb-2022	3	Updated title and Device summary on cover page. Updated Section 1 Mechanical parameters. Updated Figure 1. Die drawing (dimensions are in mm) and Figure 2. D7 drawing and die orientation. Minor text changes.

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