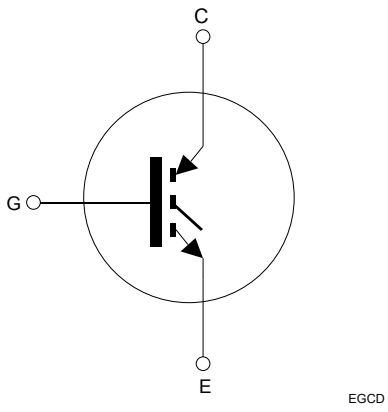
650 V, 20 A trench gate field-stop M series low-loss IGBT die in D7 packing



Features

- 6 µs of short-circuit withstand time
- Low $V_{CE(sat)}$ = 1.55 V (typ.) @ I_C = 20 A
- Positive $V_{CE(sat)}$ temperature coefficient
- Tight parameter distribution
- Maximum junction temperature: T_J = 175 °C

Applications

- Motor control
- UPS
- Solar
- General-purpose inverter

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the M series IGBTs, which represent an optimal balance between inverter system performance and efficiency where the low-loss and the short-circuit functionality is essential. Furthermore, the positive $V_{CE(sat)}$ temperature coefficient and the tight parameter distribution result in safer paralleling operation.

Product status link
STG20M65F2D7

Product summary	
Order code	STG20M65F2D7
V_{CE}	650 V
I_{CN}	20 A
Die size	3.60 x 3.32 mm²
Packing	D7

1 Mechanical parameters

Table 1. Mechanical parameters

Symbol		Value	Unit
Die size including scribe line		3.60 x 3.32	mm²
Wafer size		200	mm
Maximum possible dice per wafer		2226	dice
Die thickness		70	µm
Front side passivation		Silicone nitride	
Emitter pad size including gate pad		2.92 x 2.65	mm²
Gate pad size		0.41 x 0.45	mm²
Front side metallization	composition	AlCu	
	thickness	4.5	µm
Back side metallization	composition	Al/Ti/NiV/Ag	
	thickness	0.65	µm
Die bond		Electrically conductive glue or soft solder	
Recommended wire bonding		≤500	µm

2 Electrical ratings

2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings (T_J = 25 °C unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{CES}	Collector-emitter voltage (V_{GE} = 0 V)		650	V
V_{GE}	Gate-emitter voltage		±20	V
I_{CN} (1)	Continuous collector current at T = 100 °C		20	A
I_{CP} (2) (1)	Pulsed collector current		60	A
t_{SC} (3)	Short -circuit withstand time	V_{CC} = 400 V, V_{GE} = 13 V, $V_{CE(peak)}$ ≤ 650 V, T_{Jstart} ≤ 150 °C	10	µs
		V_{CC} = 400 V, V_{GE} = 15 V, $V_{CE(peak)}$ ≤ 650 V, T_{Jstart} ≤ 150 °C	6	µs
T_J	Operating junction temperature range		-55 to 175	°C

1. *Nominal collector current for die packaged in ST discrete solution. Current level depends on the assembly thermal properties and is limited by maximum junction temperature.*
2. *Pulse width is limited by maximum junction temperature.*
3. *Defined by design, not subject to production test.*

2.2 Electrical characteristics

Table 3. Static characteristics (tested on wafer unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	I_C = 250 µA, V_{GE} = 0 V	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 15 A			2.1	V
$V_{GE(th)}$	Gate threshold voltage	V_{CE} = V_{GE}, I_C = 500 µA	5	6	7	V
I_{CES}	Collector cut-off current	V_{GE} = 0 V, V_{CE} = 650 V			25	µA
I_{GES}	Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = ±20 V			±250	nA

Table 4. Electrical characteristics (not tested at chip level, verified by design/characterization)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CE(sat)}$	Collector-emitter saturation voltage	V_{GE} = 15 V, I_C = 20 A	-	1.55	2.0	V
		V_{GE} = 15 V, I_C = 20 A, T_J = 175 °C	-	2.1		V
C_{ies}	Input capacitance	V_{CE} = 25 V, f = 1 MHz, V_{GE} = 0 V	-	1688		pF
C_{oes}	Output capacitance		-	95		pF
C_{res}	Reverse transfer capacitance		-	35		pF
Q_g	Total gate charge	V_{CC} = 520 V, I_C = 20 A, V_{GE} = 15 V	-	63		nC

Table 5. Switching characteristics on inductive load

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{CC} = 400 V, I_C = 20 A, V_{GE} = 15 V, R_G = 12 Ω	-	26	-	ns
t_r	Current rise time		-	10.8	-	ns
$t_{d(off)}$	Turn-off-delay time		-	108	-	ns
t_f	Current fall time		-	65	-	ns
E_{off} (1)	Turn-off switching energy		-	0.56	-	mJ
$t_{d(on)}$	Turn-on delay time	V_{CC} = 400 V, I_C = 20 A, V_{GE} = 15 V, R_G = 12 Ω, T_J = 175 °C	-	28.4	-	ns
t_r	Current rise time		-	11.2	-	ns
$t_{d(off)}$	Turn-off-delay time		-	107	-	ns
t_f	Current fall time		-	145	-	ns
E_{off} (1)	Turn-off switching energy		-	0.85	-	mJ

1. *Including the tail of the collector current.*

Note: The aforementioned values are not tested at chip level and are strongly dependent on the package/module design and the mounting technology. Refer to STGWA20M65DF2 datasheet for further information.

3 Die layout

Figure 1. **Die drawing (dimensions are in mm)**

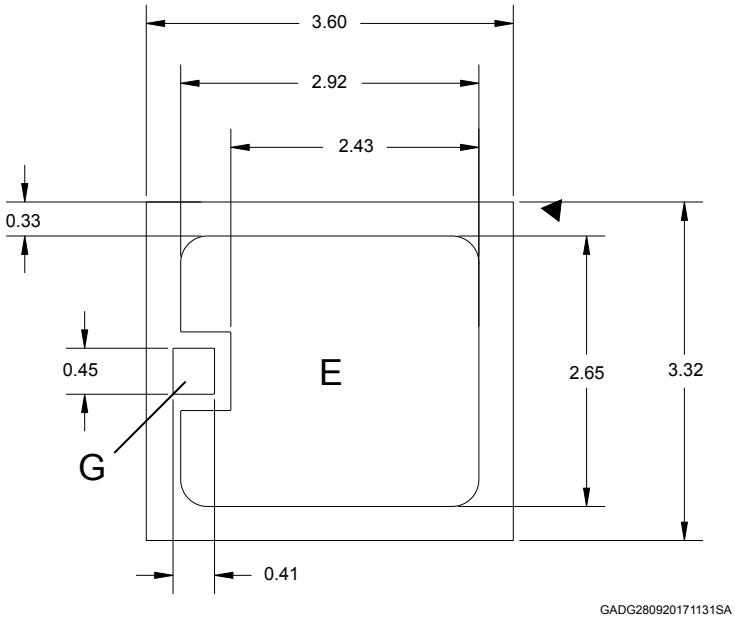
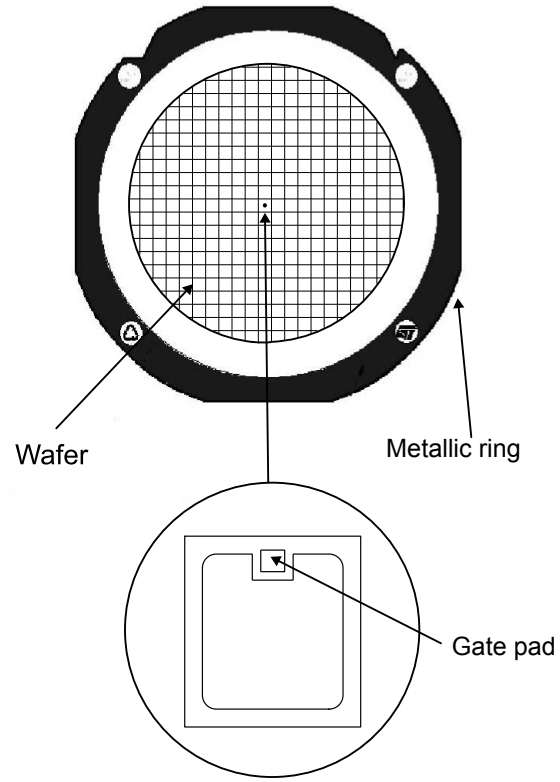


Table 6. **Die delivery**

Package option	Test condition	Details
D7	Wafer (200 mm) tested, inked, cut on sticky foil on 10.8" (276 mm) ring (see Figure 2. D7 drawing and die orientation)	Wafer (200 mm) is held by ring protected by two carton shells, inside a plastic envelope sealed under vacuum. Maximum number of wafers for each package is 5, weight is about 3.7 Kg.

Figure 2. D7 drawing and die orientation



Demonstrating picture, not in scale

GADG280920171130SA

4 Additional information

4.1 Additional testing and screening

For customers requiring product supplied as known good die (KGD) or requiring specific die level testing (i.e. for dynamic and switching characterization), please contact the local ST sales office.

If KGD is requested, the shipping delivery is D8.

4.2 Shipping

Several shipping options are offered, consult the local ST sales office for availability:

- Die on film sticky foil - suffix on sales type D7
- Carrier tape - suffix on sales type D8

4.3 Handling

- Products must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Products must be handled only in a class 1000 or better-designated clean room environment.
- Singular die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

4.4 Wafer/die storage

Once the packaging is opened, the wafer must be stored in a dry, inert atmosphere, such as nitrogen.

Optimum temperature for storage is 18 °C ±2 °C with as few variations as possible to avoid parasitic polymerization of the adhesive. Sawn wafers must be processed within 12 weeks after receipt by customer.

After the customer opens the package, the customer is responsible for the products.

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
10-Oct-2017	1	Initial release.
05-Oct-2018	2	Modified Table 3. Static characteristics (tested on wafer unless otherwise specified) and Table 6. Die delivery. Minor text changes.

Contents

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.