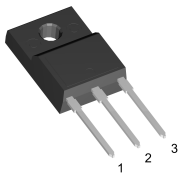
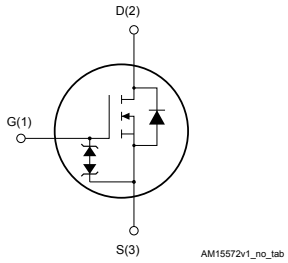
N-channel 1050 V, 0.90 Ω typ., 8 A MDmesh K5 Power MOSFET in a TO-220FP wide creepage package



TO-220FP wide creepage



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STFH12N105K5	1050 V	1.00 Ω	8 A	29 W

- Industry's lowest $R_{DS(on)}$ * area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected
- Wide creepage distance of 4.25 mm between the pins

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status link
STFH12N105K5

Product summary	
Order code	STFH12N105K5
Marking	12N105K5
Package	TO-220FP wide creepage
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current at T_C = 25 °C	8	A
I_D	Drain current at T_C = 100 °C	5	A
I_{DM} (1)	Drain current (pulsed)	15	A
P_{TOT}	Total power dissipation at T_C = 25 °C	29	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2500	V
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 7 A, di/dt ≤ 100 A/µs, $V_{DS(peak)}$ ≤ $V_{(BR)DSS}$, V_{DD} = 525 V.*
3. *V_{DS} ≤ 840 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	4.36	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max)	2.7	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	850	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1050			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1050 V			1	µA
		V_{GS} = 0 V, V_{DS} = 1050 V, Tc=125 °C(1)			50	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 4 A		0.90	1.00	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	559	-	pF
C_{oss}	Output capacitance		-	48	-	pF
C_{rss}	Reverse transfer capacitance		-	0.6	-	pF
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 V to 840 V, V_{GS} = 0 V	-	65	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related		-	22	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 840 V, I_D = 7 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	18.4	-	nC
Q_{gs}	Gate-source charge		-	4.5	-	nC
Q_{gd}	Gate-drain charge		-	11.0	-	nC

1. *Time related is defined as a constant equivalent capacitance giving the same charging time as Coss when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *Energy related is defined as a constant equivalent capacitance giving the same stored energy as Coss when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 525 V, I_D = 3.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 16. Unclamped inductive waveform)	-	13	-	ns
t_r	Rise time		-	9	-	ns
$t_{d(off)}$	Turn-off delay time		-	38	-	ns
t_f	Fall time		-	18	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
I_{SDM}	Source-drain current (pulsed)		-		15	A
V_{SD} (1)	Forward on voltage	I_{SD} = 7 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 7 A, V_{DD} = 60 V	-	537		ns
Q_{rr}	Reverse recovery charge	di/dt = 100 A/µs,	-	6.6		µC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	19.5		A
t_{rr}	Reverse recovery time	I_{SD} = 7 A,V_{DD} = 60 V	-	770		ns
Q_{rr}	Reverse recovery charge	di/dt = 100 A/µs,	-	9.10		µC
I_{RRM}	Reverse recovery current	Tj = 150 °C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	16.8		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5 %.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

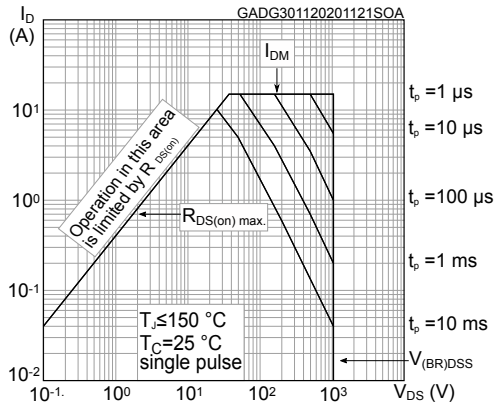


Figure 2. Maximum transient thermal impedance

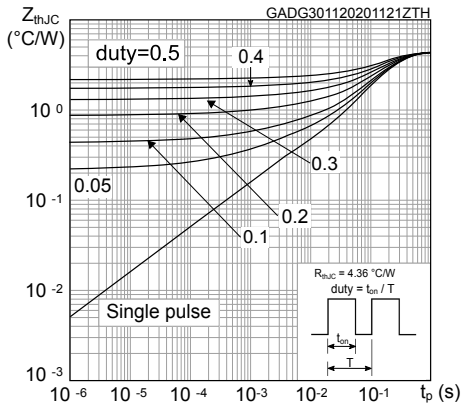


Figure 3. Typical output characteristics

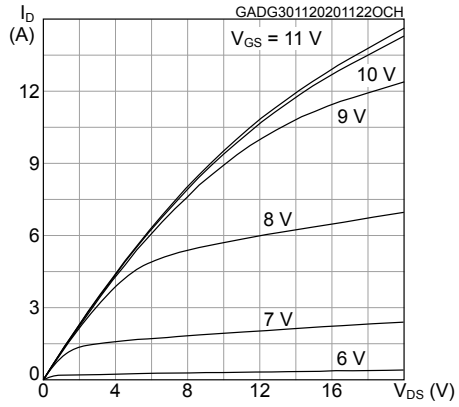


Figure 4. Typical transfer characteris

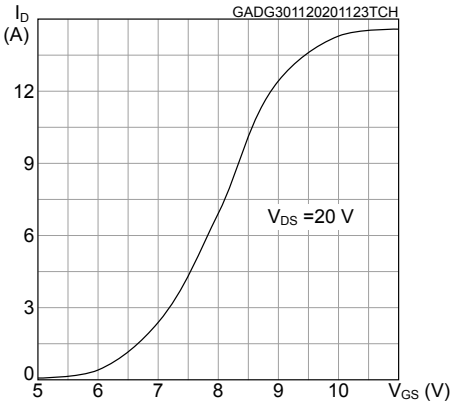


Figure 5. Typical gate charge characteristics

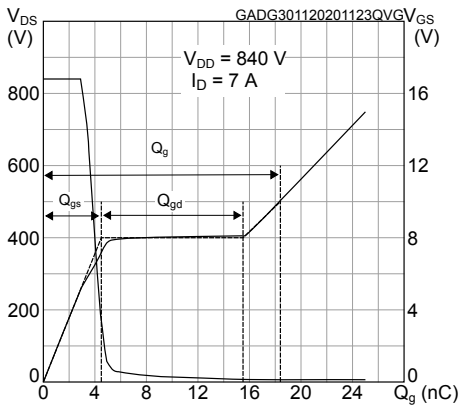


Figure 6. Typical drain-source on-resistance

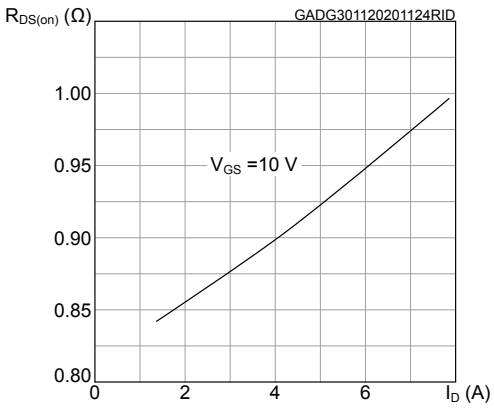


Figure 7. Typical capacitance characteristics

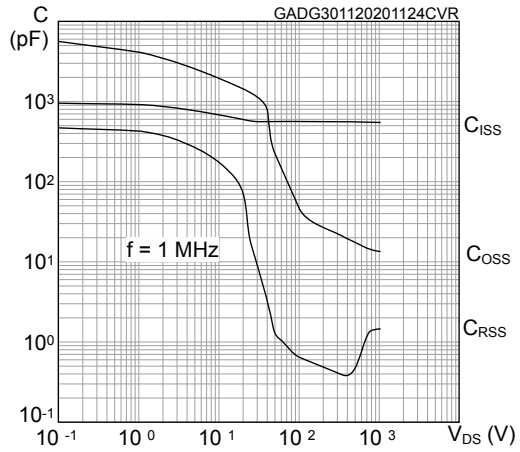


Figure 8. Normalized gate threshold vs temperature

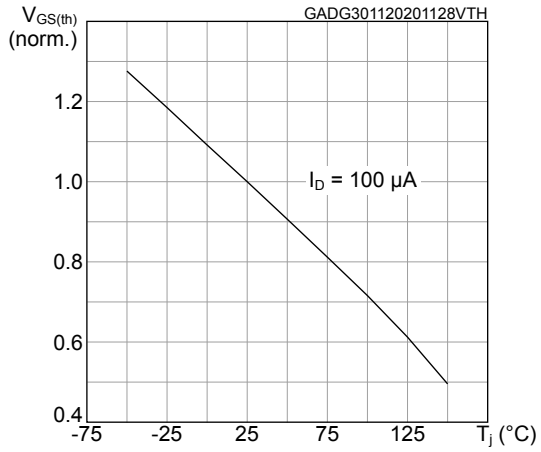


Figure 9. Normalized on-resistance vs temperature

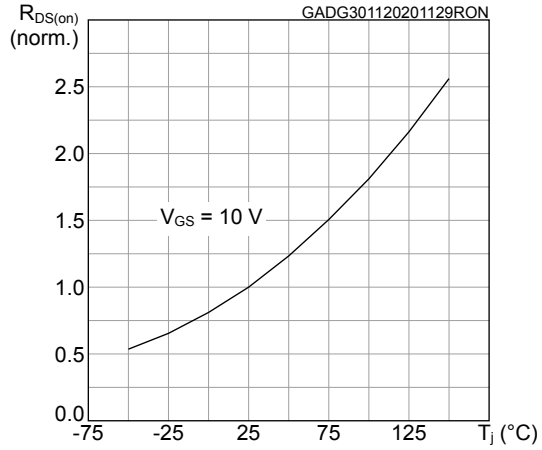


Figure 10. Normalized breakdown voltage vs temperature

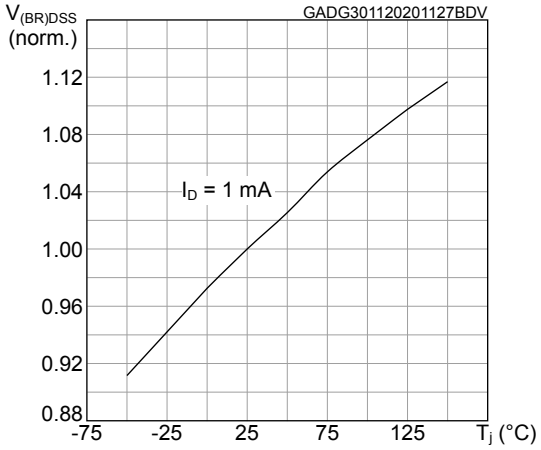
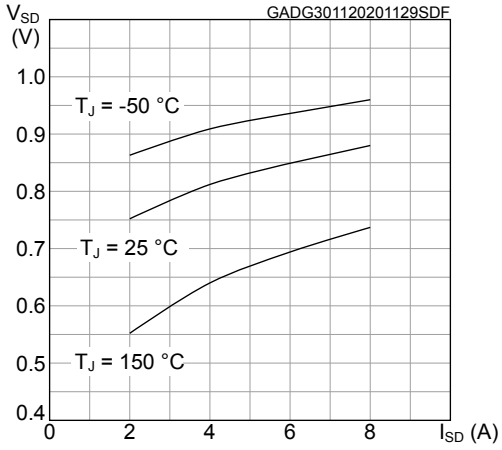


Figure 11. Typical reverse diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

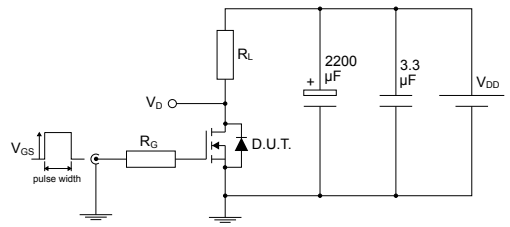


Figure 13. Test circuit for gate charge behavior

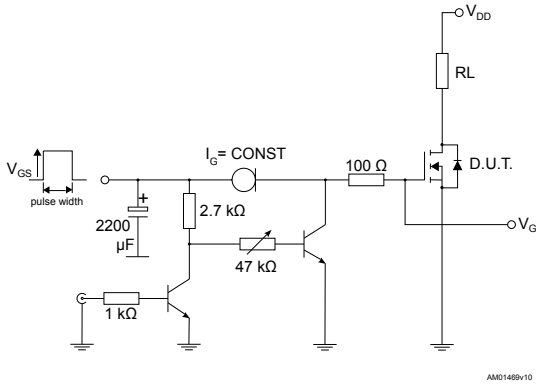


Figure 14. Test circuit for inductive load switching and diode recovery times

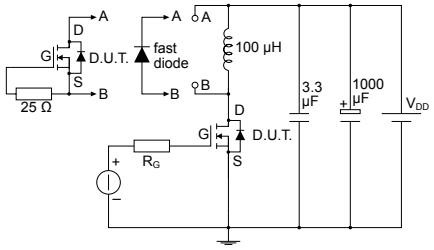


Figure 15. Unclamped inductive load test circuit

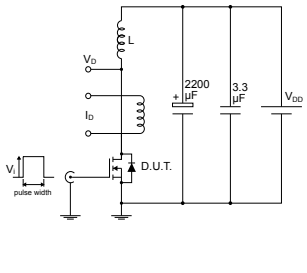


Figure 16. Unclamped inductive waveform

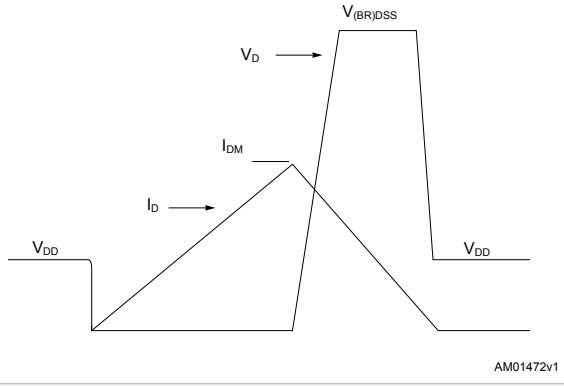
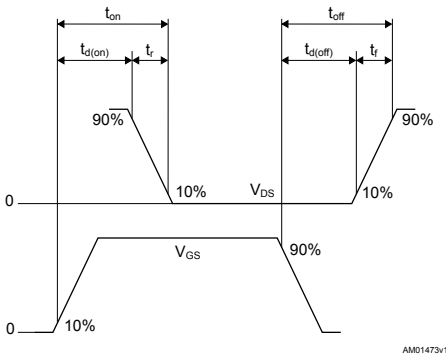


Figure 17. Switching time waveform

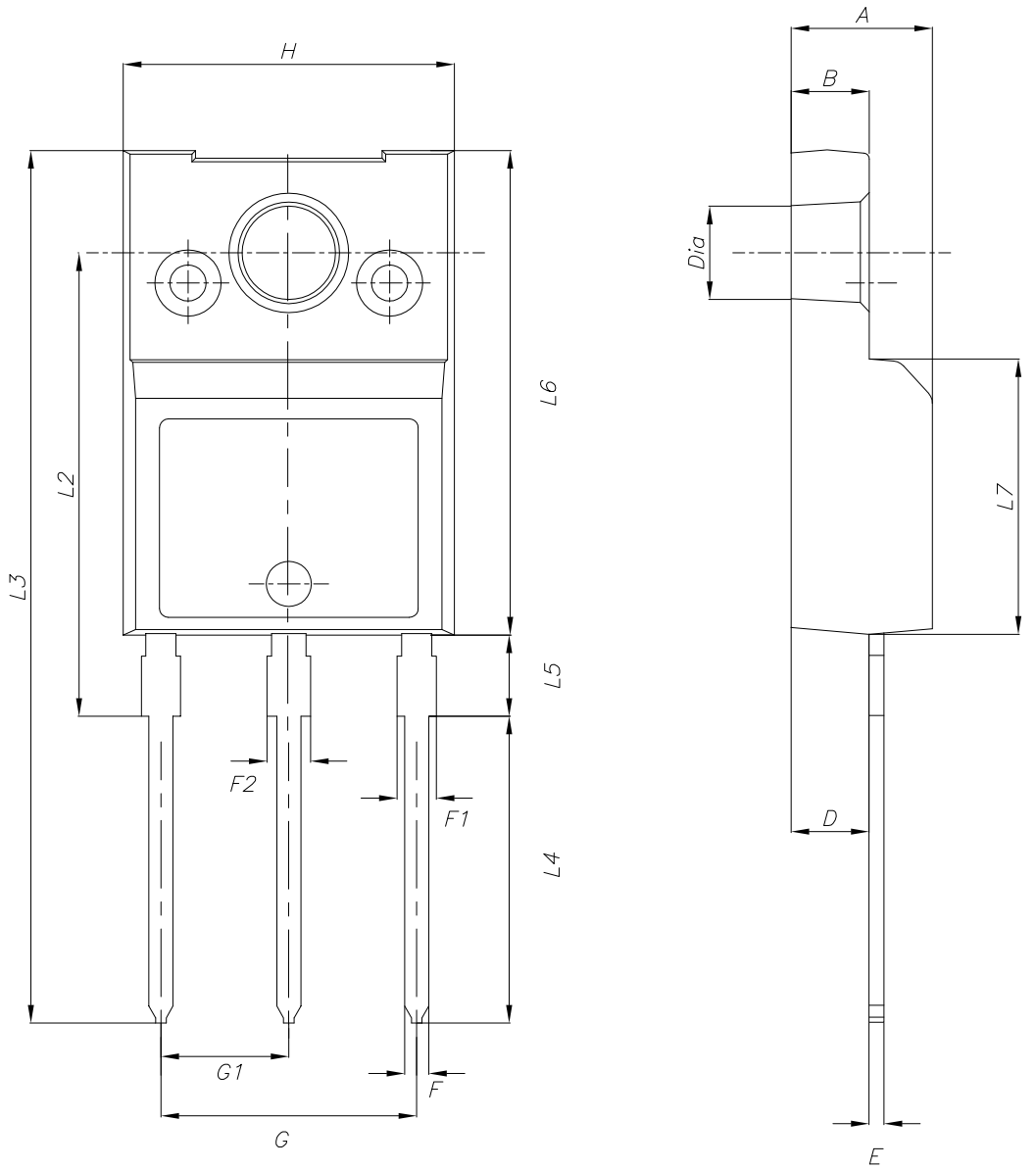


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP wide creepage package information

Figure 18. TO-220FP wide creepage package outline



DM00260252_1

Table 8. **TO-220FP wide creepage package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.60	4.70	4.80
B	2.50	2.60	2.70
D	2.49	2.59	2.69
E	0.46		0.59
F	0.76		0.89
F1	0.96		1.25
F2	1.11		1.40
G	8.40	8.50	8.60
G1	4.15	4.25	4.35
H	10.90	11.00	11.10
L2	15.25	15.40	15.55
L3	28.70	29.00	29.30
L4	10.00	10.20	10.40
L5	2.55	2.70	2.85
L6	16.00	16.10	16.20
L7	9.05	9.15	9.25
Dia	3.00	3.10	3.20

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
04-Dec-2020	1	First release.
10-Dec-2020	2	Updated Table 1. Absolute maximum ratings.