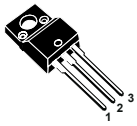
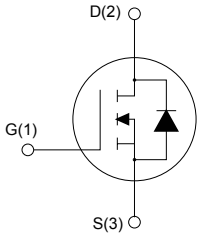
N-channel 250 V, 41 mΩ typ., 45 A STripFET II Power MOSFET in a TO-220FP package



TO-220FP



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Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF75NF25	250 V	50 mΩ	45 A	31 W

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status link
STF75NF25

Product summary	
Order code	STF75NF25
Marking	75NF25
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	250	V
V_{GS}	Gate-source voltage	±25	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	45	A
	Drain current (continuous) at T_C = 100 °C	28	
I_{DM} (2)	Drain current (pulsed)	150	A
P_{TOT}	Total power dissipation at T_C = 25 °C	31	W
dv/dt (3)	Peak diode recovery voltage slope	12	V/ns
dv/dt(4)	MOSFET dv/dt ruggedness	40	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2.5	kV
T_J	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 45 A, di/dt ≤ 400 A/µs, $V_{DS\ (peak)}$ ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*
4. *V_{DS} ≤ 200 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	4	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	29	A
E_{AS}(1)	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	416	mJ

1. *Energy during avalanche per single pulse is defined as the maximum energy that can be dissipated in the device, during a single avalanche operation, at the I_{AR} and initial junction temperature of 25 °C, to bring the junction temperature to the maximum value of 150 °C.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	250			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 250 V			1	µA
		V_{GS} = 0 V, V_{DS} = 250 V, T_C = 125 °C (1)			10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 22.5 A		41	50	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	3084	-	pF
C_{oss}	Output capacitance		-	263	-	pF
C_{rss}	Reverse transfer capacitance		-	44	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 200 V, V_{GS} = 0 V	-	338	-	pF
R_g	Gate input resistance	f = 1 MHz, I_D = 0 A	-	1.7	-	Ω
Q_g	Total gate charge	V_{DD} = 200 V, I_D = 45 A, V_{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)	-	88	-	nC
Q_{gs}	Gate-source charge		-	20	-	nC
Q_{gd}	Gate-drain charge		-	43	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 125 V, I_D = 22.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	23	-	ns
t_r	Rise time		-	35	-	ns
$t_{d(off)}$	Turn-off delay time		-	57	-	ns
t_f	Fall time		-	17	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		45	A
I_{SDM}(1)	Source-drain current (pulsed)		-		150	A
V_{SD}(2)	Forward on voltage	I_{SD} = 45 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 45 A, di/dt = 100 A/µs, V_{DD} = 200 V (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	212		ns
Q_{rr}	Reverse recovery charge		-	2.07		µC
I_{RRM}	Reverse recovery current		-	16.5		A
t_{rr}	Reverse recovery time	I_{SD} = 45 A, di/dt = 100 A/µs, V_{DD} = 200 V, T_J = 150 °C (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	280		ns
Q_{rr}	Reverse recovery charge		-	3.5		µC
I_{RRM}	Reverse recovery current		-	21		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

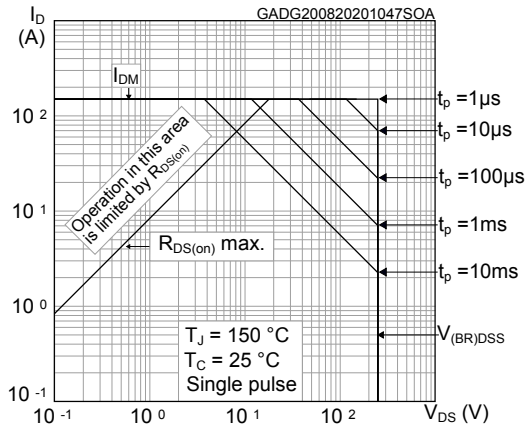


Figure 2. Maximum transient thermal impedance

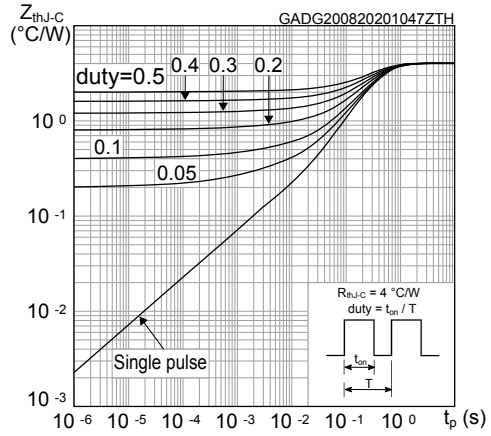


Figure 3. Typical output characteristics

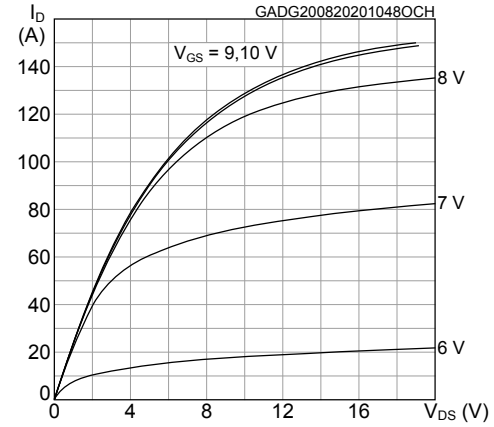


Figure 4. Typical transfer characteristics

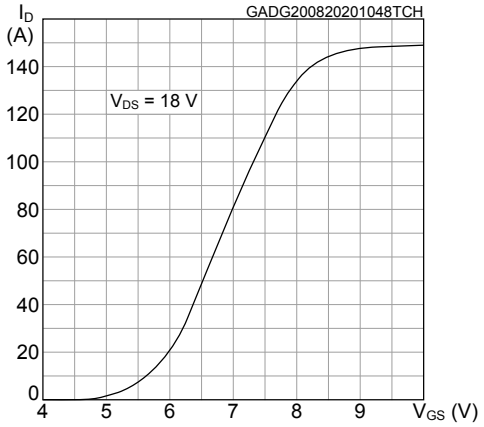


Figure 5. Normalized breakdown voltage vs temperature

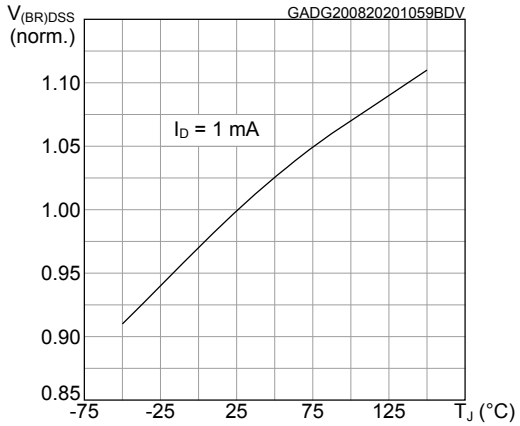


Figure 6. Typical drain-source on-resistance

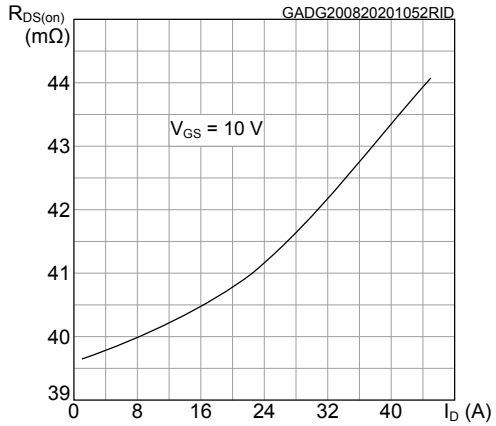


Figure 7. Typical gate charge characteristics

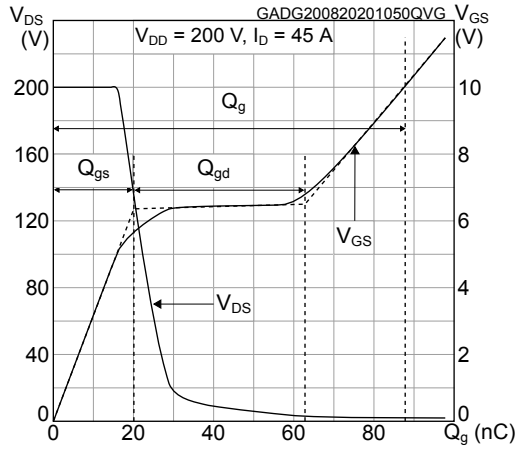


Figure 8. Typical capacitance characteristics

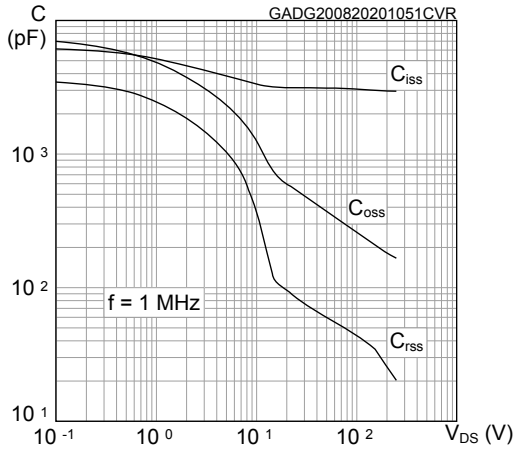


Figure 9. Normalized gate threshold vs temperature

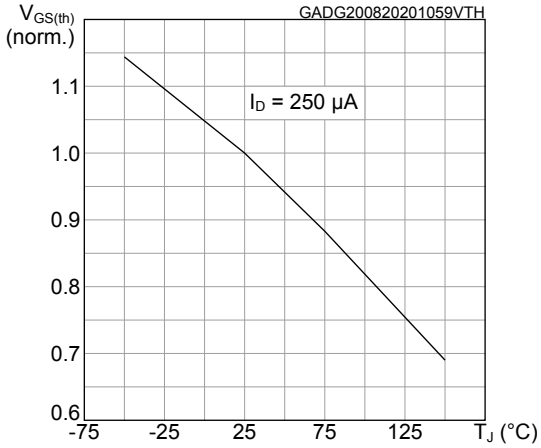


Figure 10. Normalized on-resistance vs temperature

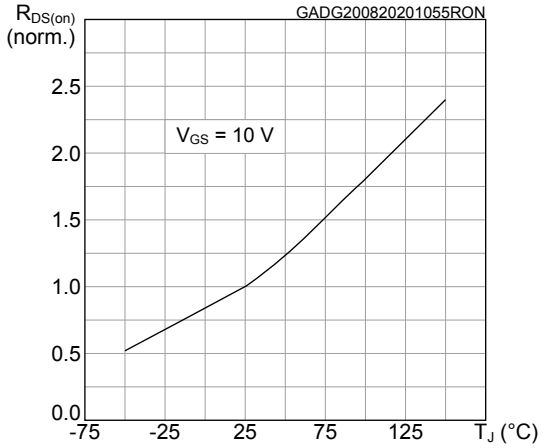


Figure 11. Typical reverse diode forward characteristics

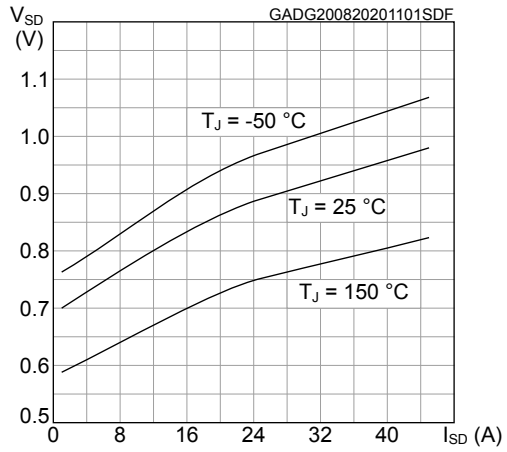
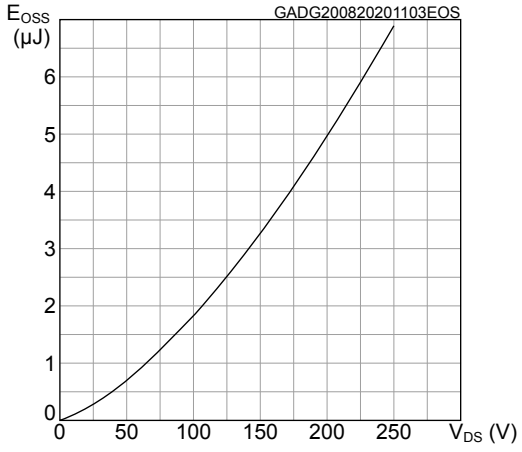


Figure 12. Typical output capacitance stored energy



3 Test circuits

Figure 13. Test circuit for resistive load switching times

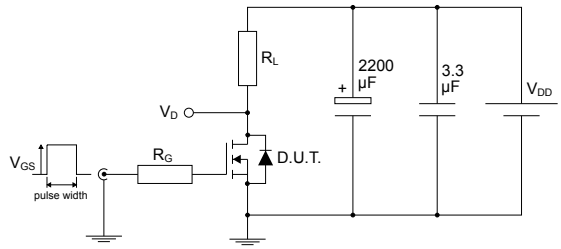


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Figure 14. Test circuit for gate charge behavior

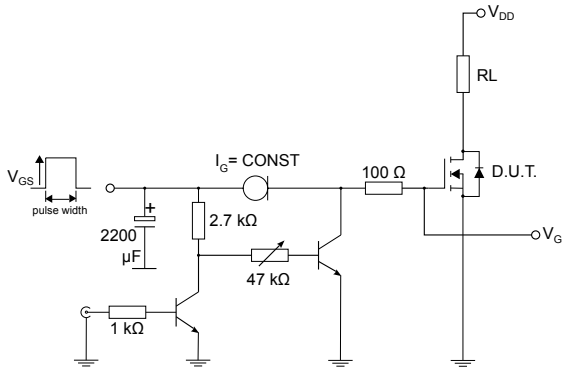

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Figure 15. Test circuit for inductive load switching and diode recovery times

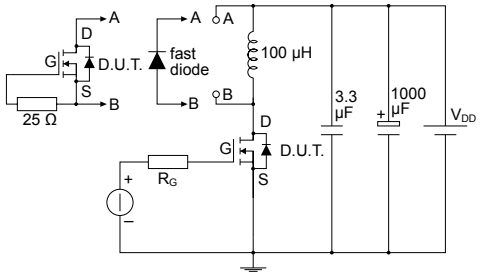

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Figure 16. Unclamped inductive load test circuit

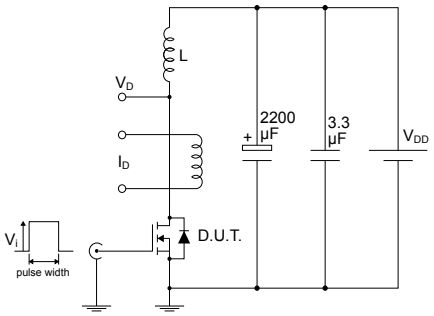

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Figure 17. Unclamped inductive waveform

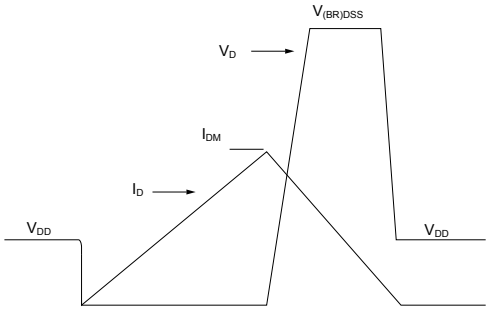

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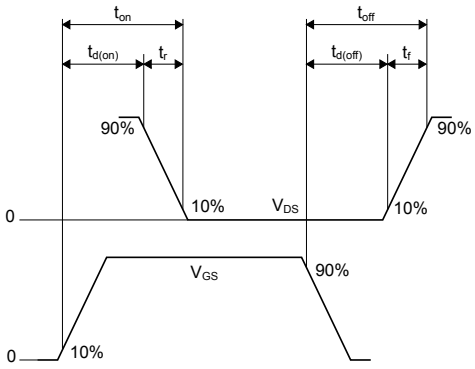
Figure 18. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 19. TO-220FP type B package outline

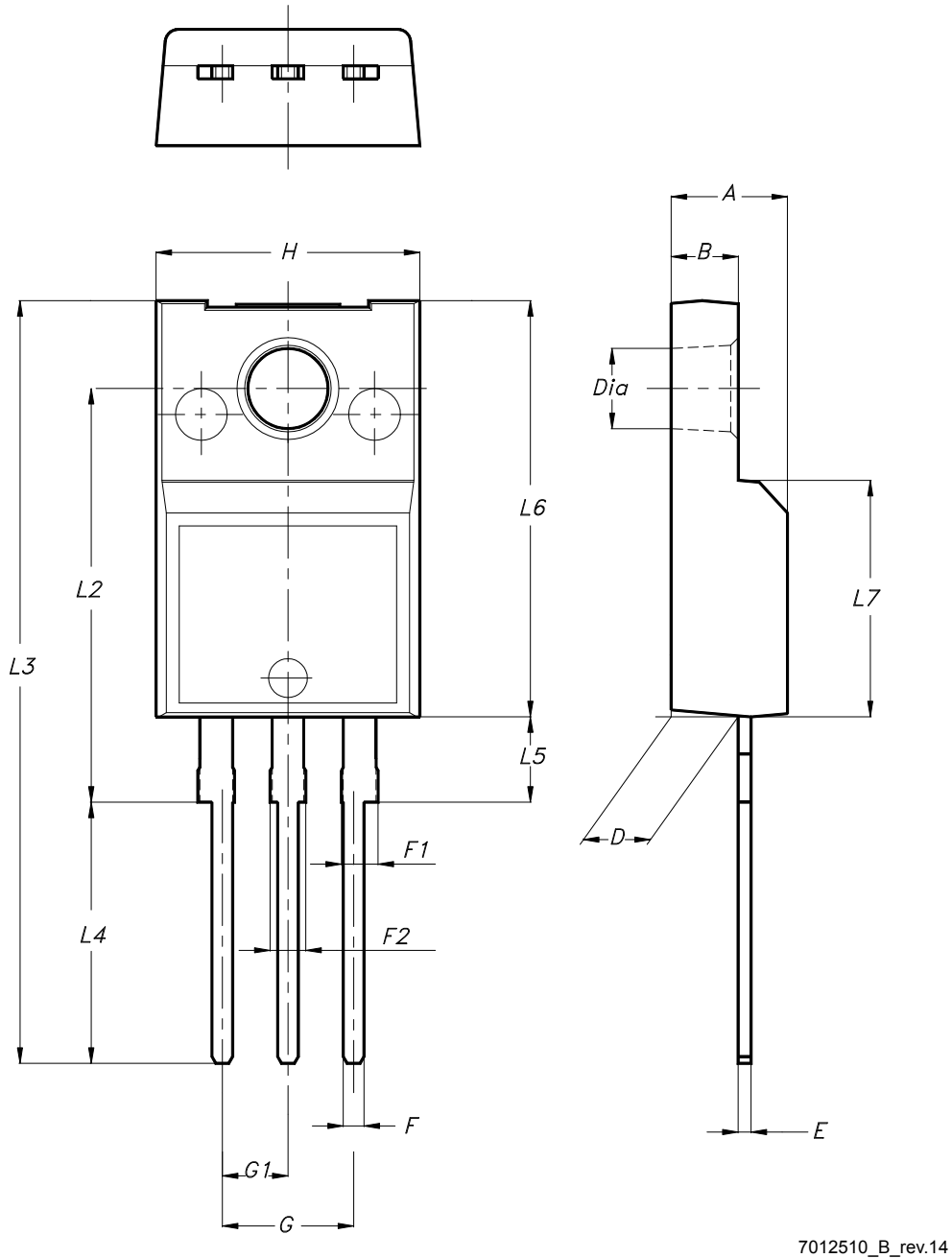

Table 8. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. **Document revision history**

Date	Version	Changes
04-Apr-2019	1	First release.
21-Aug-2020	2	Updated Title and *Features* in cover page. Updated *Section 1 Electrical ratings*. Updated *Section 2 Electrical characteristics*. Added *Section 2.1 Electrical characteristics (curves)*. Updated *Figure 14. Test circuit for gate charge behavior*.
09-Oct-2023	3	Updated Table 2. Thermal data, Table 3. Avalanche characteristics. Updated Figure 1. Safe operating area. Updated Section 4.1 TO-220FP type B package information.

Contents