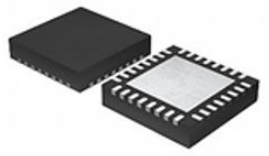
STEF12H60G

Datasheet

60 A electronic fuse for 12 V DC rail



QFN 32 (5 x 5)

Maturity status link
STEF12H60G

Features

- 60 A continuous current
- Input voltage range from 5 to 18 V
- Adjustable overcurrent protection with a 2.6 ms timed circuit breaker
- Input undervoltage lockout
- Integrated 0.85 mΩ power MOSFET
- Enable/disable pin
- Programmable turn-on time
- Accurate current monitor signal
- Precise temperature monitor
- Overcurrent and fault status flags
- Internal MOSFET self-diagnostic
- Parallel operation
- Thermal protection
- Fault management: latch-off or auto-retry versions
- QFN32- 5 x 5 package
- Temperature range: -40°C to 125°C

Applications

- Server main eFuse
- Hot-swap boards
- High power industrial 12 V rail protection

Description

The STEF12H60G is a 60 A integrated electronic fuse optimized for monitoring the output current and the input voltage, over the 12 V DC power lines.

When connected in series to the main power rail, it is able to detect and react to overcurrent conditions.

When an overload condition occurs, the device reacts as a timed circuit breaker, cutting off the output current.

A precise current monitor signal provides continuous information about the load current to the system controller IC.

Similarly, a precise temperature sensor generates a monitor signal that permits the system controller to keep the device power dissipation under control.

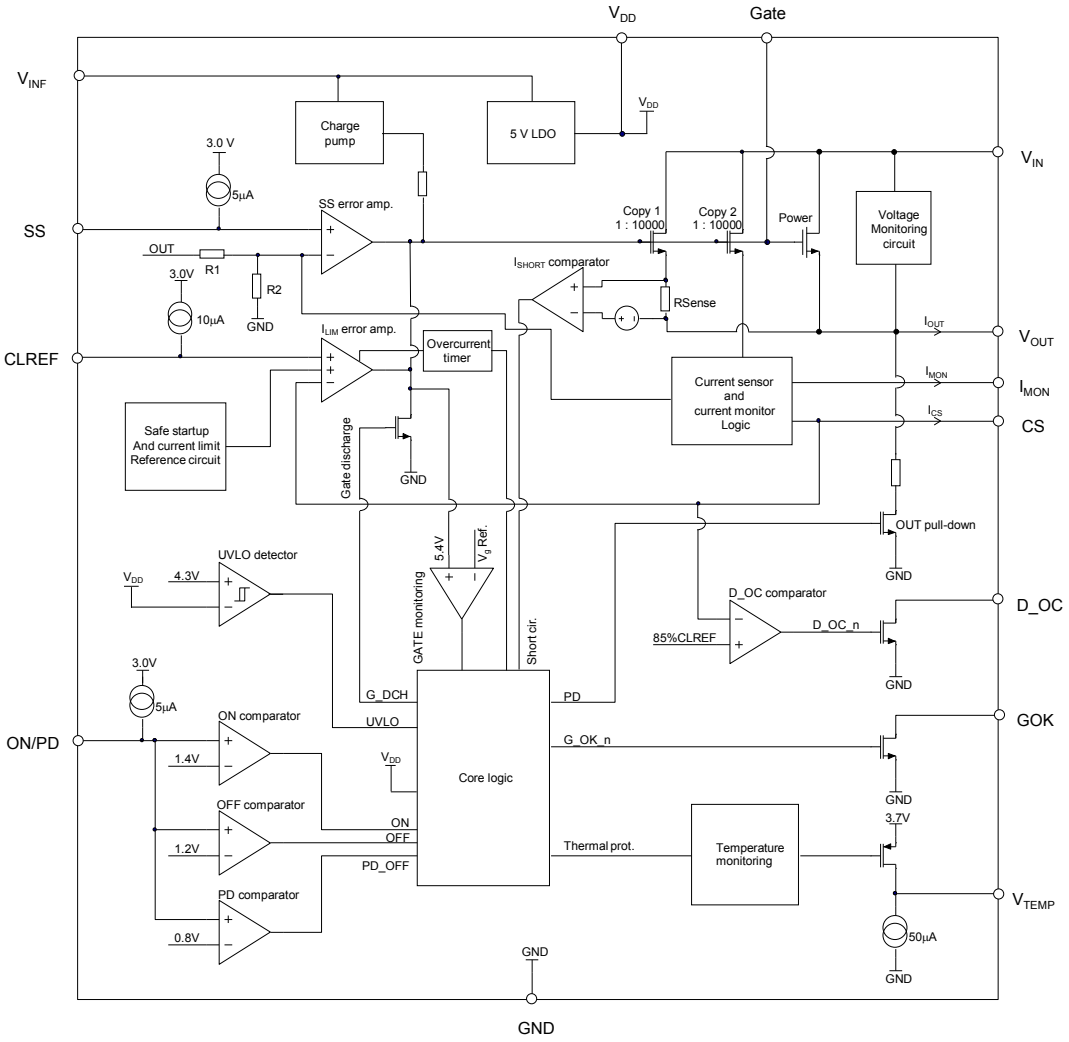
Turn-on time is programmable, which helps control the inrush current during start-up operations.

Multiple devices can work in parallel and smoothly share the current during the start-up phase, thanks to a dedicated current balancing feature.

The device also embeds an undervoltage lockout feature, self-diagnostics and absolute thermal protection.

1 Diagram

Figure 1. Block diagram



2 Pin configuration

Figure 2. **Pin connection (top view)**

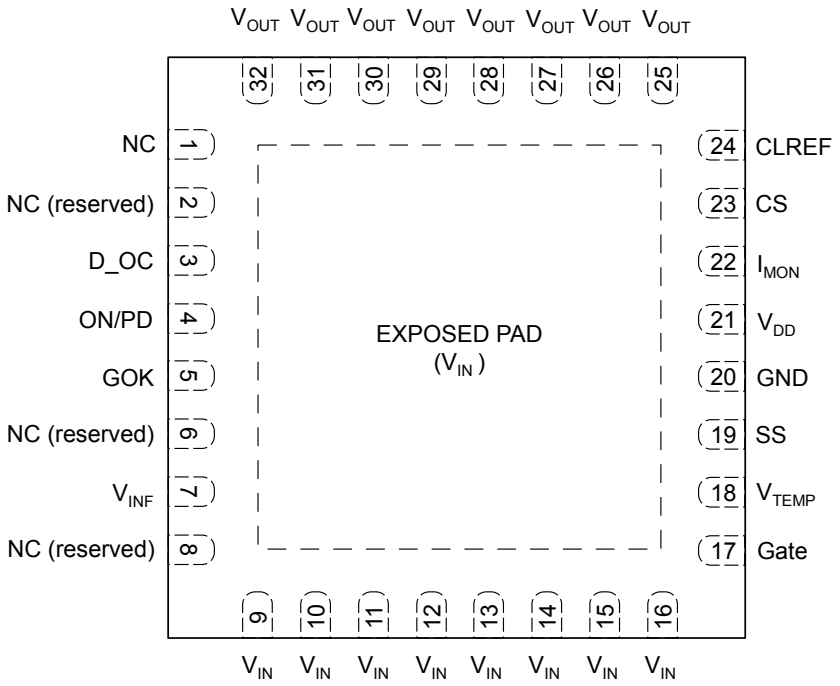


Table 1. **Pin description**

Pin #	Symbol	Function
25 - 32	V_{OUT}	Output voltage of the eFuse. All pins must be connected together on the PCB
3	D_OC	Output pin, driven low if the current set-point is exceeded. It is a 5 V compliant open-drain output
4	ON / PD	Enable/disable pin. This pin is internally pulled up. Pull this pin below the relevant threshold to shut down the chip. This pin also commands the output pull-down resistance. In case of latched fault, pulling down this pin will reset the chip. A capacitor connected between this pin and GND can be used to increase the delay during startup
5	GOK	Gate-OK output pin. It signals that a shutdown, which was not commanded by the enable pin, has happened. 5 V compliant open-drain output, low when the device is in a fault condition
1	NC	Not internally connected. It can be connected to any voltage
6, 8	NC/reserved	These pins are reserved and must be left floating
2	NC/reserved	This pin is reserved. If necessary, it can be connected to any voltage up to V_{IN}
7	V_{INF}	Input voltage for internal circuits. It is connected to V_{IN} through an R-C filter
9 - 16	V_{IN}	Input voltage of the eFuse. These pins must all be connected together and to the exposed pad
17	Gate	Gate pin of the internal MOSFET. This pin must be left floating or it can be bypassed to GND through an external R-C filter, to minimize the risk of oscillation in case of very small C_{OUT} or high input / output inductance
18	V_{TEMP}	Temperature monitor pin. Bypass to GND with 0.1 µF capacitor
19	SS	Soft-start pin. A capacitor connected between this pin and GND determines the soft-start time. If it is left floating, the start-up time is about 300 µs

Pin #	Symbol	Function
20	GND	Analog device ground
21	V_{DD}	Internal LDO output and compensation pin. It provides a regulated 5 V auxiliary output. This pin must be bypassed to GND via a 1 µF capacitor to ensure the correct functionality of the device
22	I_{MON}	Current monitor pin. A resistor (R_{MON}) connected between this pin and GND generates a voltage proportional to the output current. It is recommended to connect a capacitor (C_{MON}) in parallel to R_{MON} to filter the monitor signal
23	CS	Current feedback. A resistor (R_{CS}) connected between this pin and GND provides a feedback voltage for the overcurrent protection circuit and the overcurrent indicator (D_OC). Do not connect any capacitance to this pin
24	CLREF	Overcurrent protection set-point pin. Connect a resistor to GND or force an external control voltage to define the Overcurrent protection set-point
EXP. PAD	V_{IN}	Input voltage, internally connected to the power FET drain

3 Typical application

Figure 3. **Typical application diagram (external controller used for CLREF pin)**

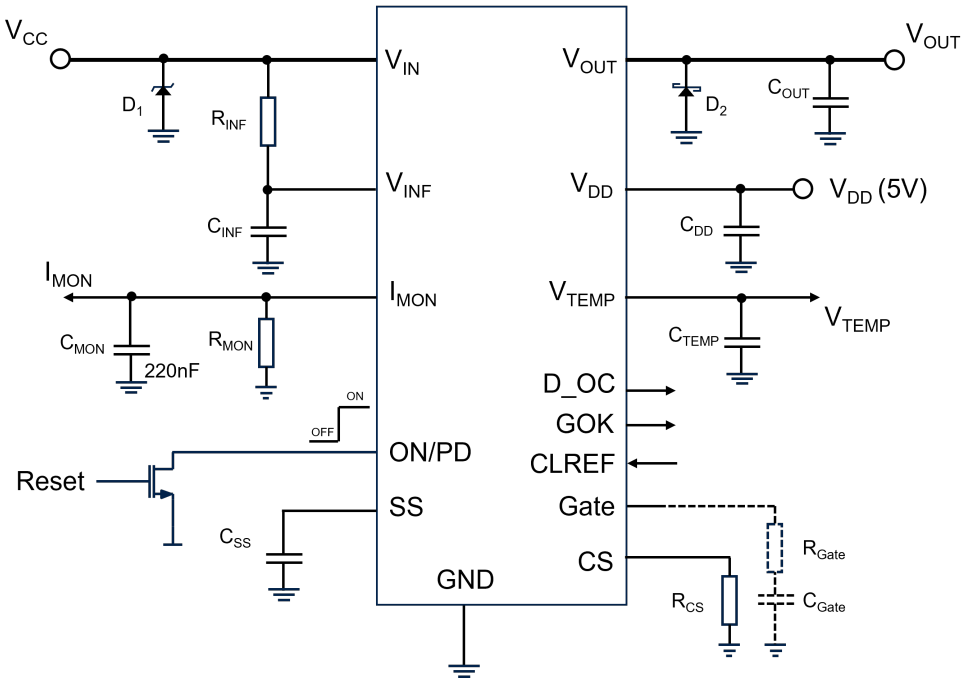


Figure 4. **Typical application diagram (current limit fixed via R_{CL})**

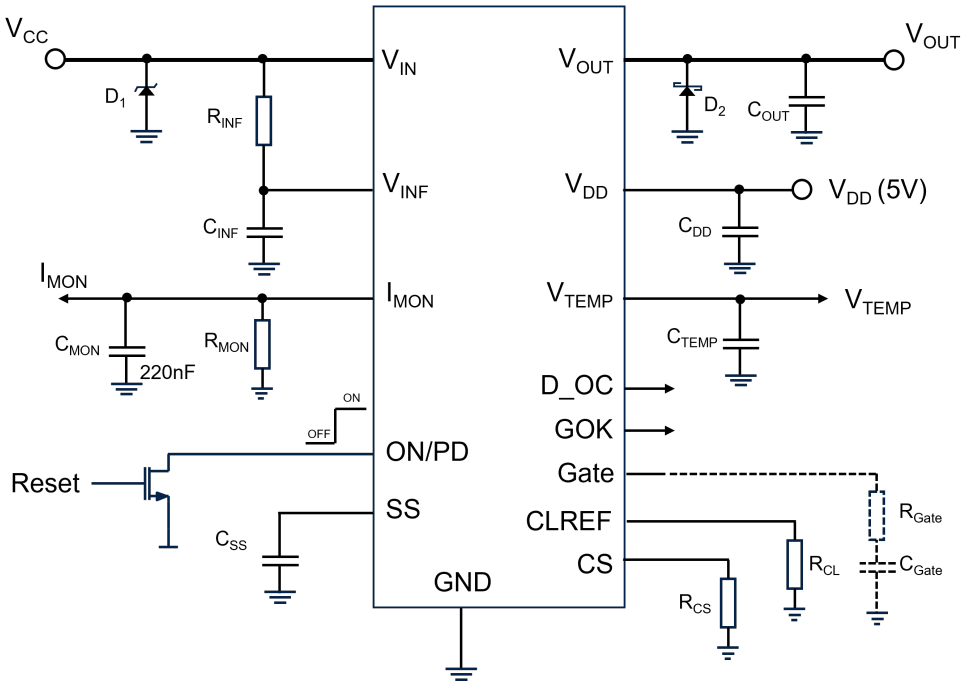
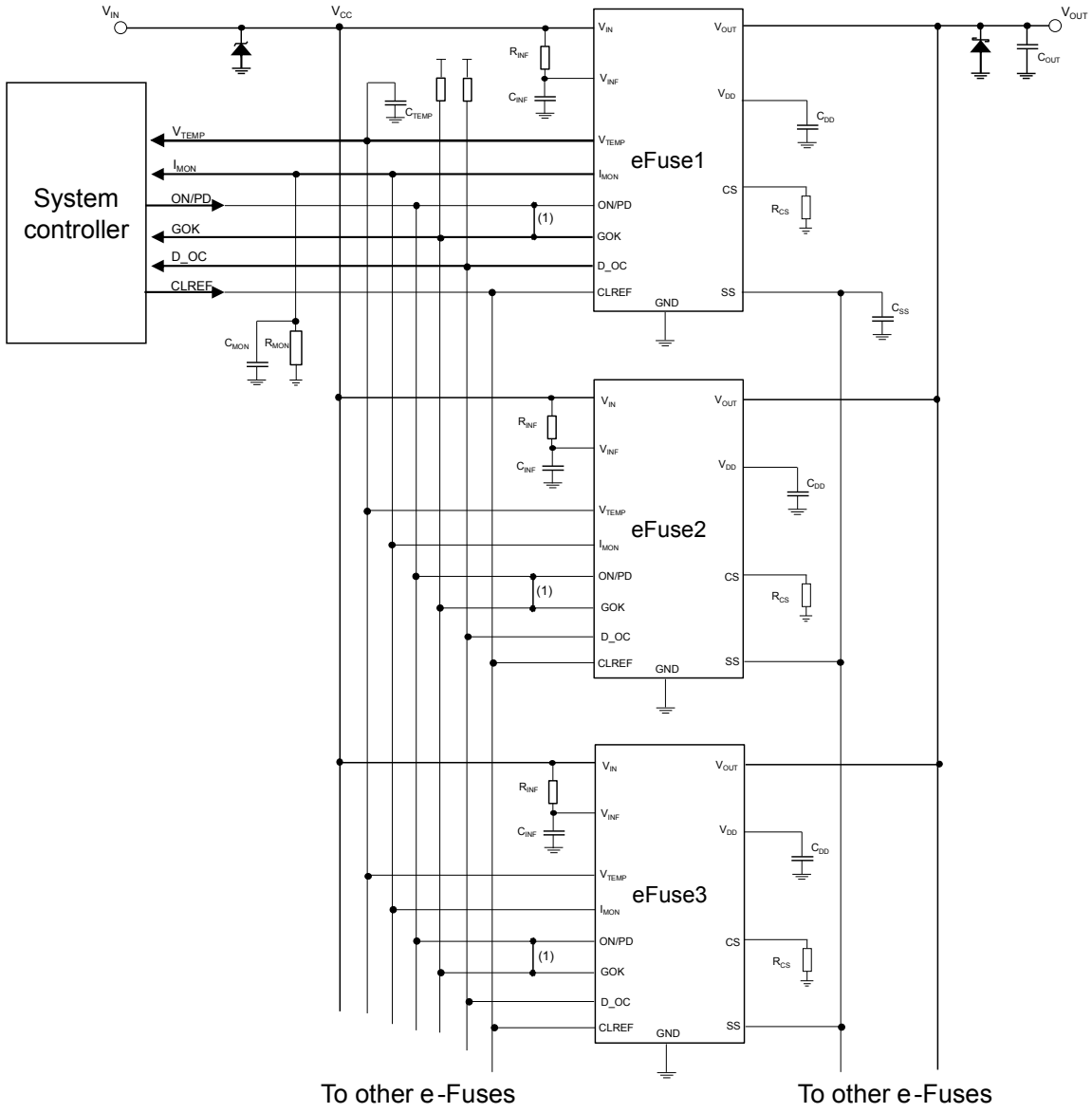


Figure 5. **Typical application diagram (multiple e-Fuses in parallel)**



Note: Connect all the GOK and ON/PD pins when using the auto-retry version (STEF12H60GAPUR) in parallel configuration, to achieve synchronous restart cycle. Refer to Parallel operation for further details.

4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN}	Input supply voltage	-0.3 to 20	V
V_{INF}	Input supply voltage	-0.3 to V_{IN}	V
V_{OUT}	Output voltage	-0.3 to V_{IN}	V
V_{DD}	LDO output voltage	-0.3 to 7	V
All other pins	Pin voltage	-0.3 to 6	V
I_{OUT}	Continuous output current	75	A
I_{DD}	LDO continuous output current	60	mA
ESD	Charge device model	± 500	V
	Human body model	± 2000	
T_{J-OP} (1)	Operating junction temperature	-40 to 125	°C
T_{J-MAX}	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	-55 to 150	°C

1. *The thermal limit is set above the maximum operating temperature. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Exposure to absolute-maximum-rated conditions may affect device reliability.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal resistance junction to ambient (1)	26	°C/W
	Thermal resistance junction to ambient, forced moving air (2)	22	
$R_{\theta JCT}$	Thermal resistance junction to top case	15	
$R_{\theta JCB}$	Thermal resistance junction to bottom case	1.4	
$R_{\theta JB}$	Thermal resistance junction to board (1)	5.4	
$R_{\theta JC}$	Thermal resistance junction to case (1)	1.4	

1. *JEDEC still air natural convection test as per JESD 51-2 A, at ambient temperature of 25 °C by using JEDEC (JESD 51-7) 4L PCB FR4 board using 1 sq−in pad, 1 oz Cu.*
2. *Forced moving air environment (100 LFM).*

Note: Functional operation beyond the recommended operating conditions is not implied.

Table 4. Recommended operating conditions

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IN}	Input voltage		8	12	15	V
I_{OUT}	Continuous output current				60	A
I_{DD}	LDO continuous output current	V_{INF} = 5.5 V			50	mA
R_{CS}	Current set resistor		1.8		4	kΩ
V_{CLREF}	Control voltage range		0.2		1.75	V
C_{OUT}	Output capacitance (1)		47			µF
t_{ss}	Soft-start duration		10	50	100	ms
C_{DD}	V_{DD} capacitor value (2)		1	2.2	10	µF

1. *The maximum allowed output capacitance to obtain a successful startup, without triggering internal fault protections, depends on the device soft-start time, the R_{CS} resistor and output load during power-up.*
2. *V_{DD} capacitor is mandatory to ensure the internal regulator stability and the device functionality.*

Note: Functional operation beyond the recommended operating conditions is not implied.

5 Electrical characteristics

T_J = -40 °C to +125 °C, typical values refer to T_J = 25 °C, V_{IN} = V_{INF} = 12 V, $V_{ON/PD}$ = 3.3 V; C_{OUT} = 100 µF; unless otherwise specified. Min. and max. values are guaranteed by design and characterization through statistical correlation.

Table 5. Electrical characteristics

Symbol	Parameter	Testconditions	Min.	Typ.	Max.	Unit
Input section						
V_{IN}	Operating input voltage		5	12	18	V
I_q	Quiescent current	Device operating, no load ($V_{ON/PD}$ > 1.4 V)		650	1000	µA
		Fault condition		300		
		Off-state, $V_{ON/PD}$ = 0 V, V_{INF} = 16 V		200	400	
LDO						
V_{DD}	LDO output voltage	I_{DD} = 1 mA, V_{INF} = 6 V	4.6	4.9	5.2	V
I_{DDmax}	LDO short circuit current (1)	V_{DD} = 0 V	60	120		mA
V_{DROP}	LDO dropout voltage	I_{DD} = 30 mA	66	100	160	mV
V_{DD_ON}	UVLO rising threshold		4.1	4.3	4.6	V
V_{DD_OFF}	UVLO falling threshold		3.8	4.0	4.2	V
Start-up						
I_{SS}	Soft-start capacitor charging current		4.5	5.2	6	µA
t_{SSMAX}	Soft-start max time	if V_{OUT} < 90% of V_{IN} after t_{SSMAX} shutdown is forced		200		ms
A_S	Soft-start gain	Relation between internal soft-start signal ramp and V_{OUT}		10		V/V
Power MOSFET						
R_{DSon}	On-resistance	T_J = 25 °C		0.85	1.1	mΩ
I_L	Off-state leakage current	$V_{ON/PD}$ = 0 V, V_{IN} = 16 V, T_J = 25 °C			1	µA
Overcurrent protection and current monitor circuit						
V_{CS_TH}	OCP activation threshold (V_{CS} = I_{RCS} x R_{CS})	V_{OUT} > 80% of V_{IN}	97	100	103	% of V_{CLREF}
V_{CL_MAX} (2)	Maximum C_L reference voltage		1.73	1.8	1.86	V
V_{CL_FD}	Internal voltage reference for foldback current limit at startup	V_{OUT} is lower than 40% of V_{IN}	130	150	170	mV
V_{CL_ST}	Internal voltage reference for current limit at startup	V_{OUT} is between 40% and 80%	470	500	530	mV
t_{CL}	OCP response time (3)	from V_{CS} > V_{CLREF} until OCP trigger		50		µs
I_{CL}	C_{LREF} pin internal biasing current	rom C_{LREF} pin into 1 V source, 0 <T_J< 125°C	9.4	10	10.4	µA
V_{CL_HI}	Maximum voltage of the C_{LREF} pin internal biasing source			3.0		V

Symbol	Parameter	Testconditions	Min.	Typ.	Max.	Unit
I_{RCS}/I_{MON}	Current sense/monitor accuracy	T_J = 25 °C, 10 A < I_{OUT} < 60 A (3) (4)	-3		3	%
A_{CS}, A_{MON}	Current sense and current monitor gain	I_{RCS}/I_{OUT}, I_{MON}/I_{OUT}, T_j = 25 °C, 10 A < I_{OUT}< 60 A (3) (4)	9.7	10	10.3	µA/A
t_{SH}	Shutdown timer (3)	From overcurrent detection to MOSFET turn-off	2.47	2.6	3.15	ms
I_{SC}	Short-circuit current limit (3)			110		A
t_{SC}	Short-circuit protection response time (3)	From I_{OUT} > I_{SC} until MOSFET gate pull-down		500		ns
V_{MON_MAX}	Internal current source maximum voltage	Internal pull-up voltage on I_{MON} pin		3.0		V
ON/PD (chip enable pin)						
V_{OFF}	Low -level input voltage	Output disabled/PD activated	1.11	1.2	1.29	V
V_{ON}	High-level input voltage	Output enabled	1.3	1.4	1.5	V
V_{PD}	Pull-down de-activation and reset threshold	Pull-down de-activated. Device reset from a latched fault	0.71	0.8	0.89	V
t_{ON}	Initial delay time	From $V_{ON/PD}$ > V_{ON} to soft-start beginning	0.8	1	1.2	ms
$I_{ON/PD}$	Enable pin bias current		4	5	6	µA
V_{ON/PD_MAX}	Internal current source maximum voltage	Internal pull-up voltage on ON/PD pin		3.0		V
R_{PD}	Output pull-down resistance	V_{OUT} = 12 V, pull-down activated		0.72		kΩ
t_{PD}	Output pull-down delay timer	From V_{OFF} < $V_{ON/PD}$ < V_{PD}		2		ms
Temperature monitor						
V_{TEMP}	V_{TEMP} voltage	T = 25 °C		450		mV
	Temp coefficient (3)	T = 0 °C to 125 °C		10		mV/°C
	Load capability	Maximum current			4	mA
	Pull-down current	T = 25 °C		50		µA
Status line						
GOK	Gate-OK output voltage	I_{SINK} = 1 mA			0.1	V
	Leakage current	V_{GOK} = 5 V			1	µA
V_{OC}	Overcurrent detection threshold	V_{CS} voltage threshold that triggers D_OC low	83	85	87	% V_{CLREF}
D_OC	Overcurrent monitor signal active low voltage	I_{SINK} = 1 mA V_{CS} > V_{OC}			0.1	V
	Leakage current	V_{D_OC} = 5 V V_{CS} < V_{OC}			1	µA
t_D	D_OC signal response time (3)			1		µs
Thermal protection						
t_{SD}	Shutdown temperature (3)	GOK pulled low	130	140	150	°C
t_{Retry}	Autoretry delay time (only on STEF12H60GAPUR)	From shutdown due to fault to automatic restart		1		s
Internal MOSFET diagnostics						
V_{DS_TH}	Drain-source short detection threshold	If V_{OUT} > V_{DS_TH} at startup, startup is postponed		90		% of V_{IN}

Symbol	Parameter	Testconditions	Min.	Typ.	Max.	Unit
V_{DS_OK}	Drain-source voltage-good detection threshold	If $V_{OUT} < V_{DS\_OK}$ startup is resumed		70		% of V_{IN}
V_{OUT_LOW}	Low V_{OUT} detection threshold	After startup, if $V_{OUT} < V_{OUT\_LOW}$, the device is turned off		90		% of V_{IN}
V_{DG_SH}	Gate-drain short detection voltage threshold	If $V_G > V_{DG\_SH}$ after enable by ON pin, startup is postponed		3.1		V
V_{DG_OK}	Gate-drain voltage-good detection threshold	If $V_G < V_{DG\text{-}OK}$ startup is resumed		3		V
V_{G_LOW}	Gate fault detection threshold	If $V_{GD} < V_{G\_LOW}$ device is turned off		5.7		V
t_{G_LOW}	Get fault timer in normal operation	After t_{SSMAX} elapses, time from $V_{GD} < V_{G\_LOW}$ transition to gate fault detection		200		ms

1. *Pulsed test. The internal LDO is not equipped with thermal protection. Short-circuit duration must not exceed 1 ms to avoid damage.*
2. *If the voltage on CLREF pin is higher than V_{CL_MAX} internal reference, the current limit reference voltage is clamped to V_{CL_MAX}.*
3. *Guaranteed by design, not tested in production.*
4. *MOSFET fully conducting, at minimum R_{ON}.*

6 Device functional description

The STEF12H60G is a 12 V electronic fuse (eFuse), which is able to protect the final application during fault events, such as output overload or short-circuit.

During the start-up phase of the eFuse, the current is actively limited to avoid startups into faulty loads and to keep the internal power element within a safe operating area. During normal operation, the eFuse works as a low-resistance power switch, therefore the output voltage follows the input voltage. If an overcurrent is detected, the eFuse behaves as a timed circuit breaker with a fixed 2.6 ms safety timer. If the overcurrent persists once the timer elapses, the output is turned off.

In any operating condition, if the die temperature hits the thermal protection threshold, due to high power dissipation, the device goes into shutdown, the internal switch is turned off and the load is disconnected from the power supply. The device is latched in this off-state until a power supply re-cycle is performed. The auto-retry version on the other hand is able to re-try starting the device after a fault event, with a typical delay of 1 ms.

The overcurrent protection and soft-start features are programmable by the user, through external components.

6.1 UVLO function

The device is supplied through the V_{IN} pins, which carry the power directly to the internal power MOSFET drain connection, and the V_{INF} pin, which is the input of the internal regulator, used to supply the analog and logic circuits. This pin must be connected externally to V_{IN} through an R-C filter (see Section 3).

The UVLO (undervoltage lockout) monitors the voltage of the internally regulated V_{DD} node and turns on the device when $V_{DD} > V_{DD\_ON}$ (typically 4.3 V). If V_{DD} falls below the UVLO hysteresis threshold ($V_{DD} < V_{DD\_OFF}$), the device is turned off including the reset of the fault state.

6.2 ON/PD function - device reset

During turn-on, provided that the UVLO rising threshold has been surpassed, the start-up procedure begins once the device is enabled via the ON/PD pin. The ON/PD is a logical input with a dual functionality, according to the following description:

1. Enable/disable the device: when $V_{ON/PD} > V_{ON}$, the device is enabled. If $V_{ON/PD}$ is pulled down to V_{OFF} or a lower voltage, the device is disabled and the output is shut down. In case the shutdown occurrs due to a fault (thermal, overcurrent, failed startup), the device cannot be turned on again via the ON/PD pin. To reset the device from this latched status, a power supply re-cycle is necessary. Alternatively, a reset can be forced without turning off the power supply, by pulling the V_{DD} pin below the UVLO voltage and then releasing it.
2. Activate/deactivate the output discharge feature (PD – output pulldown): if $V_{ON/PD}$ is kept between V_{PD} (typ. 0.8 V) and V_{OFF} (typ. 1.2 V) for at least 2 ms (t_{PD}), the integrated 0.77 kΩ R_{PD} discharging resistor is connected between V_{OUT} and GND.
3. Reset the device from a latched fault status: if the ON/PD voltage is forced below V_{PD} (typ. 0.8 V), a device reset is triggered. The system will startup again once the ON/PD pin is released.

The ON/PD pin has an internal pull-up current generator connected to the internal LDO. Therefore, if the pin is not connected to an external controller IC, it goes to the ON-state (device enabled).

The 5 µA ON/PD bias current can be used to charge an external capacitor, in this manner prolonging the initial delay time, defined as the time interval between the power supply reaching the UVLO threshold and the output voltage controlled ramp-up initialization.

6.3 Soft-start

The device provides a monotonic, controlled startup ramp, in order to keep the inrush current under control. The output voltage rise time can be set by an external C_{SS}, which is charged with a constant current during the startup phase. The soft-start range is adjustable from 1 to 100 ms.

Given the required ramp-up time, the C_{SS} capacitance can be calculated according to the following equation:

$$C_{SS} = N \times \frac{(t_{SS} \times I_{SS} \times 10)}{V_{IN}} \quad (1)$$

where V_{IN} is typically 12 V, t_{SS} is in the 10-100 ms range and N is the number of eFuses in parallel.

The table below shows typical values of soft-start duration calculated with standard capacitors and a typical I_{SS} value.

Table 6. Output voltage rise time vs. C_{SS} value (V_{IN} = 12 V)

Symbol	Value							
C_{SS} (nF)	47	82	120	180	220	270	330	390
t_{SS} (ms)	10.8	18.9	27.7	41.5	50.8	62.3	76.2	90

Important: The soft-start capacitor must be always connected to ensure controlled operation during startup. In case of absence/incorrect connection of the C_{SS}, the startup phase is short (300 µs). This might result in a significantly high charging current, eventually leading to the device shutdown due to an overcurrent/ overtemperature fault. To prevent the device from starting in faulty loads (such as: resistive load, or damaged bulk output capacitors) the following startup control flow is applied:

- Startup fold-back current limit: current limit value during startup phase is dependent on the sensed output voltage. At the very beginning of startup, when the output voltage is close to zero, the current limit internal reference voltage is reduced to V_{CL_FD}. Any higher current limit value set by the user via the CLREF pin is overridden by the device.
- Startup current limit: during the ramp-up phase, the current limit internal reference voltage is reduced to V_{CL_ST}. Any higher current limit value, set by the user via the CLREF pin, is overridden by the device.
- Maximum startup time: startup longer than 200 ms is always aborted by the device. If V_{OUT} does not reach 90% of V_{IN} in 200 ms, the device is turned off and the GOK fault indicator is asserted low.

Normal CLREF functionality is resumed at the end of the startup phase (V_{OUT} > 80 % of V_{IN}). Adding a capacitor in parallel to the ON/PD pin, the initial t_{ON} delay time between valid V_{IN} value and controlled output ramp-up start (V_{OUT} = 1 V) can be increased.

The default delay time without C_{ON} capacitor is typically 1.25 ms.

6.4 Normal operating conditions

Once the start-up phase ends, the STEF12H60G eFuse behaves like a mechanical fuse, supplying the load connected to its output with the same voltage shown at its input, minus the small voltage fall due to the N-channel MOSFET $R_{DS(on)}$. The status line open-drain indicators GOK and D_OC provide information about the status of the device.

6.5 Overcurrent protection (OCP)

STEF12H60G features a robust overcurrent protection scheme. The functionality of the OCP changes according to the operating conditions. During startup, the current is actively limited according to the load current and output voltage condition, based on internal preset thresholds.

In normal operation, the OCP threshold is configured by the user according to the application condition by setting a reference voltage on the CLREF pin. In this case, the OCP behavior is based on a timed circuit breaker approach. When the overload occurs, a 2.6 ms safety timer starts. The current is not limited during this time. If the overcurrent ends before the timer elapses, the OCP is deactivated. Otherwise, the output is turned off. The overcurrent protection consists of two sub-circuits:

- The current sense (CS) circuit, responsible for sensing the load current and providing a feedback signal to detect overcurrent. It relies on a small copy-MOSFET built into the integrated power MOSFET to generate a replica of the load current proportional by $A_{CS} = I_{RCS}/I_{OUT}$ = 10 µA/A, into the external R_{CS} resistor attached to the eFuse. This current creates a variable V_{CS} voltage across the resistor, defining the eFuse working current CS, which is continuously compared to the current limit reference voltage present on the CLREF pin.
- The current limit (CL) circuit defines the reference threshold for the intervention of the overcurrent protection. This reference point is a voltage (V_{CLREF}) usually provided externally by the system control IC to the CLREF pin, and continuously compared internally to the feedback signal from the CS circuit. In this manner, the OCP intervention point can be throttled to satisfy the system power requirements during operation. In simple standalone designs, such as the one shown in Figure 4, where no control IC is present, the reference signal can be generated by connecting a resistor between the CLREF pin and GND. An integrated bias generator sources 10 µA of current to the RCL resistor, generating a fixed V_{CLREF}, which sets the current limit thresholds.
  During startup, the CLREF signal is provided by the internal reference circuits, depending on the output voltage level:
  - if V_{OUT} is lower than 40% of V_{IN}, V_{CLREF} is set to V_{CL_FD}
  - if V_{OUT} is between 40% and 80% of V_{IN}, V_{CLREF} is set to
  - Once V_{OUT} surpasses 80% of VIN, startup current limit is deactivated, V_{CLREF} control is transferred to the CLREF external voltage and OCP works as in the normal operating condition.
  To always ensure reliability, the signal on CLREF is internally clamped to V_{CL_MAX}, therefore, even in case of a wrong signal provided externally on the pin, a safety current limit threshold is always present.
  An overcurrent event is detected when the voltage on the CS pin surpasses the V_{OC} threshold, which is typically 85% of the voltage at the CLREF pin ($V_{CS} > V_{OC}$). In this case, the status D_OC indicator is pulled down. If the load status reverts to normality (V_{CS} falls below 75% of V_{CLREF}), D_OC is released. Based on the value of the R_{CS} resistor, the load current level for D_OC triggering can be evaluated by using the following equation:

$$I_{OUT} = \frac{V_{OC}}{R_{CS} \times A_{CS}} \quad (2)$$

In case of overcurrent detection, when V_{CS} surpasses V_{CLREF}, the V_{GS} of the internal MOSFET is immediately modulated in order to clamp the load current to the I_{LIM} value defined by the user via the C_{LREF} pin, according to the following equation:

$$I_{LIM} = \frac{V_{CLREF}}{R_{CS} \times A_{CS}} \quad (3)$$

Once the timer elapses, if the current is still higher than I_{LIM}, the internal MOSFET is shut down and the GOK indicator is pulled to low status, to inform the system controller that a shutdown which is not due to ON/PD (fault) occurred.

Thermal protection intervenes if the die temperature increases too much and hits the thermal protection threshold (140 °C typ.), turning off the internal MOSFET and asserting GOK low.

A second-level current limit (I_{SC}) is quickly activated in case the load current surpasses 100 A.

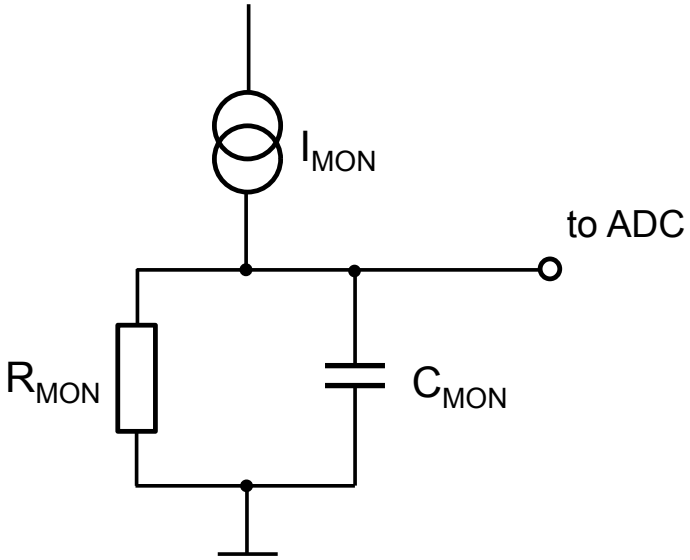
This additional protection, fixed by design, is able to respond to short-circuit events on the output. In such an occurrence, the device is immediately shut down and the D_OC pin is asserted.

6.6 Current monitor

The device is equipped with a current monitoring capability that allows the system controller to read the current flowing through the fuse. An I_{MON} current proportional to the load current flowing through the eFuse is imposed on an external R_{MON}, converting the sensed current into a voltage for further processing by the ADC. The I_{MON} signal is the output of a chopper amplifier, therefore an external bypass capacitor is recommended to reduce the output ripple and to provide a smooth signal (see image below). The suggested minimum value for the filter capacitor is 3.9 nF. Lower values result in a worse ripple amplitude.

The current, monitoring amplifier gain and defined as $A_I = I_{MON} / I_{OUT}$, is typically 10 µA/A.

Figure 6. Current monitor simplified circuit



6.7 Temperature monitor and thermal shutdown functions

The STEF12H60G embeds two thermal sensors, each one accomplishing a specific function:

- Overtemperature sensor: this is embedded into the power MOSFET. It monitors the power MOSFET temperature, which is subjected to very fast increases during overload events. If the device temperature exceeds the thermal threshold, typically 140 °C, the thermal shutdown circuit turns the power MOSFET off, thus disconnecting the load. The GOK pin is pulled down. The thermal shutdown protection is always active and overrides any other protection/control feature of the device.
- Temperature sensor: this consists of precise thermal sensors embedded in the controller die. The purpose is to statically monitor the overall device temperature, and generate a precise monitor signal (V_{TEMP}) accordingly. Overall typical accuracy is +/- 5 °C. To ensure a stable regulation of the temperature monitor signal under all operating conditions, it is recommended to bypass this pin to GND via a 0.1 µF C_{TEMP} capacitor, as shown in Figure 3 and Figure 4.

The device can be reset following a thermal shutdown condition by pulling the V_{DD} pin below the UVLO threshold or by re-cycling the supply voltage.

In parallel configuration, to accomplish a simultaneous reset, each device must have its dedicated reset switch, for instance a MOSFET. All gates of the reset MOSFETS must be tied together to the common reset signal.

6.8 Status indicators and fault conditions

Two open-drain flags can be used to monitor the status of the eFuse, along with the current and temperature monitor signals.

- D_OC - Overcurrent indicator: in normal operation and during startup it is released. It is pulled down upon detection of an overload (see Section 6.5)
- GOK - gate ok indicator: this indicator signals that there was a shutdown which was not commanded by the enable pin (ON/PD). In particular, this pin is pulled low when:
  - input voltage is too low: V_{DD} lower than UVLO threshold
  - startup time is too long: V_{OUT} does not reach 90% of V_{IN} in 200 ms
  - current limit is too long: a current limit event is longer than t_{SH} (2.6 ms typ.)

During the startup, GOK is released once UVLO is reached, under the condition that V_{OUT} is below V_{DS_OK} (drain to source short detection, see Section 6.9), therefore it cannot be used directly as a power-good flag. GOK is also pulled to a low level in the case of any of the faults described in Section 6.9.

6.9 Diagnostic functions and protections

The STEF12H60G embeds several internal diagnostic features that prevent fault conditions induced internally that may affect the application (refer to Section 5):

- Power MOSFET gate leakage check during startup and normal operation (V_{Gate}-V_{IN} < 5.6 V)
- Gate shorted-to-V_{IN}
- Drain to source short in disabled mode (ON pin low). This protection prevents a new startup until the V_{OUT} falls below the V_{DS_Ok} value.
- V_{OUT} too low (V_{OUT} < 90% of V_{IN}) after soft-start
- V_{OUT} does not reach 90% of V_{IN} in 200 ms during startup
- Charge pump error
- Pull-down circuit error

In any case of fault, the GOK indicator is pulled down and the soft-start capacitor is discharged.

6.10 Latch (STEF12H60GPUR) and auto-retry versions (STEF12H60GAPUR)

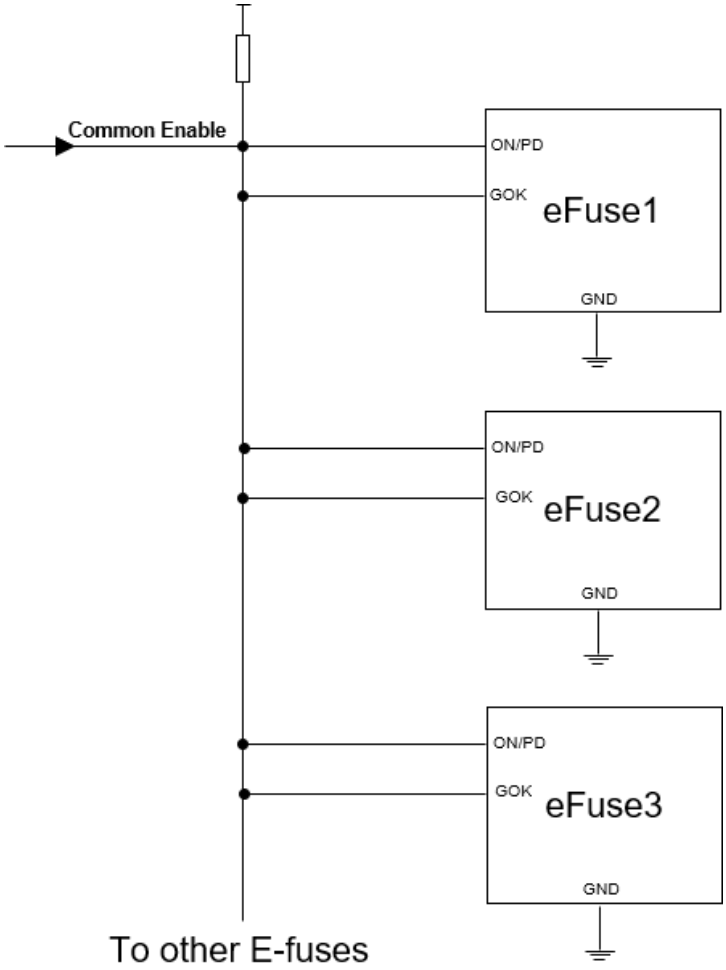
The STEF12H60G eFuse is offered in two variants that differ in how the device reacts after a fault condition (see Section 6.8 and Section 6.9). In particular, the STEF12H60GPUR latches off after a fault and can be reset by using one of the methods described in Section 6.2. The STEF12H60GAPUR on the other hand stays in OFF mode for 1 s (t_{Retry}), after which it restarts automatically, initiating a soft-start cycle. The number of restart cycles is not internally limited.

6.11 Parallel operation

Figure 5 shows a typical circuit configuration used to protect high power systems. In this case multiple STEF12H60G are used in a parallel configuration to increase the total current capability. In such design the following guidelines must be followed:

- The ON_PD pins of all eFuses must be tied together to achieve a simultaneous startup.
- All the SS pins must be connected together to a single C_{SS} capacitor. The value of this capacitor should be calculated by using , taking into account that each device provides its I_{SS} charging current to the capacitor. The SS pin is also used to discharge the C_{SS} capacitor during shutdown. In case one eFuse shuts down, the common C_{SS} capacitor is discharged causing simultaneous shutdown of all the paralleled devices.
- All the CLREF pins must be tied together to a single R_{CL} resistor or to common V_{CLREF} control signal from the system controller to set the overcurrent protection reference. When using the R_{CL} resistor, the I_{CL} bias current coming from each device must be accounted.
- Each CS pin must be connected to a local R_{CS}, to ensure the current sensing circuit is able to read the single eFuse current.
- The I_{MON} pins can be all tied together to a single R_{MON} / C_{MON} filter. In this way the I_{MON} currents coming from each eFuse all contribute to the voltage generated on the resistor, that results proportional to the total system current. If it is necessary to read the single eFuse current, the local R_{MON} resistor approach can be used.
- The V_{TEMP} pins can be all tied together in Or-ing configuration, therefore the system controller reads the highest temperature among all the eFuses.
- When needed, all of the D_OC and all of the GOK fault flag pins can be tied together and pulled up via a single resistor.
- To accomplish simultaneous reset, each device must have its dedicated reset switch, for instance a MOSFET, connected to V_{DD} pin. All the gates of the reset MOSFETS must be tied together to the common reset signal.
- If the auto-retry version (STEF12H60GAPUR) is used in parallel configuration, dedicated circuital provision should be made. Specifically, it is recommended to connect all the ON/PD pins to the GOK ones as shown in Figure 1 to ensure a proper synchronization of the auto-retry cycle. A common Enable signal can be used to start up the devices.
- During power-up in parallel operation, keeping the load current through each eFuse lower than 1.5 A (typical) helps to prevent overstress in the internal power MOSFETS at each soft-start cycle.

Figure 7. **Additional connections for multiple STEF12H60GAPUR (autoretry version)**



6.12 Application suggestions and PCB layout guidelines

STEF12H60G eFuse is used in high-power systems where high current flows through the power path. In case of overload or short-circuit events, the device instantaneously interrupts the current flow. In such cases, the input/output stray inductances cause voltage overshoots on the input and undershoots on the output of the device, which can exceed the absolute maximum ratings and damage the eFuse.

To reduce the effects of such transients, it is recommended to adopt the following application design guidelines:

- Minimize the inductance of the input and output tracks
- Use TVS diodes on the input to absorb inductive spikes, see D1 in Figure 3. The STMicroelectronics SMC50J12CA high-power TVS diode is a tested and recommended solution to protect the STEF12H60G, for operation over the 12V bus.
- Place a Schottky diode on the output to absorb negative spikes, see D2 in Figure 3. The STMicroelectronics FERD15S50 field-effect rectifier is a tested and recommended protection against output voltage undershoot.
- Use a combination of ceramic and electrolytic capacitors on the output.

7 Typical characteristics

C_{IN} = 1 µF; C_{OUT} = 10 µF, T_J = 25 °C unless otherwise specified.

Figure 8. Quiescent current vs. temperature

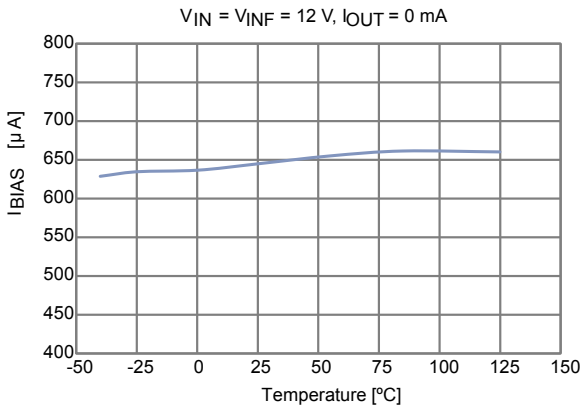


Figure 9. Shutdown current vs. temperature

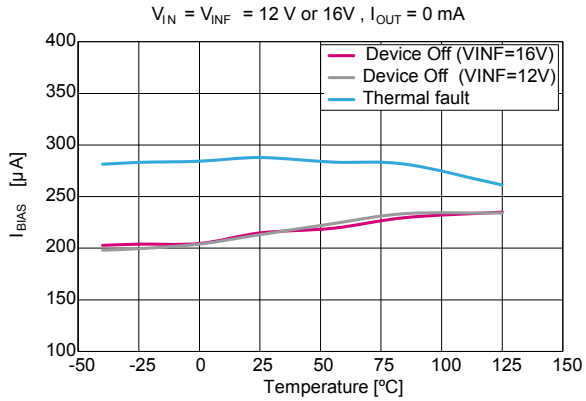


Figure 10. I_{MON} gain accuracy vs. load current and temperature

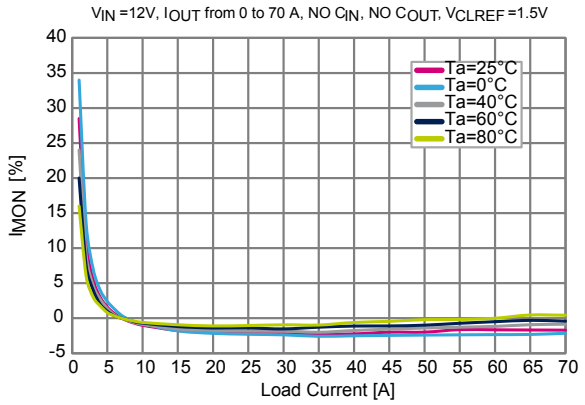


Figure 11. I_{MON} current vs. load current

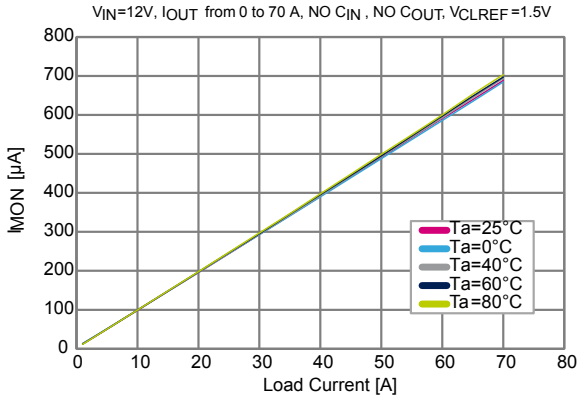


Figure 12. CS current vs. temperature

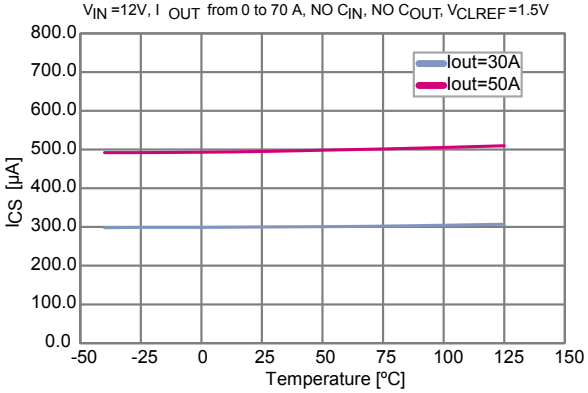


Figure 13. V_{CLREF} threshold vs. temperature

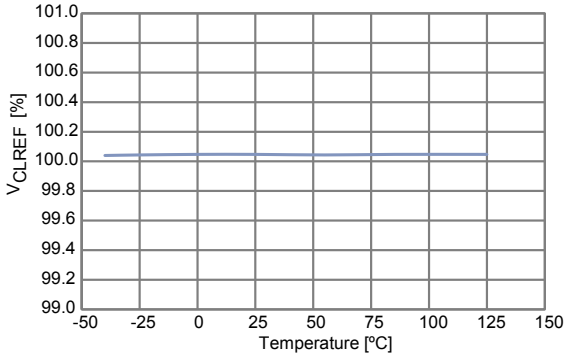


Figure 14. CLREF pin bias current vs. temperature

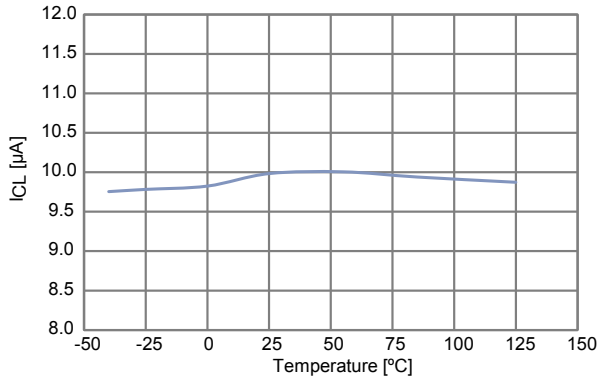


Figure 15. V_{DD} voltage vs. temperature

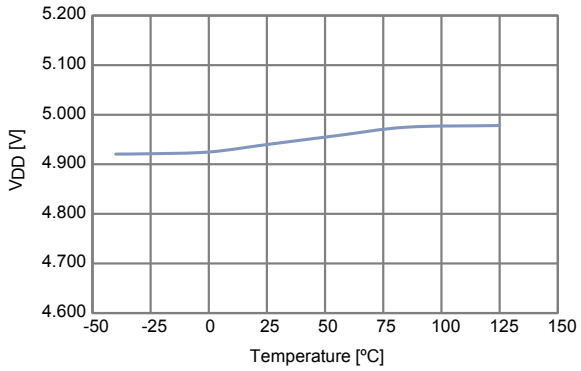


Figure 16. V_{TEMP} voltage vs. temperature

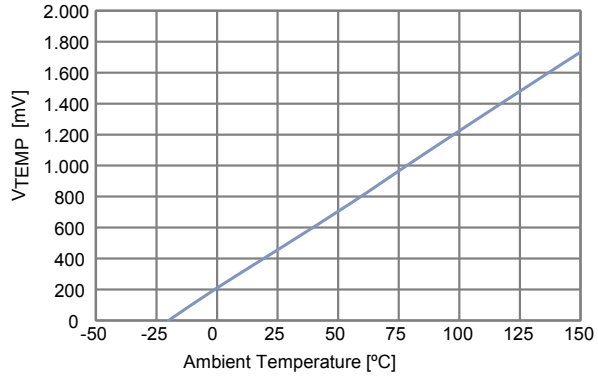


Figure 17. UVLO thresholds vs. temperature

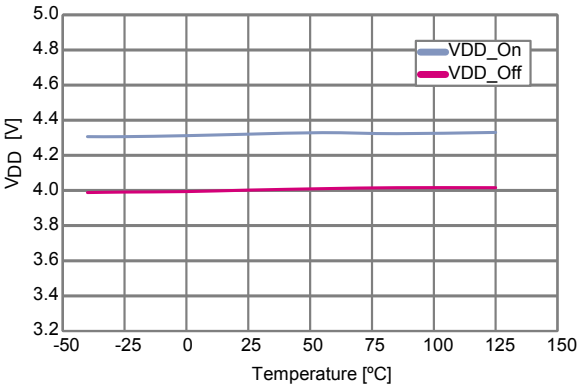


Figure 18. ON/PD thresholds vs. temperature

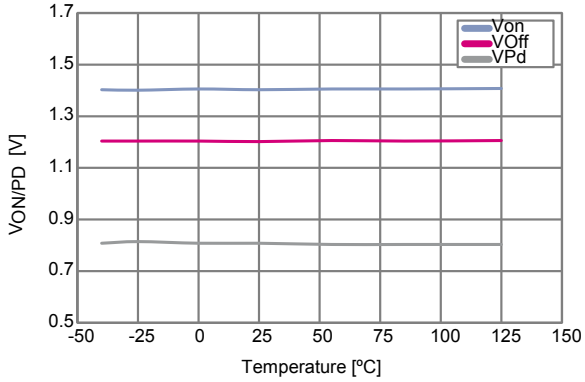


Figure 19. ON/PD pin current vs. temperature

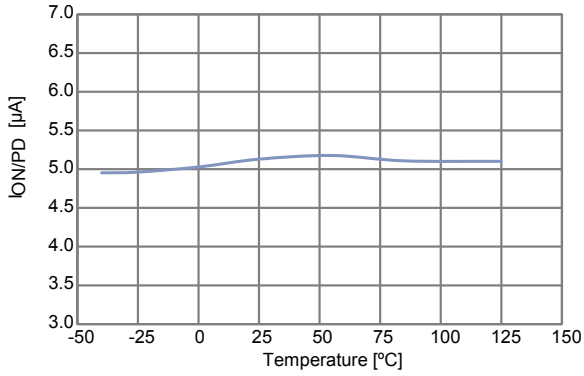


Figure 20. SS pin bias current vs. temperature

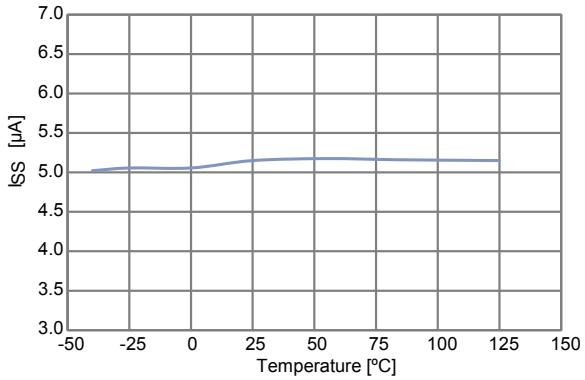


Figure 21. Turn-on initial delay vs. temperature

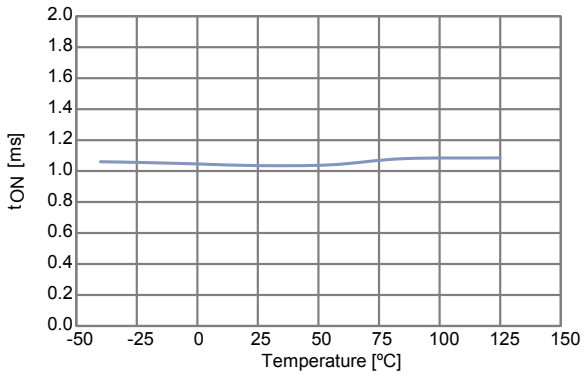


Figure 22. On-resistance vs. temperature

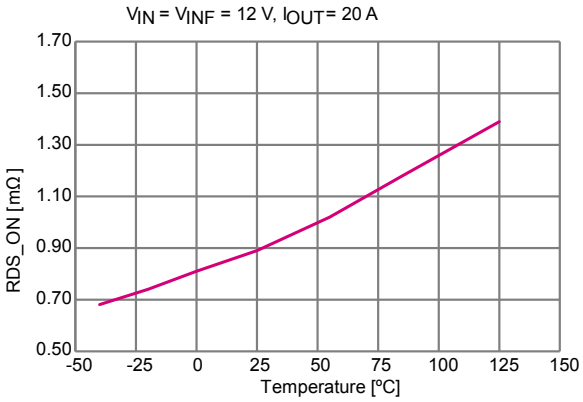


Figure 23. Off-state leakage current vs. temperature

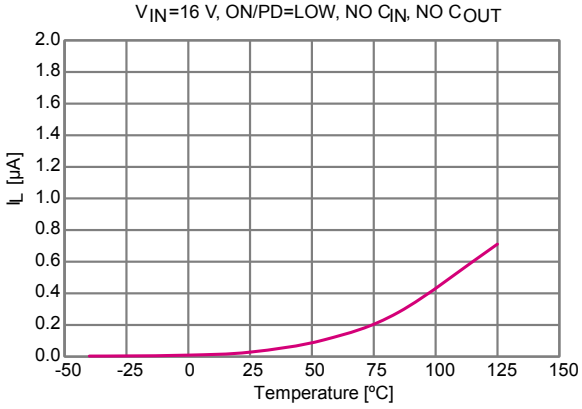


Figure 24. Startup by V_{IN} (no load)

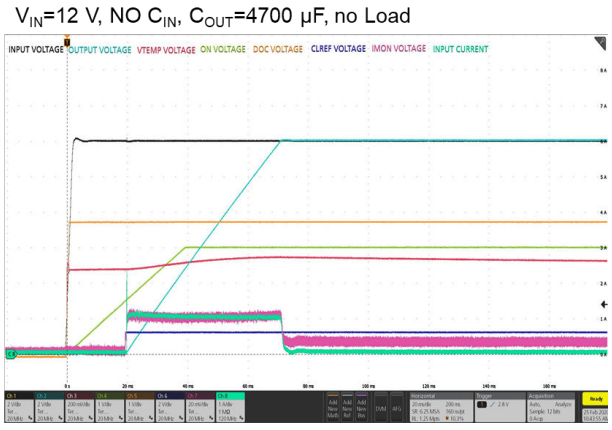


Figure 25. Shutdown by V_{IN} (no load)

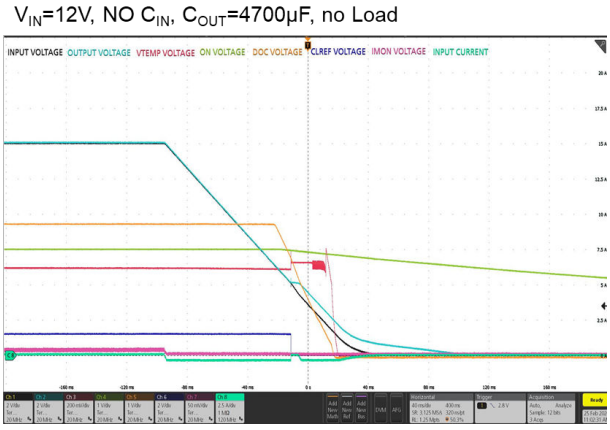


Figure 26. Startup by V_{IN} (C_{OUT} = 6200 µF, no load)

V_{IN}=12 V, $C_{ON/PD}$=4.7 nF, NO C_{IN}, C_{OUT}=6200 µF, NO LOAD

Figure 27. Startup by V_{IN} (C_{OUT} = 6200 µF, 15 A, res. load)

V_{IN}=12 V, $C_{ON/PD}$=4.7 nF, NO C_{IN}, C_{OUT}=6200 µF, R_{OUT}=0.78Ω

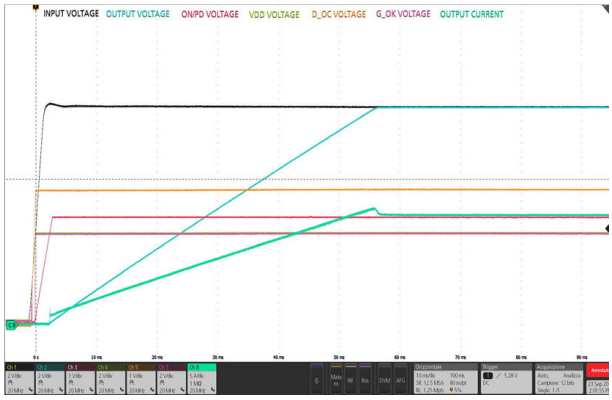


Figure 28. Startup by ON/PD (no load)

V_{IN}=12 V, NO C_{IN}, C_{OUT}=6800 µF, R_{LOAD}=0.7 Ω

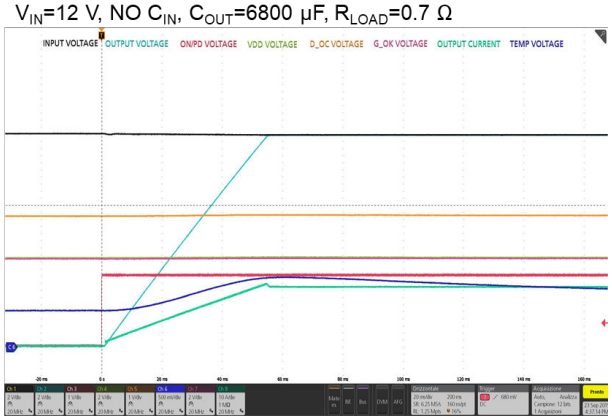


Figure 29. Shutdown by ON/PD (no load)

V_{IN}=12V, NO C_{IN}, C_{OUT}=6800µF, no Load

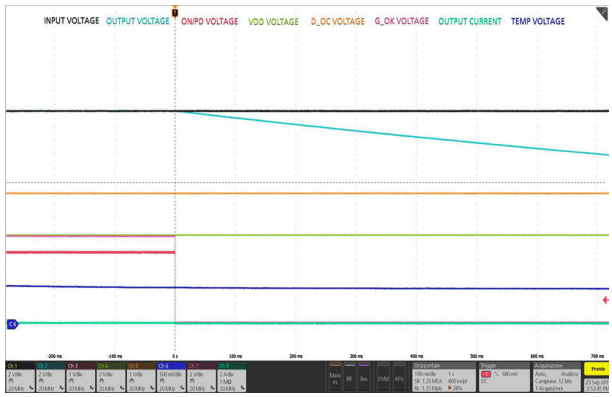


Figure 30. Startup by ON/PD (I_{OUT} = 15 A, C_{OUT} = 6800 µF)

V_{IN}=12V, NO C_{IN}, C_{OUT}=6800µF, no Load

Figure 31. Shutdown by ON/PD (I_{OUT} = 15 A, C_{OUT} = 6800 µF)

V_{IN}=12 V, NO C_{IN}, C_{OUT}=6800 µF, R_{LOAD}=0.7 Ω

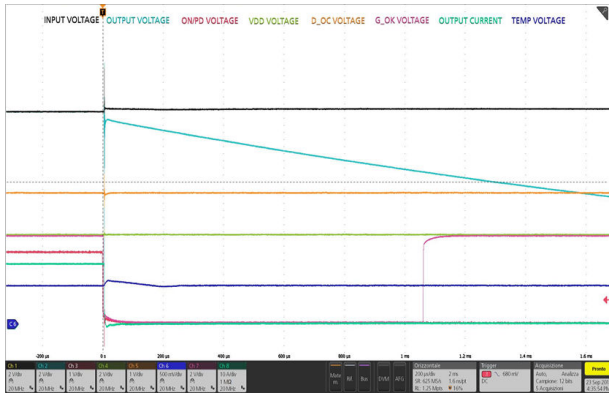


Figure 32. Startup into output short-circuit

V_{IN} = 12.5 V, $C_{ON/PD}$ = 200 nF , NO C_{IN}, NO C_{OUT}, R_{LOAD}=0 Ω, GOK=V_{DD}

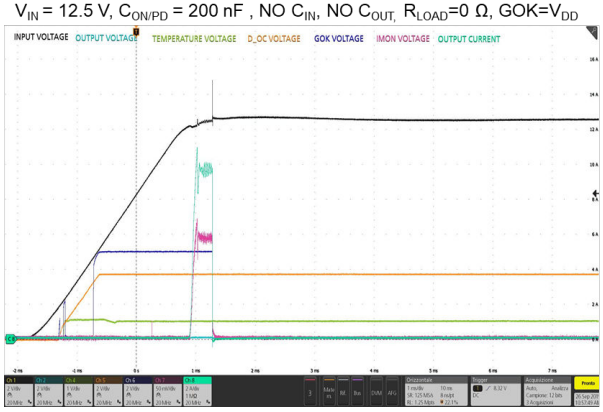


Figure 33. Output short-circuit during operation

V_{IN} = 12 V, V_{OUT} = from 12 V to 0 V, GOK=5 V , T_a=70 °C

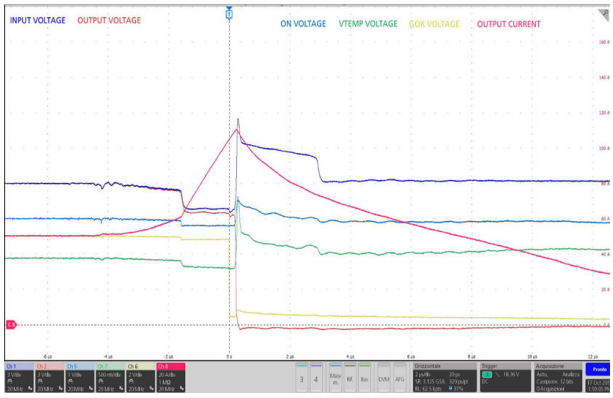


Figure 34. Overcurrent during operation

V_{IN} = 12V, R_{CS} = 2kΩ, R_{IMON} = 2kΩ, V_{CLREF} = 1.2V, I_{OUT} = from 0 to 81A, SR = 0.030A/µs

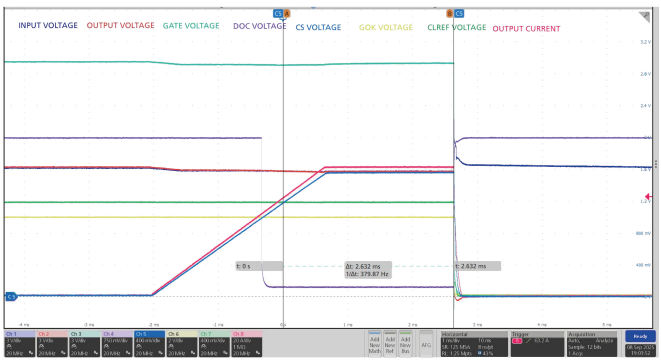
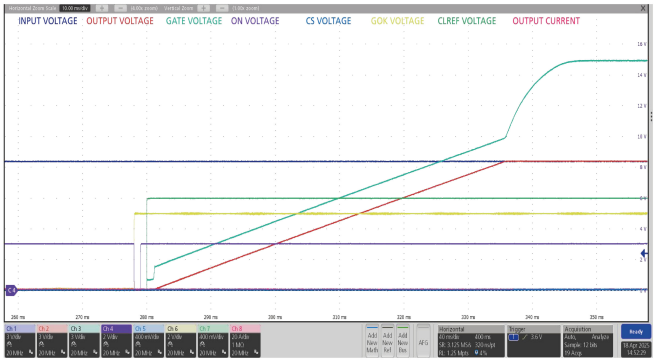


Figure 35. Device reset after fault

V_{IN} = from 0 to 12V, R_{CS} = 2kΩ, R_{IMON} = 2kΩ, V_{CLREF} = 1.2V, I_{OUT} = from 0 to 65A, SR = 0.001A/µs



8 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 QFN 32 (5 x 5) package information

Figure 36. **QFN 32 (5 x 5) package outline**

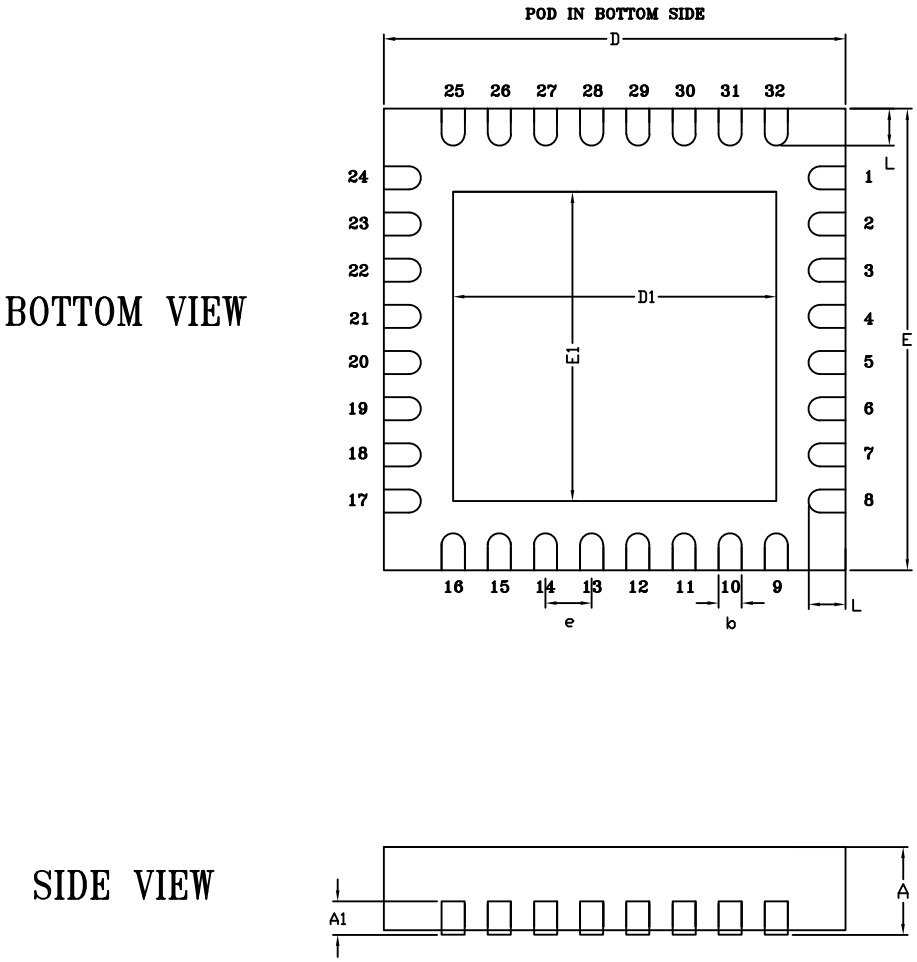
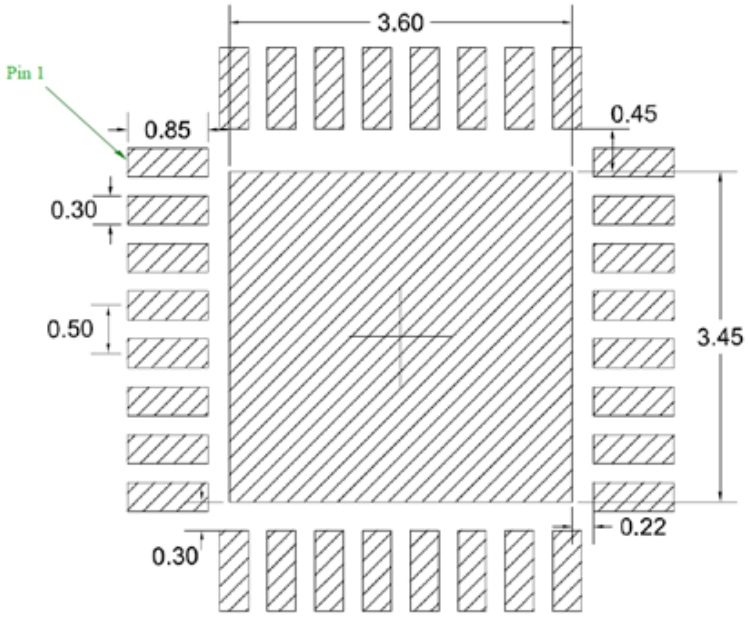


Table 7. **QFN 32 (5 x 5) package mechanical data**

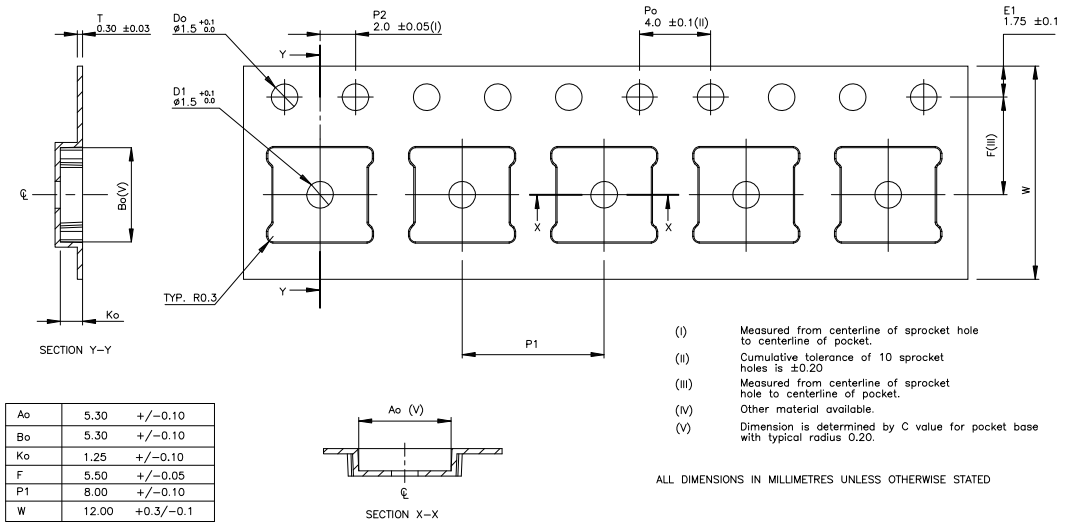
Dim.	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1
A1		0.20	
D	4.90	5.00	5.10
D1	3.40	3.50	3.60
E	4.90	5.00	5.10
E1	3.25	3.35	3.45
e		0.50	
b	0.20	0.25	0.30
L	0.30	0.40	0.50

Figure 37. **QFN 32 (5 x 5) recommended footprint**



8.2 QFN 32 (5 x 5) packing information

Figure 38. **QFN 32 (5 x 5) carrier tape**



Ao	5.30	+/−0.10
Bo	5.30	+/−0.10
Ko	1.25	+/−0.10
F	5.50	+/−0.05
P1	8.00	+/−0.10
W	12.00	+0.3/−0.1

Figure 39. **Pin 1 orientation in tape**

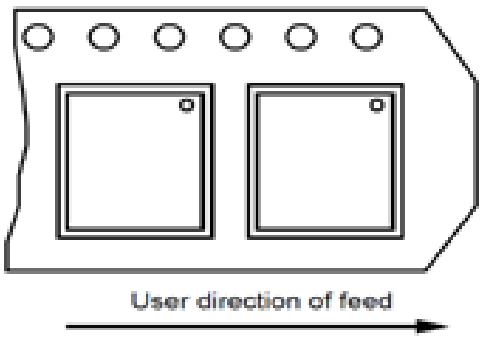


Figure 40. **QFN 32 (5 x 5) reel outline**

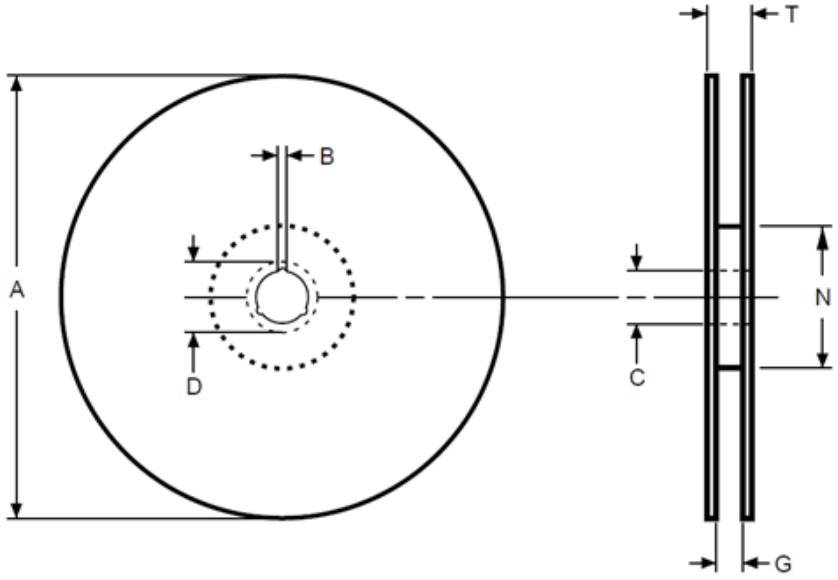


Table 8. **QFN 32 (5 x 5) reel data**

Reel size	Tape width	A (max.)	B (min.)	C	D (min.)	G (max.)	N (min.)	T (max.)	Unit
13”	0.90	330	1.5	13 ± 0.2	20.2	12.6	100	18.4	mm

9 Ordering information

Table 9. Order codes

Order code	Package	Packaging	Marking
STEF12H60GPUR	QFN32 (5 x 5)	Latch	EF12G60
STEF12H60GAPUR (1)		Auto-retry	EF12G60A

1. *Part number available on request. Contact our sales offices.*

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
15-Dec-2025	1	Initial release.

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