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STDRIVE141, STDRIVE121

Datasheet

Quad and dual half-bridge gate driver

STDRIVE

Product status link
STDRIVE141
STDRIVE121

Product label
SUSTAINABLE TECHNOLOGY

Features

- Operating voltage from 6 to 28 V
- Quad (STDRIVE141) and dual (STDRIVE121) half-bridge, or dual (STDRIVE141) and single (STDRIVE121) H-bridge, gate driver
- Adaptive MOSFET gate control:
  - Three steps gate control of external HS/LS
  - Programmable gate current up to 120 mA
- Two PWM inputs (up to 50 kHz)
- Low consumption mode (1.05 µA)
- Serial peripheral interface (SPI), 24 bits
- Full range of protections:
  - V_{DS} monitoring
  - Drain-source monitoring for short circuit detection
  - Overtemperature warning and shutdown
  - Timeout watchdog for MCU control
  - Detailed off-state diagnostic (open load, short circuit to supply or short circuit to GND) via SPI

Application

- Industrial automation
- CNC machines
- 3D printers
- Positioning systems
- Drones gimbal
- Robot vacuum cleaner and pool cleaner

Description

The STDRIVE141 is an integrated quad half-bridge gate driver designed to control up to eight N-channel MOSFETs. The STDRIVE121 is an integrated dual half-bridge gate driver designed to control up to four N-channel MOSFETs. These devices, together with the octal half-bridge STDRIVE181, extend the STDRIVE family.

A 24-bit serial peripheral interface (SPI) is used for configuring and controlling the half-bridges. SPI status registers provide high-level diagnostic information such as supply voltage monitoring, charge pump voltage monitoring, temperature warning, and overtemperature shutdown.

Each gate driver independently monitors its external MOSFET drain-source voltage for fault conditions.

A more efficient gate current control of the external MOSFETs, called “three stages gate current,” reduces switching losses and optimizes electromagnetic interference (EMI).

The device integrates a full range of protection features, such as drain-source monitoring for short circuit detection, overtemperature warning and shutdown, timeout watchdog for MCU control, and detailed off-state diagnostic via SPI.

Both the STDRIVE141 and STDRIVE121 are hosted in a VFQFN32L package with an exposed pad.

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1 Block diagram

Figure 1. **STDRIVE141 block diagram**

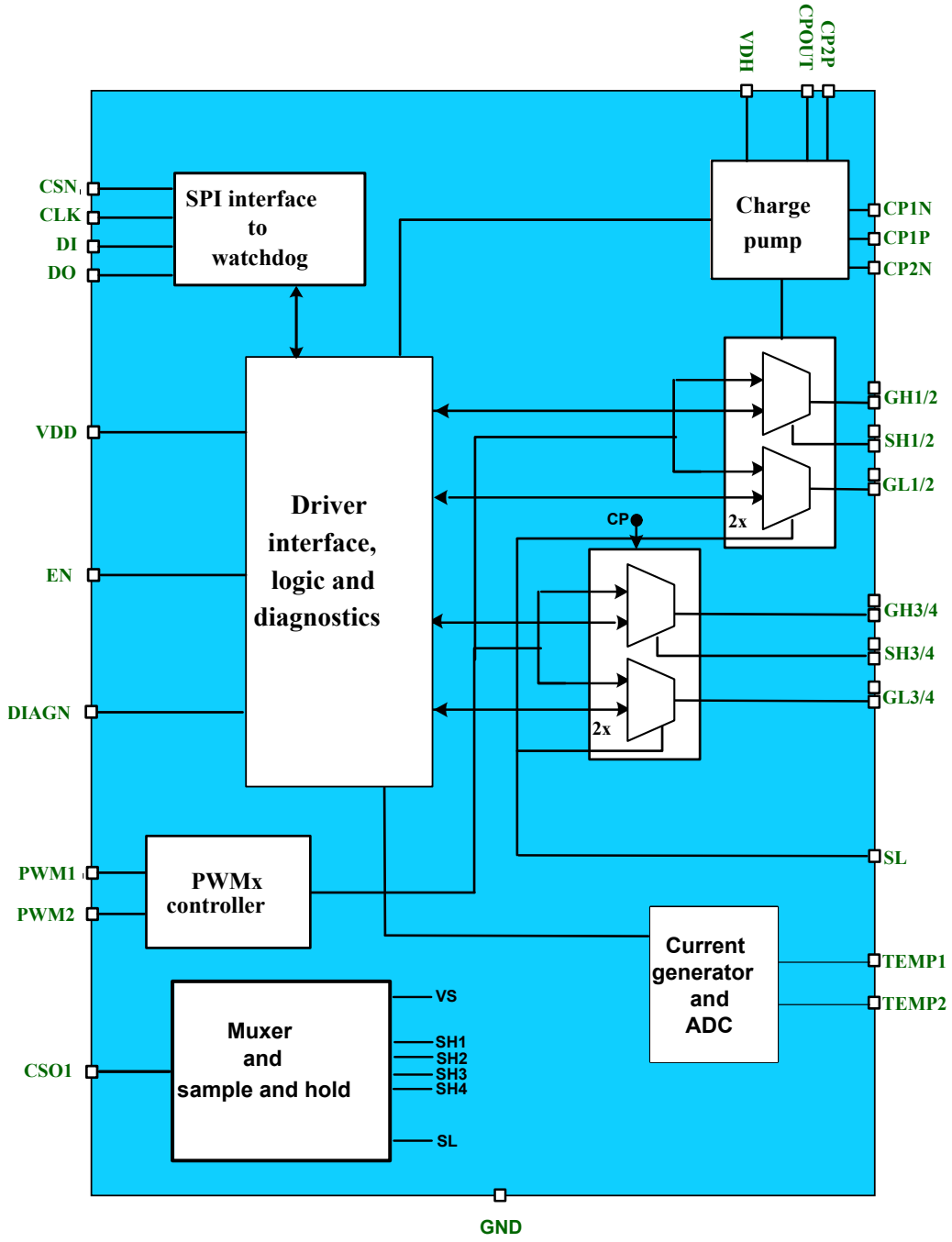
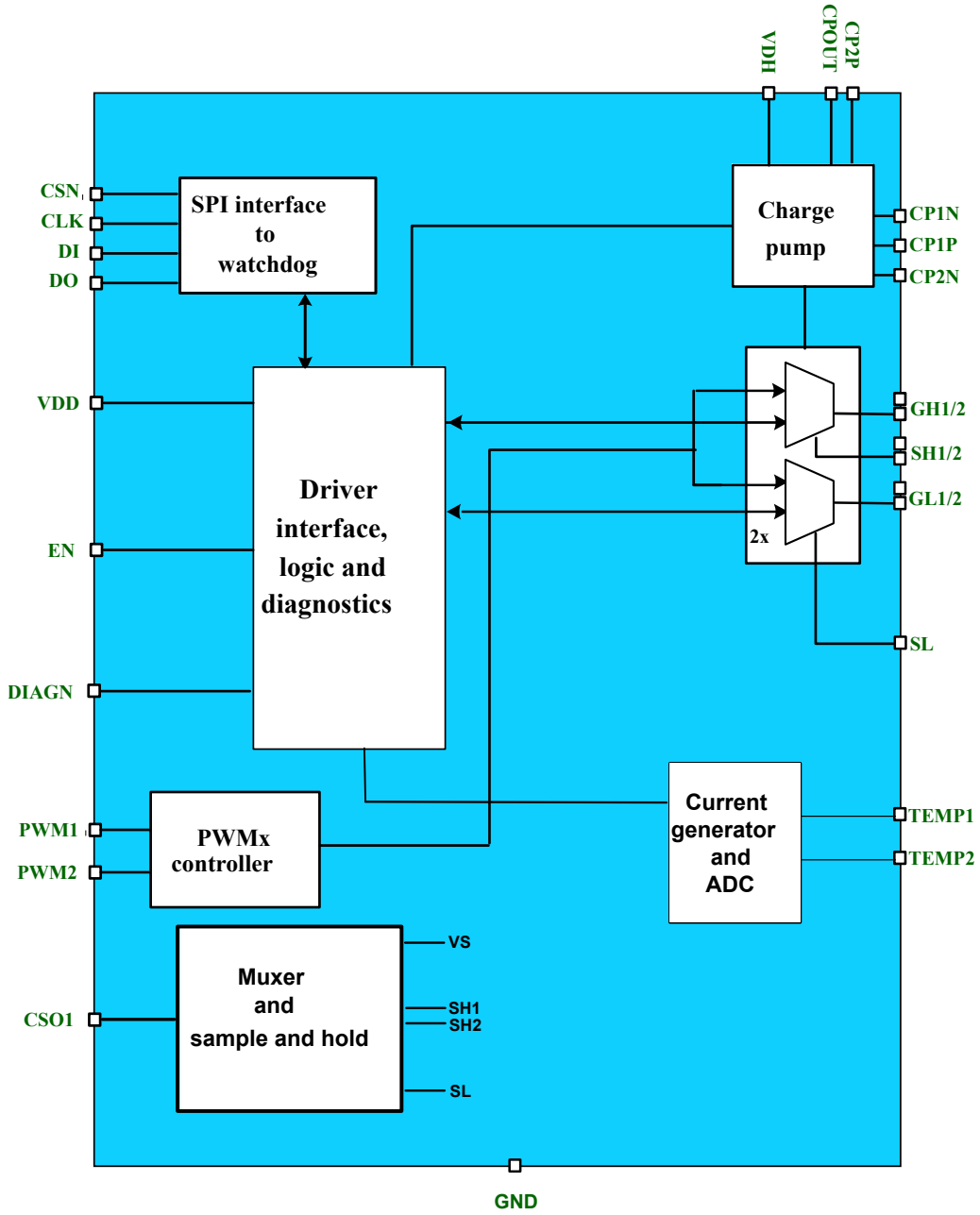


Figure 2. **STDRIVE121 block diagram**



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2 Pin description

Figure 3. STDRIVE141 - QFN32 pin connection (top view)

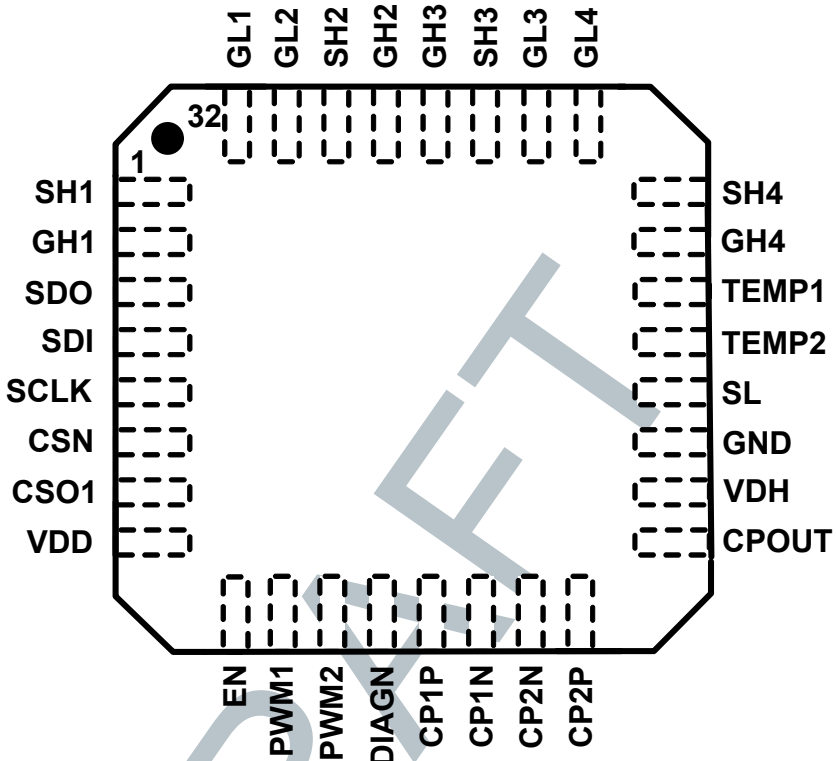

Figure 4. STDRIVE121 - QFN32 pin connection (top view)

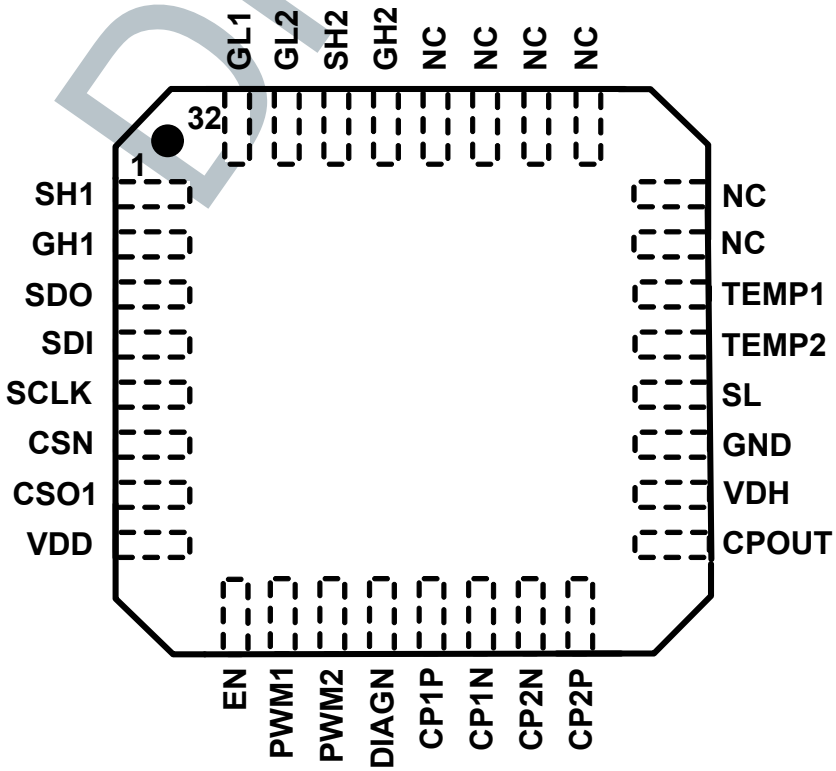

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Table 1. Pin function

#	Name	Function
1	SH1	SH1 source high-side 1: connection to source of high-side MOSFET 1
2	GH1	GH1 gate high-side 1: analog output pin to turn on/off high-side MOSFET 1. Connect to the gate of the high side
3	SDO	SDO serial data output
4	SDI	SDI serial data input with internal pull-down
5	SCLK	SCLK serial clock input with internal pull-down
6	CSN	CSN chip select with no internal pull-up
7	CSO1	CSO current sense amplifier output
8	VDD	VDD logic supply
9	EN	EN enables input with internal pull-down
10	PWM1	PWM1: PWM input 1
11	PWM2	PWM2: PWM input 2
12	DIAGN	DIAGN: diagnostic output NOT (active low)
13	CP1P	CP1P: positive connection to charge pump capacitor 1
14	CP1N	CP1N: negative connection to charge pump capacitor 1
15	CP2N	CP2N: negative connection to charge pump capacitor 2
16	CP2P	CP2P: positive connection to charge pump capacitor 2
17	CPOUT	CPOUT: charge pump output
18	VDH	VDH input pin
19	GND	GND ground connection
20	SL	SL source low-side: common connection to the source of the low-side MOSFETs
21	TEMP2	External temperature sensor 2
22	TEMP1	External temperature sensor 1
23	GH4	STDRIVE141 GH4 gate high-side 4: analog output pin to turn on/off high-side MOSFET 4. Connect to the gate of the high side
	NC	STDRIVE121 Not connected
24	SH4	STDRIVE141 SH4 source high-side 4: connection to source of high-side MOSFET 4
	NC	STDRIVE121 Not connected
25	GL4	STDRIVE141 GL4 gate low-side 4: analog output pin to turn on/off low-side MOSFET 4. Connect to the gate of the low side
	NC	STDRIVE121 Not connected
26	GL3	STDRIVE141 GL3 gate low-side 3: analog output pin to turn on/off low-side MOSFET 3. Connect to the gate of the low side
	NC	STDRIVE121 Not connected
27	SH3	STDRIVE141 SH3 source high-side 3: connection to source of high-side MOSFET 3
	NC	STDRIVE121

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#	Name	Function
27		Not connected
28	GH3	STDRIVE141 GH3 gate high-side 3: analog output pin to turn on/off high-side MOSFET 3. Connect to the gate of the high side
	NC	STDRIVE121 Not connected
29	GH2	GH2 gate high-side 2: analog output pin to turn on/off high-side MOSFET 2. Connect to the gate of the high side
30	SH2	SH2 source high-side 2: connection to source of high-side MOSFET 2
31	GL2	GL2 gate low-side 2: analog output pin to turn on/off low-side MOSFET 2. Connect to the gate of the low side
32	GL1	GL1 gate low-side 1: analog output pin to turn on/off low-side MOSFET 1. Connect to the gate of the low side
-	E.P.	Exposed pad connected to ground on the application board

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3 Device ratings

3.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 1 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_{DD}	Control logic supply voltage		-0.3 to 18	V
V_{DH}	Power stage supply voltage		-0.3 to 35	V
		Single pulse (t < 400 ms)	-0.3 to 40	V
V_{SH}	Voltage range at SH_x		-6 to V_{DH}	V
V_{IN}	Logic input voltage	All digital inputs excluded EN	-0.3 to V_{DD} + 0.3	V
		EN	-0.3 to 20	V
V_{SL}	Voltage range at SL		-6 to 6	V
V_{GH}	Voltage range at GH_x	V_{CPOUT} = +0.3 V	S_x - 0.3 to S_x + 13	V
V_{GL}	Voltage range at GL_x	V_{CPOUT} = +0.3 V	S_x - 0.3 to S_x + 13	V
V_{GS_HS}	Voltage drop between GH_x and SH_x		-0.3 to 13	V
V_{GS_LS}	Voltage drop between GL_x and SL_x		-0.3 to 13	V
V_{CP1N}, V_{CP2N}	Voltage range at CP1N and CP2N		-0.3 to V_{DH}	V
V_{CP1P}, V_{CP2P}	Voltage range at CP1P and CP2P		V_{DH} – 0.6 to V_{DH} + 13	V
V_{CPOUT}	Voltage range at CPOUT		V_{DH} – 0.6 to V_{DH} + 13	V
V_{CSO1}	Voltage range at CSO1		-0.3 to V_{DD} + 0.3	V
V_{TEMPx}	Voltage range at $TEMP_x$		-0.3 to 40	V
T_{stg}	Storage temperature		-55 to 150	°C
T_j	Junction temperature		-40 to 150	°C

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3.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{DD}	Control logic supply voltage		3	3.3	5.5	V
V_{DH} (1)	Power stage supply voltage		6		28	V
V_{SL}	SL operative range		-0.3		0.5	V
V_{SHx}	Output voltage		-0.3		V_{DH}	V
V_{IN}	Logic input voltage	Excluded EN	0		VDD	V
		EN	0		5	V
f_{PWM}	PWM switching frequency				50	kHz
C_{CP}	Boot capacitor			220		nF
C_{CPC1} C_{CPC2}	Charge pump capacitors			100		nF
T_{amb}	Ambient temperature		-40		85 (1)	°C

1. *The actual operating range depends on the application's heat dissipation performance.*

3.3 Electrical sensitivity

Table 4. ESD protection ratings

Symbol	Parameter	Test condition	Class	Value	Unit
HBM	Human Body Model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	H2	2	kV
CDM	Charge Device Model	All pins Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2a	500	V
		Corner pins only Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2	750	V
MM	Machine Model	Conforming to EIA/JESD22-A115-C	NC	200	V

3.4 Thermal data

Table 5. Thermal data

Symbol	Parameter	Test condition	Value	Unit
$R_{thj\text{-}amb}$ (1)	VFQFN32 thermal resistance junction to ambient (max.)		28.6	°C/W
$R_{thj\text{-}case}$ (2)	VFQFN32 thermal resistance junction to case (max.)		7.6	°C/W

1. *The parameter is retrieved according to JEDEC 51.2. Device mounted on a four-layer 2s2p PCB.*
2. *The $R_{thj\text{-}case}$ is retrieved according to MIL-STD-883E, referring to thermal testing method.*

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4 Electrical characteristics

Test conditions: V_{DH} = 6 V to 28 V; V_{DD} = 3.0 V to 5.5 V, T_j = -40 °C to 150 °C, all voltages are referenced to ground. Currents are defined as positive when flowing into the pin (unless otherwise specified).

Table 6. Supply, supply monitoring, and current consumption

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{DH_ext}	High-side drain voltage extended range (1)		5	-	6	V
I_{DD}	V_{DD} DC supply current	V_{DH} = 13.5 V V_{DD} = 5 V Active mode	3.5		7.5	mA
I_{DD_SDN}	V_{DD} quiescent supply current	V_{DD} = 5 V Reset mode	-	-	0.5	µA
I_{DH}	V_{DH} current consumption in active mode	V_{DH} = 13 V V_{DD} = 5 V Active mode Outputs floating	-	40	50	mA
I_{DH}	V_{DH} current consumption in active mode	V_{DH} = 6 V to 28 V V_{DD} = 5.0 V Active mode Outputs floating	-	48	60	mA
I_{DH_SDN}	V_{DH} quiescent supply current	V_{DH} = 13 V V_{DD} = 0 V Reset mode Outputs floating	-	-	0.55	µA
V_{DHUV}	V_{DH} undervoltage threshold	V_{DH}increasing/decreasing	4	-	4.5	V
V_{DHUV_hyst}	V_{DH} undervoltage hysteresis		0.04	-	0.2	V
V_{DHOVT1_LH}	V_{DH} overvoltage threshold 1 LH	V_{DH} increasing	19	-	21	V
V_{DHOVT1_HL}	V_{DH} overvoltage threshold 1 HL	V_{DH} decreasing	18.4	-	20.4	V
V_{DHOVT2_LH}	V_{DH} overvoltage threshold 2 LH	V_{DH} increasing	29	-	33	V
V_{DHOVT2_HL}	V_{DH} overvoltage threshold 2 HL	V_{DH} decreasing	28.5	-	32.5	V
V_{DHOV2_hyst}	V_{DH} overvoltage threshold 2 hysteresis	Guaranteed by design	-	0.8	-	V
V_{DHOV1_hyst}	V_{DH} overvoltage threshold 1 hysteresis	Guaranteed by design	-	0.65	-	V
t_{UV_FILT}	V_{DH} undervoltage filter time		7	10	13	µs
t_{OV_FILT}	V_{DH}/V_{DD} overvoltage filter time		7	10	13	µs
V_{DDOVT_LH}	V_{DD} overvoltage threshold LH		5.4	-	5.9	V
V_{DDOVT_HL}	V_{DD} overvoltage threshold HL		5.3	-	5.8	V
V_{DDhyst_OV}	V_{DD} overvoltage hysteresis		0.07	-	0.2	V
V_{DDPOR_OFF}	V_{DD} power-on-reset	V_{DD} increasing	2.40	2.60	2.80	V
V_{DDPOR_ON}	V_{DD} power-off-reset	V_{DD} decreasing	2.30	2.50	2.70	V

1. *Only functionality is guaranteed.*

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Table 7. Logic inputs PWMx, EN

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{ENH}	EN high voltage		0.9	-	2	V
V_{ENL}	EN low voltage		0.4	-	0.95	V
V_{ENHY}	EN hysteresis	(1)	0.45	-	0.95	V
$R_{PD\_OFF\_EN}$	EN pull-down resistor	EN pin below EN threshold	150	200	250.5	kΩ
$I_{PD\_ON\_EN}$	EN pull-down current	EN pin above EN threshold, additional current, pull-down resistor still present. Expected 80 µA + 25 µA with 5 V at EN pin	8.5	15	25	µA
V_{PWMH}	PWMx high voltage	(2)	1	-	2	V
V_{PWML}	PWMx low voltage	(3)	0.75	-	1.65	V
V_{PWMHY}	PWMx hysteresis	(1)	0.1	-	0.5	V
R_{PD_PWMx}	PWMx pull-down resistor		20	30	40	kΩ
f_{PWMH}	PWMH switching frequency	VDH = 13.5 V, VSLx = 0 V RG = 0 Ω, CG = 2.7 nF PWMH-duty-cycle = 50%	-	-	50	kHz

1. *Not subject to production test, specified by design.*
2. *High level is guaranteed above the max voltage.*
3. *Low level is guaranteed below the min voltage.*

Table 8. DIAGN outputs

V_{DH} = 6 V to 18 V

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage	I_{out} = 1 mA	-	-	0.4	V
V_{OH}	High-level output voltage	I_{out} = 1 mA	VDD - 0.4	-	-	V

Table 9. Charge pump

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
f_{CP}	Charge pump frequency	(1)	325	400	475	kHz
V_{CP}	Charge pump output voltage	V_{DH} ≥ 8 V I_{CP} ≥ -10 mA (2)	V_{DH} + 8.2	V_{DH} + 11.2	V_{DH} + 13	V
V_{CP_vbmin}	Charge pump output voltage	V_{DH} = 6 V I_{CP} = -5 mA (2)	V_{DH} + 6.2	V_{DH} + 7	-	V
V_{CP_low}	Charge pump low threshold voltage	(2)	V_{DH} + 4.5	V_{DH} + 5	V_{DH} + 5.5	V
I_{CP_lim}	Charge pump output current limitation (3)	V_{CP}= V_{DH} = 13.5 V	-36	-	-	mA
t_{CP}	Charge pump low filter time	Tested by scan	8	10	12	µs
t_{CP_blank}	Charge pump startup blanking time	Tested by scan	500	-	800	µs

1. *Not subject to production test, specified by design.*
2. *C_{CPC1} = C_{CPC2} = 100 nF, C_{CP} = 220 nF.*
3. *In case of a short to battery, this pin is not protected against a short to ground.*

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Table 10. Gate driver

$V_{CP} > V_{DH} + 8.5$ V.

The gate source and sink current level can be affected in case of high SHx/GHx slew rate due to capacitive current injected into the GATE pin from an external MOS miller capacitor. This behavior is described in a dedicated application note.

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 0000	-50%	-0.72	+50%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0000	-50%	0.88	+50%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 0001 ISTEP3_CONFx = 0000	-50%	-1.58	+50%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0001 ISTEP3_CONFx = 0000	-50%	1.77	+50%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 0010	-50%	-2.6	+50%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFX = ISTEP2_OFF_CONFx = 0010	-50%	2.6	+50%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 0011 ISTEP3_CONFx = 0001	-45%	-3.3	+45%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0011 ISTEP3_CONFx = 0001	-45%	3.5	+45%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 0100	-45%	-6	+45%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0100	-45%	6	+45%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 0101 ISTEP3_CONFx = 0010	-35%	-8	35%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0101 ISTEP3_CONFx = 0010	-35%	8	35%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 0110	-35%	-10	35%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0110	-35%	10	35%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 0111 ISTEP3_CONFx = 0011	-35%	-12	35%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 0111 ISTEP3_CONFx = 0011	-35%	12	35%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 1000	-35%	-16	35%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1000	-35%	16	35%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 1001 ISTEP3_CONFx = 0100	-35%	-20	35%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1001 ISTEP3_CONFx = 0100	-35%	20	35%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 1010	-35%	-24	35%	mA

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Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1010	-35%	24	35%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 1011 ISTEP3_CONFx = 0101	-35%	-28	35%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1011 ISTEP3_CONFx = 0101	-35%	28	35%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 1100	-35%	-32	35%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1100	-35%	32	35%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 1101 ISTEP3_CONFx = 0110	-35%	-36	35%	mA
I_{Toffx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1101 ISTEP3_CONFx = 0110	-35%	36	35%	mA
I_{onx}	Gate source current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_CONFx = 1110	-35%	-40	35%	mA
I_{offx}	Gate sink current, only I_{STEP1x} and I_{STEP2x}	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1110	-35%	40	35%	mA
I_{onx}	Gate source current	ISTEP1_CONFx = ISTEP2_CONFx = 1111 ISTEP3_CONFx = 0111	-25%	-42	+25%	mA
I_{offx}	Gate sink current	ISTEP1_CONFx = ISTEP2_OFF_CONFx = 1111 ISTEP3_CONFx = 0111	-25%	37	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1000	-25%	-52	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1000	-25%	52	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1001	-25%	-60	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1001	-25%	60	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1010	-25%	-68	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1010	-25%	68	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1011	-25%	-76	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1011	-25%	76	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1100	-25%	-84	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1100	-25%	84	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1101	-25%	-92	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1101	-25%	92	+25%	mA

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Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1110	-25%	-104	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1110	-25%	104	+25%	mA
I_{onx}	Gate source current only I_{STEP3x}	ISTEP3_CONFx = 1111	-25%	-120	+25%	mA
I_{offx}	Gate sink current only I_{STEP3x}	ISTEP3_CONFx = 1111	-25%	120	+25%	mA
V_{GSHx}	Gate-on voltage	VDH = VSH = 6 V ICP = -5 mA, DC measure GH-SH	VSHx + 6	-	-	V
V_{GSHx}	Gate-on voltage	VDH = VSH >= 8 V ICP = -10 mA, DC measure GH-SH	VSHx +- 8	VSHx + 10	VSHx + 12	V
R_{GHx}	Passive gate-pull-down resistance	Resistance between gate HS and ground when device is ON	-	1	-	MΩ
R_{SHx}	Passive source-pull-down resistance	Resistance between source HS and ground when device is ON	-	1	-	MΩ
V_{GLx}	Gate-on voltage	VSL = 0 V, VDH = 6 V ICP = -5 mA, DC measure GL-SL	VSLx + 6	-	-	V
V_{GLx}	Gate-on voltage	VSL = 0 V, VDH ≥ 8 V ICP = -10 mA, DC measure GL-SL	VSLx + 8	VSLx + 10	VSLx + 12	V
R_{GLx}	Passive gate-pull-down resistance	Resistance between gate LS and ground when device is ON	-	1	-	MΩ
R_{SL}	Passive source-pull-down resistance	Resistance between source LS and ground when device is ON	-	125	-	KΩ
$V_{step1xl}$	Step voltage1 for x channel x = 1…8	VSTEP1_CONFx = 00/01 Switch ON, command = 1	-55%	1.1	+55%	V
$V_{step1xh}$	Step voltage1 for x channel x = 1…8	VSTEP1_CONFx = 00/01 Switch OFF command = 0	-47%	1.3	+47%	V
$V_{step1xl}$	Step voltage1	VSTEP1_CONFx = 10/11 Switch ON, command = 1	-35%	2.2	+35%	V
$V_{step1xh}$	Step voltage1	VSTEP1_CONFx = 10/11 Switch OFF command = 0	-35%	2.6	+35%	V
$V_{step2xl}$	Step voltage2	VSTEP2_CONFx = 00 Switch ON, command = 1	-31%	2.67	+31%	V
$V_{step2xh}$	Step voltage2	VSTEP2_CONFx = 00 Switch OFF command = 0	-28%	3.33	+28%	V
V_{step2x}	Step voltage2	VSTEP2_CONFx = 01 Switch ON, command = 1	-27%	3.56	+27%	V
$V_{step2xh}$	Step voltage2	VSTEP2_CONFx = 01 Switch OFF command = 0	-25%	4.44	+25%	V
$V_{step2xl}$	Step voltage2	VSTEP2_CONFx = 10 Switch ON, command = 1	-24%	4.45	+24%	V
$V_{step2xh}$	Step voltage2	VSTEP2_CONFx = 10 Switch OFF command = 0	-24%	5.55	+24%	V
$V_{step2xl}$	Step voltage2	VSTEP2_CONFx = 11 Switch ON, command = 1	-24%	5.34	+24%	V
$V_{step2xh}$	Step voltage2	VSTEP2_CONFx = 11 Switch OFF command = 0	-24%	6.66	+24%	V

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Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Gate drivers dynamic parameters						
t_{GLxr}	Rise time LS	VDH = 13.5 V; VSLx = 0 V RG = 0 Ω; CG = 10 nF	-	-	2.1	µs
t_{GHxr}	Rise time HS	VDH = 13.5 V; VSLx = 0 V RG = 0 Ω; CG = 10 nF	-	-	2.1	µs
t_{GLxf}	Fall time LS	VDH = 13.5 V; VSLx = 0 V RG = 0 Ω; CG = 10 nF	-	-	2.1	µs
t_{GHxf}	Fall time HS	VDH = 13.5 V; VSLx = 0 V RG = 0 Ω; CG = 10 nF	-	-	2.1	µs
V_{GSHx}	Gate-on voltage HS	Maximum VGH-VSH in turn-on condition	-	-	VSHx + 13	V
V_{GSLx}	Gate-on voltage LS	Maximum VGL-VSL in turn-on condition	-	-	VSLx + 16	V

Figure 5. H-driver delay times

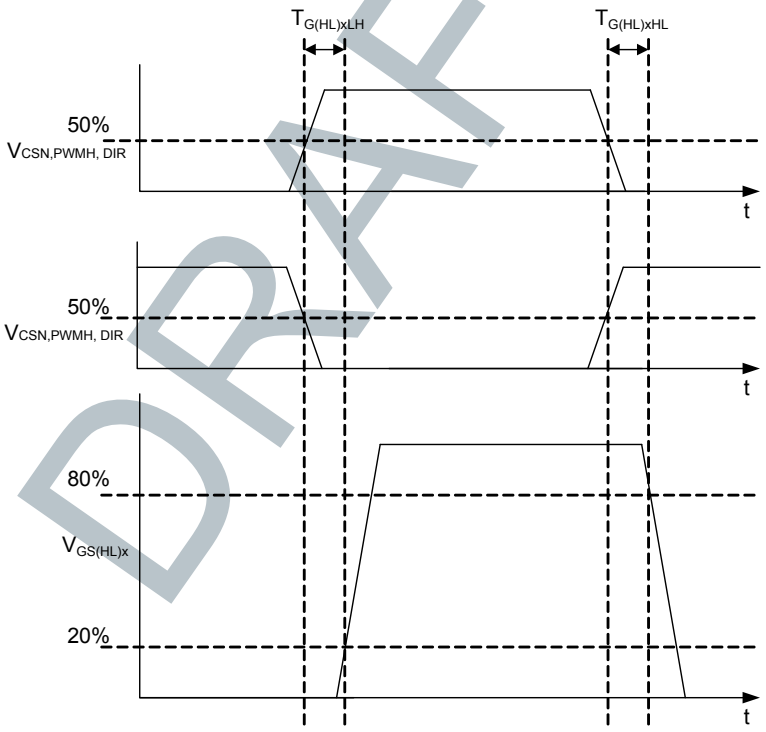

Table 11. Watchdog

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{LOW}	Long open window	Guaranteed by scan	52	-	87	ms
t_{CW}	Closed window	Guaranteed by scan	11	-	20	ms
t_{WDP}	Watchdog period	Guaranteed by scan	32	-	54	ms
$t_{timeout}$	Timeout period	Guaranteed by scan	90	-	110	ms

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Figure 6. **Watchdog early, late, and safe window**

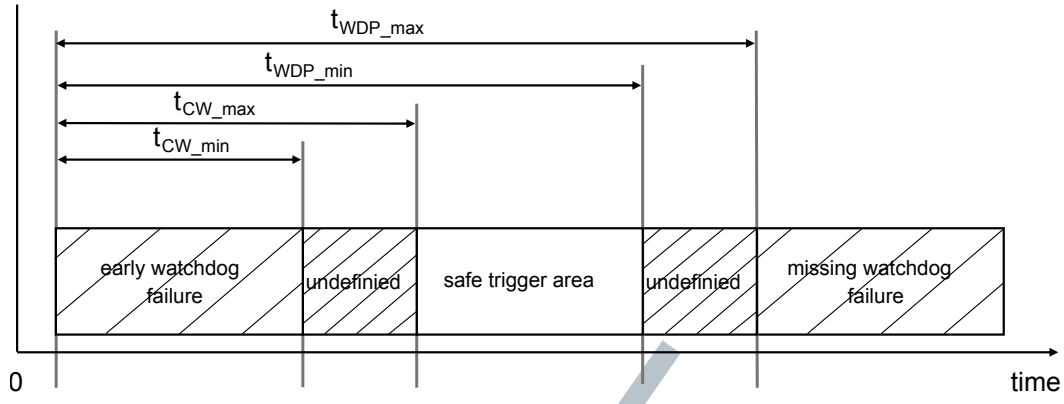

Table 12. **Open-load monitoring threshold**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{ODLS}	Low-side drain-source monitor off-state threshold voltage	VDH = 13.5 V VDS_CONFx = 1xxx or (HB_MODEx = 00, OUTEx = 1)	1.5	1.8	2.1	V
V_{ODHS}	High-side drain-source monitor off-state threshold voltage	VDH = 13.5 V VDS_CONFx = 1xxx or (HB_MODEx = 00, OUTEx = 1)	1.5	1.8	2.1	V
V_{SHx_OL}	Output voltage of selected SHx in open-load test mode	VSLx = 0 V; VDH = 13.5 V	2.1	3	3.9	V
I_{shx_PU}	Pull-up current in DIAG OFF	VSHx = 0 V; VDH = 13.5 V DIAGOFF_CURR_SEL = 0	0.5	0.9	1.25	mA
I_{shx_PU}	Pull-up current in DIAG OFF	VSHx = 0 V; VDH = 13.5 V DIAGOFF_CURR_SEL = 1	1.2	1.6	2.4	mA
I_{shx_PD}	Pull-down current in DIAG OFF	VSHx = 3 V; VDH = 13.5 V DIAGOFF_CURR_SEL = 0	200	300	400	µA
I_{shx_PD}	Pull-down current in DIAG OFF	VSHx = 3 V; VDH = 13.5 V DIAGOFF_CURR_SEL = 1	400	600	800	µA
t_{diag}	DIAG OFF time		130	200	270	µs

Table 13. **Drain-source monitoring**

$V_{CP} > V_{DH} + 8.5$ V

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{SCd0}	Drain-source monitoring threshold	VDS_CONFx = 0000	0.045	0.08	0.095	V
V_{SCd1}	Drain-source monitoring threshold	VDS_CONFx = 0001	0.12	0.16	0.18	V
V_{SCd2}	Drain-source monitoring threshold	VDS_CONFx = 0010	0.16	0.20	0.24	V
V_{SCd3}	Drain-source monitoring threshold	VDS_CONFx = 0011	0.20	0.25	0.30	V
V_{SCd4}	Drain-source monitoring threshold	VDS_CONFx = 0100	0.24	0.30	0.36	V
V_{SCd5}	Drain-source monitoring threshold	VDS_CONFx = 0101	0.32	0.40	0.48	V
V_{SCd6}	Drain-source monitoring threshold	VDS_CONFx = 0110	0.40	0.50	0.62	V

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Symbol	Parameter	Test condition	Min	Typ	Max	Unit
V_{SCd7}	Drain-source monitoring threshold	VDS_CONFx = 0111	0.48	0.60	0.72	V
t_{B0000}	DS monitoring blank time	VDS_BLANKx = 0000	0.5	0.625	0.85	µs
t_{B0001}	DS monitoring blank time	VDS_BLANKx = 0001	0.8	1	1.2	µs
t_{B0010}	DS monitoring blank time	VDS_BLANKx = 0010	1	1.25	1.5	µs
t_{B0011}	DS monitoring blank time	VDS_BLANKx = 0011	1.2	1.5	1.8	µs
t_{B0100}	DS monitoring blank time	VDS_BLANKx = 0100	1.6	2	2.4	µs
t_{B0101}	DS monitoring blank time	VDS_BLANKx = 0101	2.4	3	3.6	µs
t_{B0110}	DS monitoring blank time	VDS_BLANKx = 0110	3.2	4	4.8	µs
t_{B0111}	DS monitoring blank time	VDS_BLANKx = 0111	4	5	6	µs
t_{B1000}	DS monitoring blank time	VDS_BLANKx = 1000	4.8	6	7.2	µs
t_{B1001}	DS monitoring blank time	VDS_BLANKx = 1001	5.6	7	8.4	µs
t_{B1010}	DS monitoring blank time	VDS_BLANKx = 1010	6.4	8	9.6	µs
t_{SCS}	Drain-source comparator propagation delay	VDH = 14 V VDS jump from 10 mV to 1 V, time from filter time end to VGS external FET under threshold without external MOSFETs (1)		-	1	µs
t_{FT000}	DS monitoring filter time (1)	VDS_FILTx = 000	0.4	0.5	0.85	µs
t_{FT001}	DS monitoring filter time (1)	VDS_FILTx = 001	0.8	1	1.4	µs
t_{FT010}	DS monitoring filter time (1)	VDS_FILTx = 010	1.6	2	2.4	µs
t_{FT011}	DS monitoring filter time (1)	VDS_FILTx = 011	2.4	3	3.6	µs
t_{FT100}	DS monitoring filter time (1)	VDS_FILTx = 100	3.2	4	4.8	µs
t_{FT101}	DS monitoring filter time (1)	VDS_FILTx = 101	4	5	6	µs
t_{FT110}	DS monitoring filter time (1)	VDS_FILTx = 110	4.8	6	7.2	µs

1. *Not subject to production test, specified by design.*

Note: If the VDS_BLANKx = 1x11, the default value (VDS_BLANKx = 0000) is set.

Note: If the VDS_FILTx = 111, the default value (VDS_FILTx = 000) is set.

Table 14. Cross current protection time

$V_{CP} > V_{DH} + 8.5$ V
Not subject to production test, specified by design.

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
tDT000	Cross-current protection time	Tested by scan, DTP_REF = 0 (1)	350	500	650	ns
tDT001	Cross-current protection time	Tested by scan, DTP_REF = 0 (1)	0.8	1	1.2	µs
tDT010	Cross-current protection time	Tested by scan, DTP_REF = 0 (1)	1.6	2	2.4	µs
tDT011	Cross-current protection time	Tested by scan, DTP_REF = 0 (1)	2.4	3	3.6	µs
tDT100	Cross-current protection time	Tested by scan, DTP_REF = 0 (1)	3.2	4	4.8	µs
tDT101	Cross-current protection time	Tested by scan, DTP_REF = 0 (1)	4	5	6	µs
tDT110	Cross-current protection time	Tested by scan, DTP_REF = 0 (1)	4.8	6	7.2	µs
tDT111	Cross-current protection time	Tested by scan, DTP_REF = 0 (1)	12.8	16	19.2	µs

1. *When DTP_REF = 1, it is necessary to add 850 ns to the maximum value.*

Table 15. External temperature sensor

$V_{CP} > V_{DH} + 8.5$ V

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{SENSOR}	Sensor current	ITEMP_CONFx = 00	200	250	300	µA
I_{SENSOR}	Sensor current	ITEMP_CONFx = 01	400	500	600	µA
I_{SENSOR}	Sensor current	ITEMP_CONFx = 10	600	750	900	µA
I_{SENSOR}	Sensor current	ITEMP_CONFx = 11	800	1000	1200	µA
$V_{sensinc}$	Sensor voltage range		0.3	-	2	V
-	ADC nbit		-	11	-	bit
-	ADC offset error		-2	-	+2	mV
-	ADC gain error vs temp		-	-	+1.5	%
-	ADC total gain error		-2.5	-	+2.5	%

Table 16. SPI parameters

$V_{CP} > V_{DH} + 8.5$ V

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
DC parameters						
V_{IL}	Low-level input voltage		0.75	-	1.65	V
V_{IH}	High-level input voltage		0.85	-	1.75	V
V_{ihyst}	Input voltage hysteresis		0.1	-	0.5	V
$I_{CSN\ in}$	CSN pull-up current input	Probe current on force input pin at VHL voltage in DC conditions	20	40	60	uA
$I_{SDI\ in}$	SCLK, SDI pull-down current input	Probe current on force input pin at VIL voltage in DC conditions	20	40	60	µA
$V_{SDO\ low}$	SDO output low voltage	ISDO out = 1 mA	-	-	0.4	V
$V_{SDO\ high}$	SDO output high voltage	ISDO out = 1 mA 3.0 V ≤ VDD ≤ 5.5 V	VDD - 0.4	-	-	V
$I_{SDO\ leak}$	SDO tristate leakage current	VCSN ≥ 2 V 0 V ≤ VSDO IN ≤ VDD	-10	-	10	µA
AC parameters						
f_{CLK}	Clock frequency	CSDO = 50 pF	-	-	6	MHz
t_{CLK}	Clock period	CSDO = 50 pF	166	-	-	ns
t_1 (1)	Clock high time		75	-	-	ns
t_2 (1)	Clock low time		75	-	-	ns
t_3 (1)	CLK low before CSN active		20	-	-	ns
t_4 (1)	CLK active after CSN active		100	-	-	ns
t_5 (1)	CLK passive before CSN passive		100	-	-	ns
t_6 (1)	SDI setup time		30	-	-	ns
t_7	SDI hold time		30	-	-	ns
t_8 (1)	SDO active after CSN active	CSDO = 50 pF	-	-	100	ns
t_9 (1)	SDO tristate after CSN passive	CSDO = 50 pF	-	-	100	ns
t_{10} (1)	SDO valid time	CSDO = 50 pF	-	-	70	ns

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Symbol	Parameter	Test condition	Min	Typ	Max	Unit
t_{11} (1)	SDO hold time	CSDO = 50 pF	10	-	-	ns
t_{12} (1)	SDO rise time	CSDO = 50 pF	-	-	50	ns
t_{13} (1)	SDO fall time	CSDO = 50 pF	-	-	50	ns
t_{14} (1)	CSN passive time to next frame		600	-	-	ns
t_{15}	CLK passive time to next		100	-	-	ns
t_{16} (1)	SDI data of next frame		20	-	-	ns
t_{CSN_fail}	CSN low timeout	Tested by scan	20	35	50	ms
t_{START}	Time at the startup before a correct SPI frame can be received	Tested by scan	-	-	300	µs

1. *See Figure 27.*

Table 17. CSO parameters

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$CSO_{TOT\_error\_CHx\_50mV}$	Total error 50 mV	VDS HS or LS forces 50 mV, gain selected 10x1.5 (1) validates also for gain 10x3	-4.6	-	4.6	mV
$CSO_{TOT\_error\_CHx\_50mV}$	Total error 100 mV	VDS HS or LS forces 100 mV, gain selected 10x1.5 (1) validates also for gain 10x3	-4.85	-	4.85	mV
$CSO_{TOT\_error\_CHx\_150mV}$	Total error 150 mV	VDS HS or LS forces 150 mV, gain selected 2.5x3	-10.5	-	10.5	mV
$CSO_{TOT\_error\_CHx\_450mV}$	Total error 450 mV	VDS HS or LS forces 450 mV, gain selected 2.5x3	-10.5	-	10.5	mV
CSO_{InR_A}	VDS reading input voltage Range A		10	-	140	mV
CSO_{InR_B}	VDS reading input voltage Range B		120	-	450	mV
CSO_{OutR_A}	VDS reading output voltage Range A	(1)	0.1	-	V_{DD} - 0.3	V
CSO_{OutR_B}	VDS reading output voltage Range B	(1)	0.3	-	V_{DD} - 0.3	V
$CSO_{Setting}$	VDS reading output setting time	Out from 0.1 V to 2 V (C = 1 nF)	-	-	10	µs

1. *Not subject to production test, specified by design.*

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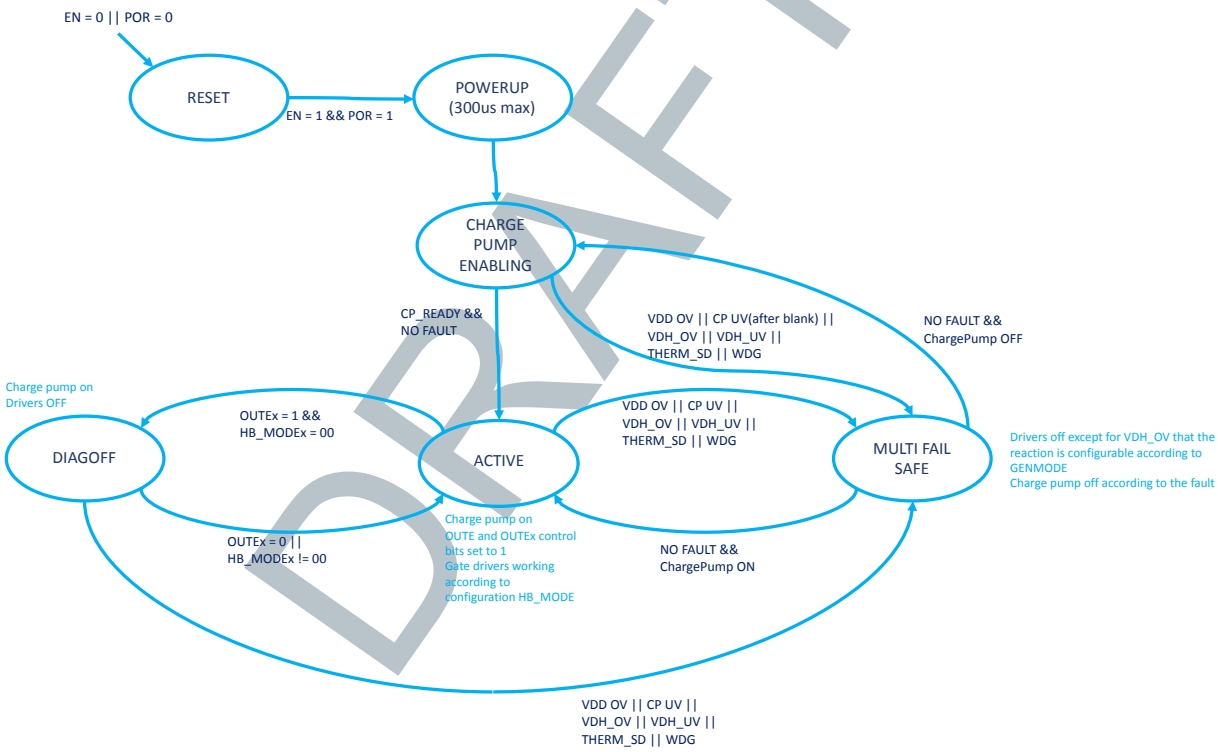
5 Functional description

5.1 Power supply

The device has two supply input pins. VDH is the supply input for the charge pump that powers the MOSFET gate drivers. VDD is the supply input for the internal voltage regulator, which powers the logic circuitry, I/Os, the amplifier's output stage for VDS measurement, and the temperature sensor reading. This voltage has to be the same as the application microcontroller supply (for example, 3.3 V or 5 V). When both VDD and VDH are provided to the device, the power supply for the internal regulators for logic is taken from the VDD power pin. None of the supply input pins are internally protected against negative voltage. The VDD supply input can tolerate a short to battery condition up to its absolute maximum rating. The decoupling capacitors on the VDD and VDH pins must be placed as close as possible.

5.2 Operation modes

Figure 7. Main operating modes



5.2.1 Reset

The device exits reset mode and enters a power-up state as soon as the EN pin is high and the V_{DD} rises above V_{DDPOR_OFF} (increasing phase). If V_{DD} falls below V_{DDPOR_ON} (decreasing phase) while the EN pin is still high, the device experiences a power-on reset and enters reset mode.

In this device, all register contents are reset to their default values. Once the device exits reset mode, the global status RSTB bit is set, indicating that all the device registers have been reset to their default values. This bit is automatically cleared by any valid SPI communication frame (after power-up state).

When the EN input pin is left floating (due to the internal pull-down resistor), the device enters (if not already in) reset mode, minimizing its current consumption. When the device is in reset mode, to ensure that a minimum current is drawn from V_{DH} (less than I_{DD_SDN}), CSN must be high (SDO in tristate), and the EN input pin must be low. In reset mode, the gate drivers together with the charge pump are switched off, all the MOSFETs are passively switched off via the internal resistive path between gate and source, and all registers are reset to their default values.

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5.2.2 Power-up state and charge pump enabling

When the device exits the reset state, before reaching the active state, it passes through an intermediate state called the power-up state. During this state, it is not possible to guarantee a proper SPI communication for a duration of t_{START}.

When the charge pump start-up phase ends (charge pump enabling state), the device reaches the active state. The start-up phase duration is t_{CP_start}.

5.2.3 Active mode and "diag off" condition

In active mode, the diagnostic is available. The charge pump is enabled if VDH > VDHUV, the gate drivers are enabled if the OUTEx (x = 1...4 for STDRIVE141 or x = 1...2 for STDRIVE121) control bits are set, and the master enable OUTE bit in GLOBAL_CFG register is set. If the OUTEx control bits are reset, or the OUTE bit is reset, all the gate drivers are low, and the external MOSFETs are strongly shut off through the internal predriver pull-down. There are additional passive pull-down resistors connected between gate and GND and between source and GND of each MOSFET.

Once the OUTEx control bit is set, the HS and LS MOSFETs can be driven according to the configuration of the 2-bit HB_MODEx registers (seeTable 18)

Table 18. HB_MODEx register settings

HB_MODEx	Setting
00	LS and HS of the half-bridge x are kept in DIAG OFF state (default)
01	LS of the half-bridge x is ON (static, no PWM), HS of the half-bridge x is OFF
10	HS of the half-bridge x is ON (static, no PWM), LS of the half-bridge x is OFF
11	LS or HS of the half-bridge x is ON according to the HB_PWMx register

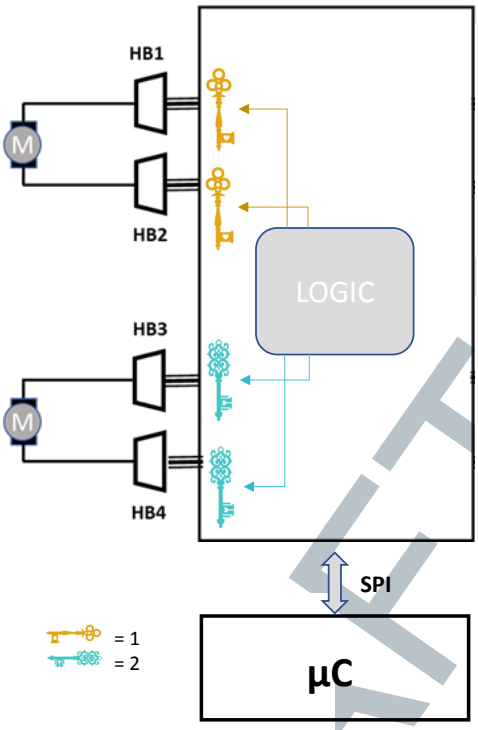
All configurations shall be changed while the diagnosis/channel is not active.

5.2.4 Multi fail-safe mode

The STDRIVE141 and the STDRIVE121 integrate a so called “multi fail-safe mode”, an automatic system that passively switches off the gate drivers to protect the device and the application in the event of a fault, according to the register settings.

In the event of a fault due to V_{ds} monitoring, the half-bridge in which the V_{ds} monitoring failure occurred is switched off. Setting the HB_FAULTx register, the user can assign a key to each half-bridge (see Figure 8). As a consequence, all the half-bridges with the same key are also turned off. All the other half-bridges are unaffected.

Figure 8. **Example of a possible fault key configuration in STDRIVE141**



5.2.5 Operational matrix

When a fault condition is detected, the behavior of the device depends on the type of the fault. The Table 19 summarizes which feature is turned off and which one remains active after a fault event.

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Table 19. Reset matrix

Functions/ faults or input	Enable pin low	VDD under POR	VDD overvoltage	VDH overvoltage	VDH undervoltage	Thermal warning	Thermal shutdown	Charge pump over UV that power-up (not ready)	Charge pump UV (CP UV FAULT)	Watchdog	VDSx monitoring	SPI error
SPI	X	X	X(1)	O	O	O	O	O	O	O	O	O
Watchdog	X	X	X(2)	O	O	O	O	O	O	O	O	O
Diagnostic logic	X	X	X	O	O	O	O	O	O	O	O	O
Register map	X	X	O	O	O	O	O	O	O	O(3)	O	O
PWM controller	X	X	X	X	X	O	X	X	X	X	X	O
DIAGN	X	X	A	A	A	A	A	A	A	A	A	A
Indirect current measurement system	X	X	X	X	X	O	X	X	X	X	O	O
Current generator and ADC for temperature measurement	X	X	X	X	X	O	X	X	X	X	O	O
Gate drivers	X	X	X	C	X	O	X	X	X	X	X(4)	O
Charge pump	X	X	X	O	O	O	X	X(5)	O	X	O	O

1. *SDO, DIAGN, and CSO1 outputs are low.*
2. *After a VDDOV event, the watchdog restarts with a long open window and must be reprogrammed.*
3. *The OUTEx registers are reset.*
4. *The half-bridge in which the failure occurred, together with all half-bridges connected to the one that failed, is turned off.*
5. *In the case of a charge pump not ready, the CP is in power-up phase.*

Note:

- *X = Power-off*
- *O = Normal operation*
- *A = Active*
- *C = All the MOSFETs are disabled if GENMODEx = 0*
  All the HS MOSFETs are disabled and LS MOSFETs are ON to brake the motor if GENMODEx = 1
  All the MOSFETs are ON if GENMODEx = 2

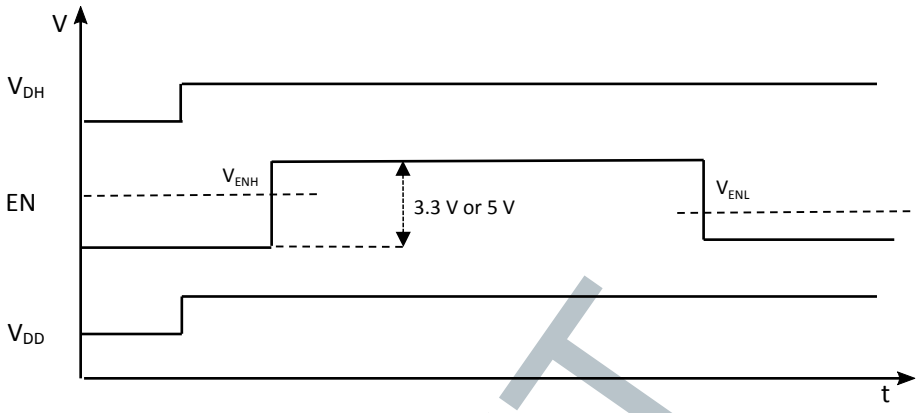
5.2.6 Power-up sequence

The power-up sequences that must be followed to turn on STDRIVE141 or STDRIVE121 are reported below.

The first possible power-on sequence is shown in Figure 9. V_{DH} and V_{DD} are raised while the EN pin is low. After the V_{DH} and V_{DD} pins are high and stable, the EN pin is set to turn on the device or reset to turn it off. The device turns on when the EN pin exceeds the rising V_{ENH} threshold and turns off when it drops below the falling V_{ENL} threshold.

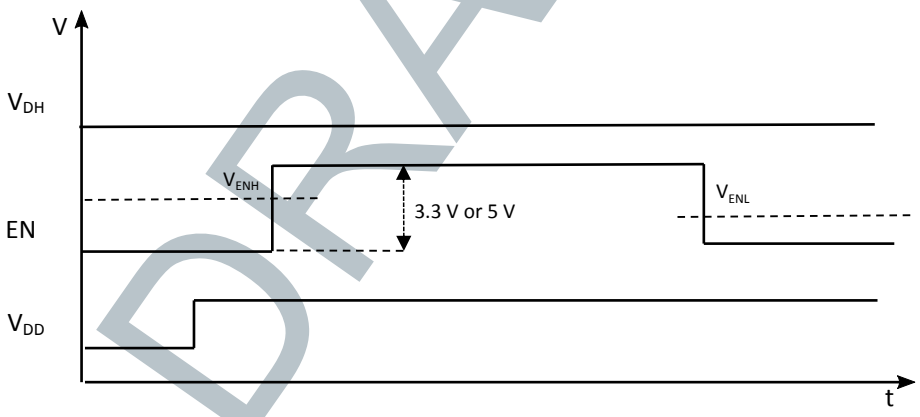
The fastest possible slew rate for V_{DD} is 100 µs at 3.3 V.

Figure 9. V_{DH} and V_{DD} high, EN pin goes high and low



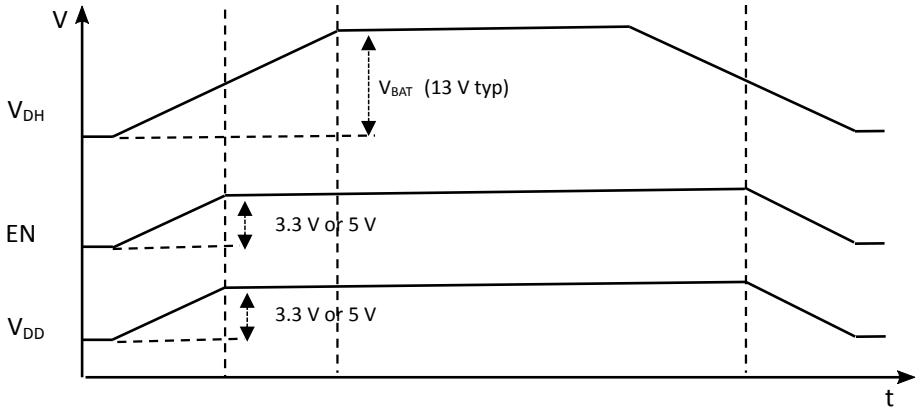
A second power-on sequence is shown in Figure 10. The V_{DD} is raised while the V_{DH} and EN pins are low. After the V_{DD} pin is high and stable, the EN pin is set to turn on the logic of the device or reset to turn it off. The device turns on when the EN pin exceeds the rising V_{ENH} threshold and will turn off when it drops below the falling V_{ENL} threshold.

Figure 10. V_{DH} low and V_{DD} high, EN pin goes high and low



Another possible power-on sequence of the device is shown in Figure 11. V_{DD}, V_{DH}, and EN pins are raised at the same time with the same slew rate.

Figure 11. V_{DH}, V_{DD}, and EN pin goes high and low with the same slew rate



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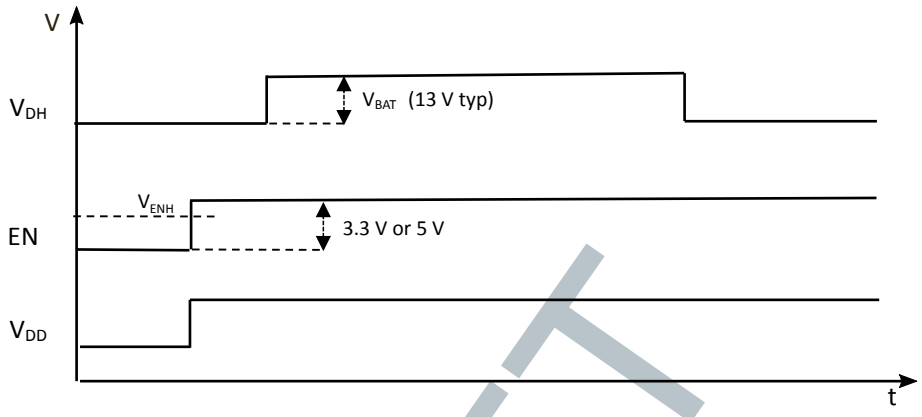
The last power-on sequence is shown in Figure 12. V_{DD} and EN pins are set at the same time and with the same slope while the V_{DH} pin is raised afterwards.

Figure 12. V_{DD} and EN goes high, V_{DH} goes high and low



5.3 Charge pump

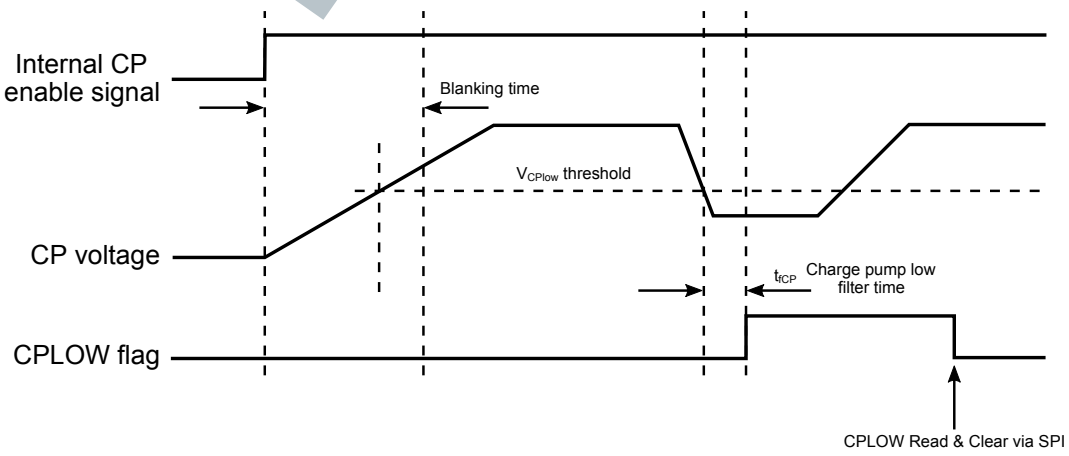
The dual stage charge pump uses two external flying capacitors, which are switched at the frequency f_{CP}, and one output capacitor connected between the CPOUT pin and the VDH pin. The output of the charge pump has a current limitation.

Once the start-up enabling state is over, a blanking time t_{CP_blank} avoids a spurious fault to be triggered and the charge pump becomes fully operative. If the charge pump output voltage falls below the charge pump output voltage low threshold V_{CP_low} for a time longer than t_{CP}, the CPLOW flag is set and the external MOSFETs are switched off.

If the CP_LOW_CONFIG control bit is set, the CPLOW status flag becomes a status bit (set and reset automatically), and the gate drivers come out of the forced disabled mode automatically upon recovery from the charge pump low voltage condition. The status bit is automatically cleared as soon as the charge pump output voltage is no longer below the under-voltage threshold for a time longer than t_{CP}. If the CP_LOW_CONFIG control bit is reset, the gate drivers come out of the forced disabled mode only once the charge pump low voltage flag CPLOW is cleared via SPI, as long as the under-voltage condition is over.

To reduce electromagnetic emissions, the charge pump frequency dithering is enabled by default. However, the dithering can be disabled acting on the CPFDD bit.

Figure 13. CPLOW flag



5.4 V_{ds} measurement

The STDRIVE141 and the STDRIVE121 use internal current-sense amplifier circuits to reflect the drain-to-source voltage across each external MOSFET on the CSO1 pin. The user can select the mapping of the CSO1 signal and monitor the load current.

The CSO1 output can be enabled/disabled by the CSOEN register. When disabled, the output is in high impedance.

To map one of the V_{ds} voltages to the CSO1 line, the two CSOSIG1 and CSOSH1 registers must be used (see Table 20).

The total gain of the CSO1 output voltage is made up of two factors:

- The gain of the first stage is related to the drain-source monitoring threshold of the MOSFET (VDS_CONFx bits). By setting the drain-source monitoring threshold to 75 mV (VDS_CONFx = 0000) or 150 mV (VDS_CONFx = 0001), the gain of the first stage is set to 10 [V/V]. With drain-source monitoring thresholds from 200 mV (VDS_CONFx = 0010) to 400 mV (VDS_CONFx = 0101), the gain of the first stage is set to 2.5 V/V.
- The second stage gain is controlled by the CSO_GAIN_SEL1 register. When CSO_GAIN_SEL1 = 0, the gain set is 1.5 V/V, and when CSO_GAIN_SEL1 = 1, it is set to 3 V/V.

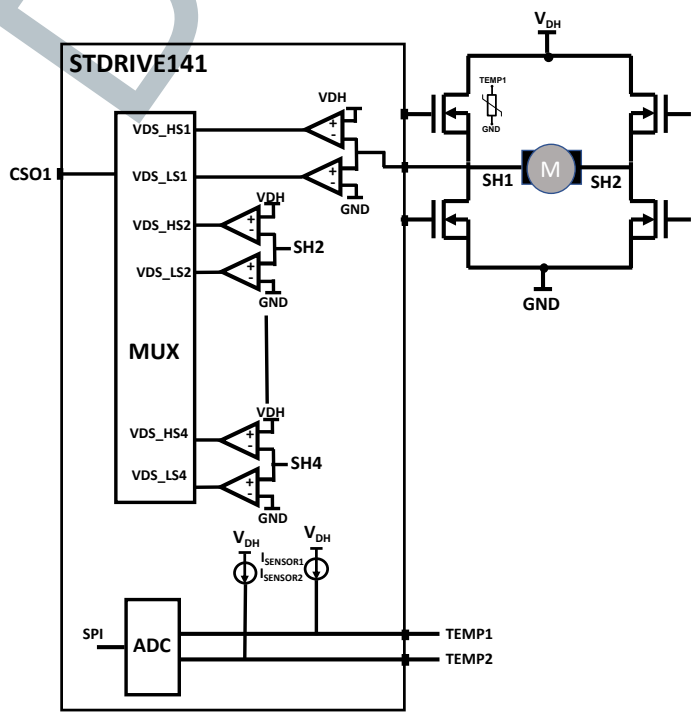
The total gain is given by the product of the two selected gains.

The choice of the gains shall be made according to the expected output voltage of the CSO1: linearity is granted only in the range between 0.1 V and VDD-0.3.

Table 20. V_{ds} mapping on CSO1

CSOSIG1	CSOSH1	Setting
0	00	V_{ds} of the HS1 mapped on the CSO1
0	01	V_{ds} of the HS2 mapped on the CSO1
0	10	V_{ds} of the HS3 mapped on the CSO1 (STDRIVE141 only)
0	11	V_{ds} of the HS4 mapped on the CSO1 (STDRIVE141 only)
1	00	V_{ds} of the LS1 mapped on the CSO1
1	01	V_{ds} of the LS2 mapped on the CSO1
1	10	V_{ds} of the LS3 mapped on the CSO1 (STDRIVE141 only)
1	11	V_{ds} of the LS4 mapped on the CSO1 (STDRIVE141 only)

Figure 14. V_{ds} measurement by CSO1 (STDRIVE141)



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5.5 Temperature measurement

The STDRIVE141 and the STDRIVE121 embed two current generators that can be used to bias two temperature sensors. They can inject a small current (programmable from 250 µA to 1 mA) in a thermistor, an NTC or into the anode of a diode while the cathode is connected to the ground pin.

The voltage across the sensors is measured by an internal ADC (with 11bit resolution) that makes the value available to the microcontroller: the converted values are recorded in two dedicated registers (TEMPx_READ, x = 1 or 2) . The interval time between one temperature measurement and another is 1 ms typ., independently of how many sensors are connected.

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6 Gate drivers

6.1 Outputs driving signals

The following registers need to be set to drive the half-bridges:

1. HB_MODEx (half-bridge mode): this register is used to control the functionality of the single half-bridge. It is a 2-bit register (see Table 21).
2. EN_PWMy (enable PWM): this 1-bit register is used to enable/disable the PWM signal, y indicates the PWM pins that must be enabled/disabled, y = 1 or 2.
3. HB_PWMx (half-bridge PWM): This 3-bit register is used to indicate which PWM signal is applied to the HS or LS of the x-th half-bridge.

When a MOSFET of a half-bridge is powered OFF or ON in the static mode, the HB_MODEx register must be used. For instance, if the HS of the half-bridge 1 and the LS of the half-bridge 2 are powered ON, the following registers must be written:

- HB_MODE**1** = 10
- HB_MODE**2** = 01

Two PWM signals can be applied. Each PWM signal can be mapped to one or more HS or LS MOSFET, properly programming the registers HB_MODEx, EN_PWMy and HB_PWMx.

For instance, an H-bridge is composed of half-bridge 1 and half-bridge 2. The HS of half-bridge 1 is always ON, while PWM2 is applied to the LS of half-bridge 2. In this case, we have:

- HB_MODE**1** = 10 → HS of the half-bridge 1 is ON in static mode
- EN_PWM**2** = 1 → PWM2 signal is activated
- HB_PWM**2** = 001 → PWM2 signal is mapped on the LS of half-bridge 2
- HB_MODE**2** = 11 → enable the HB2 to work in PWM mode

Configuration of the PWM map is shown in the table below:

Table 21. PWM signal application to the half-bridges

HB_PWMx	HB_MODEx	Setting
X	00	LS and HS of half-bridge x are kept OFF (default).
X	01	LS of half-bridge x is ON (static, no PWM), HS of half-bridge x is OFF
X	10	HS of half-bridge x is ON (static, no PWM), LS of half-bridge x is OFF
000	11	Low-side of half-bridge x mapped on PWM1. EN_PWM1 must be set to 1
001	11	Low-side of half-bridge x mapped on PWM2. EN_PWM2 must be set to 1
011	11	High-side of half-bridge x mapped on PWM1. EN_PWM1 must be set to 1
100	11	High-side of half-bridge x mapped on PWM2. EN_PWM2 must be set to 1

The PWMx input pins have an internal pull-down current to put the outputs in a well-known condition if any of the pins are no longer driven by the microcontroller.

Four different free-wheeling strategies are available: active or passive freewheeling on either high-side or low-side MOSFETs. To choose the correct free-wheeling method, the HB_WHEELx must be programmed according to the Table 22.

Table 22. Free-wheeling mode

HB_WHEELx	Setting
00	Passive free-wheeling
01	Active free-wheeling on HS of half-bridge x
10	Active free-wheeling on LS of half-bridge x
11	Passive free-wheeling

In the active free-wheeling case, the MOSFET is actively switched off by the pre-driver. In active free-wheeling, the gate current is fixed. It is possible to configure two different currents according to the STRONG_ON_WHEELx bit: 4 mA if the bit is set to 0, 30 mA if the bit is set to 1.

If both PWM mode and active free-wheeling are enabled, PWM configuration has the higher priority.

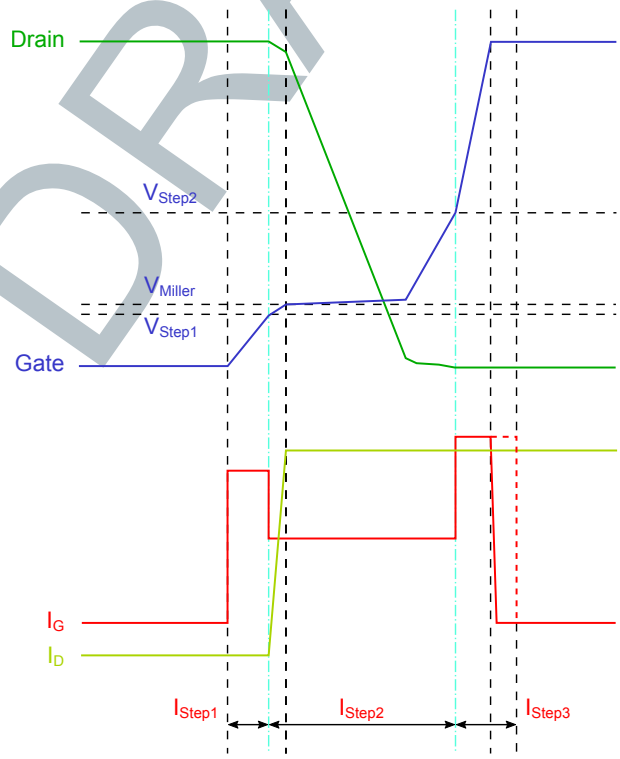
6.2 Power ON/OFF: three stages gate current

A tailored gate current strategy for the $T_{on/off}$ of the external MOSFETs, called “three stages gate current”, has been implemented in the STDRIVE141 and the STDRIVE121. Behavior is shown in Figure 15.

The new gate current strategy is implemented in the following three stages. In the below description, x ranges from 1 to 4 for STDRIVE141 and from 1 to 2 for STDRIVE121:

- **Stage 1**
  When $V_{GS} < V_{step1}$.
  The gate driver currents I_{onx} and I_{offx} are the same during turn-on and turn-off and are determined by the ISTEP1_CONFx register configuration.
- **Stage 2**
  When $V_{step1} < V_{GS} < V_{step2}$.
  During turn-on, the gate driver currents I_{onx} is determined by the ISTEP2_CONFx register configuration.
  During turn off, the gate driver currents I_{offx} is determined by the ISTEP2_OFF_CONFx register configuration.
- **Stage 3**
  When $V_{GS} > V_{step2}$.
  The gate driver currents I_{onx} and I_{offx} are the same during turn-on and turn-off and are determined by the ISTEP3_CONFx register configuration.

Figure 15. Power ON/OFF steps for gate drivers



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7 Protections and diagnostics

7.1 Programmable cross-current protection time (DT)

To avoid cross-conduction, a dead-time period is implemented between the turn-off of a MOSFET and the turn-on of the complementary counterpart (i.e., the other MOSFET of the same leg) in any condition.

Dead time can be applied in two different methods based on the DTP_REF bit value. If DTP_REF = 0, the dead time starts from the command to switch off a MOSFET and switch on the complementary counterpart. If DTP_REF = 1, it starts when the V_{gs} of the turning-off MOSFET reaches the V_{step1}voltage. The dead-time period t_{DTx} of each half-bridge is independently configurable with the control bits DTx[2:0].

7.2 Short circuit detection/drain-source monitoring (DSHS/DSLS)

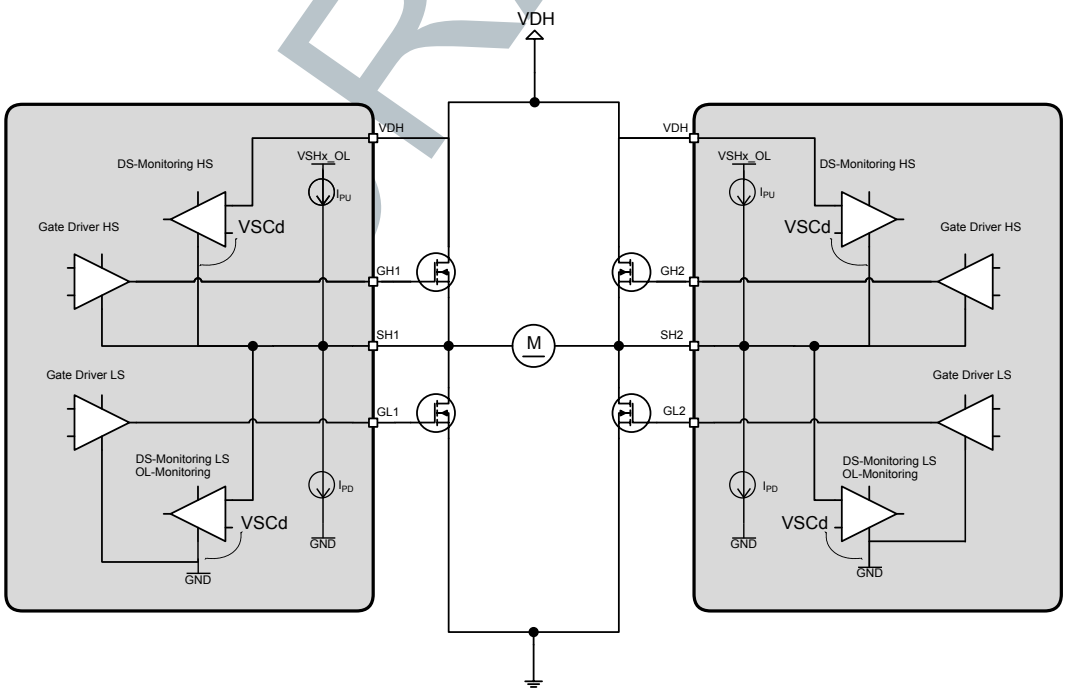
The voltage-drop across each MOSFET is sensed and compared to a programmable threshold to detect an overcurrent condition. This monitoring is activated only on the external turned-on MOSFETs. In the STDRIVE141 and the STDRIVE121, each half-bridge has its own programmable threshold (VDS_CONFx[3:0]), blanking time (VDS_BLANKx[3:0]), and filtering time (VDS_FILTx[2:0]).

As soon as the gate driver turns on a MOSFET, the corresponding drain-source monitoring comparator output is masked for the programmed blanking time. When the blanking time has expired, a filtering time is applied. Both values must be chosen according to the application requirements.

If the sensed V_{ds}voltage exceeds the programmed threshold voltage V_{SCdx} for a time longer than the programmed filtering time, either the gate drivers belonging to that leg are actively switched off or all MOSFETs are switched off with the maximum available current, regardless of the programmed gate current.

In any case, the drain-source monitoring flag VDSHSx or VDSLSx of the MOSFET detecting the fault is set. Once the fault condition is no longer present, the drain-source monitoring flags must be cleared through SPI to re-enable the gate drivers that were forced in disabled mode.

Figure 16. Full-bridge drain source monitoring diagnostics



7.3 VDH overvoltage (VDHOV)

When the VDH supply input voltage rises above the programmable overvoltage protection threshold (V_{DHOVT1} with OVTS = 0 or V_{DHOVT2} with OVTS = 1) for a time longer than t_{OV_FILT}, the corresponding overvoltage flag (VDHOV) is set to protect the application. The charge pump is switched off.

The overvoltage protection flag VDHOV can be cleared by an SPI “read and clear” command only if the VDH overvoltage condition is no longer present.

The following actions can be taken:

- The charge pump is left on. The external MOSFETs are switched off. In particular, the external HS and the LS MOSFETs are actively forced off with the maximum available current, regardless of the programmed gate discharge current. This working mode is obtained by setting the GENMODEx = 0
- The charge pump is left on. The HS external MOSFETs are switched off. The LS MOSFETs are switched on to brake the motor. This working mode is obtained by setting the GENMODEx = 1
- The charge pump and the external MOSFETs are not switched off. The device continues to work and the microcontroller is in charge of choosing how to proceed. This working mode is obtained by setting the GENMODEx = 2

7.4 VDH undervoltage (VDHUV)

When the VDH supply input voltage falls below the undervoltage protection threshold (V_{DHUV}) for a time longer than t_{UV_FILT}, the corresponding undervoltage flag (VDHUV) is set. To protect the external power stage, all the external MOSFETs are switched off. In particular, the LS MOSFET gate drivers and the HS MOSFET gate drivers (as long as $V_{CP} > V_{DH} + 3$ V) are actively switched off with the maximum available current, regardless of the programmed gate discharge current. After that, the MOSFET gate drivers are disabled, and the HS MOSFETs are passively switched off through the internal resistive connection between gate and source. Once the V_{DH} undervoltage condition is no longer present, the VDHUV flag must be cleared to re-enable the gate drivers.

7.5 VDD overvoltage (VDDOV)

When the V_{DD} exceeds the V_{DDOV} threshold for a time longer than t_{OV_FILT}, the corresponding overvoltage flag (VDDOV) is set. All the gate drivers are actively switched off with the maximum available current, regardless of the programmed gate discharge current.

Once the V_{DD} overvoltage condition is no longer present, the overvoltage VDDOV flag can be cleared by an SPI “read and clear” command.

7.6 Thermal warning and thermal shutdown (TW/TSD)

When the device junction temperature rises above the T_{jTW_ON} threshold for a time longer than $t_{fTjTW/TSD}$, the temperature warning flag TW is set and no action is taken. The TW flag can be cleared by an SPI “read and clear” command only if the thermal warning condition is no longer present for a time longer than the corresponding filtering time $t_{fTjTW/TSD}$. When the junction temperature rises above the T_{jSD_ON} threshold for a time longer than $t_{fTjTW/TSD}$, the thermal shutdown flag TSD is set and the external MOSFETs, together with the charge pump are switched off to protect the device. All the gate drivers and the charge pump remain disabled until the condition is recovered and the TSD flag is cleared.

7.7 Diagnostic in off-mode

7.7.1 Off-state diagnostic introduction

The off-state diagnostic features (i.e., the MOSFETs are off while the diagnostic is performed) offer several advantages:

- Diagnostic checks can be performed for loads that are infrequently activated.
- MOSFET short circuit conditions are detected without the stress inherent to on-state diagnostic mode. For instance, the microcontroller may perform an off-state diagnostic right before the activation request of the load. Upon the fault condition, the application software can report the failure and inhibits the load activation, avoiding any stress to the MOSFETs.

To perform the off-state diagnostic, the following conditions are required:

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- The half-bridge drivers must be in active mode: EN = High, $OUTE_x$ = 1, x = 1...4 (STDRIVE141) or x = 1...2 (STDRIVE121)
- The corresponding MOSFETs are off: HB_MODE_x = 00
- The device is operating in normal mode:
  - V_{DH} and V_{DD} are in the normal operating range
  - No watchdog fault

Note: It is highly recommended to restore the setting of V_{SCdx} once the off-state diagnostic is performed for an appropriate MOSFET protection in on-state.

The STDRIVE141 and the STDRIVE121 allow the detection of the following fault conditions while the MOSFETs are deactivated:

- SHx is shorted to V_{DH}
- SHx is shorted to GND
- Open load

Figure 1 shows the block diagram of the off-state diagnostic functionality.

The following components are used to perform the off-state diagnostic:

- Pull-up diagnostic current (I_{shx_PU})
- Pull-down diagnostic current (I_{shx_PD})
- Comparator for the high-side (HS) and low-side (LS) drain-source voltage monitoring

The V_{ds} comparators change their state after a filter time called tDIAG. The faults in the DSRx are not latched and the configurations placed in the registers are bypassed during diag off.

The I_{shx_PU} and I_{shx_PD} values can be selected in the DIAGOFF_CURR_SEL register.

The microcontroller can read the status bit VDS_HSx_DIAG or the status bit VDS_LSx_DIAG to determine if V_{SHx} is high or low.

The diagnostic process is controlled by the microcontroller, whose tasks are:

- To activate and deactivate I_{shx_PU} and I_{shx_PD}, controlled by the HB_IDIAGx registers
- To read and interpret the status bits VDS_LSx_DIAG and VDS_HSx_DIAG

The below conditions are always valid throughout this document:

- VDS_HSx_DIAG = VDS_LSx_DIAG = 0: SHx is low
- VDS_HSx_DIAG = VDS_LSx_DIAG = 1: SHx is high

7.7.2 Example with a DC motor controlled by two half-bridges

This section gives an example of an off-state diagnostic with one DC motor controlled by half-bridges 1 and 2. The voltages at SH1/SH2 (V_{SH1} and V_{SH2}) are analyzed in the following test configurations:

- **Configuration 1**
  I_{shx_PU} HB1 OFF, I_{shx_PU} HB2 OFF, I_{shx_PD} HB1 ON, I_{shx_PD} HB2 ON
- **Configuration 2**
  I_{shx_PU} HB1 ON, I_{shx_PU} HB2 OFF, I_{shx_PD} HB1 OFF, I_{shx_PD} HB2 ON
- **Configuration 3**
  I_{shx_PU} HB1 OFF, I_{shx_PU} HB2 ON, I_{shx_PD} HB1 ON, I_{shx_PD} HB2 OFF

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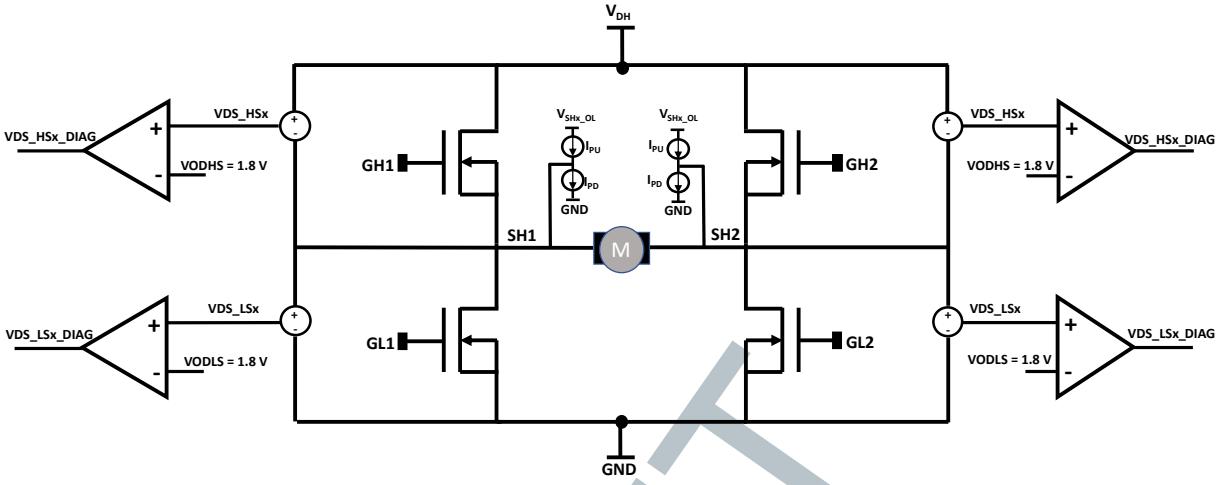
Figure 17. **Simplified block diagram with one DC motor controlled by two half-bridges**



7.7.3 Normal load conditions

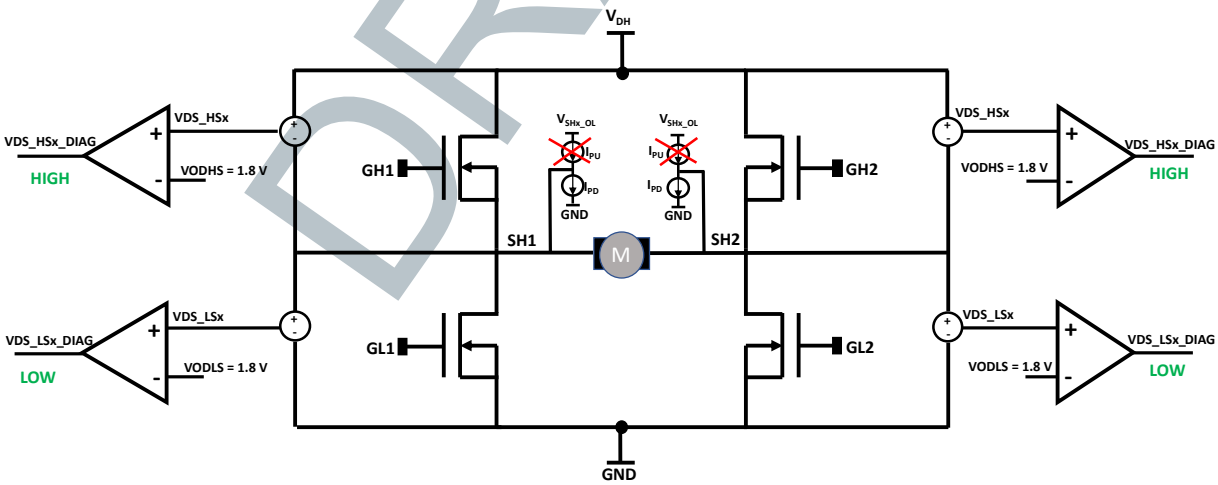
Configuration 1

- I_{shx_PU} HB1 OFF, I_{shx_PD} HB1 ON
- I_{shx_PU} HB2 OFF, I_{shx_PD} HB2 ON

In normal conditions, the motor is connected between SH1 and SH2 without any short circuit.

If I_{shx_PU} of HB1 and HB2 are off, the SH1 and SH2 are pulled down by I_{shx_PD} of HB1 and HB2 (see Figure 18), so VDS_LS1 = VDS_LS2 = LOW and VDS_HS1 = VDS_HS2 = HIGH.

Figure 18. **One motor in normal conditions, I_{shx_PU} HB1/HB2 OFF with normal load - Configuration 1**



Configuration 2

- I_{shx_PU} HB1 ON, I_{shx_PD} HB1 OFF
- I_{shx_PU} HB2 OFF, I_{shx_PD} HB2 ON

With I_{shx_PU} HB1 ON, the SH1 is pulled to V_{SHx_OL}, so VDS_LS1 and VDS_HS1 go HIGH (see Figure 19). SH2 is also pulled to V_{SHx_OL} by I_{shx_PU} of HB1 via the motor, as well as VDS_LS2 and VDS_HS2 go HIGH VDS_LS2.

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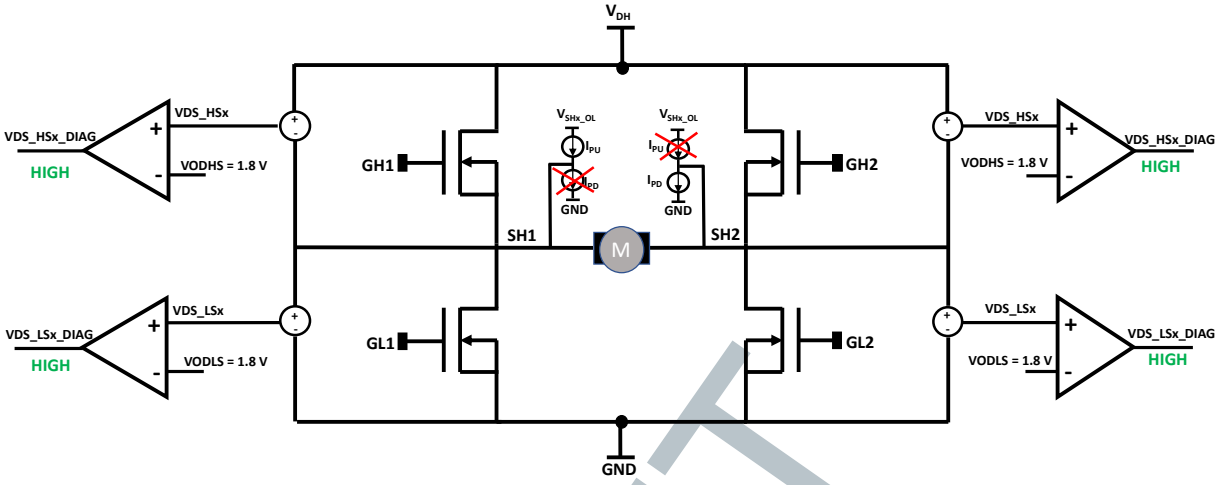
Figure 19. **One motor in normal conditions with one pull-up diagnostic current on - Configuration 2**



Configuration 3

- I_{shx_PU} HB1 OFF, I_{shx_PD} HB1 ON
- I_{shx_PU} HB2 ON, I_{shx_PD} HB2 OFF

This configuration is equivalent to configuration 2, with HB2 pull-up activated instead of HB1.

With I_{shx_PU} HB2 ON, the SH2 is pulled to V_{SHx_OL}, so VDS_LS2 and VDS_HS2 go HIGH (see Figure 19). SH1 is also pulled to V_{SHx_OL} by I_{shx_PU} of HB2 via the motor, as well as VDS_LS1 and VDS_HS1 go HIGH.

Table 23 summarizes the results obtained in normal conditions.

Figure 20. **One motor in normal conditions with one pull-up diagnostic current on - Configuration 3**

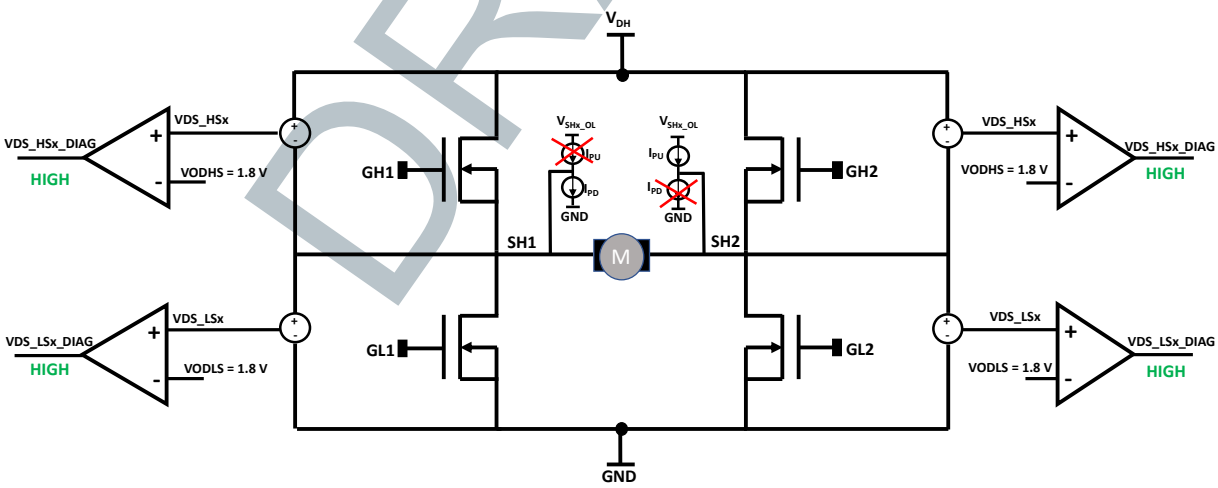


Table 23. **Truth table with normal load conditions**

Configuration	I_{PU} HB1	I_{PU} HB2	I_{PD} HB1	I_{PD} HB2	VDS_LS1	VDS_LS2	VDS_HS1	VDS_HS2
1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
2	ON	OFF	OFF	ON	HIGH	HIGH	HIGH	HIGH
3	OFF	ON	ON	OFF	HIGH	HIGH	HIGH	HIGH

7.7.4 Short circuit to V_{DH}

A short circuit between SH1 and V_{DH} results in VDS_HS1 = LOW and VDS_LS1 = HIGH when I_{shx_PD} HB1 and I_{shx_PD} HB2 are activated.

SH2 is also pulled up by the short circuit via the motor; therefore, VDS_HS2 = LOW and VDS_LS2 = HIGH. Similarly, a short circuit of SH2 to V_{DH} results in VDS_HS1/2 = LOW and VDS_LS1/2 = HIGH.

Figure 21 and Table 24 summarize the results obtained with a short circuit of one output to V_{DH}.

Figure 21. Short circuit to V_{DH}

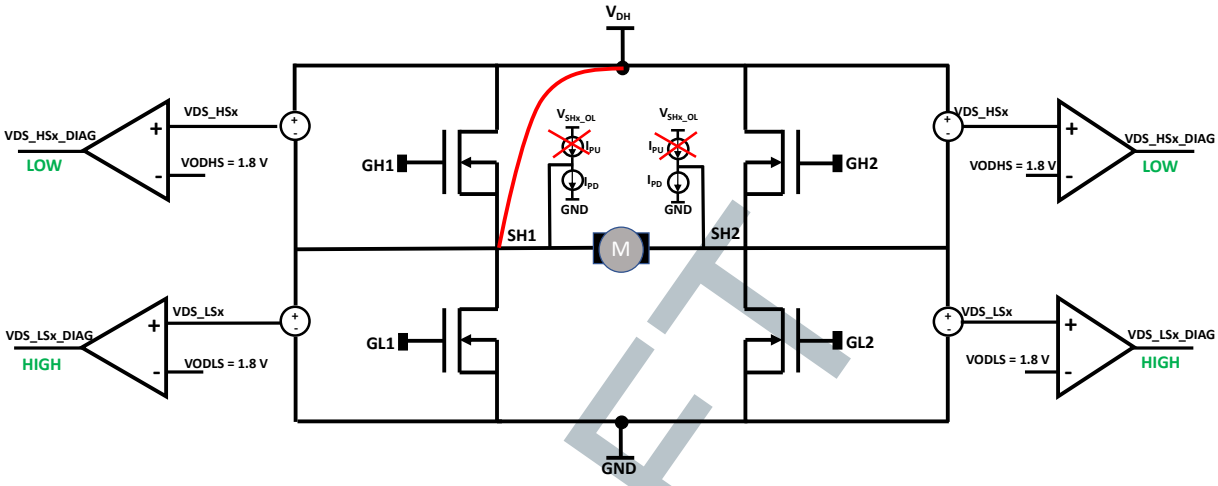


Table 24. Truth table with a short circuit to V_{DH}

Configuration	I_{PU} HB1	I_{PU} HB2	I_{PD} HB1	I_{PD} HB2	VDS_LS1	VDS_LS2	VDS_HS1	VDS_HS2
1	OFF	OFF	ON	ON	HIGH	HIGH	LOW	LOW
2	ON	OFF	OFF	ON	HIGH	HIGH	LOW	LOW
3	OFF	ON	ON	OFF	HIGH	HIGH	LOW	LOW

7.7.5 Short circuit to GND

A short circuit between SH1 and GND results in VDS_HS1 = HIGH and VDS_LS1 = LOW, even if I_{shx_PU} is activated. SH2 is pulled down by the short circuit via the motor winding; therefore, VDS_HS2 = HIGH and VDS_LS2 = LOW.

Similarly, a short circuit of SH2 to GND results in VDS_HS1/2 = HIGH and VDS_LS1/2 = LOW, independently of the state of I_{shx_PU}.

Figure 22 and Table 25 summarize the results obtained with a short circuit of one output to GND.

Figure 22. Short circuit to GND

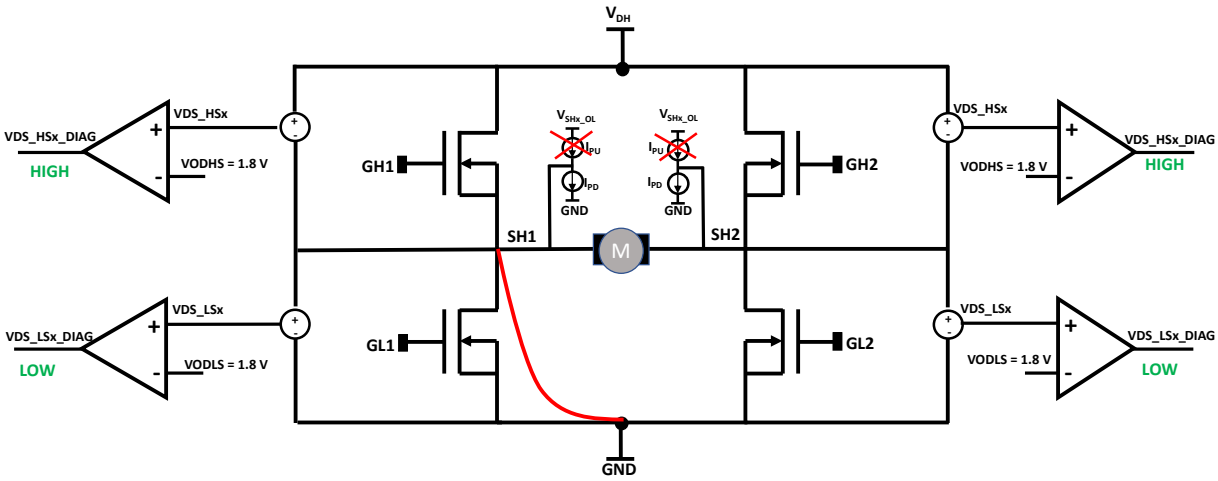


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Table 25. **Truth table with a short circuit to GND**

Configuration	I_{PU} HB1	I_{PU} HB2	I_{PD} HB1	I_{PD} HB2	VDS_LS1	VDS_LS2	VDS_HS1	VDS_HS2
1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
2	ON	OFF	OFF	ON	LOW	LOW	HIGH	HIGH
3	OFF	ON	ON	OFF	LOW	LOW	HIGH	HIGH

7.7.6 Open load - SH1 disconnected

Configuration 1

- I_{shx_PU} HB1 OFF, I_{shx_PD} HB1 ON
- I_{shx_PU} HB2 OFF, I_{shx_PD} HB2 ON

SH1 and SH2 are pulled down by their respective pull-down diagnostic current; therefore, VDS_LS1 = VDS_LS2 = LOW, whereas VDS_HS1 and VDS_HS2 are HIGH

Configuration 2

- I_{shx_PU} HB1 ON, I_{shx_PD} HB1 OFF
- I_{shx_PU} HB2 OFF, I_{shx_PD} HB2 ON

SH1 is pulled up by I_{shx_PU} HB1: therefore, VDS_LS1 = HIGH and VDS1_HS1 = HIGH. Due to the motor disconnection at SH1, SH2 is pulled down by I_{shx_PD} HB2; therefore, VDS_LS2 = LOW and VDS_HS2 = HIGH

Configuration 3

- I_{shx_PU} HB1 OFF, I_{shx_PD} HB1 ON
- I_{shx_PU} HB2 ON, I_{shx_PD} HB2 OFF

SH1 is pulled down by I_{shx_PD} HB1; therefore, VDS_LS1 = LOW and VDS_HS1 = HIGH. However, SH2 is pulled up by I_{shx_PU} HB2: VDS_LS2 = HIGH and VDS_HS2 = HIGH.

Figure 23 and Table 26 summarize the results obtained with an open load at SH1.

Figure 23. **One motor - Diagnostic results with an open load at SH1**

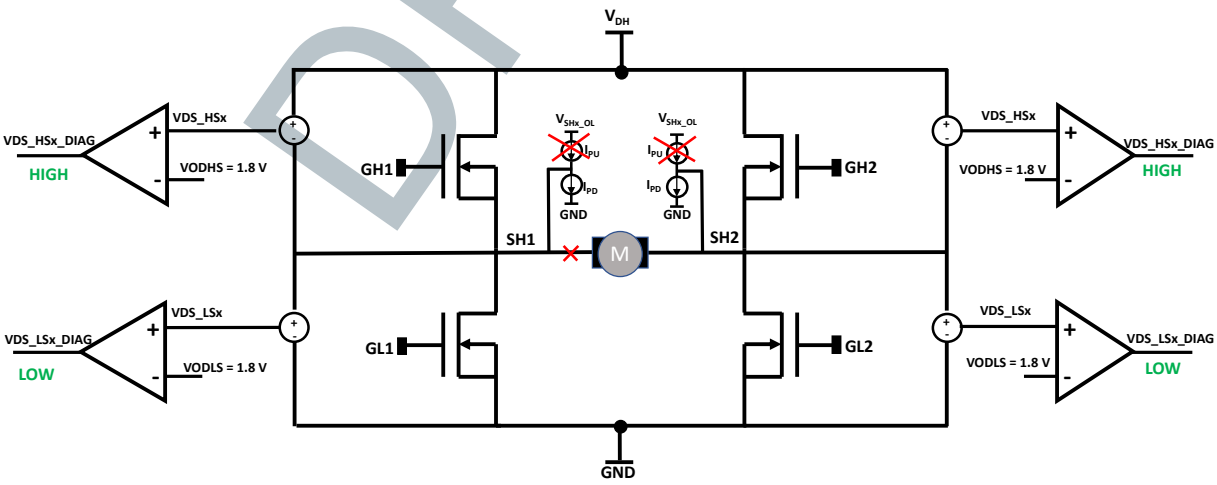


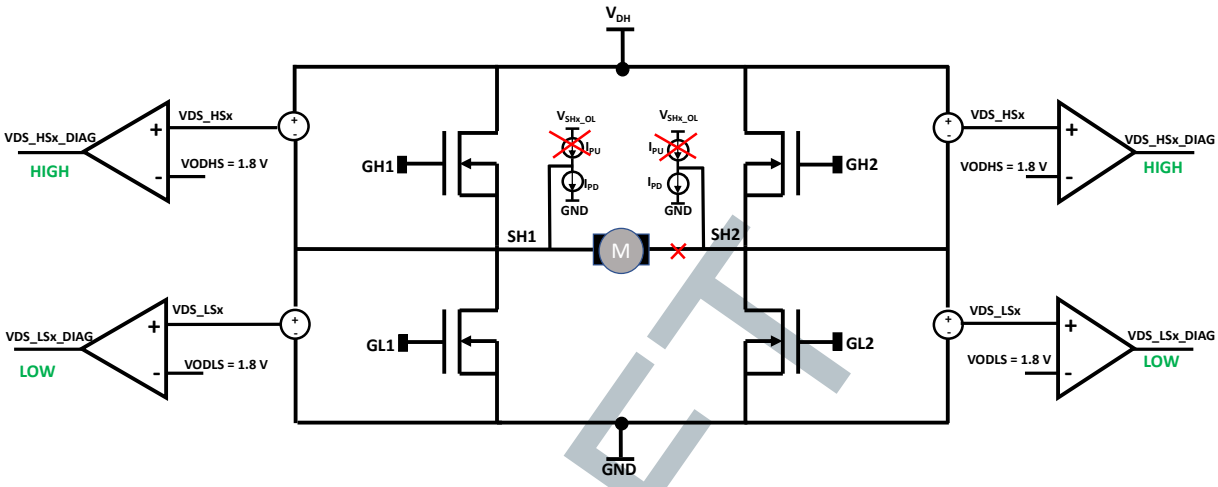
Table 26. **Truth table open load - SH1 disconnected**

Configuration	I_{PU} HB1	I_{PU} HB2	I_{PD} HB1	I_{PD} HB2	VDS_LS1	VDS_LS2	VDS_HS1	VDS_HS2
1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
2	ON	OFF	OFF	ON	HIGH	LOW	HIGH	HIGH
3	OFF	ON	ON	OFF	LOW	HIGH	HIGH	HIGH

7.7.7 Open load - SH2 is disconnected

Similarly, a motor disconnection at SH2 shows the same result as for a motor disconnection at SH1 (see Figure 24). Therefore, Table 1 is valid for an open load, independently from the location of the disconnection.

Figure 24. One motor - Diagnostic results with an open load at SH2



7.8 Summary of the off-state diagnostic

When comparing the results from Table 23, Table 24, Table 25 and Table 26, we see that test configuration 1 and test configuration 2 (or test configuration 1 and test configuration 3) are sufficient to detect and distinguish among a normal load condition, a short circuit to V_{DH}/GND, and an open load.

A summary is shown in the Table 27.

The pull-up and pull-down currents can be selected in the HB_IDIAGx registers.

Table 27. Differentiation between normal condition, short to V_{DH}, short to GND and open load with one motor

Load conditions	Configuration	I_{PU} HBx	I_{PU} HBy	I_{PD} HBx	I_{PD} HBy	VDS_LSx	VDS_LSy	VDS_HSx	VDS_HSy
Normal condition	1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
	2	ON	OFF	OFF	ON	HIGH	HIGH	HIGH	HIGH
	3	OFF	ON	ON	OFF	HIGH	HIGH	HIGH	HIGH
Short to V_{DH}	1	OFF	OFF	ON	ON	HIGH	HIGH	LOW	LOW
	2	ON	OFF	OFF	ON	HIGH	HIGH	LOW	LOW
	3	OFF	ON	ON	OFF	HIGH	HIGH	LOW	LOW
Short to GND	1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
	2	ON	OFF	OFF	ON	LOW	LOW	HIGH	HIGH
	3	OFF	ON	ON	OFF	LOW	LOW	HIGH	HIGH
Open load	1	OFF	OFF	ON	ON	LOW	LOW	HIGH	HIGH
	2	ON	OFF	OFF	ON	HIGH	LOW	HIGH	HIGH
	3	OFF	ON	ON	OFF	LOW	HIGH	HIGH	HIGH

7.9 DIAGN pin (diagnostic not an output)

The DIAGN pin is used to detect a device fault, including an SPI error, a watchdog error, or a device power-on-reset event. The purpose of the DIAGN output pin is to immediately alert the microcontroller of a new fault without the need of periodic SPI transfers.

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The logic level signal at the pin is the logical NOR combination of all the status flags and status bits set in the DIAGCR1 and DIAGCR2 control registers, together with the global status byte RSTB bit.

Once the device comes out of reset mode, the DIAGN pin is pulled low because of the global status byte RSTB bit. If only the global status byte RSTB bit is set, any valid SPI communication frame clears the RSTB bit, pulling up the DIAGN pin high. Any read access to the DSR1 and DSR2 registers reset this signal to a high level, until an error from a new source occurs again, pulling the pin low.

The DIAGN pin is active low by default; it is possible to change its polarity by acting on the DIAGN_ACTIVE_LEVEL bit.

If a fault from a new error source occurs during a read access to the DSR1 and DSR2 registers, the DIAGN output pin remains low (this avoids any loss of information, since the new error source status flag/bit will not be reported by the concomitant read access, but a new access would be required).

Even if a read operation of the status register occurs before a “read and clear” operation, any such operation on the DSR1 and DSR2 status registers pulls the DIAGN pin high.

7.10 Configurable window watchdog

By default, as soon as the device finishes the power-up phase, the watchdog is enabled and starts running with a long open window. The long open window provides more time for the microcontroller to complete the device initialization and it allows the watchdog disabling procedure to run if the watchdog is not required by the application.

To trigger the watchdog for the first time, the microcontroller must write 5555h to the trigger/disable register (WDGTRDIS) before the end of the long open window.

After the first valid trigger command, the watchdog enters the window mode. In window mode, the microcontroller must continuously reset the watchdog by alternating the commands (e.g., 2AAAh, 5555h,…) in the WDGTRDIS register within the active window. Any correct watchdog trigger will immediately start a new window.

In the event of a watchdog failure, due to a command outside the open window, an invalid or unexpected trigger value, a timeout, or a disabling procedure attempted outside the LOW window - the WDG_ERROR flag is set, and the device enters the fail-safe mode. In fail-safe mode, the OUTEx control bits are reset, and all the gate drivers are switched off with the maximum available current. To reactivate the gate drivers, the WDG_ERROR flag must be cleared via SPI. Clearing the bit runs the watchdog with a long open window.

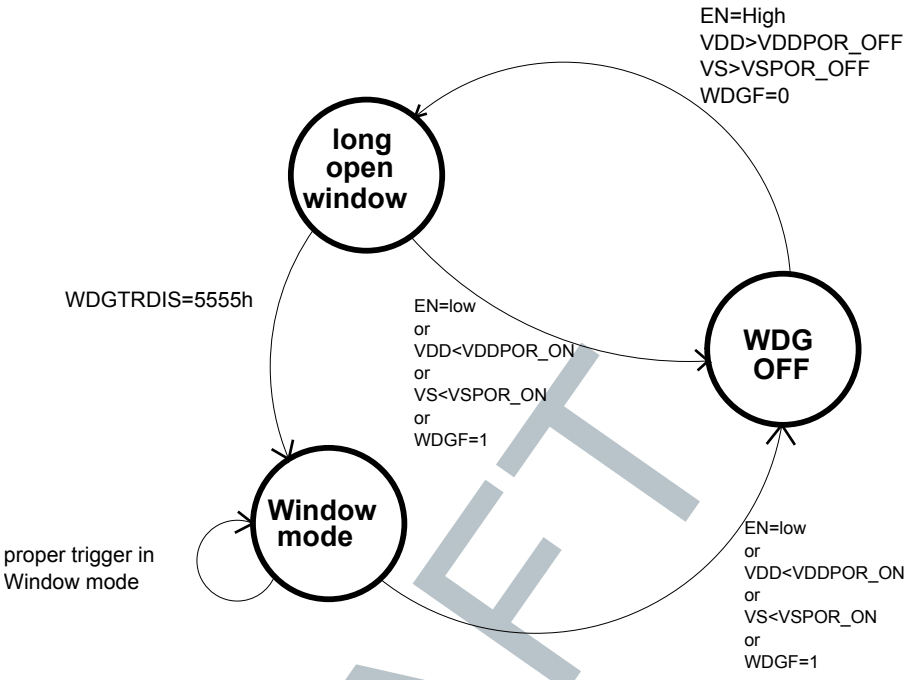
Once the watchdog starts running again with a long open window after coming out of the fail-safe mode, to re-enter window mode, the microcontroller must write 5555h in the WDGTRDIS register.

To disable the watchdog, the microcontroller must write two consecutive valid SPI frames in the correct order (2F6Bh first key word, 1097h second key word), to control the WDGTRDIS register within a window ($t_{timeout}$). To enable the watchdog, the microcontroller must write two consecutive valid SPI frames in the correct order (5C99h first key word, 4360h second key word), to control the WDGTRDIS register within a window ($t_{timeout}$).

Any other SPI transfer between the two SPI frames carrying the key, including an invalid SPI transfer or keys sent in the wrong order, will abort the disabling process and generate a watchdog fault (WDG_ERROR).

Any read access to the WDGTRDIS register provides information concerning the watchdog disabling procedure result, together with the three least significant bits of the latest write operation performed on the same register.

Figure 25. **Watchdog state diagram**



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8 Serial peripheral interface (SPI)

A 24-bit SPI is used for bidirectional communication with the microcontroller.

The microcontroller SPI peripheral must run in the following configuration:

- CPOL = 0
- CPHA = 1

In this configuration, the input data from the SDI pin is sampled on the falling edge of the serial clock CLK, and the output data changes on the rising edge of the serial clock CLK.

Proper decoding of any SPI frame is not guaranteed during a t_{START} time after the enable pin goes high with the VDD supply already ON.

The SPI protocol implemented in STDRIVE141 and STDRIVE121 is out-of-frame: the IC provides the content, requested in frame n, on frame n+1.

Note: The SPI bus can be used in a parallel configuration by controlling the CSN signal of the connected IC's.

It is recommended to read the global status SPI registers after the power-up to clear any diagnostic flags.

Chip select (CSN)

The CSN input pin is used to address the SPI communication with the device. When CSN is high, the output pin (SDO) is in high impedance. When CSN is low, the output pin (SDO) driver is enabled, and serial communication can start. The information transferred during CSN = 0 is called for a communication frame. When CSN = high for t > t_9, the SDO output switches back to high impedance to allow SPI communications with other SPI nodes.

Serial data in (SDI)

The SDI input pin is used to transfer data to the device. The data applied to the SDI is sampled on the falling edge of the serial CLK signal and shifted into an internal 24-bit shift register. At the rising edge of the CSN signal, the content of the shift register is transferred to the data input register. The writing to the selected data input register is enabled only if exactly 24 bits are transmitted within one communication frame (i.e., CSN remains low during transmission). Writing is not enabled if one of the following cases occurs:

- More or fewer than 24 clock pulses are counted within one frame
- During the falling and rising edges of CSN, the level of SCLK is not low
- All bits of a command received on SDI are logic 0 or logic 1
- The number of CKL rising edges in a frame is not 24
- The address field is unknown
- The parity check fails

Serial data out (SDO)

The SDO output driver is activated by a logical low level on the CSN input. The first two rising edges of the CLK input, after a high-to-low transition of the CSN pin, transfer the "SPI error or RESET" bit and the GSBN bit.

Serial clock (CLK)

The CLK input pin is used to synchronize input and output serial bit streams. The data input (SDI) is sampled on the falling edge of CLK, and the data output (SDO) changes on the rising edge of CLK. The interface supports a CLK frequency up to 6 MHz.

8.1 Physical layer

This chapter describes the SPI protocol configuration.

The SPI connection between the microcontroller and the STDRIVE141 or STDRIVE121 is shown in Figure 26.

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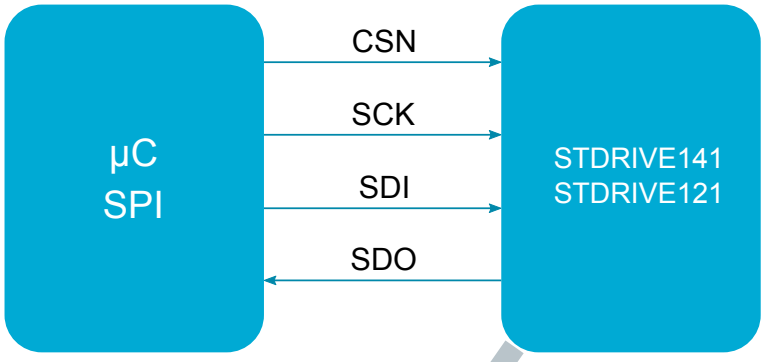
Figure 26. **SPI connection**



8.2 Clock and data characteristics

The SPI can be driven by a microcontroller through its SPI peripheral.

Any communication frame starts with the falling edge of CSN (communication start). CLK must be low.

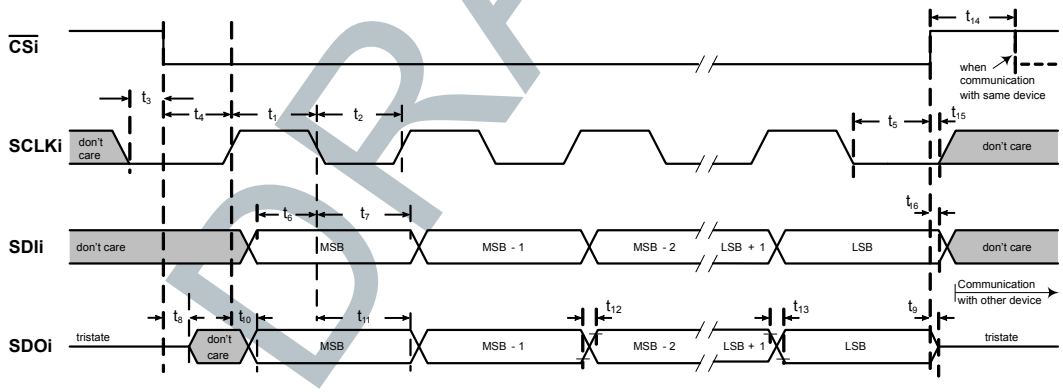
The SDI data is then latched on each subsequent rising edge of CLK into the internal shift registers.

When communication starts, the SDO leaves 3-state mode and MSB of the data is shifted out to the SDO pin.

The communication frame is completed on the rising edge of CSN. If the SPI command is valid, the requested operation is executed (write or clear operation).

The SPI signal description is shown in Figure 27.

Figure 27. **SPI signal description**



8.3 Communication protocol

8.3.1 SDI frame

The device data-in frame consists of 24 bits (OpCode (1 bit) + reserved (1 bit) + address (6 bits) + data byte 2 (8 bits) + data byte 1 (7 bits) + parity bit (1 bit)):

- **OpCode** = The first transmitted bit (MSB) contains the operation code, which represents the command/ instruction that is performed
- **Reserved** = Not used in the SDI frame (MSB-1)
- **Address** = The following 6 bits (MSB-2 to MSB-7) represent the register address on which the command/ operation is performed
- **Data bytes** = The subsequent 15 bits (MSB-8 to MSB-22) contain the payload to write
- **Parity bit** = Last bit (MSB-23) contains the parity bit for the integrity check

8.3.1.1 OpCode

The OpCode bit is used to distinguish between a read and a write operation.

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Table 28. **OpCode**

MSB	Description
0	Read command
1	Write command

A Write command (with no parity error, no wrong address and no CLK count error) modifies the content of the addressed register with the transmitted payload. The register update is performed at the beginning of the following SPI communication.

With the Read command, two different events can be performed:

- A Read event transfers the data requested in frame n during the frame n+1. In this case, all bits of the payload data sent in frame n is set to 0, and the data of the addressed register is not modified.
- A Clear on Read transfers the data requested in frame n during the frame n+1. In this case, all bits of the payload data sent must be cleared and is set to 1.

8.3.1.2 *Address*

The address bits are used to indicate the register on which the command/operationis performed:

- In case of a read command (frame n), the address bits indicate the register to be read. Its content is transferred during the next frame (n+1).
- In case of a write command, the address bits indicate the register where the data must be written.

8.3.1.3 *Data word*

The payload (data byte 2 to data byte 1) is the data transferred to the device at every SPI communication. The payload always follows the address bits.

- For a write access, the payload represents the new data written to the addressed register.
- For a read operation, the payload is not used. All bits must be set to ‘0’.
- For a clear on read operation, the payload is used. All bits that must be cleared have to be set to ‘1’.

8.3.1.4 *Parity bit*

A parity bit is added at the end of the 24 bits of each frame as an error detection code.

An odd parity bit for each communication must be calculated considering the entire 24-bit frame. The frame is considered valid only if the result of the parity check is valid, which means an odd number of ‘1’ is present in the SDI frame. Otherwise, the frame is ignored and an SPI_ERROR event is triggered.

8.3.2 SDO frame

The data-out frame consists of 24 bits (SPI ERROR (1 bit) + GSBN (1 bit) + address (6 bits) + data byte 2 (8 bits) + data byte 1 (7 bits) + parity bit (1 bit)).

- **SPI ERROR** = The first transmitted bit (MSB) contains information about an SPI error or RESET
- **GSBN** = Global status bit, used only in the SDO frame (MSB-1)
- **Address** = The following 6 bits (MSB-2 to MSB-7) represent the register address on which the command/ operation is performed
- **Data bytes** = The subsequent 15 bits (MSB-8 to MSB-22) contain the payload
- **Parity bit** = Last bit (MSB-23) contains the parity bit for the integrity check

8.3.2.1 *SPI ERROR bit*

The SPI ERROR bit contains information about an SPI error or a RESET event according to Table 29:

Table 29. **SPI ERROR bit**

MSB	Description
0	No SPI error in previous access and no RESET event before this access
1	SPI error in previous access or RESET event before this access

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8.3.2.2 *Global status bit (GSBN)*

The GSBN is the logical NOR combination of the DSR1 and DSR2 registers + the SPI error bit + the RSTB bit + the WDG error bit. The GSBN bit is directly related to the DIAGN pin.

- GSBN = 1 (no error), DSR1 bits + DSR2 bits + SPI error bit + RSBT bit all set to 0
- GSBN = 0 (error), one or more bit/s of DSR1 or DSR2 or SPI error or RSBT is/are set to 1

8.3.2.3 *Address*

The address bits are used to indicate the register on which the operation has to be performed:

- In case of SPI error, a reset event, or a first access, the address field contains the address of the DRS0 register
- In all other cases, for both read and write operations, the address field contains the address selected in the previous frame

8.3.2.4 *Data word*

The payload (data byte 2 to data byte 1) always follows the address bits and indicates:

- In case of an SPI error, a reset, or a first access, the contents of the DRS0 register
- In all other cases (both read and write), the contents of the addressed register updated at the last CSN falling edge

8.3.3 Protocol failure detection

A basic set of SPI communication failure detection mechanisms are implemented.

8.3.3.1 *Clock count*

During communication (CSN low), a clock monitor counts the valid CLK clock edges. If the count is different from 24, the SPI write command is ignored, and the SPI error bit is set and transferred during the next SPI command.

8.3.3.2 *CLK polarity (CPOL) check*

During the falling and rising edge of CSN, the level of SCLK must be low. Otherwise, the SPI write command is ignored, and the SPI error bit is set and transferred during the next SPI command.

8.3.3.3 *CSN timeout*

By pulling CSN low, SDO is actively driven and leaves its tristate condition. To ensure communication with other SPI devices within the same bus, even if CSN is stuck at a low logic state, a CSN timeout is implemented. By pulling CSN low, an internal timer is started. When the timer reaches its end, the ongoing command is rejected, the SPIE is set, and SDO returns to high impedance.

8.3.3.4 *SDI stuck at low logic state*

A first communication frame with all zeroes (OpCode ‘0’ and address ’000000’) is not allowed, and SDI is considered stuck at the low logic state. If SDI is detected as stuck, the command is rejected, and the SPIE is set, and transferred during the next communication frame.

8.3.3.5 *SDI stuck at high logic state*

A first communication frame with all ones (OpCode ‘1’ and address ’111111’) is not allowed, and SDI is considered stuck at the high logic state. If SDI is detected to be stuck, the command is rejected, and the SPIE is set and transferred during the next communication frame.

8.4 SPI communication scenarios

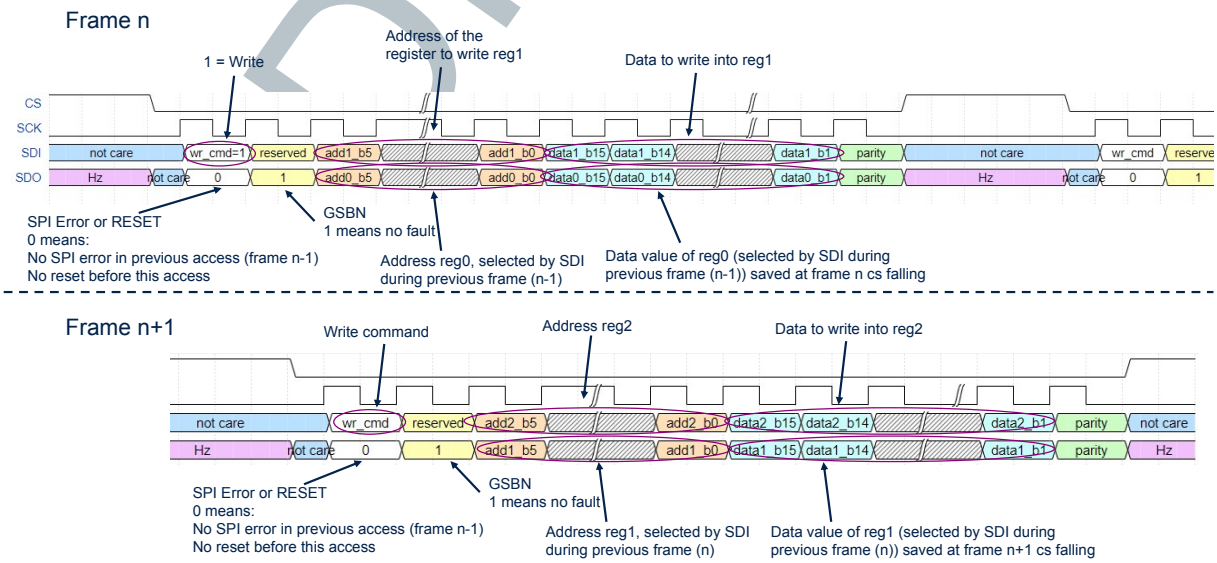
Some SPI communication scenarios are shown in the following sections.

8.4.1 Write access

When a write command must be performed, the communication frames are built as follows:

- Frame n
  - SDI:
    - Bit 23 = 1 (write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit
- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n)
    - Bit 0 = Parity bit

Figure 28. Write access scenario



8.4.2 Read access

When a read command must be performed, the communication frames are built as follows:

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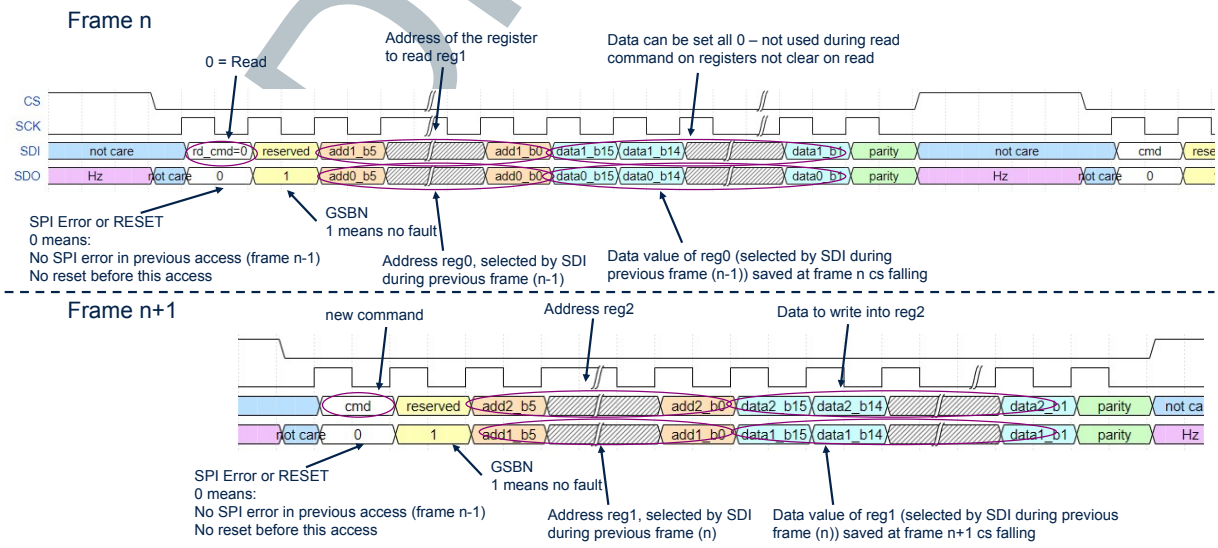
- Frame n
  - SDI:
    - Bit 23 = 0 (read command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read
    - Bits 15 to 1 = Data can be set to ‘0’
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit
- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n)
    - Bit 0 = Parity bit

Figure 29. Read access scenario



8.4.3 Clear on read

When a clear on read command must be performed, the communication frames are built as follows:

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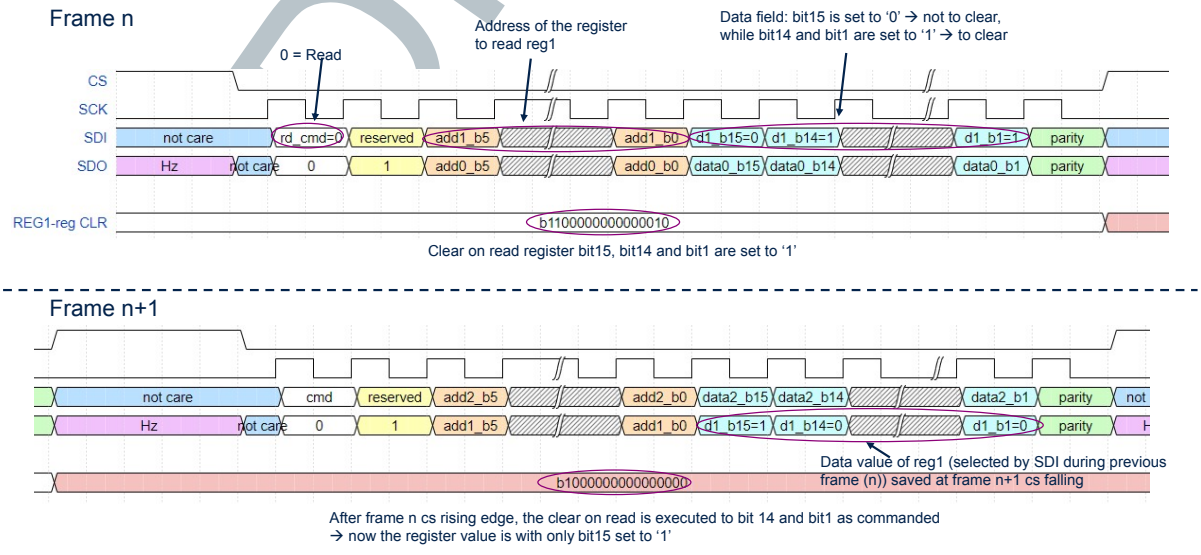
- Frame n
  - SDI:
    - Bit 23 = 0 (read command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read
    - Bits 15 to 1 = Set to 0 the bits “not to clear”, set to 1 the bits “to clear”
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit
- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n) with the bits cleared
    - Bit 0 = Parity bit

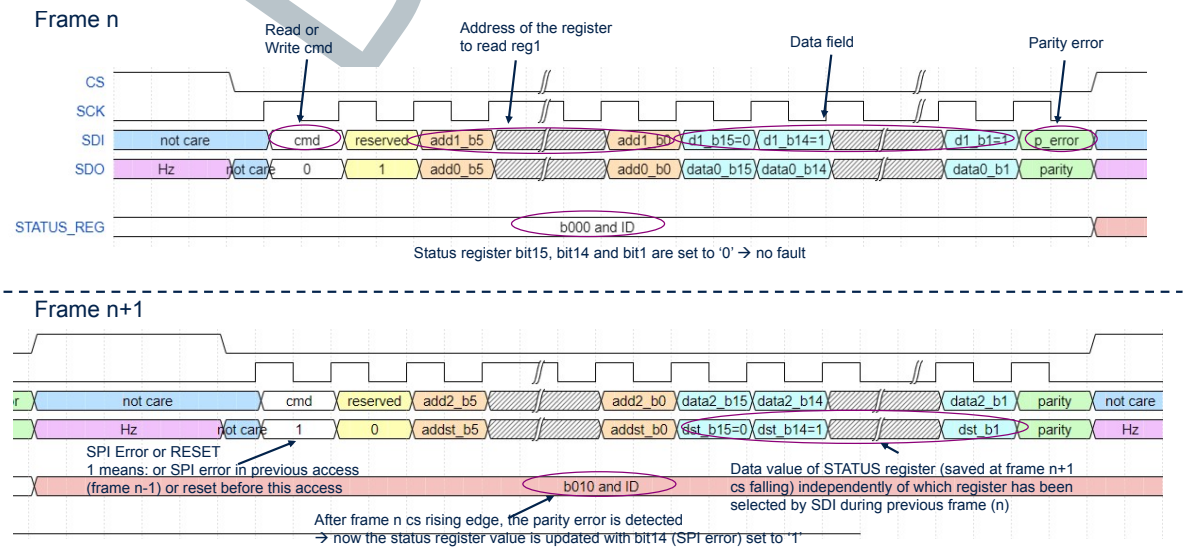
Figure 30. Clear on read scenario



8.4.4 Write or read with SPI error

- Frame n
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write (if write command was chosen) or all ‘0’ (if read command was chosen)
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit
- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 1 (SPI error or RESET detected in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n)
    - Bits 15 to 1 = Data value of the STATUS register independently of which register has been selected by SDI during the previous frame (n)
    - Bit 0 = Parity bit

Figure 31. Write or read with SPI error scenario



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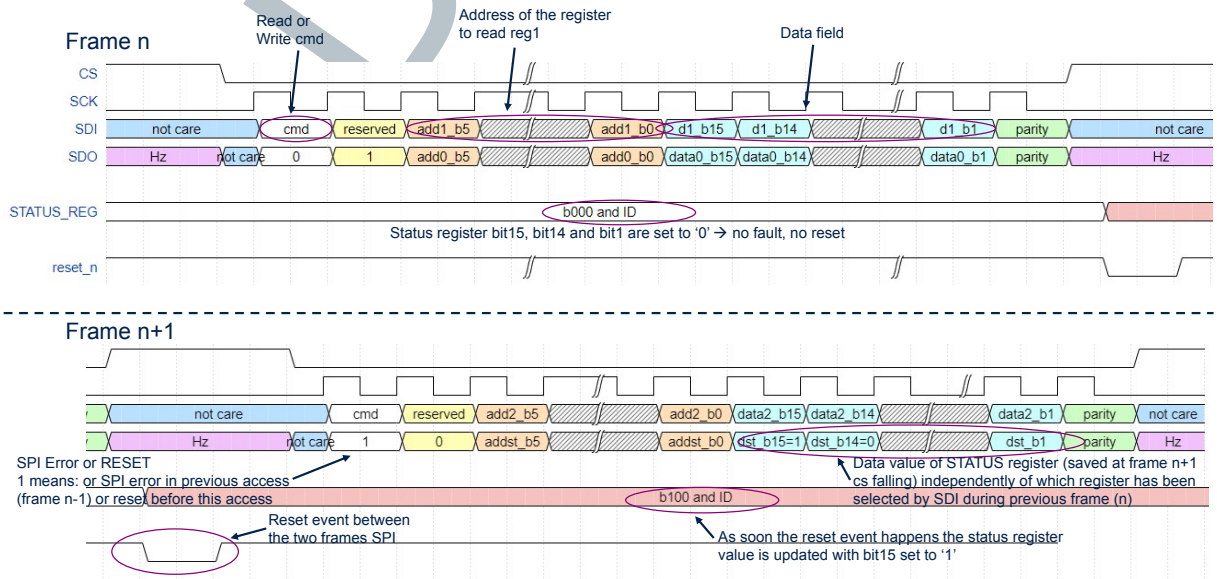
8.4.5 Access after RESET

- Frame n
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write (if write command was chosen) or all ‘0’ (if read command was chosen)
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit
- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write into the chosen register
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 1 (SPI error or RESET event in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the STATUS register
    - Bits 15 to 1 = Data value of the STATUS register
    - Bit 0 = Parity bit

Figure 32. Access after RESET scenario



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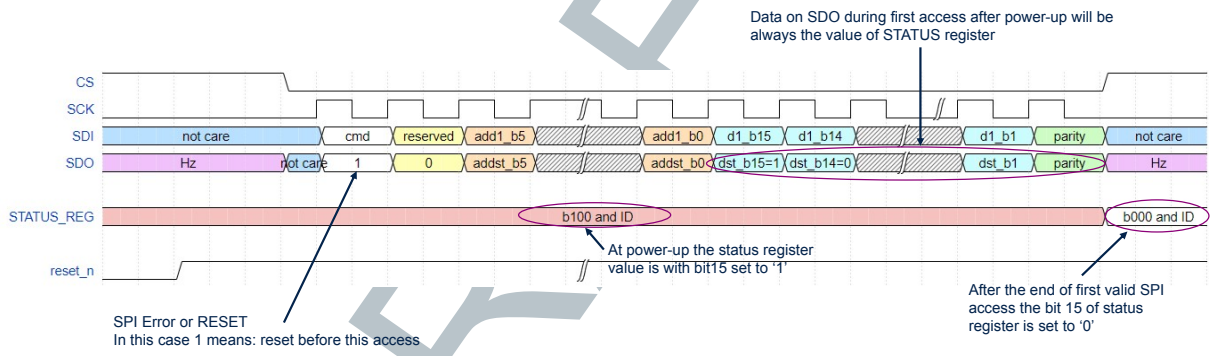
8.4.6 First SPI access at power-up

- Frame 1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write (if write command was chosen) or all ‘0’ (if read command was chosen)
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 1 (SPI error or RESET event in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the STATUS register
    - Bits 15 to 1 = Data value of the STATUS register
    - Bit 0 = Parity bit

Figure 33. First SPI access at power-up scenario



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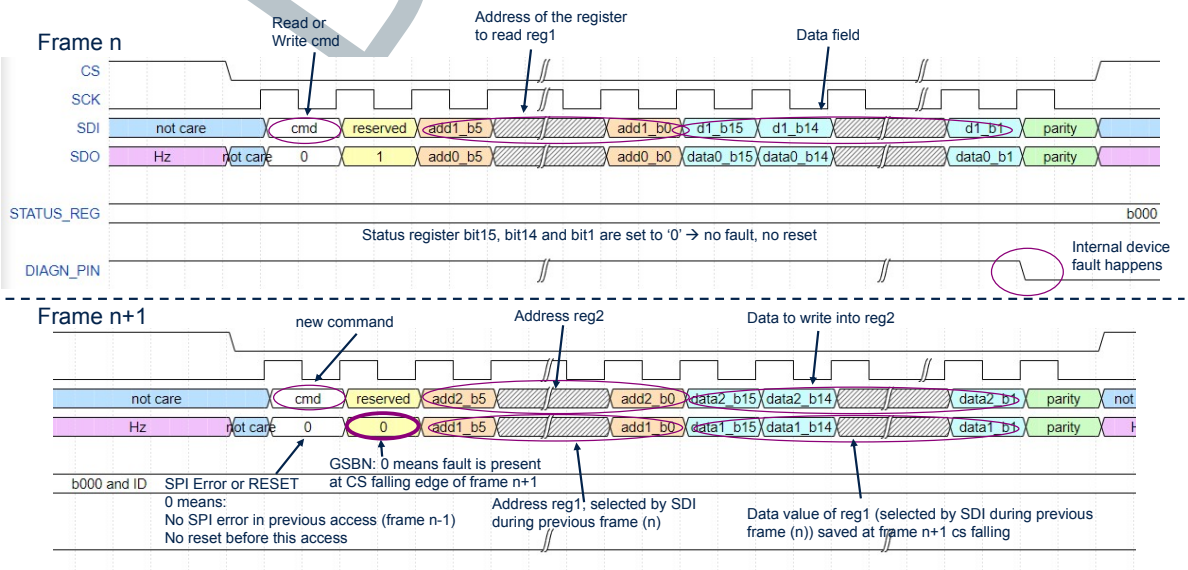
8.4.7 Access while an internal fault happens

- Frame n
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write (if write command was chosen) or all ‘0’ (if read command was chosen)
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (1 = No fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n-1)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n-1)
    - Bit 0 = Parity bit
- Frame n+1
  - SDI:
    - Bit 23 = 0 or 1 (read or write command on the OpCode)
    - Bit 22 = Not used
    - Bits 21 to 16 = Address of the register to read or write
    - Bits 15 to 1 = Data to write (if write command was chosen) or all ‘0’ (if read command was chosen)
    - Bit 0 = Parity bit
  - SDO:
    - Bit 23 = 0 (no SPI error or RESET in the previous access)
    - Bit 22 = GSBN bit (0 = Fault)
    - Bits 21 to 16 = Address of the register selected in the previous frame (n)
    - Bits 15 to 1 = Data value of the register selected in the previous frame (n)
    - Bit 0 = Parity bit

Figure 34. Access while an internal fault happens scenario



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9 SPI registers

9.1 Register map overview

Table 30. **Register map overview**

Addr.	Name	Bits	15	14	13	12	11	10	9	8	Mode
			7	6	5	4	3	2	1	0	
0x01	DSR0	MSB	-	RSTB	SPI_ERROR	WDG_ERROR	REVISION_ID[7]	REVISION_ID[6]	REVISION_ID[5]	REVISION_ID[4]	RO/CR
		LSB	REVISION_ID[3]	REVISION_ID[2]	REVISION_ID[1]	REVISION_ID[0]	DEVICE_ID[3]	DEVICE_ID[2]	DEVICE_ID[1]	DEVICE_ID[0]	
0x02	DSR1	MSB	-	RES	VDHOV	VDHUV	VDDOV	TW	TSD	DIAGCR	RO/CR
		LSB	RES	RES	RES	RES	VDSHS4(1)	VDSHS3(1)	VDSHS2	VDSHS1	
0X03	DSR2	MSB	-	RES	RES	RES	RES	RES	RES	RES	RO/CR
		LSB	RES	RES	RES	VDSLS4(1)	VDSLS3(1)	VDSLS2	VDSLS1	CPLOW	
0X04	GLOBAL_CFG	MSB	-	RES	RES	RES	OSC_SS_DIS	DIAGN_ ACTIVE_ LEVEL	DIAGOFF_ CURR_SEL	VDS_OFFSET_ ENABLE	RO/RW
		LSB	DTP_REF	OVTS	OUTE	CP_LOW_ CONFIG	CPFDD	EN_PWM1	EN_PWM2	RES	
0X05	CSO_CFG	MSB	-	RES	RES	RES	RES	CSO_GAIN_SEL1	RES	CSOSIG1	RW
		LSB	RES	CSOEN1	RES	RES	RES	RES	CSOSH1[1](1)	CSOSH1[0]	
0X06	TEMP_CFG	MSB	-	RES	RES	RES	RES	RES	RES	RES	RW
		LSB	RES	RES	RES	RES	ITEMP_CONF2 [1]	ITEMP_CONF2 [0]	ITEMP_CONF1 [1]	ITEMP_CONF1 [0]	
0X07	TEMP1_READ	MSB	-	RES	RES	RES	RES	TEMP1_READ [10]	TEMP1_READ [9]	TEMP1_READ [8]	RO
		LSB	TEMP1_READ [7]	TEMP1_READ [6]	TEMP1_READ [5]	TEMP1_READ [4]	TEMP1_READ [3]	TEMP1_READ [2]	TEMP1_READ [1]	TEMP1_READ [0]	
0X08	TEMP2_READ	MSB	-	RES	RES	RES	RES	TEMP2_READ [10]	TEMP2_READ [9]	TEMP2_READ [8]	RO
		LSB	TEMP2_READ [7]	TEMP2_READ [6]	TEMP2_READ [5]	TEMP2_READ [4]	TEMP2_READ [3]	TEMP2_READ [2]	TEMP2_READ [1]	TEMP2_READ [0]	
0X0B	DIAG_OFF_HS	MSB	-	RES	RES	RES	RES	RES	RES	RES	RO
		LSB	RES	RES	RES	RES	VDS_HS4_DIAG(1)	VDS_HS3_DIAG(1)	VDS_HS2_DIAG	VDS_HS1_DIAG	
0X0C	DIAG_OFF_LS	MSB	-	RES	RES	RES	RES	RES	RES	RES	RO
		LSB	RES	RES	RES	RES	VDS_LS4_DIAG(1)	VDS_LS3_DIAG(1)	VDS_LS2_DIAG	VDS_LS1_DIAG	
0X0D	DIAGCR1	MSB	-	DGWG	DGSPIERR	DGVDHOV	DGVDHUV	DGTW	DGTSD	DGCPLOW	RW
		LSB	RES	RES	RES	RES	DGVDSHS4(1)	DGVDSHS3(1)	DGVDSHS2	DGVDSHS1	
0X0E	DIAGCR2	MSB	-	RES	RES	RES	RES	DGVDSLS4(1)	DGVDSLS3(1)	DGVDSLS2	RW
		LSB	DGVDSLS1	RES	RES	RES	RES	RES	RES	RES	
0X0F	WDGTRDIS	MSB	-	WDGTRDIS [14]	WDGTRDIS [13]	WDGTRDIS [12]	WDGTRDIS [11]	WDGTRDIS [10]	WDGTRDIS [9]	WDGTRDIS [8]	WO
		LSB	WDGTRDIS [7]	WDGTRDIS [6]	WDGTRDIS [5]	WDGTRDIS [4]	WDGTRDIS [3]	WDGTRDIS [2]	WDGTRDIS [1]	WDGTRDIS [0]	
0X0F	WDGTRDIS	MSB	-	RES	RES	RES	RES	RES	RES	RES	RO

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Addr.	Name	Bits	15	14	13	12	11	10	9	8	Mode
			7	6	5	4	3	2	1	0	
0X0F	WDGTRDIS	LSB	RES	RES	RES	RES	WDGSTATUS	WDGINF [3]	WDGINF [1]	WDGINF [0]	RO
0X10	HB1_MODE_ CFG	MSB	-	RES	RES	DT1 [2]	DT1 [1]	DT1 [0]	STRONG_ON_ WHEEL1	HB_IDIAG1 [1]	RW
		LSB	HB_IDIAG1 [0]	HB_PWM1 [2]	HB_PWM1 [1]	HB_PWM1 [0]	HB_MODE1 [1]	HB_MODE1 [0]	HB_WHEEL1 [1]	HB_WHEEL1 [0]	
0X11	HB1_DRIVER_ CFG	MSB	-	RES	VSTEP2_CONF1 [1]	VSTEP2_CONF1 [0]	ISTEP3_CONF1 [3]	ISTEP3_CONF1 [2]	ISTEP3_CONF1 [1]	ISTEP3_CONF1 [0]	RW
		LSB	ISTEP2_CONF1 [3]	ISTEP2_CONF1 [2]	ISTEP2_CONF1 [1]	ISTEP2_CONF1 [0]	ISTEP1_CONF1 [3]	ISTEP1_CONF1 [2]	ISTEP1_CONF1 [1]	ISTEP1_CONF1 [0]	
0X12	HB1_DIAG_CFG	MSB	-	RES	RES	RES	RES	VDS_CONF1 [3]	VDS_CONF1 [2]	VDS_CONF1 [1]	RW
		LSB	VDS_CONF1 [0]	VDS_BLANK1 [3]	VDS_BLANK1 [2]	VDS_BLANK1 [1]	VDS_BLANK1 [0]	VDS_FILT1 [2]	VDS_FILT1 [1]	VDS_FILT1 [0]	
0x13	HB1_TURN_OFF_CFG	MSB	-	RES	RES	RES	RES	RES	GENMODE1 [1]	GENMODE1 [0]	RW
		LSB	RES	RES	HB_FAULT1 [1]	HB_FAULT1 [0]	ISTEP2_OFF_ CONF1 [3]	ISTEP2_OFF_ CONF1 [2]	ISTEP2_OFF_ CONF1 [1]	ISTEP2_OFF_ CONF1 [0]	
0X14	HB2_MODE_ CFG	MSB	-	RES	RES	DT2 [2]	DT2 [1]	DT2 [0]	STRONG_ON_ WHEEL2	HB_IDIAG2 [1]	RW
		LSB	HB_IDIAG2 [0]	HB_PWM2 [2]	HB_PWM2 [1]	HB_PWM2 [0]	HB_MODE2 [1]	HB_MODE2 [0]	HB_WHEEL2 [1]	HB_WHEEL2 [0]	
0X15	HB2_DRIVER_ CFG	MSB	-	RES	VSTEP2_CONF2 [1]	VSTEP2_CONF2 [0]	ISTEP3_CONF2 [3]	ISTEP3_CONF2 [2]	ISTEP3_CONF2 [1]	ISTEP3_CONF2 [0]	RW
		LSB	ISTEP2_CONF2 [3]	ISTEP2_CONF2 [2]	ISTEP2_CONF2 [1]	ISTEP2_CONF2 [0]	ISTEP1_CONF2 [3]	ISTEP1_CONF2 [2]	ISTEP1_CONF2 [1]	ISTEP1_CONF2 [0]	
0X16	HB2_DIAG_CFG	MSB	-	RES	RES	RES	RES	VDS_CONF2 [3]	VDS_CONF2 [2]	VDS_CONF2 [1]	RW
		LSB	VDS_CONF2 [0]	VDS_BLANK2 [3]	VDS_BLANK2 [2]	VDS_BLANK2 [1]	VDS_BLANK2 [0]	VDS_FILT2 [2]	VDS_FILT2 [1]	VDS_FILT2 [0]	
0x17	HB2_TURN_OFF_CFG	MSB	-	RES	RES	RES	RES	RES	GENMODE2 [1]	GENMODE2 [0]	RW
		LSB	RES	RES	HB_FAULT2 [1]	HB_FAULT2 [0]	ISTEP2_OFF_ CONF2 [3]	ISTEP2_OFF_ CONF2 [2]	ISTEP2_OFF_ CONF2 [1]	ISTEP2_OFF_ CONF2 [0]	
0X18	HB3_MODE_ CFG(1)	MSB	-	RES	RES	DT3 [2]	DT3 [1]	DT3 [0]	STRONG_ON_ WHEEL3	HB_IDIAG3 [1]	RW
		LSB	HB_IDIAG3 [0]	HB_PWM3 [2]	HB_PWM3 [1]	HB_PWM3 [0]	HB_MODE3 [1]	HB_MODE3 0]	HB_WHEEL3 [1]	HB_WHEEL3 [0]	
0X19	HB3_DRIVER_ CFG(1)	MSB	-	RES	VSTEP2_CONF3 [1]	VSTEP2_CONF3 [0]	ISTEP3_CONF3 [3]	ISTEP3_CONF3 [2]	ISTEP3_CONF3 [1]	ISTEP3_CONF3 [0]	RW
		LSB	ISTEP2_CONF3 [3]	ISTEP2_CONF3 [2]	ISTEP2_CONF3 [1]	ISTEP2_CONF3 [0]	ISTEP1_CONF3 [3]	ISTEP1_CONF3 [2]	ISTEP1_CONF3 [1]	ISTEP1_CONF3 [0]	
0X1A	HB3_DIAG_CFG(1)	MSB	-	RES	RES	RES	RES	VDS_CONF3 [3]	VDS_CONF3 [2]	VDS_CONF3 [1]	RW
		LSB	VDS_CONF3 [0]	VDS_BLANK3 [3]	VDS_BLANK3 [2]	VDS_BLANK3 [1]	VDS_BLANK3 [0]	VDS_FILT3 [2]	VDS_FILT3 [1]	VDS_FILT3 [0]	
0x1B	HB3_TURN_OFF_CFG(1)	MSB	-	RES	RES	RES	RES	RES	GENMODE3 [1]	GENMODE3 [0]	RW
		LSB	RES	RES	HB_FAULT3 [1]	HB_FAULT3 [0]	ISTEP2_OFF_ CONF3 [3]	ISTEP2_OFF_ CONF3 [2]	ISTEP2_OFF_ CONF3 [1]	ISTEP2_OFF_ CONF3 [0]	
0X1C	HB4_MODE_ CFG(1)	MSB	-	RES	RES	DT4 [2]	DT4 [1]	DT4 [0]	STRONG_ON_ WHEEL4	HB_IDIAG4 [1]	RW
		LSB	HB_IDIAG4 [0]	HB_PWM4 [2]	HB_PWM4 [1]	HB_PWM4 [0]	HB_MODE4 [1]	HB_MODE4 [0]	HB_WHEEL4 [1]	HB_WHEEL4 [0]	

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Addr.	Name	Bits	15	14	13	12	11	10	9	8	Mode
			7	6	5	4	3	2	1	0	
0X1D	HB4_DRIVER_ CFG(1)	MSB	-	RES	VSTEP2_CONF4 [1]	VSTEP2_CONF4 [0]	ISTEP3_CONF4 [3]	ISTEP3_CONF4 [2]	ISTEP3_CONF4 [1]	ISTEP3_CONF4 [0]	RW
		LSB	ISTEP2_CONF4 [3]	ISTEP2_CONF4 [2]	ISTEP2_CONF4 [1]	ISTEP2_CONF4 [0]	ISTEP1_CONF4 [3]	ISTEP1_CONF4 [2]	ISTEP1_CONF4 [1]	ISTEP1_CONF4 [0]	
0X1E	HB4_DIAG_CFG(1)	MSB	-	RES	RES	RES	RES	VDS_CONF4 [3]	VDS_CONF4 [2]	VDS_CONF4 [1]	RW
		LSB	VDS_CONF4 [0]	VDS_BLANK4 [3]	VDS_BLANK4 [2]	VDS_BLANK4 [1]	VDS_BLANK4 [0]	VDS_FILT4 [2]	VDS_FILT4 [1]	VDS_FILT4 [0]	
0x1F	HB4_TURN_OFF_CFG(1)	MSB	-	RES	RES	RES	RES	RES	GENMODE4 [1]	GENMODE4 [0]	RW
		LSB	RES	RES	HB_FAULT4 [1]	HB_FAULT4 [0]	ISTEP2_OFF_ CONF4 [3]	ISTEP2_OFF_ CONF4 [2]	ISTEP2_OFF_ CONF4 [1]	ISTEP2_OFF_ CONF4 [0]	
0x30	OUT_ENABLE	MSB	-	RES	RES	RES	RES	RES	RES	RES	RW
		LSB	RES	RES	RES	RES	OUT4(1)	OUT3(1)	OUT2	OUT1	

1. *Available in STDRIVE141 only*

9.2 Status registers

Table 31. DSR0 (0x01) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (CR)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RSTB	SPI_ERROR	WDG_ERROR	REVISION_ID [7]	REVISION_ID [6]	REVISION_ID [5]	REVISION_ID [4]
Reset bit flag	SPI fault flag	Watchdog fault flag	Revision ID flag [7]	Revision ID flag [6]	Revision ID flag [5]	Revision ID flag [4]

Table 32. DSR0 (0x01) MSB description

Bit	Name	Description
14	RSTB	RESET bit flag 1 ⇒ Device exiting the POR. This indicates that all the device registers have been reset. 0 ⇒ Device not exiting the POR It is automatically cleared after the first valid SPI communication frame has been received following the reset
13	SPI_ERROR	SPI fault flag 0 ⇒ No SPI failure detected 1 ⇒ SPI failure detected It is automatically cleared at the first valid SPI communication frame
12	WDG_ERROR	Watchdog fault flag 0 ⇒ No WDG failure detected

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Bit	Name	Description
		1 ⇒ WDG failure detected
11	REVISION_ID [7]	Revision ID bit [7] Version ID to identify the silicon version
10	REVISION_ID [6]	Revision ID bit [6] Version ID to identify the silicon version
9	REVISION_ID [5]	Revision ID bit [5] Version ID to identify the silicon version
8	REVISION_ID [4]	Revision ID bit [4] Version ID to identify the silicon version

Table 33. DSR0 (0x01) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
REVISION_ID [3]	REVISION_ID [2]	REVISION_ID [1]	REVISION_ID [0]	DEVICE_ID [3]	DEVICE_ID [2]	DEVICE_ID [1]	DEVICE_ID [0]
Revision ID flag [3]	Revision ID flag [2]	Revision ID flag [1]	Revision ID flag [0]	Device ID flag [3]	Device ID flag [2]	Device ID flag [1]	Device ID flag [0]

Table 34. DSR0 (0x01) LSB description

Bit	Name	Description
7	REVISION_ID [3]	Revision ID bit [3] Version ID to identify the silicon version
6	REVISION_ID [2]	Revision ID bit [2] Version ID to identify the silicon version
5	REVISION_ID [1]	Revision ID bit [1] Version ID to identify the silicon version
4	REVISION_ID [0]	Revision ID bit [0] Version ID to identify the silicon version
3	DEVICE_ID [3]	Device ID bit [3] Device ID to identify the STDRIVE141 device
2	DEVICE_ID [2]	Device ID bit [2] Device ID to identify the STDRIVE141 device
1	DEVICE_ID [1]	Device ID bit [1]

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Bit	Name	Description
		Device ID to identify the STDRIVE141 device
0	DEVICE_ID [0]	Device ID bit [0] Device ID to identify the STDRIVE141 device

Table 35. DSR1 (0x02) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (CR)	0 (CR)	0 (CR)	0 (CR)	0 (CR)	0 (RO)
RES	VDHOV	VDHUV	VDDOV	TW	TSD	DIAGCR
Reserved	VDH overvoltage flag	VUH overvoltage flag	VDD overvoltage flag	Thermal warning flag	Thermal shutdown flag	DIAGN flag

Table 36. DSR1 (0x02) MSB description

Bit	Name	Description
14	RES	Reserved
13	VDHOV	VDH overvoltage flag This flag is set and latched as soon as an overvoltage is detected on VDH supply. It can be cleared by SPI only if the source of the fault is no longer present. It is automatically cleared at the first valid SPI communication frame
12	VDHUV	VDH undervoltage flag This flag is set and latched as soon as an undervoltage is detected on VDH supply. It can be cleared by SPI only if the source of the fault is no longer present. It is automatically cleared at the first valid SPI communication frame
11	VDDOV	VDD overvoltage fault flag This flag is set and latched as soon as an overvoltage is detected on VDD supply. It can be cleared by SPI only if the source of the fault is no longer present. It is automatically cleared at the first valid SPI communication frame
10	TW	Thermal warning flag This flag is set and latched as soon as the device junction temperature exceeds the TW threshold for a time longer than the corresponding filter time. It can be cleared by SPI only if the source of the fault is no longer present. It is automatically cleared at the first valid SPI communication frame
9	TSD	Thermal shutdown flag This flag is set and latched as soon as the device junction temperature exceeds the TSD threshold for a time longer than the corresponding filter time. It can be cleared by SPI only if the source of the fault is no longer present. It is automatically cleared at the first valid SPI communication frame
8	DIAGCR	DIAGN flag This flag is set as soon as the DIAGN pin is activated. It is automatically cleared as soon as the DIAGN is deactivated

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Table 37. **DSR1 (0x02) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (CR)	0 (CR)	0 (CR)	0 (CR)
RES	RES	RES	RES	VDSHS4	VDSHS3	VDSHS2	VDSHS1
Reserved	Reserved	Reserved	Reserved	VDS monitoring HS4	VDS monitoring HS3	VDS monitoring HS2	VDS monitoring HS1

Table 38. **DSR1 (0x02) LSB description**

Bit	Name	Description
7	RES	Reserved
6	RES	
5	RES	
4	RES	
3	VDSHS4	VDS monitoring flags (available in STDRIVE141 only) Flag VDSHSx (x = 3 or 4) is set and latched as soon as the VDS of the corresponding HS MOSFET exceeds the relative threshold (set by VDS_CONFx, x = 3 or 4) for a time longer than the corresponding filtering time or blanking filtering time, where the blanking time is applicable. It can be cleared by SPI only if the source of the fault is no longer present
2	VDSHS3	
1	VDSHS2	VDS monitoring flags Flag VDSHSx (x = 1 or 2) is set and latched as soon as the VDS of the corresponding HS MOSFET exceeds the relative threshold (set by VDS_CONFx, x = 1 or 2) for a time longer than the corresponding filtering time or blanking filtering time, where the blanking time is applicable. It can be cleared by SPI only if the source of the fault is no longer present
0	VDSHS1	

Table 39. **DSR2 (0x03) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 40. **DSR2 (0x03) MSB description**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	

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Bit	Name	Description
10	RES	Reserved
9	RES	
8	RES	

Table 41. DSR2 (0x03) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (CR)	0 (CR)	0 (CR)	0 (CR)	0 (CR)
RES	RES	RES	VDSLS4	VDSLS3	VDSLS2	VDSLS1	CPLOW
Reserved	Reserved	Reserved	VDS monitoring LS4	VDS monitoring LS3	VDS monitoring LS2	VDS monitoring LS1	CP LOW flag

Table 42. DSR2 (0x03) LSB description

Bit	Name	Description
7	RES	Reserved
6	RES	
5	RES	
4	VDSLS4	VDS monitoring flags (available in STDRIVE141 only)
3	VDSLS3	Flag VDSLSx (x = 3 or 4) is set and latched as soon as the VDS of the corresponding LS MOSFET exceeds the relative threshold (set by VDS_CONFx, x = 3 or 4) for a time longer than the corresponding filtering time or blanking filtering time, where the blanking time is applicable. It can be cleared by SPI only if the source of the fault is no longer present
2	VDSLS2	VDS monitoring flags
1	VDSLS1	Flag VDSLSx (x = 1 or 2) is set and latched as soon as the VDS of the corresponding LS MOSFET exceeds the relative threshold (set by VDS_CONFx, x = 1 or 2) for a time longer than the corresponding filtering time or blanking filtering time, where the blanking time is applicable. It can be cleared by SPI only if the source of the fault is no longer present
0	CPLOW	CP low flag If the CP_LOW_CONFIG control bit is set to one, the CPLOW status flag becomes a status bit (set and reset automatically) and the gate drivers come out of the forced disabled mode automatically upon recovery from the charge pump low-voltage condition. In this case, the status bit is automatically cleared as soon as the charge pump output voltage is no longer below the low-voltage threshold for a time longer than t_{CP} If the CP_LOW_CONFIG control bit is set to zero, the gate drivers come out of the forced disabled mode only once the charge pump low-voltage flag CPLOW is cleared via SPI. The charge pump low-voltage flag CPLOW can be cleared by a SPI “read and clear” command only if the charge pump low-voltage condition is no longer present, namely if $V_{CP} > V_{CP\_LOW}$ for a time longer than t_{CP}

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9.3 Control registers

Table 43. **GLOBAL_CFG (0x04) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	OSC_SS_DIS	DIAGN_ACTIVE_ LEVEL	DIAGOFF_CURR_ SEL	VDS_OFFSET_ ENABLE
Reserved	Reserved	Reserved	Spread spectrum enable	DIAGN pin active level	DIAGOFF current selection	VDS offset enable

Table 44. **GLOBAL_CFG (0x04) MSB description**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	OSC_SS_DIS	Spread spectrum enable 0 ⇒ Spread spectrum enabled 1 ⇒ Spread spectrum disabled
10	DIAGN_ACTIVE_ LEVEL	DIAGN pin active level 0 ⇒ DIAGN PIN ACTIVE LOW 1 ⇒ DIAGN PIN ACTIVE HIGH
9	DIAGOFF_CURR_ SEL	DIAGOFF current selection 0 ⇒ 1 mA 1 ⇒ 2 mA
8	VDS_OFFSET_ ENABLE	Offset of 6 mV on the V_{ds} measurements. To be added in case of a short circuit to be measured 0 ⇒ No added offset 1 ⇒ Offset added

Table 45. **GLOBAL_CFG (0x04) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	1 (RW)	0 (RW)	0 (RW)	0 (RO)
DTP_REF	OVTS	OUTE	CP_LOW_CONFIG	CPFDD	EN_PWM1	EN_PWM2	RES
Cross current protection time reference	V_{DH} overvoltage protection threshold	Outputs enable	CP low configuration	CP frequency enables dithering	PWM1 enable	PWM2 enable	Reserved

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Table 46. GLOBAL_CFG (0x04) LSB description

Bit	Name	Description
7	DTP_REF	Cross current protection time reference 0 ⇒ the dead time calculation starts from the switch-off command 1 ⇒ the dead time calculation starts when V_{gs} reaches VSTEP1x
6	OVTS	VDH overvoltage protection threshold 0 ⇒ V_{DH} overvoltage threshold 1 (V_{DHOVT1}) selected 1 ⇒ V_{DH} overvoltage threshold 2 (V_{DHOVT2}) selected
5	OUTE	Outputs enable 0 ⇒ all the gate drivers are OFF independently from the OUTEx bits setting 1 ⇒ the gate drivers can be put OFF or ON according to the OUTEx bits setting
4	CP_LOW_CONFIG	CP low configuration 0 ⇒ the gate drivers come out of the forced disabled mode only once the charge pump low-voltage flag CPLOW is cleared via SPI 1 ⇒ CPLOW status flag becomes a status bit (set and reset automatically) and the gate drivers come out of the forced disabled mode automatically upon recovery from the charge pump low-voltage condition
3	CPFDD	Charge pump frequency dithering 0 ⇒ charge pump dithering disabled 1 ⇒ charge pump dithering enabled
2	EN_PWM1	PWM1 enable 0 ⇒ PWM1 disabled 1 ⇒ PWM1 enabled
1	EN_PWM2	PWM2 enable 0 ⇒ PWM2 disabled 1 ⇒ PWM2 enabled
0	RES	Reserved

Table 47. CSO_CFG (0x05) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RO)	0 (RW)
RES	RES	RES	RES	CSO_GAIN_SEL1	RES	CSOSIG1
Reserved	Reserved	Reserved	Reserved	CSO1 gain selection	Reserved	CSO1 Vds mapping

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Table 48. **CSO_CFG (0x05) MSB description**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	CSO_GAIN_SEL1	CSO1 gain selection 0 ⇒ CSO gain = 1.5 1 ⇒ CSO gain = 3
9	RES	Reserved
8	CSOSIG1	CSO1 V_{ds} mapping 0 ⇒ V_{ds} of the HSx mapped on CSO1 (to use in combination with CSOSHx) 1 ⇒ V_{ds} of the LSx mapped on CSO1 (to use in combination with CSOSHx)

Table 49. **CSO_CFG (0x05) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RW)	0 (RO)	0 (RO)	1 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	CSOEN1	RES	RES	RES	RES	CSOSH1 [1]	CSOSH1 [0]
Reserved	CSO1 enable	Reserved	Reserved	Reserved	Reserved	Mapping on CSO1 [1]	Mapping on CSO1 [0]

Table 50. **CSO_CFG (0x05) LSB description**

Bit	Name	Description
7	RES	Reserved
6	CSOEN1	CSO1 enable 0 ⇒ CSO1 output disabled 1 ⇒ CSO1 output enabled
5	RES	Reserved
4	RES	
3	RES	
2	RES	
1	CSOSH1 [1]	V_{ds} mapping on CSO1
0	CSOSH1 [0]	00 ⇒ V_{ds} of HB1 mapped on CSO1

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Bit	Name	Description
		01 ⇒ V_{ds} of HB2 mapped on CSO1 10 ⇒ V_{ds} of HB3 mapped on CSO1 (STDRIVE141 only) 11 ⇒ V_{ds} of HB4 mapped on CSO1 (STDRIVE141 only)

Table 51. TEMP_CFG (0x06) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 52. TEMP_CFG (0x06) MSB description

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	RES	
9	RES	
8	RES	

Table 53. TEMP_CFG (0x06) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	1 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	ITEMP_ CONF2 [1]	ITEMP_ CONF2 [0]	ITEMP_ CONF1 [1]	ITEMP_ CONF1 [0]
Reserved	Reserved	Reserved	Reserved	Itemp2 configuration [1]	Itemp2 configuration [0]	Itemp1 configuration [1]	Itemp1 configuration [0]

Table 54. TEMP_CFG (0x06) LSB description

Bit	Name	Description
7	RES	Reserved
6	RES	

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Bit	Name	Description
5	RES	Reserved
4	RES	
3	ITEMP_CONF2 [1]	Configuration of the current of temperature sensor 2 00 ⇒ 250 µA 01 ⇒ 500 µA 10 ⇒ 750 µA 11 ⇒ 1000 µA
2	ITEMP_CONF2 [0]	
1	ITEMP_CONF1 [1]	Configuration of the current of temperature sensor 1 00 ⇒ 250 µA 01 ⇒ 500 µA 10 ⇒ 750 µA 11 ⇒ 1000 µA
0	ITEMP_CONF1 [0]	

Table 55. TEMP1_READ (0x07) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	TEMP1_READ [10]	TEMP1_READ [9]	TEMP1_READ [8]
Reserved	Reserved	Reserved	Reserved	Temp1 read bit [10]	Temp1 read bit [9]	Temp1 read bit [8]

Table 56. TEMP1_READ (0x07) MSB description

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	TEMP1_READ [10]	ADC output bits for temperature sensor 1
9	TEMP1_READ [9]	
8	TEMP1_READ [8]	

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Table 57. **TEMP1_READ (0x07) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
TEMP1_ READ [7]	TEMP1_ READ [6]	TEMP1_ READ [5]	TEMP1_ READ [4]	TEMP1_ READ [3]	TEMP1_ READ [2]	TEMP1_ READ [1]	TEMP1_ READ [0]
Temp1 read bit [7]	Temp1 read bit [6]	Temp1 read bit [5]	Temp1 read bit [4]	Temp1 read bit [3]	Temp1 read bit [2]	Temp1 read bit [1]	Temp1 read bit [0]

Table 58. **TEMP1_READ (0x07) LSB description**

Bit	Name	Description
7	TEMP1_READ [7]	ADC output bits for temperature sensor 1
6	TEMP1_READ [6]	
5	TEMP1_READ [5]	
4	TEMP1_READ [4]	
3	TEMP1_READ [3]	
2	TEMP1_READ [2]	
1	TEMP1_READ [1]	
0	TEMP1_READ [0]	

Table 59. **TEMP2_READ (0x08) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	TEMP2_READ [10]	TEMP2_READ [9]	TEMP2_READ [8]
Reserved	Reserved	Reserved	Reserved	Temp2 read bit [10]	Temp2 read bit [9]	Temp2 read bit [8]

Table 60. **TEMP2_READ (0x08) MSB description**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	TEMP2_READ [10]	ADC output bits for temperature sensor 2
9	TEMP2_READ [9]	

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Bit	Name	Description
8	TEMP2_READ [8]	ADC output bits for temperature sensor 2

Table 61. TEMP2_READ (0x08) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
TEMP2_ READ [7]	TEMP2_ READ [6]	TEMP2_ READ [5]	TEMP2_ READ [4]	TEMP2_ READ [3]	TEMP2_ READ [2]	TEMP2_ READ [1]	TEMP2_ READ [0]
Temp2 read bit [7]	Temp2 read bit [6]	Temp2 read bit [5]	Temp2 read bit [4]	Temp2 read bit [3]	Temp2 read bit [2]	Temp2 read bit [1]	Temp2 read bit [0]

Table 62. TEMP2_READ (0x08) LSB description

Bit	Name	Description
7	TEMP2_READ [7]	ADC output bits for temperature sensor 2
6	TEMP2_READ [6]	
5	TEMP2_READ [5]	
4	TEMP2_READ [4]	
3	TEMP2_READ [3]	
2	TEMP2_READ [2]	
1	TEMP2_READ [1]	
0	TEMP2_READ [0]	

Table 63. DIAG_OFF_HS (0x0B) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 64. DIAG_OFF_HS (0x0B) MSB description

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	

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Bit	Name	Description
11	RES	Reserved
10	RES	
9	RES	
8	RES	

Table 65. DIAG_OFF_HS (0x0B) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	VDS_HS4	VDS_HS3	VDS_HS2	VDS_HS1
Reserved	Reserved	Reserved	Reserved	VDS HS4 bit	VDS HS3 bit	VDS HS2 bit	VDS HS1 bit

Table 66. DIAG_OFF_HS (0x0B) LSB description

Bit	Name	Description
7	RES	Reserved
6	RES	
5	RES	
4	RES	
3	VDS_HS4_DIAG	Status of the HSx comparator during diag off, with a symmetric filter of 200 µs (available in STDRIVE141 only) 0 ⇒ LOW 1 ⇒ HIGH
2	VDS_HS3_DIAG	
1	VDS_HS2_DIAG	Status of the HSx comparator during diag off, with a symmetric filter of 200 µs 0 ⇒ LOW 1 ⇒ HIGH
0	VDS_HS1_DIAG	

Table 67. DIAG_OFF_LS (0x0C) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Table 68. **DIAG_OFF_LS (0x0C) MSB description**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	RES	
9	RES	
8	RES	

Table 69. **DIAG_OFF_LS (0x0C) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)
RES	RES	RES	RES	VDS_LS4_DIAG	VDS_LS3_DIAG	VDS_LS2_DIAG	VDS_LS1_DIAG
Reserved	Reserved	Reserved	Reserved	VDS LS4 bit	VDS LS3 bit	VDS LS2 bit	VDS LS1 bit

Table 70. **DIAG_OFF_LS (0x0C) LSB description**

Bit	Name	Description
7	RES	Reserved
6	RES	
5	RES	
4	RES	
3	VDS_LS4_DIAG	Status of the LSx comparator during diag off, with a symmetric filter of 200 µs (available in STDRIVE141 only) 0 ⇒ LOW 1 ⇒ HIGH
2	VDS_LS3_DIAG	
1	VDS_LS2_DIAG	Status of the LSx comparator during diag off, with a symmetric filter of 200 µs 0 ⇒ LOW 1 ⇒ HIGH
0	VDS_LS1_DIAGRe	

Table 71. **DIAGCR1 (0x0D) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)	1 (RW)

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Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
DGWDG	DGSPIERR	DGVDHOV	DGVDHUV	DGTW	DGTSD	DGCPLOW
Diagnostic WDG_ERR enable bit	Diagnostic SPI_ERR enable bit	Diagnostic VDHOV enable bit	Diagnostic VDHUV enable bit	Diagnostic TW enable bit	Diagnostic TSD enable bit	Diagnostic CPLOW enable bit

Table 72. DIAGCR1 (0x0D) MSB description

Bit	Name	Description
14	DGWDG	Diagnostic WDG ERROR enable control bit Setting this bit enables the WDG_ERR status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ WDG_ERR mapped on the DIAGN pin
13	DGSPIERR	Diagnostic SPI ERROR enable control bit Setting this bit enables the SPI_ERR status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ SPI_ERR mapped on the DIAGN pin
12	DGVDHOV	Diagnostic VDHOV enable control bit Setting this bit enables the VDHOV status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ VDHOV mapped on the DIAGN pin
11	DGVDHUV	Diagnostic VDHUV enable control bit Setting this bit enables the VDHUV status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ VDHUV mapped on the DIAGN pin
10	DGTW	Diagnostic TW enable control bit Setting this bit enables the TW status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ TW mapped on the DIAGN pin
9	DGTSD	Diagnostic TSD enable control bit Setting this bit enables the TSD status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ TSD mapped on the DIAGN pin
8	DGCPLOW	Diagnostic CPLOW enable control bit Setting this bit enables the CPLOW status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping

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Bit	Name	Description
		1 ⇒ CPLOW mapped on the DIAGN pin

Table 73. DIAGCR1 (0x0D) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 (RO)	1 (RO)	1 (RO)	1 (RO)	1 (RW)	1 (RW)	1 (RW)	1 (RW)
RES	RES	RES	RES	DGVDSHS4	DGVDSHS3	DGVDSHS2	DGVDSHS1
Reserved	Reserved	Reserved	Reserved	Diagnostic enable VDS_HS4 bit	Diagnostic enable VDS_HS3 bit	Diagnostic enable VDS_HS2 bit	Diagnostic enable VDS_HS1 bit

Table 74. DIAGCR1 (0x0D) LSB description

Bit	Name	Description
7	RES	Reserved
6	RES	
5	RES	
4	RES	
3	DGVDSHS4	Diagnostic VDS_HS4 enable control bit (available in STDRIVE 141 only) Setting this bit enables the VDS_HS4 status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ VDS_HS4 mapped on the DIAGN pin
2	DGVDSHS3	Diagnostic VDS_HS3 enable control bit (available in STDRIVE 141 only) Setting this bit enables the VDS_HS3 status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ VDS_HS3 mapped on the DIAGN pin
1	DGVDSHS2	Diagnostic VDS_HS2 enable control bit Setting this bit enables the VDS_HS2 status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ VDS_HS2 mapped on the DIAGN pin
0	DGVDSHS1	Diagnostic VDS_HS1 enable control bit Setting this bit enables the VDS_HS1 status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ VDS_HS1 mapped on the DIAGN pin

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Table 75. **DIAGCR2 (0x0E) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
1 (RO)	1 (RO)	1 (RO)	1 (RO)	1 (RW)	1 (RW)	1 (RW)
RES	RES	RES	RES	DGVDSLS4	DGVDSLS3	DGVDSLS2
Reserved	Reserved	Reserved	Reserved	Diagnostic enable VDS_LS4 bit	Diagnostic enable VDS_LS3 bit	Diagnostic enable VDS_LS2 bit

Table 76. **DIAGCR2 (0x0E) MSB description**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	DGVDSLS4	Diagnostic VDS_LS4 enable control bit (available in STDRIVE 141 only) Setting this bit enables the VDS_LS4 status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ VDS_LS4 mapped on the DIAGN pin
9	DGVDSLS3	Diagnostic VDS_LS3 enable control bit (available in STDRIVE 141 only) Setting this bit enables the VDS_LS3 status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ VDS_LS3 mapped on the DIAGN pin
8	DGVDSLS2	Diagnostic VDS_LS2 enable control bit Setting this bit enables the VDS_LS2 status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ VDS_LS2 mapped on the DIAGN pin

Table 77. **DIAGCR2 (0x0E) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1 (RW)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
DGVDSLS1	RES	RES	RES	RES	RES	RES	RES
Diagnostic enable VDS_LS1 bit	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

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Table 78. DIAGCR2 (0x0E) LSB description

Bit	Name	Description
7	DGVDSLS1	Diagnostic VDS_LS1 enable control bit Setting this bit enables the VDS_LS1 status flag to be mapped on the diagnostic output pin (DIAGN) 0 ⇒ no mapping 1 ⇒ VDS_LS1 mapped on the DIAGN pin
6	RES	Reserved
5	RES	
4	RES	
3	RES	
2	RES	
1	RES	
0	RES	

Table 79. WDGTRDIS (0x0F) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (WO)	0 (WO)	0 (WO)	0 (WO)	0 (WO)	0 (WO)	0 (WO)
WDGTRDIS [14]	WDGTRDIS [13]	WDGTRDIS [12]	WDGTRDIS [11]	WDGTRDIS [10]	WDGTRDIS [9]	WDGTRDIS [8]
Watchdog trigger [14]	Watchdog trigger [13]	Watchdog trigger [12]	Watchdog trigger [11]	Watchdog trigger [10]	Watchdog trigger [9]	Watchdog trigger [8]

Table 80. WDGTRDIS (0x0F) MSB description

Bit	Name	Description
14	WDGTRDIS [14]	Watchdog trigger ⇒ the device must alternatively receive 5555h and 2AAAh. The first word must be 5555h Watchdog disable ⇒ the device must receive, in the right order, 2F6Bh (first key word) and 1097h (second key word) Watchdog enable ⇒ the device must receive, in the right order, 5C99h (first key word) and 4360h (second key word)
13	WDGTRDIS [13]	
12	WDGTRDIS [12]	
11	WDGTRDIS [11]	
10	WDGTRDIS [10]	
9	WDGTRDIS [9]	
8	WDGTRDIS [8]	

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Table 81. **WDGTRDIS (0x0F) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (WO)	0 (WO)	0 (WO)	0 (WO)	0 (WO)	0 (WO)	0 (WO)	0 (WO)
WDGTRDIS [7]	WDGTRDIS [6]	WDGTRDIS [5]	WDGTRDIS [4]	WDGTRDIS [3]	WDGTRDIS [2]	WDGTRDIS [1]	WDGTRDIS [0]
Watchdog trigger [7]	Watchdog trigger [6]	Watchdog trigger [5]	Watchdog trigger [4]	Watchdog trigger [3]	Watchdog trigger [2]	Watchdog trigger [1]	Watchdog trigger [0]

Table 82. **WDGTRDIS (0x0F) LSB description**

Bit	Name	Description
7	WDGTRDIS [7]	Watchdog trigger ⇒ the device must alternatively receive 5555h and 2AAAh. The first word must be 5555h Watchdog disable ⇒ the device must receive, in the right order, 2F6Bh (first key word) and 1097h (second key word) Watchdog enable ⇒ the device must receive, in the right order, 5C99h (first key word) and 4360h (second key word)
6	WDGTRDIS [6]	
5	WDGTRDIS [5]	
4	WDGTRDIS [4]	
3	WDGTRDIS [3]	
2	WDGTRDIS [2]	
1	WDGTRDIS [1]	
0	WDGTRDIS [0]	

Table 83. **WDGTRDIS (0x0F) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 84. **WDGTRDIS (0x0F) MSB description**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	RES	
9	RES	

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Bit	Name	Description
8	RES	Reserved

Table 85. WDGTRDIS (0x0F) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	WDGSTATUS	WDGINF [2]	WDGINF [1]	WDGINF [0]
Reserved	Reserved	Reserved	Reserved	Watchdog status	Watchdog inf [2]	Watchdog inf [1]	Watchdog inf [0]

Table 86. WDGTRDIS (0x0F) LSB description

Bit	Name	Description
7	RES	Reserved
6	RES	
5	RES	
4	RES	
3	WDGSTATUS	Watchdog status This bit is enabled if the watchdog has been successfully disabled
2	WDGINF [2]	Watchdog info These bits represent the three least significant bits of the latest write command performed on the same register
1	WDGINF [1]	
0	WDGINF [0]	

Table 87. HB1_MODE_CONFIG (0x10) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	DT1 [2]	DT1 [1]	DT1 [0]	STRONG_ON _WHEEL1	HB_IDIAG1 [1]
Reserved	Reserved	Dead time 1 [2]	Dead time 1 [1]	Dead time 1 [0]	Free-wheeling strong on HB1	HB1 diagnostic current

Table 88. HB1_MODE_CONFIG (0x10) MSB description

Bit	Name	Description
14	RES	Reserved
13	RES	

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Bit	Name	Description
12	DT1 [2]	Dead time of the HB1 000 ⇒ 0.5 µs 001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 16 µs
11	DT1 [1]	
10	DT1 [0]	
9	STRONG_ON_ WHEEL1	Free-wheeling strong ON of the HB1 0 ⇒ Strong on disabled, free-wheeling gate current set to 4 mA 1 ⇒ Strong on enabled, free-wheeling gate current set to 30 mA
8	HB_IDIAG1 [1]	Half-bridge 1 diagnostic currents setting 00 ⇒ Pull-up and pull-down currents off 01 ⇒ Pull-up current off and pull-down current on 10 ⇒ Pull-up current on and pull-down current off 11 ⇒ Pull-up and pull-down currents off

Table 89. HB1_MODE_CONFIG (0x10) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
HB_IDIAG1 [1]	HB_PWM1 [2]	HB_PWM1 [1]	HB_PWM1 [0]	HB_MODE1 [1]	HB_MODE1 [0]	HB_WHEEL1 [1]	HB_WHEEL1 [0]
HB1 diagnostic current	HB1 PWM mapping [2]	HB1 PWM mapping [1]	HB1 PWM mapping [0]	HB1 mode [1]	HB1 mode [0]	HB1 free-wheeling [1]	HB1 free-wheeling [0]

Table 90. HB1_MODE_CONFIG (0x10) LSB description

Bit	Name	Description
7	HB_IDIAG1 [0]	Half-bridge 1 diagnostic currents setting 00 ⇒ Pull-up and pull-down currents off 01 ⇒ Pull-up current off and pull-down current on 10 ⇒ Pull-up current on and pull-down current off 11 ⇒ Pull-up and pull-down currents off

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Bit	Name	Description
6	HB_PWM1 [2]	PWM mapping on HB1
5	HB_PWM1 [1]	This 3-bit register is used to indicate which PWM signal is applied to the HS or LS of the half-bridge 1
4	HB_PWM1 [0]	000 ⇒ LS of HB mapped on PWM1 001 ⇒ LS of HB mapped on PWM2 011 ⇒ HS of HB mapped on PWM1 100 ⇒ HS of HB mapped on PWM2 010 = 101 = 110 = 111 ⇒ No mapping
3	HB_MODE1 [1]	HB1 functionality mode
2	HB_MODE1 [0]	00 ⇒ LS and HS of the HB1 are kept off 01 ⇒ LS of the HB1 is ON (static, no PWM), HS of the HB1 is OFF 10 ⇒ HS of the half-bridge 1 is ON (static, no PWM), LS of the half-bridge is OFF 11 ⇒ LS or HS of the half-bridge is ON according to the HB_PWM1 register
1	HB_WHEEL1 [1]	HB1 free-wheeling mode
0	HB_WHEEL1 [0]	00 = 11 ⇒ No mapping 01 ⇒ Active free-wheeling on HS of the HB 10 ⇒ Active free-wheeling on LS of the HB

Table 91. HB1_DRIVER_CFG (0x11) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	VSTEP2_CONF1 [1]	VSTEP2_CONF1 [0]	ISTEP3_CONF1 [3]	ISTEP3_CONF1 [2]	ISTEP3_CONF1 [1]	ISTEP3_CONF1 [0]
Reserved	HB1 Vstep1 and Vstep2 conf [1]	HB1 Vstep1 and Vstep2 conf [0]	HB1 Istep3 conf [3]	HB1 Istep3 conf [2]	HB1 Istep3 conf [1]	HB1 Istep3 conf [0]

Table 92. HB1_DRIVER_CFG (0x11) MSB description

Bit	Name	Description
14	RES	Reserved
13	VSTEP2_CONF1 [1]	Vstep1 and Vstep2 thresholds configuration of the HB1
12	VSTEP2_CONF1 [0]	These two bits set the Vstep1 and Vstep2 thresholds of the HB1 00 ⇒ Vstep1 = 1.1 V, Vstep2 = 2.67 V for the switch ON 00 ⇒ Vstep1 = 1.3 V, Vstep2 = 3.33 V for the switch OFF 01 ⇒ Vstep1 = 1.1 V, Vstep2 = 3.56 V for the switch ON 01 ⇒ Vstep1 = 1.3 V, Vstep2 = 4.44 V for the switch OFF

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Bit	Name	Description
		10 ⇒ Vstep1 = 2.2 V, Vstep2 = 4.45 V for the switch ON 10 ⇒ Vstep1 = 2.6 V, Vstep2 = 5.55 V for the switch OFF 11 ⇒ Vstep1 = 2.2 V, Vstep2 = 5.34 V for the switch ON 11 ⇒ Vstep1 = 2.6 V, Vstep2 = 6.66 V for the switch OFF
11	ISTEP3_CONF1 [3]	Istep3 configuration of the HB1 0000 ⇒ 2 mA 0001 ⇒ 4 mA 0010 ⇒ 8 mA 0011 ⇒ 12 mA 0100 ⇒ 20 mA 0101 ⇒ 28 mA 0110 ⇒ 36 mA 0111 ⇒ 44 mA 1000 ⇒ 52 mA 1001 ⇒ 60 mA 1010 ⇒ 68 mA 1011 ⇒ 76 mA 1100 ⇒ 84 mA 1101 ⇒ 92 mA 1110 ⇒ 104 mA 1111 ⇒ 120 mA
10	ISTEP3_CONF1 [2]	
9	ISTEP3_CONF1 [1]	
8	ISTEP3_CONF1 [0]	

Table 93. HB1_DRIVER_CFG (0x11) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
ISTEP2_CONF1 [3]	ISTEP2_CONF1 [2]	ISTEP2_CONF1 [1]	ISTEP2_CONF1 [0]	ISTEP1_CONF1 [3]	ISTEP1_CONF1 [2]	ISTEP1_CONF1 [1]	ISTEP1_CONF1 [0]
HB1 Istep3 conf [3]	HB1 Istep3 conf [2]	HB1 Istep3 conf [1]	HB1 Istep3 conf [0]	HB1 Istep3 conf [3]	HB1 Istep3 conf [2]	HB1 Istep3 conf [1]	HB1 Istep3 conf [0]

Table 94. HB1_DRIVER_CFG (0x11) LSB description

Bit	Name	Description
7	ISTEP2_CONF1 [3]	Istep2 configuration of the HB1 for the low to high transition 0000 ⇒ 1 mA 0001 ⇒ 2 mA
6	ISTEP2_CONF1 [2]	
5	ISTEP2_CONF1 [1]	

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Bit	Name	Description
4	ISTEP2_CONF1 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
3	ISTEP1_CONF1 [3]	Istep1 configuration of the HB1 0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
2	ISTEP1_CONF1 [2]	
1	ISTEP1_CONF1 [1]	
0	ISTEP1_CONF1 [0]	

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Table 95. **HB1_DIAG_CFG (0x12) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	(RO)	(RO)	0 (RW)	0 (RW)	0 (RW)
RES	RES	0 RES	0 RES	VDS_CONF1 [3]	VDS_CONF1 [2]	VDS_CONF1 [1]
Reserved	Reserved	Reserved	Reserved	VDS conf of the HB1 [3]	VDS conf of the HB1 [2]	VDS conf of the HB1 [1]

Table 96. **HB1_DIAG_CFG (0x12) MSB description**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	VDS_CONF1 [3]	V_{ds} monitor threshold configuration of the HB1
9	VDS_CONF1 [2]	0000 ⇒ 75 mV
8	VDS_CONF1 [1]	0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V

Table 97. **HB1_DIAG_CFG (0x12) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
VDS_CONF1 [0]	VDS_BLANK1 [3]	VDS_BLANK1 [2]	VDS_BLANK1 [1]	VDS_BLANK1 [0]	VDS_FILT1 [2]	VDS_FILT1 [2]	VDS_FILT1 [2]
VDS conf of the HB1 [0]	VDS blanking time conf [3]	VDS blanking time conf [2]	VDS blanking time conf [1]	VDS blanking time conf [0]	VDS filter time conf [2]	VDS filter time conf [1]	VDS filter time conf [0]

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Table 98. **HB1_DIAG_CFG (0x12) LSB description**

Bit	Name	Description
7	VDS_CONF1 [0]	V_{ds} monitor threshold configuration of the HB1 0000 ⇒ 75 mV 0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V
6	VDS_BLANK1 [3]	V_{ds} blanking time configuration of the HB1 0000 ⇒ 0.625 µs 0001 ⇒ 1 µs 0010 ⇒ 1.25 µs 0011 ⇒ 1.5 µs 0100 ⇒ 2 µs 0101 ⇒ 3 µs 0110 ⇒ 4 µs 0111 ⇒ 5 µs 1000 ⇒ 6 µs 1001 ⇒ 7 µs 1010 ⇒ 8 µs 1x11 ⇒ 0.625 µs
5	VDS_BLANK1 [2]	
4	VDS_BLANK1 [1]	
3	VDS_BLANK1 [0]	
2	VDS_FILT1 [2]	V_{ds} filtering time configuration 000 ⇒ 0.5 µs 001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 0.5 µs
1	VDS_FILT1 [1]	
0	VDS_FILT1 [0]	

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Table 99. **HB1_TURN_OFF_CFG (0x13) MSB**

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	GENMODE1 [1]	GENMODE1 [0]
Reserved	Reserved	Reserved	Reserved	Reserved	GENMODE bit conf [1]	GENMODE bit conf [0]

Table 100. **HB1_TURN_OFF_CFG (0x13) MSB description**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	RES	
9	GENMODE1 [1]	HB1 Gate driver actions when a VDH overvoltage is detected: 00 ⇒ Gate driver off 01 ⇒ HS off, LS on 10 ⇒ Flag only 11 ⇒ Gate driver off
8	GENMODE1 [0]	

Table 101. **HB1_TURN_OFF_CFG (0x13) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	HB_FAULT1 [1]	HB_FAULT1 [0]	ISTEP2_OFF_ CONF1 [3]	ISTEP2_OFF_ CONF1 [2]	ISTEP2_OFF_ CONF1 [1]	ISTEP2_OFF_ CONF1 [0]
Reserved	Reserved	HB1 fault key [1]	HB1 fault key [0]	HB1 Istep2 conf [3]	HB1 Istep2 conf [2]	HB1 Istep2 conf [1]	HB1 Istep2 conf [0]

Table 102. **HB1_TURN_OFF_CFG (0x13) LSB description**

Bit	Name	Description
7	RES	Reserved
6	RES	
5	HB_FAULT1 [1]	HB1 fault key
4	HB_FAULT1 [0]	00 ⇒ No key

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Bit	Name	Description
		00 ⇒ key 1 10 ⇒ key 2 (STDRIVE141 only) 11 ⇒ key 1 + key 2 (STDRIVE141 only)
3	ISTEP2_OFF_CONF1 [3]	Istep2 configuration of the HB1 in case of the switch OFF of the external MOSFET 0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
2	ISTEP2_OFF_CONF1 [2]	
1	ISTEP2_OFF_CONF1 [1]	
0	ISTEP2_OFF_CONF1 [0]	

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Table 103. HB2_MODE_CONFIG (0x14) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	DT2 [2]	DT2 [1]	DT2 [0]	STRONG_ON _WHEEL2	HB_IDIAG2 [1]
Reserved	Reserved	Dead time 2 [2]	Dead time 2 [1]	Dead time 2 [0]	Free-wheeling strong on HB2	HB2 diagnostic current

Table 104. HB2_MODE_CONFIG (0x14) MSB description

Bit	Name	Description
14	RES	Reserved
13	RES	
12	DT2 [2]	Dead time of the HB2

Bit	Name	Description
11	DT2 [1]	000 ⇒ 0.5 µs 001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 16 µs
10	DT2 [0]	
9	STRONG_ON_ WHEEL2	Free-wheeling strong ON of the HB2 0 ⇒ Strong on disabled, free-wheeling gate current set to 4 mA 1 ⇒ Strong on enabled, free-wheeling gate current set to 30 mA
8	HB_IDIAG2 [1]	HB2 diagnostic currents setting 00 ⇒ Pull-up and pull-down currents off 01 ⇒ Pull-up current off and pull-down current on 10 ⇒ Pull-up current on and pull-down current off 11 ⇒ Pull-up and pull-down currents off

Table 105. HB2_MODE_CONFIG (0x14) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
HB_IDIAG2 [1]	HB_PWM2 [2]	HB_PWM2 [1]	HB_PWM2 [0]	HB_MODE2 [1]	HB_MODE2 [0]	HB_WHEEL2 [1]	HB_WHEEL2 [0]
HB2 diagnostic current	HB2 PWM mapping [2]	HB2 PWM mapping [1]	HB2 PWM mapping [0]	HB2 mode [1]	HB2 mode [0]	HB2 free-wheeling [1]	HB2 free-wheeling [0]

Table 106. HB2_MODE_CONFIG (0x14) LSB description

Bit	Name	Description
7	HB_IDIAG2 [0]	Half-bridge 2 diagnostic currents setting 00 ⇒ Pull-up and pull-down currents off 01 ⇒ Pull-up current off and pull-down current on 10 ⇒ Pull-up current on and pull-down current off 11 ⇒ Pull-up and pull-down currents off
6	HB_PWM2 [2]	PWM mapping on HB2 This 3-bit register is used to indicate which PWM signal is applied to the HS or LS of the half-bridge 2

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Bit	Name	Description
5	HB_PWM2 [1]	000 ⇒ LS of HB mapped on PWM1
4	HB_PWM2 [0]	001 ⇒ LS of HB mapped on PWM2 011 ⇒ HS of HB mapped on PWM1 100 ⇒ HS of HB mapped on PWM2 010 = 101 = 110 = 111 ⇒ No mapping
3	HB_MODE2 [1]	HB2 functionality mode
2	HB_MODE2 [0]	00 ⇒ LS and HS of the HB2 are kept off 01 ⇒ LS of the HB2 is ON (static, no PWM), HS of the HB2 is OFF 10 ⇒ HS of the HB2 is ON (static, no PWM), LS of the HB2 is OFF 11 ⇒ LS or HS of the HB2 is ON according to the HB_PWM2 register
1	HB_WHEEL2 [1]	HB2 free-wheeling mode
0	HB_WHEEL2 [0]	00 = 11 ⇒ No mapping 01 ⇒ Active free-wheeling on HS of the HB 10 ⇒ Active free-wheeling on LS of the HB

Table 107. HB2_DRIVER_CFG (0x15) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	VSTEP2_CONF2 [1]	VSTEP2_CONF2 [0]	ISTEP3_CONF2 [3]	ISTEP3_CONF2 [2]	ISTEP3_CONF2 [1]	ISTEP3_CONF2 [0]
Reserved	HB2 Vstep1 and Vstep2 conf [1]	HB2 Vstep1 and Vstep2 conf [0]	HB2 Istep3 conf [3]	HB2 Istep3 conf [2]	HB2 Istep3 conf [1]	HB2 Istep3 conf [0]

Table 108. HB2_DRIVER_CFG (0x15) MSB description

Bit	Name	Description
14	RES	Reserved
13	VSTEP2_CONF2 [1]	Vstep1 and Vstep2 thresholds configuration of the HB2
12	VSTEP2_CONF2 [0]	These two bits set the Vstep1 and Vstep2 thresholds of the HB2 00 ⇒ Vstep1 = 1.1 V, Vstep2 = 2.67 V for the switch ON 00 ⇒ Vstep1 = 1.3 V, Vstep2 = 3.33 V for the switch OFF 01 ⇒ Vstep1 = 1.1 V, Vstep2 = 3.56 V for the switch ON 01 ⇒ Vstep1 = 1.3 V, Vstep2 = 4.44 V for the switch OFF 10 ⇒ Vstep1 = 2.2 V, Vstep2 = 4.45 V for the switch ON 10 ⇒ Vstep1 = 2.6 V, Vstep2 = 5.55 V for the switch OFF 11 ⇒ Vstep1 = 2.2 V, Vstep2 = 5.34 V for the switch ON

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Bit	Name	Description
		11 ⇒ Vstep1 = 2.6 V, Vstep2 = 6.66 V for the switch OFF
11	ISTEP3_CONF2 [3]	Istep3 configuration of the HB2
10	ISTEP3_CONF2 [2]	0000 ⇒ 2 mA
9	ISTEP3_CONF2 [1]	0001 ⇒ 4 mA
8	ISTEP3_CONF2 [0]	0010 ⇒ 8 mA 0011 ⇒ 12 mA 0100 ⇒ 20 mA 0101 ⇒ 28 mA 0110 ⇒ 36 mA 0111 ⇒ 44 mA 1000 ⇒ 52 mA 1001 ⇒ 60 mA 1010 ⇒ 68 mA 1011 ⇒ 76 mA 1100 ⇒ 84 mA 1101 ⇒ 92 mA 1110 ⇒ 104 mA 1111 ⇒ 120 mA

Table 109. HB2_DRIVER_CFG (0x15) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
ISTEP2_CONF2 [3]	ISTEP2_CONF2 [2]	ISTEP2_CONF2 [1]	ISTEP2_CONF2 [0]	ISTEP1_CONF2 [3]	ISTEP1_CONF2 [2]	ISTEP1_CONF2 [1]	ISTEP1_CONF2 [0]
HB2 Istep3 conf [3]	HB2 Istep3 conf [2]	HB2 Istep3 conf [1]	HB2 Istep3 conf [0]	HB2 Istep3 conf [3]	HB2 Istep3 conf [2]	HB2 Istep3 conf [1]	HB2 Istep3 conf [0]

Table 110. HB2_DRIVER_CFG (0x15) LSB description

Bit	Name	Description
7	ISTEP2_CONF2 [3]	Istep2 configuration of the HB2 for the low to high transition
6	ISTEP2_CONF2 [2]	0000 ⇒ 1 mA
5	ISTEP2_CONF2 [1]	0001 ⇒ 2 mA
4	ISTEP2_CONF2 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA

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Bit	Name	Description
		0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
3	ISTEP1_CONF2 [3]	Istep1 configuration of the HB2 0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
2	ISTEP1_CONF2 [2]	
1	ISTEP1_CONF2 [1]	
0	ISTEP1_CONF2 [0]	

Table 111. HB2_DIAG_CFG (0x16) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	VDS_CONF2 [3]	VDS_CONF2 [2]	VDS_CONF2 [1]

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Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reserved	Reserved	Reserved	Reserved	VDS conf of the HB2 [3]	VDS conf of the HB2 [2]	VDS conf of the HB2 [1]

Table 112. HB2_DIAG_CFG (0x16) MSB description

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	VDS_CONF2 [3]	V_{ds} monitor threshold configuration of the HB2
9	VDS_CONF2 [2]	0000 ⇒ 75 mV
8	VDS_CONF2 [1]	0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V

Table 113. HB2_DIAG_CFG (0x16) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
VDS_CONF2 [0]	VDS_BLANK2 [3]	VDS_BLANK2 [2]	VDS_BLANK2 [1]	VDS_BLANK2 [0]	VDS_FILT2 [2]	VDS_FILT2 [2]	VDS_FILT2 [2]
VDS conf of the HB2 [0]	VDS blanking time conf [3]	VDS blanking time conf [2]	VDS blanking time conf [1]	VDS blanking time conf [0]	VDS filter time conf [2]	VDS filter time conf [1]	VDS filter time conf [0]

Table 114. HB2_DIAG_CFG (0x16) LSB description

Bit	Name	Description
7	VDS_CONF2 [0]	V_{ds} monitor threshold configuration of the HB2 0000 ⇒ 75 mV 0001 ⇒ 150 mV 0010 ⇒ 200 mV

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Bit	Name	Description
		0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V
6	VDS_BLANK2 [3]	V_{ds} blanking time configuration of the HB2
5	VDS_BLANK2 [2]	0000 = 0.625 µs
4	VDS_BLANK2 [1]	0001 ⇒ 1 µs
3	VDS_BLANK2 [0]	0010 ⇒ 1.25 µs 0011 ⇒ 1.5 µs 0100 ⇒ 2 µs 0101 ⇒ 3 µs 0110 ⇒ 4 µs 0111 ⇒ 5 µs 1000 ⇒ 6 µs 1001 ⇒ 7 µs 1010 ⇒ 8 µs 1x11 ⇒ 0.625 µs
2	VDS_FILT2 [2]	V_{ds} filtering time configuration of the HB2
1	VDS_FILT2 [1]	000 ⇒ 0.5 µs
0	VDS_FILT2 [0]	001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 0.5 µs

Table 115. HB2_TURN_OFF_CFG (0x17) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)

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Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
RES	RES	RES	RES	RES	GENMODE2 [1]	GENMODE2 [0]
Reserved	Reserved	Reserved	Reserved	Reserved	GENMODE bit conf [1]	GENMODE bit conf [0]

Table 116. HB2_TURN_OFF_CFG (0x17) MSB description

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	RES	
9	GENMODE2 [1]	HB2 Gate driver actions when a VDH overvoltage is detected: 00 ⇒ Gate driver off 01 ⇒ HS off, LS on 10 ⇒ Flag only 11 ⇒ Gate driver off
8	GENMODE2 [0]	

Table 117. HB2_TURN_OFF_CFG (0x17) LSB

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	HB_FAULT2 [1]	HB_FAULT2 [0]	ISTEP2_OFF_ CONF2 [3]	ISTEP2_OFF_ CONF2 [2]	ISTEP2_OFF_ CONF2 [1]	ISTEP2_OFF_ CONF2 [0]
Reserved	Reserved	HB2 fault key [1]	HB2 fault key [0]	HB2 Istep2 conf [3]	HB2 Istep2 conf [2]	HB2 Istep2 conf [1]	HB2 Istep2 conf [0]

Table 118. HB2_TURN_OFF_CFG (0x17) LSB description

Bit	Name	Description
7	RES	Reserved
6	RES	
5	HB_FAULT2 [1]	HB2 fault key 00 ⇒ No key 00 ⇒ key 1 10 ⇒ key 2 (STDRIVE141 only)
4	HB_FAULT2 [0]	

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Bit	Name	Description
		11 ⇒ key 1 + key 2 (STDRIVE141 only)
3	ISTEP2_OFF_CONF2 [3]	Istep2 configuration of the HB2 in case of the switch OFF of the external MOSFET
2	ISTEP2_OFF_CONF2 [2]	0000 ⇒ 1 mA
1	ISTEP2_OFF_CONF2 [1]	0001 ⇒ 2 mA
0	ISTEP2_OFF_CONF2 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA

Table 119. HB3_MODE_CONFIG (0x18) MSB (available in STDRIVE141 only)

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	DT3 [2]	DT3 [1]	DT3 [0]	STRONG_ON _WHEEL3	HB_IDIAG3 [1]
Reserved	Reserved	Dead time 3 [2]	Dead time 3 [1]	Dead time 3 [0]	Free-wheeling strong on HB3	HB3 diagnostic current

Table 120. HB3_MODE_CONFIG (0x18) MSB description (available in STDRIVE141 only)

Bit	Name	Description
14	RES	Reserved
13	RES	
12	DT3 [2]	Dead time of the HB3
11	DT3 [1]	000 ⇒ 0.5 µs
10	DT3 [0]	001 ⇒ 1 µs

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Bit	Name	Description
		010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 16 µs
9	STRONG_ON_ WHEEL3	Free-wheeling strong ON of the HB3 0 ⇒ Strong on disabled, free-wheeling gate current set to 4 mA 1 ⇒ Strong on enabled, free-wheeling gate current set to 30 mA
8	HB_IDIAG3 [1]	Half-bridge 3 diagnostic currents setting 00 ⇒ Pull-up and pull-down currents off 01 ⇒ Pull-up current off and pull-down current on 10 ⇒ Pull-up current on and pull-down current off 11 ⇒ Pull-up and pull-down currents off

Table 121. HB3_MODE_CONFIG (0x18) LSB (available in STDRIVE141 only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
HB_IDIAG3 [1]	HB_PWM3 [2]	HB_PWM3 [1]	HB_PWM3 [0]	HB_MODE3 [1]	HB_MODE3 [0]	HB_WHEEL3 [1]	HB_WHEEL3 [0]
HB3 diagnostic current	HB3 PWM mapping [2]	HB3 PWM mapping [1]	HB3 PWM mapping [0]	HB3 mode [1]	HB3 mode [0]	HB3 free-wheeling [1]	HB3 free-wheeling [0]

Table 122. HB3_MODE_CONFIG (0x18) LSB description (available in STDRIVE141 only)

Bit	Name	Description
7	HB_IDIAG3 [0]	HB3 diagnostic currents setting 00 ⇒ Pull-up and pull-down currents off 01 ⇒ Pull-up current off and pull-down current on 10 ⇒ Pull-up current on and pull-down current off 11 ⇒ Pull-up and pull-down currents off
6	HB_PWM3 [2]	PWM mapping on HB3 This 3-bit register is used to indicate which PWM signal is applied to the HS or LS of the half-bridge 3 000 ⇒ LS of HB mapped on PWM1 001 ⇒ LS of HB mapped on PWM2
5	HB_PWM3 [1]	
4	HB_PWM3 [0]	

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Bit	Name	Description
		011 ⇒ HS of HB mapped on PWM1 100 ⇒ HS of HB mapped on PWM2 010 = 101 = 110 = 111 ⇒ No mapping
3	HB_MODE3 [1]	HB3 functionality mode
2	HB_MODE3 [0]	00 ⇒ LS and HS of the HB3 are kept off 01 ⇒ LS of the HB3 is ON (static, no PWM), HS of the HB3 is OFF 10 ⇒ HS of the HB3 is ON (static, no PWM), LS of the HB3 is OFF 11 ⇒ LS or HS of the HB3 is ON in according to the HB_PWM1 register
1	HB_WHEEL3 [1]	HB3 free-wheeling mode
0	HB_WHEEL3 [0]	00 = 11 ⇒ No mapping 01 ⇒ Active free-wheeling on HS of the HB 10 ⇒ Active free-wheeling on LS of the HB

Table 123. HB3_DRIVER_CFG (0x19) MSB (available in STDRIVE141 only)

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	VSTEP2_CONF3 [1]	VSTEP2_CONF3 [0]	ISTEP3_CONF3 [3]	ISTEP3_CONF3 [2]	ISTEP3_CONF3 [1]	ISTEP3_CONF3 [0]
Reserved	HB3 Vstep1 and Vstep2 conf [1]	HB3 Vstep1 and Vstep2 conf [0]	HB3 Istep3 conf [3]	HB3 Istep3 conf [2]	HB3 Istep3 conf [1]	HB3 Istep3 conf [0]

Table 124. HB3_DRIVER_CFG (0x19) MSB description (available in STDRIVE141 only)

Bit	Name	Description
14	RES	Reserved
13	VSTEP2_CONF3 [1]	Vstep1 and Vstep2 thresholds configuration of the HB3
12	VSTEP2_CONF3 [0]	These two bits set the Vstep1 and Vstep2 thresholds of the HB3 00 ⇒ Vstep1 = 1.1 V, Vstep2 = 2.67 V for the switch ON 00 ⇒ Vstep1 = 1.3 V, Vstep2 = 3.33 V for the switch OFF 01 ⇒ Vstep1 = 1.1 V, Vstep2 = 3.56 V for the switch ON 01 ⇒ Vstep1 = 1.3 V, Vstep2 = 4.44 V for the switch OFF 10 ⇒ Vstep1 = 2.2 V, Vstep2 = 4.45 V for the switch ON 10 ⇒ Vstep1 = 2.6 V, Vstep2 = 5.55 V for the switch OFF 11 ⇒ Vstep1 = 2.2 V, Vstep2 = 5.34 V for the switch ON 11 ⇒ Vstep1 = 2.6 V, Vstep2 = 6.66 V for the switch OFF

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Bit	Name	Description
11	ISTEP3_CONF3 [3]	Istep3 configuration of the HB3
10	ISTEP3_CONF3 [2]	0000 ⇒ 2 mA
9	ISTEP3_CONF3 [1]	0001 ⇒ 4 mA
8	ISTEP3_CONF3 [0]	0010 ⇒ 8 mA 0011 ⇒ 12 mA 0100 ⇒ 20 mA 0101 ⇒ 28 mA 0110 ⇒ 36 mA 0111 ⇒ 44 mA 1000 ⇒ 52 mA 1001 ⇒ 60 mA 1010 ⇒ 68 mA 1011 ⇒ 76 mA 1100 ⇒ 84 mA 1101 ⇒ 92 mA 1110 ⇒ 104 mA 1111 ⇒ 120 mA

Table 125. HB3_DRIVER_CFG (0x19) LSB (available in STDRIVE141 only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
ISTEP2_CONF3 [3]	ISTEP2_CONF3 [2]	ISTEP2_CONF3 [1]	ISTEP2_CONF3 [0]	ISTEP1_CONF3 [3]	ISTEP1_CONF3 [2]	ISTEP1_CONF3 [1]	ISTEP1_CONF3 [0]
HB3 Istep3 conf [3]	HB3 Istep3 conf [2]	HB3 Istep3 conf [1]	HB3 Istep3 conf [0]	HB3 Istep3 conf [3]	HB3 Istep3 conf [2]	HB3 Istep3 conf [1]	HB3 Istep3 conf [0]

Table 126. HB3_DRIVER_CFG (0x19) LSB description (available in STDRIVE141 only)

Bit	Name	Description
7	ISTEP2_CONF3 [3]	Istep2 configuration of the HB3 for the low to high transition
6	ISTEP2_CONF3 [2]	0000 ⇒ 1 mA
5	ISTEP2_CONF3 [1]	0001 ⇒ 2 mA
4	ISTEP2_CONF3 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA

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Bit	Name	Description
		0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 = 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
3	ISTEP1_CONF3 [3]	Istep1 configuration of the HB3 0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
2	ISTEP1_CONF3 [2]	
1	ISTEP1_CONF3 [1]	
0	ISTEP1_CONF3 [0]	

Table 127. HB3_DIAG_CFG (0x1A) MSB (available in STDRIVE141 only)

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	Bit 10	Bit 9	Bit 8
RES	RES	RES	RES	0 (RW)	0 (RW)	0 (RW)
Reserved	Reserved	Reserved	Reserved	VDS_CONF3 [3]	VDS_CONF3 [2]	VDS_CONF3 [1]

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Table 128. **HB3_DIAG_CFG (0x1A) MSB description (available in STDRIVE141 only)**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	VDS_CONF3 [3]	V_{ds} monitor threshold configuration of the HB3 0000 ⇒ 75 mV 0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V
9	VDS_CONF3 [2]	
8	VDS_CONF3 [1]	

Table 129. **HB3_DIAG_CFG (0x1A) LSB (available in STDRIVE141 only)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
VDS_CONF3 [0]	VDS_BLANK3 [3]	VDS_BLANK3 [2]	VDS_BLANK3 [1]	VDS_BLANK3 [0]	VDS_FILT3 [2]	VDS_FILT3 [2]	VDS_FILT3 [2]
VDS conf of the HB3 [0]	VDS blanking time conf [3]	VDS blanking time conf [2]	VDS blanking time conf [1]	VDS blanking time conf [0]	VDS filter time conf [2]	VDS filter time conf [1]	VDS filter time conf [0]

Table 130. **HB3_DIAG_CFG (0x1A) LSB description (available in STDRIVE141 only)**

Bit	Name	Description
7	VDS_CONF3 [0]	V_{ds} monitor threshold configuration of the HB3 0000 = 75 mV 0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV

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Bit	Name	Description
		0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V
6	VDS_BLANK3 [3]	V_{ds} blanking time configuration of the HB3
5	VDS_BLANK3 [2]	0000 ⇒ 0.625 µs
4	VDS_BLANK3 [1]	0001 ⇒ 1 µs
3	VDS_BLANK3 [0]	0010 ⇒ 1.25 µs 0011 ⇒ 1.5 µs 0100 ⇒ 2 µs 0101 ⇒ 3 µs 0110 ⇒ 4 µs 0111 ⇒ 5 µs 1000 ⇒ 6 µs 1001 ⇒ 7 µs 1010 ⇒ 8 µs 1x11 ⇒ 0.625 µs
2	VDS_FILT3 [2]	V_{ds} filtering time configuration of the HB3
1	VDS_FILT3 [1]	000 ⇒ 0.5 µs
0	VDS_FILT3 [0]	001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ 0.5 µs

Table 131. HB3_TURN_OFF_CFG (0x1B) MSB (available in STDRIVE141 only)

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	GENMODE3 [1]	GENMODE3 [0]
Reserved	Reserved	Reserved	Reserved	Reserved	GENMODE bit conf [1]	GENMODE bit conf [0]

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Table 132. **HB3_TURN_OFF_CFG (0x1B) MSB description (available in STDRIVE141 only)**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	RES	
9	GENMODE3 [1]	HB3 Gate driver actions when a VDH overvoltage is detected: 00 ⇒ Gate driver off 01 ⇒ HS off, LS on 10 ⇒ Flag only 11 ⇒ Gate driver off
8	GENMODE3 [0]	

Table 133. **HB3_TURN_OFF_CFG (0x1B) LSB (available in STDRIVE141 only)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	HB_FAULT3 [1]	HB_FAULT3 [0]	ISTEP2_OFF_ CONF3 [3]	ISTEP2_OFF_ CONF3 [2]	ISTEP2_OFF_ CONF3 [1]	ISTEP2_OFF_ CONF3 [0]
Reserved	Reserved	HB3 fault key [1]	HB3 fault key [0]	HB3 Istep2 conf [3]	HB3 Istep2 conf [2]	HB3 Istep2 conf [1]	HB3 Istep2 conf [0]

Table 134. **HB3_TURN_OFF_CFG (0x1B) LSB description (available in STDRIVE141 only)**

Bit	Name	Description
7	RES	Reserved
6	RES	
5	HB_FAULT3 [1]	HB3 fault key 00 ⇒ No key 00 ⇒ key 1 10 ⇒ key 2 (STDRIVE141 only) 11 ⇒ key 1 + key 2 (STDRIVE141 only)
4	HB_FAULT3 [0]	
3	ISTEP2_OFF_CONF3 [3]	Istep2 configuration of the HB3 in case of the switch OFF of the external MOSFET 0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA
2	ISTEP2_OFF_CONF3 [2]	
1	ISTEP2_OFF_CONF3 [1]	

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Bit	Name	Description
0	ISTEP2_OFF_CONF3 [0]	0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA

Table 135. HB4_MODE_CONFIG (0x1C) MSB (available in STDRIVE141 only)

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	DT4 [2]	DT4 [1]	DT4 [0]	STRONG_ON _WHEEL4	HB_IDIAG4 [1]
Reserved	Reserved	Dead time 4 [2]	Dead time 4 [1]	Dead time 4 [0]	Free-wheeling strong on HB4	HB4 diagnostic current

Table 136. HB4_MODE_CONFIG (0x1C) MSB description (available in STDRIVE141 only)

Bit	Name	Description
14	RES	Reserved
13	RES	
12	DT4 [2]	Dead time of the HB4 000 ⇒ 0.5 µs 001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs
11	DT4 [1]	
10	DT4 [0]	

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Bit	Name	Description
		111 ⇒ 16 µs
9	STRONG_ON_ WHEEL4	Free-wheeling strong ON of the HB4 0 ⇒ Strong on disabled, free-wheeling gate current set to 4 mA 1 ⇒ Strong on enabled, free-wheeling gate current set to 30 mA
8	HB_IDIAG4 [1]	HB4 diagnostic currents setting 00 ⇒ Pull-up and pull-down currents off 01 ⇒ Pull-up current off and pull-down current on 10 ⇒ Pull-up current on and pull-down current off 11 ⇒ Pull-up and pull-down currents off

Table 137. HB4_MODE_CONFIG (0x1C) LSB (available in STDRIVE141 only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
HB_IDIAG4 [1]	HB_PWM4 [2]	HB_PWM4 [1]	HB_PWM4 [0]	HB_MODE4 [1]	HB_MODE4 [0]	HB_WHEEL4 [1]	HB_WHEEL4 [0]
HB4 diagnostic current	HB4 PWM mapping [2]	HB4 PWM mapping [1]	HB4 PWM mapping [0]	HB4 mode [1]	HB4 mode [0]	HB4 free-wheeling [1]	HB4 free-wheeling [0]

Table 138. HB4_MODE_CONFIG (0x1C) LSB description (available in STDRIVE141 only)

Bit	Name	Description
7	HB_IDIAG4 [0]	HB4 diagnostic currents setting 00 ⇒ Pull-up and pull-down currents off 01 ⇒ Pull-up current off and pull-down current on 10 ⇒ Pull-up current on and pull-down current off 11 ⇒ Pull-up and pull-down currents off
6	HB_PWM4 [2]	PWM mapping on HB4 This 3-bit register is used to indicate which PWM signal is applied to the HS or LS of the half-bridge 4 000 ⇒ LS of HB mapped on PWM1 001 ⇒ LS of HB mapped on PWM2 011 ⇒ HS of HB mapped on PWM1 100 ⇒ HS of HB mapped on PWM2 010 = 101 = 110 = 111 ⇒ No mapping
5	HB_PWM4 [1]	
4	HB_PWM4 [0]	
3	HB_MODE4 [1]	HB4 functionality mode

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Bit	Name	Description
2	HB_MODE4 [0]	00 ⇒ LS and HS of the HB1 are kept off 01 ⇒ LS of the HB1 is ON (static, no PWM), HS of the HB1 is OFF 10 ⇒ HS of the half-bridge 1 is ON (static, no PWM), LS of the half-bridge is OFF 11 ⇒ LS or HS of the half-bridge is ON according to the HB_PWM1 register
1	HB_WHEEL4 [1]	HB4 free-wheeling mode 00 = 11 ⇒ No mapping 01 ⇒ Active free-wheeling on HS of the HB 10 ⇒ Active free-wheeling on LS of the HB
0	HB_WHEEL4 [0]	

Table 139. HB4_DRIVER_CFG (0x1D) MSB (available in STDRIVE141 only)

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	VSTEP2_CONF4 [1]	VSTEP2_CONF4 [0]	ISTEP3_CONF4 [3]	ISTEP3_CONF4 [2]	ISTEP3_CONF4 [1]	ISTEP3_CONF4 [0]
Reserved	HB4 Vstep1 and Vstep2 conf [1]	HB4 Vstep1 and Vstep2 conf [0]	HB4 Istep3 conf [3]	HB4 Istep3 conf [2]	HB4 Istep3 conf [1]	HB4 Istep3 conf [0]

Table 140. HB4_DRIVER_CFG (0x1D) MSB description (available in STDRIVE141 only)

Bit	Name	Description
14	RES	Reserved
13	VSTEP2_CONF4 [1]	Vstep1 and Vstep2 thresholds configuration of the HB4
12	VSTEP2_CONF4 [0]	These two bits set the Vstep1 and Vstep2 thresholds of the HB4 00 ⇒ Vstep1 = 1.1 V, Vstep2 = 2.67 V for the switch ON 00 ⇒ Vstep1 = 1.3 V, Vstep2 = 3.33 V for the switch OFF 01 ⇒ Vstep1 = 1.1 V, Vstep2 = 3.56 V for the switch ON 01 ⇒ Vstep1 = 1.3 V, Vstep2 = 4.44 V for the switch OFF 10 ⇒ Vstep1 = 2.2 V, Vstep2 = 4.45 V for the switch ON 10 ⇒ Vstep1 = 2.6 V, Vstep2 = 5.55 V for the switch OFF 11 ⇒ Vstep1 = 2.2 V, Vstep2 = 5.34 V for the switch ON 11 ⇒ Vstep1 = 2.6 V, Vstep2 = 6.66 V for the switch OFF
11	ISTEP3_CONF4 [3]	Istep3 configuration of the HB4 0000 ⇒ 2 mA 0001 ⇒ 4 mA 0010 ⇒ 8 mA
10	ISTEP3_CONF4 [2]	
9	ISTEP3_CONF4 [1]	
8	ISTEP3_CONF4 [0]	

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Bit	Name	Description
		0011 ⇒ 12 mA 0100 ⇒ 20 mA 0101 ⇒ 28 mA 0110 ⇒ 36 mA 0111 ⇒ 44 mA 1000 ⇒ 52 mA 1001 ⇒ 60 mA 1010 ⇒ 68 mA 1011 ⇒ 76 mA 1100 ⇒ 84 mA 1101 ⇒ 92 mA 1110 ⇒ 104 mA 1111 ⇒ 120 mA

Table 141. HB4_DRIVER_CFG (0x1D) LSB (available in STDRIVE141 only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
ISTEP2_CONF4 [3]	ISTEP2_CONF4 [2]	ISTEP2_CONF4 [1]	ISTEP2_CONF4 [0]	ISTEP1_CONF4 [3]	ISTEP1_CONF4 [2]	ISTEP1_CONF4 [1]	ISTEP1_CONF4 [0]
HB4 Istep3 conf [3]	HB4 Istep3 conf [2]	HB4 Istep3 conf [1]	HB4 Istep3 conf [0]	HB4 Istep3 conf [3]	HB4 Istep3 conf [2]	HB4 Istep3 conf [1]	HB4 Istep3 conf [0]

Table 142. HB4_DRIVER_CFG (0x1D) LSB description (available in STDRIVE141 only)

Bit	Name	Description
7	ISTEP2_CONF4 [3]	Istep2 configuration of the HB4 for the low to high transition 0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA
6	ISTEP2_CONF4 [2]	
5	ISTEP2_CONF4 [1]	
4	ISTEP2_CONF4 [0]	

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Bit	Name	Description
		1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA
3	ISTEP1_CONF4 [3]	Istep1 configuration of the HB4
2	ISTEP1_CONF4 [2]	0000 ⇒ 1 mA
1	ISTEP1_CONF4 [1]	0001 ⇒ 2 mA
0	ISTEP1_CONF4 [0]	0010 ⇒ 3 mA 0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA

Table 143. HB4_DIAG_CFG (0x1E) MSB (available in STDRIVE141 only)

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	VDS_CONF4 [3]	VDS_CONF4 [2]	VDS_CONF4 [1]
Reserved	Reserved	Reserved	Reserved	VDS conf of the HB4 [3]	VDS conf of the HB4 [2]	VDS conf of the HB4 [1]

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Table 144. **HB4_DIAG_CFG (0x1E) MSB description (available in STDRIVE141 only)**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	VDS_CONF4 [3]	V_{ds} monitor threshold configuration of the HB4 0000 ⇒ 75 mV 0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV 0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V
9	VDS_CONF4 [2]	
8	VDS_CONF4 [1]	

Table 145. **HB4_DIAG_CFG (0x1E) LSB (available in STDRIVE141 only)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
VDS_CONF4 [0]	VDS_BLANK4 [3]	VDS_BLANK4 [2]	VDS_BLANK4 [1]	VDS_BLANK4 [0]	VDS_FILT4 [2]	VDS_FILT4 [2]	VDS_FILT4 [2]
VDS conf of the HB4 [0]	VDS blanking time conf [3]	VDS blanking time conf [2]	VDS blanking time conf [1]	VDS blanking time conf [0]	VDS filter time conf [2]	VDS filter time conf [1]	VDS filter time conf [0]

Table 146. **HB4_DIAG_CFG (0x1E) LSB description (available in STDRIVE141 only)**

Bit	Name	Description
7	VDS_CONF4 [0]	V_{ds} monitor threshold configuration of the HB4 0000 ⇒ 75 mV 0001 ⇒ 150 mV 0010 ⇒ 200 mV 0011 ⇒ 250 mV 0100 ⇒ 300 mV 0101 ⇒ 400 mV

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Bit	Name	Description
		0110 ⇒ 500 mV 0111 ⇒ 600 mV 1xxx ⇒ 2 V
6	VDS_BLANK4 [3]	V_{ds} blanking time configuration of the HB4
5	VDS_BLANK4 [2]	0000 ⇒ 0.625 µs
4	VDS_BLANK4 [1]	0001 ⇒ 1 µs
3	VDS_BLANK4 [0]	0010 ⇒ 1.25 µs 0011 ⇒ 1.5 µs 0100 ⇒ 2 µs 0101 ⇒ 3 µs 0110 ⇒ 4 µs 0111 ⇒ 5 µs 1000 ⇒ 6 µs 1001 ⇒ 7 µs 1010 ⇒ 8 µs 1x11 ⇒ Not used
2	VDS_FILT4 [2]	V_{ds} filtering time configuration of the HB4
1	VDS_FILT4 [1]	000 ⇒ 0.5 µs
0	VDS_FILT4 [0]	001 ⇒ 1 µs 010 ⇒ 2 µs 011 ⇒ 3 µs 100 ⇒ 4 µs 101 ⇒ 5 µs 110 ⇒ 6 µs 111 ⇒ Not used

Table 147. HB4_TURN_OFF_CFG (0x1F) MSB (available in STDRIVE141 only)

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)
RES	RES	RES	RES	RES	GENMODE4 [1]	GENMODE4 [0]
Reserved	Reserved	Reserved	Reserved	Reserved	GENMODE bit conf [1]	GENMODE bit conf [0]

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Table 148. **HB4_TURN_OFF_CFG (0x1F) MSB description (available in STDRIVE141 only)**

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	RES	
9	GENMODE4 [1]	HB4 Gate driver actions when a VDH overvoltage is detected: 00 ⇒ Gate driver off 01 ⇒ HS off, LS on 10 ⇒ Flag only 11 ⇒ Gate driver off
8	GENMODE4 [0]	

Table 149. **HB4_TURN_OFF_CFG (0x1F) LSB (available in STDRIVE141 only)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	HB_FAULT4 [1]	HB_FAULT4 [0]	ISTEP2_OFF_ CONF4 [3]	ISTEP2_OFF_ CONF4 [2]	ISTEP2_OFF_ CONF4 [1]	ISTEP2_OFF_ CONF4 [0]
Reserved	Reserved	HB4 fault key [1]	HB4 fault key [0]	HB4 Istep2 conf [3]	HB4 Istep2 conf [2]	HB4 Istep2 conf [1]	HB4 Istep2 conf [0]

Table 150. **HB4_TURN_OFF_CFG (0x1F) LSB description (available in STDRIVE141 only)**

Bit	Name	Description
7	RES	Reserved
6	RES	
5	HB_FAULT4 [1]	HB4 fault key 00 ⇒ No key 00 ⇒ key 1 10 ⇒ key 2 (STDRIVE141 only) 11 ⇒ key 1 + key 2 (STDRIVE141 only)
4	HB_FAULT4 [0]	
3	ISTEP2_OFF_CONF4 [3]	Istep2 configuration of the HB4 in case of the switch OFF of the external MOSFET 0000 ⇒ 1 mA 0001 ⇒ 2 mA 0010 ⇒ 3 mA
2	ISTEP2_OFF_CONF4 [2]	
1	ISTEP2_OFF_CONF4 [1]	

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Bit	Name	Description
0	ISTEP2_OFF_CONF4 [0]	0011 ⇒ 4 mA 0100 ⇒ 6 mA 0101 ⇒ 8 mA 0110 ⇒ 10 mA 0111 ⇒ 12 mA 1000 ⇒ 16 mA 1001 ⇒ 20 mA 1010 ⇒ 24 mA 1011 ⇒ 28 mA 1100 ⇒ 32 mA 1101 ⇒ 36 mA 1110 ⇒ 40 mA 1111 ⇒ 44 mA

Table 151. OUT_ENABLE (0x30) MSB

Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RO)
RES	RES	RES	RES	RES	RES	RES
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Table 152. OUT_ENABLE (0x30) MSB description

Bit	Name	Description
14	RES	Reserved
13	RES	
12	RES	
11	RES	
10	RES	
9	RES	
8	RES	

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Table 153. **OUT_ENABLE (0x30) LSB**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0 (RO)	0 (RO)	0 (RO)	0 (RO)	0 (RW)	0 (RW)	0 (RW)	0 (RW)
RES	RES	RES	RES	OUT4	OUT3	OUT2	OUT1
Reserved	Reserved	Reserved	Reserved	Out enable HB4	Out enable HB3	Out enable HB2	Out enable HB1

Table 154. **OUT_ENABLE (0x30) LSB description**

Bit	Name	Description
7	RES	Reserved
6	RES	
5	RES	
4	RES	
3	OUT4	Gate driver enable bit to control HB4. This bit is reset if a watchdog error is detected (available in STDRIVE141 only)
2	OUT3	Gate driver enable bit to control HB3. This bit is reset if a watchdog error is detected (available in STDRIVE141 only)
1	OUT2	Gate driver enable bit to control HB2. This bit is reset if a watchdog error is detected
0	OUT1	Gate driver enable bit to control HB1. This bit is reset if a watchdog error is detected

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10 Application examples

The STDRIVE141 is a device that integrates the control of 4 external half-bridges in a completely independent and configurable way. This allows the device to be used in multiple application scenarios. The following examples show some of the possible application configurations using the STDRIVE141. Similar scenarios are still valid with the STDRIVE121 considering half of the outputs.

A classic configuration where 4 motors are controlled simultaneously is shown in Figure 35: 2 different H-bridges are controlled simultaneously from the STDRIVE141.

Figure 35. Driving 2 DC motors simultaneously (STDRIVE141)

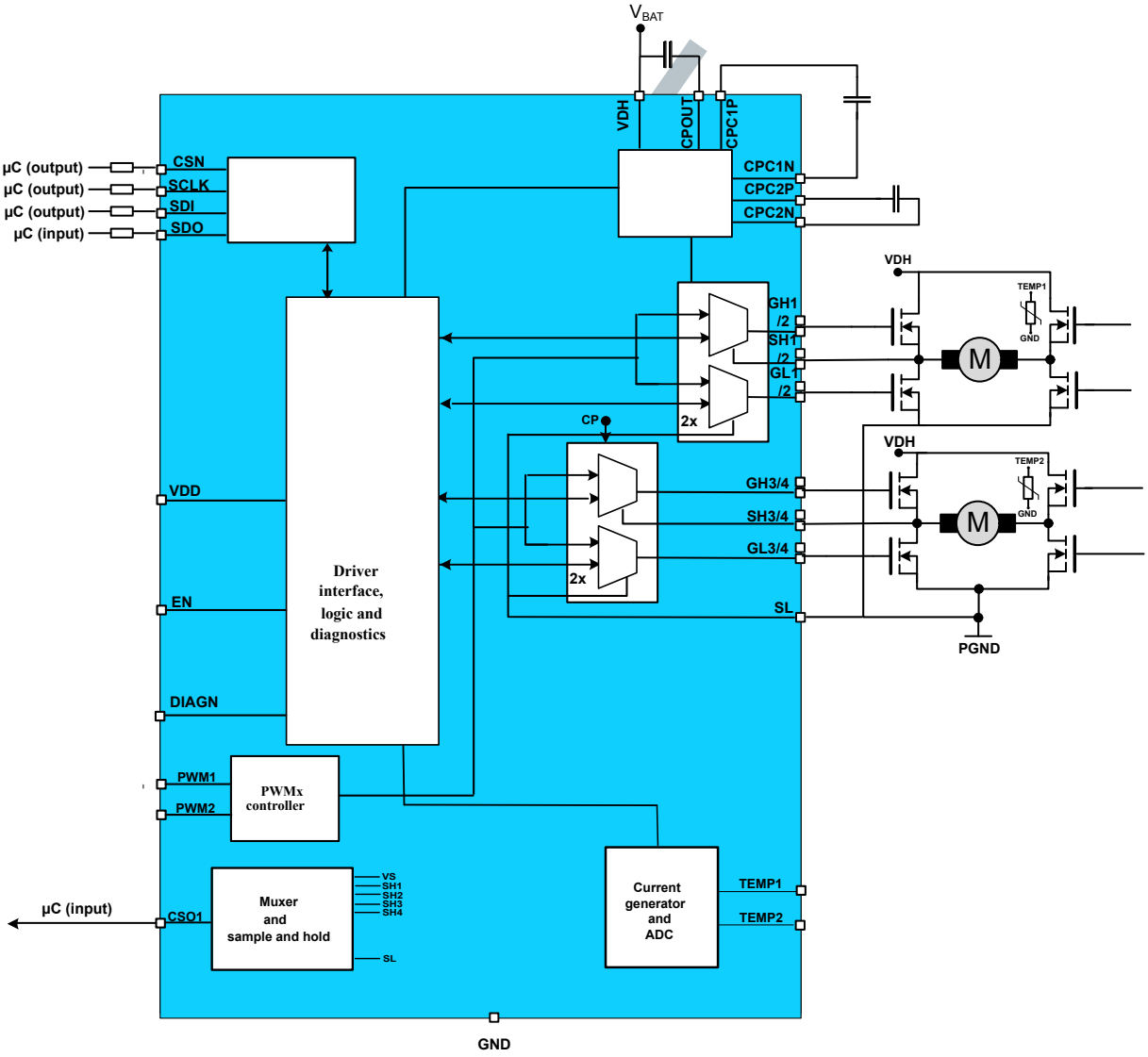


Figure 36 shows an application scenario in which 1 resistive load (heater, fan etc.) is driven by a high-side switch, and 1 motor is controlled by an H-bridge.

Figure 36. Driving 1 DC motor + 1 additional independent load simultaneously (STDRIVE141)

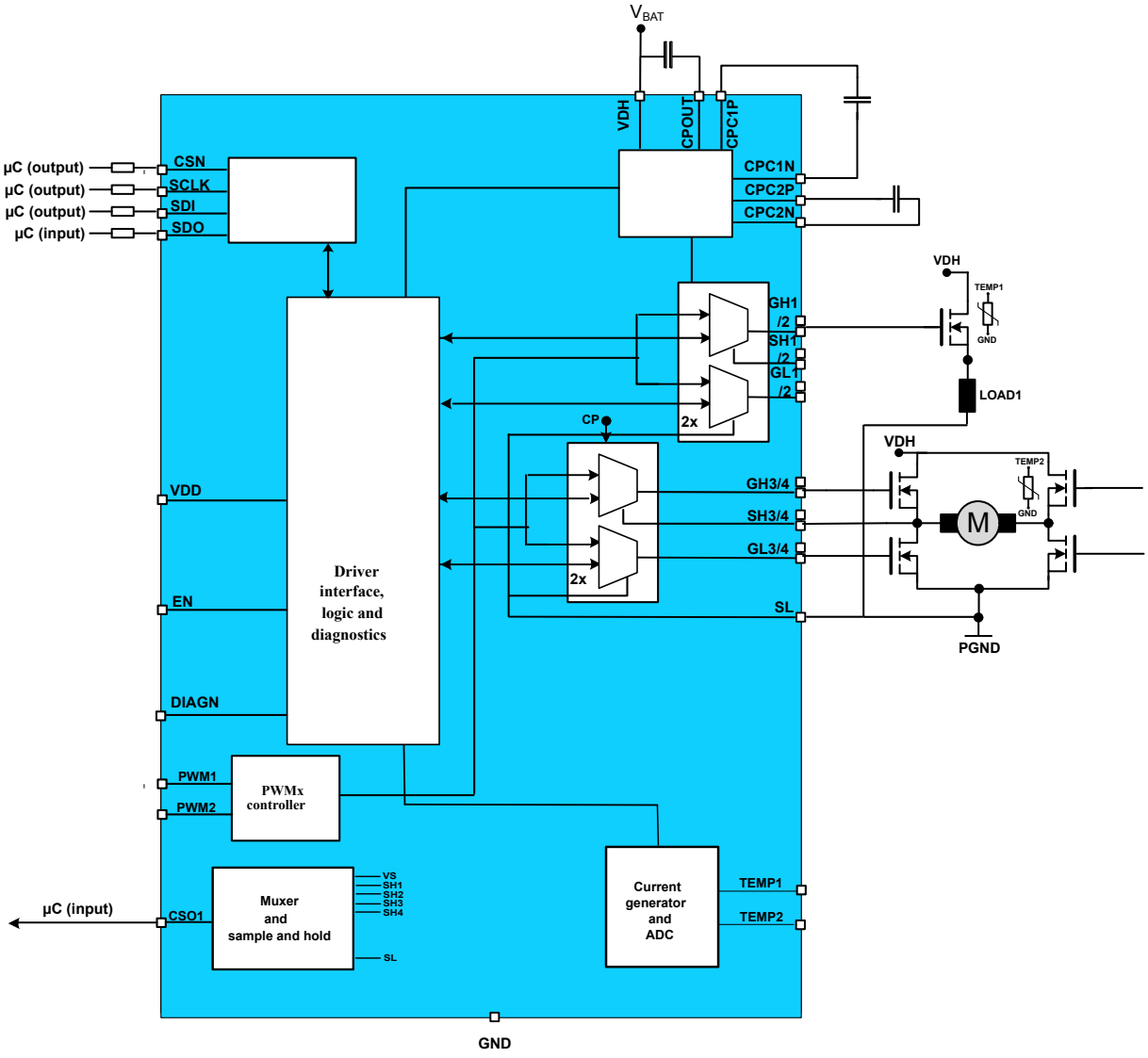
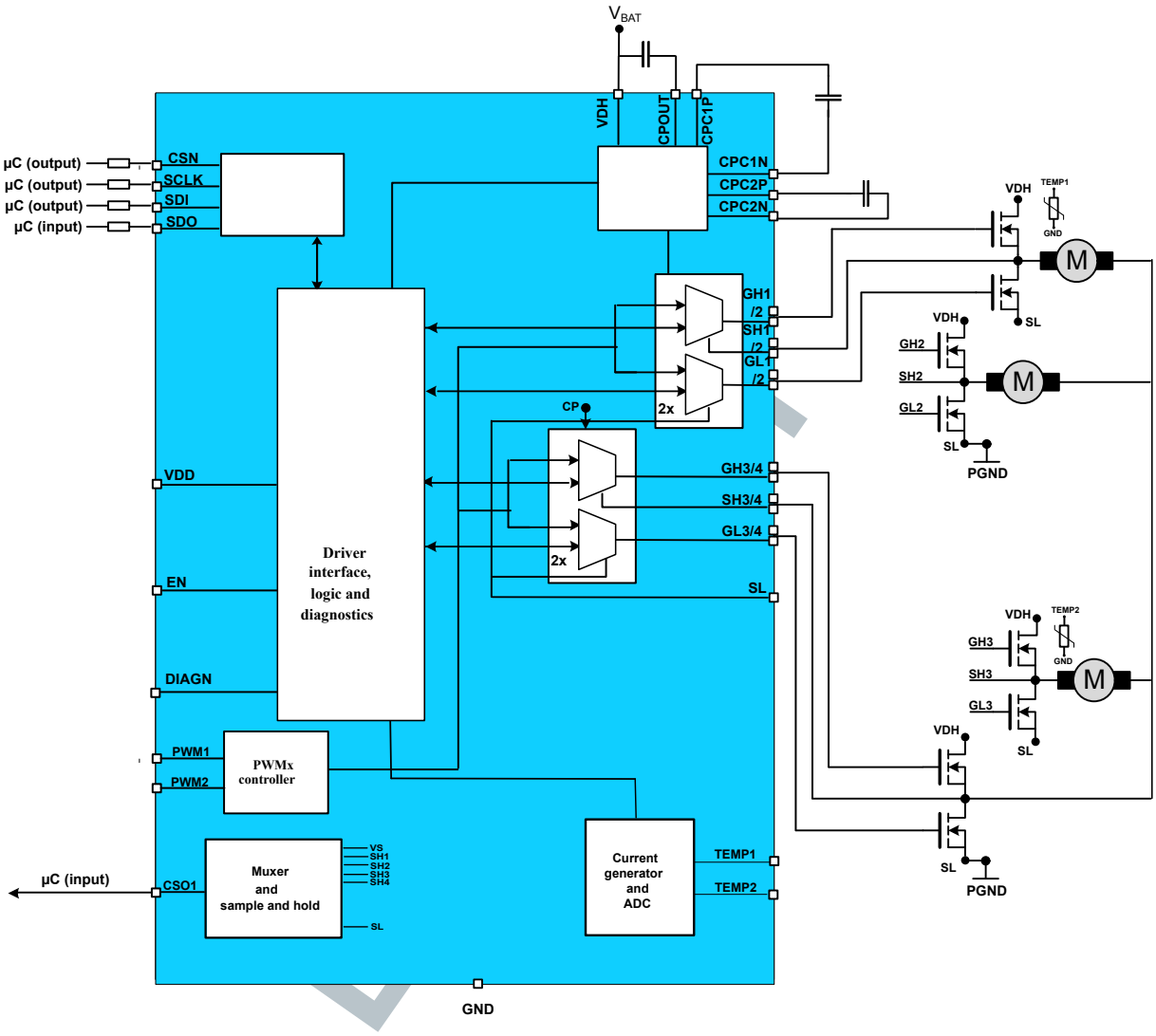


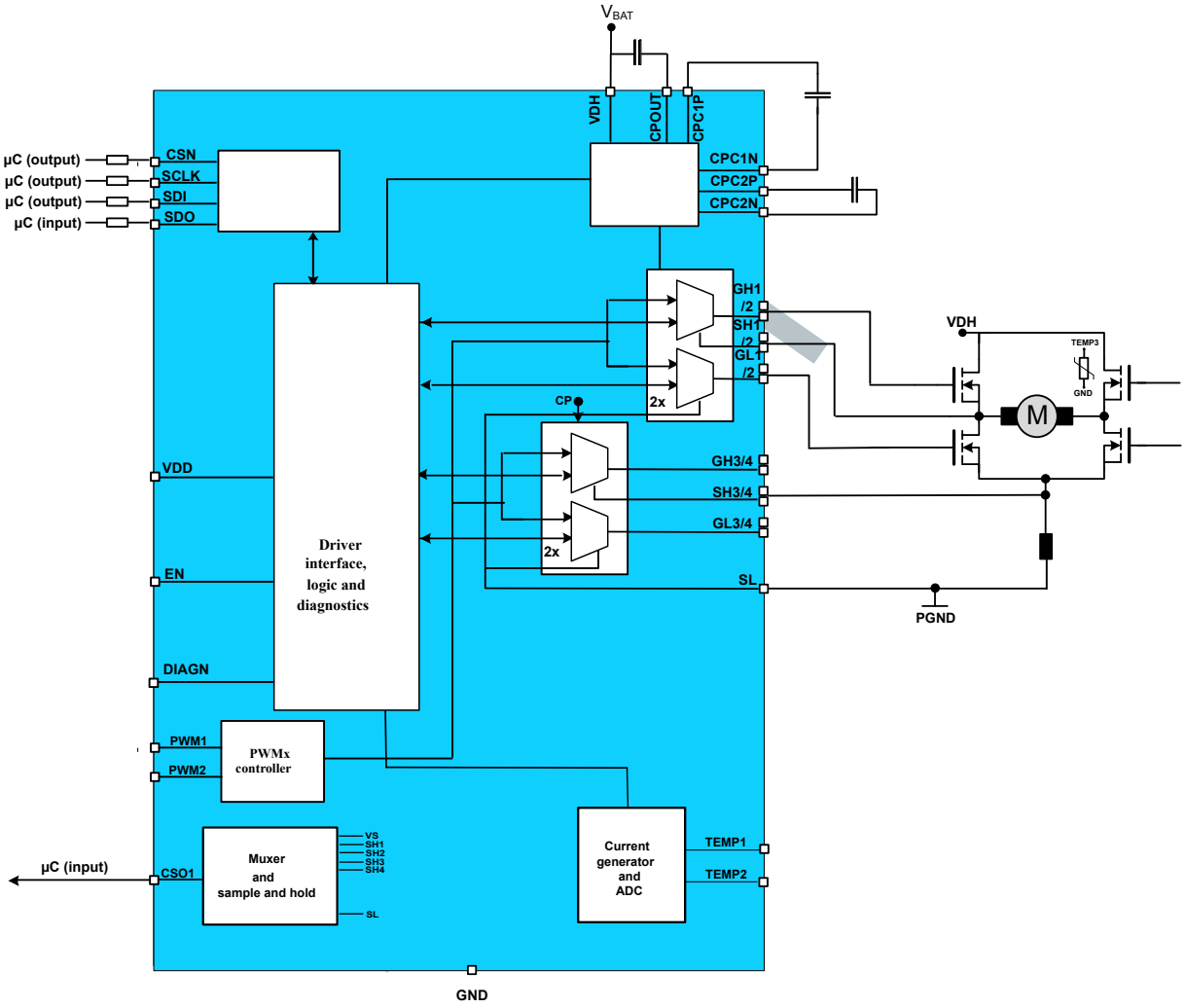
Figure 37 shows an application scenario where 3 motors are controlled by 3 half-bridges.

Figure 37. Driving 3 DC motors sequentially (STDRIVE141)



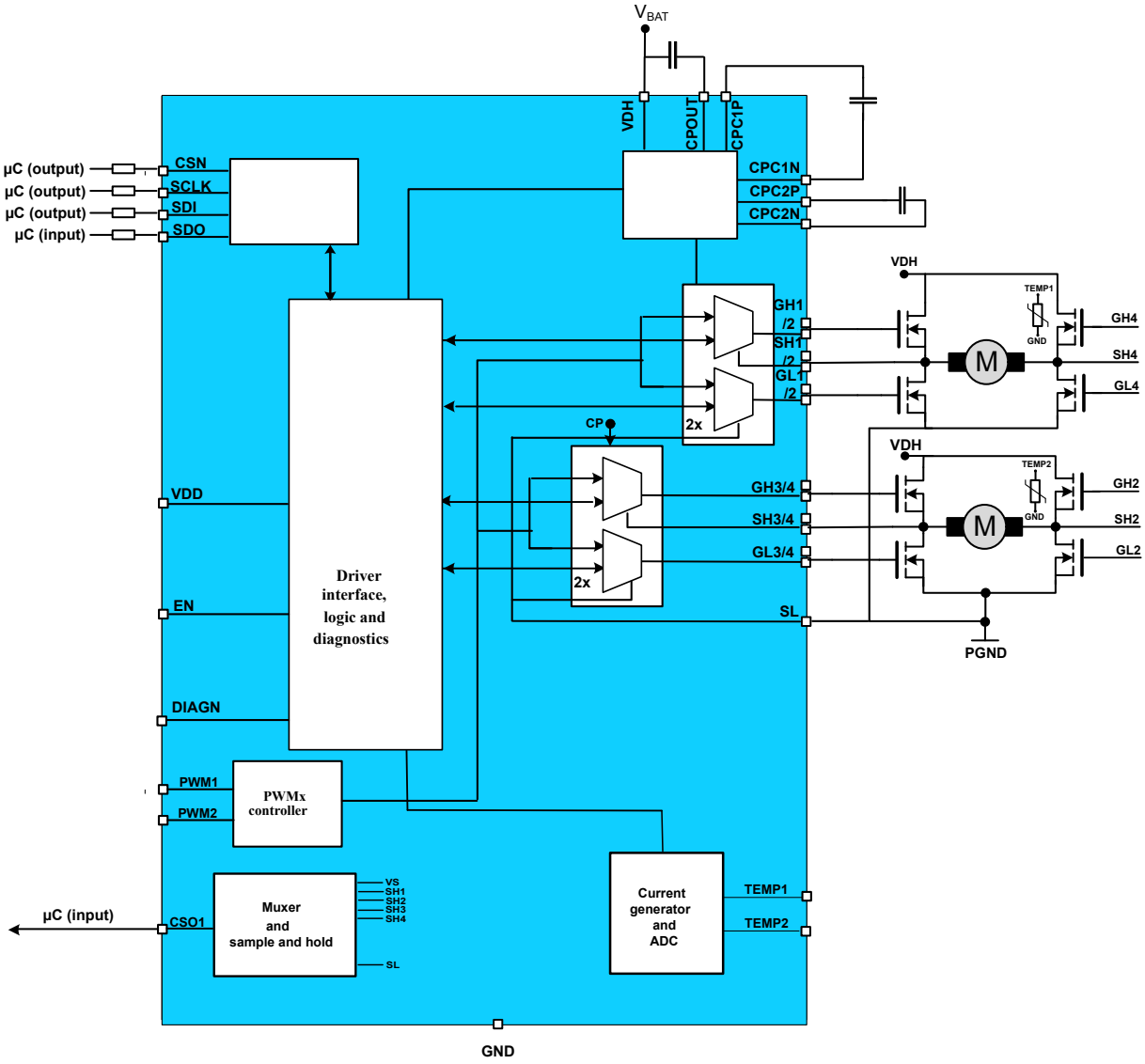
The STDRIVE141 also supports current measurement using a sensing resistor connected to the low-side sources of an H-bridge. One pin of the resistor, the one connected to the low-side sources, must be connected to the SHx pin of one of the other half-bridges, and the second pin of the resistor must be connected to the SL pin of the STDRIVE141 (see Figure 38).

Figure 38. Driving 1 DC motors: one current measurement with a shunt resistor (STDRIVE141)



The STDRIVE141 logic also allows any connection between the half-bridges of the device, GHx/SHx/GLx can be associated with any GHy/SHy/GLy (see Figure 39).

Figure 39. Driving 2 DC motors simultaneously with not sequentially gate drivers (STDRIVE141)



11 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

11.1 VFQFN32L (5x6x0.9 mm exp. pad down) package information

Figure 40. VFQFN32L (5x6x0.9 mm exp. pad down) package outline

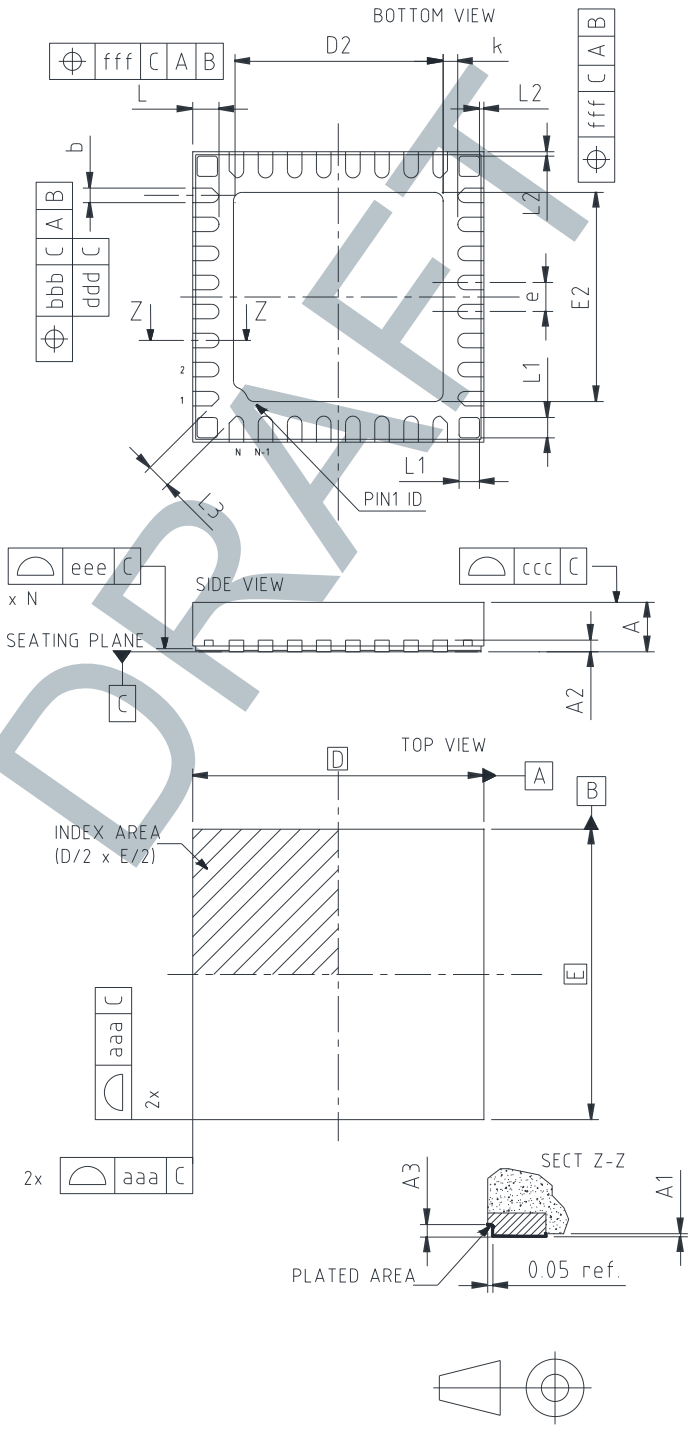


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Table 155. **VFQFN32L (5x5x0.9 mm exp. pad down) package mechanical data**

Symbol	Dimensions in mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2		0.2 REF	
A3	0.10	-	-
b	0.20	0.25	0.30
D	-	5.00	-
e	-	0.5	-
E	-	5.00	-
L	0.35	0.45	0.55
L1	-	0.35	-
L2	-	0.075	-
L3	-	0.42	-
k	0.20	-	-
N		32+4	
Tolerance of form and position			
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

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12 Ordering information

Table 156. **Order code**

Order code	Package	Package marking	Packing
STDRIVE141	VFQFPN 32L 5x5x0.9 mm, pitch 0.5 mm	DRIVE141	Tray
STDRIVE141TR	VFQFPN 32L 5x5x0.9 mm, pitch 0.5 mm	DRIVE141	Tape and reel
STDRIVE121	VFQFPN 32L 5x5x0.9 mm, pitch 0.5 mm	DRIVE121	Tray
STDRIVE121TR	VFQFPN 32L 5x5x0.9 mm, pitch 0.5 mm	DRIVE121	Tape and reel

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Revision history

Table 157. **Document revision history**

Date	Version	Changes
04-Jun-2026	1	Initial release.

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