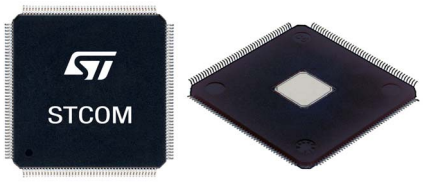
STCOM

Powerline communication and application system-on-chip

Datasheet - production data



TQFP176 (20 x 20 x 1 mm)

Features

- Integrated differential PLC analog front-end
  - PGA with automatic gain control and ADC
  - Current DAC with transmission predriver
  - Digital transmission level control
  - Zero crossing comparator
  - Up to 500 kHz PLC signal bandwidth
- Integrated dual line driver
  - 14 V p-p single ended, 28 V p-p differential output range
  - Very high linearity for EMC compliance
  - Externally configurable amplifier topology
  - 1 A rms max. current
  - Embedded overtemperature protection
  - Suitable for all PLC signals up to 500 kHz
- Fully reprogrammable real-time engine (RTE) modem for PLC standards up to 500 kHz
- Integrated application core: ARM® 32-bit Cortex™-M4F CPU
  - 96 MHz maximum frequency
  - 8-channel direct memory access controller
  - 8-region memory protection unit
  - Serial wire and JTAG interfaces
  - Cortex-M4 Embedded Trace Macrocell™
  - Up to 86 multiplexed GPIOs
  - 11 timers
  - 1 flexible CRC calculation unit
  - 5 USARTs (ISO 7816 compliant), 5 SPI, 3 I^2C
  - 12-bit general purpose ADC with 6 channels
- Cryptographic engine
  - AES 128/192/256 engine
  - True random number generator
- Memories
  - 640 kB or 1 MB of embedded Flash
  - 128 kB of embedded SRAM
  - 8 kB of embedded shared RAM
  - Flexible static memory controller
- Clock management
  - 24 MHz external crystal for system clock with internal QFS synthesizer
  - 32.768 kHz external crystal for RTC
- Power management
  - 3.3 V and 8 - 18 V external supply voltages
  - 1.2 V and 5 V integrated linear regulators
  - Normal and low power modes
- Real-time clock (RTC)
  - VBAT supply with battery health monitoring for RTC and backup registers
- -40 °C to +85 °C operating temperature range

Applications

- Smart metering, smart grid and “Internet of Things” applications
- Compliant with CENELEC, FCC, ARIB regulations

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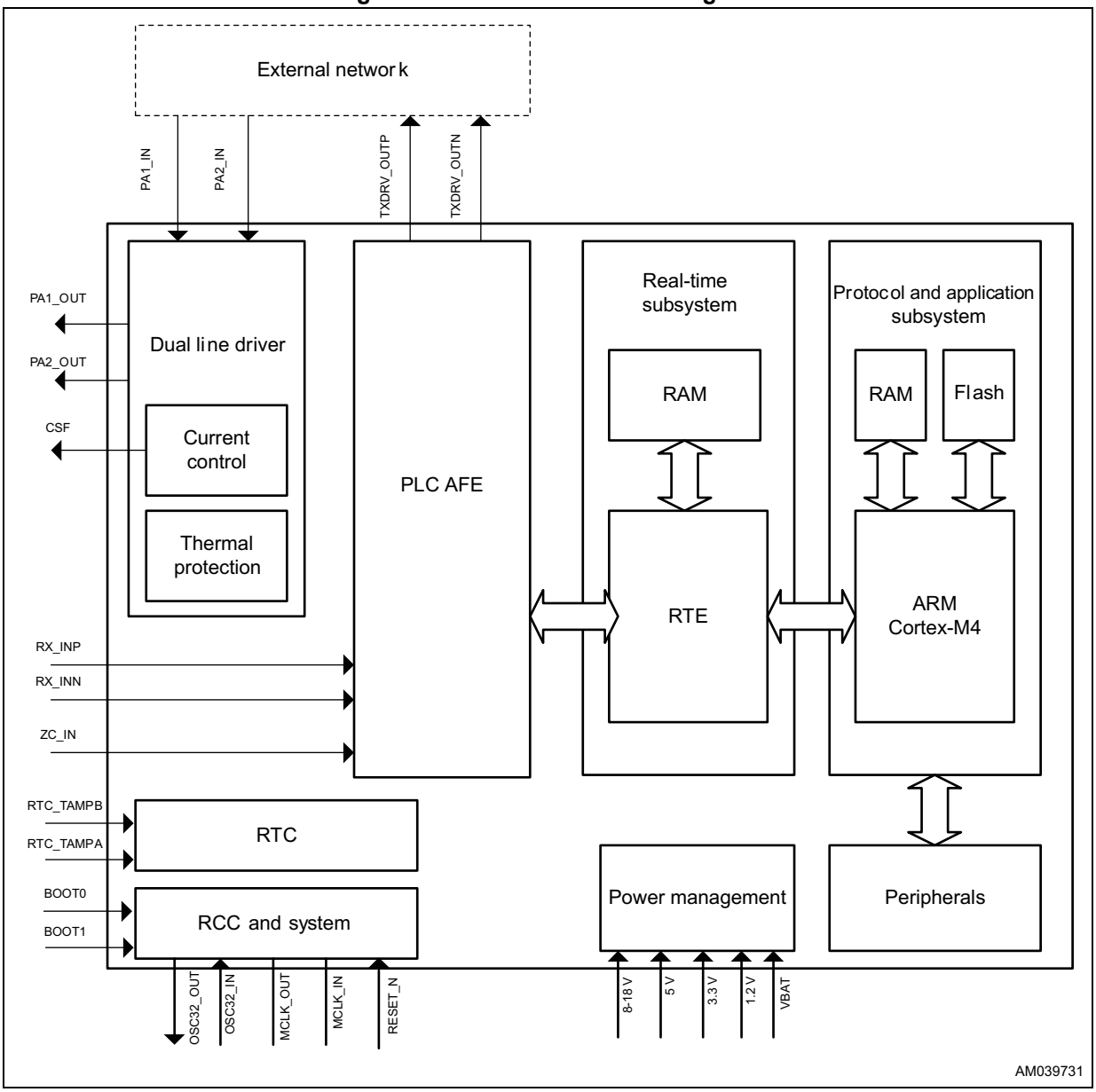
1 Description

The STCOM is a device that integrates a power line communication (PLC) modem and a high-performance application core.

The PLC modem architecture has been designed to target the EN50065, FCC, ARIB compliant PLC applications. Together with the application core, it enables the STCOM to support the ITU-T G.9001, ITU-T G.9903 (G3-PLC®), ITU-T G.9904 (PRIME), IEEE 1901.2, IEC 61334-5-1 (G1), CLC/TS 50568 (METERS AND MORE®) and other narrow band PLC protocol specifications.

The STCOM basic block diagram is shown in *Figure 1*.

Figure 1. STCOM basic block diagram



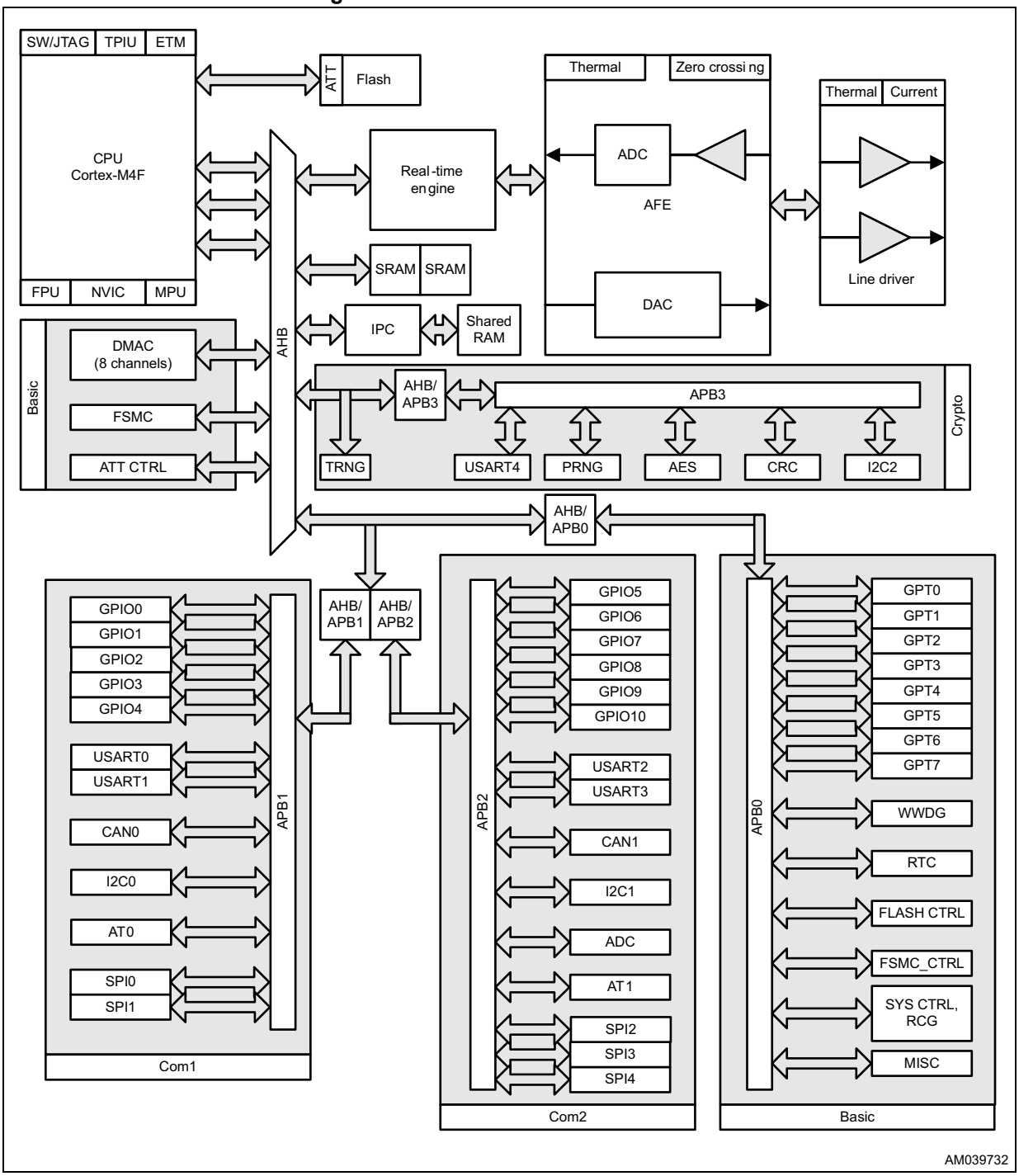
1.1 Device architecture

The architecture is composed of the following parts:

1. PLC front-end including digital front-end and analog front-end
2. PLC line driver
3. Real-time engine: the digital core running the lower layers of the PLC protocol stack and implementing modulation and demodulation
4. Protocol engine: the main digital core for running the upper layers of the PLC protocol stack
5. Wide range of peripherals logically divided into 4 blocks:
   - Basic peripherals
   - Com1 peripherals
   - Com2 peripherals
   - Crypto peripherals.

The STCOM detailed architecture is shown in *Figure 2*.

Figure 2. STCOM detailed architecture



1.2 Power line communication (PLC) sub-system

The STCOM device embeds a full narrow band power line communication (NB-PLC) sub-system, comprising the RTE, DFE, AFE and line driver.

The AFE and line driver have been designed for a differential power line interface; however, single-ended operation is possible for simpler hardware application development.

The DC to 500 kHz signal bandwidth is supported, targeting a number of possible NB-PLC solutions.

1.2.1 Real-time engine (RTE)

To match a performance required by emerging NB-PLC standards, the STCOM embeds a proprietary dedicated reprogrammable machine, the real-time engine. It is able to address specific functionalities exploited by OFDM and the ones adopted in the current and future NB- PLC standards in an efficient way.

1.2.2 Digital front-end (DFE)

Transmission and reception filter chains

The DFE includes programmable transmission/reception digital filter chains to fit the signal bandwidth in different PLC modulation cases. The ADC and DAC clock frequencies are controlled by the DFE to get the right sample rate fitting the filter chain configuration.

Automatic gain control (AGC)

The DFE implements the automatic gain control (AGC) block for the PGA, whose purpose is to adapt the signal to the ADC dynamic.

Current control (CC)

The DFE includes also the current control (CC) block for the line driver to limit the maximum output current.

1.2.3 Analog front-end (AFE)

Receiving chain

The STCOM AFE features a programmable gain amplifier (PGA) and a dedicated analog-to-digital converter (ADC) to achieve high RX sensitivity and a wide input range.

Transmission chain

The transmitted signal, generated in the digital domain, is fed into a dedicated digital-to-analog converter (DAC).

The DAC output is then fed into a predriver for buffering and applying an additional gain before the line driver.

Zero crossing comparator

The mains line zero crossing can be detected by providing a mains synchronous bipolar (AC) signal at the input of this comparator.

The zero crossing comparator provides positive and negative event information (rising/falling edge or high/low level).

1.2.4 Line driver

The STCOM is equipped with an integrated high-performance dual power line driver. It has very low distortion, allowing the device to comply with EMC requirements.

When supplied at maximum voltage, the line driver is capable to provide 28 V p-p in differential configuration or 14 V p-p in single-ended configuration.

The output current can reach 1 A rms in both differential and single-ended configurations, in order to drive very low power line impedance.

Any overtemperature event will force the line driver to shut down, thus preventing the STCOM to get damaged.

1.3 Application core sub-system

1.3.1 ARM® Cortex™-M4F core

The Cortex™-M4 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high end processing hardware including IEEE754-compliant single precision (32-bit) floating point computation, a range of a single cycle and SIMD multiplication and multiply with accumulate capabilities, saturating arithmetic and dedicated hardware division.

To facilitate the design of cost-sensitive devices, the Cortex™-M4 processor implements tightly coupled system components that reduce processor area while significantly improving interrupt handling and system debug capabilities. The Cortex™-M4 processor implements a version of the Thumb® instruction set based on Thumb-2® technology, ensuring high code density and reduced program memory requirements. The Cortex™-M4 instruction set provides the exceptional performance expected of a modern 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers.

The Cortex™-M4 processor provides multiple interfaces using AMBA™ technology to provide high-speed, low latency memory accesses. It supports unaligned data accesses and implements atomic bit manipulation that enables faster peripheral controls, system spinlocks and thread-safe Boolean data handling.

Table 1. Cortex™-M4F core configuration

Component	Presence	Comment
JTAG	Yes	Full-featured debug access port (DAP), SWJ-DP and AHB access port
ETM	Yes	Embedded Trace Macrocell present
ITM	Yes	Instrumentation Trace Macrocell
TPIU	Yes	Trace port unit interface present
FPB	Yes	Flash patch breakpoint
DWT	Yes	Data watchpoint and trace
DEBUG level	N/A	Full debug with data matching for watchpoint generation
IRQ	N/A	80 IRQ source
Priority level	N/A	Set to 5:32 levels
MPU	Yes	Memory protection unit present. 8 regions implemented
FPU	Yes	Floating point unit present (single precision)
BB	Yes	Bit banding region present
RESET_ALL_REGS	Yes	Reset all synchronous state
CLKGATE	Yes	Possibility to minimize dynamic power dissipation by clock gating
WIC	Yes	10 lines: NMI, WWDG, RTC, GPIOs, IPC, DMA, GPT0, SPI0 and USART0

1.3.2 Floating point unit (FPU)

The FPU fully supports single precision add, subtract, multiply, divide, multiply and accumulate, and square root operations. It also provides conversions between the fixed point and floating point data formats, and floating point constant instructions.

The FPU provides floating point operations that are compliant with the NSI/IEEE Std 754-2008 A, IEEE Standard for Binary Floating-point Arithmetic©, referred to as the IEEE 754 Standard.

The FPU contains 32 single precision extension registers, which can also be accessible as 16 double word registers for load, store, and move operations.

1.3.3 Nested vectored interrupt controller (NVIC)

The STCOM embeds a NVIC able to handle 80 maskable interrupts. The software priority level is configurable in the range of 0 - 31 for each interrupt. A higher level corresponds to a lower priority, so the level 0 is the highest interrupt priority. In case two or more interrupt lines share the same software priority level, the hardware priority level, which is described in *Table 2*, is used.

Table 2. Interrupt definition and position

Position	Priority	Acronym	Description
-	-3	Reset	Reset
-	-2	NMI	Wake-up interrupt - non maskable interrupt - system error
-	-1	HardFault	All class of fault
-	0	MemManage	MPU mismatch
-	1	BusFault	Prefetch fault, memory access fault
-	2	UsageFault	Undefined instruction or illegal state
-	3	SVCall	System service call via SWI instruction
-	4	DebugMonitor	Debug monitor
-	5	PendSV	Pendable request for system service
-	6	SysTick	System tick timer
0	7	WDG_WIC	Wake-up interrupt - window watchdog
1	8	RTC_WIC	Wake-up interrupt - RTC interrupts
2	9	-	Reserved
3	10	GPIO_WIC	Wake-up interrupt - GPIO interrupts
4	11	IPC_WIC	Wake-up interrupt - IPC interrupts
5	12	DMAC_WIC	Wake-up interrupt - DMAC interrupts
6	13	GPT0_WIC	Wake-up interrupt - GPT0 global interrupt
7	14	SPI0_WIC	Wake-up interrupt - SPI0 global interrupt
8	15	USART0_WIC	Wake-up interrupt - USART0 global interrupt
9	16	-	Reserved
10	17	TAMPER	Tamper pin interrupt
11	18	RTC	Real-time clock
12	19	FLASH_FATAL_ERROR	Flash interface
13	20	FLASH_ECC_RWW_ERROR	Flash interface
14	21	FLASH_ARY_DONE	Flash interface
15	22	IPC_MBOX	IPC mailbox
16	23	IPC_QUEUES	IPC queues
17	24	IPC_SHAREDRAM	IPC shared memory
18	25	DMA_Ch(1)	DMA global interrupt channel 1
19	26	DMA_Ch(2)	DMA global interrupt channel 2
20	27	DMA_Ch(3)	DMA global interrupt channel 3
21	28	DMA_Ch(4)	DMA global interrupt channel 4
22	29	DMA_Ch(5)	DMA global interrupt channel 5
23	30	DMA_Ch(6)	DMA global interrupt channel 6
24	31	DMA_Ch(7)	DMA global interrupt channel 7

Table 2. Interrupt definition and position (continued)

Position	Priority	Acronym	Description
25	32	DMA_Ch(8)	DMA global interrupt channel 8
26	33	ADC	ADC global interrupt
27	34	-	Reserved
28	35	-	Reserved
29	36	FSMC_FILL_FIFO	FSMC interface
30	37	SPI1	SPI1 global interrupt
31	38	SPI2	SPI2 global interrupt
32	39	SPI3	SPI3 global interrupt
33	40	SPI4	SPI4 global interrupt
34	41	I2C0_EVENT	I2C0 global event interrupt
35	42	I2C0_ERROR	I2C0 global error interrupt
36	43	I2C1_EVENT	I2C1 global event interrupt
37	44	I2C1_ERROR	I2C1 global error interrupt
38	45	I2C2_EVENT	I2C2 global event interrupt
39	46	I2C2_ERROR	I2C2 global error interrupt
40	47	AT0_BRK	Advanced timer 0 - BRK
41	48	AT0_UP	Advanced timer 0 - update
42	49	AT0_TRG_COM	Advanced timer 0 - trigger and commutation (COM)
43	50	AT0_CC	Advanced timer 0 - 4 CAPCOM
44	51	AT1_BRK	Advanced timer 1 - BRK
45	52	AT1_UP	Advanced timer 1 - update
46	53	AT1_TRG_COM	Advanced timer 1 - trigger and commutation (COM)
47	54	AT1_CC	Advanced timer 1 - 4 CAPCOM
48	55	GPT1	GPT1 - global interrupt
49	56	GPT2	GPT2 - global interrupt
50	57	GPT3	GPT3 - global interrupt
51	58	USART1	USART1 global interrupt
52	59	USART2	USART2 global interrupt
53	60	USART3	USART3 global interrupt
54	61	USART4	USART4global interrupt
55	62	CAN0	CAN0 global interrupt
56	63	CAN1	CAN1 global interrupt
57	64	AES	AES global interrupt
58	65	GPIO00	GPIO00 global interrupt
59	66	GPIO01	GPIO01 global interrupt

Table 2. Interrupt definition and position (continued)

Position	Priority	Acronym	Description
60	67	GPIO02	GPIO02 global interrupt
61	68	GPIO03	GPIO03 global interrupt
62	69	GPIO04	GPIO04 global interrupt
63	70	GPIO05	GPIO05 global interrupt
64	71	GPIO06	GPIO06 global interrupt
65	72	GPIO07	GPIO07 global interrupt
66	73	GPIO08	GPIO08 global interrupt
67	74	GPIO09	GPIO09 global interrupt
68	75	GPIO10	GPIO10 global interrupt
69	76	GPT4	GPT4 - global interrupt
70	77	GPT5	GPT5 - global interrupt
71	78	GPT6	GPT6 - global interrupt
72	79	GPT7	GPT7 - global interrupt
73	80	-	Reserved
74	81	-	Reserved
75	82	-	Reserved
76	83	-	Reserved
77	84	-	Reserved
78	85	-	Reserved
79	86	-	Reserved

1.3.4 DMA controller (DMA)

The STCOM embeds 1 general purpose dual port DMA controller with 8 channels. It is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. It features dedicated FIFOs for APB/AHB peripherals, a supports burst transfer and is designed to provide the maximum peripheral bandwidth (AHB/APB).

The DMA controller supports circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. It also has a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each channel is connected to dedicated hardware DMA requests, with support for a software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

Table 3. DMA channels muxing scheme

Peripheral	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8[1]
ADC	ADC	-	-	-	-	-	-	-
SPI0	-	SPI0_TX	SPI0_RX	-	-	-	-	-
SPI1	-	-	-	SPI1_TX	SPI1_RX	-	-	-
SPI2	-	SPI2_TX	SPI2_RX	-	-	-	-	-
SPI3	-	-	-	SPI3_TX	SPI3_RX	-	-	-
SPI4	-	-	-	-	-	SPI4_TX	SPI4_RX	-
USART0	-	USART0_TX	USART0_RX	-	-	-	-	-
USART1	-	-	-	USART1_TX	USART1_RX	-	-	-
USART2	-	-	-	-	-	USART2_TX	USART2_RX	
USART3	-	USART3_TX	USART3_RX	-	-	-	-	-
USART4	-	-	-	-	-	USART4_TX	USART4_RX	
I2C0	-	-	-	I2C0_TX	I2C0_RX	-	-	-
I2C1	-	I2C1_TX	I2C1_RX	-	-	-	-	-
I2C2	-	-	-	-	-	I2C2_TX	I2C2_RX	
AT0	-	AT0_CH1	AT0_CH2	AT0_CH4	-	-	-	-
AT0_TRIG	-	-	-	-	-	-	-	-
AT0_COM	AT0_UP	AT0_CH3	-	-	-	-	-	-
AT1	AT1_CH3	-	-	-	-	-	-	-
AT1_TRIG	-	-	-	-	-	-	-	-
AT1_COM	AT1_UP	-	-	AT1_CH1	-	AT1_CH2	-	-
AT1_CH4	-	-	-	-	-	-	-	-
GPT0	-	-	GPT0_UP	-	-	-	-	-
GPT1	-	-	-	GPT1_UP	-	-	-	-
GPT2	-	-	-	-	-	GPT2_UP	-	-
GPT3	-	-	-	-	-	-	GPT3_UP	-
GPT4	GPT4_UP	-	-	-	-	-	-	-
GPT5	-	GPT5_UP	-	-	-	-	-	-
GPT6	-	-	-	-	GPT6_UP	-	-	-
GPT7	-	-	-	GPT7_UP	-	-	-	-

1. Channel 8 is reserved.

1.3.5 Memory protection unit (MPU)

The MPU divides the memory map into up to 8 regions, and defines the location, size, access permissions, and memory attributes of each region. It supports:

- Independent attribute settings for each region
- Overlapping regions
- Export of memory attributes to the system.
- Background region

When memory regions overlap, memory access is affected by the attributes of the region with the highest number.

The background region has the same memory access attributes as the default memory map, but is accessible from privileged software only.

The MPU is useful to isolate and protect different parts of the firmware by giving different levels of access privileges. If a part of the firmware tries to access a memory location that is prohibited by the MPU, the processor generates a fault. This causes a fault exception that could be detected by the privileged firmware, which can take the appropriate action.

The MPU is optional and can be bypassed for applications that do not need it.

1.3.6 Debug and trace

Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Embedded Trace Macrocell™ (ETM)

The ARM Embedded Trace Macrocell provides greater visibility of the instruction and data flow inside the Cortex™-M4 core by streaming compressed data at a very high rate from the STCOM device through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is then connected to a host in order to record and then format the information for displaying and analysis.

1.3.7 General purpose input/outputs (GPIOs)

The STCOM device has 11 GPIOs ports named from GPIO00 to GPIO10. Each port is able to manage 8 pins, except the GPIO08 port that manages 6 pins. Each GPIO pin can be individually configured by software as output (push-pull or open drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate functions (with or without pull-up or pull-down). Each GPIO pin can also generate interrupt depending on a level (low and high), or a transactional value of the pin (rising or falling edge).

External interrupt

Each GPIOs port can generate interrupts. For each port one interrupt line is dedicated. The pins of one port share the same interrupt line.

1.3.8 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (Cortex™-M4, DMA, and real-time engine) and the slaves (Flash memory, RAM, AHB and APB peripherals, and real-time engine) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

1.3.9 Timers and watchdog

The STCOM embeds 8 general purpose timers, two advanced timers and one window watchdog. The Cortex™-M4 is also equipped with a SysTick timer.

General purpose timer (GPT)

The STCOM device includes 8 full-featured general purpose timers based on a 16-bit autoreload up/down counter and a 16-bit programmable prescaler.

Advanced timers (AT)

The STCOM includes 2 advanced-control timers based on a 16-bit autoreload up/down counter driven by a 16-bit programmable prescaler. They all feature 4 independent channels for input capture, output compare, PWM generation or one pulse mode output.

It may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM, complementary PWM with deadtime insertion).

Window watchdog (WWDG)

The window watchdog is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence. The watchdog circuit generates a device reset on expiry of a programmed time period, unless the program refreshes the contents of the down counter register. A device reset is also generated if the down counter value is refreshed before the down counter has reached the proper window register value. This implies that the counter must be refreshed in a limited window.

The window watchdog is based on a 7-bit free-running down counter with two conditional resets: the down counter is reloaded outside the window or the down counter value becomes less than 0x40.

The window watchdog supports early wake-up interrupt trigged when the down counter is equal to 0x40.

SysTick timer

The Cortex™-M4 has a 24-bit system timer, SysTick, which counts down from the programmable reload value to zero. It supports the autoreload and can generate a maskable system interrupt when the counter reaches zero.

1.3.10 CRC (cyclic redundancy check) calculation unit

The cyclic redundancy check (CRC) is a widely used method for detecting errors. The CRC calculation unit is used to get a CRC code in a flexible way using a configurable polynomial. Output data size can be selected between 8, 16, 24 or 32 bits.

Input data size can be configured between 1, 8, 16, 24 or 32 bits with selectable bit and byte endianness.

The CRC unit allows the specification of the initial value (all zero, all one, or a generic value) and the possibility to select an automatic XOR with all one when reading the data output.

1.3.11 Communication interfaces

Inter-integrated circuit interface (I^2C)

The STCOM embeds 3 I^2C bus interfaces that can operate in multimaster and slave modes. They can support the Standard and Fast modes. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

The I^2C peripherals can be served by DMA and support SMBus 2.0/PMBus™ operations.

Universal synchronous/asynchronous receiver transmitters (USART)

The STCOM embeds 5 universal synchronous/asynchronous receiver transmitters.

These five interfaces provide asynchronous communication, IrDA® SIR ENDEC support, a multiprocessor communication mode, single-wire half-duplex communication mode and have an LIN Master/Slave capability.

The peripherals also provide hardware management of the CTS and RTS signals, a Smartcard mode (ISO 7816 compliant) and a SPI-like communication capability. All interfaces can be served by the DMA controller.

Serial peripheral interface (SPI)

The STCOM embeds 5 SPIs in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card™/MMC™ modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in a TI™ mode for communications in master mode and slave mode.

Controller area network (CAN)

The STCOM embeds 2 CAN modules able to perform communication according to the CAN protocol version 2.0 part A and B. The bitrate can be programmed to values up to 1 MBit/s. For communication on a CAN network, individual message objects are configured. Each message object has its own identifier mask. The message objects and identifier masks are stored in the 256 byte size message RAM with a programmable FIFO mode. All functions concerning the handling of messages are implemented in the message handler. Those functions are the acceptance filtering, the transfer of messages between the CAN core and the message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

General purpose analog-to-digital converter (ADC)

One 12-bit SAR ADC working at a maximum conversion rate of 2 Msps is embedded in the STCOM. The ADC has 6 external available input channels performing conversion in a single, continuous or scan mode. The core accesses to the peripheral through a 4x12-bit FIFO interface.

The ADC can be served by the DMA controller. Additional 2 channels are internally used to monitor the VBAT and the low power temperature sensor.

1.4 Cryptographic engine (CRYP)

The STCOM embeds an advanced hardware AES peripheral which implements an advanced standard cryptographic algorithm according to the NIST FIPS 197. The block processes 128-bit data blocks using a key with the following possible sizes: 128, 192, 256 bits. The peripheral also supports the following modes: “Electronic Code Book” (ECB), “Cipher Block Chaining” (CBC), “Counter “mode (CTR), “Galois/Counter Mode” (GCM), GMAC and CCM modes.

The peripheral is able to encrypt and decrypt data. Interrupt can be generated when one operation is finished.

1.4.1 True random number generator (TRNG)

The STCOM embeds a TRNG processor based on a continuous analog noise that provides a random 16-bit value. To avoid pseudo random sequences, two consecutive accesses have to be performed when the ready bit in the status register is set to 1.

1.4.2 Pseudo random number generator (PRNG)

The STCOM embeds a PRNG processor that provides a pseudo random 32-bit value. Initial seed can be configured by software.

1.5 Interprocessor communication (IPC)

The Cortex™-M4 core and the real-time engine communicate by means of an additional 8 kByte shared static RAM. This memory can be accessed by the two cores through an interprocessor communication block that guarantees coherent and consistent read and modify operations, to provide several functionalities to the system, among the others:

- Configuration of real-time engine modes and functionalities during the normal working operations
- Data and information exchange between the Cortex™-M4 and real-time engine in both directions.
- The Cortex™-M4 wake up from a low power mode triggered by the real-time engine.

The real-time engine wakes up from a low power mode triggered by the Cortex™-M4.

1.6 Memories

1.6.1 Embedded Flash memory

The embedded Flash has the following features:

- 640 kB or 1 MB of size
- 128-bit wide data read
- 64-bit data write through a double 32-bit bus write
- Sector erase with possibility to suspend erase procedure in case of read access to other flash sectors
- Multiple sector erase.

Table 4. Embedded Flash sectors

Block	Name	Number	Base address	Size	Note
Main memory	B0F0	0	0x00000000	16 kB	-
-	B0F1	1	0x00004000	16 kB	-
-	B0F2	2	0x00008000	32 kB	-
-	B0F3	3	0x00010000	32 kB	-
-	B0F4	4	0x00018000	16 kB	-
-	B0F5	5	0x0001C000	16 kB	-
-	B0F6	6	0x00020000	64 kB	-
-	B0F7	7	0x00030000	64 kB	-
-	B0F8	8	0x00040000	128 kB	-
-	B0F9	9	0x00060000	128 kB	-
-	B0FA	10	0x00080000	128 kB	Not available in STCOM05
-	B0FB	11	0x000A0000	128 kB	Not available in STCOM05
-	B0FC	12	0x000C0000	128 kB	Not available in STCOM05
-	B0FD	13	0x000E0000	128 kB	-
Shadow sector	B0SH	14	0x00100000	16 kB	-

Shadow sector is accessible only in some security levels (see *Section 1.12: Boot modes on page 29*).

1.6.2 One-time programmable (OTP) section

The STCOM embeds a one-time programmable (OTP) section in the shadow sector of the embedded Flash memory. During the manufacturing process, the EUI48 is stored in this section. The user can also write its private key used during the boot process to verify and authenticate the firmware image. This OTP section can be configured to avoid reads by firmware in order to protect user confidential information (see *Section 1.12*).

1.6.3 Embedded SRAM

The STCOM device has 128 kB of a static RAM. The Cortex™-M4 can perform byte, half word (16 bits) or full word (32 bits) access to the SRAM at maximum speed, with zero wait states for both read and write operations. The SRAM start address is 0x20000000, the end address is 0x20001FFFF.

The SRAM is split into two blocks of 64 kB with a capability for concurrent access by AHB master sub-systems.

The Cortex™-M4 can also execute a code from the RAM at a zero wait state.

1.6.4 Flexible static memory controller (FSMC)

The STCOM embeds a FSMC peripheral able to interface external memory devices. The types of memory supported are:

- Asynchronous parallel NOR Flash with up to 21-bit address bus (no synchronous parallel NOR supported)
- Asynchronous SRAM memories

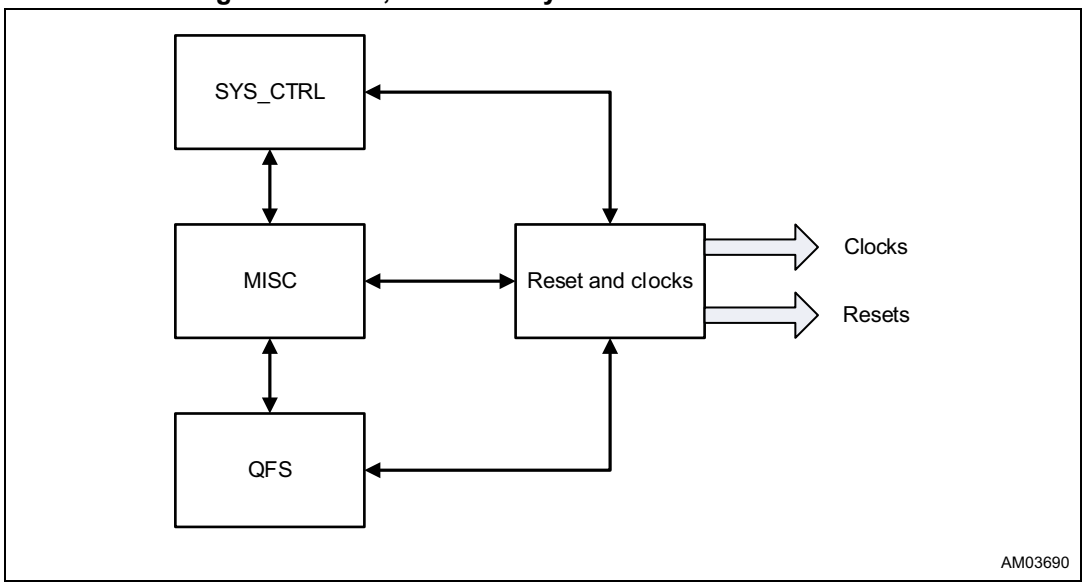
The data bus can be selected between 16 bits or 8 bits (reducing the total amount of accessible memory), for little or big endian operation.

The FSMC peripheral can connect up to 2 memories with 2 independent chip select lines (Ebar). The maximum size of each memory is 4 MB. Having 2 chip select lines, the maximum external memory size is 8 MB.

1.7 Reset, control, clock generation (RCC) and system controller (SYS_CTRL)

All the clock and reset configuration registers are located in the MISC and SYSCTRL blocks. *Figure 3* shows the interaction between these blocks.

Figure 3. Reset, clock and system controller interaction



The system reset is generated by the RESETn pin (active low). Through the system controller is also possible to assert a system software reset. The software reset to single peripherals can be forced through MISC registers.

Clock management

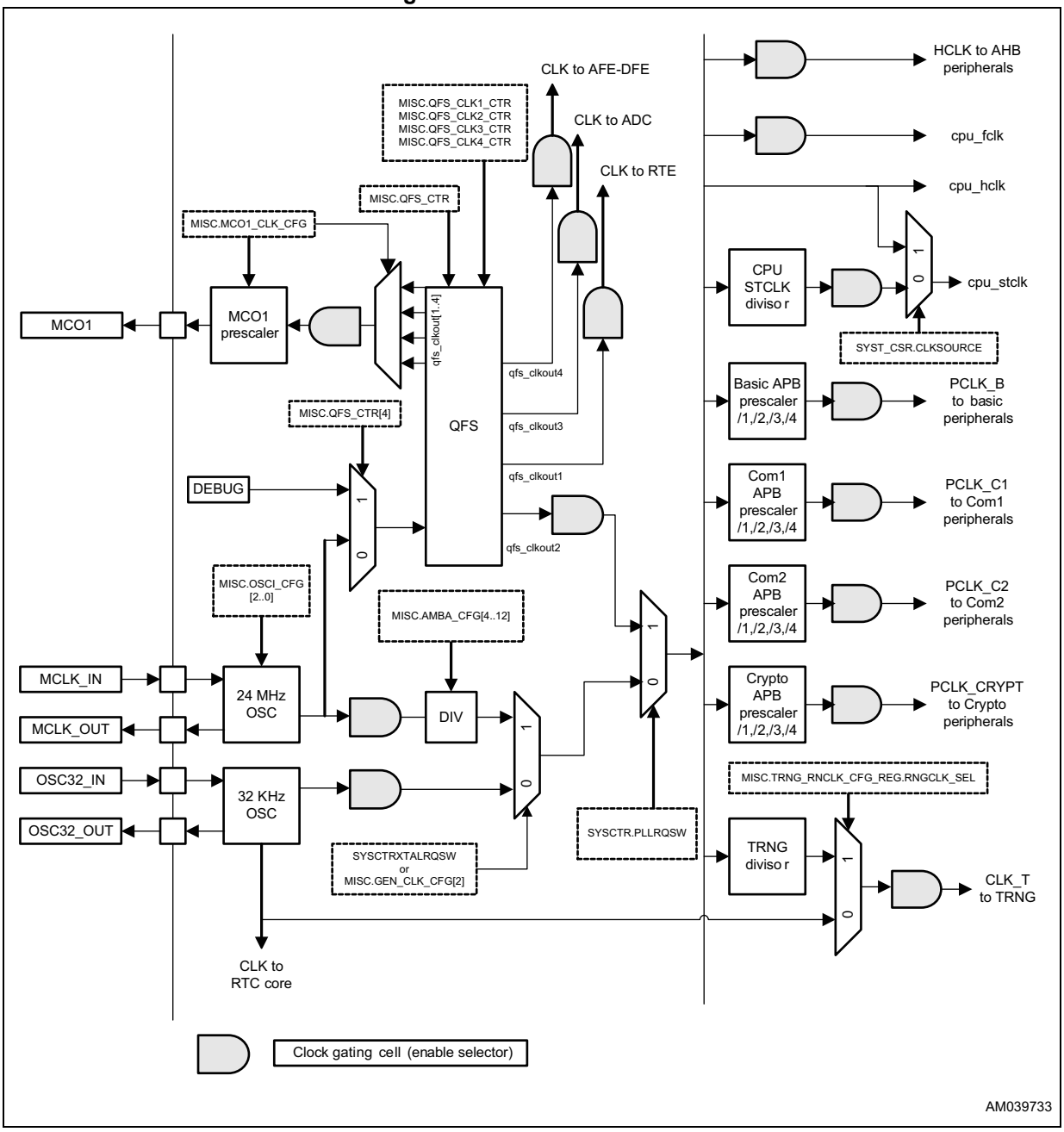
Two external clock sources are required for the STCOM:

1. 24 MHz frequency
2. 32.768 kHz frequency

Internal clocks are generated by a quadruple frequency synthesizer (QFS) that is fed by the 24 MHz source. Digital blocks can also use the external sources as clock reference.

The clock strategy is depicted in *Figure 4*.

Figure 4. STCOM clock tree



At a startup the 24 MHz oscillator clock is selected. This source must be always present to allow the STCOM starting correctly. 24 MHz can be provided by a quartz crystal or by any other source. In this latter case, the clock must be provided through the MCLK_IN pin while the MCLK_OUT pin must be tied to DGND. 32.768 KHz must be provided by a quartz crystal.

APB peripherals can work up to 48 MHz. Each PCLK prescaler to the sub-systems should be configured to respect this maximum frequency.

The general purpose ADC clock can run up to 33 MHz. The RTC core uses only the 32 KHz external oscillator. The TRNG can work with the external 32 kHz or with the internal cpu_hclk. If the internal clock is selected, the divisor should be configured to provide an accurate 32 kHz clock in order to respect the requirements for a true random generation.

One master clock output line can be enabled. The MCO1 is multiplexed with one general purpose I/O and can take one of the QFS outputs with a configurable prescaler.

1.8 Power management

The STCOM should be powered with, at least, two external supply voltages:

- 3.3 V for I/Os, embedded Flash, QFS, DAC, OSC, ADC general purpose, 1.2 V regulator
- 8 - 18 V for line driver

The device needs also two more supply voltages that can be generated internally:

- 1.2 V for digital cores and logic, embedded Flash, QFS and oscillator
- 5 V for the PLC AFE

1.2 V and 5 V can be provided by two internal linear regulators connected respectively to DVDD_1V2 and AVDD_5V pins and supplied respectively by DVDD_3V3_REG and PVCC pins. A bypass mode is available for the 1.2 V regulator in case an external source is used.

The power-on reset (POR) is conditioned by the level of DVDD_3 V3_IO and DVDD_1V2: at power on, the whole STCOM device is kept under reset until the two supply voltages are above the respective turn-on thresholds named V(DVDD_3 V3_IO)_TH and V(DVDD_1V2)_TH, while the device is turned off as soon as one of the voltages goes below its turn-off thresholds, namely V(DVDD_3 V3_IO)_TL and V(DVDD_1V2)_TL.

An internal comparator checks the supply voltage on AVDD_5V_AFE as well, enabling the use of the PLC AFE when the voltage is above V(AVDD_5V_AFE)_TH and disabling it when the voltage goes below V(AVDD_5V_AFE)_TL.

Refer to *Figure 5* and *Figure 6* for the detailed power supply scheme.

In case the 5 V PLC AFE supply voltage is provided externally, it is recommended to rise before or along with the 3V3 rail. Having all the supply voltages ready before the end of the boot procedure guarantees that the device is ready for operation.

Figure 5. Power supply scheme - digital section

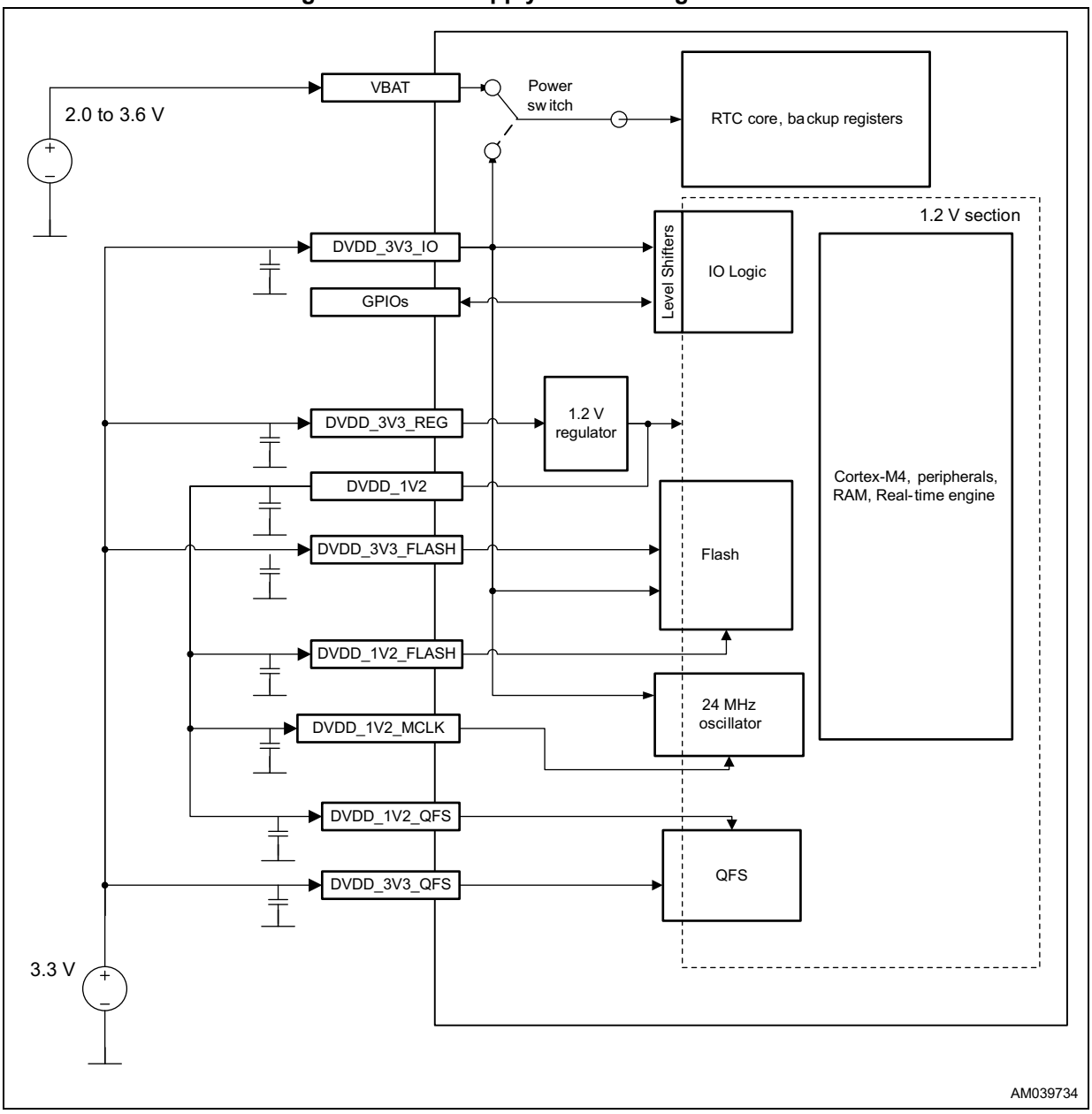
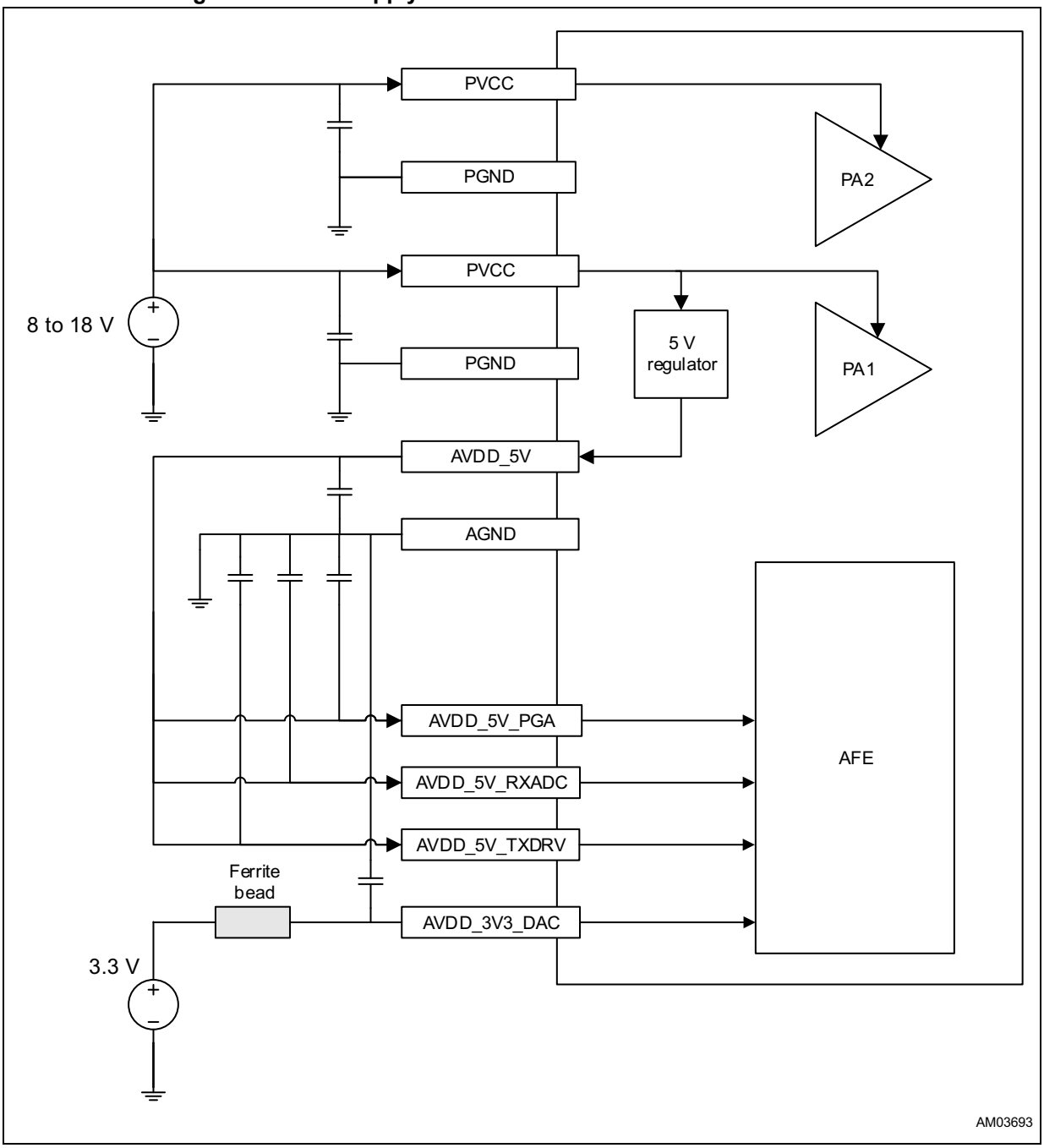


Figure 6. Power supply scheme - PLC AFE and line driver section



VBAT operation

In case the RTC peripheral is used, the VBAT pin shall be supplied (2.0 V to 3.6 V) for the RTC core operation and persistence of backup registers. An external battery or a similar power source can be used.

The VBAT operation is activated, through an on-chip power switch, when the DVDD_3V3_IO is not present. In this case the main core of the RTC and the backup registers are under the VBAT domain.

The application can constantly monitor the health of the battery by reading the voltage level present at the VBAT pin through the channel 7 of the general purpose 12-bit ADC.
A dedicated cutoff switch has been included to avoid continuous leakage from the battery when the ADC is not sampling the line.

The following formula may be used to calculate the voltage level of the VBAT pin (mV):

Equation 1

$$mV = 2 \times ADC\_data \times 3300 / 4096$$

1.9 Low power modes

A clock gating is available for any peripheral in order to save all the dynamic power contributes related the resources not used by the application.

The CPU is able to run at maximum frequency but, in case lower speed is sufficient to meet the application requirements, also scaled values are allowed. The CPU could be in low power modes waiting for wake-up events.

1.10 Real-time clock (RTC) and backup registers

The STCOM embeds an integrated real-time clock (RTC). The RTC provides a hardware calendar implementation, instead of a simple 32-bit free-running counter. The calendar can be initialized to set the current time/date of the system and provide information on sub-seconds, seconds, minutes, hours (12 or 24 format), day (day of week), date (day of month), month, and year.

Software can program the daylight saving compensation; it can control two programmable alarms (with interrupt function) that can be triggered by any combination of the calendar fields.

Synchronization can be done with an external clock using the sub-second shift feature.

RTC maskable interrupts/events are:

- Alarms: two alarms are present
- Timestamps: two timestamps are present
- Tamper: two tamper detection inputs are present

The RTC is clocked with a 32.768 kHz external crystal and has coarse calibration (periodic digital calibration), smooth calibration (0.954 ppm) and analog calibration functionalities.The 1 Hz /512 Hz internal reference clock is optionally available on RTC_TAMPB for calibration.

The RTC has also twenty 32-bit backup registers (80 bytes), available for user defined data storage. The possibility that backup registers are reset when a tamper detection event occurs is selectable by software.

1.11 Temperature sensors and overtemperature protection

The STCOM embeds an overtemperature protection mechanism, with fixed temperature threshold, preventing the device from overheating. This automatic protection acts by shutting down the PLC line driver when overheating occurs during PLC transmission. The normal operation of the line driver is restored automatically as the overtemperature event has ended.

In addition to the overtemperature automatic protection, information from two temperature sensors is provided:

- The line driver temperature sensor
- The low power temperature sensor

The first sensor monitors the line driver temperature and can be used by the RTE to prevent the line driver to be shut down abruptly by the overtemperature protection. The way to use this information may depend on the protocol and on the version of the RTE firmware, so its usage (if any) will be described within the specific firmware documentation released by STMicroelectronics®.

The second sensor monitors the temperature of the low power section of the device. It is internally connected to the channel 6 of the general purpose 12-bit ADC (see *General purpose analog-to-digital converter (ADC) on page 19* for further details) and it can be used by the application for its own purposes.

The following formula may be used to calculate the temperature (°C):

Equation 2

$$T = 30 + [(ADC\_mV - 837) / 2.59]$$

where:

ADC_mV = ADC_data x 3300 / 4096

The accuracy of the sensors is guaranteed by design. In case a higher accuracy is required on the low power temperature sensor, the user shall adopt its own calibration procedure during the application manufacturing.

1.12 Boot modes

The STCOM provides different security levels of protection:

1. **Level 1: unsecure**
   The Cortex™-M4 is accessible through the JTAG and it's possible to download the firmware in the embedded Flash using debugger plug-in or to load it from the external NVM using the system boot functionality. It's also possible to download customer OTP data such as cryptography keys. The shadow sector is not accessible.
2. **Level 2: secure**
   The JTAG is blocked and it's not possible to access the embedded Flash for external read or write operation. It's possible to load the ciphered firmware image from the external NVM and upgrade the firmware thanks to the IAP functionality. Read access to the embedded Flash is possible to the Cortex™-M4 code, including the shadow sector.
3. **Level 3: secure and locked**
   The JTAG is blocked and it's not possible to access the embedded Flash for external read or write operation. Some embedded Flash sectors are locked. It's possible to upgrade the firmware thanks to the IAP functionality unless the new image tries to change a locked area. Read access to the embedded Flash is possible to the Cortex™-M4 code, including the shadow sector.
4. **Level 4: secure for customer loader**
   The JTAG is blocked and it is not possible to access the embedded Flash for the external read or write operation via the JTAG, while the read and write access is allowed to the Cortex™-M4 code (with the exception of the shadow sector). With respect to the Level 2, there is no load or upgrade of the firmware image from the external NVM. The firmware image shall be already present in the embedded Flash (loaded in Level 1) and a customer application (secondary bootloader) can manage upgrades.
5. **Level 1*: secure erase and unlocking**
   The Cortex™-M4 is accessible through the JTAG and it's possible to download firmware in the embedded Flash. Before the unlocking, the embedded Flash is fully erased including the customer OTP data. The shadow sector is not accessible.

In order to respect these security requirements, the STCOM embeds a bootloader code. The user can also configure the boot mode through the BOOT0/1 pins to select the proper mode. The following boot modes are available:

1. **Normal mode:** this is the standard way of booting the code and eventually load (or restore) a new image version from the external NVM.
2. **Customer OTP write mode:** in this mode the user can write its security keys and data (e.g.: custom EUI48). After booting in this mode the security level is 2 (secure) or 4 (secure for customer loader) based on the selected option. In the security level 2 only ciphered firmware can be loaded from an external memory while in the security level 4 the firmware upgrade is left to a customer bootloader.
3. **Unlocking mode:** this is the boot mode that enables again all the debug feature.
4. **Low power mode:** the minimal boot mode to guarantee low power operations. The RTE is not enabled and the Cortex™-M4 code is executed as soon as possible at 24 MHz (the user can then scale the clock up or down).

The relationship between the security level and boot mode are shown in *Table 5*.

Table 5. Boot mode and security level relationship

Boot mode	Level 1	Level 2	Level 3	Level 4	Level 1*
Normal mode	Yes	Yes If lock option selected for some area → go to level 3	Yes, but no update is performed on locked sector	Yes (no update is performed)	Yes
Customer OTP write mode	Yes → go to level 2 or 4	No	No	No	No
Unlocking mode	Yes → go to level 1*	Yes → go to level 1*	Yes → go to level 1*	Yes → go to level 1*	Yes → go to level 1*
Low power mode	Yes	Yes	Yes	Yes	Yes

Table 6 shows the values of the boot pins for each boot mode.

Table 6. Boot modes and BOOT0/1 pin values

Boot mode	Boot mode value	BOOT1	BOOT0
Normal boot	0x2	1	0
Customer OTP write	0x0	0	0
Unlocking	0x1	0	1
Low power	0x3	1	1

1.13 System reprogrammability

The STCOM supports both in-system and in-application programming (ISP and IAP) modes through the use of the embedded Flash and an external non-volatile memory (NVM). If the external NVM contains two firmware copies, it's also possible to roll back to the previous firmware version in case of firmware malfunctioning. The change of firmware to enable different functionalities will require a complete reset of the device if the customer does not implement its own bootloader.

1.13.1 In-system programming (ISP)

The ISP mode allows the user to erase and program the embedded Flash through the JTAG port. This mode can be inhibited to enhance the security level of the device.

1.13.2 In-application programming (IAP)

The IAP mode allows the application on board to store in an external non-volatile memory the firmware to be downloaded into the internal embedded Flash. The firmware image in the NVM is copied into the internal embedded Flash at the power-on. The boot code inside the device takes care of the integrity check, embedded Flash erasure and programming. IAP can be done using the power line or by the local upgrade port. The customer can also write its dedicated bootloader to perform IAP with the activation of a specific security level.

2 Pinout and pin description

2.1 Pin definition

Figure 7. TQFP176 pinout

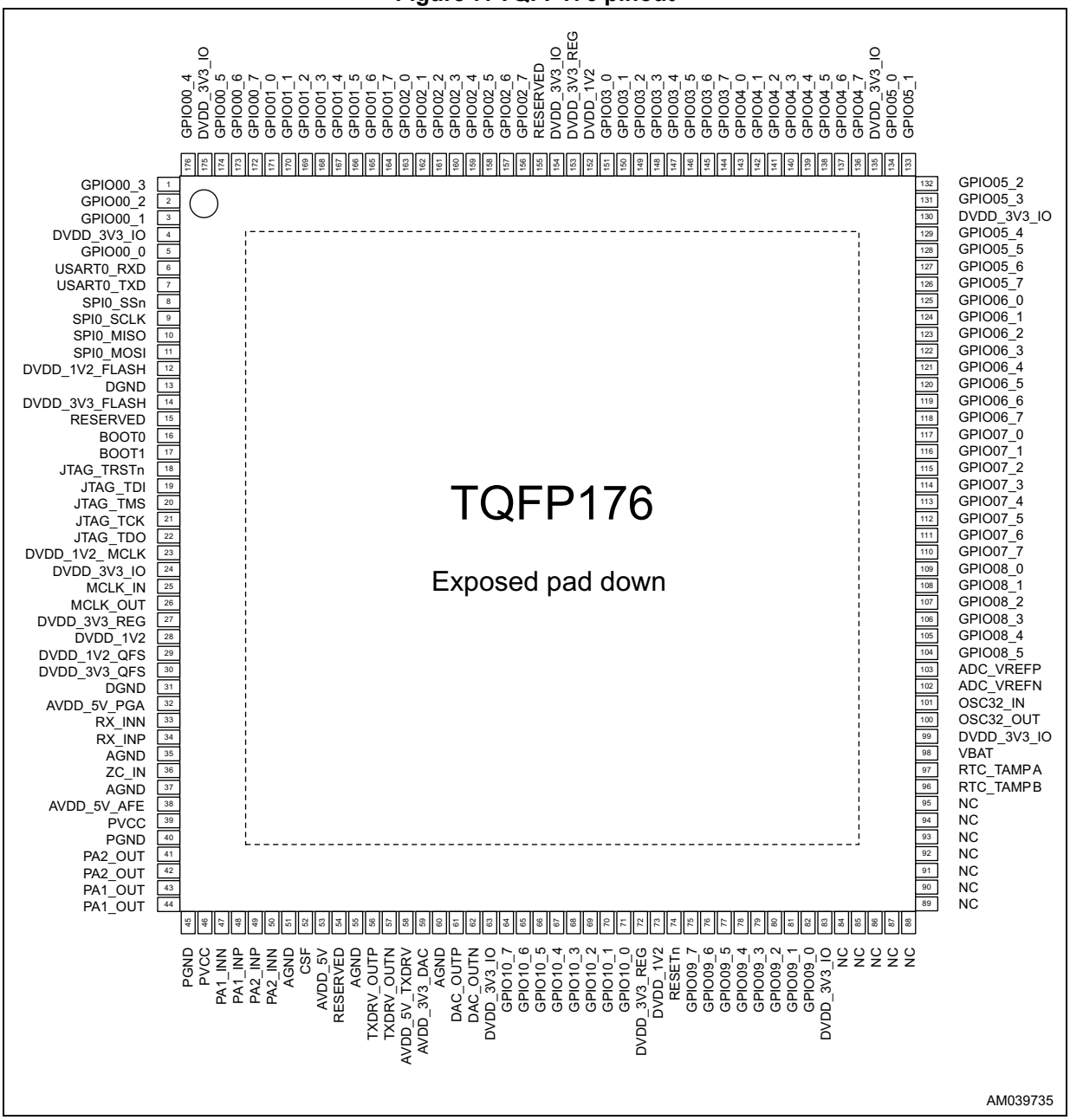


Table 7. Pin description

Pin	Pin name	Type(1)	Dir.(2)	RS(3)	Description
1	GPIO00_3	D	I/O	I	General purpose I/O, SPI1_MOSI, AT1_CH_1, FSMC_PCAD_17
2	GPIO00_2	D	I/O	I	General purpose I/O, SPI1_SS, AT1_BKIN, FSMC_PCAD_18, USART0_SCLK
3	GPIO00_1	D	I/O	I	General purpose I/O, USART0_CTS, FSMC_PCAD_19
4	DVDD_3 V3_IO	S	I	I	I/O 3.3 V supply
5	GPIO00_0	D	I/O	I	General purpose I/O, USART0_RTS, FSMC_PCAD_20
6	USART0_RXD	D	I	I	USART0_RXD
7	USART0_TXD	D	O	I	USART0_TXD
8	SPI0_SSn	D	OD	I	SPI0_SSn
9	SPI0_SCLK	D	O	I	SPI0_SCLK
10	SPI0_MISO	D	I	I	SPI0_MISO
11	SPI0_MOSI	D	O	I	SPI0_MOSI
12	DVDD_1V2_FLASH	S	I	I	Embedded Flash memory 1.2 V supply
13	DGND	S	-	-	Embedded Flash memory ground
14	DVDD_3 V3_FLASH	S	I	I	Embedded Flash memory 3.3 V supply
15	RESERVED	-	-	-	Reserved, tie to DGND
16	BOOT0	D	I	I	Boot mode selector pin 0
17	BOOT1	D	I	I	Boot mode selector pin 1
18	JTAG_TRSTn	D	I	I	JTAG test reset - active low
19	JTAG_TDI	D	I	I	JTAG test data input
20	JTAG_TMS	D	I	I	JTAG test mode select input, SWIO
21	JTAG_TCK	D	I	I	JTAG test clock input, SWCLK
22	JTAG_TDO	D	O	I	JTAG test data output, SWV
23	DVDD_1V2_ MCLK	S	I	I	24 MHz oscillator 1.2 V supply
24	DVDD_3 V3_IO	S	I	I	I/O 3.3 V supply
25	MCLK_IN	A	-	-	24 MHz oscillator input
26	MCLK_OUT	A	-	-	24 MHz oscillator output
27	DVDD_3 V3_REG	S	I	I	3.3 V input for the 1.2 V regulator
28	DVDD_1V2	S	I/O	I/O	1.2 V regulator output / external supply input
29	DVDD_1V2_QFS	S	I	I	QFS 1.2 V supply
30	DVDD_3 V3_QFS	S	I	I	QFS 3.3 V supply
31	DGND	S	-	-	QFS ground
32	AVDD_5V_PGA	S	I	I	PGA 5 V supply
33	RX_INN	A	I	I	PGA negative input

Table 7. Pin description (continued)

Pin	Pin name	Type(1)	Dir.(2)	RS(3)	Description
34	RX_INP	A	I	I	PGA positive input
35	AGND	S	-	-	PGA ground
36	ZC_IN	A	I	I	Zero crossing comparator input
37	ZC_AGND_REF	A	I	I	Zero crossing comparator ground reference - connect to AGND
38	AVDD_5V_AFE	S	I	I	PLC AFE 5 V supply + receiver ADC supply
39	PVCC	S	I	I	PA supply
40	PGND	S	-	-	PA ground
41	PA2_OUT	A	O	O	PA2 output
42	PA2_OUT	A	O	O	PA2 output
43	PA1_OUT	A	O	O	PA1 output
44	PA1_OUT	A	O	O	PA1 output
45	PGND	S	-	-	PA ground
46	PVCC	S	I	I	PA supply / 5 V regulator input voltage
47	PA1_INN	A	I	I	PA1 inverting input
48	PA1_INP	A	I	I	PA1 non-inverting input
49	PA2_INP	A	I	I	PA2 non-inverting input
50	PA2_INN	A	I	I	PA2 inverting input
51	AGND	S	-	-	5 V regulator ground
52	CSF	A	I/O	I/O	Current sense feedback
53	AVDD_5V	S	I/O	I/O	5 V regulator output / external supply input
54	RESERVED	-	-	-	Reserved - connect to AGND
55	AGND	S	-	-	Transmission predriver ground
56	TXDRV_OUTP	A	O	O	Transmission predriver positive output
57	TXDRV_OUTN	A	O	O	Transmission predriver negative output
58	AVDD_5V_TXDRV	S	I	I	Transmission predriver 5 V supply
59	AVDD_3 V3_DAC	S	I	I	Transmission DAC 3.3 V supply
60	AGND	S	-	-	Transmission DAC ground
61	DAC_OUTP	A	O	O	Transmission DAC positive output
62	DAC_OUTN	A	O	O	Transmission DAC negative output
63	DVDD_3 V3_IO	S	I	I	I/O 3.3 V supply
64	GPIO10_7	D	I/O	I	General purpose I/O, USART4_SCLK, AT0_BKIN, SPI2_SSn, I2C2_SCL
65	GPIO10_6	D	I/O	I	General purpose I/O, USART4_TXD, AT0_CH_1, SPI2_SCLK, I2C2_SDA

Table 7. Pin description (continued)

Pin	Pin name	Type(1)	Dir.(2)	RS(3)	Description
66	GPIO10_5	D	I/O	I	General purpose I/O, USART4_RXD, AT0_CH_2, SPI2_MISO, I2C0_SCL
67	GPIO10_4	D	I/O	I	General purpose I/O, USART4_CTS, AT0_CH_3, SPI2_MOSI, I2C0_SDA
68	GPIO10_3	D	I/O	I	General purpose I/O, USART4_RTS, AT0_CH_4, USART3_CTS, I2C2_SMBA
69	GPIO10_2	D	I/O	I	General purpose I/O, AT0_CHN_1, USART3_RTS, I2C0_SMBA
70	GPIO10_1	D	I/O	I	General purpose I/O, AT0_CHN_2, USART3_RXD
71	GPIO10_0	D	I/O	I	General purpose I/O, AT0_CHN_3, USART3_TXD
72	DVDD_3 V3_REG	S	I	I	3.3 V input for the 1.2 V regulator
73	DVDD_1V2	S	I/O	I/O	1.2 V regulator output / external supply input
74	RESETn	D	I/OD	I/OD	Reset input, open drain output - active low
75	GPIO09_7	D	I/O	I	General purpose I/O, AT0_ETR, ETM_SWO, SPI4_SCLK
76	GPIO09_6	D	I/O	I	General purpose I/O, USART3_SCLK, ETM_DATA_3, SPI4_MISO
77	GPIO09_5	D	I/O	I	General purpose I/O, ETM_DATA_2, SPI4_MOSI
78	GPIO09_4	D	I/O	I	General purpose I/O, ETM_DATA_1, SPI4_SSn
79	GPIO09_3	D	I/O	I	General purpose I/O, ETM_DATA_0, USART2_CTS
80	GPIO09_2	D	I/O	I	General purpose I/O, ETM_CLKOUT, USART2_RTS
81	GPIO09_1	D	I/O	I	General purpose I/O, CAN1_RX, USART2_RXD
82	GPIO09_0	D	I/O	I	General purpose I/O, CAN1_TX, USART2_TXD
83	DVDD_3 V3_IO	S	I	I	I/O 3.3 V supply
84	N. C.	-	-	-	Not connected
85	N. C.	-	-	-	Not connected
86	N. C.	-	-	-	Not connected
87	N. C.	-	-	-	Not connected
88	N. C.	-	-	-	Not connected
89	N. C.	-	-	-	Not connected
90	N. C.	-	-	-	Not connected
91	N. C.	-	-	-	Not connected
92	N. C.	-	-	-	Not connected
93	N. C.	-	-	-	Not connected
94	N. C.	-	-	-	Not connected
95	N. C.	-	-	-	Not connected
96	RTC_TAMPB	D	I/O	I	Tamper input B, RTC clock output

Table 7. Pin description (continued)

Pin	Pin name	Type(1)	Dir.(2)	RS(3)	Description
97	RTC_TAMPA	D	I	I	Tamper input A
98	VBAT	S	I	I	2.0 to 3.6 V battery supply input
99	DVDD_3 V3_IO	S	I	I	I/O 3.3 V supply
100	OSC32_OUT	A	-	-	32 kHz oscillator output
101	OSC32_IN	A	-	-	32 kHz oscillator input
102	ADC_VREFN	A	I	I	General purpose ADC negative reference voltage input
103	ADC_VREFP	A	I	I	General purpose ADC positive reference voltage input
104	GPIO08_5	D	I/O	I	General purpose I/O, ADC_MUX_VIN_5, SPI3_SSn, USART2_SCLK
105	GPIO08_4	D	I/O	I	General purpose I/O, ADC_MUX_VIN_4, SPI3_SCLK
106	GPIO08_3	D	I/O	I	General purpose I/O, ADC_MUX_VIN_3, USART1_CTS, SPI3_MISO
107	GPIO08_2	D	I/O	I	General purpose I/O, ADC_MUX_VIN_2, USART1_RTS, SPI3_MOSI
108	GPIO08_1	D	I/O	I	General purpose I/O, ADC_MUX_VIN_1, USART1_RXD, I2C1_SCL
109	GPIO08_0	D	I/O	I	General purpose I/O, ADC_MUX_VIN_0, USART1_TXD, I2C1_SDA, AT1_ETR
110	GPIO07_7	D	I/O	I	General purpose I/O, AT1_CHN_3, SPI1_SCLK
111	GPIO07_6	D	I/O	I	General purpose I/O, AT1_CHN_2, SPI1_MISO
112	GPIO07_5	D	I/O	I	General purpose I/O, AT1_CHN_1, SPI1_MOSI
113	GPIO07_4	D	I/O	I	General purpose I/O, AT1_CH_4, SPI1_SSn
114	GPIO07_3	D	I/O	I	General purpose I/O, AT1_CH_3
115	GPIO07_2	D	I/O	I	General purpose I/O, AT1_CH_2
116	GPIO07_1	D	I/O	I	General purpose I/O, AT1_CH_1, CAN0_RX
117	GPIO07_0	D	I/O	I	General purpose I/O, AT1_BKIN, CAN0_TX
118	GPIO06_7	D	I/O	I	General purpose I/O, SPI4_SSn, ETM_SWO
119	GPIO06_6	D	I/O	I	General purpose I/O, SPI4_SCLK, ETM_DATA_3
120	GPIO06_5	D	I/O	I	General purpose I/O, SPI4_MISO, ETM_DATA_2
121	GPIO06_4	D	I/O	I	General purpose I/O, SPI4_MOSI, ETM_DATA_1
122	GPIO06_3	D	I/O	I	General purpose I/O, USART3_CTS, I2C1_SCL, ETM_DATA_0
123	GPIO06_2	D	I/O	I	General purpose I/O, USART3_RTS, I2C1_SDA, ETM_CLKOUT
124	GPIO06_1	D	I/O	I	General purpose I/O, USART3_RXD, I2C1_SMBA, I2C2_SCL
125	GPIO06_0	D	I/O	I	General purpose I/O, USART3_TXD, I2C2_SDA
126	GPIO05_7	D	I/O	I	General purpose I/O, USART3_SCLK, I2C2_SMBA

Table 7. Pin description (continued)

Pin	Pin name	Type(1)	Dir.(2)	RS(3)	Description
127	GPIO05_6	D	I/O	I	General purpose I/O, USART0_CTS
128	GPIO05_5	D	I/O	I	General purpose I/O, USART0_RTS
129	GPIO05_4	D	I/O	I	General purpose I/O, MCO1
130	DVDD_3 V3_IO	S	I	I	I/O 3.3 V supply
131	GPIO05_3	D	I/O	I	General purpose I/O, FSMC_Ebar_1
132	GPIO05_2	D	I/O	I	General purpose I/O, USART2_SCLK, FSMC_Ebar_0
133	GPIO05_1	D	I/O	I	General purpose I/O, USART2_RXD, SPI2_SSn, FSMC_BLn_0
134	GPIO05_0	D	I/O	I	General purpose I/O, USART2_TXD, SPI2_SCLK, FSMC_BLn_1
135	DVDD_3 V3_IO	S	I	I	I/O 3.3 V supply
136	GPIO04_7	D	I/O	I	General purpose I/O, USART2_CTS, SPI2_MISO, FSMC_PCDA_0
137	GPIO04_6	D	I/O	I	General purpose I/O, USART2_RTS, SPI2_MOSI, FSMC_PCDA_1, MCO1
138	GPIO04_5	D	I/O	I	General purpose I/O, FSMC_PCDA_2
139	GPIO04_4	D	I/O	I	General purpose I/O, FSMC_PCDA_3
140	GPIO04_3	D	I/O	I	General purpose I/O, FSMC_PCDA_4
141	GPIO04_2	D	I/O	I	General purpose I/O, FSMC_PCDA_5
142	GPIO04_1	D	I/O	I	General purpose I/O, FSMC_PCDA_6
143	GPIO04_0	D	I/O	I	General purpose I/O, FSMC_PCDA_7
144	GPIO03_7	D	I/O	I	General purpose I/O, SPI3_SSn, FSMC_PCDA_8
145	GPIO03_6	D	I/O	I	General purpose I/O, SPI3_SCLK, FSMC_PCDA_9
146	GPIO03_5	D	I/O	I	General purpose I/O, SPI3_MISO, FSMC_PCDA_10
147	GPIO03_4	D	I/O	I	General purpose I/O, SPI3_MOSI, FSMC_PCDA_11, USART3_SCLK
148	GPIO03_3	D	I/O	I	General purpose I/O, SPI2_SSn, USART3_CTS, FSMC_PCDA_12
149	GPIO03_2	D	I/O	I	General purpose I/O, SPI2_SCLK, USART3_RTS, FSMC_PCDA_13
150	GPIO03_1	D	I/O	I	General purpose I/O, SPI2_MISO, USART3_RXD, FSMC_PCDA_14
151	GPIO03_0	D	I/O	I	General purpose I/O, SPI2_MOSI, USART3_TXD, FSMC_PCDA_15
152	DVDD_1V2	S	I/O	I/O	1.2 V regulator output / external supply input
153	DVDD_3 V3_REG	S	I	I	3.3 V input for the 1.2 V regulator
154	DVDD_3 V3_IO	S	I	I	I/O 3.3 V supply
155	RESERVED	-	-	-	Reserved - connect to DGND

Table 7. Pin description (continued)

Pin	Pin name	Type(1)	Dir.(2)	RS(3)	Description
156	GPIO02_7	D	I/O	I	General purpose I/O, AT0_BKIN, FSMC_Lbar, USART4_SCLK
157	GPIO02_6	D	I/O	I	General purpose I/O, AT0_CH_1, FSMC_PCWEn, USART4_TXD
158	GPIO02_5	D	I/O	I	General purpose I/O, AT0_CHN_1, FSMC_PCOEn, USART4_RXD
159	GPIO02_4	D	I/O	I	General purpose I/O, AT0_CH_2, FSMC_PCAD_0, USART4_CTS
160	GPIO02_3	D	I/O	I	General purpose I/O, AT0_CHN_2, FSMC_PCAD_1, USART4_RTS
161	GPIO02_2	D	I/O	I	General purpose I/O, AT0_CH_3, FSMC_PCAD_2
162	GPIO02_1	D	I/O	I	General purpose I/O, AT0_CHN_3, I2C2_SCL, FSMC_PCAD_3
163	GPIO02_0	D	I/O	I	General purpose I/O, AT0_CH_4, I2C2_SDA, FSMC_PCAD_4
164	GPIO01_7	D	I/O	I	General purpose I/O, AT0_ETR, I2C2_SMBA, FSMC_PCAD_5, I2C1_SMBA
165	GPIO01_6	D	I/O	I	General purpose I/O, I2C1_SCL, CAN1_RX, FSMC_PCAD_6
166	GPIO01_5	D	I/O	I	General purpose I/O, I2C1_SDA, CAN1_TX, FSMC_PCAD_7
167	GPIO01_4	D	I/O	I	General purpose I/O, USART1_CTS, CAN0_RX, FSMC_PCAD_8
168	GPIO01_3	D	I/O	I	General purpose I/O, USART1_RTS, CAN0_TX, FSMC_PCAD_9
169	GPIO01_2	D	I/O	I	General purpose I/O, USART1_RXD, AT1_ETR, FSMC_PCAD_10
170	GPIO01_1	D	I/O	I	General purpose I/O, USART1_TXD, AT1_CHN_3, FSMC_PCAD_11
171	GPIO01_0	D	I/O	I	General purpose I/O, I2C0_SMBA, AT1_CHN_2, FSMC_PCAD_12, USART1_SCLK
172	GPIO00_7	D	I/O	I	General purpose I/O, I2C0_SCL, AT1_CHN_1, FSMC_PCAD_13
173	GPIO00_6	D	I/O	I	General purpose I/O, I2C0_SDA, AT1_CH_4, FSMC_PCAD_14
174	GPIO00_5	D	I/O	I	General purpose I/O, SPI1_SCLK, AT1_CH_3, FSMC_PCAD_15
175	DVDD_3 V3_IO	S	I	I	I/O 3.3 V supply

Table 7. Pin description (continued)

Pin	Pin name	Type(1)	Dir.(2)	RS(3)	Description
176	GPIO00_4	D	I/O	I	General purpose I/O, SPI1_MISO, AT1_CH_2, FSMC_PCAD_16
177	EXPAD	S	-	-	Exposed pad - DGND

1. Type: D = digital; A = analog; S = supply/ground.
2. Direction: I = input; O = output; I/O = input/output, OD = open drain.
3. Reset status: I = input, I/O = input/output, O = output.

2.2 GPIOs multiplexing scheme

In the STCOM, peripherals are connected to I/Os through a multiplexer. At a time one single peripheral can control the I/Os. In this way, there is no conflict between peripherals sharing the same I/O pins.

Thanks to a set of configuration registers, the user can select one of the 4 possible alternate functions for each pin as described in *Table 8*.

Table 8. GPIOs multiplexing scheme

Pin name	Selection: 000	Selection: 001	Selection: 010	Selection: 011
GPIO00_0	USART0_RTS	-	FSMC_PCAD_20	-
GPIO00_1	USART0_CTS	-	FSMC_PCAD_19	-
GPIO00_2	SPI1_SS	AT1_BKIN	FSMC_PCAD_18	USART0_SCLK
GPIO00_3	SPI1_MOSI	AT1_CH_1	FSMC_PCAD_17	-
GPIO00_4	SPI1_MISO	AT1_CH_2	FSMC_PCAD_16	-
GPIO00_5	SPI1_SCLK	AT1_CH_3	FSMC_PCAD_15	-
GPIO00_6	I2C0_SDA	AT1_CH_4	FSMC_PCAD_14	-
GPIO00_7	I2C0_SCL	AT1_CHN_1	FSMC_PCAD_13	-
GPIO01_0	I2C0_SMBA	AT1_CHN_2	FSMC_PCAD_12	USART1_SCLK
GPIO01_1	USART1_TXD	AT1_CHN_3	FSMC_PCAD_11	-
GPIO01_2	USART1_RXD	AT1_ETR	FSMC_PCAD_10	-
GPIO01_3	USART1_RTS	CAN0_TX	FSMC_PCAD_9	-
GPIO01_4	USART1_CTS	CAN0_RX	FSMC_PCAD_8	-
GPIO01_5	I2C1_SDA	CAN1_TX	FSMC_PCAD_7	-
GPIO01_6	I2C1_SCL	CAN1_RX	FSMC_PCAD_6	-
GPIO01_7	AT0_ETR	I2C2_SMBA	FSMC_PCAD_5	I2C1_SMBA
GPIO02_0	AT0_CH_4	I2C2_SDA	FSMC_PCAD_4	-
GPIO02_1	AT0_CHN_3	I2C2_SCL	FSMC_PCAD_3	-
GPIO02_2	AT0_CH_3	-	FSMC_PCAD_2	-
GPIO02_3	AT0_CHN_2	-	FSMC_PCAD_1	USART4_RTS
GPIO02_4	AT0_CH_2	-	FSMC_PCAD_0	USART4_CTS
GPIO02_5	AT0_CHN_1	-	FSMC_PCOEn	USART4_RXD
GPIO02_6	AT0_CH_1	-	FSMC_PCWEn	USART4_TXD
GPIO02_7	AT0_BKIN	-	FSMC_Lbar	USART4_SCLK
GPIO03_0	SPI2_MOSI	USART3_TXD	FSMC_PCDA_15	-
GPIO03_1	SPI2_MISO	USART3_RXD	FSMC_PCDA_14	-
GPIO03_2	SPI2_SCLK	USART3_RTS	FSMC_PCDA_13	-
GPIO03_3	SPI2_SS	USART3_CTS	FSMC_PCDA_12	-
GPIO03_4	SPI3_MOSI	-	FSMC_PCDA_11	USART3_SCLK

Table 8. GPIOs multiplexing scheme (continued)

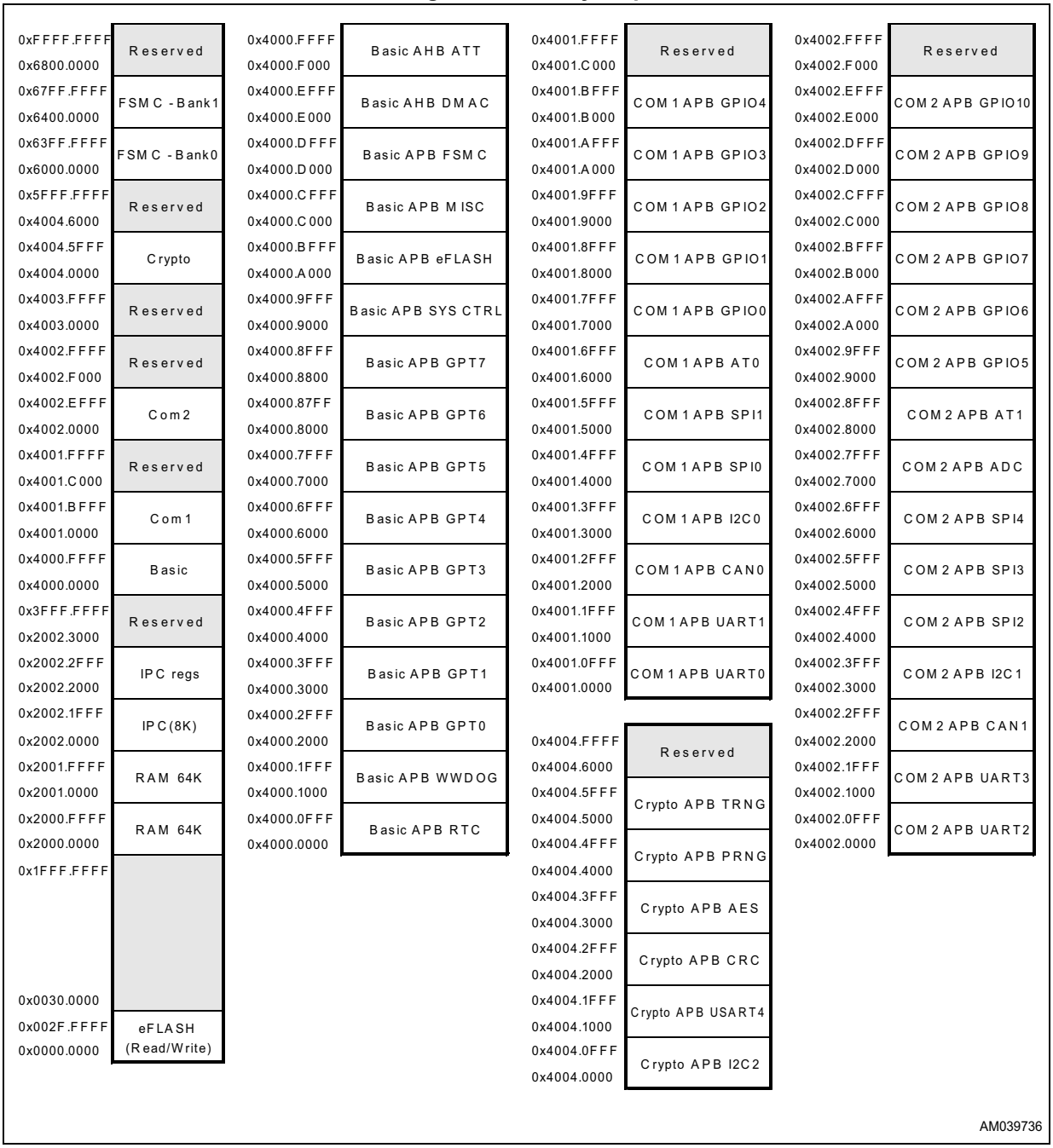
Pin name	Selection: 000	Selection: 001	Selection: 010	Selection: 011
GPIO03_5	SPI3_MISO	-	FSMC_PCDA_10	-
GPIO03_6	SPI3_SCLK	-	FSMC_PCDA_9	-
GPIO03_7	SPI3_SS	-	FSMC_PCDA_8	-
GPIO04_0	-	-	FSMC_PCDA_7	-
GPIO04_1	-	-	FSMC_PCDA_6	-
GPIO04_2	-	-	FSMC_PCDA_5	-
GPIO04_3	-	-	FSMC_PCDA_4	-
GPIO04_4	-	-	FSMC_PCDA_3	-
GPIO04_5	-	-	FSMC_PCDA_2	-
GPIO04_6	USART2_RTS	SPI2_MOSI	FSMC_PCDA_1	-
GPIO04_7	USART2_CTS	SPI2_MISO	FSMC_PCDA_0	-
GPIO05_0	USART2_TXD	SPI2_SCLK	FSMC_BLn_1	-
GPIO05_1	USART2_RXD	SPI2_SS	FSMC_BLn_0	-
GPIO05_2	USART2_SCLK	-	FSMC_Ebar_0	-
GPIO05_3	-	-	FSMC_Ebar_1	-
GPIO05_4	MCO1	-	-	-
GPIO05_5	-	USART0_RTS	-	-
GPIO05_6	-	USART0_CTS	-	-
GPIO05_7	USART3_SCLK	-	I2C2_SMBA	-
GPIO06_0	USART3_TXD	-	I2C2_SDA	-
GPIO06_1	USART3_RXD	I2C1_SMBA	I2C2_SCL	-
GPIO06_2	USART3_RTS	I2C1_SDA	-	ETM_CLKOUT
GPIO06_3	USART3_CTS	I2C1_SCL	-	ETM_DATA_0
GPIO06_4	SPI4_MOSI	-	-	ETM_DATA_1
GPIO06_5	SPI4_MISO	-	-	ETM_DATA_2
GPIO06_6	SPI4_SCLK	-	-	ETM_DATA_3
GPIO06_7	SPI4_SS	-	-	ETM_SWO
GPIO07_0	AT1_BKIN	-	CAN0_TX	-
GPIO07_1	AT1_CH_1	-	CAN0_RX	-
GPIO07_2	AT1_CH_2	-	-	-
GPIO07_3	AT1_CH_3	-	-	-
GPIO07_4	AT1_CH_4	SPI1_SS	-	-
GPIO07_5	AT1_CHN_1	SPI1_MOSI	-	-
GPIO07_6	AT1_CHN_2	SPI1_MISO	-	-
GPIO07_7	AT1_CHN_3	SPI1_SCLK	-	-

Table 8. GPIOs multiplexing scheme (continued)

Pin name	Selection: 000	Selection: 001	Selection: 010	Selection: 011
GPIO08_0	ADC_CH_0	USART1_TXD	I2C1_SDA	AT1_ETR
GPIO08_1	ADC_CH_1	USART1_RXD	I2C1_SCL	-
GPIO08_2	ADC_CH_2	USART1_RTS	SPI3_MOSI	-
GPIO08_3	ADC_CH_3	USART1_CTS	SPI3_MISO	-
GPIO08_4	ADC_CH_4	-	SPI3_SCLK	-
GPIO08_5	ADC_CH_5	-	SPI3_SS	USART2_SCLK
GPIO09_0	-	-	CAN1_TX	USART2_TXD
GPIO09_1	-	-	CAN1_RX	USART2_RXD
GPIO09_2	-	-	ETM_CLKOUT	USART2_RTS
GPIO09_3	-	-	ETM_DATA_0	USART2_CTS
GPIO09_4	-	-	ETM_DATA_1	SPI4_SS
GPIO09_5	-	-	ETM_DATA_2	1SPI4_MOSI
GPIO09_6	-	USART3_SCLK	ETM_DATA_3	SPI4_MISO
GPIO09_7	-	AT0_ETR	ETM_SWO	SPI4_SCLK
GPIO10_0	-	AT0_CHN_3	USART3_TXD	-
GPIO10_1	-	AT0_CHN_2	USART3_RXD	-
GPIO10_2	-	AT0_CHN_1	USART3_RTS	I2C0_SMBA
GPIO10_3	USART4_RTS	AT0_CH_4	USART3_CTS	I2C2_SMBA
GPIO10_4	USART4_CTS	AT0_CH_3	SPI2_MOSI	I2C0_SDA
GPIO10_5	USART4_RXD	AT0_CH_2	SPI2_MISO	I2C0_SCL
GPIO10_6	USART4_TXD	AT0_CH_1	SPI2_SCLK	I2C2_SDA
GPIO10_7	USART4_SCLK	AT0_BKIN	SPI2_SS	I2C2_SCL

3 Memory map

Figure 8. Memory map



4 Electrical characteristics

4.1 Absolute maximum ratings

Table 9. Absolute maximum ratings - voltage

Symbol	Parameter	Min.	Max.	Unit
PVCC	Line driver supply voltage range	PGND -0.3	20	V
AVDD_5V	5 V internal regulator voltage range	AGND -0.3	Min. (5.5, PVCC +0.3)	V
AVDD_5V_AFE, AVDD_5V_PGA, AVDD_5V_TXDRV	5 V PLC AFE supply voltage range	AGND -0.3	Min. (5.5, PVCC +0.3)	V
AVDD_3 V3_DAC	3.3 V PLC AFE supply voltage range	AGND -0.3	5.2	V
DVDD_3 V3_IO, DVD_3 V3_REG	I/O supply voltage range	GND-0.3	5.2	V
DVDD_3 V3_QFS	3.3 V QFS supply voltage range	DGND -0.3	5.2	V
DVDD_1V2, DVDD_1V2_FLASH	1.2 V digital supply voltage range	GND -0.3	2.4	V
DVDD_1V2_QFS	1.2 V QFS supply voltage range	GND -0.3	2.4	V
ADC_VREFP	General purpose ADC positive reference voltage range	GND -0.3	Min. (5.2, DVDD_3V3_IO + 0.3)	V
ADC_VREFN	General purpose ADC negative reference voltage range	GND -0.3	Min. (5.2, DVDD_3V3_IO + 0.3)	V
VBAT	VBAT voltage range	GND -0.3	5.2	V
DGND, AGND	Variations between different ground pins	GND -0.3	GND +0.3	V
PGND	Variations between different ground pins	AGND -0.3	AGND +0.3	V
V(DIG_IN)	Input voltage range	GND -0.3	Min. (5.2, DVDD_3V3_IO + 0.3)	V
PA_OUT	PA output pins voltage range	PGND -0.3	Min. (20, PVCC +0.3)	V
PA_IN	PA input pins voltage range	AGND -0.3	Min. (20, PVCC +0.3)	V
RX_IN	RX_IN input pins voltage range	-5.5	9	V
ZC_IN	ZC_IN voltage range	-5.5	Min. (5.5, AVDD_5V_ AFE +0.3)	V
DAC_OUT	DAC output pins voltage range	AGND -0.3	Min. (5.2, AVDD_5V_ AFE +0.3)	V
TXDRV_OUT	TXDRV output voltage range	AGND -0.3	Min. (5.5, AVDD_5V_ AFE +0.3)	V
CSF	CSF pin voltage range	AGND-0.3	AVDD_5V +0.3	V
V(MCLK)	24 MHz oscillator pins voltage range	GND-0.3	Min. (5.2, DVDD_3 V3_IO+0.3)	V

Table 9. Absolute maximum ratings - voltage (continued)

Symbol	Parameter	Min.	Max.	Unit
V(OSC32)	32 kHz oscillator pins voltage range	GND-0.3	Min. (5.2, DVDD_3V3_IO + 0.3)	V
V(ESD)	Maximum withstanding voltage range Test condition: ANSI-ESDA-JEDEC_JS-001 “human body model” acceptance criteria: “normal performance”	-2	+2	kV

Table 10. Absolute maximum ratings - current

Symbol	Parameter	Min.	Max.	Unit
I(PA_OUT)	PA repetitive RMS current	-	1.5	A rms

4.2 Thermal characteristics

Table 11. Thermal characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
T(J)	Junction temperature	-	-	125	°C
T(AMB)	Operating ambient temperature	-	-40	85	°C
T(STG)	Storage temperature	-	-50	150	°C

4.3 Operating conditions

T(AMB) = -40 to +85 °C, T(J) < 125 °C, PVCC = 18 V unless otherwise specified.

All typical values are referred to T(AMB) = 25 °C.

Power supply characteristics

Table 12. Analog supply characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(PVCC)	Line driver supply voltage	-	8	15	18	V
I(PVCC)_RX	Line driver supply current Rx mode	No load on AVDD_5V	-	500	700	µA
I(PVCC)_TX	Line driver supply current Tx mode, no load	No load on AVDD_5V Dual power amplifier configuration	-	40	60	mA
		No load on AVDD_5V Single power amplifier configuration	-	20	30	mA
V(PVCC)_TH	Line driver supply voltage turn-on threshold	-	6.6	7	7.4	V
V(PVCC)_TL	Line driver supply voltage turn-off threshold	-	6.1	6.5	6.9	V
V(PVCC)_HYST	Line driver supply voltage hysteresis	-	0.4	0.5	0.6	V
V(AVDD_5V)	5 V regulator output voltage , no load	-	4.5	5	5.5	V
V(AVDD_5V_AFE)_TH	5 V PLC AFE supply voltage turn-on threshold	-	4.07	4.14	4.21	V
V(AVDD_5V_AFE)_TL	5 V PLC AFE supply voltage turn-off threshold	-	3.98	4.05	4.12	V
V(AVDD_5V_AFE)_HYST	5 V PLC AFE supply voltage hysteresis	-	75	95	115	mV
I(5V)_RX	5 V PLC AFE supply current Rx mode	See(1) PGA maximum gain	-	54	62	mA
	5 V PLC AFE supply current Rx active mode	See(1) PGA maximum gain Rx in progress	-	61	70	mA
I(5V)_TX	5 V PLC AFE supply current Tx mode, no load	See(1)	-	9	-	mA

Table 12. Analog supply characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I(AVDD_3V3_DAC) RX	3.3 V PLC AFE supply current Rx mode	-	-	1.6	4	mA
I(AVDD_3V3_DAC) TX	3.3 V PLC AFE supply current Tx mode	DAC full scale current = 4 mA Sine wave output f = 100 kHz	-	9	13	mA
V(DVDD_3V3_IO)	Digital I/O supply voltage	-	3.0	3.3	3.6	V
V(DVDD_3V3_IO)_TH	Digital I/O supply voltage turn-on threshold	-	2.69	2.82	2.91	V
V(DVDD_3V3_IO)_TL	Digital I/O supply voltage turn-off threshold	-	2.59	2.7	2.8	V
V(DVDD_3V3_IO)_HYST	Digital I/O supply voltage hysteresis	-	91	110	127	mV
V(DVDD_3V3_REG)	1.2 V regulator input voltage	Regulator ON	3.0	3.3	3.6	V
V(DVDD_3V3_REG)	1.2 regulator input voltage	Regulator in bypass mode	-	DVDD_1V2	-	V
V(DVDD_1V2)	1.2 V regulator output voltage	Low power mode	1.218	1.233	1.26	V
		High power mode	1.275	1.285	1.3	V
I(DVDD_1V2)	1.2 V regulator output current	Low power mode	-	-	15	mA
		High power mode	-	-	300	mA
V(DVDD_1V2)_TH	1.2 V supply voltage turn-on threshold	Low and high power modes	0.86	1.11	1.4	V
V(DVDD_1V2)_TL	1.2 V supply voltage turn-off threshold	Low and high power modes	0.84	1.025	1.07	V
V(DVDD_1V2)_HYST	1.2 V supply voltage hysteresis	Low and high power modes	17	86	360	mV

1. I(5 V) = I(AVDD_5V_AFE) + I(AVDD_5V_PGA) + I(AVDD_5V_TXDRV).

Table 13. Digital supply characteristics - RTE

Symbol	Parameter(1)	Conditions	Min.	Typ.	Max.	Unit
I(DVDD_1V2)	1.2 V digital supply current	RTE frequency = 48 MHz see(2)	-	29	-	mA
I(DVDD_1V2)	1.2 V digital supply current	RTE frequency = 120 MHz see(2)	-	68	-	mA

1. Based on characterization, not tested in production.
2. The tests are performed with the following enabled digital blocks: 2 x GPT, 2 x SPI, 2 x USART, IPC, DMA, 2 x I^2C, AES, TRNG, QFS. Cortex™ frequency equals to 48 MHz and Cortex™ fetching by RAM. The value is calculated by measuring the difference in the supply current with and without RTE enabled and running.

Table 14. Digital supply characteristics - Cortex™-M4 fetching from RAM

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I(DVDD_1V2)	1.2 V digital supply current	Cortex™ frequency = 24 MHz see(1)	-	9.6	-	mA
I(DVDD_1V2)	1.2 V digital supply current	Cortex™ frequency = 48 MHz see(1)	-	16.4	-	mA
I(DVDD_1V2)	1.2 V digital supply current	Cortex™ frequency = 72 MHz see(1)	-	23.8	-	mA
I(DVDD_1V2)	1.2 V digital supply current	Cortex™ frequency = 96 MHz see(1)	-	30.9	-	mA

1. All the tests are performed with the following enabled digital blocks: 2 x GPT, 2 x SPI, 2 x USART, IPC, DMA, 2 x I^2C, AES, TRNG, QFS.

Table 15. Digital supply characteristics - Cortex™-M4 fetching data from eFlash

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I(DVDD_1V2)	1.2 V digital supply current	Cortex™ frequency = 24 MHz see(1)	-	11.2	-	mA
I(DVDD_1V2)	1.2 V digital supply current	Cortex™ frequency = 48 MHz see(1)	-	17.6	-	mA
I(DVDD_1V2)	1.2 V digital supply current	Cortex™ frequency = 72 MHz see(1)	-	24.2	-	mA
I(DVDD_1V2)	1.2 V digital supply current	Cortex™ frequency = 96 MHz see(1)	-	30.6	-	mA

1. All the tests are performed with the following enabled digital blocks: 2 x GPT, 2 x SPI, 2 x USART, IPC, DMA, 2 x I2C, AES, TRNG, QFS.

Table 16. Digital supply characteristics - DOZE (sleep)/deepsleep mode

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I(DVDD_1V2)	1.2 V digital supply current	Cortex™ in DOZE mode see(1)	-	6.5	-	mA
I(DVDD_1V2)	1.2 V digital supply current	Cortex™ in deepsleep mode see(1)	-	6.5	-	mA

1. The test is performed with the following enabled digital blocks: 2 x GPT, 2 x SPI, 2 x USART, IPC, DMA, 2 x I^2C, AES, TRNG.

Table 17. Supply characteristics - QFS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I(DVDD_1V2_QFS)	QFS power consumption from 1.2 V power supply	Master clock = 24 MHz see(1)	-	5.1	7	mA
I(DVDD_3V3_QFS)	QFS power consumption from 3.3 V power supply	Master clock = 24 MHz see(1)	-	1.1	1.6	mA

1. The test is performed with the following enabled digital blocks: 2 x GPT, 2 x SPI, 2 x USART, IPC, DMA, 2 x I^2C, AES, TRNG. The value is calculated by measuring the difference in the supply current with and without QFS enabled and running.

Table 18. 24 MHz oscillator

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f(MCLK)	Crystal oscillator frequency	-	-	24	-	MHz
C0	External quartz crystal Shunt capacitance	-	-	-	3.5	pF
ESR	External quartz crystal ESR value	See(1)	-	-	60	Ω
CL	MCLK_IN , MCLK_OUT load capacitance	See(1)	10	-	15	pF

1. Guaranteed by design, not tested in production.

Table 19. 32 kHz oscillator

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f(OSC32)	Crystal oscillator frequency	-	-	32.768	-	kHz
C0	External quartz crystal Shunt capacitance	-	-	0.9	-	pF
ESR	External quartz crystal ESR value	See(1)	-	-	60	kΩ
CL	External quartz crystal load capacitance	See(1)	-	12.5	-	pF

1. Guaranteed by design, not tested in production.

Table 20. Digital supply characteristics - I/O

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I(DVDD_3V3_IO)	3.3 V I/O digital supply current	Static consumption	-	0.9	2.9	mA
I(DVDD_3V3_IO)	3.3 V I/O digital supply current	8 GPIO toggling at 0.5 MHz with Cext ~= 50 pF see(1)	-	23.0	34	mA
I(DVDD_3V3_IO)	3.3 V I/O digital supply current	8 GPIO toggling at 1 MHz with Cext ~= 50 pF see(1)	-	24.9	39	mA
I(DVDD_3V3_IO)	3.3 V I/O digital supply current	8 GPIO toggling at 8 MHz with Cext ~= 50 pF see(1)	-	49.4	78	mA

1. The tests are performed with the following enabled digital blocks: 2 x GPT, 2 x SPI, 2 x USART, IPC, DMA, 2 x I^2C, AES, TRNG, QFS. Cortex™ frequency equals to 96 MHz and Cortex™ fetching by RAM. The values are calculated by measuring the difference in the supply current with and without 8 GPIOs enabled and toggling at the given frequency.

Table 21. I/O characteristics

Symbol	Parameter(1)	Conditions	Min.	Typ.	Max.	Unit
I (I/O)	Output current sunk by any I/Os and control pin	See(1)	-	-	8	mA
	Output current source by any I/Os and control pin	See(1)	-	-	8	

1. Guaranteed by design, not tested in production.

Table 22. Digital supply characteristics - power consumption under battery

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I(DVDD_VBAT)	Digital supply current under V_{BAT}	Static consumption	-	1.3	-	µA

4.4 PLC analog front-end (AFE) and line driver characteristics

4.4.1 Line driver characteristics

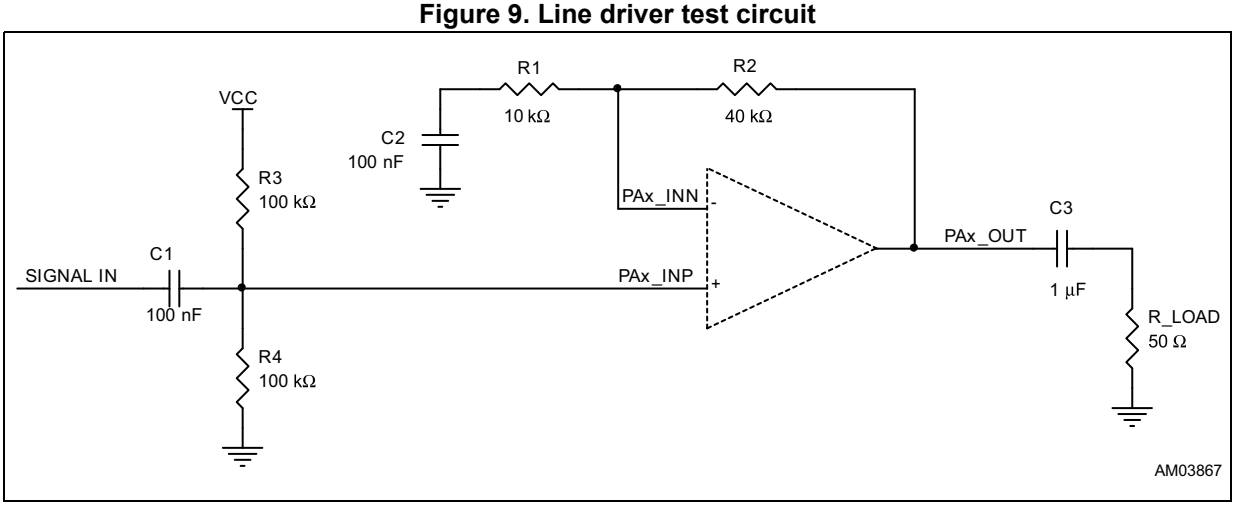
Table 23. Line driver characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(PAx_OUT) BIAS	Power amplifier output Bias voltage - Rx mode	-	-	PVCC/2	-	V
GBWP	Power amplifier Gain-bandwidth product	-	-	149	-	MHz
I(PAx_OUT) MAX	Power amplifier Maximum output current	-	-	-	1000	mA rms
V(PAx_OUT) HD2	Power amplifier output 2nd harmonic distortion	VCC = 18 V, V(PA_OUT) = 13 Vpp, Rload = 50 Ω, f = 100 kHz V(PA_OUT) DC = PVCC/2	-	-64	-51.5	dBc
V(PAx_OUT) HD3	Power amplifier output 3rd harmonic distortion		-	-67	-52.5	dBc
V(PAx_OUT) THD	Power amplifier output Total harmonic distortion		-	-61	-50	dB
V(PAx_OUT) HD2	Power amplifier output 2nd harmonic distortion	VCC = 18 V, V(PA_OUT) = 13 Vpp, Rload = 50 Ω, f = 500 kHz V(PA_OUT) DC = PVCC/2	-	-57	-50	dBc
V(PAx_OUT) HD3	Power amplifier output 3rd harmonic distortion		-	-58	-46	dBc
V(PAx_OUT) THD	Power amplifier output Total harmonic distortion		-	-54	-45	dB
C(PAx_INP), C(PAx_INN)	Power amplifier Input capacitance	PA_IN+ vs. VSS (see(1))	-	10	-	pF
		PA_IN- vs. VSS (see(1))	-	10	-	pF
PSRR	Input referred power supply rejection ratio	50 Hz	-	100	-	dB
		1 kHz	-	88	-	dB
CSF_RATIO	Ratio between PA_OUT and CSF output current	-	85	110	138	-

1. Not tested in production, guaranteed by design.

4.4.2 Line driver test circuit

Figure 9. Line driver test circuit



4.4.3 AFE characteristics

Transmission path characteristics

Table 24. DAC and predriver characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I(DAC_OUT) CURRENT	DAC output current	Rx mode, current measured on both outputs	-	0	-	mA
I(DAC_OUT) CURRENT	DAC output current	Tx mode, current measured on both outputs	-	4	-	mA
V(DAC_OUT)	Tx mode, differential	Rload = 120 Ω ± 1%	0.9	1	1.3	Vpp
V(TX_OUT) BIAS	Transmitter output bias voltage	Rx mode	-	AVDD_5V_TXDRV/2	-	V
-	Predriver load impedance	-	1	-	-	kΩ
V(TX_OUT) HD2	Transmitter output 2nd harmonic distortion - see(1)	V(TX_OUT) = 4.7 V pk-pk, no load, Fout = 100 KHz	-	-76	-	dBc
V(TX_OUT) HD3	Transmitter output 3rd harmonic distortion see(1)		-	-83	-	dBc
V(TX_OUT) THD	Transmitter output total harmonic distortion see(1)		-	-74	-	dB
V(TX_OUT) HD2	Transmitter output 2nd harmonic distortion - see(1)	V(TX_OUT) = 4.7 V pk-pk, no load, Fout = 500 KHz	-	-74	-	dBc
V(TX_OUT) HD3	Transmitter output 3rd harmonic distortion see(1)		-	-82	-	dBc
V(TX_OUT) THD	Transmitter output total harmonic distortion see(1)		-	-73	-	dB

1. DAC + predriver chain distortion.

Reception path characteristics

Table 25. Receiver input referred noise

Symbol	Parameter[1]	Conditions	Min.	Typ.	Max.	Unit
V(RX_INP - RX_INN)	Receiver input referred noise	CENELEC-A (35 kHz to 95 kHz)	-	16	-	dBµV
		CENELEC -B (95 kHz to 125 kHz)	-	12	-	dBµV
		CENELEC -C (125 kHz to 140 kHz)	-	8	-	dBµV
		CENELEC -D (140 kHz to 148 kHz)	-	5	-	dBµV
		ARIB STD-T84 (35 kHz to 400 kHz)	-	22	-	dBµV
		FCC-LOW (35 kHz to 125 kHz)	-	17	-	dBµV
		G3-FCC (150 kHz to 490 kHz)	-	21	-	dBµV

1. Not tested in production, guaranteed by design.

Table 26. PLC PGA characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(RX_INP), V(RX_INN)	Receiver input maximum voltage	Single-ended mode	-	10	-	V p-p
V(RX_INP-RX_INN)	Receiver input maximum voltage	Differential mode	-	20	-	V p-p
-	Receiver input bias voltage	-	-	AVDDD_5V_PGA/2	-	V
-	Receiver input impedance	-	-	5.2	-	kΩ
GPGA(PLC)	PLC PGA minimum gain	-	-	-12	-	dB
	PLC PGA maximum gain	-	-	42	-	dB
GPGA(PLC)_Step	PLC PGA gain step	-	-	6	-	dB

Table 27. ADC characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
ADC input range	Differential mode	-	5	-	V p-p
Resolution	-	-	12	-	bit

Zero crossing comparator characteristics

Table 28. Zero crossing characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V(ZC_IN) MAX	Zero crossing Detection input Voltage range	-	-		10	V p-p
V(ZC_IN) TL	Zero crossing Detection input Low threshold	-	-	-6	-	mV
V(ZC_IN) TH	Zero crossing Detection input High threshold	-	-	+6	-	mV
ZC_IN d.c.	Zero crossing Input duty cycle	-	-	50	-	%
ZC_IN delay	Mains zero crossing to detection delay time	-	-	5.8	7.5	µs

4.5 Embedded Flash characteristics

Table 29. Flash memory characteristics

Symbol	Parameter[1]	Conditions	Min.	Typ.[2]	Max.[3]	Max.[4]	Unit
t_{DWPRG}	Double word program	Not including SW overhead	-	18	50	500	µs
t_{MPRG}	Module program (512 kB)	Not including SW overhead	-	1.3	1.65	33	s
t_{BKPRG}	Bank program (1056 KB)	Not including SW overhead	-	2.6	6.6	66	s
t_{ER16K}	Sector pre-program and erase (16 KB)	-	-	0.2	0.5	5.0	s
t_{ER32K}	Sector pre-program and erase (32 KB)	-	-	0.3	0.6	5.0	s
t_{ER64K}	Sector pre-program and erase (64 KB)	-	-	0.4	0.9	5.0	s
t_{ER128K}	Sector pre-program and erase (128 KB)	-	-	0.6	1.3	5.0	s
t_{MKER}	Module erase (512 KB)	-	-	4.8	7.6	55	s
t_{BKER}	Bank erase (1056 KB)	-	-	8	12.6	91	s
t_{PABT}	Program abort latency	-	-	-	10	10	µs
t_{EABT}	Erase abort latency	-	-	-	30	30	µs
t_{ESUS}	Erase suspend latency	-	-	-	30	30	µs
t_{ESRT}	Erase suspend request rate	-	20	-	-	-	ms

1. Based on characterization, not tested in production.
2. Assuming nominal supply values and operation at 25 °C, 0 cycles.
3. Assuming nominal supply values and operation at 25 °C, 100 cycles.
4. Assuming nominal supply values and operation at 125 °C, 100 Kcycles.

Table 30. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min.(1)	Typ.	Max.	Unit
N_{END}	Endurance	TA = -40 to +85 °C	1 K	-	-	Cycles
t_{RET}	Data retention	1 kcycle at TA = +85 °C(2)	15	-	-	Years
		1 kcycles(2) at TA = +55 °C (see(2))	30	-	-	Years

1. Based on characterization, not tested in production.
2. Cycling performed over the whole temperature range.

Table 31. Flash memory current consumption

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I(DVDD_3V3_FLASH)	Current consumption from 3.3 V supply source	Static consumption	-	2.5	3.8	mA
I(DVDD_3V3_FLASH)	Current consumption from 3.3 V supply source	During the erase of all the sectors - see(1)	-	1.6	-	mA
I(DVDD_1V2_FLASH)	Current consumption from 1.2 V supply source	During the erase of all the sectors(1)	-	2.5	-	mA

1. During characterization, not tested in production. The values exclude the consumption from other pins.

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

5.1 TQFP176 package information

Figure 10. TQFP176 (20 x 20 x 1 mm) package outline

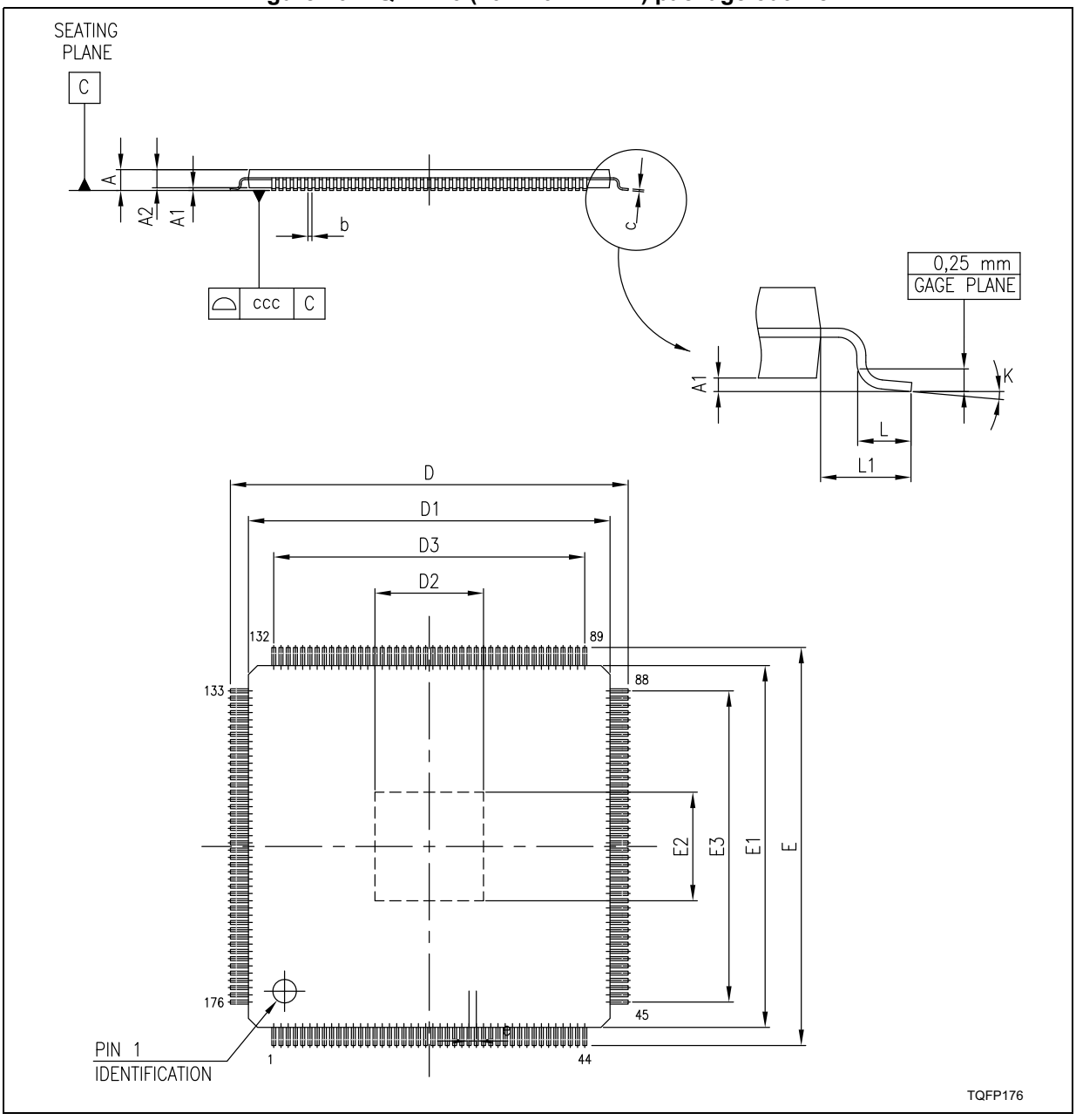


Table 32. TQFP176 (20 x 20 x 1 mm) package mechanical data

Symbol	Dimensions (millimeters)		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.127
A2	0.95	1.00	1.05
b	0.13	0.18	0.23
c	0.09	-	0.20
D	21.80	22.00	22.20
D1	19.80	20.00	20.20
D2	-	8.70	-
D3	-	17.20	-
E	21.80	22.00	22.20
E1	19.80	20.00	20.20
E2	-	8.70	-
E3	-	17.20	-
e	-	0.40	-
L	0.45	0.60	0.75
L1	-	1.00	-
k	0°	3.5°	7°
ccc	-	-	0.08

5.2 Thermal data

Table 33. Thermal data

Symbol	Parameter	Conditions	Typ. value	Unit
R_{thJA}	Maximum thermal resistance junction ambient steady state	Mounted on a 2s2p PCB, with a dissipating surface, connected through vias, on the bottom side of the PCB.	34	°C/W

6 Ordering information

Table 34. Ordering information

Order code	Package	Packing	eFlash size
STCOM10	TQFP176 (20 x 20 x 1 mm)	Tray	1 MB
STCOM05	TQFP176 (20 x 20 x 1 mm)	Tray	640 kB

7 Revision history

Table 35. Document revision history

Date	Revision	Changes
15-Oct-2015	1	Initial release.
19-Dec-2016	2	Updated *Section 1: Description on page 6* (replaced by new Description). Added *Equation 1: on page 27* and *Equation 2: on page 28*. Updated *Section 1.11 on page 28* (replaced “channel 8” by “channel 6”). Updated *Table 12 on page 45*, from *Table 14 on page 47* to *Table 17 on page 47*, *Table 20 on page 48*, from *Table 22 on page 49* to *Table 24 on page 50*, and *Table 25 on page 51* (replaced by new tables). Removed Table Predriver characteristics. Minor modifications throughout document.
11-Sep-2017	3	Updated *Section 1.8 on page 24* (added text). Minor modifications throughout document.