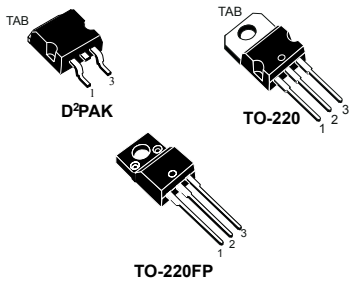
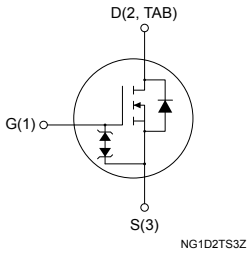
STB9NK50ZT4, STP9NK50Z, STP9NK50ZFP

Datasheet

N-channel 500 V, 700 mΩ typ., 7.2 A SuperMESH Power MOSFET in a D²PAK, TO-220 and TO-220FP packages





Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB9NK50ZT4	500 V	850 mΩ	7.2 A
STP9NK50Z			
STP9NK50ZFP			

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status links
STB9NK50ZT4
STP9NK50Z
STP9NK50ZFP

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D^2PAK TO-220	TO-220FP	
V_{DS}	Drain-source voltage	500		V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	500		V
V_{GS}	Gate-source voltage	±30		V
I_D	Drain current (continuous) at T_C = 25 °C	7.2	7.2(1)	A
	Drain current (continuous) at T_C = 100 °C	4.5	4.5(1)	
I_{DM}(2)	Drain current (pulsed)	28.8	28.8(1)	A
P_{TOT}	Total power dissipation at T_C = 25 °C	110	30	W
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	3.5		kV
dv/dt(3)	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	-	2.5	kV
T_J	Operating junction temperature range	-55 to 150		°C
T_{stg}	Storage temperature range			

1. *Limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 7.2 A, di/dt ≤ 200 A/µs.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		D^2PAK TO-220	TO-220FP	
R_{thJC}	Thermal resistance, junction-to-case	1.14	4.2	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5		°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	7.2	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	190	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	500	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 500 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 500 V, T_C = 125 °C(1)	-	-	50	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 3.6 A	-	700	850	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	910	-	pF
C_{oss}	Output capacitance		-	125	-	pF
C_{rss}	Reverse transfer capacitance		-	30	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{DS} = 0 to 400 V, V_{GS} = 0 V	-	75	-	pF
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 7.2 A, V_{GS} = 0 to 10 V (see the Figure 16. Test circuit for gate charge behavior)	-	32	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain charge		-	18	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 250 V, I_D = 3.6 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	17	-	ns
t_r	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	45	-	ns
t_f	Fall time		-	22	-	ns
$t_{r(Voff)}$	Off-voltage rise time	V_{DD} = 400 V, I_D = 7.2 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	15	-	ns
t_f	Fall time		-	13	-	ns
t_c	Cross-over time		-	30	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	-	-	-	7.2	A
I_{SDM} (1)	Source-drain current (pulsed)		-	-	28.8	A
V_{SD} (2)	Forward on voltage	I_{SD} = 7.2 A, V_{GS} = 0 V	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 7.2 A, di/dt = 100 A/µs, V_{DD} = 40 V, T_J = 150 °C (see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	238	-	ns
Q_{rr}	Reverse recovery charge		-	1.5	-	µC
I_{RRM}	Reverse recovery current		-	12.6	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics curves

Figure 1. Safe operating area for D²PAK and TO-220

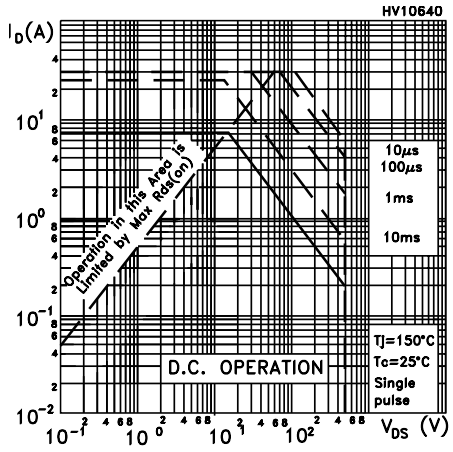


Figure 2. Normalized transient thermal impedance for D²PAK and TO-220

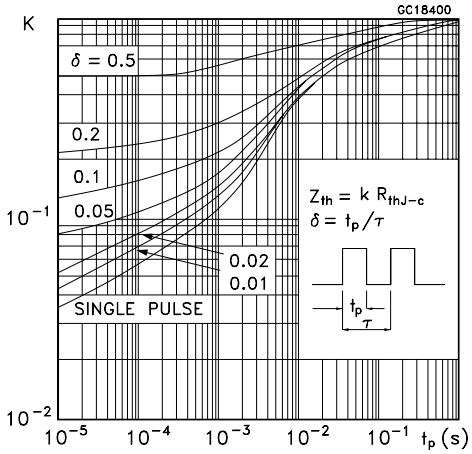


Figure 3. Safe operating area for TO-220FP

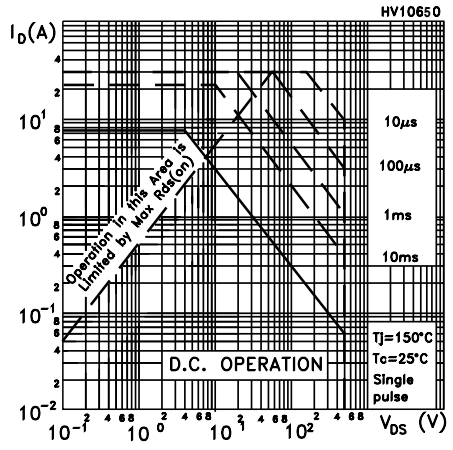


Figure 4. Normalized transient thermal impedance for TO-220FP

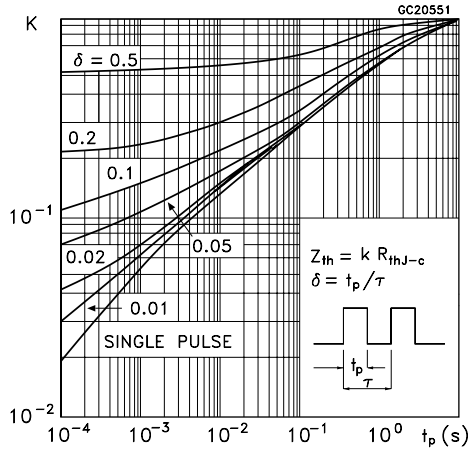


Figure 5. Typical output characterisics

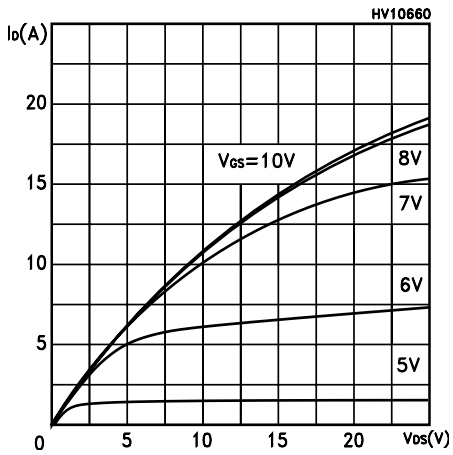


Figure 6. Typical transfer characteristics

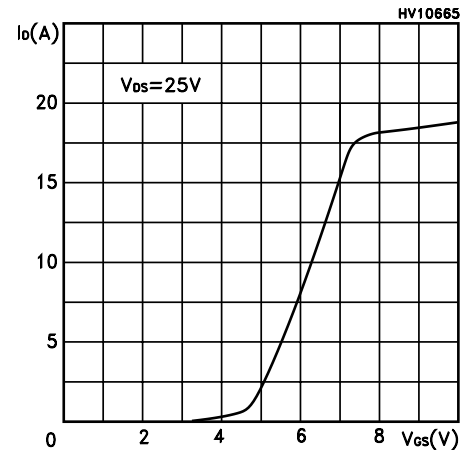


Figure 7. Typical static drain-source on-resistance

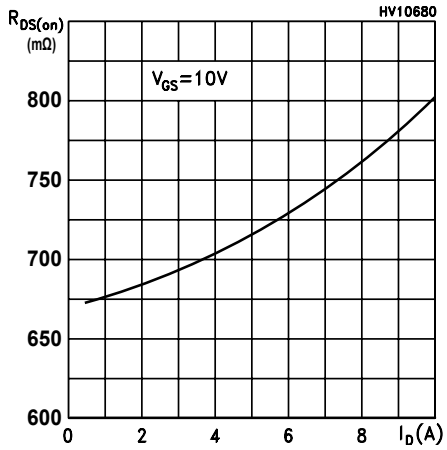


Figure 8. Typical gate charge characteristics

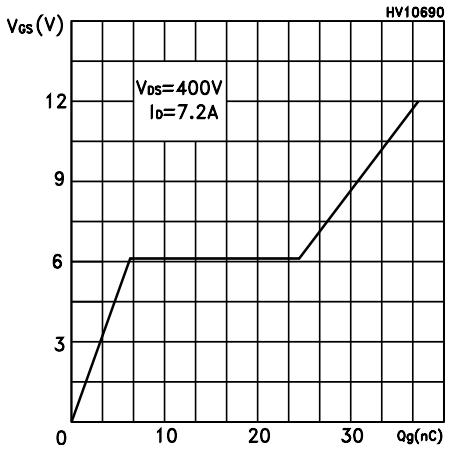


Figure 9. Typical capacitance variations

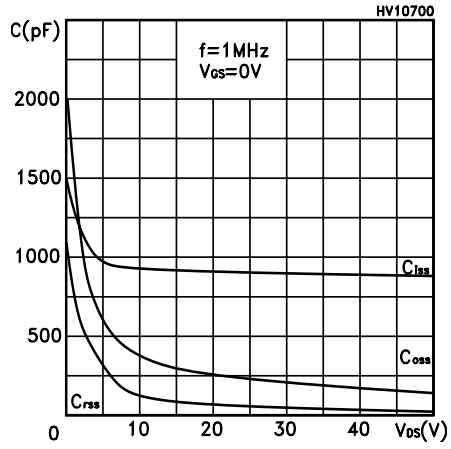


Figure 10. Normalized gate threshold vs temperature

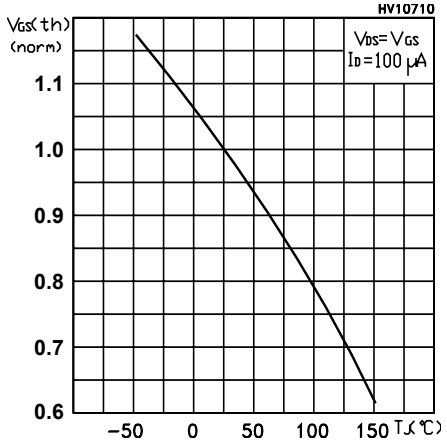


Figure 11. Normalized on-resistance vs temperature

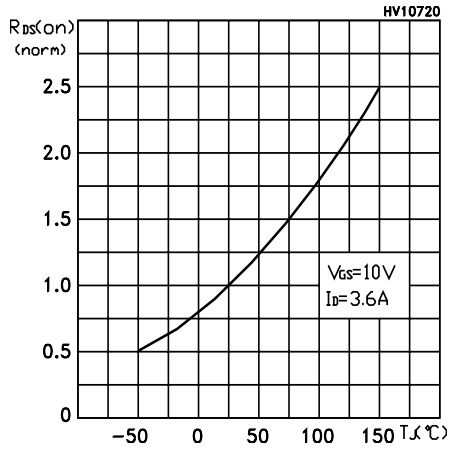


Figure 12. Typical reverse diode forward characteristics

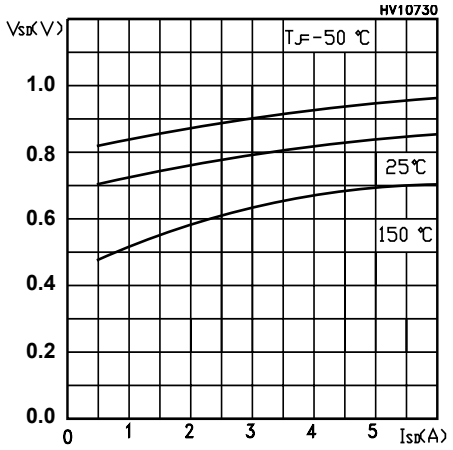


Figure 13. Normalized breakdown voltage vs temperature

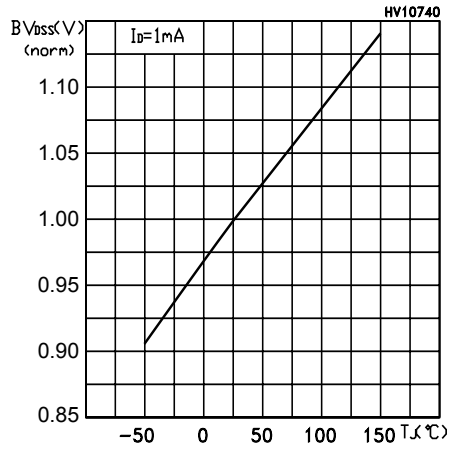
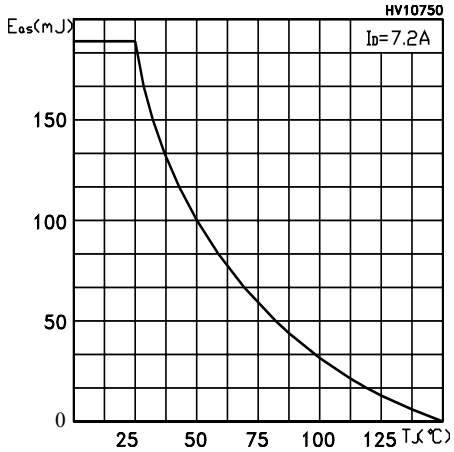


Figure 14. Maximum avalanche energy vs temperature



3 Test circuits

Figure 15. Test circuit for resistive load switching times

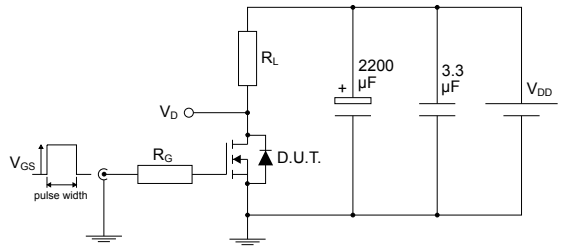


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Figure 16. Test circuit for gate charge behavior

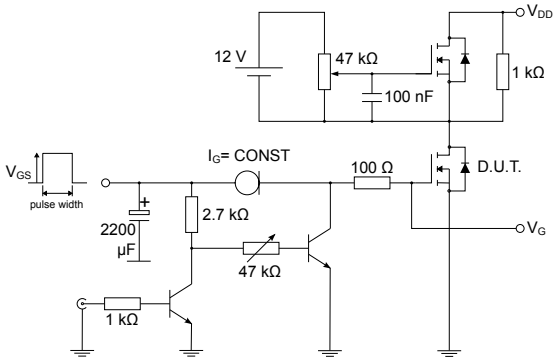

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Figure 17. Test circuit for inductive load switching and diode recovery times

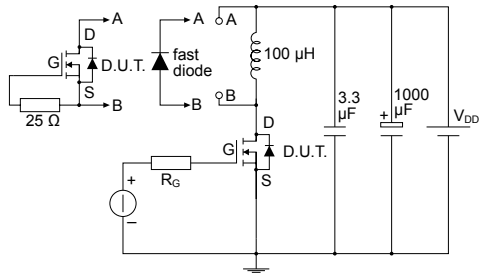

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Figure 18. Unclamped inductive load test circuit

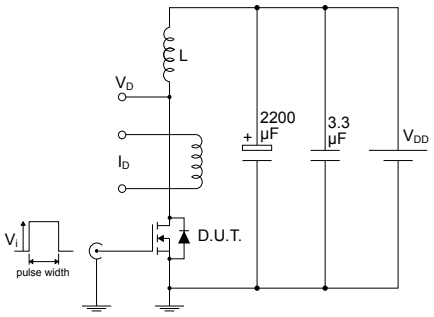

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Figure 19. Unclamped inductive waveform

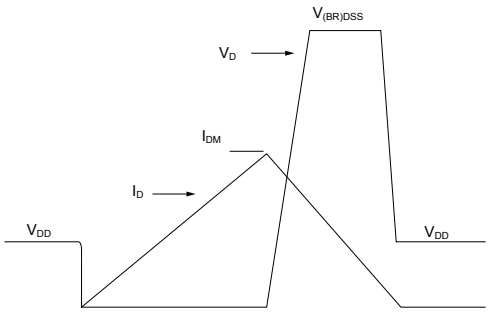

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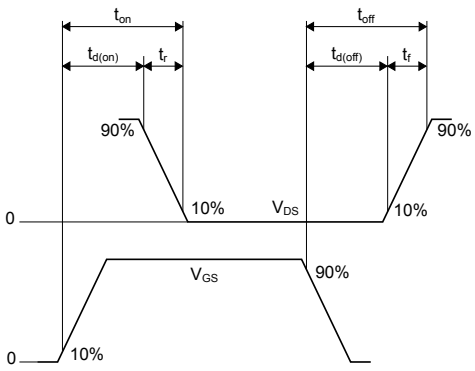
Figure 20. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type B package information

Figure 21. D²PAK (TO-263) type B package outline

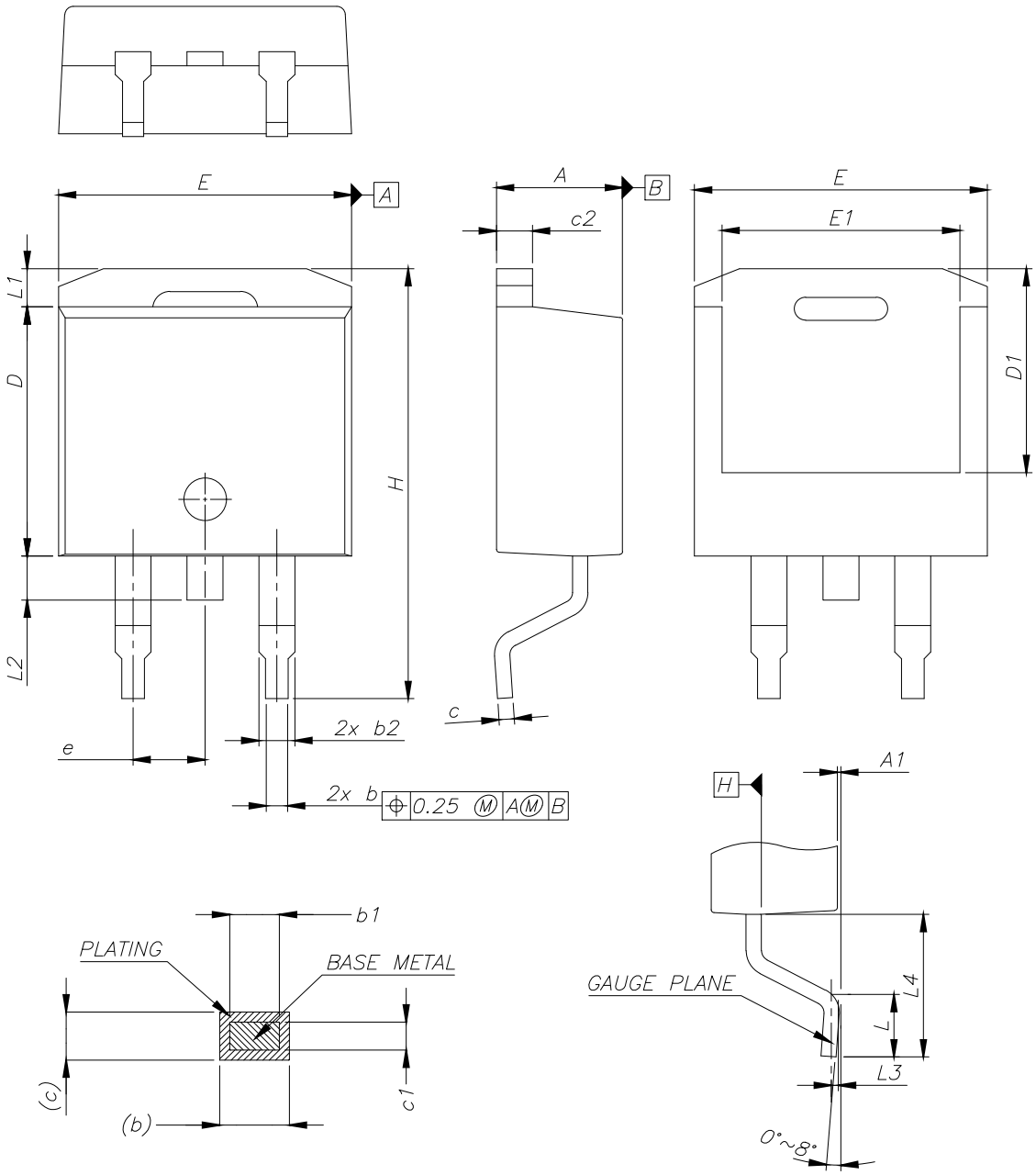

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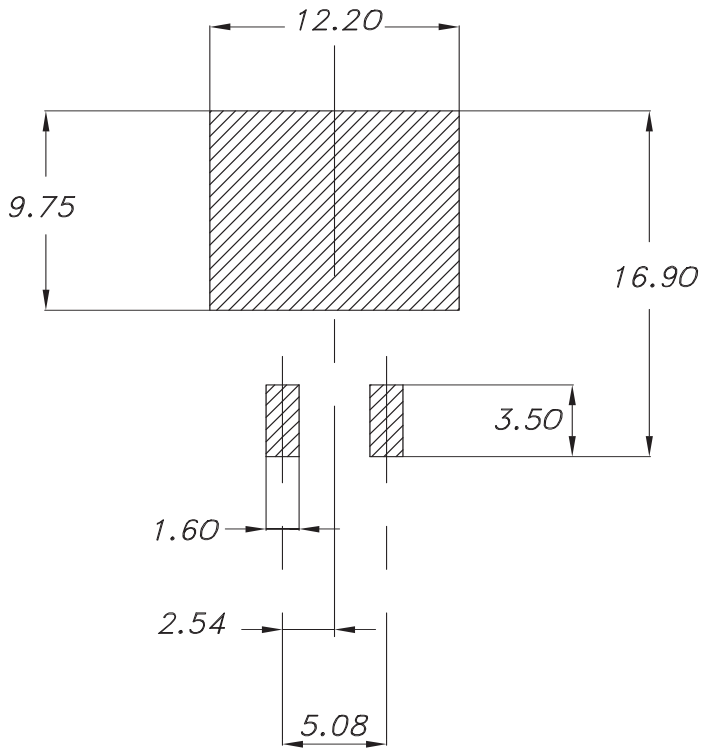
Table 8. D²PAK (TO-263) type B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0.00		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 22. D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 TO-220 type A package information

Figure 23. **TO-220 type A package outline**

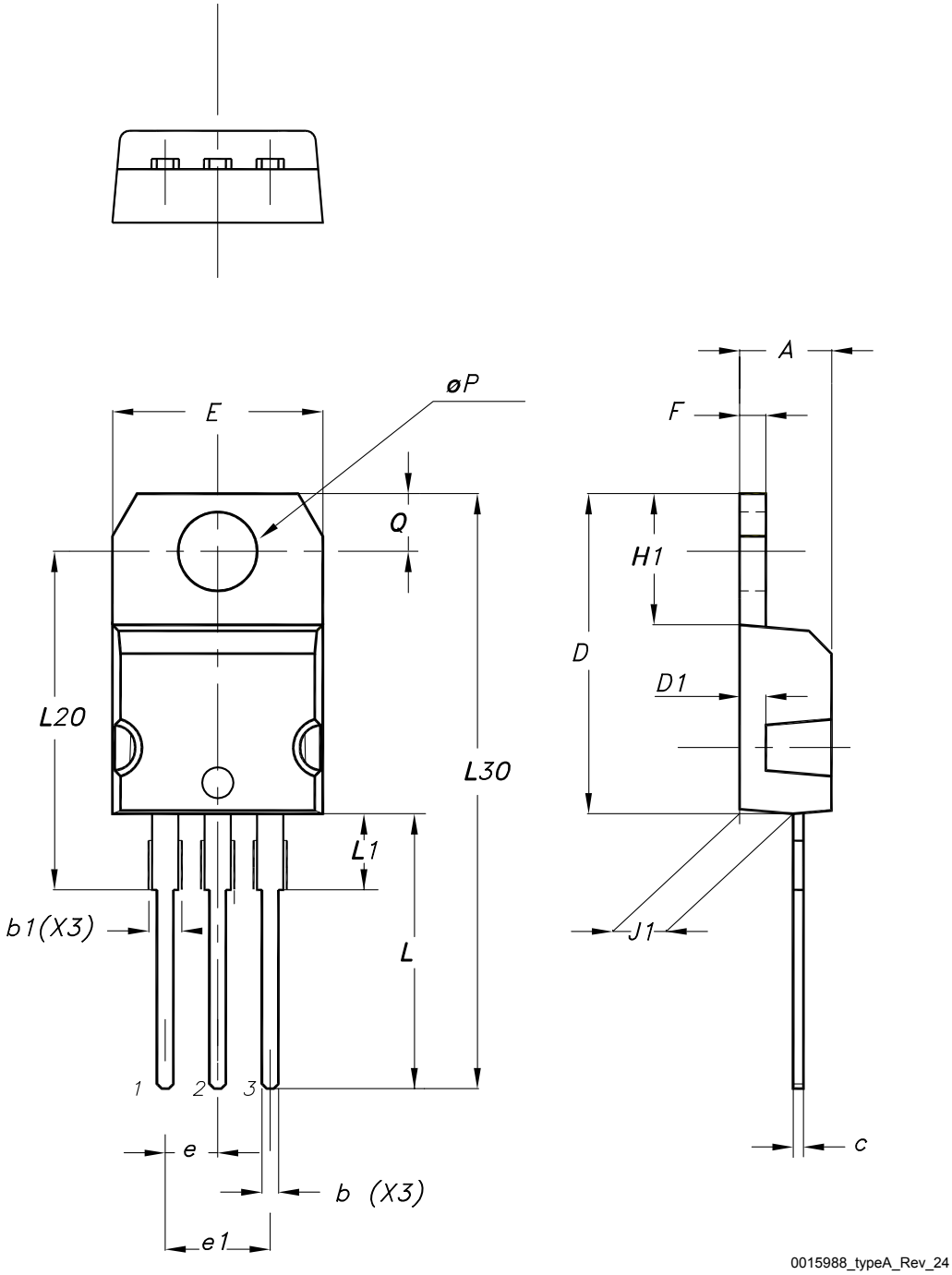


Table 9. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

4.3 TO-220FP type B package information

Figure 24. **TO-220FP type B package outline**

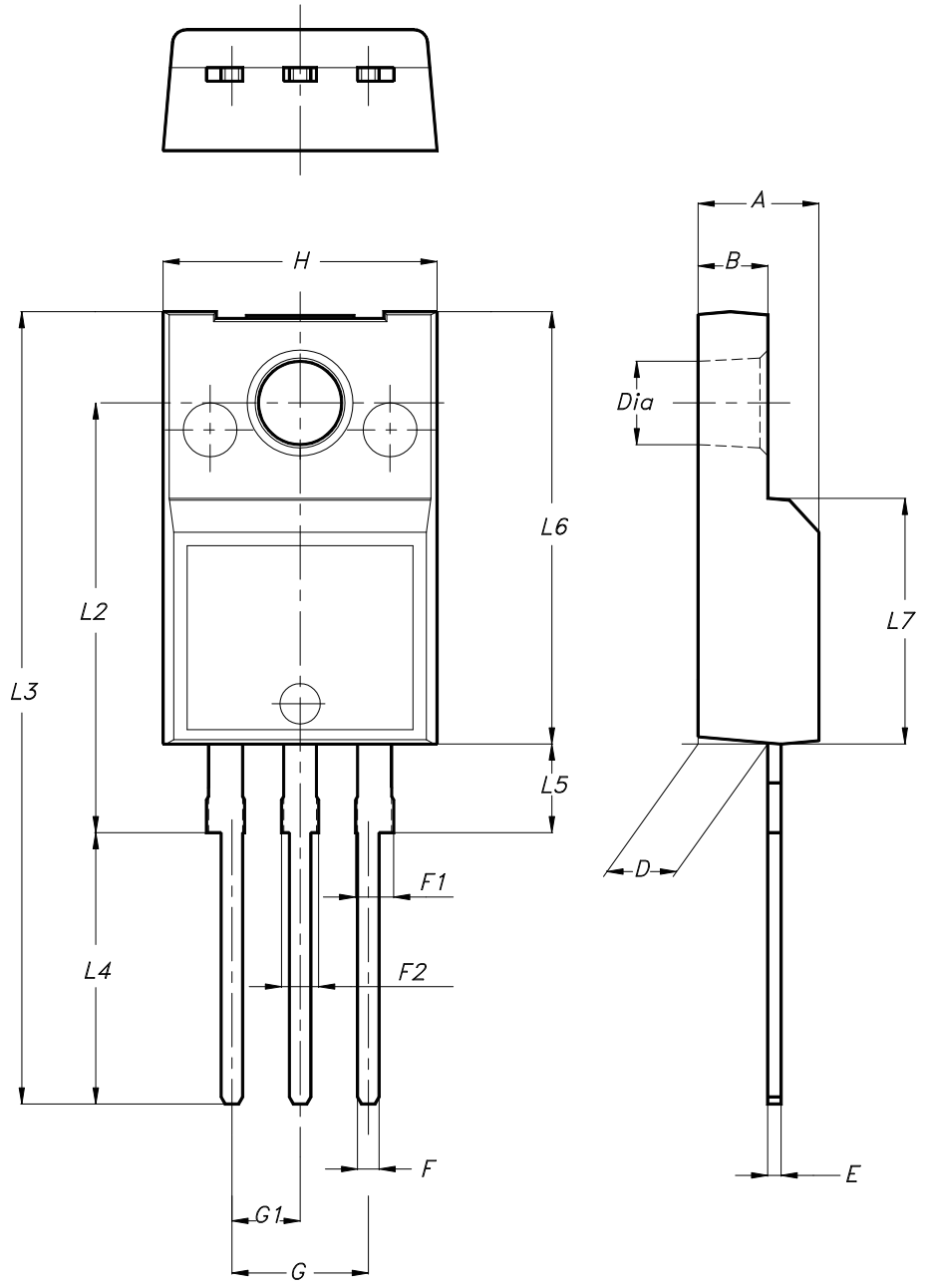
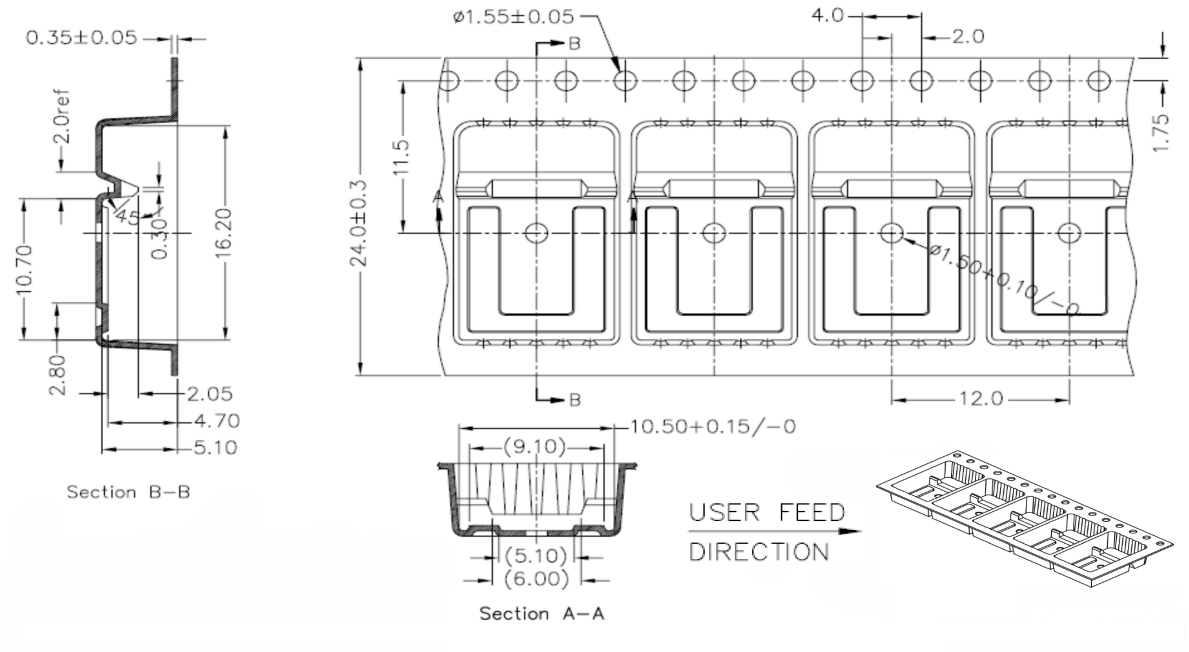


Table 10. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.4 D²PAK packing information

Figure 25. **D²PAK tape drawing (dimensions are in mm)**



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5 Ordering information

Table 11. **Order codes**

Order codes	Marking	Package	Packing
STB9NK50ZT4	B9NK50Z	D²PAK	Tape and reel
STP9NK50Z	P9NK50Z	TO-220	Tube
STP9NK50ZFP	P9NK50ZFP	TO-220FP	

Revision history

Table 12. **Document revision history**

Date	Version	Changes
27-Oct-2025	3	Updated Section 4: Package information. Removed order code STB9NK50Z-1. Minor text changes.

Contents