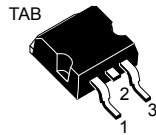
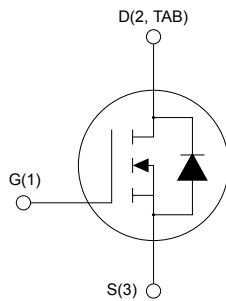


N-channel 600 V, 0.9 Ω typ., 8 A MDmesh Power MOSFET in a D²PAK package


D²PAK


AM01475v1_noZen


Product status link
[STB8NM60T4](#)
Product summary

Order code	STB8NM60T4
Marking	B8NM60
Package	D ² PAK
Packing	Tape and reel

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STB8NM60T4	600 V	1.0 Ω	8 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This N-channel Power MOSFET is developed using STMicroelectronics' revolutionary MDmesh technology, which associates the multiple drain process with the company's PowerMESH horizontal layout. This device offers extremely low on-resistance, high dv/dt, and excellent avalanche characteristics. Using STMicroelectronics's proprietary strip technique, this Power MOSFET boasts an overall dynamic performance that is superior to similar products on the market.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	8	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	5	
$I_{DM}^{(1)}$	Drain current (pulsed)	32	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	100	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		$^{\circ}\text{C}$

1. Pulse width is limited by safe operating area.

2. $I_{SD} \leq 8\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	1.25	$^{\circ}\text{C}/\text{W}$
$R_{thJA}^{(1)}$	Thermal resistance, junction-to-ambient	35	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	2.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	200	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			10	
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.5\text{ A}$		0.9	1.0	Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	400	-	pF
C_{oss}	Output capacitance		-	100	-	pF
C_{rss}	Reverse transfer capacitance		-	10	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }480\text{ V}$	-	50	-	pF
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 5\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 12. Test circuit for gate charge behavior)	-	13	-	nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain charge		-	6	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 2.5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	14	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 11. Test circuit for resistive load switching times and Figure 16. Switching time waveform)	-	23	-	ns
t_f	Fall time		-	10	-	ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD} = 480\text{ V}$, $I_D = 5\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	7	-	ns
t_f	Fall time		-	10	-	ns
t_c	Cross-over time	(see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	17	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$ (see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	300		ns
Q_{rr}	Reverse recovery charge		-	1.95		μC
I_{RRM}	Reverse recovery current		-	13		A
t_{rr}	Reverse recovery time	$I_{SD} = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 13. Test circuit for inductive load switching and diode recovery times)	-	445		ns
Q_{rr}	Reverse recovery charge		-	3		μC
I_{RRM}	Reverse recovery current		-	13.5		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

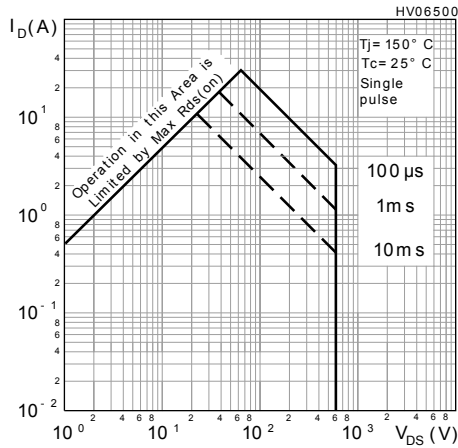
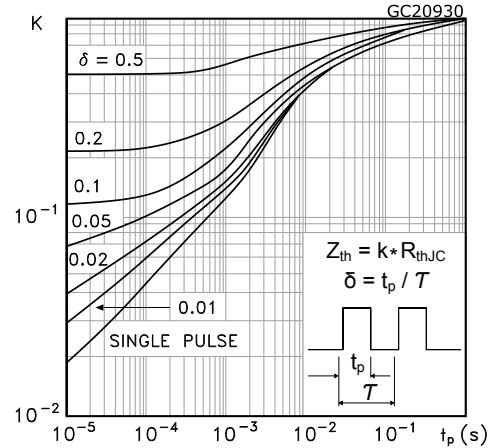
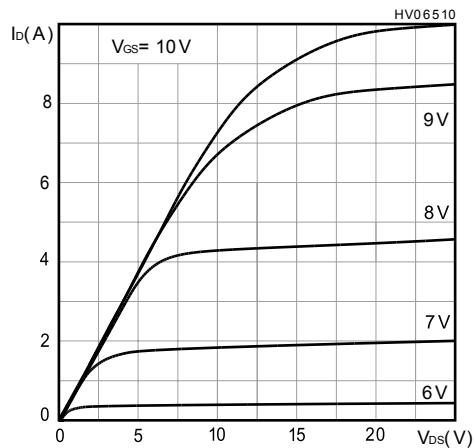
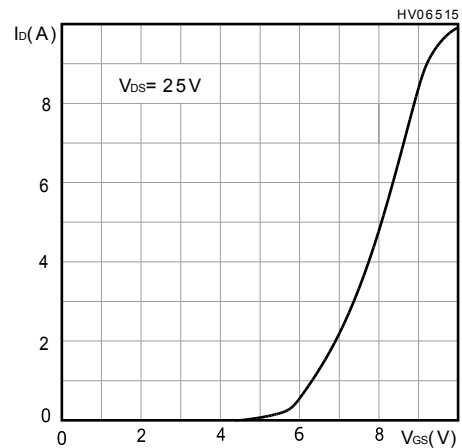
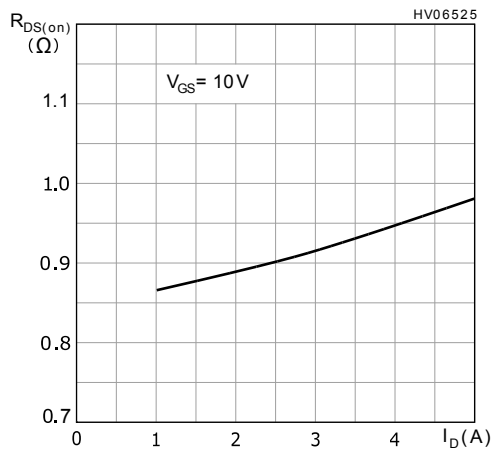
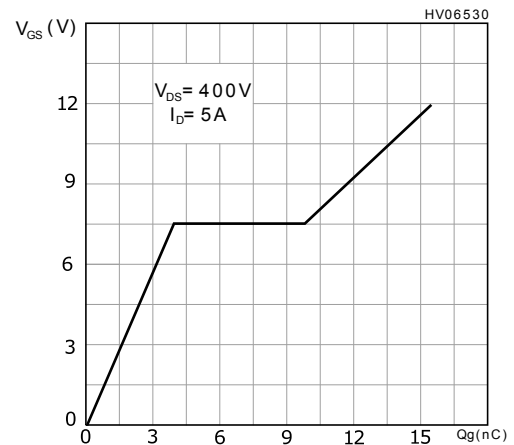
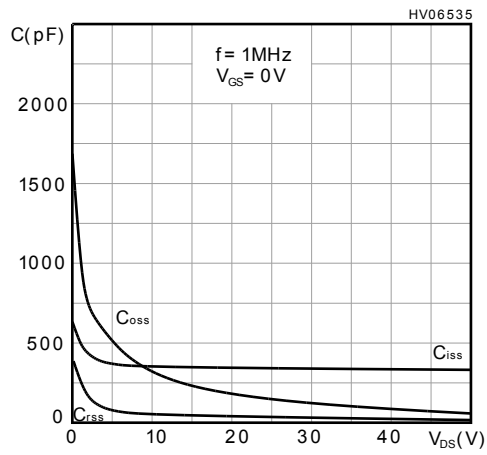
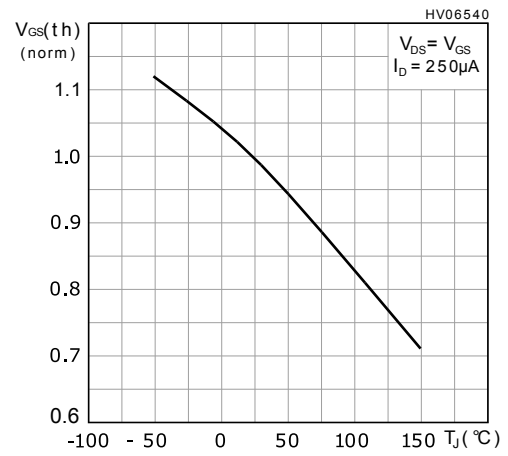
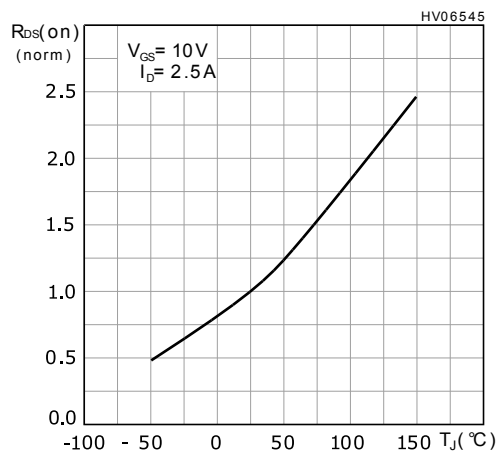
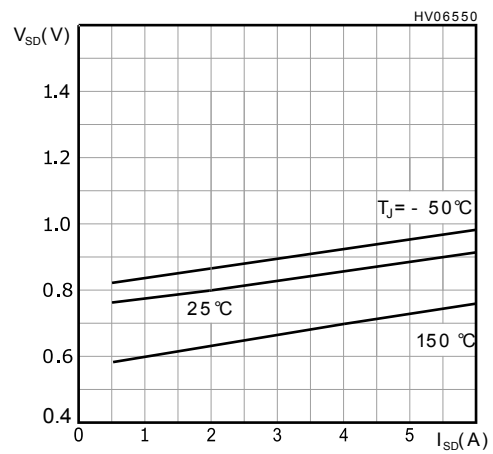
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Static drain-source on-resistance

Figure 6. Gate charge vs gate-source voltage


Figure 7. Capacitance variations

Figure 8. Normalized gate threshold voltage vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Source-drain diode forward characteristics


3 Test circuits

Figure 11. Test circuit for resistive load switching times


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Figure 12. Test circuit for gate charge behavior

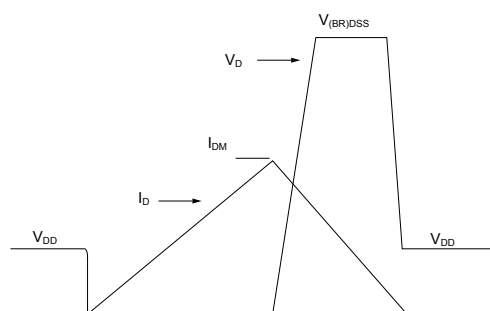

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Figure 13. Test circuit for inductive load switching and diode recovery times


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Figure 14. Unclamped inductive load test circuit


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Figure 15. Unclamped inductive waveform


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Figure 16. Switching time waveform

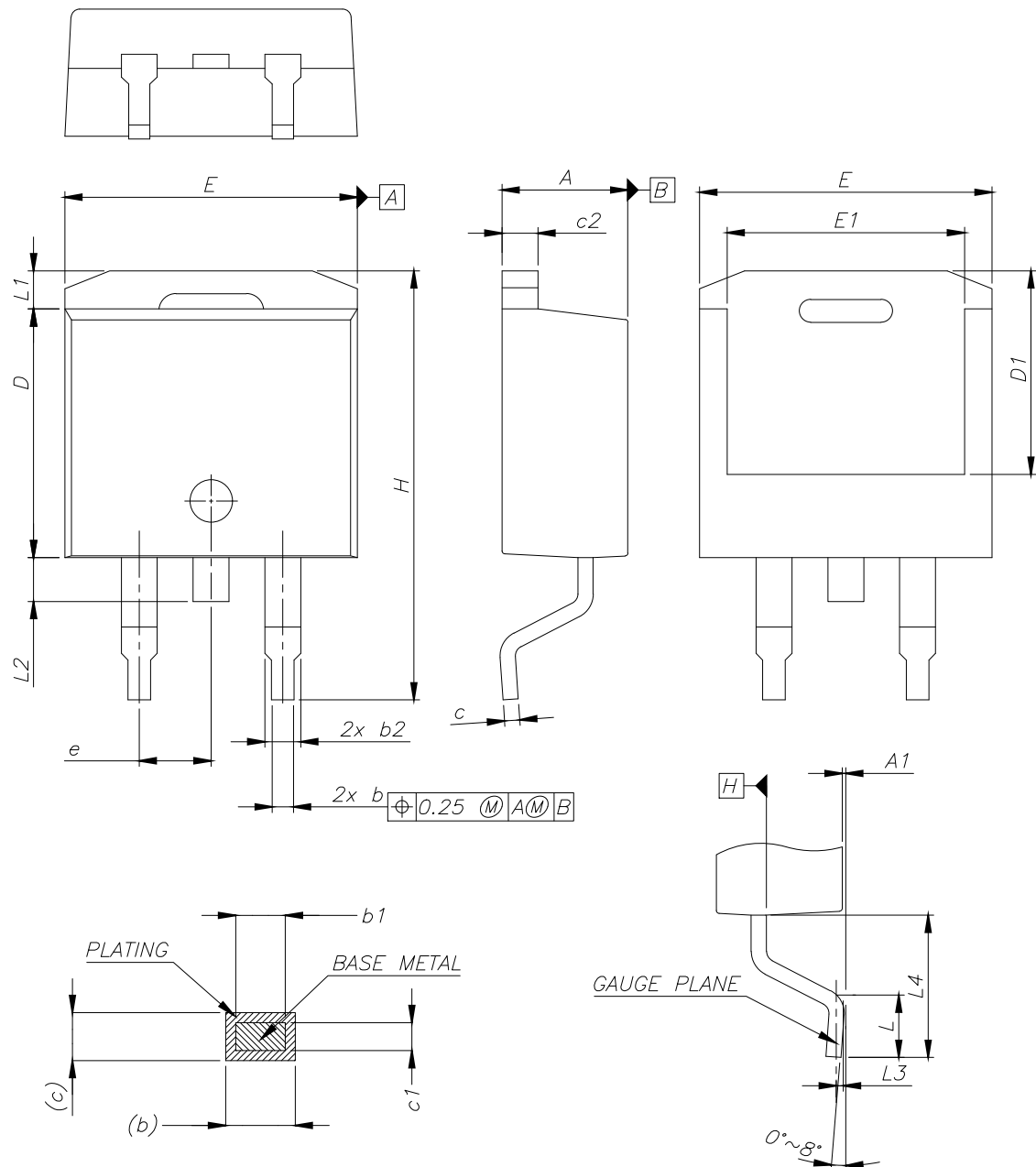

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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type B package information

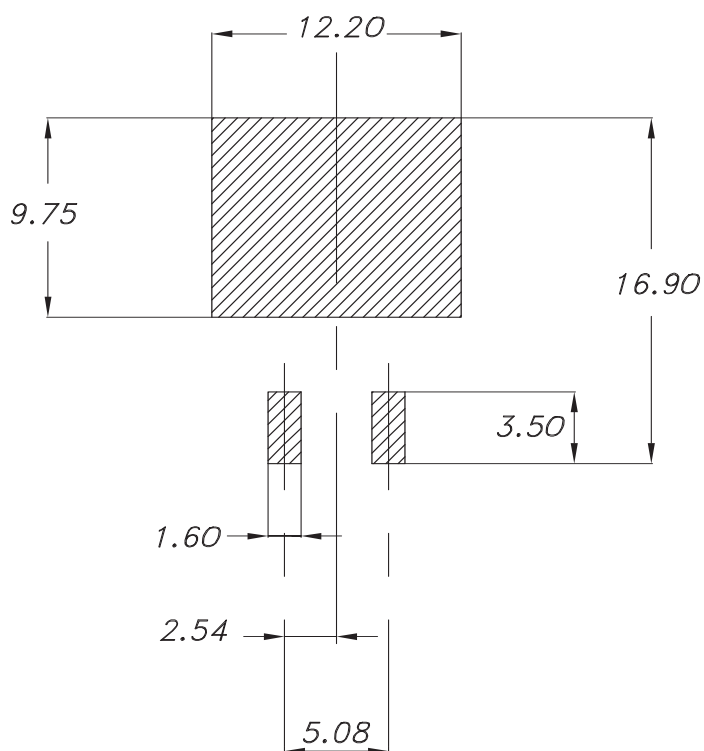
Figure 17. D²PAK (TO-263) type B package outline



0079457_27_B

Table 8. D²PAK (TO-263) type B mechanical data

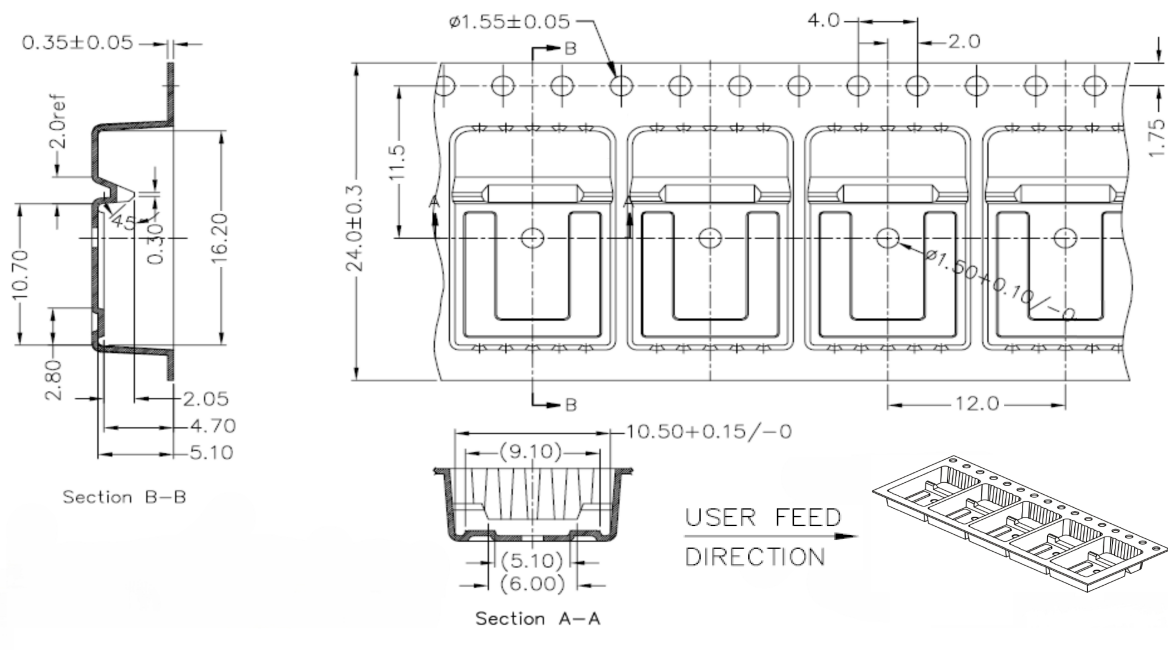
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	Min.	Typ.	Max.
A	4.36		4.56
A1	0.00		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

Figure 18. D²PAK (TO-263) recommended footprint (dimensions are in mm)


0079457_Rev27_footprint

4.2

Figure 19. D²PAK tape drawing (dimensions are in mm)



DM01095771 2

Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Jun-2023	1	First release. The part number STB8NM60T4 was previously inserted in the DS1949.
18-Aug-2025	2	Updated Section 4: Package information .

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