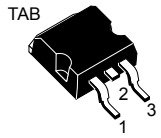
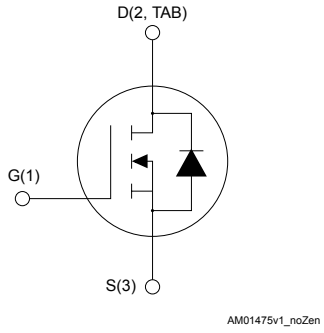
Automotive-grade N-channel 650 V, 58 mΩ typ., 42 A MDmesh M5 Power MOSFET in a D²PAK package



D²PAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STB43N65M5	650 V	63 mΩ	42 A

- AEC-Q101 qualified
- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

Product status link
STB43N65M5

Product summary	
Order code	STB43N65M5
Marking	43N65M5
Package	D²PAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	42	A
	Drain current (continuous) at T_C = 100 °C	26.5	
I_{DM}(1)	Drain current (pulsed)	168	A
P_{TOT}	Total power dissipation at T_C = 25 °C	250	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 42 A, di/dt=150 A/µs; V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.*
3. *V_{DS} ≤ 520 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.5	°C/W
R_{thJA}(1)	Thermal resistance, junction-to-ambient	30	

1. *When mounted on a standard 1 inch^2 area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	7	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	650	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C(1)	-	-	100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V	-	-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 21 A	-	58	63	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	4400	-	pF
C_{oss}	Output capacitance		-	100	-	pF
C_{rss}	Reverse transfer capacitance		-	5.3	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 520 V, V_{GS} = 0 V	-	300	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	1.2	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 21 A, V_{GS} = 0 to 10 V (see the Figure 15. Test circuit for gate charge behavior)	-	100	-	nC
Q_{gs}	Gate-source charge		-	23	-	nC
Q_{gd}	Gate-drain charge		-	40	-	nC

1. *$C_{oss\ eq.}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 28 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	73	-	ns
$t_{r(v)}$	Voltage rise time		-	15	-	ns
$t_{f(i)}$	Current fall time		-	12	-	ns
$t_{c(off)}$	Crossing time		-	19	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	42	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	168	A
V_{SD}(2)	Forward on voltage	I_{SD} = 42 A, V_{GS} = 0 V	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 42 A, di/dt = 100 A/µs,	-	420	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V	-	8	-	µC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	40	-	A
t_{rr}	Reverse recovery time	I_{SD} = 42 A, di/dt = 100 A/µs,	-	530	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, T_J = 150 °C	-	12	-	µC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	44	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

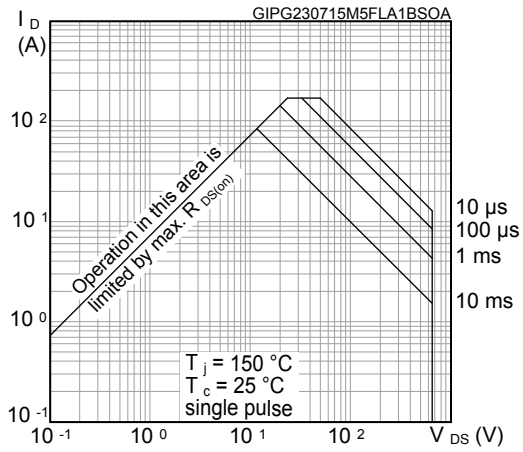


Figure 2. Thermal impedance

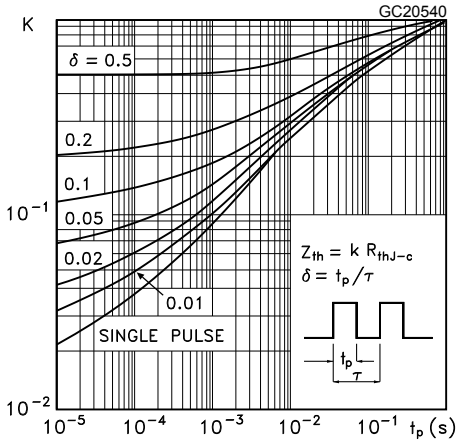


Figure 3. Output characteristics

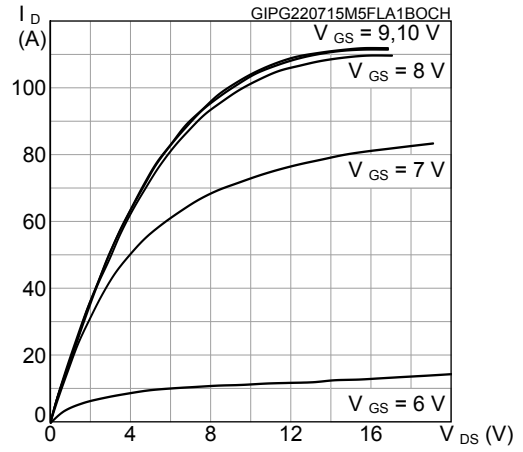


Figure 4. Transfer characteristics

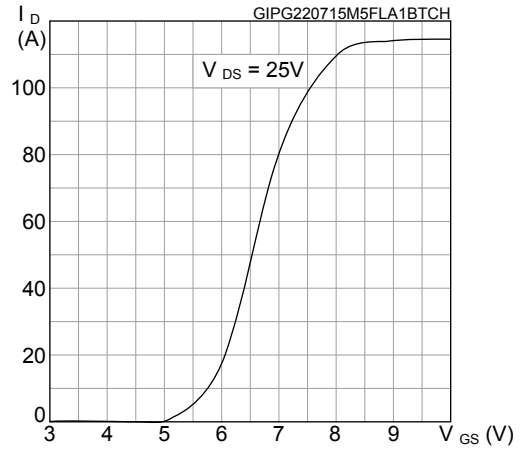


Figure 5. Gate charge vs gate-source voltage

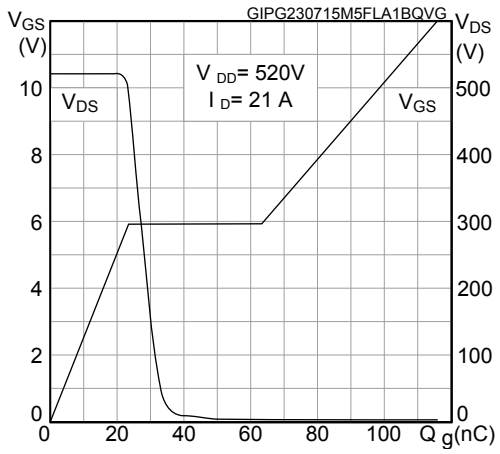


Figure 6. Static drain-source on-resistance

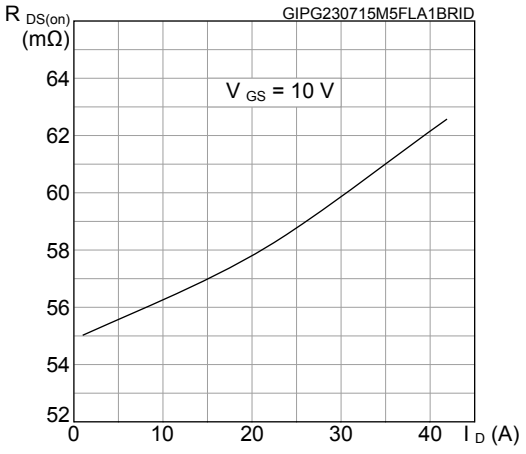


Figure 7. Capacitance variations

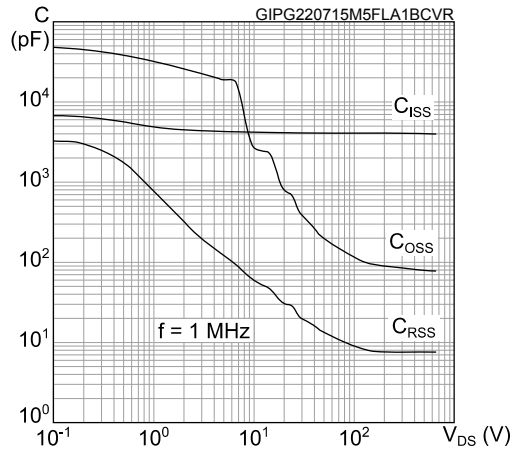


Figure 8. Normalized gate threshold voltage vs temperature

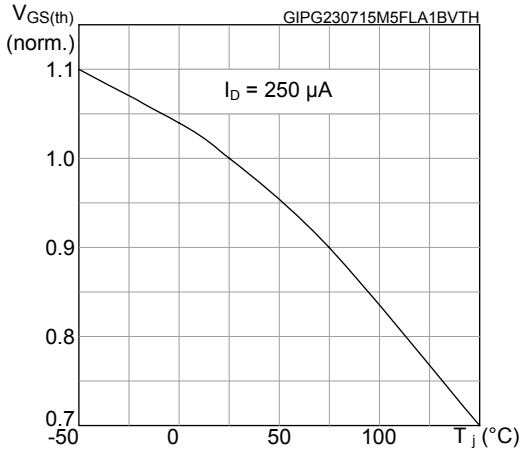


Figure 9. Normalized on-resistance vs temperature

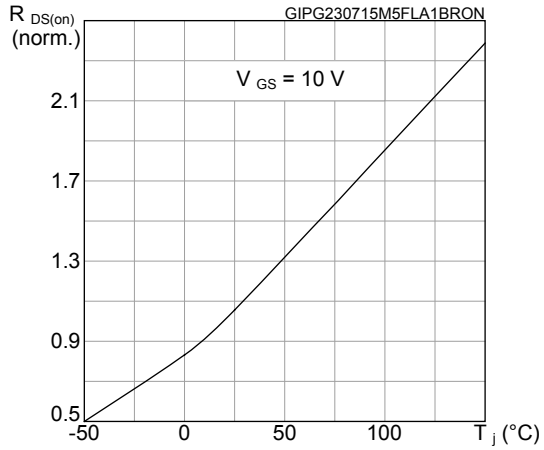


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

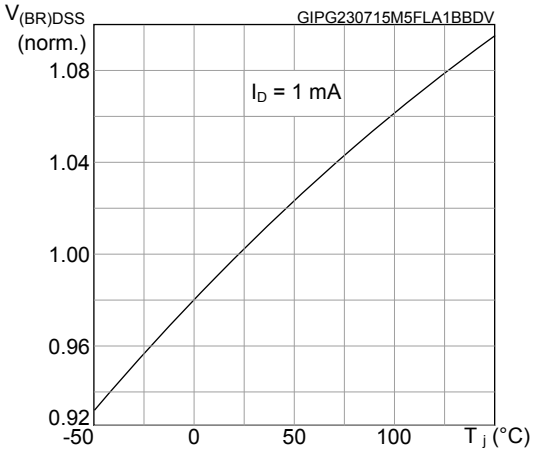


Figure 11. Output capacitance stored energy

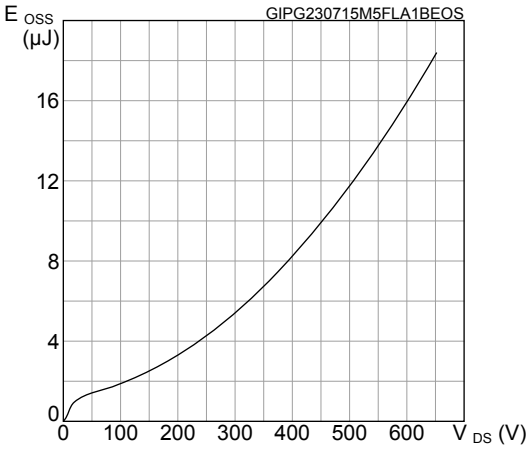


Figure 12. Source- drain diode forward characteristics

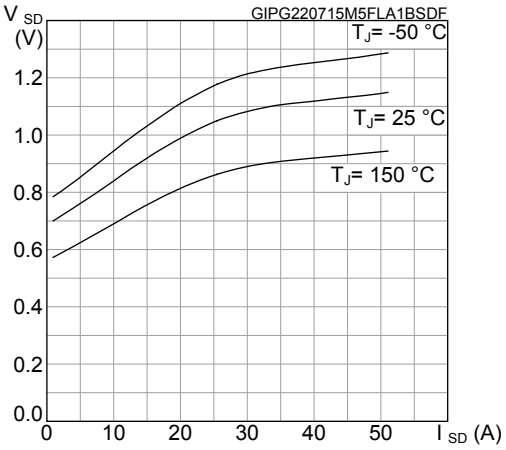
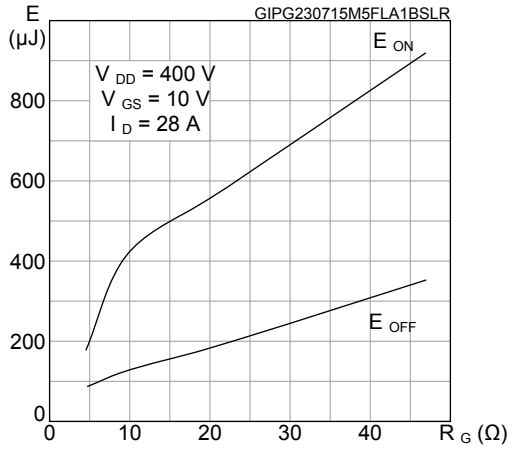


Figure 13. Switching energy vs gate resistance



Note: E_{on} including reverse recovery of a SiC diode.

3 Test circuits

Figure 14. Test circuit for resistive load switching times

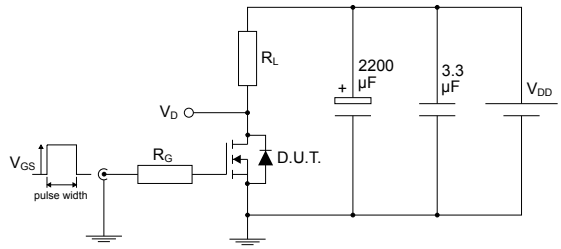


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Figure 15. Test circuit for gate charge behavior

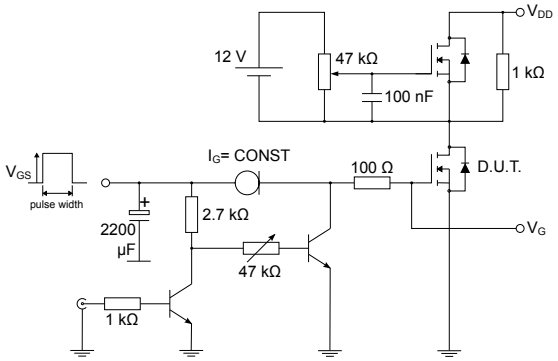

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Figure 16. Test circuit for inductive load switching and diode recovery times

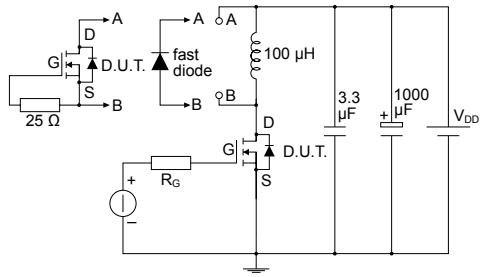

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Figure 17. Unclamped inductive load test circuit

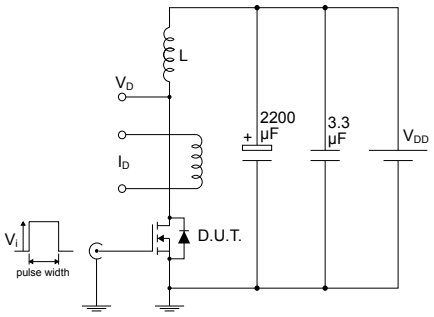

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Figure 18. Unclamped inductive waveform

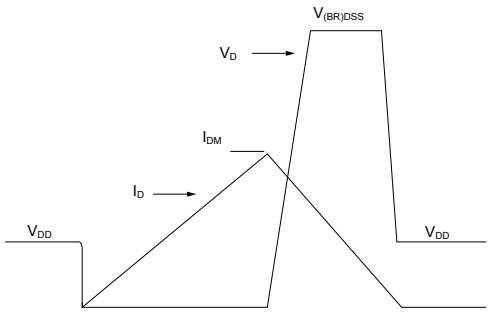

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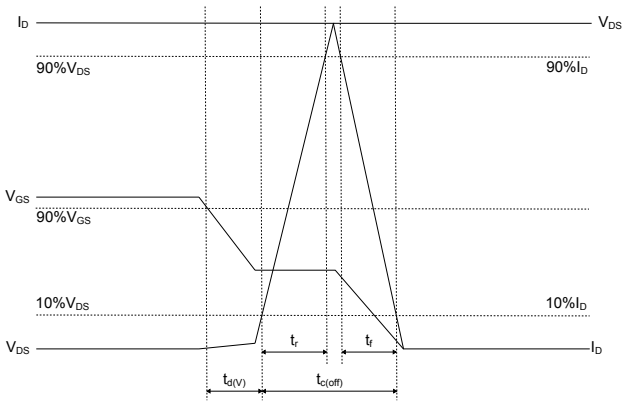
Figure 19. Switching time waveform



AM05540v2

4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 20. **D²PAK (TO-263) type A2 package outline**

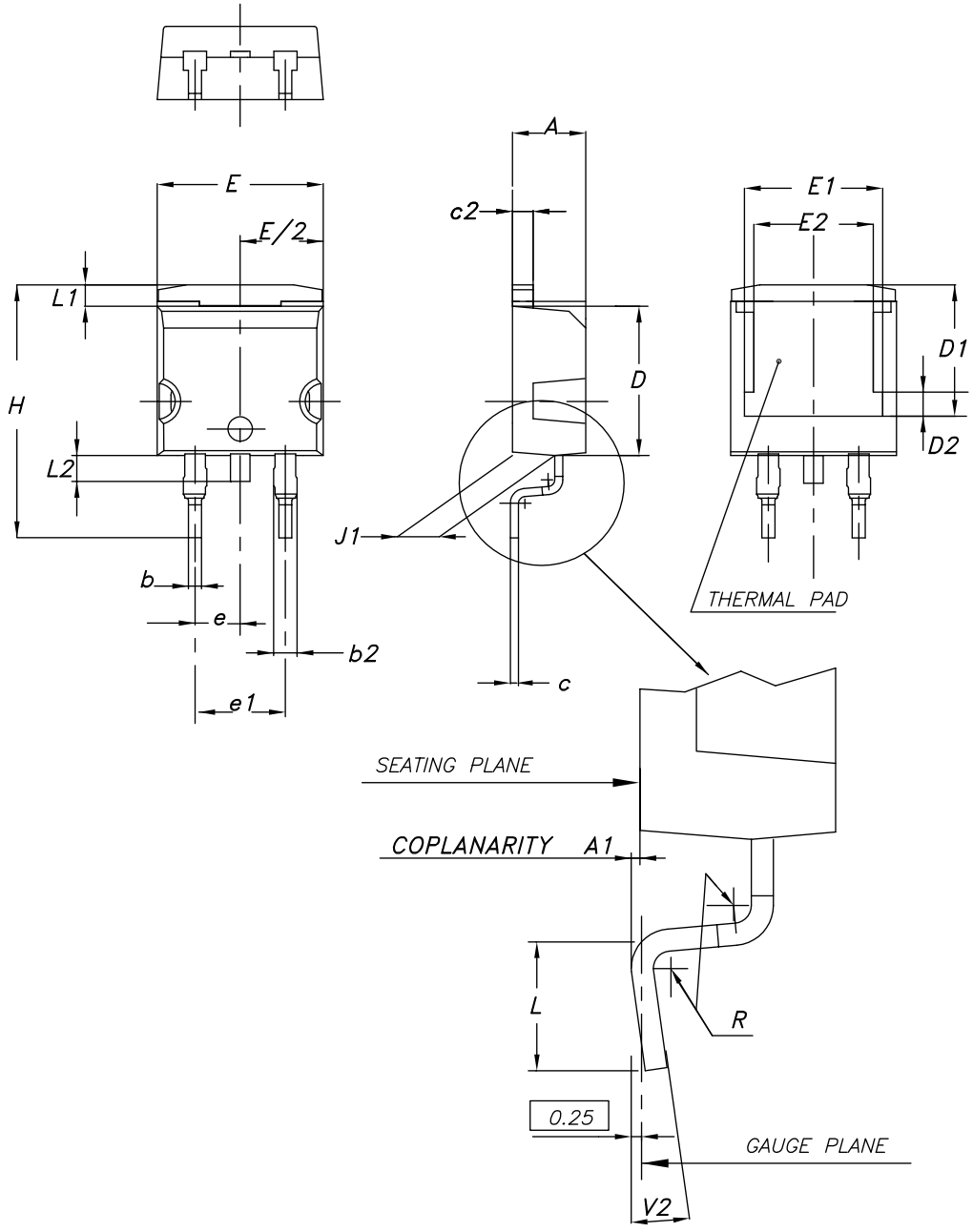


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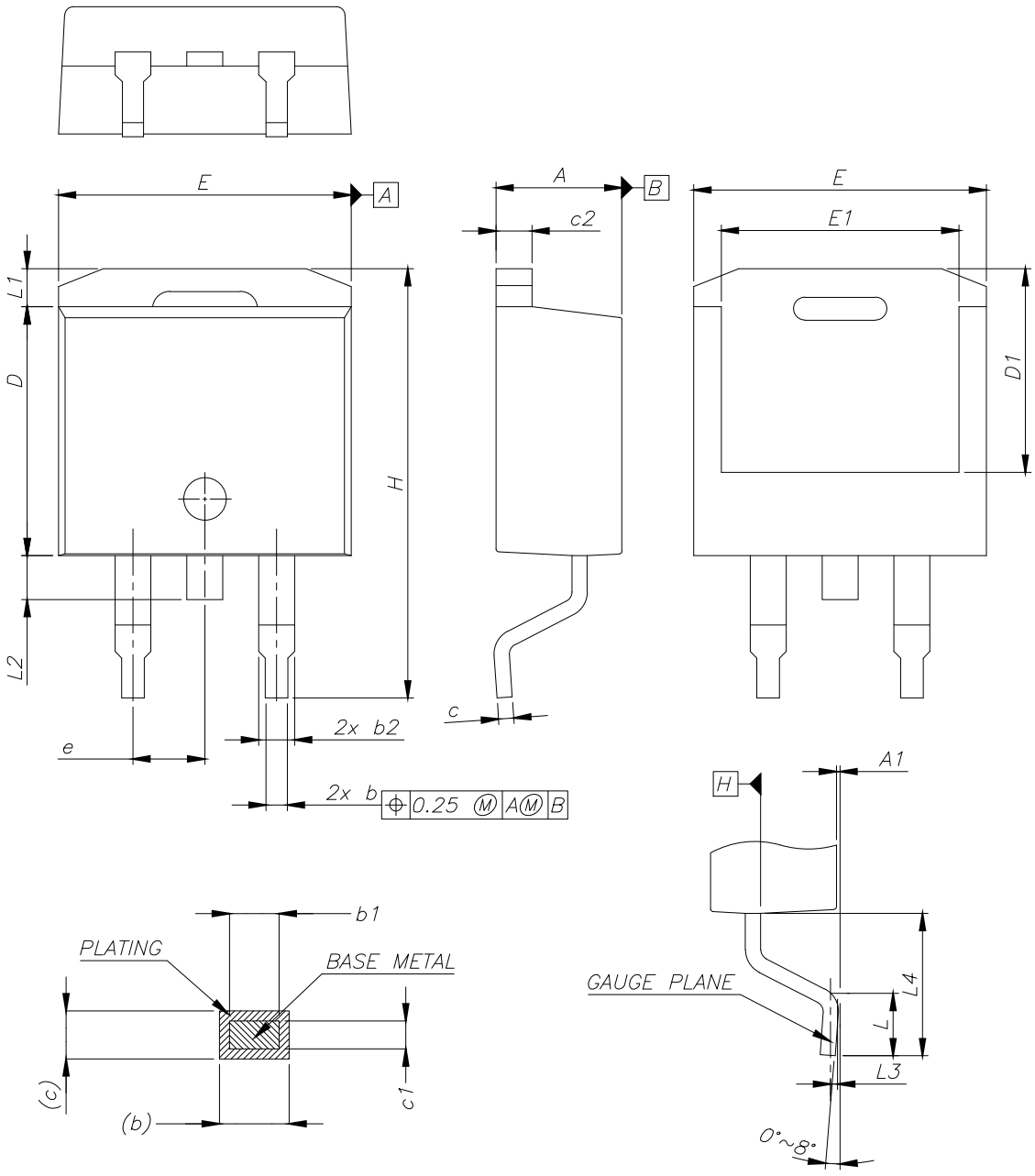
Table 8. D²PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

4.2 D²PAK (TO-263) type B package information

Figure 21. D²PAK (TO-263) type B package outline

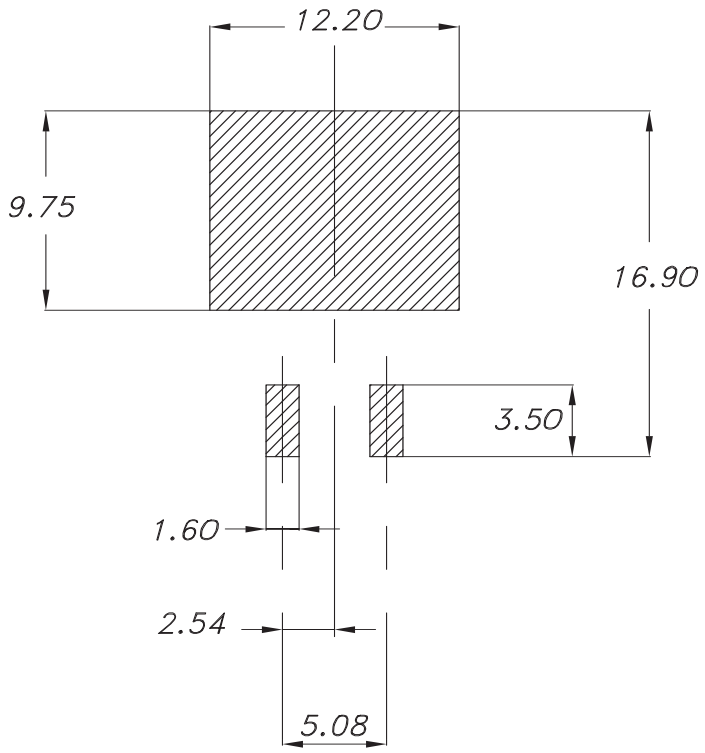


0079457_27_B

Table 9. D²PAK (TO-263) type B mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.36		4.56
A1	0.00		0.25
b	0.70		0.90
b1	0.51		0.89
b2	1.17		1.37
c	0.38		0.694
c1	0.38		0.534
c2	1.19		1.34
D	8.60		9.00
D1	6.90		7.50
E	10.15		10.55
E1	8.10		8.70
e	2.54 BSC		
H	15.00		15.60
L	1.90		2.50
L1			1.65
L2			1.78
L3		0.25	
L4	4.78		5.28

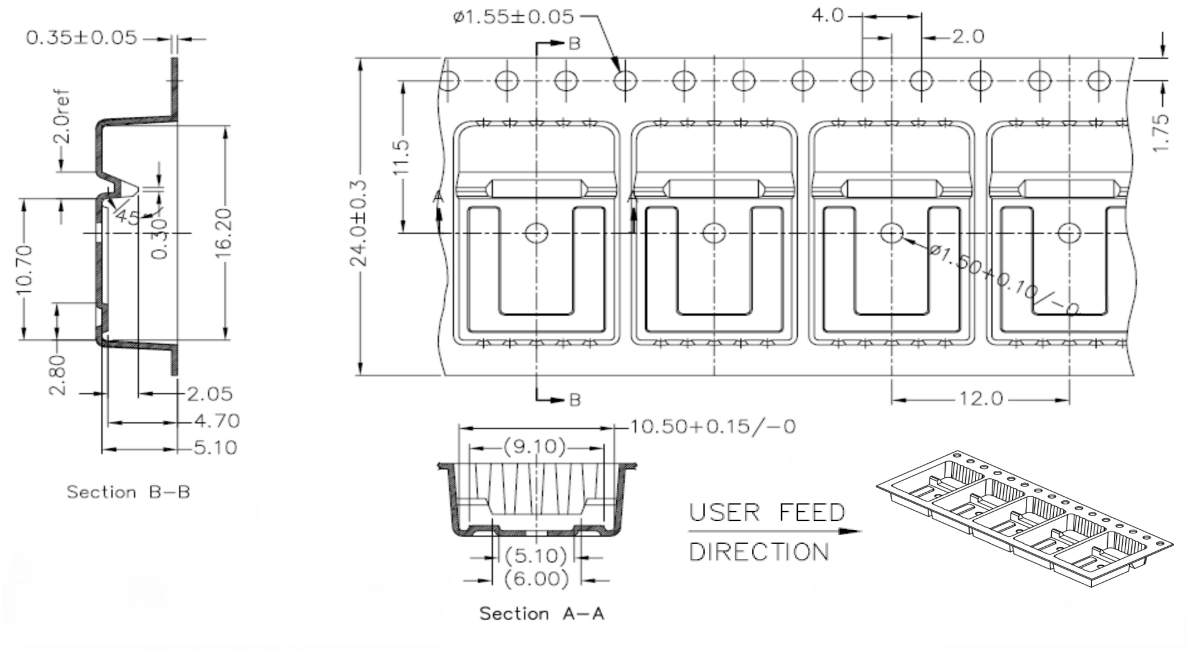
Figure 22. D²PAK (TO-263) recommended footprint (dimensions are in mm)



0079457_Rev27_footprint

4.3 D²PAK packing information

Figure 23. **D²PAK tape drawing (dimensions are in mm)**



Revision history

Table 10. **Document revision history**

Date	Revision	Changes
23-Jul-2015	1	Initial release.
13-Nov-2018	2	Updated features in cover page. Updated *Section 3 Test circuits* and *Section 4.1 D²PAK (TO-263) type A2 package information*. Minor text changes.
19-Aug-2025	3	Updated Section 4: Package information. Minor text changes.

Contents

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